UNIVERSIDADE FEDERAL DO RIO GRANDE DO SUL
INSTITUTO DE INFORMÁTICA
PROGRAMA DE PÓS-GRADUAÇÃO EM COMPUTAÇÃO

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Low Cost BIST Techniques for Linear and Non-Linear Analog Circuits

Thesis presented in partial fulfillment of the requirements for the degree of Doctor of Computer Science

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Porto Alegre, July 2005.

CIP – CATALOGAÇÃO NA PUBLICAÇÃO

Negreiros, Marcelo

Low Cost BIST Techniques for Linear and Non-Linear Analog Circuits / Marcelo Negreiros – Porto Alegre: Programa de Pós-Graduação em Computação, 2005.

15 f.:il.

Thesis (Ph.D.) – Universidade Federal do Rio Grande do Sul. Programa de Pós-Graduação em Computação. Porto Alegre, BR – RS, 2005. Advisor: Luigi Carro; Co-advisor: Altamiro Amadeu Susin.

1.Analog and Mixed Signal Testing. 2.Testing of Embedded Analog Cores 3. Analog BIST. I. Carro, Luigi. II. Susin, Altamiro Amadeu. III. Título.

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ACKNOWLEDGMENTS

After four years, this thesis is finally finished. The author received a special honor (*voto de louvor,* the first one from the PPGC for years!) after authoring (or actively co-authoring) 22 conference papers and 7 journal publications related to the work described here. I would like to share this honor with all people that contributed to this work.

I would like to acknowledge the financial support from the CNPq - *Conselho Nacional de Desenvolvimento Científico e Tecnológico* (National Council for Scientific and Technological Development), which provided scholarship for the development of this thesis. I would also acknowledge the support from the *PPGC - Programa de Pós Graduação em Computação da UFRGS* (Post Graduation Course in Computer Science at UFRGS) and from the *Instituto de Informática da UFRGS*, which supported the development of this work and provided the necessary infrastructure, including auxiliary financial support. The support from the GME - Microelectronics Group at UFRGS was also important during this thesis. Most of this work was developed in the *LaPSI - Laboratório de Processamento de Sinais e Imagens* at the Electrical Engineering Department at UFRGS, which provided equipment resources and a pleasant environment. I would like thank other institutions that helped the development of this work by providing free samples of some of their products: Analog Devices, Texas Instruments, Epcos AG and Rogers Corporation. I would also like to mention the Merrian-Webster Online Dictionary, a very helpful tool.

I am in debt to many people that supported the development of this work. I would like to express my gratitude to prof. Cláudio Fernandez for being always helpful regarding the diverse problems faced during the development of the RF test methodolog, and to prof. Eric Fabris for some helpful discussions regarding noise figure measurements. I would also like to thank the colleagues at the laboratory for providing a nice place to work, even under "deadline circumstances", and for helping the development of this work both directly and indirectly: Osvaldo, Letícia, Adão, Borin, Erik Schüler, Nívea and Álisson. A special thanks is due to Maria da Glória for easing the task of co-authoring her papers. I would also like to thank Josias, Socal, Thiago Figueiró, Bonatto and Davi Poyastro regarding the management of the lab servers and workstations. I should also apologize for not mentioning other people here that, because of limited space and lack of author's memory, were not mentioned.

A special thanks is due to my advisor prof. Luigi for his valuable suggestions, determination and help in the development of this work. I would also like to thank my co-advisor prof. Susin for the usual support and suggestions at "critical" times.

Finally, I should also thank my family for providing support during the development of this thesis, even at moments when you become a very unpleasant person...

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LIST OF ABBREVIATIONS AND ACRONYMS

ATE	Automatic Test Equipment
AD	Analog to Digital
ADC	Analog to Digital Converter
ANG	Analog Noise Generator
BIST	Built-In Self Test
BILBO	Built In Logic Block Observer
CUT	Circuit under test
DA	Digital to Analog
DAC	Digital to Analog Converter
DUT	Device under Test
DFT	Design for Test
FFT	Fast Fourier Transform
FPGA	Field Programmable Gate Array
IP	Intellectual Property
ITRS	International Technology Roadmap for Semiconductors
LFSR	Linear Feedback Shift Register
MISR	Multiple Input Signature Register
P1500 SECT	P1500 Standard for Embedded Core Test
PSD	Power Spectrum Density
RF	Radio Frequency
SoC	System On a Chip
SNR	Signal to Noise Ratio
TAM	Test Access Mechanism
TAP	Test Access Port

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ABSTRACT

With the ever increasing demands for high complexity consumer electronic products, market pressures demand faster product development and lower cost. SoC-based design can provide the required design flexibility and speed by allowing the use of IP cores. However, testing costs in the SoC environment can reach a substantial percent of the total production cost. Analog testing costs may dominate the total test cost, as testing of analog circuits usually require functional verification of the circuit and special testing procedures. For RF analog circuits commonly used in wireless applications, testing is further complicated because of the high frequencies involved. In summary, reducing analog test cost is of major importance in the electronic industry today.

BIST techniques for analog circuits, though potentially able to solve the analog test cost problem, have some limitations. Some techniques are circuit dependent, requiring reconfiguration of the circuit being tested, and are generally not usable in RF circuits. In the SoC environment, as processing and memory resources are available, they could be used in the test. However, the overhead for adding additional AD and DA converters may be too costly for most systems, and analog routing of signals may not be feasible and may introduce signal distortion.

In this work a simple and low cost digitizer is used instead of an ADC in order to enable analog testing strategies to be implemented in a SoC environment. Thanks to the low analog area overhead of the converter, multiple analog test points can be observed and specific analog test strategies can be enabled. As the digitizer is always connected to the analog test point, it is not necessary to include muxes and switches that would degrade the signal path. For RF analog circuits, this is specially useful, as the circuit impedance is fixed and the influence of the digitizer can be accounted for in the design phase. Thanks to the simplicity of the converter, it is able to reach higher frequencies, and enables the implementation of low cost RF test strategies.

The digitizer has been applied successfully in the testing of both low frequency and RF analog circuits. Also, as testing is based on frequency-domain characteristics, non-linear characteristics like intermodulation products can also be evaluated. Specifically, practical results were obtained for prototyped base band filters and a 100MHz mixer. The application of the converter for noise figure evaluation was also addressed, and experimental results for low frequency amplifiers using conventional opamps were obtained. The proposed method is able to enhance the testability of current mixed-signal designs, being suitable for the SoC environment used in many industrial products nowadays.

Keywords: Analog testing, Analog BIST, RF test, low cost analog test.

Técnicas de Teste Embarcado de Baixo Custo para Circuitos Analógicos Lineares e Não-Lineares

RESUMO

Com a crescente demanda por produtos eletrônicos de consumo de alta complexidade, o mercado necessita de um rápido ciclo de desenvolvimento de produto com baixo custo. O projeto de equipamentos eletrônicos baseado no uso de núcleos de propriedade intelectual ("IP cores") proporciona flexibilidade e velocidade de desenvolvimento dos chamados "sistemas num chip". Entretanto, os custos do teste destes sistemas podem alcançar um percentual significativo do valor total de produção, principalmente no caso de sistemas contendo "IP cores" analógicos ou "mixed-signal".

Técnicas de teste embarcado (BIST e DFT) para circuitos analógicos, embora potencialmente capazes de minimizar o problema, apresentam limitações que restringem seu emprego a casos específicos. Algumas técnicas são dependentes do circuito, necessitando reconfiguração do circuito sob teste, e não são, em geral, utilizáveis em RF. No ambiente de "sistemas num chip", como recursos de processamento e memória estão disponíveis, eles poderiam ser utilizados durante o teste. No entanto, a sobrecarga de adicionar conversores AD e DA pode ser muito onerosa para a maior parte dos sistemas, e o roteamento analógico dos sinais pode não ser possível, além de poder introduzir distorção do sinal.

Neste trabalho um digitalizador simples e de baixo custo é usado ao invés de um conversor AD para possibilitar a implementação de estratégias de teste no ambiente de "sistemas num chip". Graças ao baixo acréscimo de área analógica do conversor, múltiplos pontos de teste podem ser usados. Graças ao desempenho do conversor, é possível observar características dos sinais analógicos presentes nos "IP cores", incluindo a faixa de freqüências de RF usada em transceptores para comunicações sem fio. O digitalizador foi utilizado com sucesso no teste de circuitos analógicos de baixa freqüência e de RF. Como o teste é baseado no domínio freqüência, características não-lineares como produtos de intermodulação podem também ser avaliadas. Especificamente, resultados práticos com protótipos foram obtidos para filtros de banda base e para um mixer a 100MHz. A aplicação do conversor para avaliação da figura de ruído também foi abordada, e resultados experimentais utilizando amplificadores operacionais convencionais foram obtidos para freqüências na faixa de áudio.

O método proposto é capaz de melhorar a testabilidade de projetos que utilizam circuitos de sinais mistos, sendo adequado ao uso no ambiente de "sistemas num chip" usado em muitos produtos atualmente.

Palavras-Chave: BIST Analógico, Teste RF, Teste Analógico de Baixo Custo.

1 INTRODUCTION

Nowadays, complex and portable consumer electronics products are in widespread use, being present in different circuits like cellular phones, portable digital assistants, notebooks, audio and video players, digital cameras and others. These and other devices emerged because of the great development in microelectronics and integration capacity. As fabrication processes became more advanced, more transistors fit in the same die area. This enables the integration of a large number of system components onto a single chip, increasing circuit complexity, as shown in Figure 1.1.

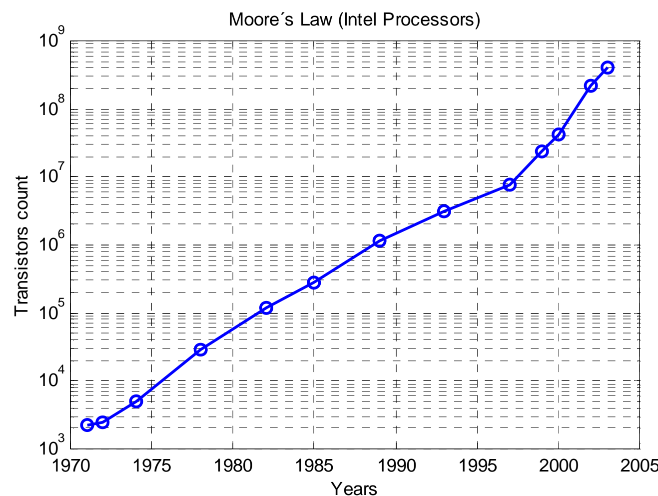


Figure 1.1: Moore's Law and integrated circuit complexity (INTEL, 2005).

The design of these electronic systems has several challenges. There are a large number of components to deal with, and the inclusion of a new product function requires additional modules. There is a broad diversity of characteristics of each integrated component (digital, analog, high-speed serial interfaces working at Gb/s, RF and microwave circuits), as each additional module is targeted to a specific function. Finally, there is limited external access to a specific component because of the limited number of pins in the package. These constraints are continuously increased by market pressures demanding new products with added features, which results in pressures for shorter design time and product life-cycle.

One approach adopted to reduce development time and effort is the core-based or IP (Intellectual Property) design (ZORIAN; MARINISSEN, 2000). It is based on third-party proprietary designs of specific blocks needed by the system. This allows fast development and reuse of components, reducing the work load to introduce new functionality on a new design. On the other hand, the designer may have only limited access to the core functions, or they may not be accessible at all. This is due to the

nature of the cores, that can be soft (register-transfer level), firm (netlist) and hard (technology dependent layout) (ZORIAN; MARINISSEN, 2000).

As the design of electronic systems evolves from ASICs and multi-module to Systems-on-Chip (SoCs), the challenges faced by system designers are related to integration of all components and the system test.

The project development of a core based system is shown in Figure 1.2. The core developer should provide mechanisms for the test of the core. This is needed because the system integrator needs to be able to perform the test of the core after manufacturing, in addition to the test of the entire system. Due to these characteristics, the test of a core may involve the work of several teams (from core provider and core user) and exchange of test data information. In addition, the system designer will need to provide mechanisms to allow the test of the SoC (called Test Access Mechanisms - TAM). These mechanisms for test should be carefully designed to optimize test quality, area, performance, power and cost.

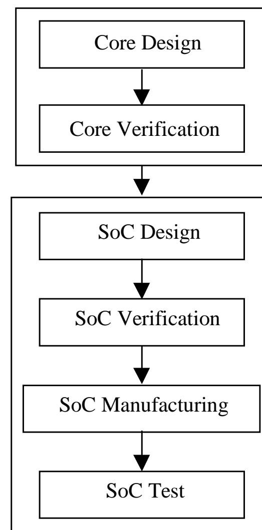


Figure 1.2: SoC project development sequence (ZORIAN; MARINISSEN, 2000).

A generic test structure consisting of three elements is illustrated in Figure 1.3. The elements are: a test source to provide stimulus generation and a test sink to evaluate the responses, a test path between the source/sink and the CUT (Circuit Under Test) - the TAM, and a thin shell around the core that connects the TAM(s) to the core, the wrapper.

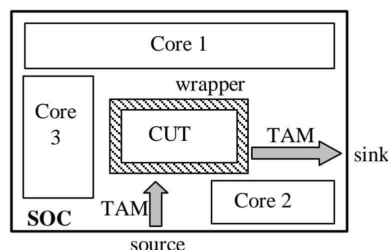


Figure 1.3: Generic test architecture (ZORIAN; MARINISSEN, 2000).

The IEEE 1500 (IEEE, 2005; MARINISSEN, 2002) standard deals with this structure only regarding the test wrapper and its interface to the TAM(s). The knowledge of the test is specified through a Core Test Language (CTL), which is also standardized by the same standard. Current version of the standard covers digital logic

and memory cores, but future versions are planned to cover analog and mixed-signal cores (ZORIAN; MARINISSEN, 2000; MARINISSEN, 2002).

Although the IEEE 1500 standard mechanism eases the task of reaching the core, the test itself is specific to the core, and must be previously designed, during the core development phase. Also, from the manufacturer point of view, different tests are needed during design phase and production phase. From the application point of view, applications involving life-support and control require periodic tests during the normal operation of the equipment, called on-line tests, to ensure correct operation. These facts make it difficult to establish general test methodologies that would allow the test of all classes of circuits under all circumstances.

Test strategies have been developed first for digital circuits, like boundary-scan and BIST, and are well consolidated (ABRAMOVICI, 1990; IEEE, 1990). For analog and mixed-signal circuits, on the other hand, existing solutions are circuit-specific and can not be generally applied (MILOR, 1998; ROBERTS, 96). Mixed-signal and analog test are distinctive from digital test also because of the nature of the test. While for digital circuits structural tests based on fault models are common, there is no similar approach for analog circuits.

Structural test (MILOR, 1998; ROBERTS, 96) is based on physical information of the manufactured device, so the applied test patterns can be optimally chosen and fault coverage can be evaluated based on fault models (built based on manufacturing data). Functional test, on the other hand, evaluates the functionality of the circuit and compares it to a set of functional specifications.

Functional mixed-signal and analog circuits test strategies require the application of analog stimulus and measurement of analog outputs (MILOR, 1998). For analog circuits, the quality of the applied input and measured output is important to the test and highly dependent on the test setup and equipment. Considering again Figure 1.3, the application and measurement of analog signals to/from an analog or mixed-signal core would require the existence of adequate (high-noise immunity and low signal distortion) analog TAMs (IEEE, 2000). These requirements may be difficult to achieve under the SoC environment.

For production testing of these mixed-signal devices, the test should not only verify the functionality of the individual parts, but of the whole system working at nominal speed. This can become hard, specially for complex systems and the test effort on program development and test equipment lead to a significant increase in the time-to-market and in the total cost of the system.

The cost of the test is a very important aspect: testing a SoC can represent 50% of the total cost of the chip (ZORIAN; DEY; RODGERS, 2000). The cost of testing the analog part of a mixed-signal design could reach about 50% of the total production cost of a device in 1997 (ROBERTS, 1997). As new technologies favors the digital part of a circuit, the test of the analog part of the circuit is expected to dominate the production cost (ROBERTS, 1997).

Test in a SoC is still an open issue, especially regarding the test of mixed signal and analog cores. The characteristics of SoCs, like availability of processing power and digital signal processing (DSP) capability, large amounts of available memory and programmable logic can be used to enable test strategies. However, the overhead for

adding additional ADC and DAC converters may be too costly for most systems, and analog routing of signals may not be feasible and may introduce signal distortion.

BIST and on-line test for analog and mixed-signal cores is certainly desirable. BIST solutions, however, are circuit specific or need extra ADC and DAC. This work proposes a solution to the problem of on-line testing and BIST for analog circuits in the SoC context. A simple and low cost digitizer is used instead of an ADC. Thanks to the low analog area overhead of the converter, multiple analog test points can be observed. As the digitizer is always connected to the analog test point, it is not necessary to include muxes and switches that would degrade the signal path. The converter is able to to reach higher frequencies because of its simplicity, enabling the implementation of low cost RF test strategies.

The digitizer has been applied successfully in the test of both low frequency and RF analog circuits. As testing is implemented in the frequency-domain, non-linear characteristics like intermodulation products can also be evaluated. Specifically, practical results were obtained for prototyped baseband filters and a 100MHz mixer. The application of the converter for noise figure evaluation was also addressed, and experimental results for low frequency amplifiers using conventional opamps were obtained.

This thesis is organized as follows: in chapter 2 a review of techniques for the test of analog and mixed signal circuits is presented, emphasizing techniques suitable to the SoC environment. In chapter 3 an analog test method based on frequency-domain is presented, followed by the motivation for the use of low-resolution converters in analog testing. In chapter 4 a simple digitizer, the statistical sampler, is presented. It allows the development of an on-line test strategy based on the statistics of the signals in the analog circuit. In chapter 5, the use of single-bit AD and DA converters in pseudorandom analog test is discussed. The application of the statistical sampler in the RF test scenario is presented in chapter 6. The capabilities of the technique are extended in order to allow the measurement of noise figure in chapter 7. Chapter 8 finishes this thesis with conclusions and suggestions for future work.

2 ANALOG AND MIXED-SIGNAL TEST TECHNIQUES

When embedding a core into a SoC the accessibility is reduced. If not taken into account in the design phase, signals may be neither observable nor controllable, and no test is possible. In this chapter we analyze methods that have been suggested in order to increase the testability of analog circuits, specially methods that could be applied in the SoC context.

As the limited access to signals in the cores is one of the most important limitations in SoCs, several strategies were developed in order to overcome this limitation, and some are presented in section 2.1. Built-in self-test methods and on-line test techniques are discussed in sections 2.2 and 2.3. The chapter closes in section 2.4, where we situate the present thesis in the context of analog test.

2.1 Methods that increase the observability of analog circuits

Design for test or simply DFT is the first attempt to solve the accessibility problem, where one tries to observe the signals of interest and apply test patterns (MILOR, 1998). DFT has been successful in the digital domain through the boundary scan technique. In the analog domain, however, no strategy has allowed the implementation of a similar successful general approach. Cost and area overhead, among others, would make it unfeasible to add an ADC and a DAC to each analog test point.

2.1.1 Analog routing

Some strategies have proposed methods that allow the routing of analog signals. They have not specified a test strategy, but a way to observe the analog signals. To be used in the SoC context to allow BIST or on-line test, these techniques would need an additional AD converter and signal generation circuitry. They are analog scan, transparent blocks and the mixed-signal test bus.

In the analog scan, analog voltages are shifted through an analog shift-register. It provides a way to observe multiple points inside analog blocks simultaneously, but it is only suitable to observe low frequency signals (WEY, 1990).

An approach suggested by (VAZQUEZ, 1996) is the use of a transparent mode for designs with several analog blocks. This mode is enabled during the test and allows the excitation of internal blocks and measurements of their responses. Thus special components are required in the analog design, but the area overhead is very small and there is little impact on dynamic signals. A similar approach is presented in (RENOVELL, 1996-b; RENOVELL, 1998).

To apply dynamic test signals and make measurements, a direct connection to the analog block is desirable. The IEEE 1149.4 standard (IEEE, 2000), is an extension of

the boundary scan standard (IEEE, 1990) and allows the test of mixed-signal devices. The 1149.4 standard defines an analog test bus architecture as shown in Figure 2.1, where several test points inside the system are addressable. Two extra pins are required for the analog signals. They allow the injection of analog test signals and measurement of outputs. These signals are routed through the system by an analog bus of two wires. All other interconnection points are connected to the bus by analog switches. Although this approach allows the measurement of dynamic signals, they are routed through the system and are likely to be distorted by noise and non-linearities in the signal path (caused by coupling and parasitic loads).

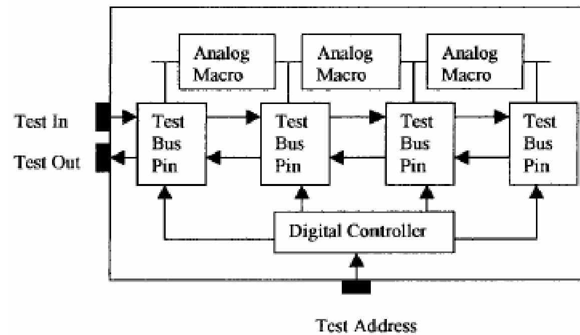


Figure 2.1: Analog test bus (IEEE, 2000).

2.1.2 Analog routing with a digital interface

There are strategies that allow the observation of analog signals and propose methods to digitize them, which could be used in the SoC context to develop test methods. They are a simple extension of the digital scan, the implementation of window comparators with logical gates and the use of an analog comparator as a digitizer for periodic signals.

By including the data registers of AD and DA converters on the scan path, analogue levels could be observed and applied by the system converters (MILOR, 1998). This simple modification in the boundary scan allows the observation and injection of an analog signal in a mixed-signal system, as shown in Figure 2.2. It is also a solution with minimum area overhead and good reusability of resources, but the flexibility is low as only signals connected to the AD converters are observable. Also, this technique is only suited to low-frequency signals.

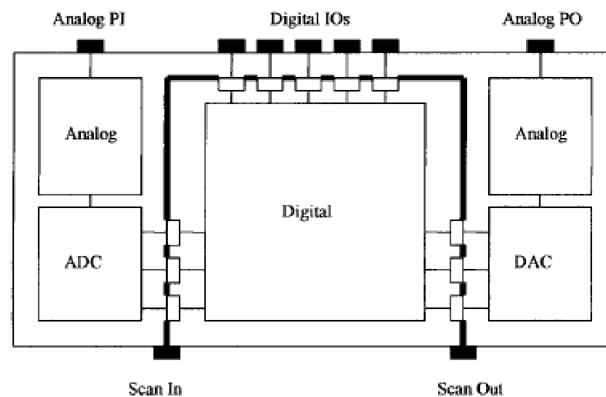


Figure 2.2: Modified boundary scan (MILOR, 1998).

It is also possible to build window comparators using logic gates, and this has been used to allow the verification of voltage levels in analog circuits, allowing the creation of a dc test scheme (VENUTO, 2001-a; VENUTO, 2001-b). One advantage of this method is the low area overhead and simplicity, as the comparators are built using standard logic gates.

Another way to increase visibility is the use of analog voltage comparators with a variable reference threshold. For periodic signals it is possible to build a multiple-pass digitizer with the aid of a precision timing scheme (LOFSTROM, 1996). This limits the application of this technique to ones where the input signal is controlled. It is suited to BIST development, but not to on-line test. Acquisition time can be long for higher resolution acquisitions, and the need for synchronization circuitry can lead to an increase in the area overhead of this solution.

A recent implementation of this scheme has been reported in (NOGUCHI, 2005), where a multi-channel scheme was used in order to reduce the total acquisition time of the technique, as illustrated in Figure 2.3. The prototype was able to perform equivalent acquisition at 40-ps (about 25GHz).

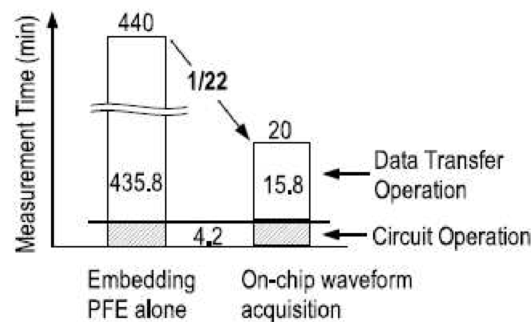


Figure 2.3: Acquisition time reduction because of parallel acquisition (NOGUCHI, 2005)

The access methods analyzed in this brief review are summarized in table 2.1.

Table 2.1: Access methods

CLASS	METHOD	PROBLEM
Fully analog	Analog scan (WEY,1990)	needs digitizer
	Transparent blocks (VAZQUEZ, 1996; RENOVELL, 1996-b)	needs digitizer
	Mixed-signal test bus (IEEE, 2000)	needs digitizer
Digital output	Modified digital boundary scan (MILOR, 1998)	low-frequency, not flexible
	Window comparator (VENUTO, 2001-a)	low-frequency
	Periodic waveform digitizer (LOFSTROM, 1996; NOGUCHI,2005)	periodic signals

2.2 BIST methods for analog circuits

Several methods have been proposed to address the need for built-in self-test of analog circuits. These methods can be based on the application of test vectors or not.

2.2.1 Vector -based BIST schemes

These are the methods that require the application of an input signal to the analog circuit. This can be a dc-level, a sinusoidal waveform, a special waveform or noise.

The test based on dc-level measurement allows simple digitizers like (VENUTO, 2001-a) to be used, being a very low area overhead and cost test strategy. Some dc-based test schemes propose the use of a scaled sum of several dc-levels in the circuit as a signature, as this allows a test based on just a single analog voltage measurement (SASHO, 1998; RENOVELL, 1996-b; CHATTERJEE, 1996). All dc-level schemes have the limitation of testing dc characteristics, but this may be enough for some cases like production testing.

The use of sinusoidal signals allows the transfer function of a linear circuit to become known after a frequency scan is made. This characterizes the amplitude and phase response of the system and verifies the functionality of the system. Nevertheless, the application of a large number of sinusoidal components is a slow process. This situation is worsen if the dynamics of the system are slow, requiring the application of low frequency signals. This can lead to long test times to correctly characterize the system. The optimization of the test set is the selection of the minimum number of input frequencies that allows the verification of the correct functionality of the circuit. This choice can be made based on a sensitivity analysis of the analog circuits (SLAMANI, 1992; HAMIDA, 1993; SLAMANI, 1995). The use of sinusoidal signals can lead to simple implementations of BIST, like in (COTA, 2000-b).

An alternate method is to use simulation tools to evaluate the most probable physical defects and their impact on the function of the circuit. This structural analysis will help find the smaller test set that can detect the majority of the faults that a circuit may suffer (HUYNH, 1998; SAHU, 2001). This approach allows a measure of quality of the test to be evaluated, the fault coverage, who expresses the ratio of the detected faults by the total number of faults simulated. In this case, other input signals can be defined. The simulation approach can lead to methods capable of identifying or diagnosing the defects in the circuit. The simulated responses to the input stimuli are recorded in a database for comparison with real data. Each defect is an element of a dictionary of faults. The diagnosis is based on distance measurement from real data to elements in the fault dictionary. Several factors like measurement errors and intrinsic variation in circuit components will impact the performance of these methods. Also, simulation time can be very high for large analog circuits.

Another BIST technique (OHLETZ, 1991) applies pseudorandom noise and uses AD and DA converters already present in the system. It considers a topology as shown in Figure 2.4, where a digital block is surrounded by analog blocks. This scheme generates a signal through the DAC (specifically, a LFSR generates a pseudorandom noise sequence) that is routed to the input block and captured by the ADC. The BILBO and MISR registers analyze the sequence (signature analysis) (MILOR, 1998). Other approaches like (MARZOCCA, 2002; PAN, 1997; TOFTE, 2000) suggest the use of other analysis methods to improve test quality and enable fault diagnosis. These

methods are interesting for SoCs as they have little area overhead and can reuse system resources. On the other hand, they are not suitable to on-line test.

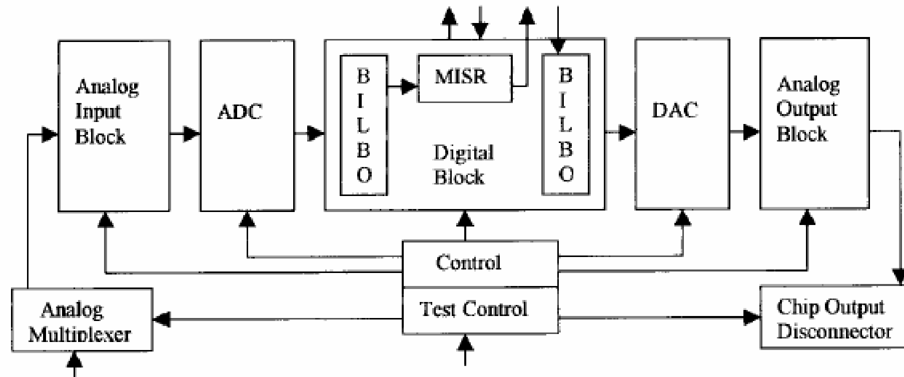


Figure 2.4: System modification to enable test in the HBIST scheme (OHLETZ, 1991).

2.2.2 Vectorless BIST schemes

There are some schemes intended for BIST that do not require an analog signal generator and can lead to a small area overhead. The oscillation-based test method turns the analog circuit into an oscillator. Methods based on supply current measurement analyze the load of the analog circuit supply.

The oscillation-based technique (ARABI, 1997; HUERTAS, 2000) allows the test of filters and amplifiers without the use of a signal generator, as the circuit under test is converted into an oscillator during test. If a fault is present, the frequency and amplitude characteristics of the oscillation will change. This method has the need to insert switches in the circuit to allow reconfiguration, and this could lead to performance degradation.

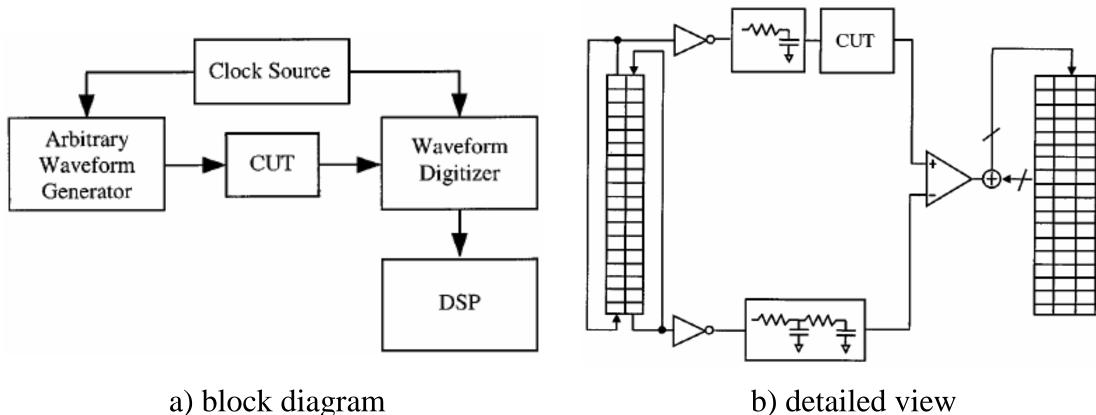
Methods like (SILVA, 1996) analyze the supply current of the analog circuit. They need special current sensors and associated digitizers to be implemented, and require calibration for each specific circuit to be tested, as the consumption is technology-dependent. On the other hand, they could be used also in on-line test schemes.

2.2.3 A structure for BIST in the SOC context

The built-in self-test (BIST) approach enables the test at full speed without external test equipment. If an adequate analyzer is present, just one digital output pin is necessary to output the test result. The drawbacks are related to the area overhead needed by the test circuit and the design of high-quality generators and analyzers (MILOR, 1998). This hardware overhead can be minimized if the test circuitry is used by other components in the system. In the SOC context, this area overhead could be further reduced if hardware resources already available in the system were used by the test.

One example of analog BIST structure is shown in Figure 2.5a (HAFED, 2002), where a signal generator and a waveform digitizer are implemented on a chip. This approach implements an arbitrary waveform generator, which generates a periodic input to the CUT. This scheme basically applies a high-speed bit stream to an analog low-pass filter to obtain the desired waveform, as shown in Figure 2.5b. The waveform digitizer uses a voltage comparator and a variable reference threshold, so multiple passes of the

input waveform are needed (LOFSTROM, 1996). This does not limit the bandwidth of the signals, as a 4 GHz bandwidth has been reported (HAFED, 2002; HAFED, 2003).



a) block diagram b) detailed view

Figure 2.5: DSP-based BIST (HAFED, 2002).

The analysis of the data obtained should be performed by a DSP processor, which could be on chip (if available) or external. In this case, only digital data should be transferred to the test equipment. This scheme is suitable to be implemented on an analog or mixed-signal core, as its analog area overhead is small (HAFED, 2002). It also allows several BIST methods to be used, as an arbitrary periodic waveform generator is available. On the other hand, the scheme is useful for BIST only, as the input signal must be controlled. The analog overhead of the solution presented is related to the filters needed by the signal generator and by the digitizer. It also requires a high precision synchronization scheme.

Table 2.2: BIST methods.

CLASS	METHOD	PROBLEM
Vector-based	Sinusoidal input (SLAMANI, 1992; HAMIDA, 1993)	input selection
	General waveform input (HUYNH, 1998)	simulation time, input selection
	DC-level (VENUTO, 2001-a; RENOVELL, 1996-a)	dc only
	Pseudorandom (OHLETZ, 1991; MARZOCCA, 2002)	signal generation, test time
	BIST framework (HAFED, 2002)	periodic signals
Vector-less	Oscillation-based (ARABI, 1997; HUERTAS, 2000)	may degrade circuit performance
	Supply current based (SILVA, 1996)	needs calibration, specific

2.3 On-line test methods for analog circuits

Although suited for the production test, BIST techniques are generally not able to be used for on-line test, as the circuit has its topology modified during the test (VAZQUEZ, 1996; ARABI, 1997) or its input signal is being controlled by the test

mechanism (SLAMANI, 1995; HAFED, 2002). Thus on-line test requires the development of test strategies that continuously evaluate the operation of the circuit during normal operation. This problem of on-line monitoring becomes more important due to the use of sub-micron technologies, which are more sensitive to noise and radiation effects (ABRAHAM, 1999).

One strategy to enable concurrent testing is the use of duplicates of the circuit, as shown in Figure 2.6 (LUBASZEWSKI, 1995). In this scheme a comparison mechanism verifies the similarity between the programmable reference block and the block under test. This scheme could be used also for BIST, but the programmable reference block may be difficult to obtain for a variety of analog circuits.

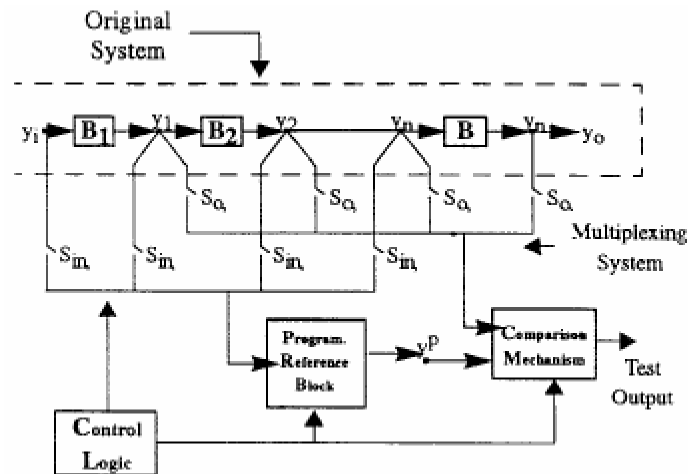


Figure 2.6: On-line test through replication (LUBASZEWSKI, 1995).

A technique that uses digital replication to the on-line test of analog circuits was proposed in (COTA, 2000-a), and is based on a system identification approach. The area overhead in this solution is large, as at least two AD converters are needed to sample the input and output signals of the system to be modeled. The computational power needed to implement the strategy is also large, but could be used for non-linear analog circuits (SOUZA, 2002).

For the case of fully differential circuits there is the possibility of building analog checkers (LUBASZEWSKI, 1995). An analog checker also can be used to verify an operational amplifier (VELASCO-MEDINA, 1998). For linear analog filters, continuous checksums have been proposed (CHATTERJEE, 1993) and are implemented by a cascade of analog integrators. They generate a non-zero signal in the case of an error in the transfer function of the circuit. These three solutions are circuit or topology dependent and need a digitizer in order to evaluate the checker or checksum output. The techniques are summarized in table 2.3.

Table 2.3: On-line test methods

CLASS	METHOD	PROBLEM
Duplication	Analog replication (LUBASZEWSKI, 1995)	area overhead, specific
	Digital modeling (COTA, 2000-a; SOUZA, 2002)	area overhead, computational load
Checksum	Continuous checksums (CHATTERJEE, 1993)	specific, needs digitizer for check
Checkers	Analog checkers (LUBASZEWSKI, 1995; VELASCO-MEDINA, 1998)	specific, needs digitizer for check

2.4 Conclusion

All the techniques mentioned have not yet solved the general problem of BIST and on-line test, as the requirements for BIST are different for on-line test. This has motivated the appearance of BIST proposals that modify the circuit topology or forces a specific input signal during the test phase. On-line test approaches, on the other hand, have relied on circuit replication and analog checkers that are circuit specific and require extra area and calibration. This makes it difficult to apply these techniques in general.

Testing of analog and mixed-signal cores in the SoC environment is still an open issue, as only specific solutions are used for analog circuits, like ADCs and PLLs (SIA, 2004). The characteristics of SoCs, like availability of processing power and digital signal processing (DSP) capability, large amounts of available memory and programmable logic can be used to implement test strategies on chip.

As process integration technology evolves, the area occupied by a digital design shrinks, allowing more functionality to be included in the same area. This digital computing availability increases exponentially, following Moore's law. However, for analog circuits the trend is not the same (WALDEN, 1999). This way, the digital area in a mixed-signal circuit is expected to shrink in the future, but the analog part will tend to dominate the design, as illustrated in Figure 2.7 (SIA, 2004). With this continuous trend, while the analog part of designs will tend to dominate, large amounts of digital processing power will be available at low cost.

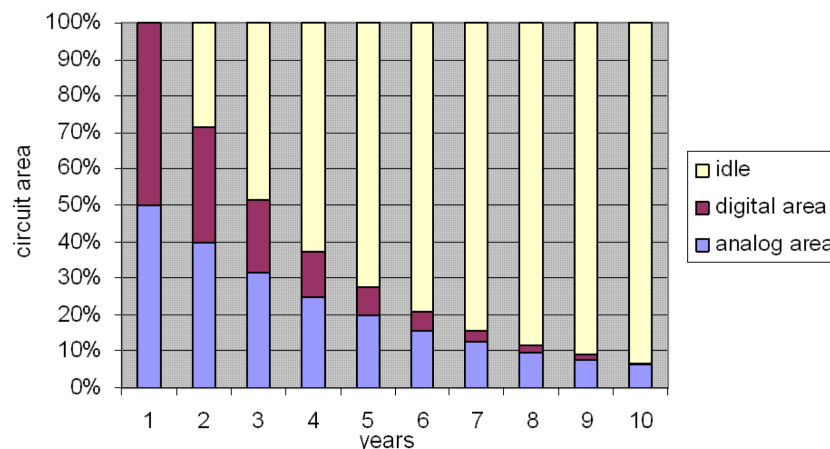


Figure 2.7: Example of analog and digital area distribution in a hypothetical design.

Considering the need for additional test structures for mixed-signal circuits, it would be desirable to introduce only additional digital area, or the smallest possible analog area. This way, the additional cost in area due to test structures would follow the trend of digital circuits. Furthermore, techniques that enable the exchange of analog area by digital processing would also take advantage of technology scaling. Besides area cost, another issue regarding additional analog area is the need for testing these extra structures.

BIST and on-line test for analog and mixed-signal cores is certainly desirable. The SoC environment can provide resources for test implementation at no cost, since they are already built inside the system. However, the overhead for adding additional ADC and DAC converters may be too costly for most systems, and analog routing of signals may not be feasible and may introduce signal distortion. This way, there is a need for low cost digitizers with minimum analog area in order to enable analog test in the SoC environment.

In the next chapter the motivation for reusing digital resources already built in the SoC environment is explored. A technique for testing analog circuits using entirely digital resources is developed. The need for lowering analog area overhead in analog tests is also explored in a study to relax ADC requirements in analog test.

3 LOWERING ANALOG TEST COSTS

In this chapter we analyze two approaches that are able to lower analog test costs. In the first approach, a test method that is able to reuse SoC resources in order to implement the test response analyzer is presented. Test methods entirely based on digital resources can benefit from SoC resources already available in the system at practically no cost. In the second approach, an analysis of the impact of reducing the resolution requirements of ADCs used in analog test is presented. The use of low resolution ADCs can reduce the cost of additional ADCs in the monitoring of extra test points. Besides, lowering the requirements of conventional ADCs allows faster and smaller analog to digital converters to be built, or extend the capabilities of actual devices on chip.

3.1 A test strategy for analog circuits using spectral analysis

Spectral analysis of discrete time series is a well known (KAY, 1981; HAYES, 1996; BENDAT, 1986) subject and is widely used. The estimation of the power spectrum density (PSD) is usually based on procedures employing the fast Fourier transform. It is computationally efficient and produces reasonable results for a large class of signal processes (KAY, 1981).

In this chapter we propose the use of an estimate of the PSD as a signature of the circuit. The basic idea is shown in Figure 3.1. In the training phase, a random noise with known statistical characteristics is applied to the input of the fault-free circuit, and the PSD of the output is estimated. This is kept as the signature of the fault-free circuit. In the testing phase, the PSD of the circuit under test is estimated and compared to the signature of the fault-free circuit. The comparison can be tuned to allow specific frequency response needs, based on a set of comparison parameters.

The required spectral characteristics of the noise should be a spectrally flat distribution, in order to excite the system under test in all frequencies of interest and obtain meaningful results from the evaluation of the PSD.

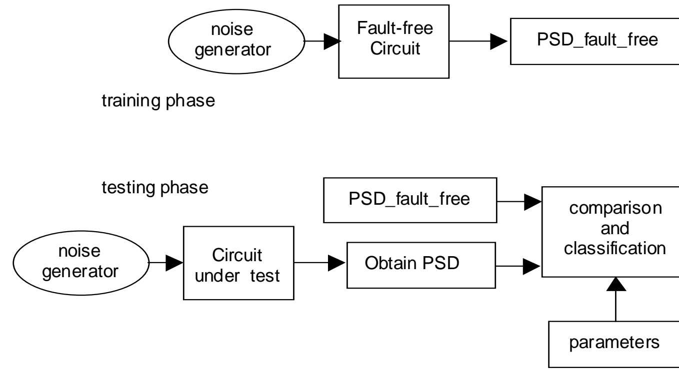


Figure 3.1: Test strategy using power spectral density (PSD) estimation (NEGREIROS, 2003-a).

3.1.1 Estimating the power spectral density

The Fourier transform of the correlation function for a random process is called the *power spectral density function*, being denoted by $S_{xx}(f)$. The plot of $S_{xx}(f)$ versus f is called the *power density spectrum.* According to Bendat (BENDAT, 1986), the *power spectral* or *autospectral density function* is given by

$$S_{xx}(f) = \int_{-\infty}^{+\infty} R_{xx}(\tau) \exp(-2j\pi f\tau)\, d\tau\,. \tag{3.1a}$$

The *one-sided power spectral density function* is given by ($0 \le f < \infty$)

$$G_{xx}(f) = 2 \cdot S_{xx}(f)\,. \tag{3.1b}$$

The true PSD of the system can not be acquired from the observation of the output, but only an estimate of the PSD can be obtained (KAY, 1981; BENDAT, 1986). This is true not only for PSD estimates, but for other parameters like mean and correlation, and is a characteristic of stochastic signals. For PSD estimates based on the fast Fourier transform (FFT) and periodogram averaging, an associated normalized error can be obtained. This normalized error presents a boundary to the variation of the estimates around the true, unknown PSD.

In Figure 3.2 the estimated PSD for a unit variance zero mean gaussian noise is shown, together with the true PSD obtained from the biquad (shown in Figure 3.5) circuit model parameters, and the associated normalized error.

The normalized error in the PSD estimates depends basically on the number of FFT estimates used in the averaging process. Depending on the sampling frequency used and FFT resolution, the total acquisition time can be easily estimated.

The error in the PSD estimates can be obtained by using (BENDAT, 1986, equation 8.160).

$$(1-\frac{2}{\sqrt{n_d}})\,\hat{G}_{xx}(f) \le G_{xx}(f) \le (1+\frac{2}{\sqrt{n_d}})\,\hat{G}_{xx}(f) \tag{3.2}$$

where n_d is the number of FFTs needed by the estimate and $\hat{G}_{xx}(f)$ is the estimated one-sided *power spectral density function* .

One can observe that the percent error in the estimate, a/100, is given by

$$\frac{a}{100} = \frac{2}{\sqrt{n_d}} \tag{3.3}$$

Solving Equation 3.3 for n_d, one obtains

$$n_d = \frac{4 \cdot 10^4}{a^2} \tag{3.4}$$

Equation 3.4 gives n_d, the number of FFTs needed to achieve a given percent error (a) in the PSD estimate. It also shows that there is a direct link between test time and test resolution. For example, for a 20% error in the estimates, n_d=100, meaning that averaging over 100 FFTs is needed. When performing a FFT over a data window of 128 points, 12800 samples from the signal of interest need to be acquired.

The smaller the required error, the larger the number of required FFTs. Unfortunately, this dependence is quadratic, meaning that a fine resolution will require a long test time. We must stress that this limitation is due to the use of noise, and any pseudorandom test method is subject to these estimation errors in the parameters. Expressions 3.2 to 3.4 clearly state this fact.

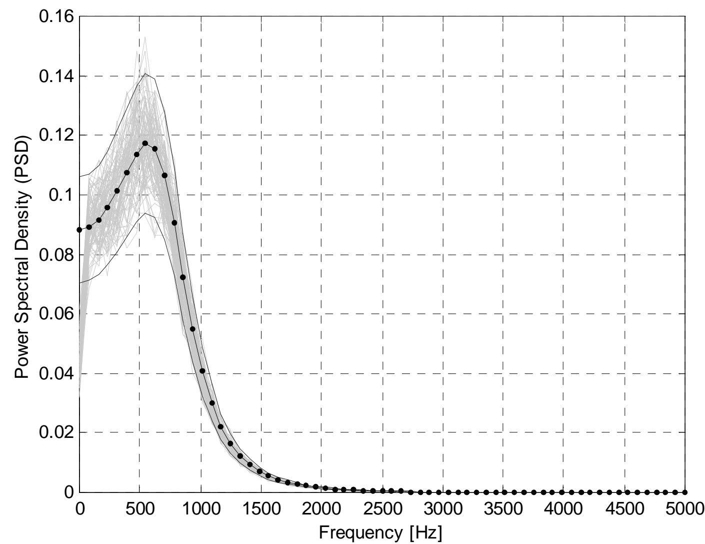


Figure 3.2: True PSD (.), theoretical error (dark lines) and 100 PSD estimates (light lines) using Welch's method (HAYES, 1996) with 0% overlap and Hanning window (MATLAB simulation) (NEGREIROS,2003-a).

3.1.2 Comparing power spectral density estimates

In order to compare the reference PSD and the estimated PSD of the circuit under test (CUT), the error associated with the estimates must be taken into account. As illustrated in Figure 3.3, a region of overlap exists for PSD estimates for circuits with and without faults. If the two PSDs are close to each other, a large overlap region will result, making it difficult to establish a threshold to separate the curves. On the other hand, the expected true value of each PSD is clearly distinguished.

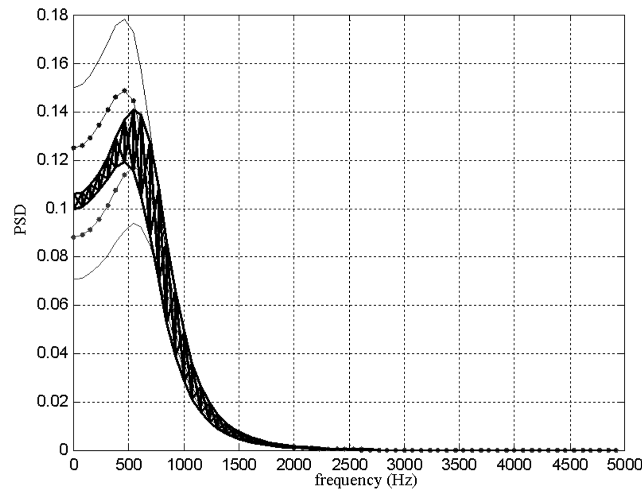


Figure 3.3: The theoretical PSD for a fault-free system and faulty system, showing the normalized error expected, with the overlapped PSD region marked (NEGREIROS,2003-a).

To compare the reference and estimated PSD curves in Figure 3.3, two vectors must be analyzed. It is desirable in an automatic test strategy to have a single parameter in order to make the comparison simpler. In this work two parameters are proposed based on the difference between the estimated PSD curve and the reference PSD curve, as shown in Figure 3.4.

The comparison parameters, which build the signature of the circuit, are formed using the distance value marked as “A” in Figure 3.4. For each frequency used in the comparison, this difference is evaluated. The first parameter (par_sum) is formed by the sum of the absolute values of the difference "A". The second parameter (par_mean) is formed by the mean value of the squares of the difference "A". Equation 3.5 expresses this idea mathematically.

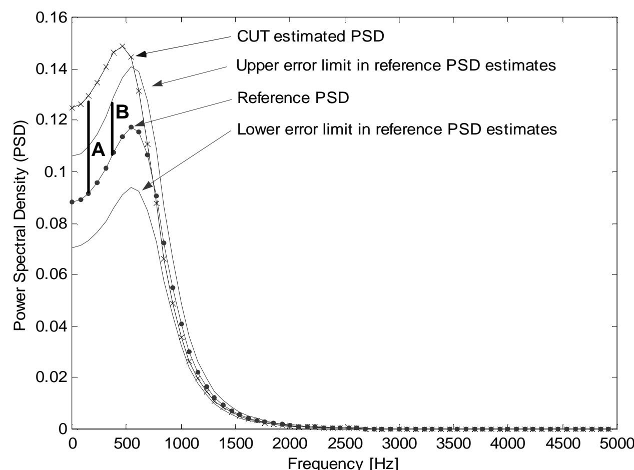


Figure 3.4: The theoretical PSD for a fault-free system and faulty system showing the difference between the estimated PSD and the reference PSD ("A"), and the difference between the error limit for the reference PSD and the reference PSD itself ("B") (NEGREIROS,2003-a).

$$par_sum = \sum_{f=Fmin}^{Fmax} \left| Estimated_PSD(f) - Reference_PSD(f) \right|$$
$$par_mean = \frac{1}{N_{freq}} \sum_{f=Fmin}^{Fmax} (Estimated_PSD(f) - Reference_PSD(f))^2 \quad (3.5)$$

A comparison threshold is defined calculating the parameters for the error limit curves, as indicated by the point "B" in Figure 3.4 and expressed in Equation 3.6. In the former definition, the threshold is the same for both the upper and lower error limit curves.

$$threshold_{sum} = \sum_{f=Fmin}^{Fmax} \left| Error_limit_PSD(f) - Reference_PSD(f) \right|$$
$$threshold_{mean} = \frac{1}{N_{freq}} \sum_{f=Fmin}^{Fmax} (Error_limit_PSD(f) - Reference_PSD(f))^2 \quad (3.6)$$

3.1.3 Testing analog circuits using spectral analysis

In this section the performance of the proposed method is evaluated by means of simulation and experimental results. In section 3.1.3.1, the biquad filter shown in Figure 3.5 is simulated using Matlab and the two parameters in Equation 3.5 are analyzed. In section 3.1.3.2 the parameter par_mean is established as a distance measure, and issues regarding the influence of errors in the estimation of the PSD are addressed.

3.1.3.1 Testing a biquad filter

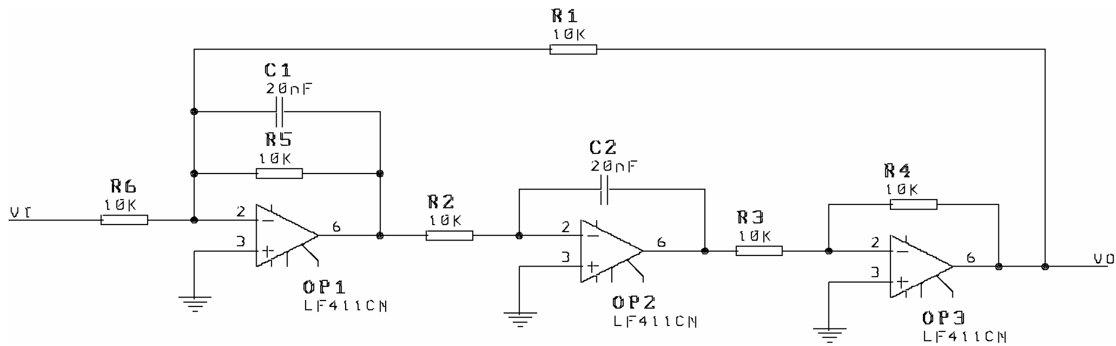


Figure 3.5: Schematic diagram of the biquad filter (NEGREIROS,2003-a).

A bilinear transformation (OPPENHEIM,1989) of the transfer function of the biquad circuit shown in Figure 3.5 was performed in order to obtain a discrete-time model suitable for simulation in the Matlab environment. The simulation considered a 10kHz sampling frequency and a length 128 FFT. For a 20% error limit in the estimated PSD, the total record length is 12800 samples (from Equation 3.2). For a 10% error limit, the record length increases to 51200 samples.

The used input signal was random noise with uniform distribution and unitary variance. The estimated PSD was calculated using Matlab Welch's method implementation (MATHWORKS, 1997), with a 50% overlap (in order to reduce the variance of the estimate).

The nominal component values were used to obtain the reference PSD and associated error limit. A variation from -99% to +99% of the nominal value was applied to the selected component.

The test results for capacitor C1 are shown in Figure 3.6. In Figure 3.6a, the test results for par_mean are shown, while in Figure 3.6b the results for par_sum are presented. The test for total record length of 12800 samples is shown by the "x" marker. The test for 51200 samples is shown by the "." marker. Both tests used the same threshold (to decide if the PSD is the same as the reference PSD or not) derived from the 12800 samples case. Each point in the curve is the percent failure in the test, averaged over 1000 trials. For a -60% variation, for example, all parameters indicate a failure in the circuit, and this result was obtained in 100% of the 1000 isolated tests.

In Figure 3.6, the proposed parameters were able to detect faults larger than +/- 60% on C1. In the same figure, circuits with variations as large as (+/-) 20% in C1 were classified as fault-free. For about (+/-) 30% to (+/-) 50% variation, there is a region of uncertainty. For (+/-) 30 % variations, most of the cases were classified as fault-free, but not all. For (+/-) 50% variations, most of the cases were classified as faulty, but not all. The increase in test time provided a sharper transition, as shown in Figure 3.7 by the "." marked lines, thus reducing the uncertainty region.

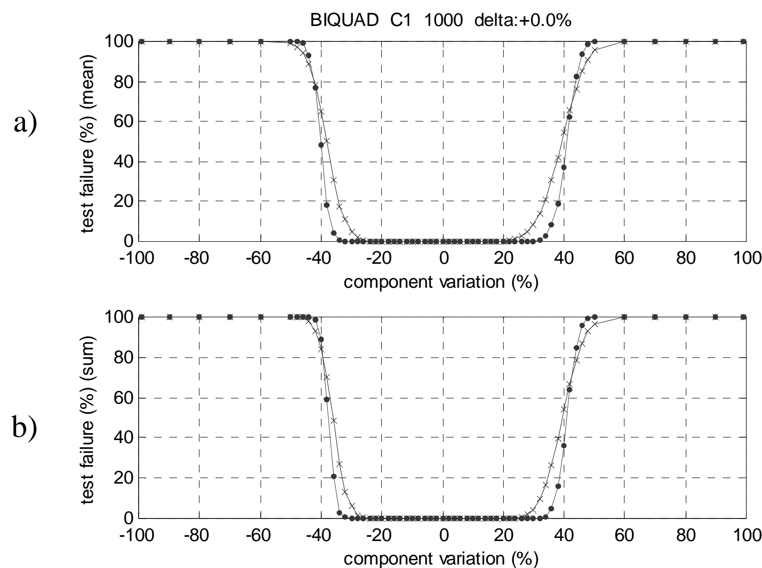


Figure 3.6: Test for capacitor C1 and record lengths of 12800 ("x") and 51200 (".") samples: (a) results for parameter par_mean, and (b) results for parameter par_sum (NEGREIROS,2003-a).

As the threshold parameter defined in Equation 3.6 is used to decide if the CUT PSD is the same as the reference PSD or not, its value can be used to tune the test strategy. As indicated in Figure 3.7, a reduction of 50% in this parameter (the threshold for 12800 samples used in Figure 3.6) reduces the tolerance of the test to faults in C1, allowing the detection of deviations of about 30% or less. The transition region remained the same as shown in Figure 3.6. The parameter par_sum, for this reduction and 12800 samples, classifies a very small region of deviations as fault-free, and has a large transition region.

A further reduction of 70% in the threshold parameter renders useless the simulations for 12800 points, as none of the parameters is capable of assuring 100%

fault-free circuits ("x" marker), as shown in Figure 3.8. For 51200 points ("." marker), it is still possible to incorrectly classify fault-free circuits, and the parameter par_sum has a smaller region for accepting a circuit as fault-free than the parameter par_mean.

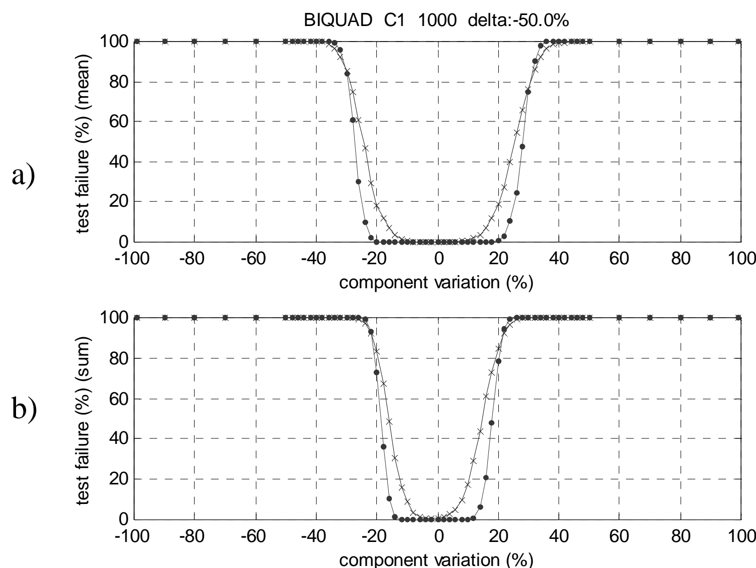


Figure 3.7: Test for capacitor C1 with a reduced comparison threshold: (a) results for parameter par_mean and (b) results for parameter par_sum (NEGREIROS, 2003-a).

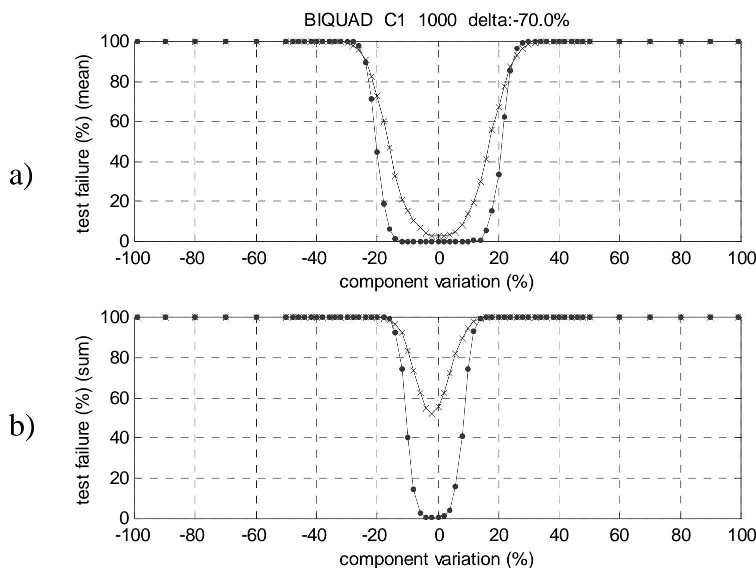


Figure 3.8: Test for capacitor C1 with a 70 % reduction in the comparison threshold: (a) results for parameter par_mean and (b) results for parameter par_sum (NEGREIROS, 2003-a).

3.1.3.2 Issues regarding errors in the PSD estimates

The proposed parameters of Equation 3.5 can be viewed as a distance measurement from the reference PSD. In the following we use the parameter par_mean to measure the distance in order to perform the simulations. According to the number of points used in the PSD estimates, a threshold can be defined to separate the faulty and fault-free circuits. In Figure 3.9 the biquad circuit was simulated and variations in component C1

were introduced. As it can be seen, the distance from the reference has a minimum at the nominal value, and increases as larger variations are introduced. The threshold for 20% error in PSD estimates is shown as a line.

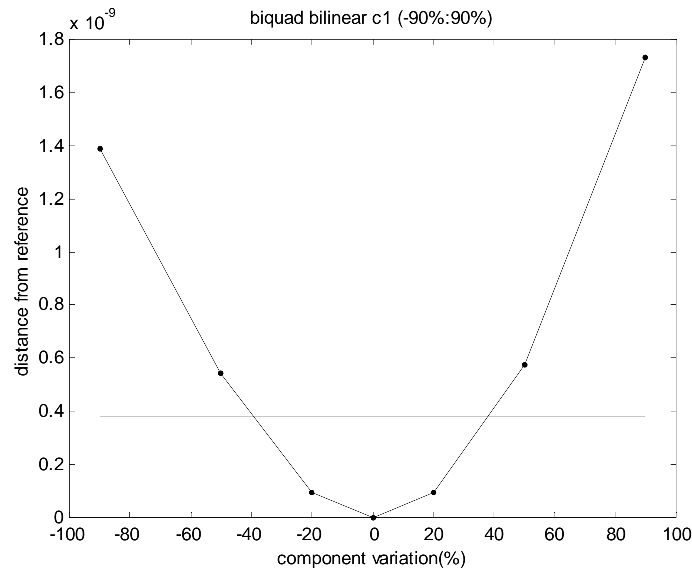


Figure 3.9: Distance measures for changes in C1 from -90%, -50%,-20%, 0%,20%,50% and 90% and threshold for 20% error in PSD estimates (NEGREIROS, 2003-a).

It should be stressed that the curve in Figure 3.9 does not take into account the effects of PSD estimation using noise. If one considers this fact, the distance measured for a given component variation is no longer constant, because of the variations in the PSD estimates, as shown in Figure 3.10. In the case of Figure 3.10a, simulations with 70% variation in C1 were all above the threshold, but some simulations with 60% variation in C1 were bellow. Some simulations with 20% variation were above the threshold.

The performance of the test can be improved if one uses longer data records, as the uncertainty in the PSD estimates diminishes. This is illustrated in Figure 3.10b, where it can be seen that the variations in the estimated distance for a given component variation is reduced.

a)

b)

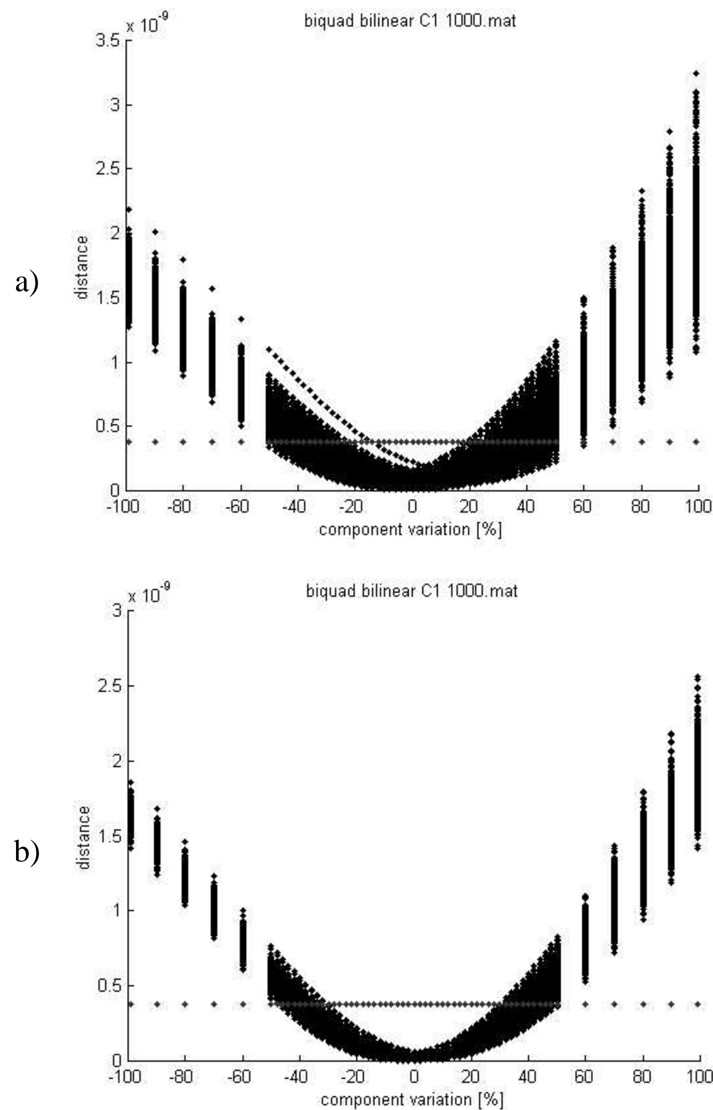


Figure 3.10: Distance measures for changes in C1 from -99% to +99%, using noise as input signal and PSD estimates. (a) Estimates using 12800 points and (b) estimates using 51200 points (NEGREIROS, 2003-a).

3.1.4 Practical results

In this section a practical evaluation of the method was performed by prototyping two circuits with discrete components and manually performing the injection of the faults in the discrete components. Only single faults were considered in these experiments. The analyzed faults were parametric or soft (20% and 50% variation), and hard (stuck-open and stuck-short).

The experimental setup used is shown in Figure 3.11. A gaussian noise was generated in Matlab and downloaded to an arbitrary waveform generator. Data was acquired and transferred to a PC for processing using Matlab. The biquad circuit shown in Figure 3.5 was prototyped using discrete components. Faults were inserted by changing the values of the components. Record lengths of 12800 samples were acquired using 16 bit samples and 8000 kHz sampling rate, ac coupled.

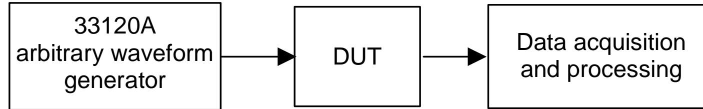


Figure 3.11: Experimental setup (NEGREIROS, 2003-a).

For the experimental evaluation, the distance was calculated using the parameter par_mean. In Table 3.1 the PSD distance between the faulty circuit (with a specific variation in the component) and the reference PSD was evaluated, for a threshold calculated based on a 20% variation in the reference PSD. For component C1, for example, the parametric deviations of 20% were not detected as a fault, as expected after analyzing the results of the previous sections.

In Table 3.2 the same measurements were repeated, but the biquad filter was replaced by another circuit, the state-variable low-pass filter from the ITC'97 analog circuits benchmarks (KAMINSKA, 1997). In this case the behavior is close to the biquad, but more components with soft faults are not detected.

Table 3.1: PSD distance measured for 20% error in the PSD estimates (12800 points, threshold: 1.5e+7) (marked cells indicate no fault detected)

	-50%	+50%	-20%	+20%	OPEN	SHORT
C1	2.2e+7	2.5e+7	**5.2e+6**	**8.1e+6**	3.8e+8	6.7e+7
C2	3.9e+8	5.6e+7	1.9e+7	2.1e+7	3.8e+8	3.5e+9
R1	1.9e+8	1.7e+8	4.4e+7	2.7e+7	3.8e+8	1.5e+11
R2	4.2e+8	5.1e+7	3.9e+7	**1.1e+7**	3.6e+8	3.8e+8
R3	3.7e+8	5.0e+7	3.4e+7	1.7e+7	1.1e+10	3.8e+8
R4	1.2e+8	8.8e+7	2.2e+7	**1.4e+7**	3.8e+8	1.1e+10
R5	1.2e+8	1.4e+8	2.6e+7	1.9e+7	9.7e+10	9.7e+10
R6	3.3e+9	1.2e+8	1.5e+8	3.3e+7	1.3e+10	3.8e+8

Source: NEGREIROS, 2003-a.

Table 3.2: PSD distance measured for 20% error in the PSD estimates (12800 points, threshold: 1.8e+7) (marked cells indicate no fault detected)

	-50%	+50%	-20%	+20%	OPEN	SHORT
C1	3.1e+7	4.1e+7	**6.5e+6**	**6.1e+6**	4.4e+8	9.3e+7
C2	5.4e+8	6.8e+7	3.1e+7	2.0e+7	4.4e+8	7.2e+9
R1	2.0e+9	1.1e+8	1.2e+8	2.3e+7	6.3e+10	4.4e+8
R2	6.8e+7	2.3e+7	**1.0e+7**	**4.4e+6**	4.4e+8	8.3e+7
R3	3.5e+7	3.6e+7	**8.7e+6**	**5.6e+6**	9.3e+7	4.4e+8
R4	5.3e+8	6.1e+7	5.3e+7	**1.2e+7**	1.8e+8	4.4e+8
R5	2.4e+8	3.1e+8	5.5e+7	4.0e+7	4.4e+8	1.8e+11
R6	3.8e+8	3.8e+7	2.7e+7	**8.7e+6**	8.4e+10	2.6e+8
R7	7.8e+7	9.8e+7	2.2e+7	**1.3e+7**	2.5e+8	9.1e+10

Source: NEGREIROS, 2003-a.

3.1.5 Analysis

The results shown in the preceding section demonstrate the feasibility of a test strategy for analog circuits based on a comparison of the PSD. The technique is able to

detect deviations in the transfer function of a system using the PSD as a basic signature. A distance is evaluated between the faulty and faulty-free PSD.

If a given analog circuit has a very low sensitivity to one component, then the transfer function will have a small deviation from the faulty free case. On the other hand, if the sensitivity is high, even small component variations will produce large deviations in the PSD from the faulty free case.

The key point here is that the technique is not limited to large deviations in components, but to deviations in the transfer function of the DUT. So, it is possible to detect 1% deviations in a given component, if this change produces a significant change in the PSD of the DUT.

The test time is an important issue, since it is directly related to the cost of the SOC. In the proposed strategy, test time can be tuned to comply with specific test requirements. A fast test can be made using a predefined number of samples, which will have a specific uncertainty region. This number of samples should be chosen accordingly to the equations presented earlier, for the time requirement used.

If the uncertainty region should be minimized (or if test sensitivity should be increased) then the number of samples used in the estimation of the PSD should be increased. This will also increase test time, but will allow the test strategy to conform to more restrictive requirements. In the practical results section, test time regarding only the data acquisition process is 12800 [samples]/8000 [Hz]= 1.6 s.

If one wants to reduce test time, one could reduce the number of points in the FFT by two. In this case the same error in the PSD estimate would be achieved for half the test time. The drawback is that the PSD estimate will have a lower frequency resolution, and this could mask the presence of soft deviations in the circuit under test.

The practical results presented for the biquad and state-variable low pass filters have shown that the method is able to detect both hard and soft faults, but its sensitivity depends on the circuit and on the number of samples used for test. Furthermore, the method is not able to diagnose the faults.

The influence of the noise in the components can be evaluated by referring the noise sources of the system to its input. Considering thermal noise for resistors, their amplitude is too small compared to a noise generator with full amplitude range like the one used in the proposed technique. On the other hand, even if the input referred source of noise reaches a large amplitude, its distribution would be uniform (white noise, flat spectrum), and could be helpful in the test.

Regarding the influence of the noise of the measurement system, it will be added to the evaluated PSD. The PSD estimates tend to filter noise and other non-correlated imperfections. In order to influence the comparison, the noise of the measurement system should be very large, even larger than the signal itself. Quantization noise is not a serious issue, for example, as the technique has been applied successfully in a continuing work using a single bit AD converter (NEGREIROS, 2003-b).

Future work includes the evaluation of suitable noise power levels in order to prevent circuit saturation and non-linear behavior.

3.2 Low Resolution AD Converters Applied to Analog Testing

This section provides a comparison of the use of low resolution converters to analog test, in order to illustrate the basic trade-offs regarding test time, ADC resolution and analog test method. Although the idea of using low resolution ADCs for analog test is not new, their use with sinusoidal signals was not suggested to date. This is mainly because of the distortions introduced.

Although there are published works using low resolution data converters, none has already been presented in order to illustrate and compare their application. Also, lower resolution test strategies for non-noise signals usually require a reference analog waveform. In this work we analyze the direct application of low resolution ADCs for analog test, without using other reference analog signals.

3.2.1 Methodology

In this section the setup used for comparison is described. Fault model and test approaches used in the comparison are also briefly presented.

3.2.1.1 Test setup and fault model

In order to provide flexibility, simulation and analysis were carried out using Matlab. A second order low pass filter (see Figure 3.5) has been selected as the device under test (DUT). The DUT model has been constructed using bilinear transform.

In order to ease the comparison of multiple resolution ADCs in the test, only the quality factor of the filter has been changed. The equation for a second-order low-pass filter is given below:

$$H(s) = \frac{K w_o^{2}}{s^2 + s\frac{w_o}{Q} + w_o^{2}} \tag{3.7}$$

For the biquad filter, the quality factor is given by Equation 3.8. Changing the quality factor can be easily accomplished by changing the value of R5, as this component influences neither the DC gain nor the cut-off frequency of the filter.

$$Q = \sqrt{\frac{R_4 R_5^{2} C_1}{R_1 R_2 R_3 C_2}} \tag{3.8}$$

In figure 3 the effect of changing the quality factor of the filter is illustrated. It presents the nominal value, 50% variations and 90% variations.

We will consider deviations above 10% and larger as parametric faults. Deviations of 10% or less will be considered as acceptable values from process variation.

The biquad low-pass filter topology presented in Figure 3.5 has the quality factor (Q) equal to unity for nominal component values.

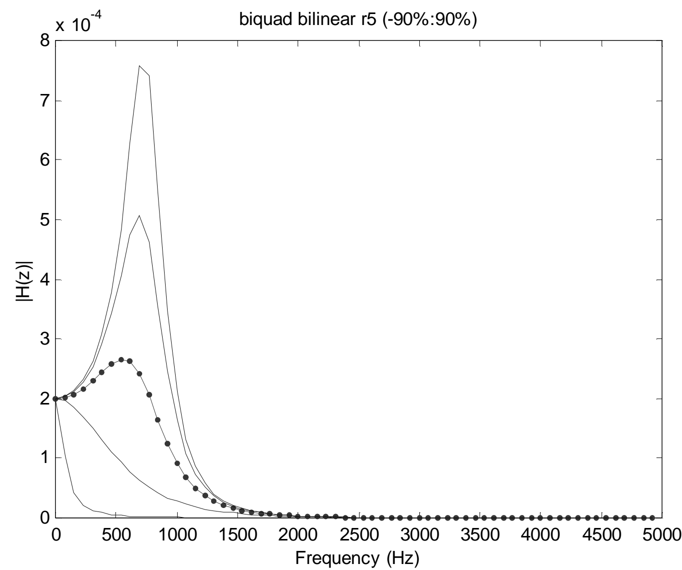


Figure 3.12: Frequency response of biquad filter after Q (quality factor) deviation from -90% to 90% from nominal value (NEGREIROS, 2003-b).

3.2.1.2 DUT output analysis

Sensitivity analysis (SLAMANI, 1995) was carried out for the DUT in order to verify what frequencies would be suitable for the test. For variations in the quality factor, changes in the component R5 were introduced and the largest frequency deviation from the nominal was recorded. For the biquad filter, the test signal at a frequency of 703 Hz presented the largest response deviations from the nominal values when the quality factor was changed.

The analysis of the DUT for the chosen test technique is based on the amplitude of the test frequency. No phase information was required. This evaluation can be carried out using spectral analysis of sampled data or by amplitude evaluation of the time-domain output signal waveform.

In this work a single-frequency test signal has been applied to the DUT. The signal-to-noise ratio (SNR) of the input signal was controlled during simulation. Gaussian noise was added to the sinusoidal test signal in order to obtain a previously specified SNR value. Spectral analysis has been carried out at the DUT output for testing purposes. The setup is presented in Figure 3.13. The ADC influence on test results will be discussed in the following sections.

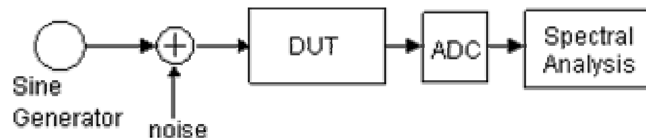


Figure 3.13: Complete test setup.

For simulation purposes, data has been sampled at 10 kHz. A maximum of 12.8k samples have been used to perform spectral analysis. A data window using 128 samples (with no overlap) has been used for analysis, providing 64 frequency zones. When using 12800 samples, averaging of FFT results is used in order to obtain the power spectrum density (PSD).

3.2.1.3 ADC model

The AD converter has been treated as an ideal quantizer (WANNAMAKER, 2000) and an amplitude limiting block, as illustrated in Figure 3.14. The amplitude limiter maintains the input signal in the amplitude range between -1 and 1. In order to simulate ADCs of different resolutions, different quantization steps are assumed for the same amplitude range. This way, a 16 bit converter has a quantization step of 2/2^16 and a 4-bit converter has a quantization step of 2/2^4.

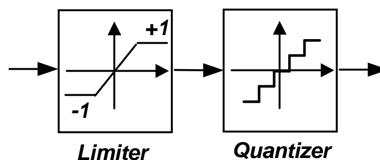


Figure 3.14: ADC model.

3.2.2 Results

Simulations were run in order to compare the results obtained for an ideal ADC (floating point) and from several other resolutions. The results are summarized in Figure 3.15. The figure shows the magnitude of the PSD of the DUT output obtained at the fixed test frequency of 703Hz. The quality factor of the DUT has been changed from -15 to 15% (in the figure) and the magnitude of the response, evaluated using several ADCs, was recorded. The number of samples was 12800 and the test signal SNR was 96dB.

Simulations using floating point, 16, 8 and 6 bits can not be distinguished in this figure. One should observe that a 1% variation in the quality factor of the DUT is detected by the output magnitude.

For the lower resolution converters (4 bits and lower), one can notice that the response is still monotonic, thus their response can be used in order to provide a test strategy. However, the thresholds should be adjusted for each converter. Even the 2 bits converter could be used in order to implement a test strategy. However, it is not able to provide resolutions of 1% in the quality factor, as observed in Figure 3.15.

Nearly identical results are obtained if the number of samples is lowered to 128 (while keeping the SNR as low as 48dB). This indicates a dependency between ADC resolution and maximum test sensitivity. The lower resolution converters are not able to follow the performance of their higher resolution counterparts.

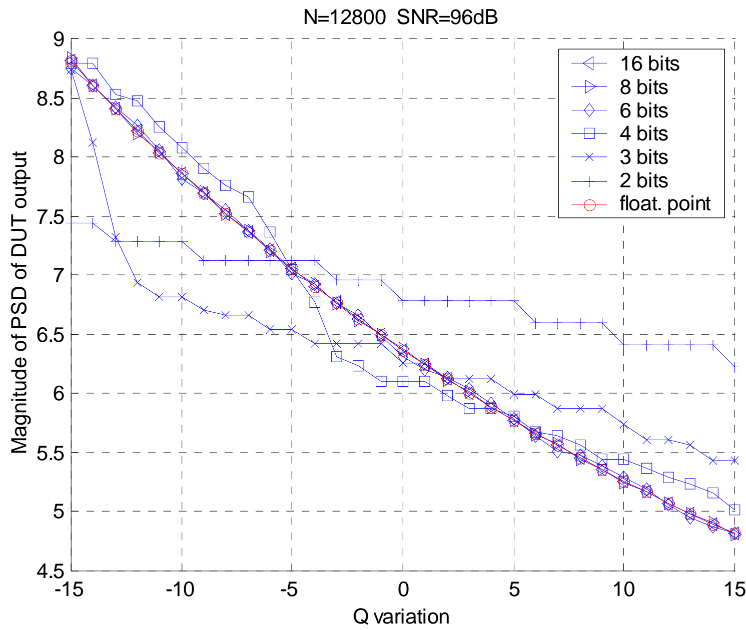


Figure 3.15: Spectrum magnitude at test frequency (703Hz) observed for different Q (quality factor) values and different quantizers (from 16 bit to 2 bit). Note that even the 2 bit converter gives a monothonic curve, thus allowing a test procedure to be implemented. The input signal has SNR of 96 dB and 12800 samples were used (NEGREIROS, 2005-b).

If the SNR of the input signal is decreased from 96dB to 20dB, the test sensitivity and linearity for lower resolutions ADCs is enhanced, as shown in Figure 3.16. This behavior is a result of the averaging operation used in the estimation of the PSD. One is able to compare Figure 3.16 to Figure 3.17, where no averaging was used due to the reduced number of samples.

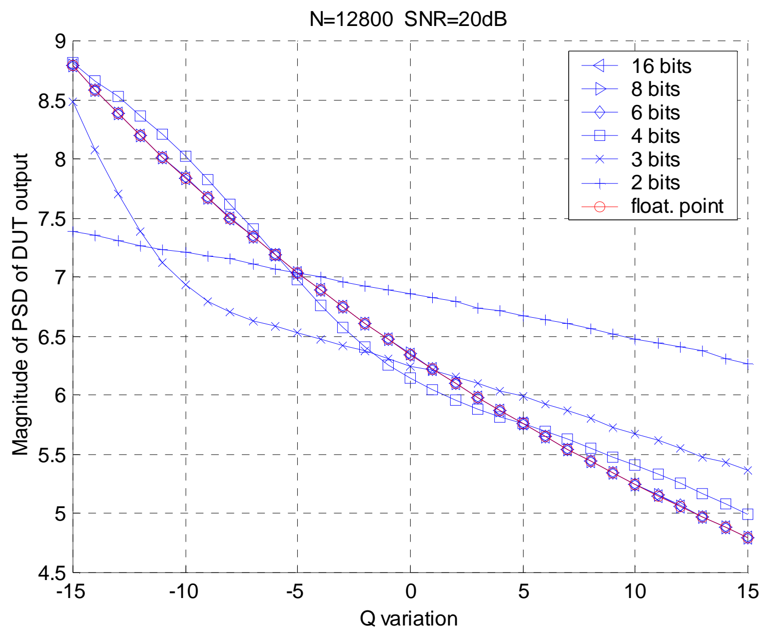


Figure 3.16: Effect of changing the input signal SNR from 96dB to 20dB. Lower resolution ADCs benefit from noise averages (NEGREIROS, 2005-b).

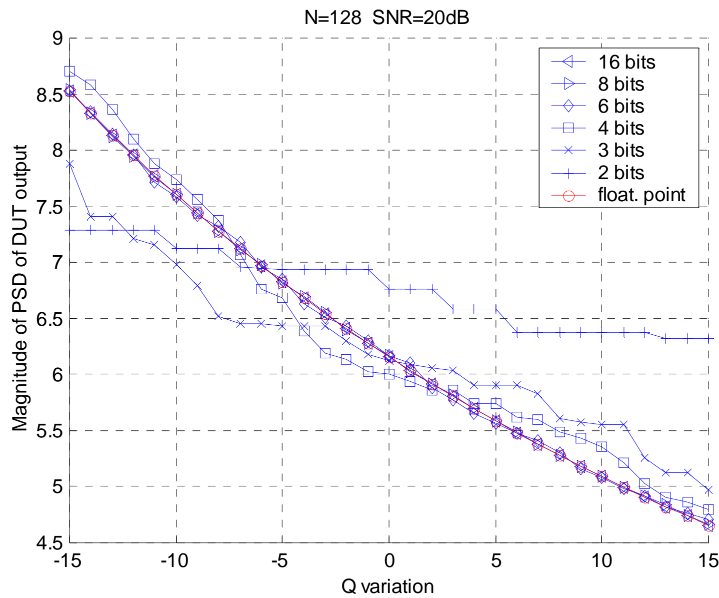


Figure 3.17: Effect of changing the input signal SNR from 96dB to 20dB, for 128 samples (no averages used due to the reduced number of samples) (NEGREIROS, 2005-b).

Lower SNR signals enable low resolution ADCs to benefit from noise averages. In extreme situations, there's no point in use a high resolution ADC, as illustrated in Figure 3.18.

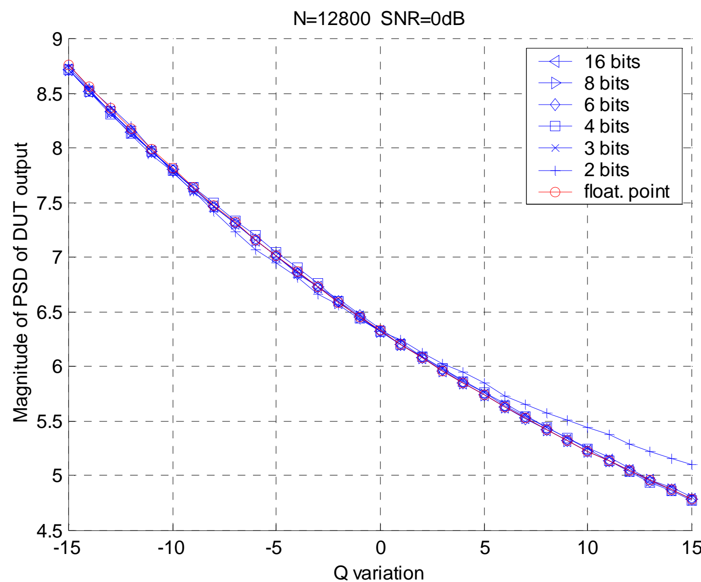


Figure 3.18: Effect of changing the input signal SNR to 0dB (NEGREIROS, 2005-b).

3.2.3 Discussion

As quantization effects are taken into account, test performance should be worsening for lower resolution. Although this is the general trend shown in Figure 3.15, it also shows interesting possibilities of developing test strategies with low resolution ADCs.

For high SNR situations, the lower resolution ADCs have decreased test sensitivity. Averaging can not help in this situation, as the noise level is too low. However, for

situations where a lower SNR is verified, the use of lower resolutions ADCs is able to achieve increased sensitivity if averaging is possible. The averaging operation implies in an increase in test time, so higher resolution ADCs would provide a faster test. For situations where the SNR is very low, the sensitivity of the test is the same for both high and low resolutions ADCs, as shown in Figure 3.18.

3.3 Conclusion

In this chapter two methods to reduce analog test costs were studied.

First, a test strategy based on spectral analysis was proposed. The power spectrum density estimate of the output of the analog system is used as a system signature, provided that the system is submitted to a random noise of known statistics as the input signal. The random noise generator is a very small circuit, incurring in a very small area penalty (FLORES, 2002; FLORES, 2004).

This test is suited to an implementation of BIST in a SOC environment, as it can use resources already present in the complete system and is purely digital. The overhead needed is the analog noise generator of known statistics. There is no need for an additional AD converter to sample the input signal.

The second part of this chapter analyzed the impact of reducing ADC resolution in an analog test example. It was verified that for a given test specification and SNR conditions, there is "the best ADC choice", that trades ADC cost by test speed and sensitivity.

In the next chapter we address the use of a digitizer that uses noise as the reference signal in order to develop analog test strategies.

4 THE STATISTICAL SAMPLER

In this chapter we analyze the application of a single bit digitizer to analog test. The proposed single-bit digitizer is comprised of only an analog voltage comparator with a noise reference. In the following, the theoretical background and applications to on-line test are developed.

4.1 The statistical sampler

The proposed statistical sampler is shown in Figure 4.1. It is composed by a voltage comparator and a white analog noise generator connected to one reference level. The input signal is connected directly to the input of the comparator. The digitized signal is obtained at the output of the comparator, which is naturally a digital output.

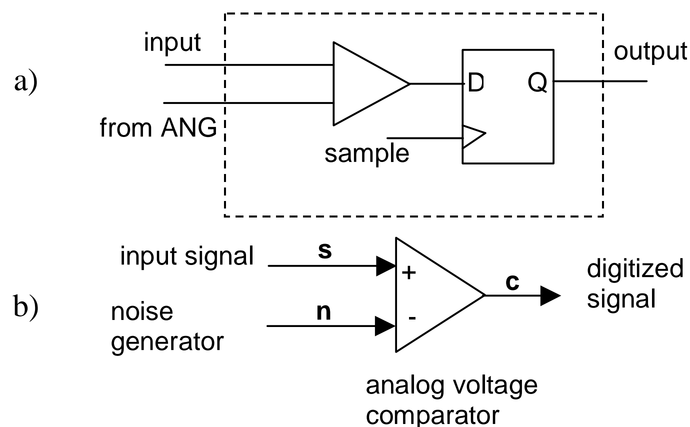


Figure 4.1: Statistical sampler: a) example structure and b) signal labels for mathematical analysis.

The amplitude of the noise should be greater than the amplitude of the input signal. In the following subsections it is shown that, although the input signal cannot be reconstructed from the digitized output, its second order statistics (autocorrelation and power spectra) can be recovered from the output. This is a key feature and allows the use of the proposed test strategy.

In the following subsections the sampler is analyzed. The comparator is shown to behave like an adder and a hard limiter. The formula relating the effect of the hard limiter over the statistics of the input signal is presented. As this input signal is the sum of two other signals, the statistical behavior of this sum is studied, and after the spectra of this sum is shown. The effect of adding noise to a sine wave is shown as an example.

4.1.1 Analysis of the proposed statistical sampler

The voltage comparator shown in figure 5 performs the function

$$c(t) = \begin{cases} +1, \text{if } s(t) > n(t) \\ -1, \text{if } s(t) < n(t) \end{cases} \quad (4.1a)$$

or

$$c(t) = \begin{cases} +1, \text{ if } s(t) - n(t) > 0 \\ -1, \text{ if } s(t) - n(t) < 0 \end{cases} . \quad (4.1b)$$

This is the same as having the subtraction of the input signal by the noise, and passing this through a hard limiter (PAPOULIS, 1991), as shown in Figure 4.2.

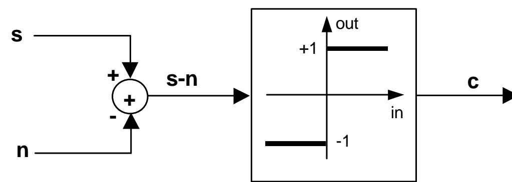


Figure 4.2: Decomposing the comparator into a (a) subtracter and a hard limiter (NEGREIROS, 2003-c).

According to Papoulis (PAPOULIS, 1991, equation 10-71, p.307), if the input signal, x(t), to a limiter is a normal stationary process with zero mean, the autocorrelation of the output, y(t), is given by

$$R_y(\tau) = \frac{2}{\pi} \arcsin\left(\frac{R_x(\tau)}{R_x(0)} \right) \quad (4.2)$$

which is known as the arcsine law. Equation 4.2 allows us to state that the statistics of the input signal will be at the output of the sampler. They will be at a different scale due to the multiplication by a constant and due to the effect of the arcsine function.

The linearity error for the arcsine function is shown in Figure 4.3. For small values of the input, the function is approximately linear.

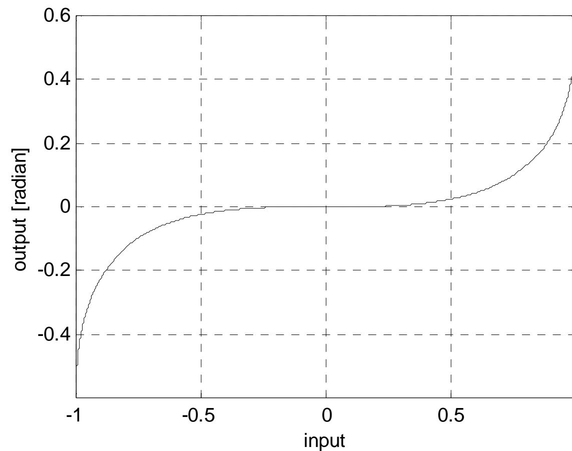


Figure 4.3: Linearity error for arcsine function (NEGREIROS, 2003-c).

4.1.1.1 Autocorrelation for a sum of two random processes

Assuming that $\{y_k(t)\}$ is a random process formed by the sum of two stationary zero mean processes $\{x_{1,k}(t)\}$ and $\{x_{2,k}(t)\}$, such that each sample function is given by

$$y_k(t) = a_1 x_{1,k}(t) + a_2 x_{2,k}(t) \tag{4.3}$$

where a_1 and a_2 are constants. If the processes x_1 and x_2 may be correlated, it can be shown that (BENDAT, 1986, example 5.3-p.116).

$$R_{yy}(\tau) = a_1{}^2 R_{x_1x_1}(\tau) + a_1 a_2 \left[R_{x_1x_2}(\tau) + R_{x_2x_1}(\tau)\right] + a_2{}^2 R_{x_2x_2}(\tau) \tag{4.4}$$

If the processes are independent and zero mean (which is the case in the sampler), then Equation 4.4 reduces to

$$R_{yy}(\tau) = a_1{}^2 R_{x_1x_1}(\tau) + a_2{}^2 R_{x_2x_2}(\tau) \, . \tag{4.5}$$

By equation 4.5 it is shown that the statistics observed at the input of the hard limiter will be the sum of the statistics of the white noise and the signal to be sampled. This sum will be scaled at the output of the sampler, according to Equation 4.2.

4.1.1.2 Autospectral Density Function for a sum of two random processes

According to Bendat (BENDAT, 1986), the autospectral density function is the Fourier transform of the autocorrelation function (BENDAT, 1986, eq. 5.27)

$$S_{xx}(f) = \int_{-\infty}^{+\infty} R_{xx}(\tau) \exp(-2j\pi f\tau)\, d\tau \, . \tag{4.6}$$

The one-sided autospectral density function is given by $(0 \le f < \infty)$

$$G_{xx}(f) = 2 \cdot S_{xx}(f) \, . \tag{4.7}$$

For a sum of two random stationary processes with zero mean, independent processes, then the one-sided autospectral density function is (BENDAT, 1986, example 5.7, p.129)

$$G_{yy}(f) = a_1{}^2 G_{x_1x_1}(f) + a_2{}^2 G_{x_2x_2}(f) \, . \tag{4.8}$$

Equation 4.8 shows that the PSD of both signals will also be scaled at the output of the sampler, according to Equation 4.2.

4.1.1.3 Effect of adding white noise to a signal

The autocorrelation function for white noise is given by (BENDAT, 1986, Table 5.1, p.114).

$$R_{xx}(\tau) = \frac{a}{2} \delta(\tau) \, , \tag{4.9}$$

and for a sine wave with amplitude A and frequency f_0, it is given by

$$R_{xx}(\tau) = \frac{A^2}{2} \cos(2\,\pi\, f_0\, \tau) \, . \tag{4.10}$$

These functions are presented in Figure 4.4. So the effect of adding white noise to a signal is to increase the value of the autocorrelation at zero lag. One can also see that

controlling the noise amplitude can be a way of making the hard limiter transparent to the autocorrelation of the composed input signal, as the linearity of the arcsine is better for a smaller ratio of autocorrelations (see Equation 4.2).

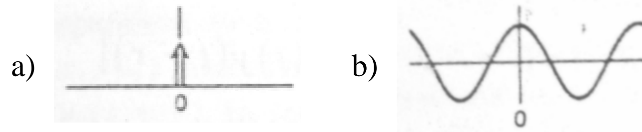


Figure 4.4: Autocorrelation functions for a) white noise and b) sine wave. (NEGREIROS, 2003-c).

4.1.2 Historical perspective and related work

The result shown in Equation 4.2, to the author's knowledge, was originally obtained by van Vleck in 1943 (VLECK, 1966; LAWSON, 1964).

The use of noise in analog to digital conversion is not a new subject. The use of low resolution quantizers to evaluate the correlation with good performance has already been recognized in the early work of Widrow (WIDROW, 1956; WIDROW, 1960) and has been used in the development of high frequency correlators (CASTANIE, 1974; ANDREWS, 1980).

The subject continues to receive attention in the signal processing community (KOLLÁR, 1984; WANNAMAKER, 2000) and also in other areas (related work has recently received interest in the literature under the name of stochastic resonance (GODIVIER, 1997; ANDO, 2001)).

The use of the statistical sampler as an AD converter has been addressed. A method to correct for the non-linearity has been developed and, the use of parallelism in order to increase resolution has been addressed in (SOUZA, 2004-a; SOUZA, 2004-b).

4.2 An on-line test strategy for analog circuits

Spectral analysis of discrete time series is a well studied subject (KAY, 1981; BENDAT, 1986). The estimation of the power spectrum density (PSD) is usually based on procedures employing the fast Fourier transform, being computationally efficient (KAY, 1981). In this chapter we propose the use of the PSD to allow the on-line identification of the transfer function of a linear system, as shown in Figure 4.5.

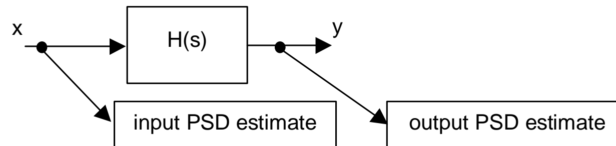


Figure 4.5: On-line PSD estimates required by the proposed test method (NEGREIROS, 2003-c).

The transfer function H(s) can be obtained, over the bandwidth of the input signal, by the ratio of the power spectrum of the output and input to the system, as shown in Equation 4.11.

$$H(s) = \frac{Y(s)}{X(s)} \tag{4.11}$$

The basic test idea is shown in Figure 4.6. In an earlier phase, the transfer function of the fault-free system is estimated for each point to be evaluated by the PSD. This is kept as the signature of the fault-free circuit.

During the testing phase, or under normal operation of the system, the ratio of the PSDs for the circuit under test is estimated and compared to the signature of the fault-free circuit. This ratio should be evaluated over the bandwidth of the input signal to the system, to assure that a suitable signal to noise ratio is achieved. The comparison can be tuned to allow specific frequency response needs, based on a set of comparison parameters.

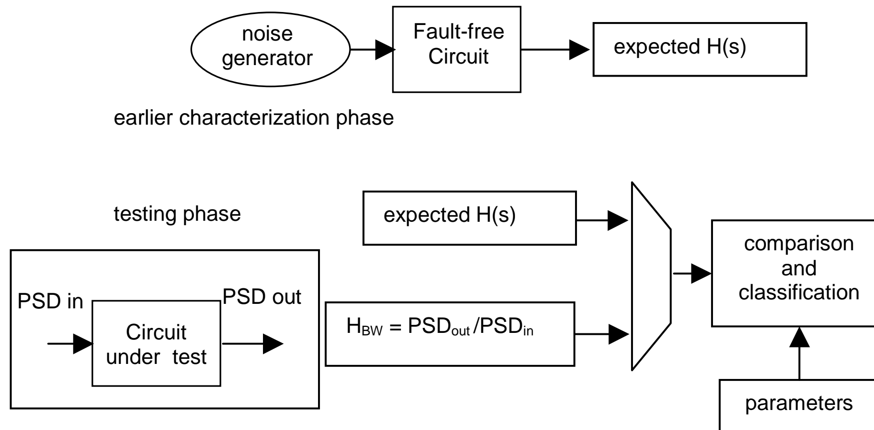


Figure 4.6: Test strategy using power spectral density (PSD) estimation (top: characterization phase; bottom: testing phase) (NEGREIROS, 2003-c).

4.2.1 On-line test example

In order to illustrate the performance of the proposed method, the biquad filter shown in Figure 3.5 was simulated using Matlab. A bilinear transformation (OPPENHEIM, 1989) of the circuit transfer function was used to obtain the circuit model.

4.2.1.1 Sine wave

The goal of this experiment was to perform an on-line test of the biquad, that could be receiving a sine waveform of 500Hz and amplitude 0.8. Noise is uniformly distributed with amplitude in the interval [-1,+1]. The waveforms for the input and output of the filter, and the input to the hard limiter are shown in Figure 4.7.

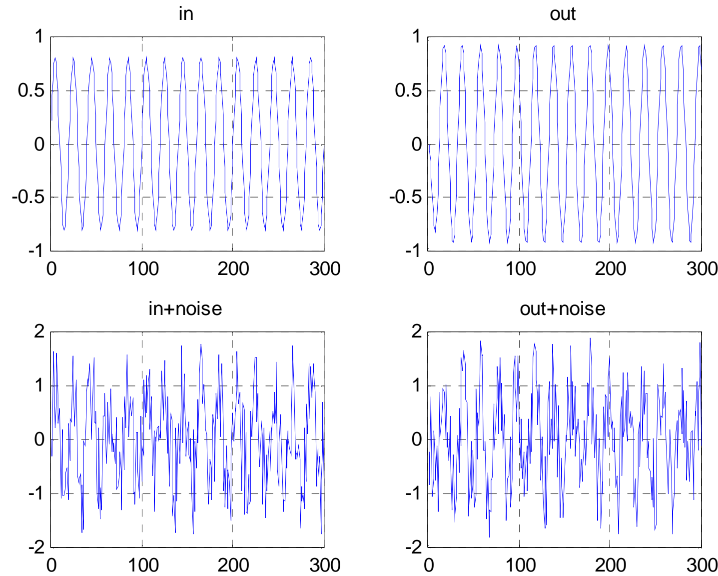


Figure 4.7: Waveforms for the test using a sine wave (NEGREIROS, 2003-c).

These signals were passed through the proposed statistical sampler, and the results obtained are shown in Figure 4.8. These plots show a good agreement between the PSD estimates before and after the statistical sampler.

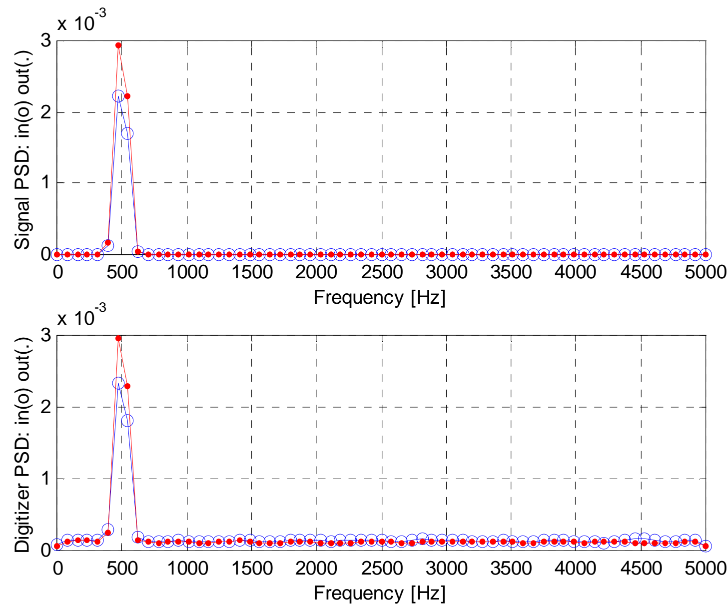


Figure 4.8: PSD estimate of the signals before (top) and after the statistical sampler (bottom) (NEGREIROS, 2003-c).

The PSD ratio obtained using the PSD estimates from the statistical sampler outputs is shown in Figure 4.9. These values were for various sine wave amplitudes. In this case, the biquad filter remained fault-free.

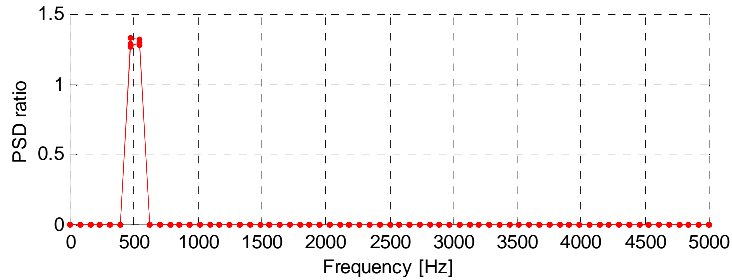


Figure 4.9: PSD ratio estimates for sine wave amplitudes from 0.5 to 0.9 (NEGREIROS, 2003-c).

The test is performed by introducing a variation of +50% and -50% in the capacitor C1. As shown in Figure 4.10, the PSD ratio obtained is clearly different from the fault-free case. The same sine wave amplitudes were used.

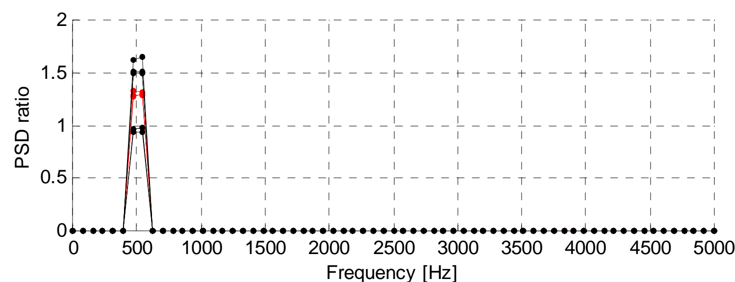


Figure 4.10: PSD ratio estimates for a variation in the capacitor C1 of +50% and -50%. (NEGREIROS, 2003-c).

4.2.2 Experimental Results

A photograph of the prototyped on-line test system for a biquad filter is presented in Figure 4.11. One signal generator was used for the 500 Hz sine wave, simulating the input of the biquad. The other generator was used as the noise source. The input and output of the biquad were sampled by the proposed statistical sampler, and the digital output of the sampler was acquired at 10kS/s. Data was transferred to a computer and analyzed using Matlab. The statistical samplers were implemented using standard voltage comparators.

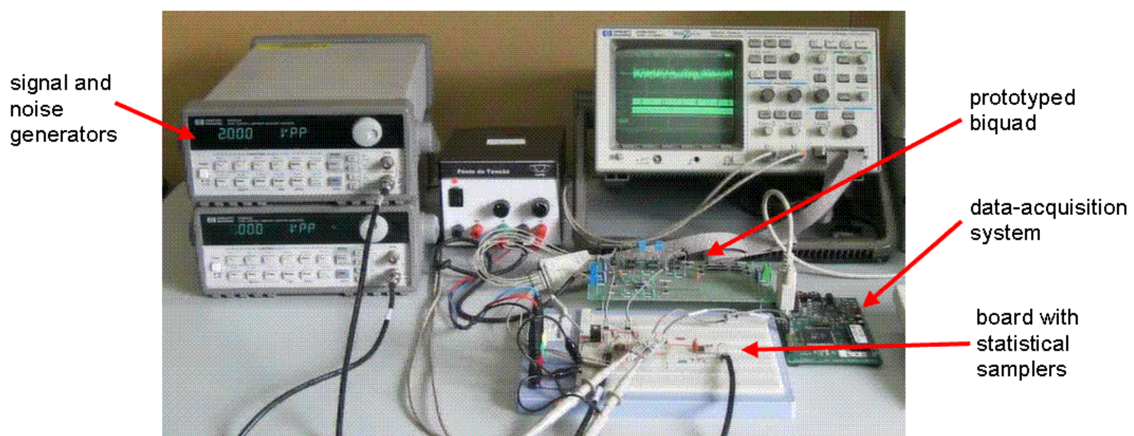


Figure 4.11: Photograph of prototyped system (NEGREIROS, 2003-c).

Figure 4.12 shows a scope screen image where the input to one of the samplers is presented by the two analog waveforms (channels A1 and A2). Channel A1 is noise and channel A2 is a 500 Hz sine wave. The remaining digital waveforms are the output of the two samplers (channel 0 and channel 1) and a trigger signal generated by the acquisition system (channel 2) each time an acquisition is performed.

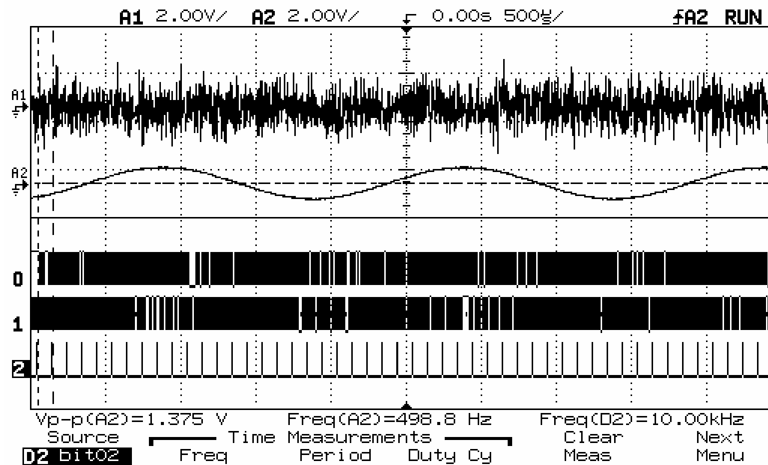


Figure 4.12: Captured scope image showing (A1) noise input to the sampler, (A2) sine wave at the second input to the sampler, (0) sampler "0" output, (1) sampler "1" output, (2) trigger signal showing the time where the output of the samplers is acquired (NEGREIROS, 2003-c).

Figure 4.13 shows the same scope screen image, but at a different time scale. In this figure one can see, by noting the two vertical lines, the time instants where the samplers outputs are acquired. Only digital information is acquired by the acquisition system, two channels at a time.

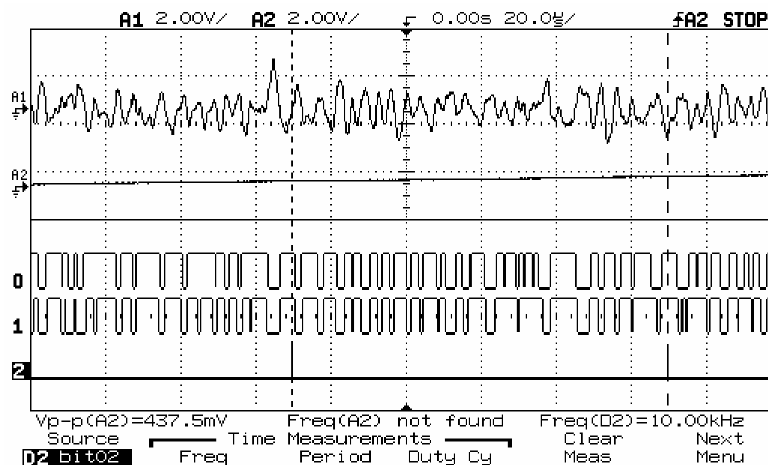


Figure 4.13: Captured scope image showing (A1) noise input to the sampler, (A2) sine wave at the second input to the sampler, (0) sampler "0" output, (1) sampler "1" output, (2) trigger signal showing the time where the output of the samplers is acquired. Note vertical lines showing the time instant when the outputs of the samplers are acquired (NEGREIROS, 2003-c).

The power spectrum estimates obtained from the sampler output signals (input [o] and output[.] of the biquad) for a fault-free biquad are shown in Figure 4.14.

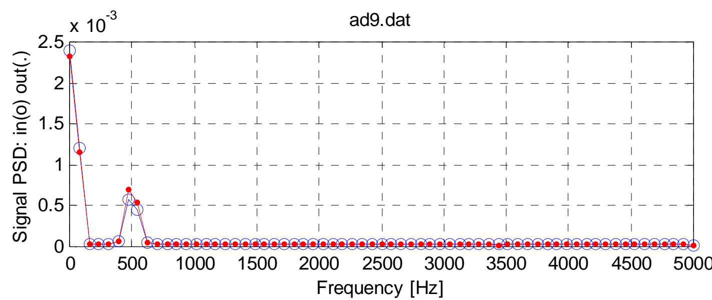


Figure 4.14: Power spectrum estimates for sampler output signals (input [o] and output[.] of the biquad), in a fault-free biquad (NEGREIROS, 2003-c).

Figure 4.15 shows the power spectrum ratio obtained for the fault-free biquad ("o") and the corresponding PSD ratio for a +50% and a -50% deviation in component C1 ("."). Note that this figure agrees with the simulation presented in Figure 4.10, disregarding the dc level represented by the initial points in the PSD.

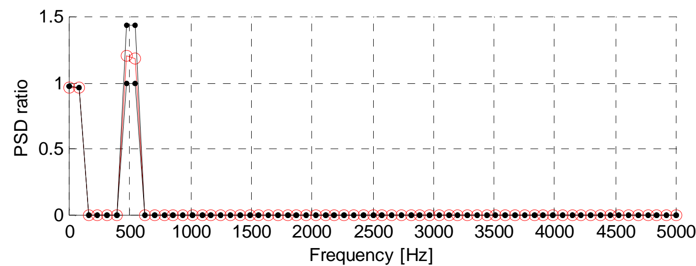


Figure 4.15: Measurement of power spectrum ratio estimates for the fault-free biquad (o) and for a +50% and a -50% fault inserted in component C1 (.) (NEGREIROS, 2003-c).

These power spectrum ratio estimates were used to verify the percent variation obtained when the discrete components of the circuit under test are deviated from their nominal value.

The PSD ratio deviation (evaluated at the indicated test frequency in Tables 4.1 to 4.4) is the percent value of variation in the PSD ratio from the nominal (fault free) case to the faulty case.

Parametric faults were introduced by modifying the nominal values from 20% and 50%. Catastrophic faults were introduced by opening and shorting the terminals of each tested component. Table 4.1 shows the results obtained by processing 12800 samples, and Table 4.2 presents results obtained after processing 51200 samples. As shown in the tables, all component variations have produced noticeable deviations from the nominal PSD ratio at the specified frequency.

Table 4.1: PSD ratio deviation from nominal(12,800 samples - 20% error in PSD estimates).

	-20%	-50%	+20%	+50%	open	short	freq[Hz]
C1	-9	-22	+13	+23	-37	-100	500
C2	+36	+141	-32	-56	-98	-87	1000
R1	-12	-59	+18	+22	-100	-93	500
R2	+48	+158	-34	-49	-92	-98	1000
R3	+55	+148	-26	-57	-90	-88	1000
R4	-42	-70	+52	+89	-55	-86	1000
R5	-29	-63	+15	+55	+170	-100	1000
R6	+25	+67	-17	-40	-94	+108	500

Source: NEGREIROS, 2003-c.

Table 4.2: PSD ratio deviation from nominal (51,200 samples - 10% error in PSD estimates).

	-20%	-50%	+20%	+50%	open	short	freq[Hz]
C1	-9	-18	+7	+21	-34	-100	500
C2	+36	+144	-35	-58	-98	-88	1000
R1	-20	-61	+12	+24	-100	-93	500
R2	+44	+151	-34	-52	-91	-97	1000
R3	+47	+149	-29	-56	-89	-88	1000
R4	-38	-71	+36	+92	-56	-87	1000
R5	-27	-64	+20	+49	+164	-100	1000
R6	+24	+66	-20	-41	-93	+110	500

Source: NEGREIROS, 2003-c.

In order to evaluate the tolerance range of the PSD ratio for fault-free circuits, a series of experiments using 12800 samples (for a 20% error in PSD estimates according to equation 2) and 51200 samples (for a 10% error in PSD estimates according to Equation 3.2) were performed for the frequencies used. The results are shown in Figure 4.16, and it is clear that even a fault free circuit will present a small ratio deviation due to the estimation errors in the PSD.

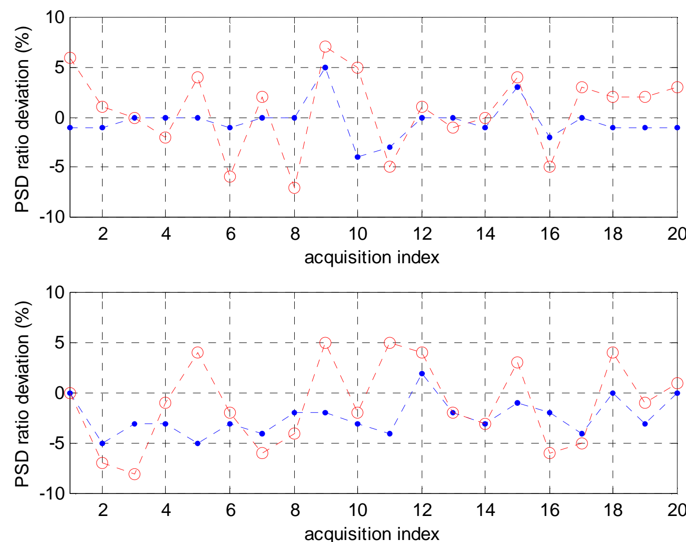


Figure 4.16: Measurement of power spectrum ratio estimates for the fault-free biquad at 500 Hz (upper plot) and 1000Hz (lower plot) using 12800 data points (marker 'o') and 51200 (marker '.') (NEGREIROS, 2003-c).

The influence of the test frequency on the fault detection is related to the transfer function of the linear system. If the fault causes a deviation in the transfer function at a frequency present in the input, this will be reflected at the output of the system. The

PSD ratio evaluation should be capable of detecting this deviation if it is large than the expected noise for fault-free circuits.

In another experiment, the proposed method was applied to the state-variable low pass filter specified in the ITC'97 analog benchmark circuits (KAMINSKA, 1997). The same experimental setup was used in this case. The power spectrum ratio estimates obtained after processing are shown in Tables 4.3 and 4.4.

Table 4.3: PSD ratio deviation from nominal (12,800 samples - 20% error in PSD estimates).

	-20%	-50%	+20%	+50%	open	short	freq[Hz]
C1	+19	+34	-18	-49	-4	-100	1100
C2	+43	+218	-37	-54	-98	-87	1100
R1	+25	+110	-15	-33	-87	+105	1100
R2	-30	-67	+31	+55	+29	-100	1100
R3	+31	+41	-16	-46	-100	-25	1100
R4	+68	+219	-28	-52	-88	-99	1100
R5	-25	-66	+32	+41	-100	-92	500
R6	+18	+46	-17	-24	-81	+79	700
R7	-16	-44	+12	+30	+85	-82	700

Source: NEGREIROS, 2003-c.

Table 4.4: PSD ratio deviation from nominal (51,200 samples - 10% error in PSD estimates).

	-20%	-50%	+20%	+50%	open	short	freq[Hz]
C1	+20	+38	-22	-46	-3	-100	1100
C2	+44	+214	-34	-54	-99	-87	1100
R1	+28	+98	-20	-36	-87	+98	1100
R2	-30	-66	+28	+56	+28	-100	1100
R3	+22	+42	-20	-44	-100	-28	1100
R4	+62	+212	-29	-54	-90	-98	1100
R5	-30	-67	+15	+36	-100	-93	500
R6	+17	+52	-15	-26	-81	+87	700
R7	-13	-42	+15	+33	+90	-80	700

Source: NEGREIROS, 2003-c.

To evaluate the tolerance range of the PSD ratio for fault-free circuits, a series of experiments were performed and the results are shown in Figure 4.17. One can note that a large data acquisition set will produce a less noisy PSD ratio estimate.

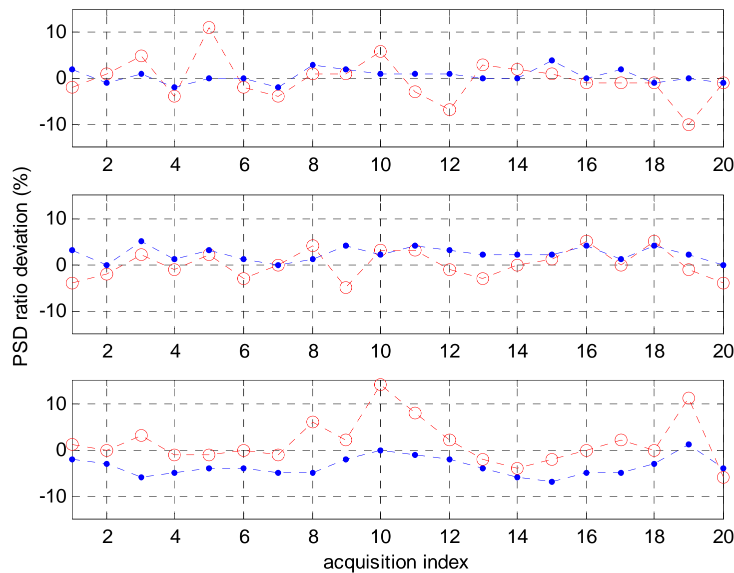
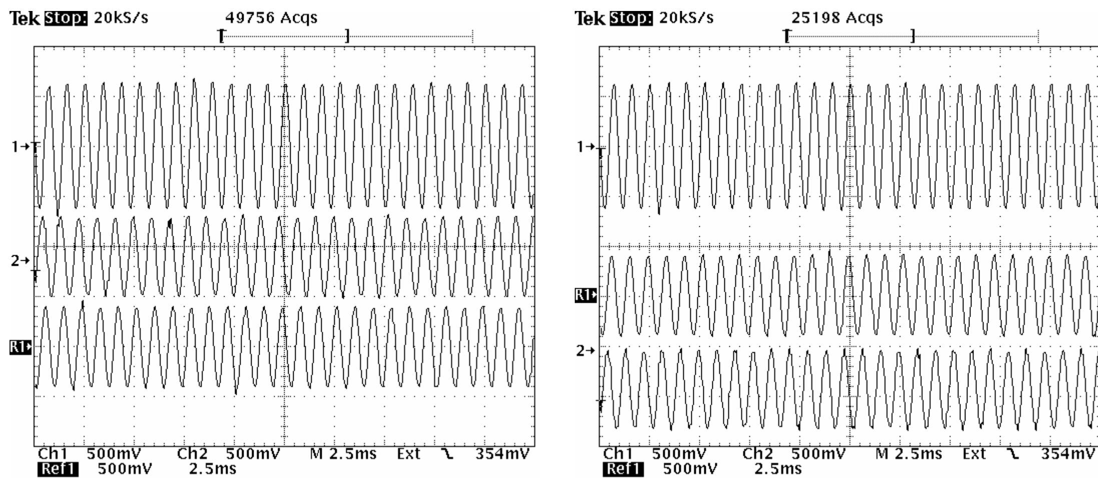


Figure 4.17: Measurement of power spectrum ratio estimates for the fault-free state-variable filter at 1100Hz (upper plot), 700Hz (middle plot) and 500Hz (lower plot) using 12800 data points (marker 'o') and 51200 (marker '.') (NEGREIROS, 2003-c).

In the presented case, a comment regarding the behavior for C1 and R3 should be done. In Figure 4.18 the scope' screen was captured and we can note that, as shown by the lower two plots (fault free response and faulty response), the amplitude of the output at the specified frequency has little changes. One can note that phase changes were observed and, in the case of R3, a dc level is present at the output. The phase change does not affect the PSD ratio for the specified frequency, as indicated in Table 4.3 and Table 4.4. For R3, the PSD ratio either does not indicate the large amount of dc.



(a) C1 open: phase change (b) R3 short: dc level and phase change

Figure 4.18: Scope' screen for the analysis of faults in (a)C1 and (b)R3 (NEGREIROS, 2003-c).

4.2.3 Analysis

The results shown in the preceding section indicate that a test strategy based on the power spectrum (PSD) estimate is feasible. The proposed statistical sampler has

permitted the evaluation of the power spectrum without the use of an AD converter, thus simplifying the problem of accessing test points in complex analog systems.

Although AD converters are expected to be present in a SoC, their availability is limited because the system is expected to be functional in an on-line test framework. The cost of AD converters is another limiting factor for the use of an on-line test scheme like the one presented, when compared to the statistical sampler. Furthermore, the statistical sampler provides a way to test partitioning without the use of switches and without introducing topological changes in the analog circuit.

The test time is an important issue, since it is directly related to the cost of the SoC. A BIST technique can be implemented using the proposed strategy. The test time will be related to the accuracy of the required PSD estimates. As an on-line strategy, any fault in the components affecting the transfer function of the system can be detected, once the input signal has frequencies over the affected frequency band. Latency will be related to PSD processing and data acquisition issues.

The limitations imposed on the input signal are that the signal should be a stationary zero mean process. This limitation does not impose a heavy constraint on the input signal like periodicity (HAFED, 2002). It suffices to the input signal to be stationary during the evaluation of the PSD estimates, and this time can be tuned according to the application.

The proposed technique is purely digital and has a low analog area penalty. The extra circuit required is an analog random noise generator and a sampler for each analyzed test point. This strategy also has a low memory overhead in the digital domain, as each sample of the signal uses only one bit. So, for a given 8-bits memory area, one can store 8 samples in each available word location, or 8 sampled signals in the same location. This is achieved at normal sampling frequency of the system, so no over-sampling is required.

As the output of a linear system is proportional to its input signal, the ratio of the PSD of the output signal by the PSD of the input signal gives the transfer function gain for the specific frequencies used. The signal to noise ratio must be evaluated during this calculation, as low amplitude signals can result in a high gain due to the division by a small number. A solution for this problem is to estimate the ratio for the bandwidth of the input signal, where a proper signal to noise ratio can be expected.

The signal to noise ratio can be a limiting factor for the application of the method to large bandwidth signals, as the amplitude of individual frequency components will become smaller than a signal with a single or a few frequency components. If the observed signal to noise ratio is low, it becomes difficult to establish a zone for the evaluation of the PSD ratio. For signals with a few components this is not an issue, as shown by the results presented in the previous section.

4.3 Increasing Analog Circuits Observability

This section discusses a method to increase the observability of analog circuits through the use of a statistical sampler. This sampler acquires statistical properties of the input signal. Its main advantages are simplicity, low analog area overhead and suitability to multi-channel acquisition, as only one bit samplers are used. This qualifies it for use in a System-On-Chip environment.

In order to provide test capabilities to a system, an expected behavior of the fault-free system should be known (predictability). This behavior can be described in terms of parameters, like a frequency response curve. Using spectral analysis, several parameters like amplitude and frequency can be estimated from a signal.

The statistical sampler can be used to perform spectral analysis of an analog signal. Due to the low area overhead, it is also suitable for multi-channel measurements, and could be used in a system as shown in Figure 4.19, where a core is shown allowing access to several analog test points in a circuit.

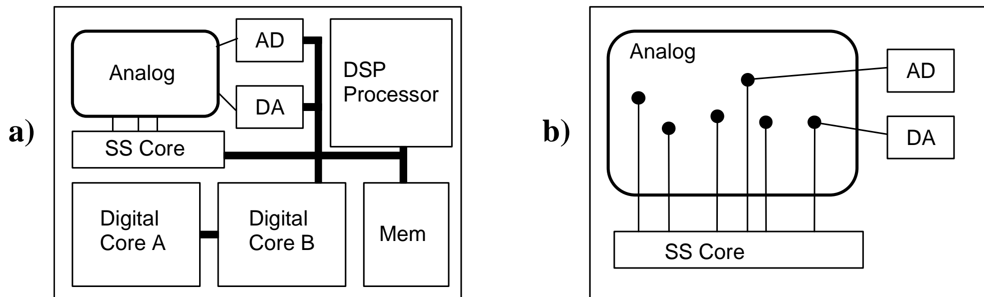


Figure 4.19: a) SOC example showing the statistical sampler (SS) core and b) details of multi-point measurements (NEGREIROS, 2002-a).

The structure of the statistical sampler core is shown in Figure 4.20, where a multi-stage analog circuit is being monitored as an example. As the measurement is not restricted to a particular kind of signal, an on-line test strategy could also be devised using this approach.

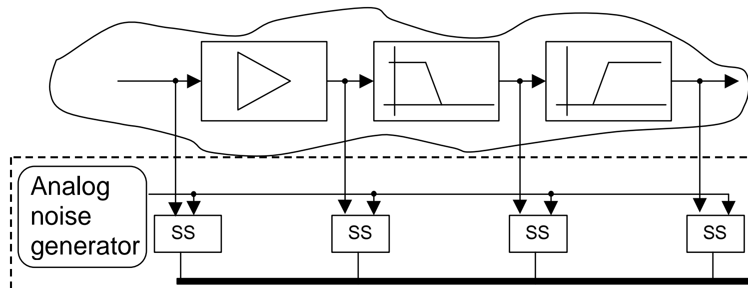


Figure 4.20: Structure of statistical sampler core for multi channel measurement (NEGREIROS, 2002-a).

4.4 An analog test framework

In this section we propose the development of an analog test core based on the statistical sampler, using test strategies based on the power spectrum density.

In chapter 2 we observed that analog test solutions that allow BIST and on-line test simultaneously are rare (only for fully differential circuits). It was also noted that BIST schemes proposed so far are not designed to allow the tested circuit to be in normal operation. The reasons for that are diverse: in order to do the test without a signal generator, the oscillation-based test technique (ARABI, 1997) converts the circuit into an oscillator; in order to evaluate the circuit response, most test strategies (HAFED, 2002; SLAMANI, 1995) forces the input signal to a specific one; some of them use resources present in the system to perform the test, like the pseudorandom technique (OHLETZ, 1991).

A framework for analog test in the System on a Chip context is presented in Figure 4.21. Several analog and mixed-signal cores could be tested if a test core (or wrapper) could be implemented close to the core under test. Test data provided by the test core should be digital in order to allow the reuse of system resources, like memory and processing capability, so the test core is shown connected to the system bus.

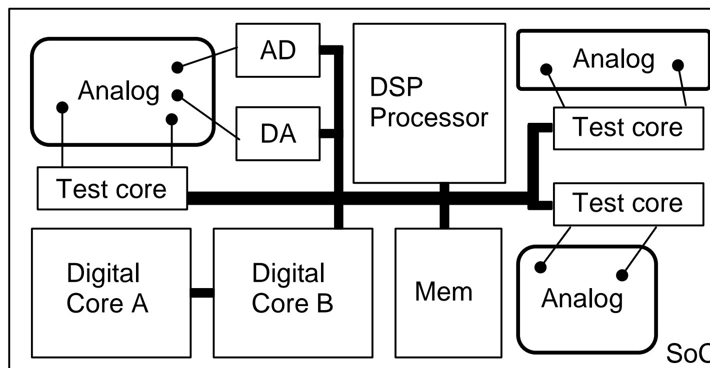


Figure 4.21: Analog test framework for the SoC environment

For the implementation of most BIST methods like (SLAMANI, 1992; OHLETZ, 1991; HUYNH, 1998), test core requirements are the generation of an input signal to the analog core and the acquisition of the output waveform, as the processing can be made by other system resources. Test automation can be achieved by replication of test cores in the SoC.

The last approach is used in the test core proposed in (HAFED, 2002). This core is able to generate and sample periodic signals, achieving low analog area overhead by using digital signal processing techniques like oversampling and noise-shaping in the implementation of the signal generator and digitizer. It also allows reuse of SoC resources by the test. As noted in chapter 2, this solution is not suited to on-line test, because the digitized signals need to be periodic and synchronized to the generator. Also, the time needed to perform the acquisition and memory requirements for high resolution measurements can impact the performance and applicability of this implementation.

Test core requirements to implement on-line analog test methods do not include the signal generator, as the SoC system will be in normal operation mode, and the analog cores will have their own signals. The simultaneous acquisition of several analog inputs is desirable, as it allows the partitioning of the test for larger analog cores. Reuse of system resources is still desirable in the SoC environment, and the proposed approach allows reuse of memory and processing resources available. If there are no resources available, a specific test memory and processing core could be added, as in Figure 4.22. As test data is digital, the system data bus can be used to transfer test data to the test processor. To increase test data transfer speed and reduce test data transfer overhead from the system bus, a dedicated data bus could also be used (see Figure 4.22).

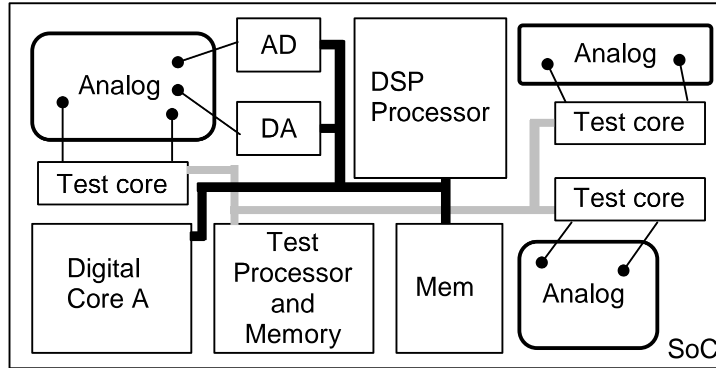


Figure 4.22: Analog test framework with dedicated test processor core and test data bus.

On-line test methods based on analog replication (LUBASZEWSKI, 1995), continuous checksums (CHATTERJEE, 1993) and analog checkers (LUBASZEWSKI, 2000), are circuit specific and need specific modifications in the analog core. The digitizer of the test core could be used to perform the acquisition of the analog test result (as the analog checksum, for example).

An example implementation of the test core could be as shown in Figure 4.23. The signal generator is used only for BIST. For on-line test, the input signal of the system should provide adequate excitation, if properly monitored.

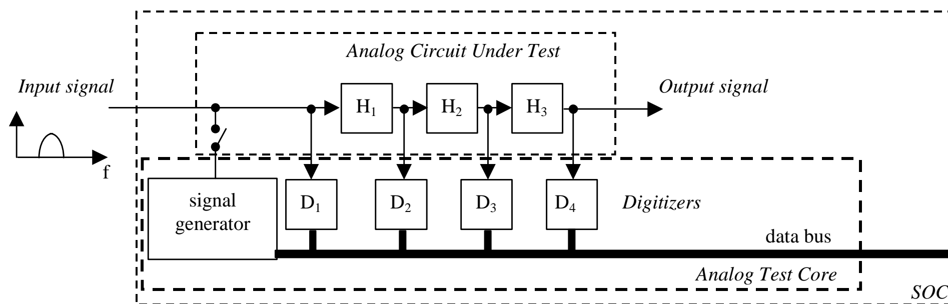


Figure 4.23: Test core structure example.

4.4.1 An approach to the analog test problem in the SoC environment

The approach depicted in Figure 4.23 for on-line test, allows the evaluation of the transfer function of every analog block, by evaluating $H_i(f)=Output_i(f)/Input_i(f)$ ($i=\{1,2,3\}$) for every frequency f in the input signal band. The cost of the digitizer is associated with requirements in the measures like sampling frequency, input bandwidth, signal to noise ratio and resolution. These requirements, on the other hand, are strongly related to adopted test method, to the specifications of the circuit under test and to what characteristics are being measured and observed in the test.

Analog test methods based on PSD estimates are well suited for the framework depicted in Figures 4.21 and 4.22., and could benefit from an analog test core as the one in Figure 4.23. We propose the implementation of a test core structure based on the statistical samplers presented in the last chapter, as shown in figure 4.24, where an additional analog noise generator for use with the statistical samplers is included. Analog test methods developed in chapters 3 and 4 can be used with the proposed samplers.

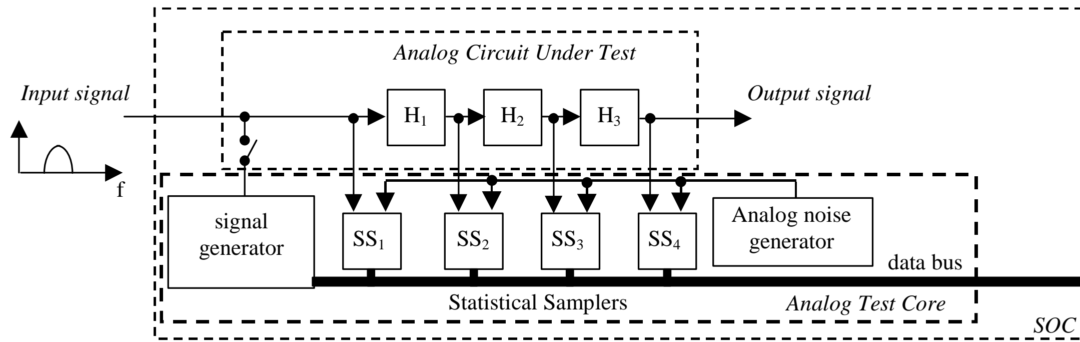


Figure 4.24: Test core example using statistical samplers.

4.5 Conclusion

In this chapter the statistical sampler was presented, and a mathematical analysis of its behavior has been developed. Although the input signal itself cannot be reconstructed, the sampler can be made transparent to the statistics of the input signal. This way, test methods based on spectral analysis (like the one presented in Chapter 3) can be employed with this sampler.

A new test strategy based on spectral analysis was proposed in this chapter. The power spectrum density estimates of the input and output of an analog linear system is sampled, and a transfer function estimate is obtained on-line. The obtained estimate is compared to a previously obtained reference transfer function, thus allowing the on-line detection of variations.

This chapter also focused on a method to increase the observability of analog circuits by the use of a statistical sampler. The suitability to analog test implementation in the SOCs environment was discussed and an analog test framework based on a statistical sampler core was suggested.

In the next chapter we apply this sampler in analog test strategies using noise as the input signal to the CUT, also called pseudorandom testing. This way, no reference waveform is needed, and there's no need for an additional signal generator for the sampler.

5 PSEUDORANDOM TESTING

In this chapter we use the statistical sampler in the framework of pseudorandom testing, or analog test using (pseudo)random noise as the input signal to the circuit. Using noise as the input signal to the statistical sampler is advantageous, in the sense that no reference signal is needed. The mathematical framework developed in the last chapter, however, can be applied, as it is a simplified case. This allows the implementation of the lowest cost test solution possible: only a single bit ADC and DAC. The noise generator and the test response analyzer are completely digital: the noise is output through a single bit DAC and the test response analyzer is fed with a single bit stream from a comparator.

In the next sections we develop this framework. First, a mathematical background is presented in section 5.1. In section 5.2 the effect of using a single bit DAC in the implementation of the signal generator in the pseudorandom testing is studied. In section 5.3, we analyze the effects of a single bit ADC. The chapter finishes with a test solution comprised of both approaches, the "ultimate low cost" analog test.

5.1 Previous work

The lack of general test strategies for analog circuits has caused the appearance of solutions targeted to specific circuits or classes of circuits, like the oscillation-based technique (ARABI, 1997; HUERTAS, 2000). Other test approaches are based on sensitivity analysis and the use of sinusoidal input frequencies (SLAMANI, 1992; HAMIDA, 1993). Although the latter techniques do not require a modification in the circuit topology, the choice of the input vector is an issue, and a complete characterization of the frequency response of the circuit can not be obtained without a time-consuming frequency sweep.

The use of pseudorandom noise to test analog circuits in a BIST scheme was proposed in (OHLETZ, 1991). This approach uses the DA and AD converters of the system to generate and capture test data. The analysis is performed by the digital processor of the system.

The use of noise as an input vector to a circuit provides a way to characterize a linear analog circuit. Noise can also be used to characterize the full bandwidth of the circuit without the need to verify specific frequencies.

Other approaches following (OHLETZ, 1991) targeted an improvement in test quality by using different methods to classify the circuits. In (PAN, 1997) the same framework was used, but the signature of the circuit is based on samples of the autocorrelation function. In (TOFTE, 2000) the same method in (PAN, 1997) is characterized using more samples of the autocorrelation function.

In (MARZOCCA, 2002) the autocorrelation is used to obtain estimates of the impulse response of the circuit, which is used as a signature, and a signature bank is used to improve the classification. This work reports the use of two-level random noise to generate the stimuli for the analog circuit, thus it does not require a DA.

All pseudorandom approaches have reached the required number of samples to perform the test based on simulation or experimental criteria.

In this work we highlight the need for a careful examination of the estimation errors when processing random noise, and we provide the mathematical expressions for the number of samples required for a given error in the estimated parameter, needed in *any* technique that uses noise.

Furthermore, we substitute the DA converter by an analog noise generator and the AD converter is replaced by a simple low cost digitizer with low area overhead, enabling an ultra low cost test.

5.2 Pseudorandom test based on PSD estimation

The use of noise allows one to fully characterize a linear analog system in contrast to sinusoidal measurements that need a frequency sweep in order to cover the frequency range of interest, which is a time-consuming operation. In Figure 5.1, time and frequency domain measurements for stochastic signals are presented for a linear system. R_{xx} stands for the autocorrelation of the signal "x". R_{xy} stands for the cross-correlation of the signals "x" and "y". G_{xx} is the power spectrum density (PSD) of the signal "x" (the Fourier transform of R_{xx}).

The magnitude of the transfer function can be obtained by

$$|H(f)| = \frac{G_{xy}(f)}{G_{xx}(f)} \tag{5.1}$$

and the magnitude squared of the transfer function can be estimated by

$$|H(f)|^2 = \frac{G_{yy}(f)}{G_{xx}(f)} \tag{5.2}$$

For noise, $G_{xx}(f)$ is a known constant value, and then only $G_{yy}(f)$ is needed in order to obtain $|H(f)|$.

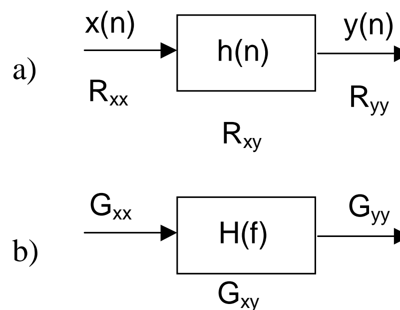


Figure 5.1: Definitions for stochastic signals in the a)time domain and b)frequency domain.

Noise-based testing approaches like (MARZOCCA, 2002; TOFTE, 2000) used time-domain quantities, like correlation, in order to obtain a signature for the circuit. In this work we use the PSD to derive a signature to the circuit.

5.2.1 Pseudorandom test based on PSD

The method proposed in section 3.1 is used here, and illustrated in Figure 5.2. In the training phase, random noise with known statistical characteristics is applied to the input of the fault-free circuit, and the power spectrum density of the output is estimated. This is kept as the signature of the fault-free circuit. In the testing phase, the PSD of the circuit under test is estimated and compared to the signature of the fault-free circuit.

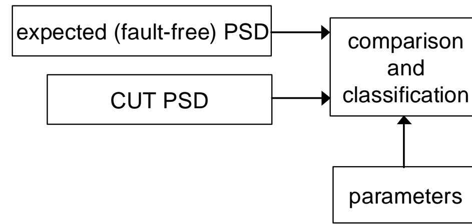


Figure 5.2: Test strategy using PSD estimates (NEGREIROS, 2003-d).

The comparison is based on the distance from the reference PSD. This distance is evaluated using the mean value of the squares of the difference "A" (see Figure 5.3), and Equation 5.3 expresses it mathematically (parameter par_mean from section 3.1) .

$$d = \frac{1}{N_{freq}} \sum_{f=Fmin}^{Fmax} (Estimated_PSD(f) - Reference_PSD(f))^2 \qquad (5.3)$$

A comparison threshold is defined calculating the parameters for the error limit curves, as indicated by the distance “B” in Figure 5.3 and expressed in Equation 5.4 bellow.

$$d_t = \frac{1}{N_{freq}} \sum_{f=Fmin}^{Fmax} (Error_limit_PSD(f) - Reference_PSD(f))^2 \qquad (5.4)$$

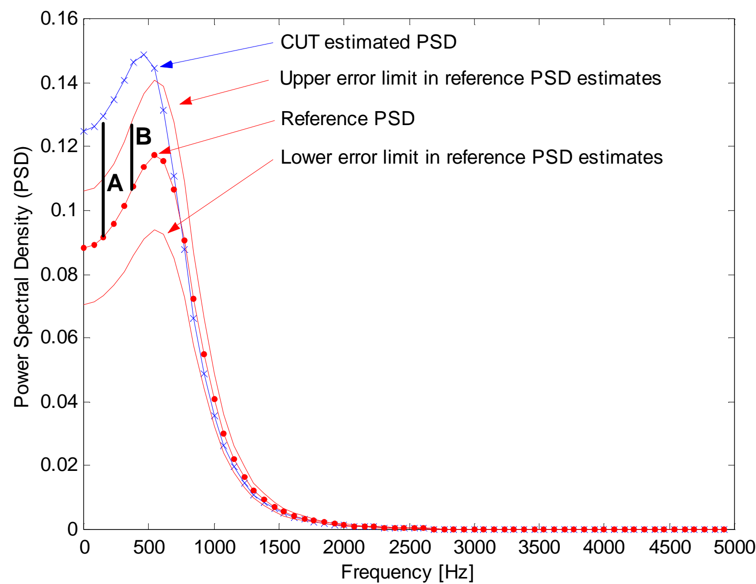


Figure 5.3: Reference PSD and estimated PSD (NEGREIROS, 2003-b).

5.3 Pseudorandom test using Binary Noise

Many test methods for analog circuits are based on the application of an input signal and the analysis of the output of the system. The stimuli generator must be included in the core for an effective BIST strategy. The generation of high quality analog signals may be costly and difficult, so a simple signal generator is desirable. Furthermore, the use of analog area is undesirable because of the sensitivity of the analog components to variations in the fabrication process, which could lead to a decrease in signal quality. This makes it desirable to reduce the analog area use to a minimum, favoring digital techniques.

In this section, we use a test strategy based on the estimation of the power spectrum density (NEGREIROS, 2003-a). As it will be shown, this test scheme can be used with binary noise sequences with minimal or no degradation, thus eliminating the need for a complex signal generator. Only a two-level analog signal is needed (like $+V_{dd}$ and $-V_{dd}$), which could be controlled by a processor or a logic circuit, thus reducing the generator cost. Although the idea of using binary sequences in pseudorandom testing is not new (MARZOCCA, 2002), issues like sequence length, statistical behavior of the signature parameters and mathematical background have not been addressed.

5.3.1 Amplitude quantization effects on noise

The effect of quantization of analog signals is commonly expressed as the addition of noise, so the signal to noise ratio of the acquired signal depends on the number of bits of the quantizer (B), as expressed by Equation 5.5 (OPPENHEIM, 1989, eq. 3.113).

$$SNR = 6 \cdot B - 1.25 \text{ dB} \tag{5.5}$$

The development of such expression is based on assumptions like small quantizer steps, also called fine quantization (KOLLÁR, 1984). For the case of rough quantization (like one bit) and large quantizer step, this model does not apply, as the signal to noise ratio is very low.

In Figure 5.4 we present a simplification that can be made on the signal generator. The idea is expressed using analog blocks: the output of a gaussian random noise generator is passed through a comparator. In the SoC environment, this would be replaced by a digital generator block, followed by an analog buffer.

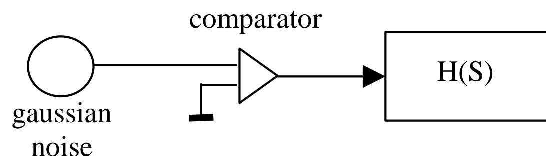


Figure 5.4: The noise generator.

If we consider the quantization of gaussian signals, the problem of coarse quantization has already been addressed, and the analysis presented in section 4.1.1 applies here. The voltage comparator behaves like a hard-limiter. Thus, the autocorrelation results from section 4 apply here also, as expressed by Equation 5.6.

$$R_y(\tau) = \frac{2}{\pi} \arcsin\left(\frac{R_x(\tau)}{R_x(0)} \right) \tag{5.6}$$

In this case, R_x is the autocorrelation of the noise before suffering the 1-bit quantization. As the power spectrum density is the Fourier transform of the autocorrelation function, Equation 5.6 allows us to state that the spectrum of the one-bit quantized noise will be proportional to the spectrum of the original signal. The following reasoning explains this point: as only $R_x(0)$ is (theoretically) nonzero for white noise, the argument for Equation 5.6 is normalized to $R_x(0)=1$. Thus, the non-linear function only scales the original autocorrelation function. This point is illustrated in the following section.

5.3.2 Results

In order to verify the theoretical results presented in the previous section, we have simulated in Matlab the application of gaussian noise to a band pass filter, using floating point input signal and single-bit quantized input signal. The evaluation of the PSD for the input and output of the system is shown in Figure 5.4. As it can be seen in the upper plot showing two level quantized and unquantized gaussian noise, no significant difference is noted when the two-level analog signal is applied.

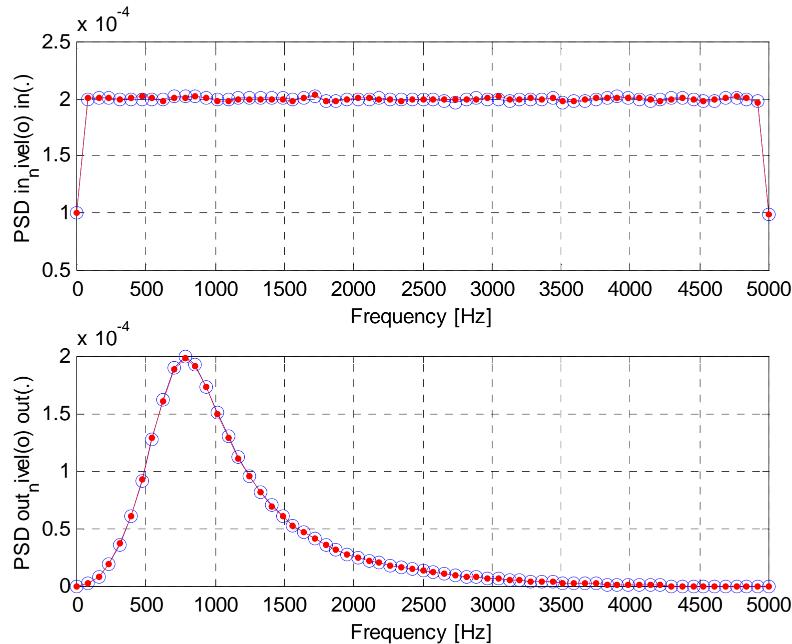


Figure 5.5: PSD evaluated for multilevel and two-level quantized gaussian noise. Input (top) and output (bottom) of band pass filter (NEGREIROS, 2003-d).

5.3.3 Experimental test

In order to evaluate the performance of the PSD-based test method using binary sequences, an experimental setup was built according to Figure 5.6. The arbitrary waveform generator was programmed with multilevel and two-bit gaussian noise, both created using Matlab. The generator was adjusted so that output frequency is about 8kHz, the same frequency used in the data acquisition system. The device under test (DUT) is the state-variable filter from the ITC'97 analog and mixed-signal benchmark circuits, shown in Figure 5.7 (KAMINSKA, 1997).

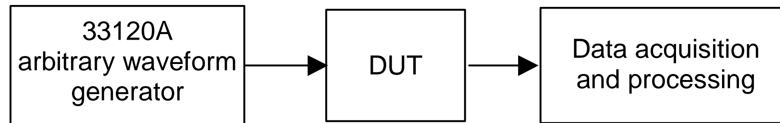


Figure 5.6: Experimental setup (NEGREIROS, 2003-d).

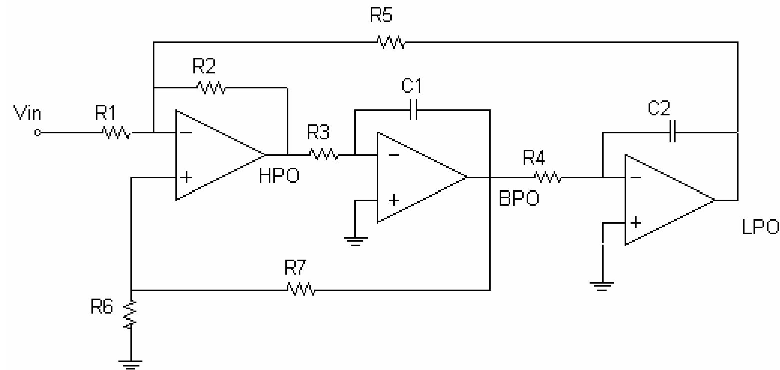


Figure 5.7: State-variable filter.

In Figure 5.8 the input signal to the filter is shown, as long as the output response. Note that the smallest noise pulse has duration of about 1/8000 s. The data acquisition was made using 16 bit samples.

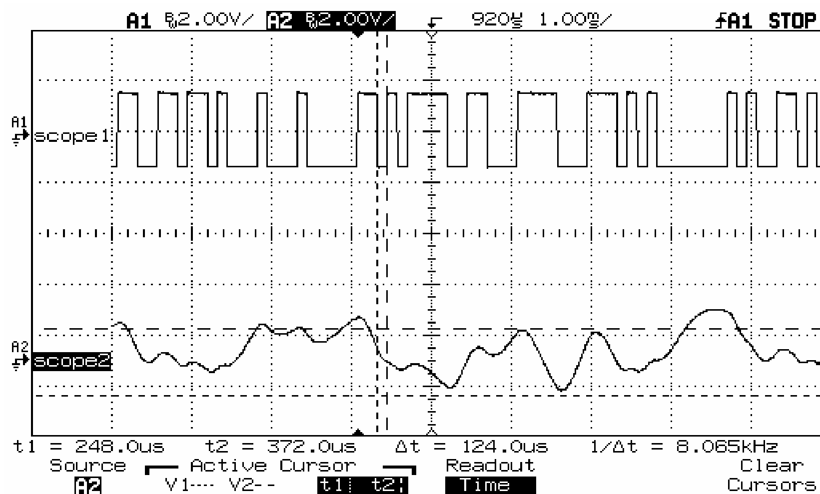


Figure 5.8: Binary noise (scope1) and filter output response (scope2) (NEGREIROS, 2003-d).

Table 5.1 presents test results obtained when using multilevel gaussian noise as the input signal. Some soft faults are not detected in this case. In Table 5.2, the results obtained for binary quantized gaussian noise are shown. As one can see, the tables are very similar, as all hard and large deviation faults are detected. Also, only soft faults in component R7 are not detected, in comparison to the multilevel case.

Table 5.1: PSD distance measured for 20% error in the PSD estimates using multilevel input signal (12800 points, threshold: 1.8e+7, marked cells indicate no fault detected).

	-50%	+50%	-20%	+20%	OPEN	SHORT
C1	3.1e+7	4.1e+7	**6.5e+6**	**6.1e+6**	4.4e+8	9.3e+7
C2	5.4e+8	6.8e+7	3.1e+7	2.0e+7	4.4e+8	7.2e+9
R1	2.0e+9	1.1e+8	1.2e+8	2.3e+7	6.3e+10	4.4e+8
R2	6.8e+7	2.3e+7	**1.0e+7**	**4.4e+6**	4.4e+8	8.3e+7
R3	3.5e+7	3.6e+7	**8.7e+6**	**5.6e+6**	9.3e+7	4.4e+8
R4	5.3e+8	6.1e+7	5.3e+7	**1.2e+7**	1.8e+8	4.4e+8
R5	2.4e+8	3.1e+8	5.5e+7	4.0e+7	4.4e+8	1.8e+11
R6	3.8e+8	3.8e+7	2.7e+7	**8.7e+6**	8.4e+10	2.6e+8
R7	7.8e+7	9.8e+7	2.2e+7	**1.3e+7**	2.5e+8	9.1e+10

Source: NEGREIROS, 2003-d.

Table 5.2: PSD distance measured for 20% error in the PSD estimates using single-bit quantized input signal (12800 points, threshold: 2.2e+8, marked cells indicate no fault detected).

	-50%	+50%	-20%	+20%	OPEN	SHORT
C1	4.4e+8	6.0e+8	**8.9e+7**	**1.3e+8**	5.4e+9	1.1e+9
C2	4.8e+9	9.4e+8	3.1e+8	2.5e+8	5.4e+9	5.1e+9
R1	8.3e+9	1.3e+9	1.2e+9	3.2e+8	2.2e+10	5.4e+9
R2	8.9e+8	2.8e+8	**1.7e+8**	**1.1e+8**	5.4e+9	1.1e+9
R3	4.2e+8	4.2e+8	**8.9e+7**	**1.3e+8**	1.2e+9	5.4e+9
R4	6.6e+9	7.6e+8	5.7e+8	**1.6e+8**	3.2e+9	5.4e+9
R5	3.1e+9	3.3e+9	6.9e+8	5.6e+8	5.4e+9	6.4e+10
R6	3.6e+9	4.7e+8	4.2e+8	**1.3e+8**	4.9e+10	3.3e+9
R7	9.3e+8	1.2e+9	1.4e+8	2.3e+8	3.2e+9	4.6e+10

Source: NEGREIROS, 2003-d.

5.3.4 Analysis

The use of the PSD-based testing technique was applied in the previous section in both simulation and practical experiments. It was noticed that the coarse quantization of the gaussian input signal doesn't impact significantly on the PSD estimates results. In the proposed test technique, the test is performed based on a distance parameter. The reference distance should be evaluated using the appropriate signal for each case.

The experimental setup used the same sampling and output frequency for the acquisition and generation of signals. This allowed the analog circuit to have enough time to respond to excitation signal, and has permitted the acquisition of the system dynamics with a low sampling rate data acquisition system. The threshold levels in Tables 5.1 and 5.2 are different mainly because the analog noise levels were changed in each case. Also, both signals were applied without a DC level, like a zero mean gaussian noise. The data acquisition system also was ac coupled.

In the experimental measurements, the results shown in Tables 5.1 and 5.2 are very similar, and this indicates that the use of simple test sequences is feasible. Also, as the PSD methods are sensitive to estimation errors, the result obtained regarding component R7 does not imply in a worse performance for the single bit quantized noise. This could also be the result of a small data record for obtaining the PSD estimates.

5.4 Ultra Low Cost Analog BIST using Spectral Analysis

In this section we analyze the effects of using a simple and low cost 1-bit digitizer to capture analog information from pseudorandom test.

5.4.1 PSD-based test using one-bit samples

The structure shown in Figure 5.9 is composed by an analog comparator which has one input connected to the input signal, and the other input is connected to a fixed reference or ground. The output of the comparator is sampled by the digital system and processed by a DSP.

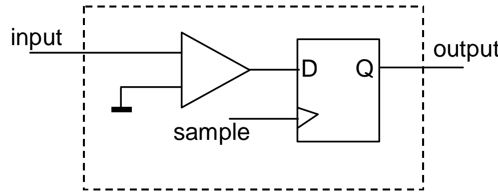


Figure 5.9: Example structure of the simplified sampler (NEGREIROS, 2003-b).

In the following we compare the pseudorandom testing performance of an ideal ADC and the proposed sampler in Figure 5.9. A low-pass second order filter has been tested using the proposed scheme. The test has been simulated in Matlab using a bilinear transform of the circuit transfer function. A general equation for a second-order low-pass transfer function is given by

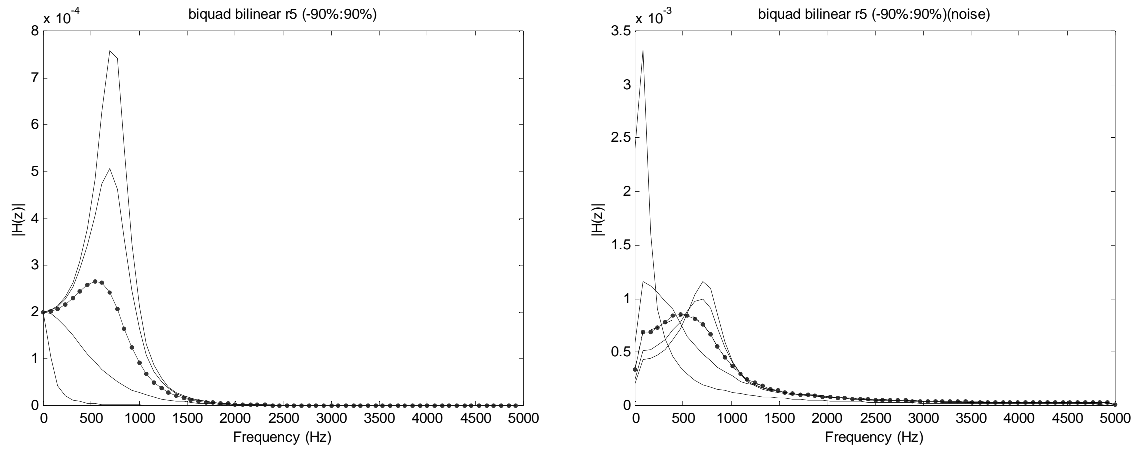
$$H(s) = \frac{K w_o^{\ 2}}{s^2 + s\frac{w_o}{Q} + w_o^{\ 2}} \tag{5.7}$$

The biquad low-pass filter topology presented in Figure 3.5 has the quality factor (Q) equal to unity for nominal component values.

$$Q = \sqrt{\frac{R_4 R_5^{\ 2} C_1}{R_1 R_2 R_3 C_2}} \tag{5.8}$$

Component R_5 affects only the quality factor of this circuit. Any constant multiplying this component will affect the quality factor in the same manner. We will use this in the example to follow.

In Figure 5.10a the quality factor was changed from -90% to +90%, and the magnitude of the transfer function is shown. In figure 5.10b, the same experiment is repeated using 1-bit samples in the PSD estimation. One can see that the shape of the curves is very similar, but their amplitude is different. We have verified that the area of the curves is the same.

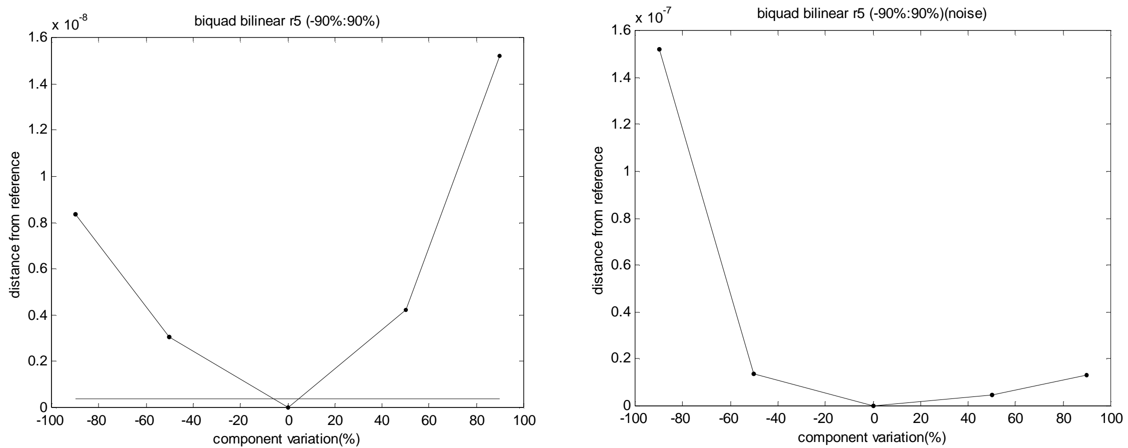


a) |H(z)| observed from ideal ADC b) |H(z)| observed from 1-bit sampler

Figure 5.10: Impact of 1-bit ADC in observing |H(z)| for changes in Q from -90%, -50%, 0%,50% and 90% (NEGREIROS, 2003-b).

The distance measured in each case is shown in Figure 5.11a. The threshold for the 20% error in the PSD estimates is also presented. This figure shows that the PSD distance from a reference one can be effectively used as a parameter to classify the response of the circuit under test. For large deviations in the expected transfer function, a large distance will be assured.

The effect of 1-bit ADC in distance measurements is shown in Figure 5.11b. The large positive variations in the Q factor are not as evident now as in Figure 5.11a. This means that the sensitivity of the test could be reduced when comparing to a high-resolution digitizer solution.



a) Distance from PSD using ideal ADC b) Distance from PSD using 1-bit ADC

Figure 5.11: Impact of 1-bit digitizer in distance measures for changes in Q from -90%, -50%, 0%, 50% and 90% (NEGREIROS, 2003-b).

It should be stressed that variation in the PSD estimates occurs when one estimates the PSD of the circuit under test. This will be reflected as a variation in the distance from the reference. So, instead of having a sharp curve like in Figure 5.11b, one should expect a thicker line, like the one shown in Figure 5.12, obtained through simulation using 10% error in PSD estimates.

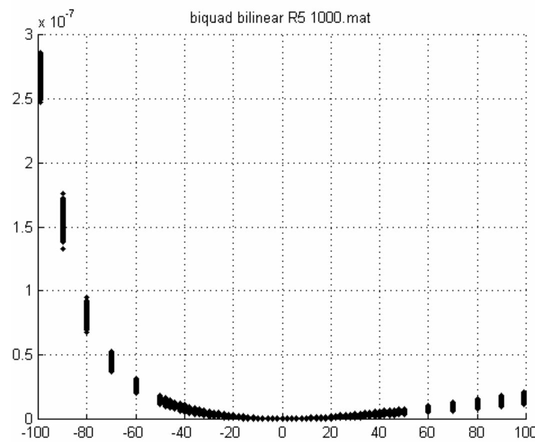


Figure 5.12: Distance measures for changes in Q for 10% error in PSD estimates (NEGREIROS, 2003-b).

5.4.2 Practical results

In order to evaluate the technique, the biquad circuit from Figure 3.5 was prototyped using discrete components and tested. The analog data was acquired at 10kHz using 1-bit samples and processed using Matlab (with rectangular window and no overlap).

The results obtained for 20% error in the PSD estimates are shown in Table 5.3. All large deviations and catastrophic faults were detected. Soft faults (we consider 20% in this case) were detected in some components, but positive soft faults were not detected.

When considering a smaller PSD error (10%), test time increases, and the results are shown in Table 5.4. The number of soft faults detected is larger now. All soft faults in component R5 were detected correctly in this case.

So, for a more sensitive test, one should use a large number of data samples in order to reduce the error in the PSD estimates.

Table 5.3: PSD distance measured for 20% error in the PSD estimates (12800 points, threshold: 3.9e-9) (marked cells indicate no fault detected).

	-50%	+50%	-20%	+20%	OPEN	SHORT
C1	1.0e-8	9.1e-9	**2.2e-9**	**3.1e-9**	9.8e-8	1.7e-8
C2	2.1e-8	1.1e-8	**3.0e-9**	**3.0e-9**	9.8e-8	9.5e-8
R1	4.1e-8	9.8e-9	4.6e-9	**2.7e-9**	1.3e-7	9.8e-8
R2	2.2e-8	8.7e-9	4.1e-9	5.2e-9	3.2e-7	9.8e-8
R3	2.7e-8	1.1e-8	**3.6e-9**	4.9e-9	7.9e-7	9.8e-8
R4	2.5e-8	7.3e-9	5.5e-9	**3.5e-9**	4.3e-7	1.1e-6
R5	1.5e-8	4.7e-9	4.6e-9	**9.7e-10**	9.8e-8	1.1e-6
R6	1.3e-8	7.5e-9	**2.6e-9**	**1.5e-9**	7.1e-8	9.8e-8

Source: NEGREIROS, 2003-b.

Table 5.4: PSD distance measured for 10% error in the PSD estimates (51200 points, threshold: 9.8e-10) (marked cells indicate no fault detected).

	-50%	+50%	-20%	+20%	OPEN	SHORT
C1	5.6e-9	4.1e-9	**6.4e-10**	1.3e-9	9.8e-8	1.5e-8
C2	2.0e-8	8.7e-9	2.0e-9	2.4e-9	9.8e-8	9.6e-8
R1	4.1e-8	8.1e-9	3.0e-9	1.8e-9	1.3e-7	9.8e-8
R2	2.1e-8	7.2e-9	3.3e-9	2.1e-9	3.2e-7	9.8e-8
R3	2.2e-8	8.7e-9	2.6e-9	1.8e-9	8.1e-7	9.8e-8
R4	2.3e-8	6.7e-9	2.7e-9	1.5e-9	5.6e-7	1.1e-6
R5	1.2e-8	4.9e-9	1.7e-9	1.3e-9	9.8e-8	1.2e-6
R6	1.3e-8	6.4e-9	**9.6e-10**	**5.1e-10**	6.8e-8	9.8e-8

Source: NEGREIROS, 2003-b.

5.5 Ultimate Low Cost Analog BIST

In this section we use the results from previous sections in the implementation of an analog test core for pseudorandom testing using the simplest possible analog hardware, in order to reduce the cost of the analog area overhead.

5.5.1 Simplifications using 1-bit converters

The complete test system is shown in Figure 5.13, indicating the digital noise generator and the one bit AD converter. In the following section results for the setup shown in Figure 5.13 are developed.

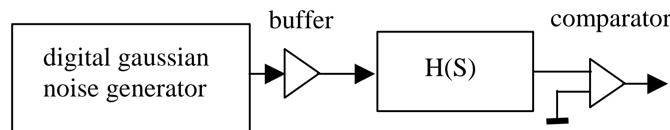


Figure 5.13: Ultimate low cost hardware setup (NEGREIROS, 2003-e).

5.5.2 Results

In order to evaluate the performance of the proposed test method, an experimental setup was built according to Figure 5.14. The arbitrary waveform generator was programmed with a digital gaussian noise created using Matlab. The generator was adjusted so that the output frequency is about 8kHz. The frequency used in the data acquisition system is 10kHz. All data is transferred to a computer running Matlab for analysis. The device under test (DUT) is the low-pass state-variable filter from the ITC'97 analog and mixed-signal benchmark circuits shown in Figure 5.7, prototyped using discrete components.

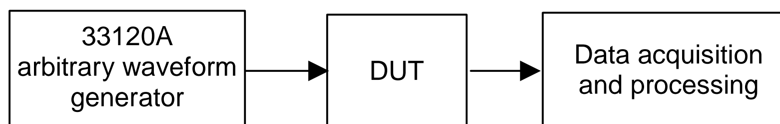


Figure 5.14: Experimental setup.

In Figure 5.15 the binary noise applied to the filter is shown, along with the filter response. One bit versions of these signals (`in/out`) are shown bellow. The data acquisition system samples the binary version of the filter response (`out`).

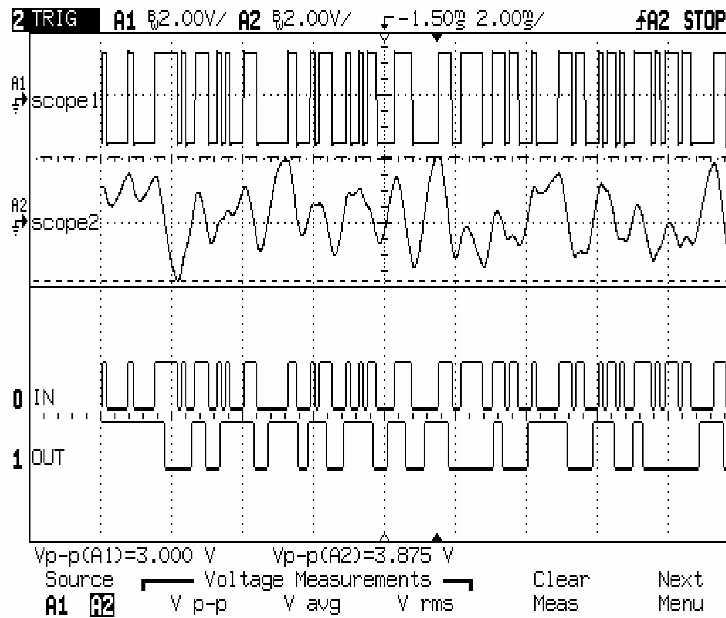


Figure 5.15: Binary noise (scope1), filter response (scope2), one-bit acquisition of input (`in`) and filter response (`out`) (NEGREIROS, 2003-e).

In Figure 5.16 we illustrate the PSD evaluated for 1e5 data points, using a FFT of 128 points, which would be our reference level for the state variable filter. The PSD for the nominal (fault-free) circuit is shown by the marker ".". The other PSDs were evaluated after the injection of a +/- 50% fault in C1.

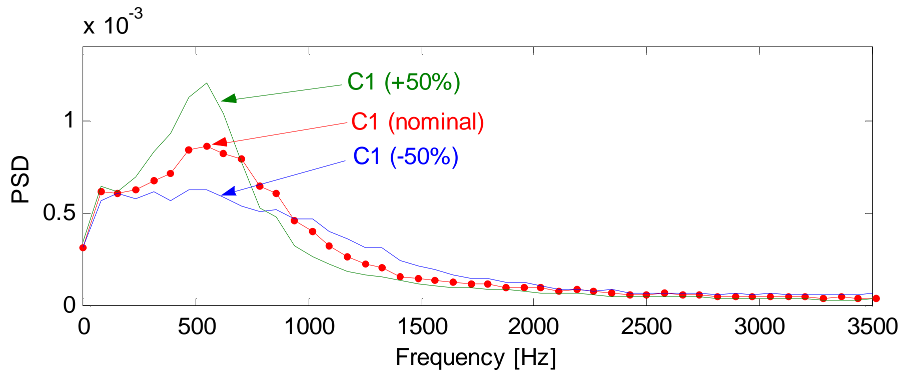


Figure 5.16: PSD for the fault-free SV filter, and after injection of +/-50% deviation faults in C1 (NEGREIROS, 2003-e).

In Tables 5.5 and 5.6 we present data for all components of the state variable filter, for 20% error in PSD estimates (using 12800 samples) and 10% error in PSD estimates (using 51200 samples). Notice that the increase in the acquired data size allows a more sensitive test, as only some faults in R1,R6 and R7 are not detected in Table 5.6.

Table 5.5: PSD distance measured for 20% error in the PSD estimates using binary gaussian noise and 1-bit acquisition (12800 points, threshold: 4.1e-9) (marked cells indicate no fault detected).

	-50%	+50%	-20%	+20%	OPEN	SHORT
C1	5.5e-9	6.3e-9	**1.4e-9**	**2.5e-9**	1.0e-7	1.7e-8
C2	2.1e-8	1.3e-8	**2.7e-9**	**2.5e-9**	1.0e-7	3.5e-8
R1	**2.4e-9**	**1.2e-9**	**4.7e-10**	**1.9e-10**	2.2e-7	7.4e-8
R2	1.4e-8	**3.8e-9**	**2.4e-9**	**1.9e-9**	1.0e-7	3.4e-8
R3	6.8e-9	6.9e-9	**2.0e-9**	**1.4e-9**	2.1e-8	1.0e-7
R4	2.4e-8	7.5e-9	**2.9e-9**	**2.3e-9**	3.2e-7	1.0e-7
R5	1.1e-8	8.6e-9	**2.0e-9**	**1.9e-9**	5.7e-7	1.4e-7
R6	8.3e-9	**2.8e-9**	**1.1e-9**	**1.6e-9**	9.5e-7	3.8e-8
R7	5.6e-9	**3.5e-9**	**6.6e-10**	**6.2e-10**	4.5e-8	9.1e-7

Source: NEGREIROS, 2003-e.

Table 5.6: PSD distance measured for 10% error in the PSD estimates using binary gaussian noise and 1-bit acquisition (51200 points, threshold: 1.0e-9) (marked cells indicate no fault detected).

	-50%	+50%	-20%	+20%	OPEN	SHORT
C1	5.4e-9	6.4e-9	1.0e-9	1.8e-9	1.0e-7	1.7e-8
C2	2.1e-8	1.0e-8	1.7e-9	2.5e-9	1.0e-7	3.5e-8
R1	2.1e-9	**5.5e-10**	**2.1e-10**	**9.4e-11**	1.8e-7	7.5e-8
R2	1.4e-8	3.6e-9	1.8e-9	1.3e-9	1.0e-7	3.5e-8
R3	5.5e-9	6.1e-9	1.3e-9	1.2e-9	2.0e-8	1.0e-7
R4	2.3e-8	8.2e-9	2.4e-9	1.9e-9	3.1e-7	1.0e-7
R5	1.0e-8	7.1e-9	1.8e-9	1.6e-9	5.8e-7	1.2e-7
R6	6.6e-9	1.9e-9	**7.8e-10**	**6.5e-10**	9.3e-7	3.9e-8
R7	4.8e-9	2.7e-9	**5.9e-10**	**4.2e-10**	3.8e-8	9.0e-7

Source: NEGREIROS, 2003-e.

In Figure 5.17 we investigate the behavior of the PSD estimates observed through the sampler regarding R1. The PSD curve for a deviation of +50% in R1 remains close to the reference level, and hence it is not detected. For a deviation of -50% in R1 the PSD curve is clearly different, being detected using a larger data size.

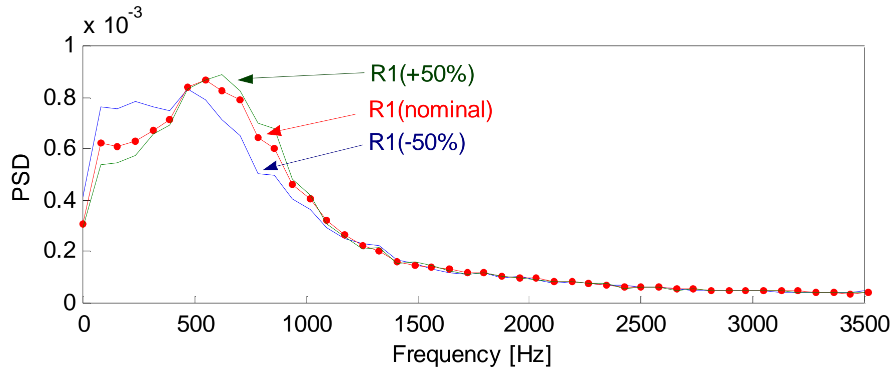


Figure 5.17: PSD for the fault-free SV filter, and after injection of +/-50% deviation faults in R1 (NEGREIROS, 2003-e).

In Table 5.7 we present data using multilevel gaussian noise and a 16 bit AD converter, for the same test time used in Table 5.5. We note that the use of a simpler noise generator and sampler makes the test less sensitive, as 20% variations are not detected in Table 5.5. If one needs a more sensitive test, an increased test time can help (as shown in Table 5.6). In fact, a trade-off between analog area and test time can be seen when one compares the results in Table 5.6 and Table 5.7.

Table 5.7: PSD distance measured for 20% error in the PSD estimates using multilevel input signal and 16 bit AD (12800 points, threshold: 1.8e+7) (marked cells indicate no fault detected).

	-50%	+50%	-20%	+20%	OPEN	SHORT
C1	3.1e+7	4.1e+7	**6.5e+6**	**6.1e+6**	4.4e+8	9.3e+7
C2	5.4e+8	6.8e+7	3.1e+7	2.0e+7	4.4e+8	7.2e+9
R1	2.0e+9	1.1e+8	1.2e+8	2.3e+7	6.3e+10	4.4e+8
R2	6.8e+7	2.3e+7	**1.0e+7**	**4.4e+6**	4.4e+8	8.3e+7
R3	3.5e+7	3.6e+7	**8.7e+6**	**5.6e+6**	9.3e+7	4.4e+8
R4	5.3e+8	6.1e+7	5.3e+7	**1.2e+7**	1.8e+8	4.4e+8
R5	2.4e+8	3.1e+8	5.5e+7	4.0e+7	4.4e+8	1.8e+11
R6	3.8e+8	3.8e+7	2.7e+7	**8.7e+6**	8.4e+10	2.6e+8
R7	7.8e+7	9.8e+7	2.2e+7	**1.3e+7**	2.5e+8	9.1e+10

Source: NEGREIROS, 2003-e.

5.5.3 Analysis

The results shown in the previous section indicate the feasibility of the low cost technique proposed. The use of a digital gaussian noise has allowed the implementation of an entirely digital signal generator - the only analog portion is the output buffer. Although the signal has only two amplitude levels, its frequency content allows the excitation of all the input bandwidth of the analog circuit

It was noticed that the coarse quantization of the gaussian input signal does not significantly impact the obtained PSD estimates. The use of gaussian noise has also allowed the replacement of an AD converter by a simple analog voltage comparator. Although AD converters are expected to be present in a SoC, their cost is a limiting factor, as the observation of several analog test points in an analog circuit would require several converters. Also, for the implementation of an analog test core, the overall cost of the tester must be kept to a minimum. The proposed method also provides a way to test partitioning without the use of switches for the data acquisition, and without introducing topological changes in the analog circuit.

The test time is an important issue, since it is directly related to the cost of the SoC. In the proposed approach, test time is related to the accuracy of the required PSD estimates, so a more sensitive test would require more data samples.

The proposed strategy also has a low memory overhead in the digital domain, as each sample of the signal uses only one bit. This is achieved at normal sampling frequency of the system, so no over-sampling is required.

The results obtained in Tables 5.5 and 5.6 indicate that the increase in the number of acquired samples enables a more sensitive test. These tables also indicate that the sensitivity of the PSD observed through the comparator may hide some faults that could be observed using higher resolution but costly AD converter. One solution to this problem may be the use of a large number of samples, but this may not be practical because of the increase in test time.

5.6 Conclusions

This chapter has presented the utmost low analog area cost technique for analog BIST. Mathematical and practical results showed that the implementation of the tester is feasible. The performance of the method can be compared to the same solution using an analog noise generator and a high resolution AD converter, if sufficient test time is available.

The technique can be easily implemented in the SOC environment and is intrinsically noise-immune, as it benefits from noise characteristics in order to make it possible to use a simple digitizer and noise generator.

In the next chapter we apply the statistical sampler to RF test, as the simplicity of the converter allows higher sampling rates to be achieved.

6 RF TEST

The SoC approach to the design of electronic products allows rapid development of new products through reuse of basic design blocks or IP (intellectual property) cores (ZORIAN, 2000). Using this approach one can have a new functionality in the system by the addition of a new IP core. Thanks to market needs, the presence of wireless communication blocks to be embedded in systems-on-chip (SoC) is ever more present. Although the design time problem seems to be tackled by the IP reuse approach, the testability of such chips, especially for the high performance analog RF part, is still an open issue.

The need for BIST structures for analog and RF circuits is increasing, as recent technology products require high-speed testers with analog and RF capabilities, thus increasing the test cost. One way to alleviate the test cost is to provide internal BIST structures that could be used to perform the test of specific parts, embedding the most demanding part of the analog tester on chip. As the test of analog RF circuits is usually a specification-based test that should be performed at speed, incorporating structures that could ease the test and lower its cost would be desirable

Although there is a widespread use of wireless communications and portable devices, there are few methods in the literature that address BIST for analog RF signal paths. Current techniques are often based on some kind of loopback approach, in order to reuse the transmitter or receiver section. While enabling some reuse, the reconfiguration required by these approaches is achieved through the use of switches and muxes that may degrade the performance of the circuit under normal operation, since non-linearities are introduced in the signal path. Also, the analog circuit will not observe a constant load - normal operation and test operation are performed on different circuits caused by the configuration mechanism, which makes the design of the analog circuit itself harder.

In the following sections we analyze the RF signal path in more detail, followed by a brief review of RF test methods. After that a test technique based on subsampling is proposed. The chapter concludes with BIST and on-line testing approaches based on the statistical sampler.

6.1 RF signal path considerations

In this section the RF signal path is analyzed. The receiver path (RX section in Figure 6.1) will be detailed, specially the mixer. Linearity effects on the RF path are also discussed. It is observed that the normal behavior of the path can be characterized and observed by spectral analysis.

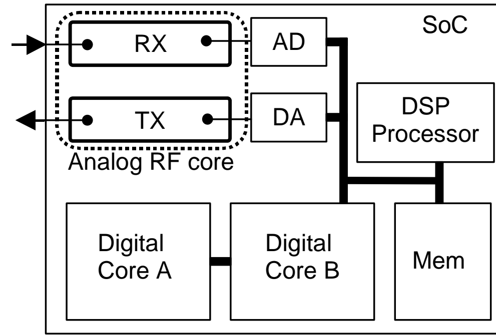


Figure 6.1: SoC environment with a transceiver (NEGREIROS, 2003-f).

6.1.1 Typical RF signal path

A typical RF link is composed by a receiver and a transmitter section. The basic transmitter section is shown in Figure 6.2, where an input signal passes through a modulator. The modulator translates the center frequency of the input signal to the carrier frequency. This signal is then filtered, amplified and transmitted. The transmitter can employ more than one modulator block in order to complete the upconvertion process. If only one block is used the system is called "direct conversion" (RAZAVI, 1998).

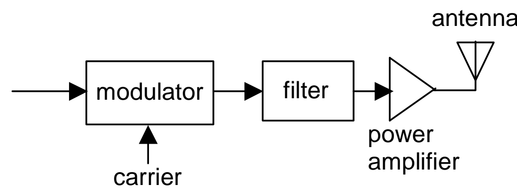


Figure 6.2: Basic transmitter (NEGREIROS, 2003-f).

The basic receiver section is shown in Figure 6.3. The signal from the antenna is amplified by a low noise amplifier (LNA), filtered and applied to a downconverter. The center frequency of the signal is then translated to a lower frequency by the downconverter. If more than one downconverter stage is used, the receiver is called heterodyne. If the input spectrum is translated to the baseband in the first downconversion, the system is called direct conversion or zero-IF (intermediate frequency) (RAZAVI, 1998). The ideal frequency translation operation is shown in Figure 6.4, where the center frequency of the output is f_{input}-$f_{carrier}$.

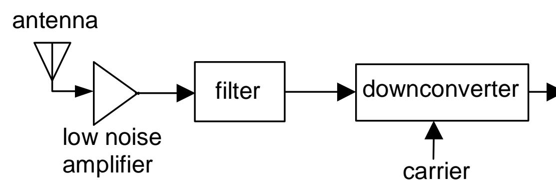


Figure 6.3: Basic receiver (NEGREIROS, 2003-f).

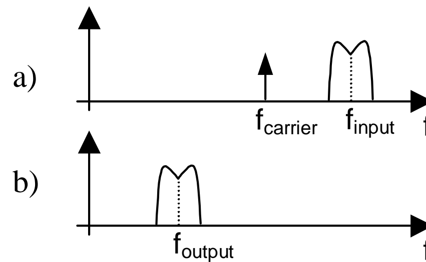


Figure 6.4: Signal spectra in ideal receiver: (a) input signal and (b) desired output at f_{input}-$f_{carrier}$ (NEGREIROS, 2003-f).

One should note that the transmitter and receiver have basically three blocks: amplifiers, filters and up/down converters. The converters can be implemented using multipliers, being similar blocks.

In the SoC environment, modern applications like the software-radio are strongly based on digital signal processing. Digital blocks with enough processing resources, together with AD and DA converters are used to enable the implementation of the demodulation or modulation schemes. In Figure 6.5 a generic transceiver architecture details the similarities between the transmitter and receiver blocks.

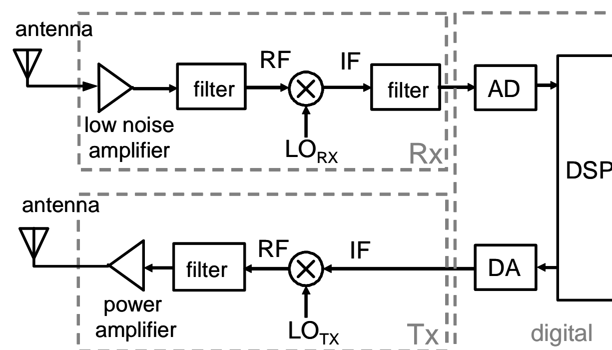


Figure 6.5: Generic transceiver system (NEGREIROS, 2004-a).

Being the initial stages in the reception, the performance of the LNA and the mixer directly affect the performance of the entire receiver. The most important parameters are related to noise and linearity characteristics. These performance requirements are expressed using special parameters, like those listed in Table 6.1.

Table 6.1: Typical mixer characteristics.

Noise Figure (NF)	12 dB
Input third-order Intersect Point (IIP_3)	5 dBm
Gain	10 dB
Port-to-Port Isolation	10-20 dB

Source: RAZAVI, 1998.

The noise figure is a measure of how much the signal to noise ratio (SNR) degrades as the signal passes through a RF stage. The intersect point is a measure of intermodulation distortion caused by a non-linearity in the signal path. The third order intersect point characterizes a 3rd order non-linear distortion.

In the next section a receiver block is analyzed in more detail, focusing on the frequency converters.

6.1.2 Analyzing the receiver path

If one considers the up/downconverters presented in the last subsection, they can be ideally implemented using multipliers. Considering Figure 6.6, if a single RF tone at f_{RF} reaches the receptor, and that a carrier at f_{LO} is also a sinusoidal, the product of the tones is given by Equation 6.1.

$$\cos(\omega_{RF}) \cdot \cos(\omega_{LO}) = \frac{1}{2}\cos(\omega_{RF} - \omega_{LO}) + \frac{1}{2}\cos(\omega_{RF} + \omega_{LO}) \tag{6.1}$$

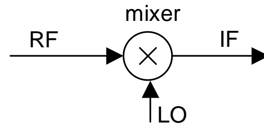


Figure 6.6: Downconverter mixer as a multiplier.

The difference term is used in a downconverter mixer, while the addition term is used in an upconverter mixer.

It is common in several types of mixers (both active and passive) the multiplication by a square wave instead of a sine, because of implementation issues (usually the input signal is switched accordingly to the LO frequency, and the switching operation can be seen as multiplication by a square wave). In this case, the output of the mixer will not be band-limited. A square wave can be written in a series form,

$$square(\omega t) = \frac{4}{\pi} \sum_{n=1,3,5,...}^{\infty} \frac{1}{n} \sin(n\omega t) \tag{6.2}$$

and developing the product the output of the mixer can be shown to be

$$\cos(\omega_{RF}) \cdot square(\omega_{LO}) = \frac{2}{\pi} \sum_{n=1,3,5,...}^{\infty} \frac{1}{n} \left(\sin(n\omega_{LO}t + \omega_{RF}) + \sin(n\omega_{LO}t - \omega_{RF})\right) \tag{6.3}$$

The undesired frequency components should be filtered out by other stages following the mixer. Other issues like noise and signal power must also be considered. Among these, linearity issues are addressed in the next subsection.

6.1.3 Linearity issues

Linearity is an important issue in the receptor front-end, specially in the mixer and LNA, because strong interferences may be present at the antenna. Third order non-linear distortion is particularly important, because intermodulation products may fall in the desired signal band. A performance parameter called "third order intercept point" (IP3) is defined to characterize this specific behavior (RAZAVI, 1998).

The non-linear behavior of linear blocks will be reflected in the spectrum as the addition of several frequency components, namely intermodulation terms and harmonics. Harmonics are frequency terms which are multiple from the input frequency applied to the non-linear system. Intermodulation terms are frequency components that appear at the output of a non-linear system in response to a two-tone input signal.

Considering a memoryless nonlinearity of 2nd and 3rd order, defined by

$$y(t) = \alpha x(t) + \beta x^2(t) + \gamma x^3(t) \tag{6.4}$$

If one applies a sinusoidal signal ($A\cos(\omega t)$) to this system, the output will be given by (RAZAVI, 1998)

$$y(t) = \frac{\beta A^2}{2} + \left(\alpha A + \frac{3\gamma A^3}{4} \right) \cos(\omega t) + \frac{\beta A^2}{2} \cos(2\omega t) + \frac{\gamma A^3}{4} \cos(3\omega t) \qquad (6.5)$$

The terms at 2ω and 3ω are the harmonics. One can see that higher order non-linearities would generate higher frequency harmonics.

If a two-tone signal of the form ($A_1\cos(\omega_1 t)+ A_2\cos(\omega_2 t)$) is applied to the system in Equation 6.4, the output will contain frequency terms at ($\omega_1\pm\omega_2$), ($2\omega_1\pm\omega_2$), ($\omega_1\pm2\omega_2$) and at the fundamental components (ω_1, ω_2) (RAZAVI, 1998). The measurement of the IP3 of the system is based on the amplitude measurements of the terms at ω_1, ω_2, $2\omega_1$-ω_2 and $2\omega_2$-w_1, as illustrated in Figure 6.7.

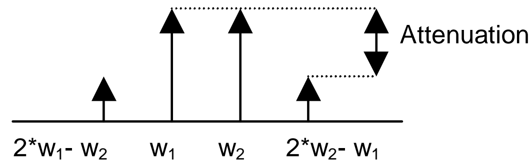


Figure 6.7: Intermodulation terms.

The IIP3 is measured in a two-tone test (where the amplitudes of the tones are the same and known), by measuring the attenuation of the intermodulation products with respect to the desired IF outputs, as shown in Figure 6.7. One can observe that the measurement procedure is based on spectral analysis of the output of the mixer. In Figure 6.7, signals at frequencies ω_1 and ω_2 are the desired IF outputs, and signals at frequencies ($2*\omega_1$-ω_2) and ($2*\omega_2$-ω_1) are the undesired intermodulation products. The measurement of IP3 is usually done by the use of two signal generators (one for each frequency) and the measurement of the output using a spectrum analyzer (for example, see (ANALOG DEVICES, 1995-a)).

6.2 Review of RF analog testing approaches

The problem of testing high frequency analog circuits has not been thoroughly addressed in the literature. The main test strategy currently used is the *loopback technique*, which routes the signal from the transmitter back to the receiver.

Loopback techniques are based on the idea of routing the output of a system directly back to the input of the system, without using a wireless link. The idea is illustrated in Figure 6.8. In RF signals the blocks work usually at different frequencies (R1 and T1 would be working at the radio frequency, while R2 and T2 would be working at the intermediate frequency). In a SoC environment, a digital block with AD and DA converters is also expected to be present.

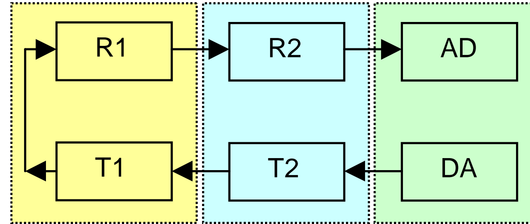


Figure 6.8: Basic loopback strategy.

One issue noted in loopback strategies is the possibility of specific faults being masked by the analog path used, since the entire RF signal path is tested and intermediate test points do not exist. For example, a defect in the transmitter could be masked by the use of an excellent receiver that filters the out-of-band distortion. Also, a weak transmitter could be compensated by a strong receiver. Another issue is that the signal level at the output of the transmitter may not be the signal level that is desirable or possible to measure with the receiver. The loopback application to on-line testing is also not possible due to the required controllability of the input signal to the DUT.

Some variations of the idea were already presented in the literature. In (VEILLETTE, 1995) a setup like the one shown in Figure 6.9 is used. First, the receiver channel of the transceiver is tested, by the application of an input signal generated by the 1-bit DA converter. The signal is a bit-stream that should be filtered by the analog path itself. After testing the receiver, the transmitter is verified using a loopback connection. In Figure 6.9 the loopback connection is made at the intermediate frequency (IF) stage.

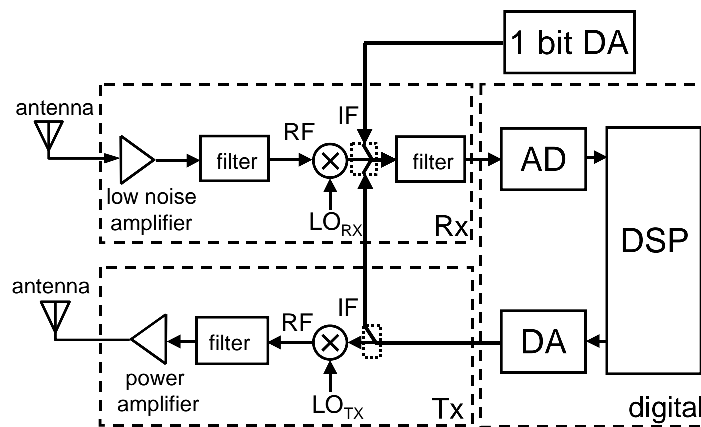


Figure 6.9: Loopback strategy (VEILLETTE, 1995).

Other loopback test techniques were presented in (JARWALA, 1995; LUPEA, 2003). In these approaches the transmitter section is tested first using an additional AD converter and frequency translation elements (see Figure 6.10). After that, the receiver is verified using the signal generated by the transmitter.

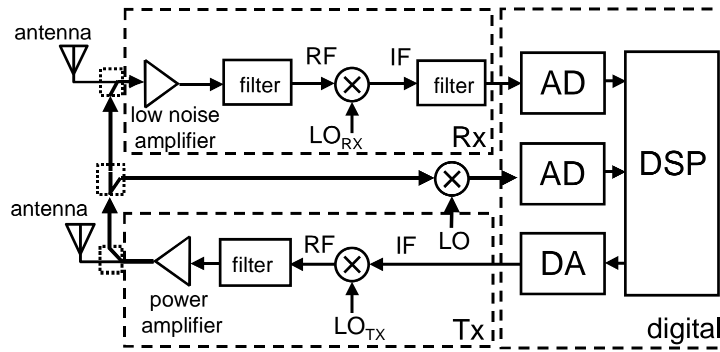


Figure 6.10: Loopback strategy (JARWALA, 1995; LUPEA, 2003).

In (VOORAKARANAM, 2002) a method targeted to the test of RF components based on signature concept is developed. It uses two mixers in order to apply signals to a RF device, enabling the use of low frequency signals for processing. The method may not be suited for BIST implementation because of the additional resources needed, however. Other authors have focused on testability analysis of RF circuits in order to reduce overall system cost (OZEV, 2002).

In (RYU, 2004) a technique targetted at low noise amplifiers was developed. However, analog area overhead is an issue in the proposed BIST method because of the amount of additional analog circuitry.

Some approaches using alternate testing methodologies for RF have also been suggested recently. In (BHATTACHARYA, 2004-a) an algorithm is presented on how to place a set of available sensors at the outputs of a system under test to get maximum accuracy in prediction of a set of target specifications. In (BHATTACHARYA, 2004-b) a method to evaluate functional characteristics by exciting the RF circuit with periodic bitsetreams is proposed. In (HALDER, 2005) optimized periodic bitstreams are used in a loopback configuration and functional parameters like IP3 are estimated. However, the approach suffers from loopback reduced observability.

Although suited for the production test, BIST techniques are generally not able to be used for on-line test. This is the case for BIST strategies that modify the circuit topology during the test or its input signal is being controlled by the test mechanism. Thus, on-line test of RF circuits requires the development of test strategies that continuously evaluates the operation of the circuit during normal operation.

One strategy to enable concurrent testing is the use of duplicates of the circuit (LUBASZEWSKI, 1995). In this scheme, a comparison mechanism verifies the similarity between the programmable reference block and the block under test. The application of this strategy for RF is challenging, as the analog comparison will require special routing of signals. Also, variable load may be observed by the circuit under test, which is undesirable in RF. For the case of fully differential circuits there is the possibility of building analog checkers (LUBASZEWSKI, 2000). To the authors' knowledge, no checkers able to cope with RF specific circuits have been proposed.

6.3 Testing RF Signal Paths Using Spectral Analysis and Subsampling

In this section a technique based on spectral analysis and subsampling is developed. It enables the partitioning of the RF signal path, making it easier to locate faulty stages. A synchronization scheme is proposed in order to enable the direct sampling of the high

frequency signal, thus avoiding the use of an extra anti-alias filter. Furthermore, as the technique is done mainly digitally, it is suitable to be implemented by a common external digital tester, or even in a BIST scheme for a SoC environment. Theoretical background and experimental results are provided in order to evaluate the feasibility of the method.

6.3.1 Sampling considerations

If one wants to observe the spectra in the RF signal path, one should include a high speed AD converter and an adequate analog path and switches to the ADC. Unfortunately, the frequencies involved are too high for being acquired by the system ADC at the Nyquist rate.

One strategy used is subsampling, when the RF signal has a small frequency band, centered in high frequency. As shown in Figure 6.11, as the signal is band limited and the spectrum outside its band is filtered, the effective sampling rate needed (FS) is very small.

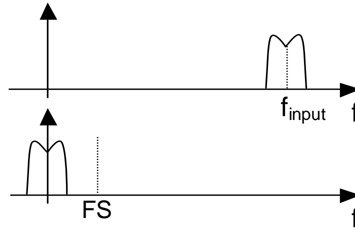


Figure 6.11: Subsampling a high frequency band limited signal (NEGREIROS, 2003-f).

6.3.1.1 Aliasing

In general, the sampling operation will be able to represent the input signal adequately if the input frequency is below FS/2. If the input frequency is higher than the Nyquist rate, this frequency will be aliased. The aliased frequency is a function of the input signal and the sampling frequencies.

Consider that an ideal ADC is sampling at FS. Nyquist frequency is therefore F=FS/2. In order to verify the aliased frequency, one should obtain the ratio between the input signal frequency (f_{in}) and the Nyquist frequency (F),

$$p = \text{integer_part_of } (f_{in}/F) \qquad (6.6a)$$

$$q = \text{fractional_part_of } (f_{in}/F) \qquad (6.6b)$$

The aliased frequency is given by

$$a = \begin{cases} q.F & \text{,if p is even} \\ (F - q.F) & \text{,if p is odd} \end{cases} \qquad (6.7)$$

Equations 6.6 and 6.7 can be verified using an example. Considering F=12.5 and f_1=10, one gets f_1/F=0.8, so p=0 and q=.8. The aliased frequency is a_1=.8*12.5=10 (no aliasing results). If the input is changed to f_2=13, then f_2/F=1.04, so p=1 and q=.04. The aliased frequency is now a_2=(12.5-.04*12.5)=12.0. Finally, if f_3=26, f_3/F=2.08, so a=2 and q=0.08. The aliased frequency is a_3=.08*12.5=1.0. These transformations are presented in Figure 6.12.

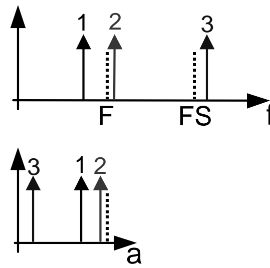


Figure 6.12: Subsampling and aliasing (NEGREIROS, 2003-f).

From Equation 6.6, one should realize that if the input frequency is a multiple from F, then it will appear at dc or F in the aliased spectra. If this input signal has harmonics, their effect will be combined at the mentioned extremes points of the spectra.

6.3.2 A test strategy for the RF signal path

The basic idea in the proposed test methodology is shown in Figure 6.13. In order to observe and characterize the RF signal path, a two-tone RF signal generator excites the path. The system ADC is then used to acquire signals at different test points in the signal path.

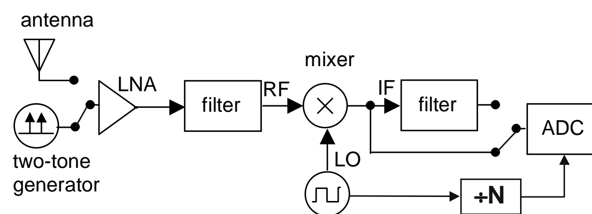


Figure 6.13: Observing the mixer output (NEGREIROS, 2003-f).

After the IF filter the input signal spectra is limited, which eases the spectral analysis of the acquired signal. The mixer output, on the other hand, is not frequency limited, as several harmonics of RF and LO signals will be present at its output.

If one desires to observe the spectral characteristics at the output of the mixer, one should insert another analog filter in the route to the ADC, in order to avoid alias.

In this work no extra filter is inserted and the aliased spectra at the mixer output are taken as signature of the mixer. In order to avoid the effects of harmonics of the LO signal, a frequency divider is used in order to provide the ADC sampling frequency. This allows to isolate effects of the LO signal on the test.

6.3.3 Results

In order to evaluate the capabilities of the method, the setup in Figure 6.13 was simplified and simulated in Matlab. A two tone signal was applied directly to the mixer, and the mixer output was sampled by an ADC converter. The behavioral mixer model from (LEENAERTS, 2001) was used in order to provide more realistic results (including third order non-linear effects).

The two-tone RF signal had frequencies at 401 and 404 MHz, and the LO signal was a sinusoidal at 100MHz. Simulation considered an ideal ADC running at 10GS/s. The output of the ADC is subsampled by a factor of 1000 in order to illustrate the reduction in sampling frequency requirements (from 10GS/s to 10MS/s).

The expected frequencies are the terms at RF±LO (301,304,501 and 504 MHz) and the intermodulation products (298,307,498 and 507 MHz). Other frequencies will occur because of the non-linearities. When the output-referred IP3 of the mixer is changed from 10 to 0 dBm, spectral analysis at the ADC output shows the results in Figure 6.14. One can see two clearly different spectra because of the change in the non-linear behavior of the mixer.

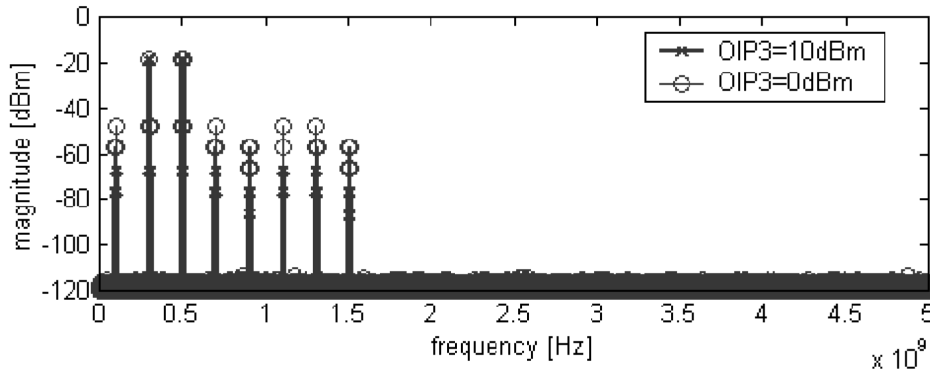


Figure 6.14: Spectra after changing the non-linear behavior of the mixer (FS=10GHz) (NEGREIROS, 2003-f).

In order to evaluate the aliased spectrum, one should consider the results presented in section 6.3.1.1. Considering a subsampling factor of 1000, then F=5MHz (FS=10MHz). The aliased components of terms at RF±LO (301,304,501 and 504 MHz) and IM3 (298,307,498 and 507 MHz) are shown in Table 6.2, after using Equations 6.6 and 6.7.

Table 6.2: Frequencies expected in simulation.

terms	**frequencies**			
(RF±LO)	301	304	501	504
(RF±LO)/5	60.2	60.8	100.2	100.8
aliased RF±LO	1.0	4.0	1.0	4.0
IM3	298	307	498	507
IM3/5	59.6	61.4	99.6	101.4
aliased IM3	2.0	3.0	2.0	3.0

Source: NEGREIROS, 2003-f.

The spectral analysis for the mixer output, after reducing the sampling rate using a 1:1000 factor is shown in Figure 6.15. The frequencies are those expected from Table 6.2 and one can see clearly two different behaviors because of the change in IP3.

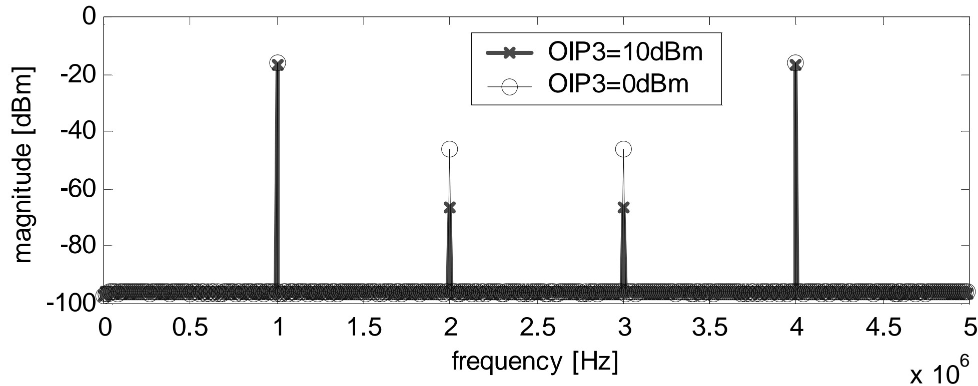


Figure 6.15: Aliased spectra after changing the non-linear behavior of the mixer (FS=10MHz) (NEGREIROS, 2003-f).

The presented reduction in sampling rate should be followed by a careful estimation of the spectra. In the simulation presented 1000 FFTs were evaluated and their mean was presented.

6.3.3.1 Experimental results

An experimental setup was built in order to evaluate the technique. The circuit presented in Figure 6.16 was prototyped using discrete components, as an easy way to introduce faults in the mixer. The mixer is a passive type (RAZAVI, 1998) with differential output. The load was set to 1kΩ, which is a value encountered in real applications (because most passive IF filters have input impedances from 500 to 1000 Ω (RAZAVI, 1998)).

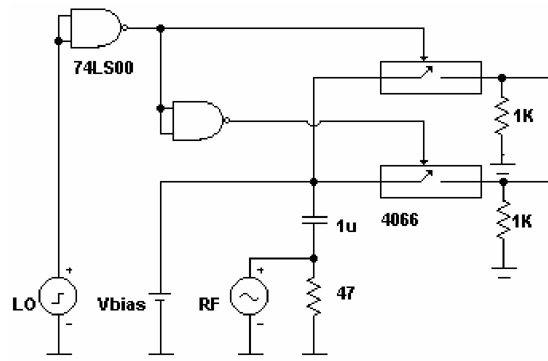


Figure 6.16: Schematic of the passive mixer (NEGREIROS, 2003-f).

Figure 6.17 describes the equipment used and measurement setup. A two-tone signal is applied by the arbitrary waveform generator at frequencies 60kHz and 63kHz. The local oscillator signal is a square wave of 50kHz applied by another generator. Both outputs of the mixer are sampled by an HP54645D digital oscilloscope and 500k samples (for each channel) are transferred to a PC for analysis using Matlab. Data is sampled at 25MHz.

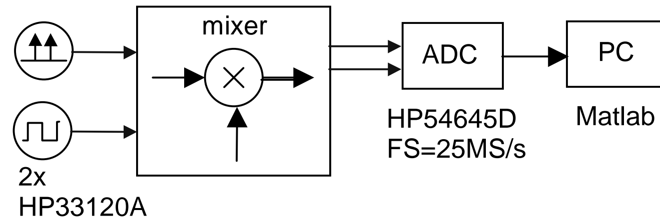


Figure 6.17: Experimental setup and equipment used (NEGREIROS, 2003-f).

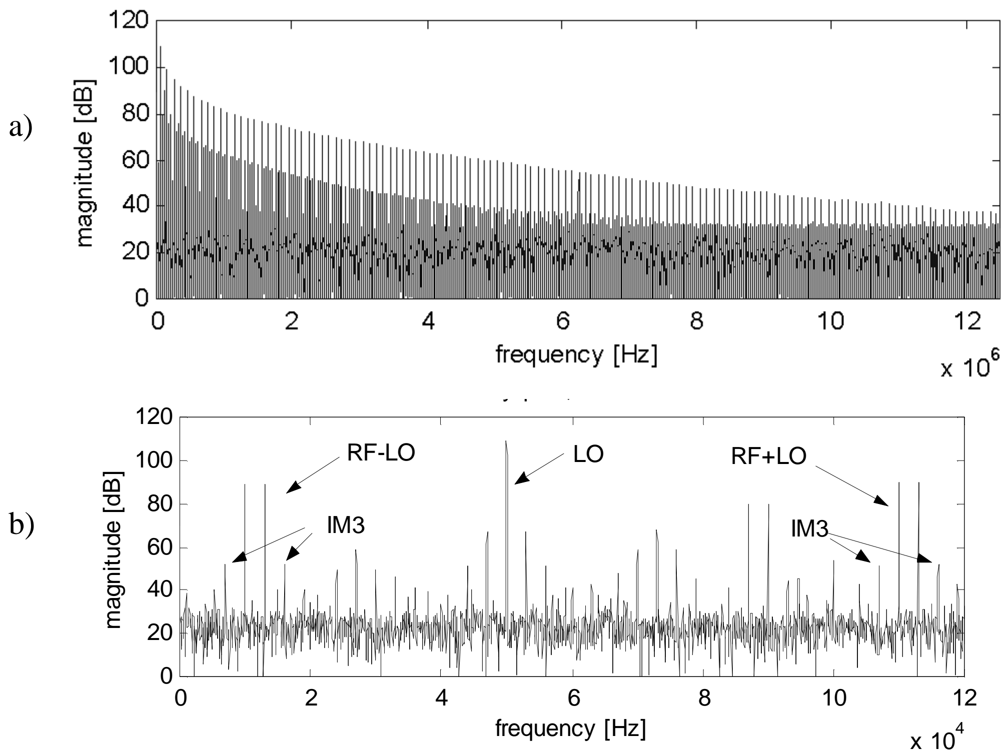


Figure 6.18: Spectrum of mixer output:a) full bandwidth and b) zoom to 120kHz (NEGREIROS, 2003-f).

Figure 6.18 shows the spectral analysis of the mixer output, after acquisition using the setup in Figure 6.17. One can observe clearly the frequency components at the output of the mixer, as shown in Figure 6.18b.

Two faults were injected in the passive mixer of Figure 6.16: one of the switches was held opened first, and after it was held shorted. Spectral analysis for the three situations is shown in Figure 6.19, being acquired at 25MHz. A 500k points FFT was evaluated and the frequency band up to 15kHz is shown. One can observe the marked regions were it is possible to separate the spectra for each case.

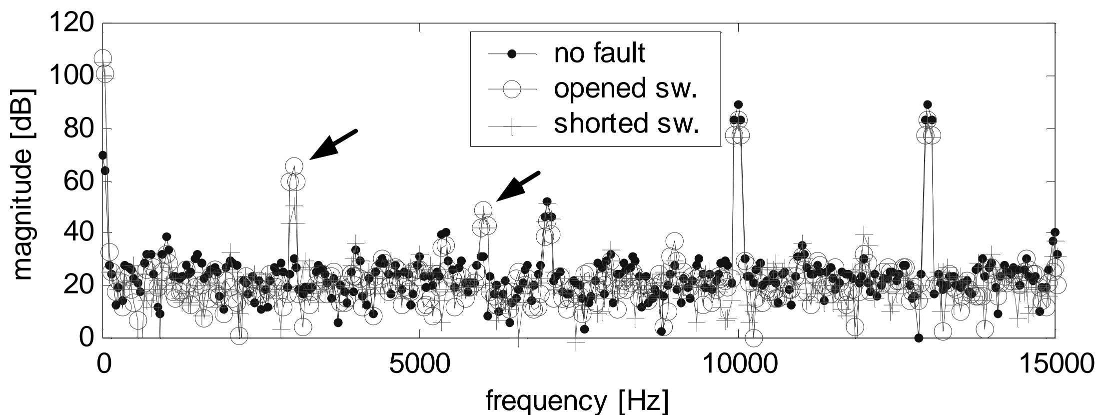


Figure 6.19: Spectrum of faulty and fault-free mixer up to 15kHz (NEGREIROS, 2003-f).

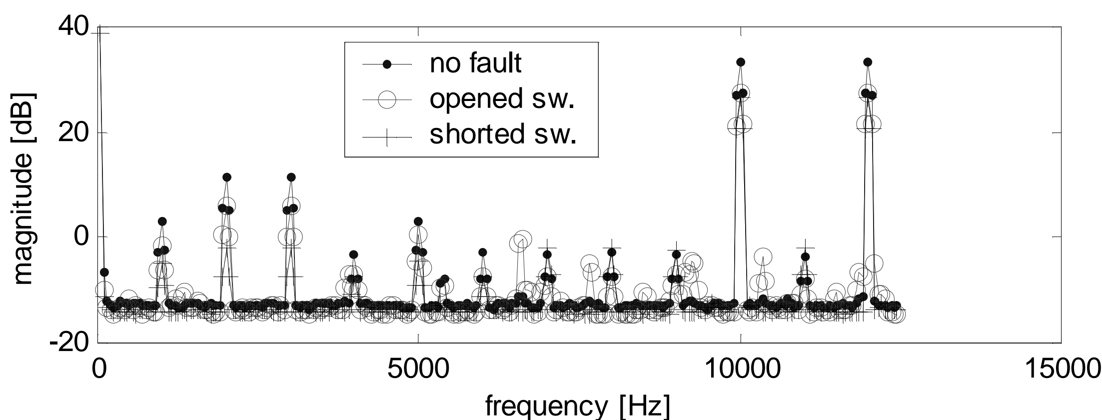


Figure 6.20: Spectrum of faulty and fault-free mixer up to 15kHz (NEGREIROS, 2003-f).

After subsampling the acquired data by a factor of 1000 (which means using 1 sample out of 1000 available - effective FS=25kHz), and performing spectral analysis using means of FFTs, data shown in Figure 6.20 is obtained. One can see now that the spectrum is less noisy than that in Figure 6.19, and more clearly distinguishable.

6.3.4 Analysis

The results presented in the previous section have demonstrated the feasibility of applying subsampling in order to evaluate the spectrum of RF signals that are not frequency limited, thus incurring in an alias spectrum. Data provided in Figure 6.20 could be processed in order to verify the status of the mixer, when subjected to the two-tone input stimuli.

Synchronization in the preceding section was not needed because of the high quality time-base of the generators and data acquisition system. If the local oscillator frequency was deviated from 50kHz, several components could be introduced in the aliased spectra because of the harmonics that would not end-up in the dc FFT bin.

Noise can be a problem because the aliasing process causes alias of noise, thus increasing the noise level from the one obtained at Nyquist rate. On the other hand, RF systems have the minimum bandwidth needed, thus limiting noise. Also, as the input signal is generated by the test setup, its input level should be adjusted adequately.

The analog bandwidth of the ADC will impact the capability of the method to detect faults, as higher frequencies would be eliminated by a limited bandwidth ADC. The use of sample-and-hold circuits could help alleviate the problem.

Processing requirements of the technique are related to evaluating a Fourier transform of the acquired data. This could be evaluated by on-chip resources in a SoC environment, thus enabling a BIST scheme to be built. An external digital tester could be used if no resources are available, discarding the need for an expensive analog tester.

6.4 Low Cost Analog Testing of RF Signal Paths

In this section a low cost method for testing analog RF signal paths suitable for BIST implementation in a SoC environment is described. The method is based on the use of a simple and low-cost one-bit digitizer that enables the reuse of processor and memory resources available in the SoC, while incurring little analog area overhead. The proposed method also allows a constant load to be observed by the circuit, since no switches or muxes are needed for digitizing specific test points.

6.4.1 Test Method

The proposed test method is based on the evaluation of the spectrum at specific test points in the analog signal path, as illustrated in Figure 6.21. Memory and processing resources from the SoC environment could be used in order to implement the test. As the output of the sampler is a digital signal, it can be interfaced directly to the digital part of the system through a data bus.

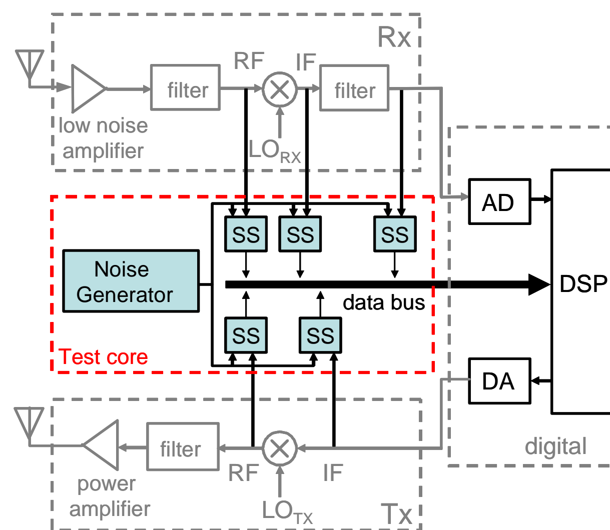


Figure 6.21: Generic transceiver system with testing capabilities (NEGREIROS, 2004-a).

6.4.2 Test example using Matlab simulation

In order to illustrate the proposed approach, a simulation for a two-tone test was run in Matlab using a behavioral model for the mixer, which allows the fine-tuning of third-order distortion. Two tests were executed with different values of IP3, so one would expect to observe different levels of distortion.

The simulations considered an input signal with two tones, and a sinusoidal signal at the LO input. The spectrum of the IF signal was evaluated using a single FFT of the

entire signal. In Figure 6.22, the spectrum of the IF signal observed through the proposed sampler is also shown. One can observe that the noise floor has significantly raised, and completely hides the intermodulation products, but the main components are clearly visible.

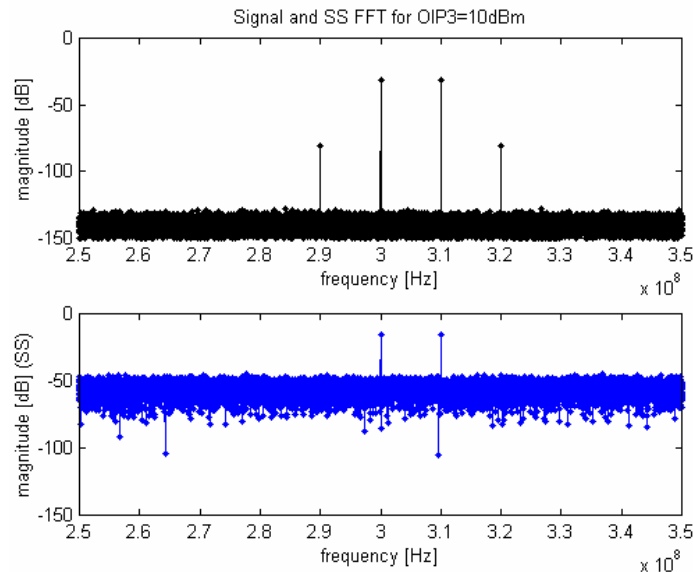


Figure 6.22: IF Spectrum with infinite resolution converter and spectrum obtained from sampler (NEGREIROS, 2004-a).

If the OIP3 is decreased from 10dBm to -3dBm, while the remaining parameters are held constant, the intermodulation products now become as shown in Figure 6.23. One can see that the intermodulation terms are clearly visible in the spectrum evaluated from the sampler output.

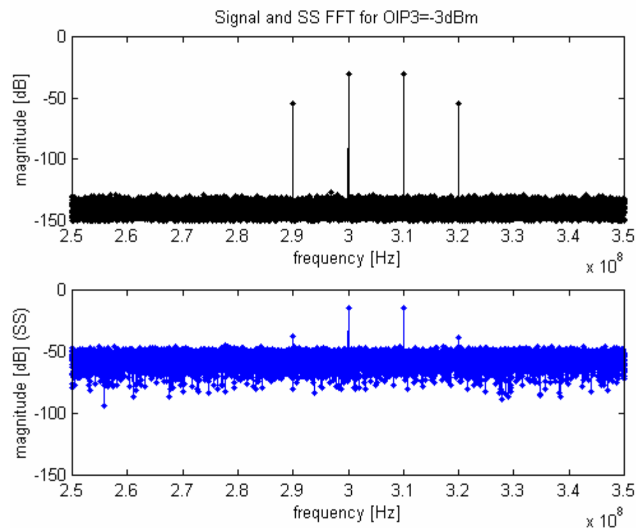


Figure 6.23: IF Spectrum with infinite resolution and spectrum obtained from sampler for a large distortion (NEGREIROS, 2004-a).

6.4.3 Experimental results

In this section we address implementation issues by prototyping a single-balanced active mixer in real hardware. The first implementation is at low frequency and contains

the mixer block and an active low pass filter. It illustrates the insertion of faults in the filter and the variation of the bias voltage influencing the third-order intermodulation products. The second implementation addresses a relatively high frequency.

6.4.3.1 Testing a mixer and filter

The setup in Figure 6.24 has been prototyped using a CD4007 device (for implementing a single-balanced active mixer) and a programmable low pass filter. Two-tone signals were applied at 60 and 63 kHz. The local oscillator frequency was set to 50 kHz. Statistical samplers were used in each one of the differential signals at the output of the mixer and at the output of the filter.

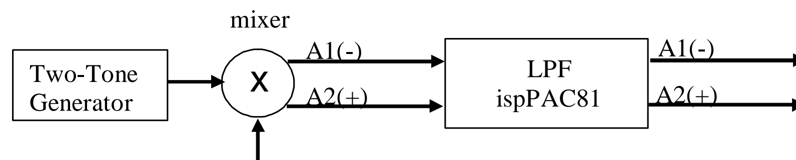


Figure 6.24: Mixer and filter setup (NEGREIROS, 2004-a).

For a bias voltage of 3.3V one obtains the results shown in Figure 6.25. In the lower trace it is shown the spectra observed through the statistical samplers. The large tone at 50 kHz dominates the spectra. As the noise floor is related to the maximum signal level, the intermodulation tones of the demodulated mixer signal at 7 and 16 kHz are completely masked. In the upper trace it is shown the spectra after low-pass filtering. The 4th order filter has a cutoff frequency of 30.1 kHz. As the amplitude of the local oscillator has been reduced, the intermodulation terms are clearly visible and could be used in order to estimate the third order distortion.

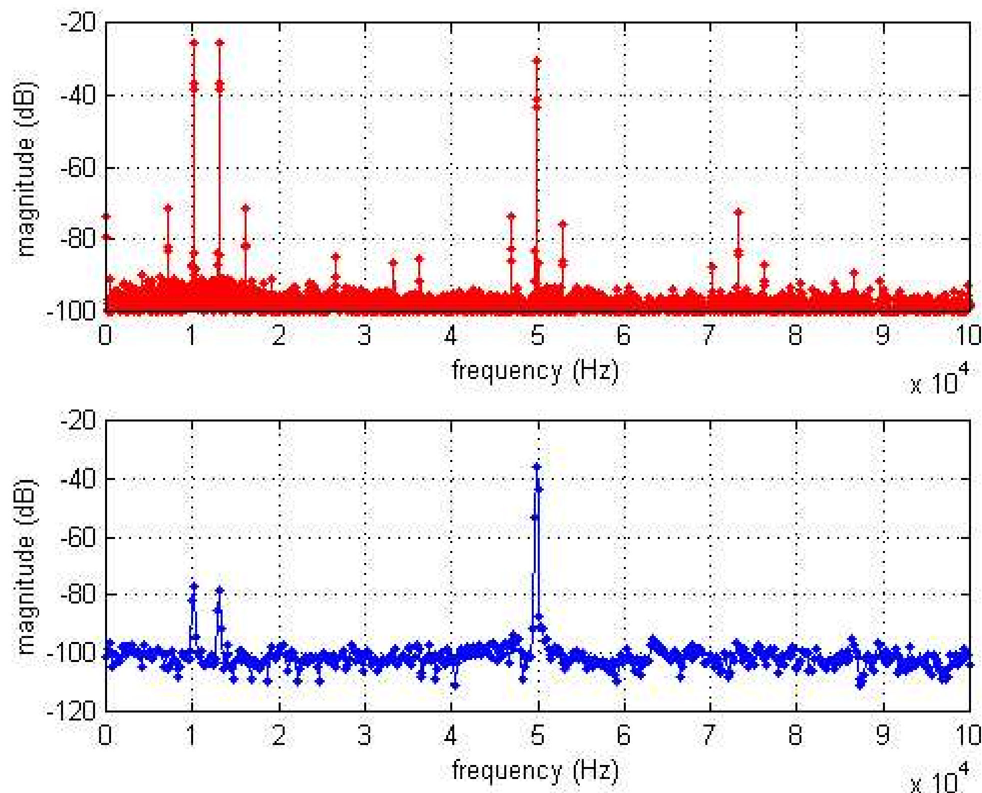


Figure 6.25: Spectra at the mixer output (lower) and filter output (upper) (NEGREIROS, 2004-a).

If one now changes the bias voltage of the mixer to 3.0V the intermodulation terms change, as it could be verified in the upper plot of Figure 6.26. If one goes further and changes the filter cutoff frequency to 35.6kHz the results shown in the lower trace of Figure 6.26 indicate a significant increase in the local oscillator magnitude, as the filter attenuation is greatly reduced at the oscillator frequency.

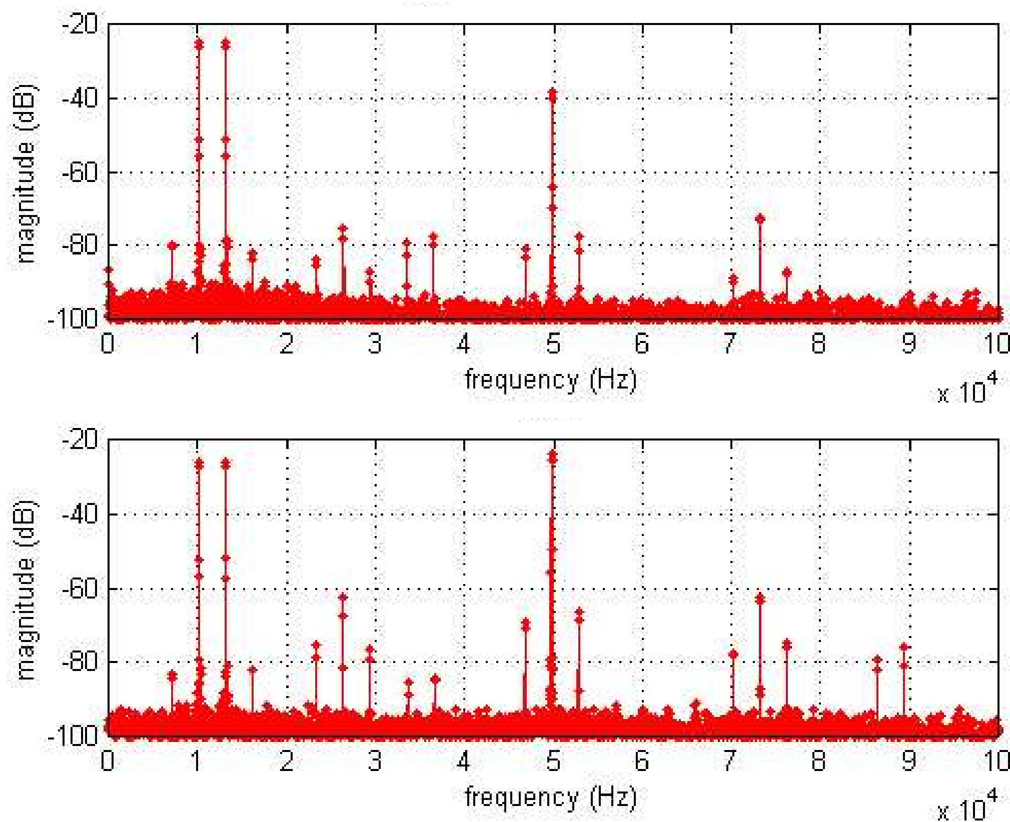


Figure 6.26: Spectra at the mixer output for 3.0V(upper) and for different filter (lower) (NEGREIROS, 2004-a).

6.4.3.2 Testing a mixer at 100MHz

In order to verify the applicability of the approach to more realistic circuits, a prototype mixer and a local oscillator circuit running at 100MHz were built using discrete RF components (see Figure 6.27). Fast voltage comparators (2.5ns propagation delay) (ANALOG DEVICES, 2001) were used to implement the statistical sampler, allowing the observation of the signals at the output of the mixer. A logic analyzer was connected to the comparators output in order to acquire the resulting bit stream (digital data was sampled at 400MS/s). Data was transferred to a PC and analyzed using Matlab. The block diagram of the measurement setup is shown in Figure 6.28.

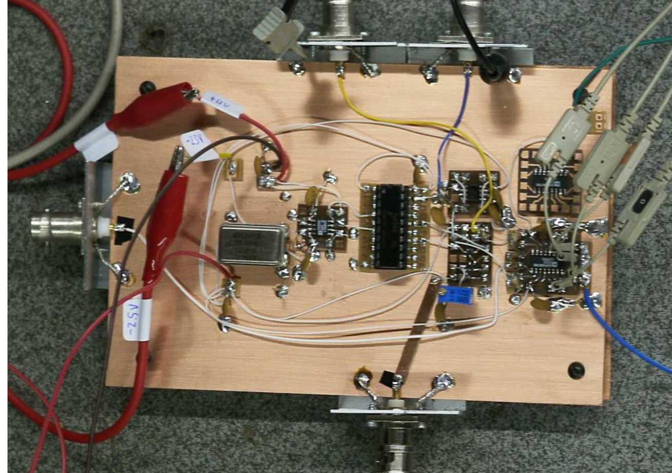


Figure 6.27: Prototyped mixer board (NEGREIROS, 2004-a).

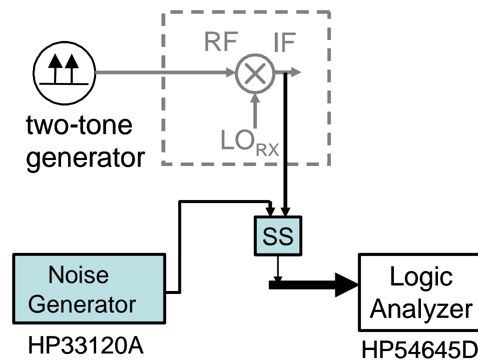


Figure 6.28: Block diagram of experimental setup.

After applying two tones at 101.00 MHz and 101.06 MHz, diverse harmonics are expected at the output of the mixer. This is confirmed by the output of the spectrum analyzer (Anritsu, MS2711) in Figure 6.29.

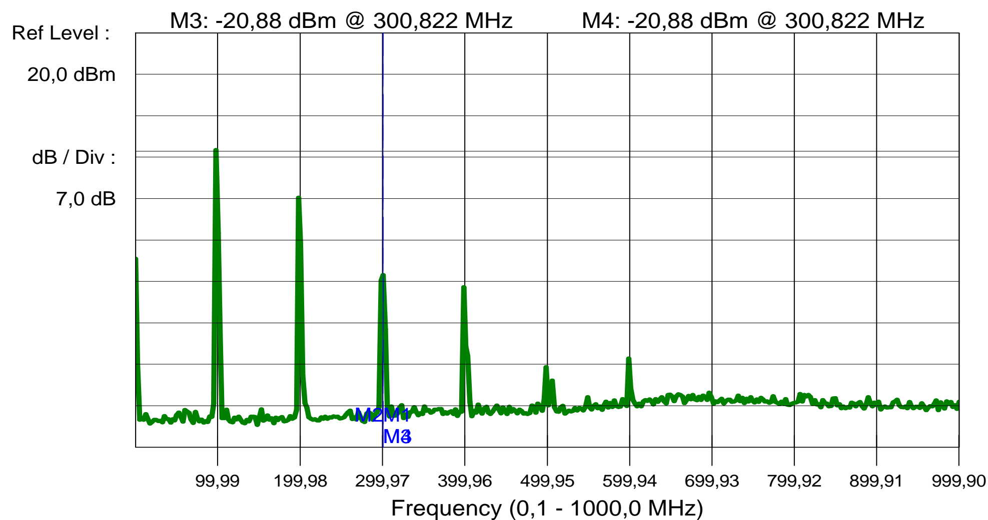


Figure 6.29: Spectral analysis of mixer output (NEGREIROS, 2004-a).

As the local oscillator is running at 100MHz, the two-tones should be down-converted to the 1.00MHz and 1.06MHz bands. The results of observing this frequency

band using the spectrum analyzer are presented in Figure 6.30. The large intermodulation distortion components were already present in the original input signal to the mixer.

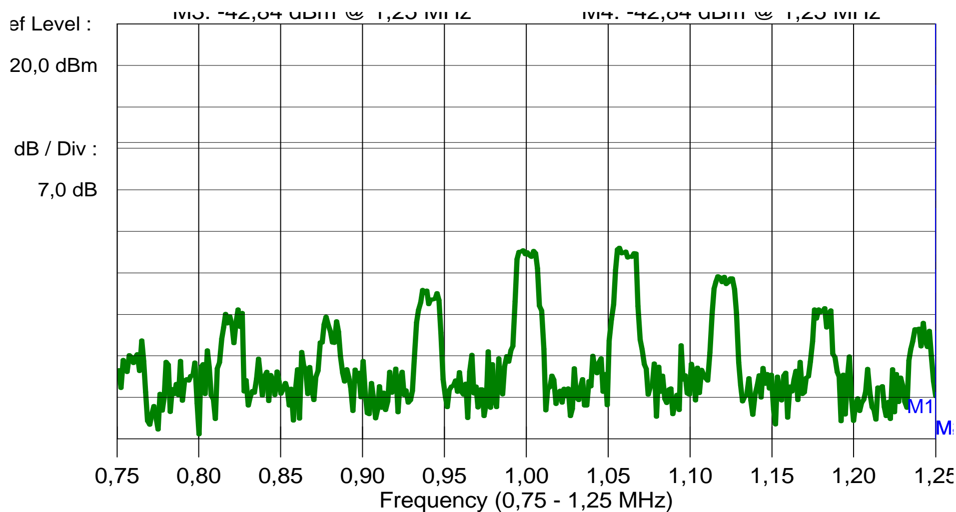


Figure 6.30: Spectral analysis of mixer output (NEGREIROS, 2004-a).

The same frequency band was analyzed using the output of the comparators and produced the results shown in Figure 6.31. This figure also shows results after changing the bias voltage of the active mixer, simulating a parametric fault. One can clearly distinguish the two traces in the figure, confirming that the use of the statistical sampler to probe non-linear circuits is a valid test approach.

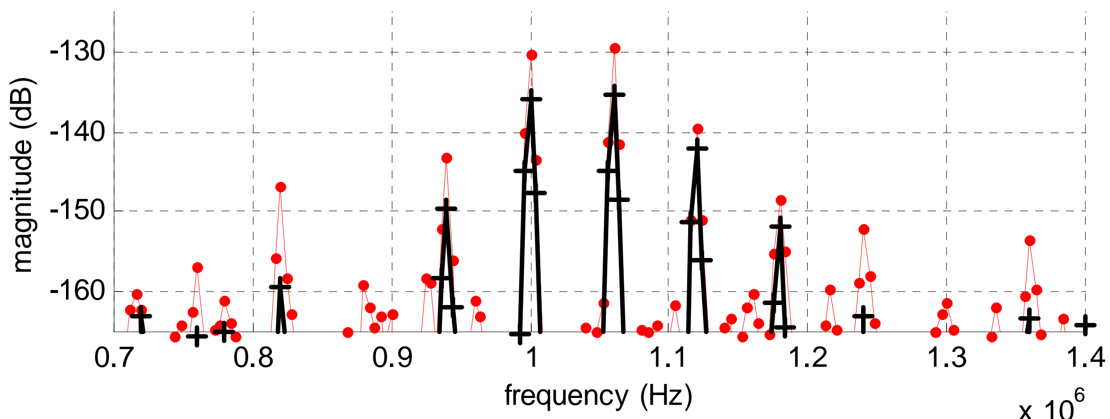


Figure 6.31: Spectral analysis of mixer output (NEGREIROS, 2004-a).

6.4.3.3 Analyzing higher frequencies

As the data acquisition system runs at 400MS/s, the maximum bandwidth is around 200MHz. We have changed the local oscillator circuit from 100MHz to 80MHz to allow acquisitions at higher frequencies around 180MHz, using the same input signals. An analog fault was simulated by changing the bias voltage of the mixer. This could be caused by any deviation in the bias circuit of a mixer (a fault in a resistor of the voltage divider). The effects are different circuit behavior because of linearity and gain characteristics. In Figure 6.32 the spectral analysis performed using a spectral analyzer is shown, and the same frequency range is analyzed with statistical sampler data in Figure 6.33.

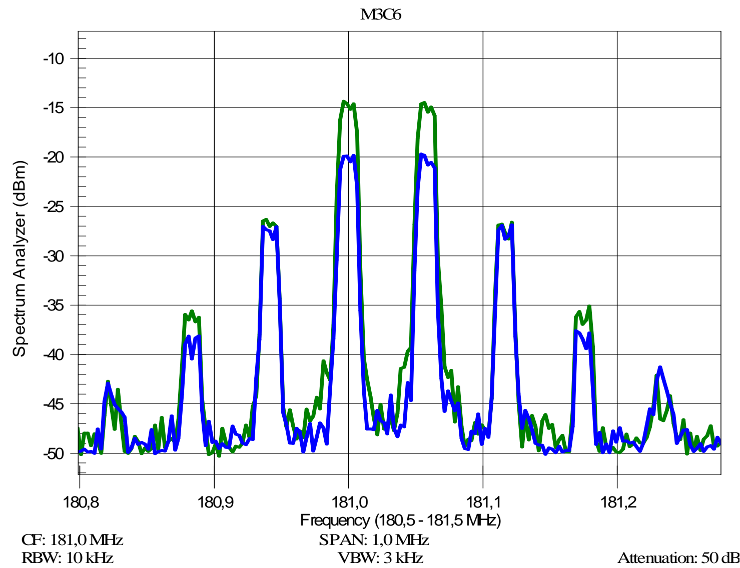


Figure 6.32: Spectral analyzer output around 181 MHz (NEGREIROS, 2004-b).

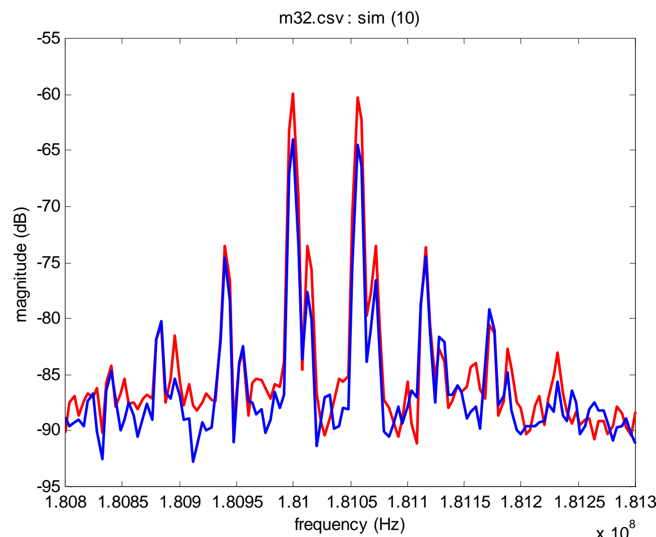


Figure 6.33: Spectral analysis using sampler data (NEGREIROS, 2004-b).

6.4.4 Analysis

The insertion of low cost sampler in the RF path has key advantages when compared to a loopback approach: less reconfiguration, constant loading for the analog circuit, an increase in observation and circuit partitioning capabilities.

Simulation and practical results have shown that it is possible to use the approach to verify spectral dependent parameters like IP3. The use of a voltage comparator as a 1-bit sampler enables the construction of high speed acquisition systems, making it more realistic to sample signals at IF and RF. Another advantage is that sub-sampling techniques can be used with this sampler, and could be used in a way to provide a signature for the mixer and other blocks (as shown in section 6.3 (NEGREIROS, 2003-f)).

The analog noise generator needed for the samplers can be realized with little analog overhead (FLORES, 2002; FLORES, 2004), as only one generator is needed for all

samplers. One issue is that the amplitude of the noise should be greater than or equal to the amplitude of the signal being measured, at each test point.

The application of the test signal has not been addressed yet, and should be provided by a stand-alone generator (like the one proposed in (VEILLETTE, 1995)), or by deviating the transmitter signal to the receiver using some kind of loopback technique. The main advantage of the proposed test technique over loopback is the increased observation capability enabled by the use of the sampler. This approach would be able to detect a faulty transmitter that outputs a tone at an out-of-band frequency, for example.

6.5 Low Cost On-Line Testing of RF Circuits

On line test strategies are generally not able to take advantage of systems resources, since the circuit is in normal operation. This means that online test comes at an extra price, the introduction of extra circuitry. As far as analog observers are regarded, the introduction of extra high speed analog to digital converters could lead to a great analog area overhead and increased cost.

In this work, our goal is to allow online testing, but maintain development costs and analog area overhead to a minimum. This can be achieved through the use of the statistical sampler, extending previous work from chapter 4 to the domain of RF circuits. Specifically, more in-depth discussion regarding test overhead and low cost processing is presented, together with additional experimental results. The use of a real application illustrates the trade-off between test response time and overhead, which can be easily achieved with the proposed test strategy.

6.5.1 On-line test approach

In chapter 4 an on-line test strategy for analog circuits based on spectral analysis was presented. In Figure 6.34 the required power spectrum density estimates are shown.

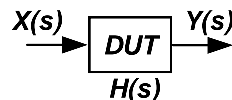


Figure 6.34: On-line PSD estimates (X(s), Y(s)) required by the test method.

For linear analog circuits, the PSD allows the on-line identification of the transfer function of the linear system represented by the analog circuit. The transfer function H(s) can be obtained, over the bandwidth of the input signal, by the ratio of the power spectrum of the output and input to the system, as shown in Equation 6.8.

$$H(s) = \frac{Y(s)}{X(s)} \tag{6.8}$$

The test strategy for linear analog circuits is basically the comparison of the expected and estimated transfer functions. Under normal operation of the system, the ratio of the PSDs for the circuit under test is estimated and compared to the signature of the fault-free circuit. This ratio should be evaluated over the bandwidth of the input signal to the system, to assure that a suitable signal to noise ratio is achieved.

For RF analog circuits, however, non-linear behavior is expected from some components like mixers and amplifiers, and should be under certain limits. This way, a

more generic test framework should be used, like a non-linear model. The test strategy is still PSD-based, as important characterization parameters like third-order intercept point (IP3) and even noise figure can be evaluated using PSD data.

More specific strategies can be developed according to system requirements. The specific strategy depends on the component or analog block being tested. For example, in the case of an oscillator, frequency and amplitude should be within a given tolerance range. This can be evaluated analyzing directly the PSD data. For an amplifier or filter, the input and output should be evaluated over the required frequency bands, in order to verify the functional behavior of the block, as long as an acceptable margin for errors. For a 3-port device like the mixer, monitoring of the local oscillator and the expected frequency bands will give indication of its behavior.

The use of the statistical sampler makes possible the analysis of input and output signals of an analog block in the system, and the verification of its functional behavior. This behavior could be validated by a functional model of the analog block. The model could be the transfer function (for linear analog blocks, like in chapter 4) specific characteristics of non-linear analog blocks (like second and third order distortion).

6.5.2 Test scenarios

As the output of the statistical sampler is a completely digital signal, it can be easily interfaced to the digital part of the System-on-Chip.

A general test scenario is shown in Figure 6.35, where an analog core is shown, together with other typical SoC components. The output of the statistical sampler core could be processed by local SoC resources. This would be the situation where sufficient memory and processing resources are available (which could be the case for large time intervals between test results or test parameter evaluation), and no dedicated extra processor or memory would be needed. This configuration would also be used in the implementation of off-line BIST.

In a general case, however, a test analyzer should be incorporated in the SoC. This test analyzer comprises basically an FFT analyzer and memory for the 1-bit data acquisitions, FFT results and circuit signatures.

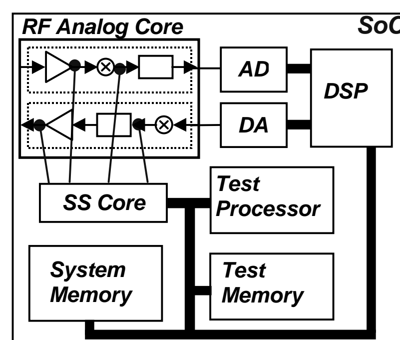


Figure 6.35: General test scenario (NEGREIROS, 2005-c).

A possible test core implementation is shown in Figure 6.36, where an analog noise generator is connected to the reference levels of the samplers. The output of each sampler is connected directly to a data bus. Timing is controlled by an acquisition control block.

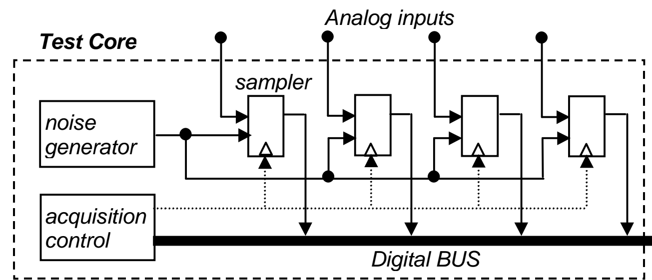


Figure 6.36: Example test core (NEGREIROS, 2005-c).

The test itself is carried in the following way. Using the statistical sampler one obtains data to compute the FFT of any point required in the circuit. This frequency domain information is compared to a good one, previously stored as a signature in an extra memory. The threshold defining whether a circuit is malfunctioning or not must be previously defined by simulations, taking into account process deviation.

It is important to notice that the number of points of the FFT is directly connected with the required resolution when comparing to the previously stored signature. As the number of points increases, so increases the resolution, but the longer the test, as it will be commented in the next section. Moreover, since we are using a black box window, the signature threshold must also take into account the windowing effect. This allows one to acquire any number of points, without the need for synchronous sampling data using an integer number of periods, what would be difficult to achieve in the field.

6.5.3 RF test example

In order to illustrate the test approach, an experimental setup using a non-controlled input signal was prepared. It consists of an upconverter mixer, with an AM modulated signal as input. The input signal is built using a signal generator with an audio signal as input and a 500kHz sine wave as the carrier. The mixer should shift the frequency contents of its input to 80MHz, as illustrated in Figure 6.37.

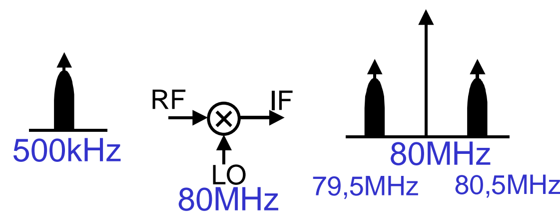


Figure 6.37: Upconvertion example (NEGREIROS, 2005-c).

The equipment used and their connection is shown in Figure 6.38 (for the measurement at the output of the mixer). The prototyped board contains the mixer, the local oscillator circuit and the high-speed voltage comparator. An additional noise generator is needed. Also, for the data acquisition, a mixed-signal scope with logic analyzer was used. Digital data was sampled at 400MS/s and transferred to a computer. Analysis was performed under Matlab. The schematic of the mixer is shown in Figure 6.39. In Figure 6.27 a photograph of the mixer board was already presented.

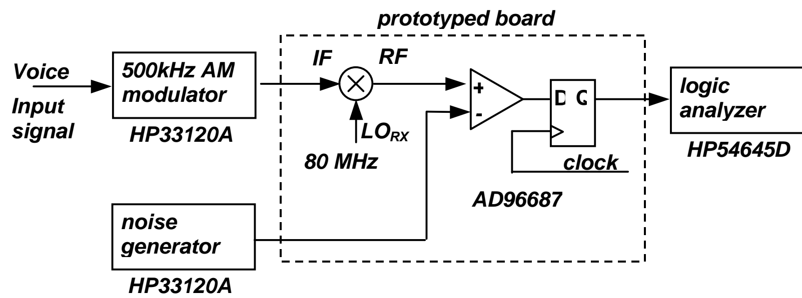


Figure 6.38: Diagram of experimental setup and equipment used (NEGREIROS, 2005-c).

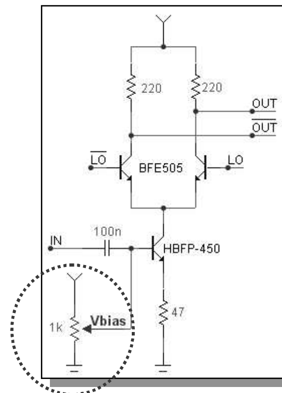


Figure 6.39: Schematic circuit of prototyped mixer, showing the bias circuit that was used in order to simulate an analog fault (NEGREIROS, 2005-c).

For the current example, total data acquired for each channel was 500e3 1-bit samples. The FFT used 10e3 samples. For evaluation of the PSD, 50 FFTs were performed and their mean was taken (HAYES, 1996).

By connecting the sampler to the input of the mixer, one should be able to analyze the spectra of the input signal. This was done in Figure 6.40, where the input data signal to the 500kHz modulator was removed in order to demonstrate the effects on the PSD. One can notice the correct frequency and different amplitudes for each case. This example is similar to monitoring an oscillator, as the signal band is small compared to the carrier frequency.

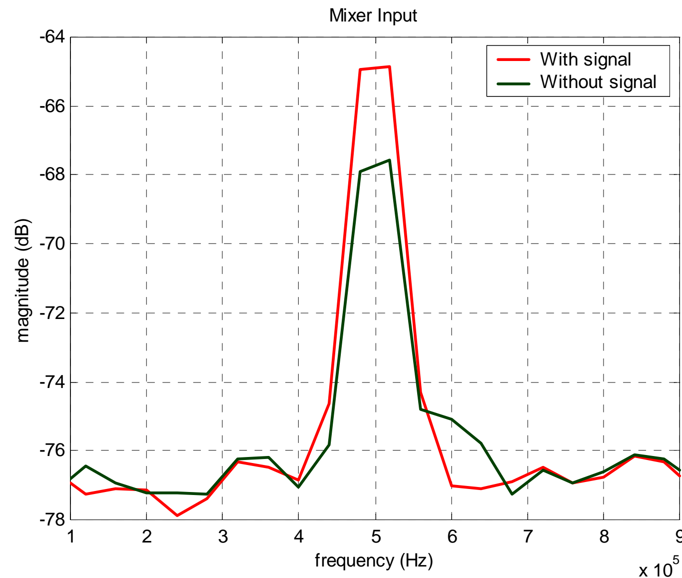


Figure 6.40: Mixer input: AM signal, with and without modulating signal (NEGREIROS, 2005-c).

By using the connections shown in Figure 6.38, one should be able to analyze the spectra of the output of the mixer. If an analog fault is inserted in the mixer, one should be able to observe it through the PSD. In order to simulate an analog fault, the bias voltage of the mixer was changed (as in Figure 6.39). Results are presented in Figure 6.41.

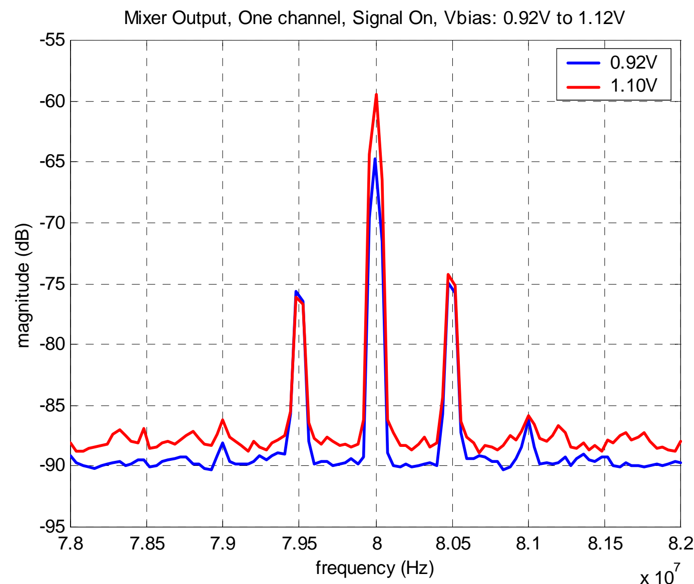


Figure 6.41: Mixer output: AM signal translated to 80 MHz, for two different biasing voltages of the mixer - note amplitude variation of the main carrier (NEGREIROS, 2005-c).

One should also be able to distinguish faults in the mixer from the PSD obtained from different input signal levels. It should be noted that the carrier level is not influenced by the input signal, as shown in Figure 6.42, where the input signal levels where changed. Likewise, changes in IIP3 and Noise Figure will cause changes in the frequency spectra, and can be detected by the technique.

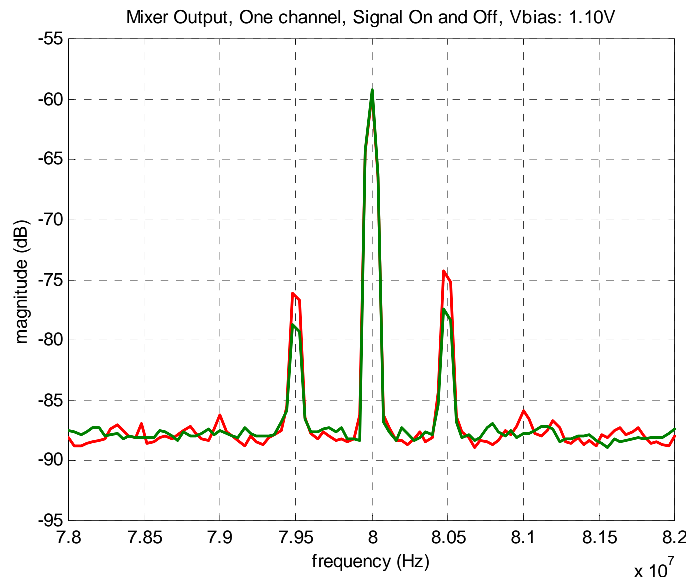


Figure 6.42: Mixer output: AM signal translated to 80 MHz, for different input signal conditions: with and without a modulating signal. Note amplitude variation of the side bands (NEGREIROS, 2005-c).

6.5.4 Analysis of test overhead

In this section an analysis of the overhead caused by the application of the test method is presented. Memory and processing overhead are analyzed, for a real application in the instrumentation domain, using a DSP processor platform. This allows one to focus the analysis, with real experimental data. It is shown that the technique allows the exploration of a design space in which there is a trade-off between test response time and application overhead.

6.5.4.1 Application resources

The application is an on-chip three-phase AC power analyzer that has a RF interface to an external device. A DSP-based power analyzer provides information for each phase (voltage and current signals) in a three-phase system. The analyzer enables the measurement of harmonics in industry power systems (SUTHERLAND, 1995). In the example this information is obtained from spectral analysis of the voltage and current waveforms.

For a FFT-based analyzer, the main tasks are signal acquisition, Fourier analysis using the FFT and evaluation of required parameters. The parameters include harmonic content of each signal, total harmonic distortion (THD), root-mean-square (RMS) value, power and power-factor. In a three-phase system, data from 6 channels (voltage and current of each phase) must be processed. The analyzer must be able to produce output measurements in a time slot of 100ms.

The example uses a fixed-point DSP processor (ANALOG DEVICES, 1995-b). In order to evaluate the test overhead, one should be able to identify the load of the application itself. In Table 6.3 the memory usage for data is detailed. The memory word length is 16 bits and the FFT size is 1024 points. The processor usage is shown in Table 6.4, and 28ms out of the 100ms available time slot are used. One should note that most overhead is because of the FFT evaluation, as detailed in Table 6.5.

Table 6.3: Memory (words) usage by the application.

Memory Usage	**length**	**no.**	**Total**	**%**
signal buffer	1,824	6	10,944	66
signal parameters	161	6	966	6
phase parameters	215	3	645	4
FFT data buffer	1,024	2	2,048	12
FFT coefficients	512	2	1,024	6
window coefficients	1,024	1	1,024	6
TOTAL	-	-	16,651	100

Source: NEGREIROS, 2005-c.

Table 6.4: Processor usage (cycles and time) by the application in a time slot of 100ms (Fclock=33MHz).

Routine	**cycles**	**no.**	**total cycles**	**total time (μs)**
signal processing	152,771	6	916,626	27,777
phase processing	2,902	3	8,706	263
Total	-	-	925,332	28,040

Source: NEGREIROS, 2005-c.

Table 6.5: Detailed processor usage in the signal processing routine (Fclock=33MHz).

Subroutine	**Cycles**	**Time (μs)**	**%**
window	2,063	62.5	1.4
scramble	2,060	62.4	1.4
init. FFT	3,096	93.8	2.0
FFT	88,408	2,679.0	57.9
Modulo	28,033	849.0	18.3
Phase	20,752	628.8	13.6
Peak detect	6,749	204.0	4.4
Peak Interp.	1,008	30.5	0.6
RMS,THD	602	18.2	0.4
Total	152,771	4,629.4	100

Source: NEGREIROS, 2005-c.

6.5.4.2 Test requirements

The overhead of the test will be the additional memory and processing resources required. As an estimate of the power spectrum density is required, signal processing for each analog test input is as shown in Figure 6.43. Input data is a length-M single bit vector from the statistical sampler. The modulo of the FFT is evaluated, and a mean value is then obtained. After that, the test processor is able to compare the PSDs of the observed test points.

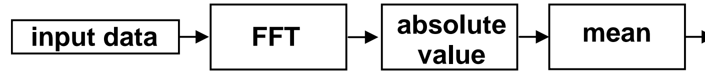


Figure 6.43: Data processing required by each test input (NEGREIROS, 2005-c).

For on-line monitoring of an oscillator, a single input test would be enough. For a 2-port device, two analog inputs would be required. In Table 6.6 the memory requirements for implementing the data processing scheme from Figure 6.43 are shown. The implementation of the *mean* block was done using a simple accumulation approach, like an IIR filter. It is interesting to observe that memory is linear with the number of test inputs.

Table 6.6: Memory (words) required by the test, for a M-length FFT and P test inputs.

Memory Usage	**length**	**no.**	**Total**
input data	M/16	P	P*M/16
FFT data buffer	M	2	2*M
FFT coefficients	M/2	2	M
Mean	M/2	P	P*M/2
TOTAL	-	-	M*(3+9*P/16)

Source: NEGREIROS, 2005-c.

Processing requirements from Figure 6.43 are related to the FFT and modulo evaluation, as no windowing is required. Table 6.7 details the processing requirements per block, where K is the number of cycles needed by the implementation of the square root function in the DSP processor. One can only provide an estimate of the number of cycles, as it is very dependent on the DSP processor architecture and algorithm used (see Table 6.14).

Table 6.7: Test processing requirements for each input channel and M-length FFT.

Block	**Complexity**
FFT	O(M*log2(M))
Modulo	O(M/2*K)
Mean	O(M/2)

Source: NEGREIROS, 2005-c.

6.5.4.3 Test overhead

In this section we analyze some possible test implementation scenarios and their associated trade-offs, for the application described in section 6.5.4.1.

In order to obtain some numeric data, let M=1024. The memory overhead can be easily evaluated using Table 6.6. For the processor overhead and 1024 FFT size, one can use data from Table 6.5 to evaluate the number of cycles. We consider the *mean block* overhead to be 1024 cycles. This way, the processing overhead is given by 122,621*P cycles, where P is the number of test inputs. The evaluation of the test overhead for P=1, 2 and 3 is shown in Table 6.8.

Table 6.8: Application load and analog test overhead in a 100ms application time slot, for P test inputs and M=1024.

Case	App. load	Overhead P=1	Overhead P=2	Overhead P=3
Memory (words)	16,651	3,648 21.9%	4,224 25.4%	4,800 28.8%
Processor (cycles)	925,332	122,621 13.2%	245,242 26.5%	367,863 39.7%
Time (ms) f_{clk}=33MHz	28.0	3.7	7.4	11.1

Source: NEGREIROS, 2005-c.

Analyzing Table 6.8 one should note that the test processing overhead can reach a significant value for 2 and more input signals. Although the memory overhead is also significant, it grows slowly because of the single-bit nature of the input signal.

For higher resolution spectral analysis (which requires a greater M), the test overhead will increase. One could use data from Table 6.6 to evaluate memory usage of the test. For the processing resources, Table 6.7 could be used, but some correction factor is needed in order to translate complexity to number of processor cycles. We considered a factor of 2, as presented in Equation 6.9 (where K=50 and P=2), and hence

$$N_{cycles}=2*P*M*(\log_2(M)+ (K+1)/2) \quad (6.9)$$

The estimated processor and memory overhead for the implementation of the on-line test are shown in Table 6.9. The overhead for processor and memory may reach unacceptable levels for large M, the number of points in the FFT, and this is directly related to test quality. Some methods to alleviate this problem are discussed in the next section.

Table 6.9: Analog test overhead for 2 analog test points in a 100ms application time slot as a function of M.

Case	M=4,096	M=8,192	M=16,384
Memory (words)	16,896 101%	33,792 203%	67,584 406%
Processor (cycles)	614,400 66%	1,261,568 136%	2,588,672 280%
Time (ms) f_{clk}=33MHz	18.6	38.2	78.4

Source: NEGREIROS, 2005-c.

6.5.4.4 Reducing the test overhead

One way to reduce the test processing overhead is to increase test latency. For example, instead of having a test response at every 100ms, one could wait 1s or even 10 seconds. This way, the test processing overhead in each application time slot can be reduced by a significant amount, as illustrated in Table 6.10. This strategy can be used whenever an increase in test latency is acceptable.

The memory overhead is not directly affected by this strategy. However, if additional test time is available, a significant reduction in test memory (see Table 6.12)

could be achieved by calculating the FFT coefficients on the fly, instead of using a table in memory (for faster execution).

Table 6.10: Test processing overhead in a 100ms application time slot, for increased test response latency.

Latency	Overhead (%)		
(s)	M=4,096	M=8,192	M=16,384
0.1	66	136	280
1	6.6	13.6	28.0
10	0.7	1.4	2.8

Source: NEGREIROS, 2005-c.

The use of optimized FFT algorithms should also be considered, as their complexity in terms of real additions and products can be reduced, as illustrated in Table 6.11. Also, as DSP processors are able to evaluate multiplications and additions in a single cycle, some efficient algorithms have been proposed in the literature (SORENSEN, 1990; LI, 1986).

Table 6.11: Complexity of FFT algorithms in real operations (not complex), for 1024 data points.

Operation	radix-2	radix-4	split-radix
Multiplication	10,248	7,856	7,172
Addition	30,728	28,336	27,652

Source: LI, 2003.

A significant reduction in memory overhead can be achieved by the evaluation of the FFT for the real-data DFT, instead of the complex-data DFT (SMITH, 1997). This way, one can evaluate an M-point FFT of real data using FFT of M/2 complex data-points. If the FFT coefficients are evaluated on the fly, the overhead is further reduced, as presented in Table 6.12.

Table 6.12: Memory overhead of the test as a function of the FFT algorithm (for M=16384 and P=2)

FFT algorithm	**Memory Usage**	**Overhead reduction**
Complex FFT and twiddles in memory	M*(3+9*P/16)	0%
Complex FFT and twiddles on-the-fly	M*(2+9*P/16)	24%
Real FFT and twiddles in memory	M*(3/2+9*P/16)	36%
Real FFT and twiddles on-the-fly	M*(1+9*P/16)	48%

Source: NEGREIROS, 2005-c.

Another point that is worth noticing is that, for RF testing, one might be interested in only a small portion of the spectrum, centered around some frequency and with a high resolution. These requirements may lead to an increase in the number of FFT points, and also in the test overhead.

One solution to this problem would be the evaluation of the FFT only for those output points effectively needed. It turns out that there are some algorithms with this goal, as in (SORENSEN, 1993), where the main target has been the reduction of

computational load. This way, one can use smaller FFTs in order to obtain computational efficiency.

The minimal memory overhead seems to be achieved only by the use of the extremely inefficient DFT (in terms of computational complexity). If the coefficients are calculated on the fly, only the required number of output bins is required. This is shown in Table 6.13. For M=16384, P=2 analog test inputs and N=100 output bins, the memory overhead would be 2248 16-bit words (or a 13.5% overhead, considering the application load in Table 6.8). On the other hand, the processing complexity is in the order of O(2*100*16384) operations, disregarding the evaluation of the DFT coefficients. Other problems like round-off errors will impact the DFT method (SMITH, 1997).

Table 6.13: Memory (words) required by the test, for N DFT bins and P test inputs.

Memory Usage	length	no.	Total
input data	M/16	P	P*M/16
DFT output bins	N	1	N
Mean	N	P	P*N/2
TOTAL	-	-	P*N/2+N+P*M/16

Source: NEGREIROS, 2005-c.

Another factor that can influence the overhead of the method, for a given application time slot, is the DSP processor architecture. This can impact the performance of the algorithms, and is best illustrated by the number of cycles used in different benchmark implementations of the 1024 points FFT, as shown in Table 6.14. If one considers that current clock frequencies of DSP processors have reached 1GHz, even a small increase in test latency results in significant processing resources.

Table 6.14: 1024-points FFT (radix-4) in different DSP processors.

Processor	cycles
TI C6000 family, C62	13,237
AD ADSP 2187	34,625
TI TMS320C50	84,833
TI TMS320C25	113,467

Source: NEGREIROS, 2005-c.

6.5.5 Analysis

The results shown in section 6.5 have illustrated the idea of applying the statistical sampler to a RF test example. The effects of the analog faults injected in the mixer (by changing the bias voltage) could be the observed in the PSD performed using 1-bit data. Furthermore, signal amplitude changes could also be detected using the same strategy.

In order to perform on-line test, the analysis has been performed at specific signal bands. In the test strategy, one could also verify the PSD results against previously defined limits, or identify threshold settings based on the input PSD of the DUT and a behavioral model of the DUT, which could run in the test processor.

One should note that the statistical sampler enables the observation of the PSD of diverse test points. The specific on-line test strategy will be strictly dependent on the application, as the AM modulation example presented.

As the test is based on spectral analysis, a Fourier transform of the statistical sampler output is required. If one needs a higher spectral resolution in some frequency band, a large size FFT is likely to be needed.

In order to analyze the compromises between test and application resources, section 6.5.4 presented an example where an on-line test is implemented in a DSP processor, running a real life application. The trade-offs between processing and memory resources were shown to be related to the available time for test output evaluation, or test latency. Also, other factors like specific DSP platforms, algorithms and optimizations were addressed.

6.6 Conclusions

In this chapter we have applied the statistical sampler to the test of RF analog circuits. The typical RF signal path has been studied. After, a technique that reuses the ADC of the SoC in order to test the analogue interface has been developed, being based on subsampling. After that, the statistical sampler has been applied for BIST and on-line test scenarios.

Practical results have demonstrated the feasibility of using a low-cost 1-bit converter in test schemes for high frequency analog circuits, for both on-line and BIST. The proposed techniques are based on spectral analysis, extending the method presented in chapter 3.

In the next chapter we extend the capabilities of the proposed sampler in order to measure noise levels, allowing the evaluation of noise figure.

7 NOISE FIGURE

Noise figure is a key parameter in the design of low noise systems, like communication and instrumentation devices. For communication systems, the noise figure is used in the characterizations of the entire system, starting from components (like transistors) to complete functional blocks (like mixers and amplifiers). The noise figure of the whole communication system can be determined if the individual noise figures from the system components are known. Also, the sensitivity of the communication system can be determined from the knowledge of the bandwidth and noise figure (HEWLETT-PACKARD, 1983).

In this section we develop a measurement method for noise figure based on digital signal processing, suitable to be implemented in the SoC environment, as it reuses processing and memory resources already available in the SoC. A one-bit digitizer that is permanently connected to the desired analog test point is used, thus minimally disturbing the circuit under test. Thanks to the simplicity of the converter, low analog area overhead is obtained, and no impact is made on the noise figure of the circuit being tested, that is, the proposed BIST does not increase the noise level to be measured.

The ultimate goal of this work is to show that, by using the simple BIST cell presented in chapter 4, one can measure not only frequency related parameters of the circuit under test, but rather one can obtain information of other important characteristics like noise figure.

The first section presents a technical review of concepts regarding noise in analog circuits. Then, measurement techniques are presented and their suitability for implementation in the SoC environment is discussed. The Y-factor method is then discussed in more details, regarding practical implementation issues. After that a measurement technique based on reusing an ADC already present in the system is discussed. The chapter finishes with the development of a measurement technique based on the statistical sampler, providing practical results that indicate the performance of the method.

7.1 Noise in analog circuits

In this section some background information regarding noise characterization in analog circuits is provided. First noise figure is defined, and then measurement methods are presented.

7.1.1 Definitions

A common parameter used to characterize the noise behavior of an analog electric *signal* (such as the output of a sensor or amplifier) is the signal-to-noise ratio (SNR). It

is a ratio of the signal power to the noise power, expressed in dB, as shown in Equation 7.1. In this equation, V_S is the signal RMS value, and V_N is the noise RMS value.

$$SNR = 10 \cdot \log_{10}\left(\frac{V_S{}^2}{V_N{}^2}\right) \quad \text{dB} \tag{7.1}$$

Thermal Noise or Johnson Noise is the noise generated from a real resistor at a given temperature (MOTCHENBACHER, 1993). In Figure 7.1 it is illustrated the noise model of a real resistor.

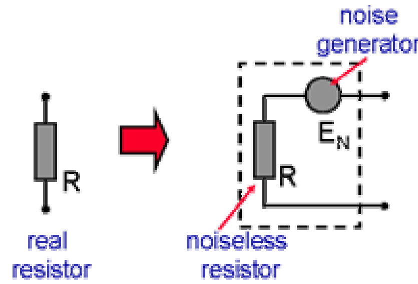


Figure 7.1: Noise model of a real resistor.

The noise generated depends on several factors, as shown in Equation 7.2. In this equation, T is the temperature in Kelvin, R is the resistance value in Ohms, B is the bandwidth being analyzed and k is the Boltzmann's Constant (1.38e-23). A 1kΩ resistor produces a noise voltage of 4nV rms when considering a bandwidth B of 1Hz and the standard temperature of 290K (17ºC).

$$E_N = \sqrt{4 \cdot k \cdot T \cdot R \cdot B} \tag{7.2}$$

Noise Figure (NF) and noise factor (F) are parameters used to characterize the noise behavior of a *device or circuit*. In Figure 7.2, the input signal to a device comes from a real resistor with resistance R_S at temperature of 290K.

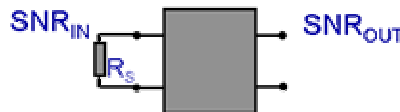


Figure 7.2: Noise characterization of a 2-port device.

The following is the definition of Noise Factor:

> "Noise factor (F) of a two-port device is the ratio of the available output noise power per unit bandwidth to the noise caused by the actual source connected to the input terminals of the device, measured at the standard temperature of 290K" (HEWLETT-PACKARD,1983).

The expression for the Noise Factor is given by

$$F = \frac{SNR_{IN}}{SNR_{OUT}} \tag{7.3}$$

The `noise figure` (NF) is defined as the `noise factor` (F) in dB (HEWLETT-PACKARD, 1983; MOTCHENBACHER, 1993). In (RAZAVI, 1998) no similar distinction is made.

$$NF = 10 \cdot \log_{10}(F) \quad dB \tag{7.4}$$

The IEEE standard definition (from (HEWLETT-PACKARD,1983)) is given by Equation 7.3, where $\mathbf{N_a}$ is the noise added by system, $\mathbf{T_0}$ is 290K (standard temperature), **B** is the system bandwidth, **k** is the Boltzmann constant and **G** is the gain of the system.

$$F = \frac{N_a + k \cdot T_0 \cdot B \cdot G}{k \cdot T_0 \cdot B \cdot G} \tag{7.5}$$

The definition of noise figure is based on the assumption of a linear system. Some extensions for non-linear systems have been proposed, like in (GEENS, 2001), but are not going to be analyzed in this work.

Some usual noise figure values are illustrated in Table 7.1, together with the corresponding noise factor. Note that the typical value of noise figure for an RF low noise amplifier is 3dB. For an RF mixer, the value is about 10 dB. A circuit that does not add noise to its input would have a noise figure of 0 dB.

Table 7.1: Some reference values for noise figure and noise factor.

NF(dB)	F	Example
0	1	noiseless analog circuit
3	2	RF low noise amplifier
10	10	RF mixer

Source: RAZAVI, 1998.

Another definition is the `noise temperature`, which is the temperature of the source resistance that generates thermal noise equal to the device noise, as shown in Figure 7.3.

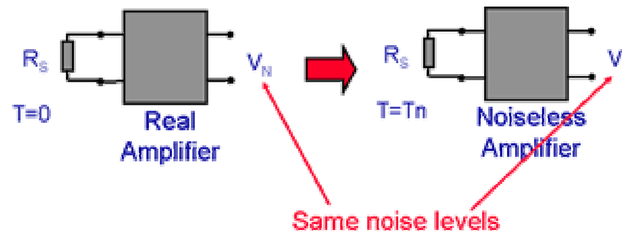


Figure 7.3: Noise temperature of an amplifier.

Regarding a cascade of blocks, the noise figure would be mostly influenced by the first block if the gain of this block is large, according to the Friis formula expressed in Equation 7.6 and illustrated in Figure 7.4 (MOTCHENBACHER, 1993).

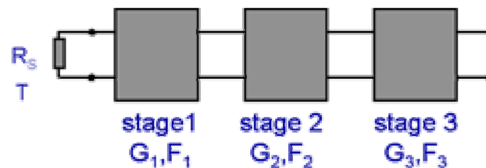


Figure 7.4: Noise in cascaded stages.

$$F_{123} = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} \tag{7.6}$$

7.1.2 Measurement Techniques

Some methods have been developed in order to evaluate the noise figure of the system under test. The methods are based on the application of a known signal (noise and/or sinusoidal) and measurement of the output of the system, as shown in Figure 7.5.

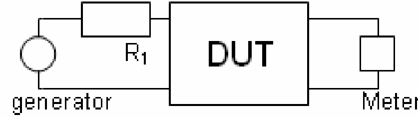


Figure 7.5: General noise figure measurement setup.

7.1.2.1 Direct Noise Measurement Method

In this method the signal generator is not used. A load is connected to the input of the system, at a temperature of 290K. The meter reading gives the output noise power of the DUT (numerator of Equation 7.5). If one knows the measurement bandwidth (B) and the gain of the DUT (G), the denominator in Equation 7.5 can be determined and the noise factor is evaluated directly (HEWLETT-PACKARD, 1983).

7.1.2.2 Signal Generator Twice Power Method

In this method a two-step process is required: first, the output power is measured with a load connected to the input of the system at a temperature of 290K. Then, a signal generator is connected (as in Figure 7.5) and its output power is adjusted in order to produce a 3dB increase in the output power of the DUT. If one knows the generator power level and measurement bandwidth, one can use Equation 7.7 to obtain the noise figure, without knowledge of the DUT gain (HEWLETT-PACKARD, 1983).

$$F = \frac{P_{gen}}{k \cdot T_0 \cdot B} \tag{7.7}$$

7.1.2.3 The Y-Factor Method

This method is based on the use of a calibrated noise source, and is used in commercial noise figure analyzers (HEWLETT-PACKARD, 1983). A calibrated noise source is usually a reverse-biased diode noise source (HEWLETT-PACKARD, 1983). The method is also a two-step process: with the noise source turned off (at a temperature of 290K, or cold temperature), the DUT output power - $\mathbf{N_c}$ - is measured. Then the noise generator is turned on, and the noise output power - $\mathbf{N_h}$ - for the hot temperature is recorded. The Y factor is the ratio of these powers:

$$Y = \frac{N_h}{N_c} \tag{7.8}$$

Knowing that the noise power at the output of the DUT is simply the noise added by the system (N_a) plus the amplified input noise, one can write

$$N_h = k \cdot T_h \cdot B \cdot G + N_a \tag{7.9}$$

$$N_c = k \cdot T_c \cdot B \cdot G + N_a \tag{7.10}$$

After applying Equations 7.9 and 7.10 to Equation 7.8 and developing using Equation 7.5, one obtains the Y-Factor formula (COLLANTES, 2002),

$$F = \frac{\left(\frac{T_h}{T_0} - 1\right) - Y\left(\frac{T_c}{T_0} - 1\right)}{Y - 1} \tag{7.11}$$

T_0 is the reference temperature of 290K. If the noise source cold temperature is not 290K, this provides a correction term. This equation can be rewritten in order to take into account the noise powers, instead of temperatures (GEENS, 2001), as shown in Equation 7.12.

$$F = \frac{\left(\frac{N_h}{N_0} - 1\right) - Y\left(\frac{N_c}{N_0} - 1\right)}{Y - 1} \tag{7.12}$$

7.1.3 Noise Figure Techniques for BIST

The use of embedded noise sources for noise figure measurements has already been reported. In (BELAND, 1999) a thin-film resistor has been used as an on-wafer noise source. Diode noise sources have been investigated in (RANDA, 1999). To the authors' knowledge no technique dedicated to BIST has been proposed. A production test scheme based on signature testing has been proposed in (VOORAKARANAM, 2002), where noise figure measurements have been indirectly made.

7.2 A NF BIST in the SoC environment

In this section the implementation of methods for estimating noise figure suitable for BIST in a SoC environment are discussed.

7.2.1 Direct method

An implementation of the direct method would be as shown in Figure 7.6. A nominal load R_s must be applied at the input at a temperature of T_0=290K. The output of the DUT must be amplified and routed to the ADC of the system for further processing.

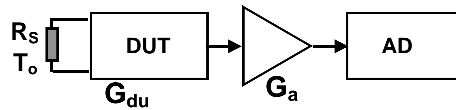


Figure 7.6: Direct method setup (NEGREIROS, 2005-a).

One practical disadvantage of this setup is related to variations in the gain of the amplifier (G_a). This gain multiplies both terms in Equation 7.13, but only the numerator is measured. This way, any deviation in the amplifier gain (from G_a to G_a') will cause an error in the noise factor estimation. This issue is expected to occur because of process variations that may affect the gain of the amplifier.

$$F = \frac{(N_a + k \cdot T_o \cdot B \cdot G_{DUT})G_a'}{k \cdot T_o \cdot B \cdot G_{DUT} \cdot G_a} \tag{7.13}$$

7.2.2 Y-factor method

If one could embed a suitable noise generator, being able to provide two known noise levels, it would be feasible to implement a noise figure measuring system based

on the Y-factor technique. The system level setup is presented in Figure 7.7. A programmable attenuator provides the noise levels needed for the NF measurement. The generator noise level can be measured through an auxiliary analog path to the ADC.

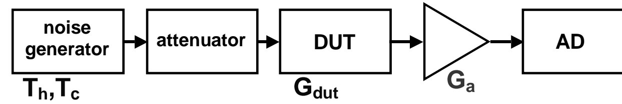


Figure 7.7: Y-factor setup (NEGREIROS, 2005-a).

This setup does not possess the same sensitivity to changes in the amplifier gain as the direct method. Both numerator and denominator in Equation 7.14 are measured, so any deviations in the amplifier gain (from G_a to G_a') are corrected.

$$Y = \frac{(N_a + k \cdot T_h \cdot B \cdot G_{DUT})G_a'}{(N_a + k \cdot T_c \cdot B \cdot G_{DUT})G_a'} \tag{7.14}$$

In the next section an analysis of uncertainty in commercial noise sources is provided, and it is shown that even large errors like 5% in the hot temperature can still provide useful measurements for noise figure estimation, if an error of ±0.3dB is acceptable (for noise figures of 3dB and 10dB). These errors could be used as guidelines in the design of the noise generator and attenuator.

7.3 Practical issues in the Y-factor method

In this section some results regarding value and accuracy of noise temperatures and its impact on noise figure measurements are discussed.

7.3.1 Noise temperature values

In Table 7.2 simulation results are presented regarding a unit gain amplifier with a fixed 10dB noise figure. The simulation used T_h=10000K and the Y factor method. Evaluation of output power was made using 10000 samples from the DUT output for the given cold temperature.

By looking at the NF error presented in Table 7.2, one can notice that the error increases as the Y factor approaches unity. On the other hand, noise figure errors of less than 0.1 dB could be obtained using higher noise temperatures for the `cold` measurement.

Table 7.2: Noise figure measurements for a 10dB noise figure device and for different values of T_c.

T_c (K)	Y	F	NF (dB)	NF Error (dB) mean	NF Error (dB) deviation
290	4.3	10.02	10.0082	0.0284	0.0364
1000	3.49	9.98	9.9936	0.0280	0.0364
5000	1.66	9.99	9.9918	0.1405	0.1896
9000	1.08	10.59	9.8528	1.5497	2.0904

Source: NEGREIROS, 2004-c.

7.3.2 Noise temperature accuracy

In this section we are interested in obtaining the noise temperature accuracy from the specifications of commercial noise sources (HEWLETT-PACKARD, 1989; AGILENT, 2002). In Table 7.3 some noise sources are presented, with its ENR (excess noise ratio) value and associated uncertainty.

The ENR is defined as shown in Equation 7.15. T_c is assumed to be 290K (T_0) when it is calibrated (HEWLETT-PACKARD, 1983).

$$ENR = 10 \cdot \log_{10}\left(\frac{T_h - T_c}{T_0}\right) \quad dB \tag{7.15a}$$

$$ENR = 10 \cdot \log_{10}\left(\frac{T_h}{T_0 - 1}\right) \quad dB \tag{7.15b}$$

According to Equation 7.15b, if one knows the ENR of a given noise source, then it is easy to estimate the values of the noise temperatures. As shown in Table 7.3, for a 15dB noise source the ENR is about 32, so the hot temperature is about 30 times T_0. For a 3dB noise source the hot temperature is about 5 times T_0.

Table 7.3: Noise sources specifications and ENR ranges.

noise source	ENR	Uncertainty	ENR values (linear)		
	(dB)	(dB)	min.	nom.	max.
N4001A	15	0.14	30.62	31.62	32.66
346B	15	0.24	29.92	31.62	33.42
N4000A	6	0.16	3.84	3.98	4.13
346A	6	0.25	3.76	3.98	4.22

Source: NEGREIROS, 2004-c.

If we assume that all uncertainty is associated to the hot temperature, we could estimate a percent error in the hot temperature itself, for the commercial noise sources. This is presented in Table 7.4. For example, a 6dB ENR noise source has a nominal T_h of $4.98T_0$ or 1444.2K (for T_c=T_0=290K). The +5% error means that the real temperature could be 1516.41K. Note that noise temperature is equivalent to noise power (in the context of Equation 7.12).

Table 7.4: Worst case percent uncertainty in T_h.

noise source	error (%)
N4001A	± 3
346B	± 5
N4000A	± 3
346A	± 5

Source: NEGREIROS, 2004-c.

7.3.3 Effect of temperature uncertainty in noise figure evaluation

In this section we analyze the effects of uncertainty in T_h in the evaluation of two different noise figure levels: a 3 dB device (ex.: low noise amplifier) and 10dB device (ex.: mixer).

Variations of ± 5% have been used in T_h, justified by the results in Table 7.4. For a 3dB noise figure device (like a low noise amplifier), results are shown in Figure 7.8. The noise source has a 6dB ENR. Analysis of Figure 7.8 reveals that the maximum error in the noise figure estimation is about ± 0.3 dB, for a 3dB nominal noise figure value.

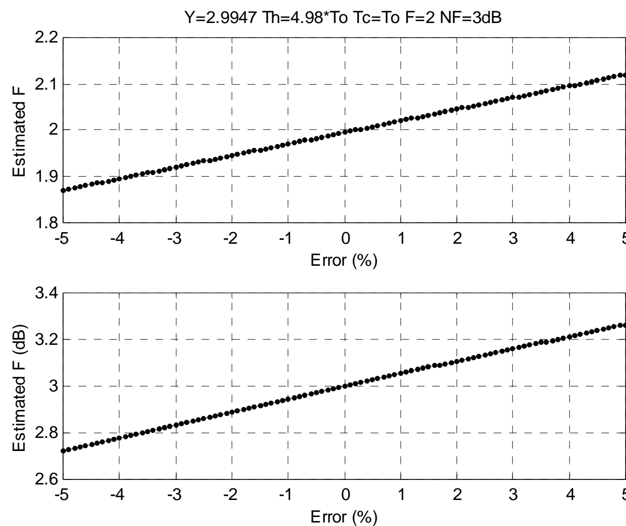


Figure 7.8: Effect of T_h variation in noise factor (up) and noise figure (down) for a 3dB nominal noise figure (NEGREIROS, 2004-c).

In Figure 7.9 a 10dB nominal noise figure device (like a mixer) was simulated, and the error obtained for the same temperature variations is shown. The maximum error is about ± 0.3 dB.

We conclude that even large errors like 5% in the hot temperature can still provide useful measurements for noise figure estimation, if an error of ± 0.3 dB is acceptable.

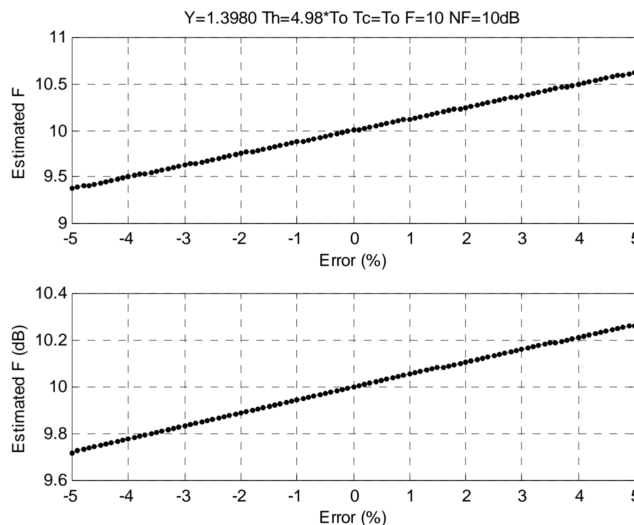


Figure 7.9: Effect of T_h variation in noise factor (up) and noise figure (down) for a 10dB nominal noise figure (NEGREIROS, 2004-c).

7.4 A method for noise figure BIST reusing the ADC of the system

In this section we discuss a method for estimating noise figure suitable for BIST in a SoC environment. One can notice that current SoCs have plenty of processing and memory resources. Also, digital to analog converters (ADC and DAC) are expected to exist.

If one could embed a suitable noise generator, being able to provide two known noise levels (with bounded error levels of about 5%), it would be feasible to implement a noise figure measuring system. The system level setup is presented in Figure 7.10. A programmable attenuator provides the noise levels needed for the NF measurement. The generator noise level is measured through an auxiliary analog path to the ADC. This setup provides a way to evaluate the ENR of the noise source, as one is able to estimate the error in the attenuators.

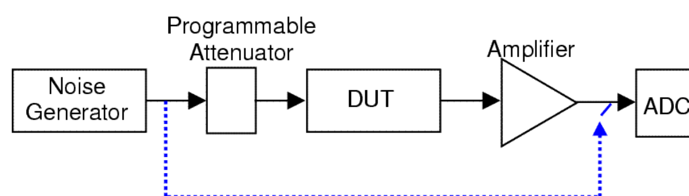


Figure 7.10: Noise figure BIST (NEGREIROS, 2004-c).

The power meter or spectrum analyzer can be built using resources already available in the SoC: analog to digital converter, memory and processor. Observability of the analog circuitry can be increased by the use of muxes and analog routing to additional analog test points.

The injection of the noise signal in a specific point in the circuit is an issue. The use of circuit reconfiguration is not recommended because of the analog path degradation introduced by muxes and switches. An ideal solution would be the insertion of the noise only in a single point (at the input of the whole system) and the observation of several test points by the data acquisition system (through analogue routing to the AD, for example).

As noise levels are expected to be quite low in certain cases, signal conditioning will be required in the general case. So, one might need an analogue amplifier in order to observe noise levels in initial sections of the signal path. This may impact the capability of observing other test points.

On the other hand, the noise figure of the entire analog section can be determined from the proposed approach. For some BIST problems this could be enough, as the noise figure can be defined for the whole system.

7.4.1 Low cost noise generator

As previously observed, an error of 5% in hot temperature knowledge had little impact on the measured noise figure. This indicates that noise could be generated by a low cost generator, as precision requirements are somewhat relaxed.

For low frequencies a low cost generator can be built using a switch-controlled resistive-capacitive circuit that will be randomly sampled, as illustrated in Figure 7.11. This sampling process is clocked according to the output of a Linear Feedback Shift Register (LFSR). Then the output value of this circuit will change randomly. Waveforms are as shown in Figure 7.12.

In order to address the needs of higher frequency circuits, the scheme proposed in Figure 7.13 could be used. The noise is frequency-translated to the measurement band using an additional mixer. Then noise figure measurements can be carried out at the nominal frequency of the device being analyzed.

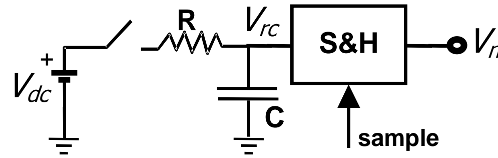


Figure 7.11: Noise generator (FLORES, 2002).

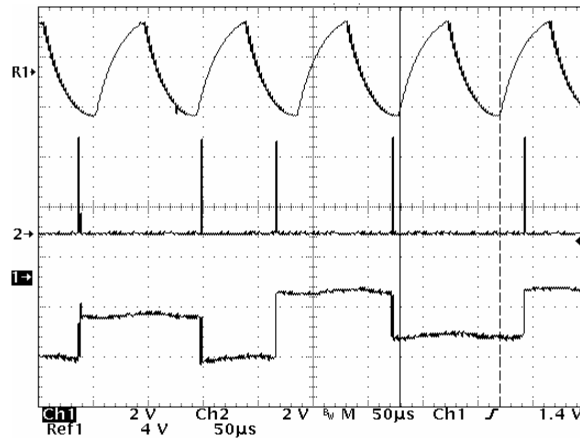


Figure 7.12: Signal generation waveforms (FLORES, 2002).

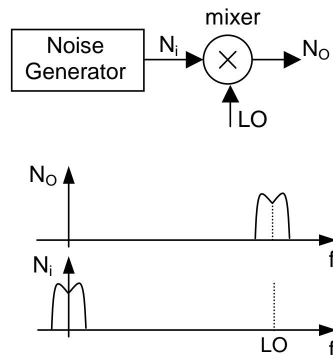


Figure 7.13: Noise frequency translation for higher frequencies (NEGREIROS, 2004-c).

7.5 Noise Figure Evaluation Using Low Cost BIST

A technique for evaluating noise figure suitable for BIST implementation is described. It is based on a low cost single-bit digitizer, which allows the simultaneous evaluation of noise figure in several test points of the analog circuit. The method is also able to benefit from SoC resources like memory and processing power.

7.5.1 Proposed method for NF measurement

Some problems are not addressed in the strategy presented in Figure 7.10: the AD converter of the system is used, so simultaneous acquisition is not possible. Also, routing of analog signals to the ADC may be difficult. There is a need for a

multiplexing device at the input of the ADC, which introduces non-linearity and distortion in the signal.

If the ADC is replaced by a simple digitizer, like in Figure 7.11, some advantages like the possibility of simultaneous observability and no need for multiplexing devices is achieved. Also, because of the simplicity of the digitizer, it can be permanently connected to the analog test point, thus avoiding switches which degrade the performance of the analog circuit under test.

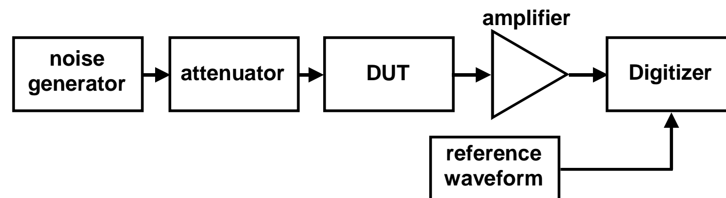


Figure 7.14: Proposed NF setup using statistical sampler (NEGREIROS, 2005-a).

As the Y-factor method requires the evaluation of a ratio of signal power, the digitizer must be able to measure noise power levels.

In this work the digitizer uses a voltage comparator and a reference signal in order to perform the data acquisition. The requirements of the reference signal are modest (in the sense that only a small frequency band is used in the calibration process), allowing a simple and low-cost signal generator to be used.

7.5.2 Evaluating power levels

In the following, a Matlab simulation illustrates the idea of measuring noise levels using a reference waveform. In a real application, noise and reference waveforms should be amplified in order to enable the use of a voltage comparator.

If one applies a constant-amplitude square wave signal to the digitizer of Figure 7.15 as a reference signal, noise levels can be determined if a simple strategy is followed.

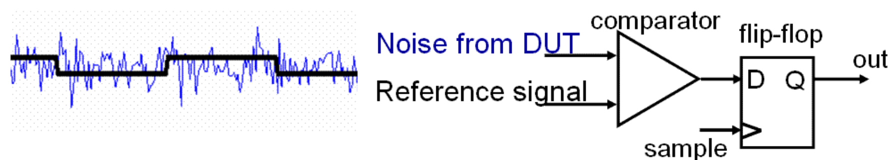


Figure 7.15: Signals for noise level measurements.

Two noise levels were applied to the digitizer using the same square wave as reference. Signals are as shown in Figure 7.16. One should notice that noise levels should be always greater than the reference levels.

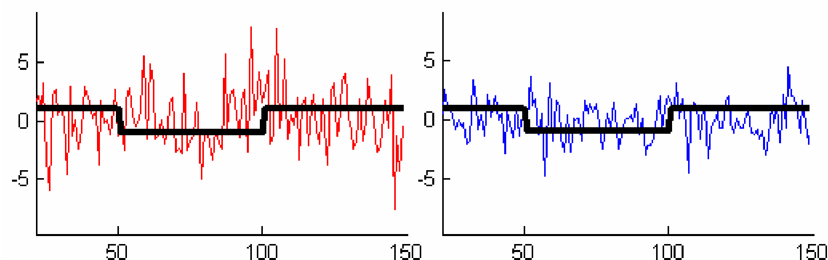


Figure 7.16: Noise and reference waveforms for hot (left) and cold (right) noise temperatures.

The power spectrum density evaluation of the bit stream at the output of the digitizer is shown in Figure 7.17. One can notice that the noise levels remain similar, while amplitude levels of the reference square wave are larger.

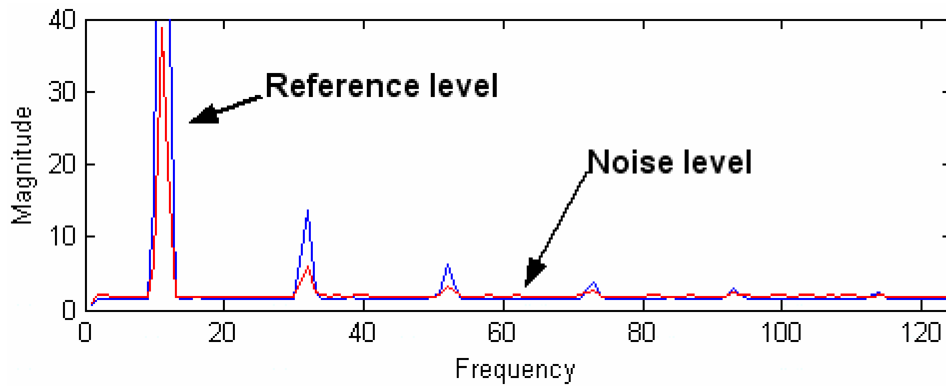


Figure 7.17: Power spectrum density (NEGREIROS, 2005-a).

As the reference level is constant, a simple normalization procedure can be used. One can evaluate the maximum amplitude of both spectra and apply a correction factor to one of the power spectral density plots.

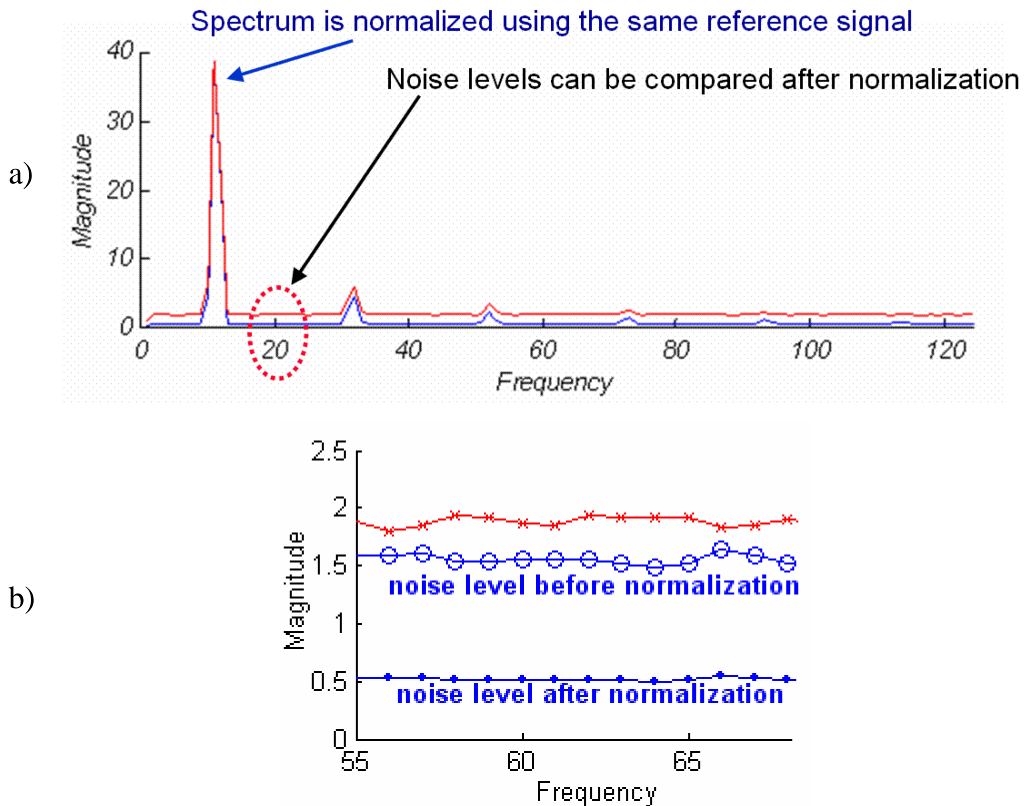


Figure 7.18: Power spectrum density after normalization a) full view and b) *zoom* at 60 Hz.

Figure 7.18 shows different noise levels, obtained before and after the normalization procedure. One can observe that the noise levels were very close before the normalization procedure. In order to make a numeric comparison, noise power ratio was evaluated using three different methods: ratio of mean square values (evaluated in time domain), ratio of PSD data and ratio of PSD data from the 1-bit digitizer. The values

obtained are presented in Table 7.5. For the 1-bit data, the reference waveform must be excluded from the power ratio evaluation (the reference is not part of the signal being measured). If this is accomplished, about 2.5% error in the power ratio was observed in the simulation, as presented by the last line in Table 7.5.

Table 7.5: Noise power ratio evaluation and derived parameters for T_h=10000K and T_c=1000K.

Method	Noise power ratio	F	NF(dB)
Mean square ratio	3.4866	10.03	10.01
PSD ratio	3.4766	10.08	10.03
1-bit PSD ratio **excluding** reference	3.5620	9.66	9.85

Source: NEGREIROS, 2005-a.

7.5.3 Noise and reference levels

Simulations were carried out in order to evaluate the accuracy of noise power ratio estimates as a function of the amplitude of the reference waveform. Figure 7.19 shows the error in power ratio estimates for gaussian noise. The reference waveform amplitude level is related to the overall accuracy of the method: for very small amplitude references, a large error is expected because of noise levels disturbing the reference amplitude. Very large references may lead to non-linear distortion of the digitizer. Amplitudes in the range of 10% to 40% of the noise level should give reasonable results.

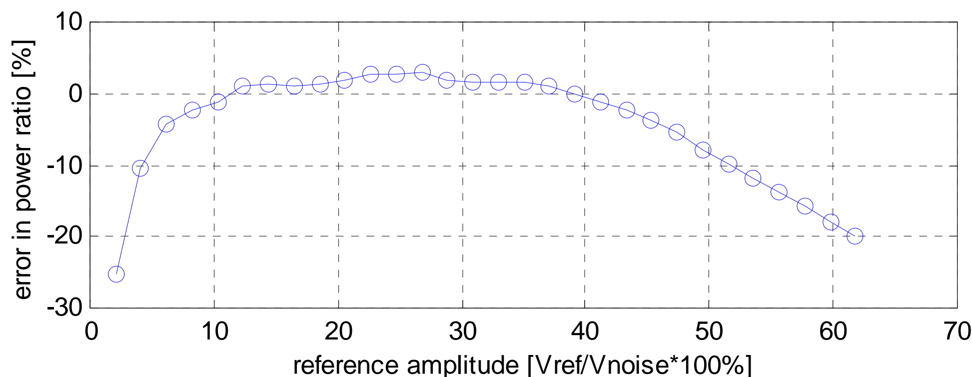


Figure 7.19: Error in power ratio estimates versus reference amplitude (NEGREIROS, 2005-a).

7.5.4 Experimental results

In order to verify the approach a test setup was implemented in order to measure the noise figure of a non-inverting amplifier. The general setup is shown in Figure 7.20. In order to change the value of the noise figure of the circuit, a different operational amplifier was used. As the equivalent noise voltages are provided by the data-sheets of the components, one is able to calculate the expected nominal value of the noise figure of the circuit, according to the opamp used (STEFFES, 1996).

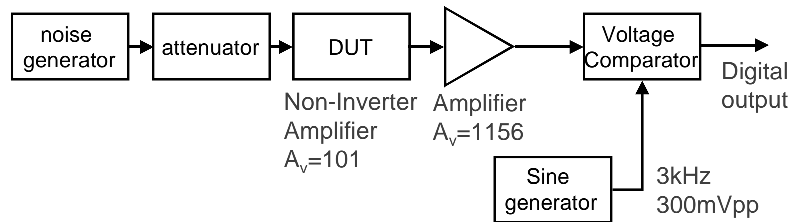


Figure 7.20: Diagram of the experimental setup (NEGREIROS, 2005-a).

The opamps used were the OP27, OP07, TL081 and CA3140. The corresponding expected noise figures where in the range of 3.7dB to 16.2dB. In order to avoid interference pickup, the circuit was assembled in an aluminum case, being battery powered, as shown in Figure 7.21.

Figure 7.21: Prototyped circuit (NEGREIROS, 2005-a).

External noise generator and sine wave generator (both HP33120A) were used. The reference waveform was at 3kHz, while the noise measurement bandwidth was at 1kHz, as indicated in Figure 7.22. The output of the digitizer was acquired using a digital scope (HP54645D). Data was processed using Matlab. Total acquisition length was 1e6 samples and the FFT size was 1e4 samples. The results obtained after processing are presented in Table 7.6, including the expected noise figure values from noise circuit analysis (STEFFES, 1996).

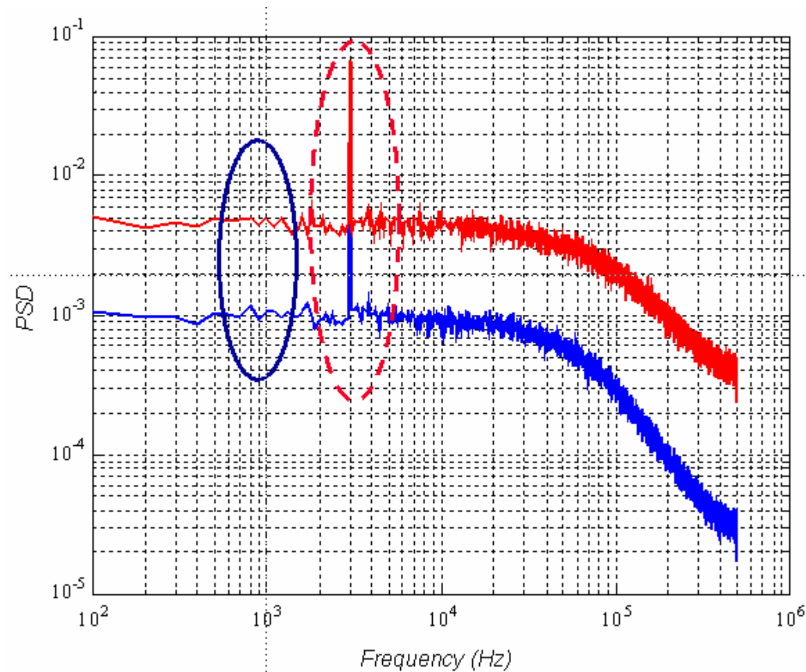


Figure 7.22: PSD plot for noise levels after normalization (NEGREIROS, 2005-a).

Table 7.6: Noise figure results for T_0=290K and T_h=2900K.

Opamp	Expected	Measured
OP27	3.7	3.69
OP07	6.5	4.841
TL081	10.1	9.698
CA3140	16.2	14.02

Source: NEGREIROS, 2005-a.

7.5.5 Analysis

The experimental results presented in the last section have indicated the feasibility of implementing the approach for practical circuits. Noise figure measurements were carried out with a 2 dB maximum absolute error.

The proposed strategy makes use of a reference signal in order to perform the normalization process. Even a low-cost generator could be used, as the normalization process would track the main frequency component (disregarding harmonics, for example). This would enable the use of low quality reference waveforms, as the harmonics are not used in the normalization process. The amplitude of the main component, however, should be constant.

The need for analog signal conditioning, as a high gain amplifier, is related to the signal levels that should be measured. In general, an amplifier will be required for noise measurements (MOTCHENBACHER, 1993). This overhead could be minimized by observing that the noise figure of a cascade of stages is mainly the noise figure of the first stage as indicated by Friis (Equation 7.6).

7.6 Conclusions

In this chapter techniques for the evaluation of noise figure in a BIST environment were discussed. As the techniques are based on DSP, they are able to benefit from resources already available in the SoC environment.

A simple voltage comparator was used as digitizer, thus discarding the need for an ADC. The technique also extends the capabilities of a simple and low cost BIST cell presented in chapter 4, allowing one to perform frequency and noise measurements.

8 FINAL REMARKS

Analog test in the SoC environment is still an open issue. The availability of processing power and digital signal processing capabilities, large amounts of available memory and programmable logic can be used in the development of test strategies targeted for BIST. However, the overhead of additional ADC and DAC converters may be too costly for most systems, even for on-line test.

In this work, a method that can enable BIST and on-line test for analog and mixed-signal cores in the SoC environment was developed. One of the main goals was to trade analog area for digital area, to benefit from technology scaling. Also, to develop a test technique mainly digital, that could benefit from SOC resources.

In order to reach these goals, a simple and low cost digitizer was used instead of an ADC. It has several unique characteristics like low analog area overhead, simplicity and low cost. Because of these characteristics, multiple analog test points can be observed, as the converter can be replicated and used in several test points.

As the digitizer is always connected to the analog test point, it is not necessary to include muxes and switches that would otherwise degrade the signal path or disturb the analog circuit in an unacceptable way. This results also in an increase in the observability of the analog signal path, enabling both on-line and BIST strategies.

The converter is able to reach higher frequencies because of its simplicity, enabling the implementation of low cost RF test strategies. As the converter is always connected to the test point, its input impedance can be taken into account in the design of the circuit, and no impedance change will occur while in test mode.

The converter also allows one to perform frequency and noise measurements, being intrinsically noise-immune, as it benefits from noise characteristics.

The test strategy is based on a statistical sampler that can be made transparent to the statistics of the input signal, although the signal itself cannot be reconstructed. A mathematical analysis of this statistical sampler has been developed. The underlying philosophy of the test method, with results for linear and non-linear analog systems was presented.

The proposed sampler also allows the use of digital testers to perform the test of analog and mixed signal circuits: as the output of the statistical sampler is a digital signal, it could be routed easily to an external digital tester.

8.1 Contributions

In this section we analyze the main contributions of this thesis. As the focus has been analog test in the SoC environment, the development of a simple and low cost digitizer was essential. The proposed digitizer enabled the development of several testing approaches that were discussed throughout this thesis. We summarize these contributions in the following.

The statistical sampler developed in chapter 4 enables the observation of the statistics of analog signals. In Table 8.1 it is classified as a new access method, along with other works. The table is taken from chapter 2.

Table 8.1: Access methods.

CLASS	METHOD	PROBLEM
Fully analog	Analog scan (WEY,1990)	needs digitizer
	Transparent blocks (VAZQUEZ, 1996; RENOVELL, 1996-b)	needs digitizer
	Mixed-signal test bus (IEEE, 2000)	needs digitizer
Digital output	Modified digital boundary scan (MILOR, 1998)	low-frequency, not flexible
	Window comparator (VENUTO, 2001-a)	low-frequency
	Periodic waveform digitizer (LOFSTROM, 1996; NOGUCHI,2005)	periodic signals
	Statistical sampler **(NEGREIROS, 2003-c)**	**only signal statistics are acquired**

In chapter 3 a test method based on frequency domain was developed. This method was successfully used with the proposed sampler, but can also be used with any ADC. As a new test method, Table 8.2 lists the technique along with other works.

Table 8.2: BIST methods.

CLASS	METHOD	PROBLEM
Vector-based	Sinusoidal input (SLAMANI, 1992; HAMIDA, 1993)	input selection
	General waveform input (HUYNH, 1998)	simulation time, input selection
	DC-level (VENUTO, 2001-a; RENOVELL, 1996-a)	dc only
	Pseudorandom (OHLETZ, 1991; MARZOCCA, 2002)	signal generation, test time
	BIST framework (HAFED, 2002)	periodic signals
	Analog random-noise (NEGREIROS, 2003-a)	**analog noise generator**
Vector-less	Oscillation-based (ARABI, 1997; HUERTAS, 2000)	may degrade circuit performance
	Supply current based (SILVA, 1996)	needs calibration, specific

The statistical sampler developed in chapter 4 has been employed in the on-line test scenario. We have classified it in Table 8.3.

Table 8.3: On-line test methods.

CLASS	METHOD	PROBLEM
Duplication	Analog replication (LUBASZEWSKI, 1995)	area overhead, specific
	Digital modeling (COTA, 2000-a; SOUZA, 2002)	area overhead, computational load
Checksum	Continuous checksums (CHATTERJEE, 1993)	specific, needs digitizer for check
Checkers	Analog checkers (LUBASZEWSKI, 2000; VELASCO-MEDINA, 1998)	specific, needs digitizer for check
Digital monitor	**PSD-based (NEGREIROS, 2003-c)**	**analog noise generator**

Besides general techniques, some research lines have received more attention, namely pseudorandom testing, RF testing and noise figure evaluation.

In the context of pseudorandom testing studied in chapter 5, this work verified the use of single bit conversion for analog testing. First, the use of a single bit noise generator was proposed (NEGREIROS, 2003-d). After that the use of 1-bit conversion was verified (NEGREIROS, 2003-b). Finally, a complete 1-bit test system was developed for pseudorandom testing (NEGREIROS, 2003-e). The technique developed in (NEGREIROS, 2003-e) presents the lowest cost in terms of digitizers for pseudorandom techniques. This line of research is presented in Table 8.4.

Table 8.4: Pseudorandom test.

METHOD	
Analog random-noise	(NEGREIROS, 2003-a)
digital noise	(NEGREIROS, 2003-d)
1-bit ADC	(NEGREIROS, 2003-b)
digital noise and 1-bit ADC	(NEGREIROS, 2003-e)

The test of high speed analog circuits has been developed in chapter 6. Subsampling, BIST and on-line techniques were addressed, as shown in Table 8.5.

Table 8.5: RF test.

METHOD	
Subsampling	(NEGREIROS, 2003-f)
BIST	(NEGREIROS, 2004-a)
On-line	(NEGREIROS, 2005-c)

In order to allow the measurement of noise with the statistical sampler, a technique for noise figure measurement was developed in chapter 7, and this work is summarized in Table 8.6.

Table 8.6: Noise figure measurement.

METHOD	
Using the statistical sampler	(NEGREIROS, 2005-a)
Using the system ADC	(NEGREIROS, 2004-c)

The work presented here has been referenced by other research groups in some publications, as indicated in Table 8.7.

Table 8.7: Citations in the literature.

CITATION	WORK
AKBAY, 2004-a	2003-b, 2002-b
AKBAY, 2004-b	2003-e
BHATTACHARYA, 2004-a	2003-b, 2004-a
BHATTACHARYA, 2004-c	2003-b, 2004-a
HONG, 2004	2003-b
HSIEH, 2005	2004-a
SANAHUJA, 2005-a	2002-b
SANAHUJA, 2005-b	2002-b
SILVA, 2005	2004-a
SU, 2004	2002-b

8.2 Future works

Although much effort has been made in this work, there are still open issues.

In the application side, the effective use of the statistical sampler in practical applications was restricted to prototyped circuits with discrete components. Its application to an integrated circuit as a BIST core would add significant improvement to

this work, mainly for practical purposes. Methods to allow fault insertion and validate the methodology in silicon should be addressed in this case.

The use of the statistical sampler has been restricted to ac coupled circuits. The use of dc-coupling could be addressed, using as starting point the strategy presented in (NOGUCHI, 2005).

For RF testing, pushing the limits of current high-speed voltage comparators is work in progress and could not be included here. Further characterization of the technique and its application to other RF blocks like frequency synthesizers and to measure other parameters like jitter could also enhance the work. The implementation of RF checkers with the statistical sampler is another possible extension to this work.

Additional theory for low frequency signals (in comparison to noise frequency) has been developed in a related work (SOUZA, 2004-a; SOUZA, 2004-b). Other cases should also be analyzed in order to effectively use the technique.

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APPENDIX TÉCNICAS DE TESTE EMBARCADO DE BAIXO CUSTO PARA CIRCUITOS ANALÓGICOS LINEARES E NÃO-LINEARES

Com a crescente demanda por produtos eletrônicos de consumo de alta complexidade, o mercado necessita de um rápido ciclo de desenvolvimento de produto com baixo custo. Uma estratégia utilizada atualmente para resolver esse problema é o projeto de equipamentos eletrônicos baseado no uso de núcleos de propriedade intelectual, ou simplesmente IPs, do inglês *IP cores* (ZORIAN; MARINISSEN, 2000). Estes núcleos são blocos funcionais previamente projetados e que podem ser adicionados a um projeto eletrônico integrado num chip. Essa metodologia de projeto proporciona flexibilidade e velocidade de desenvolvimento dos chamados sistemas num chip, ou SoCs, do inglês *system-on-chip*. Entretanto, embora o uso de núcleos facilite o projeto do sistema, o teste de SoCs é dificultado devido ao limitado acesso externo aos blocos funcionais internos.

Os custos do teste de SoCs podem alcançar um percentual significativo do valor total de produção, principalmente no caso de sistemas contendo IPs analógicos ou de sinais mistos (ROBERTS, 1997; ZORIAN; DEY; RODGERS, 2000). Esse valor se explica devido ao alto custo dos testadores de circuito integrado necessários no caso de sistemas analógicos ou de sinais mistos. Outro fator é a dificuldade de testar vários sistemas em paralelo, devido ao limitado número de ponteiras de teste analógicas no testador.

Técnicas de teste embarcado e projeto para teste (BIST e DFT) para circuitos analógicos, embora potencialmente capazes de minimizar o problema, apresentam limitações que restringem seu emprego a casos específicos. Algumas técnicas são dependentes do circuito, necessitando reconfiguração do circuito sob teste, e não são, em geral, utilizáveis em RF. No ambiente de SoCs, como recursos de processamento e memória geralmente estão disponíveis, eles poderiam ser utilizados durante o teste. No entanto, a sobrecarga de adicionar conversores AD e DA pode ser muito onerosa para a maior parte dos sistemas, e o roteamento analógico dos sinais pode não ser possível, além de poder introduzir distorções nos sinais a serem avaliados.

No capítulo 2 deste trabalho é feita uma revisão sobre diversas técnicas de teste analógico apresentadas na literatura. São apresentados métodos que buscam aumentar a observabilidade de pontos internos dos circuitos analógicos através de estratégias como registradores de deslocamento analógico e blocos analógicos transparentes. Também são mostradas técnicas que possuem uma interface digital de saída, como a implementação de comparadores de janela com portas lógicas e o uso de um

comparador analógico como conversor analógico-digital para sinais analógicos periódicos.

Métodos para teste embarcado (BIST) também são apresentados. Algumas técnicas que utilizam um gerador de sinais embarcado, e podem ser classificadas de acordo com o tipo de sinal gerado (senóide, rampa, e outros). Em geral, o custo de integração de geradores de alta qualidade é alto, sendo uma desvantagem desses métodos. Uma outra abordagem mostrada é o uso da técnica de oscilação, que dispensa o uso de um gerador de sinais. Entretanto, essa técnica possui aplicação limitada a filtros. Também são apresentadas técnicas para teste de circuito analógico sob funcionamento (*on-line*), já que estratégias de teste em geral não requerem que o circuito esteja em operação normal.

Com a evolução da tecnologia de fabricação de circuitos integrados, nota-se o aumento da capacidade de integração de lógica digital. No entanto, a implementação de circuitos analógicos sob tecnologia digital apresenta diversas dificuldades que tornam difícil à tecnologia analógica seguir a mesma tendência de integração que os circuitos digitais (WALDEN 1999). Por essa razão, para que um sistema possa aproveitar ao máximo a diminuição de área total do circuito proveniente das novas tecnologias, é interessante minimizar o uso de área analógica, mesmo que isso signifique aumentar a área do circuito digital.

Considerando-se a necessidade de acréscimo de estruturas de teste para circuitos analógicos e mistos, é desejável que esse acréscimo seja apenas de área digital, ou que apenas o mínimo possível de área analógica seja acrescentada. Desse modo, o custo adicional da área devido às estruturas de teste seguirá a tendência de circuitos digitais, sendo capaz de se beneficiar com as novas tecnologias de integração. Além desse fator, a inclusão de circuitos analógicos adicionais implica também em métodos e estruturas adicionais para o teste desses circuitos.

O ambiente de SoCs pode prover recursos para a implementação de estratégias de teste a um custo mínimo, uma vez que esses recursos já estão incluídos no sistema. Para o caso de circuitos analógicos e mistos, seria necessária a inclusão de digitalizadores para implementação dos métodos de teste. No entanto, mesmo para o caso de SoCs a inclusão de diversos conversores analógico-digitais (AD) e digital-analógicos seria onerosa demais. Desse modo, existe uma necessidade de desenvolvimento de conversores de baixo custo com mínimo acréscimo de área analógica para possibilitar a implementação de estratégias de teste analógico nesses sistemas.

Essa motivação leva ao desenvolvimento, no capítulo 3, de um método de teste analógico capaz de reaproveitar os recursos já disponíveis em SoCs, como memória e processadores. A técnica proposta é baseada na aplicação de ruído para a caracterização do circuito analógico sendo testado, sendo que o uso de ruído possibilita a implementação de um gerador com menor custo (FLORES, 2002). O método utiliza como assinatura a densidade espectral de potência (PSD) do sinal de saída do circuito analógico sob teste. São apresentados diversos resultados de simulação e envolvendo a injeção de falhas em circuitos analógicos prototipados com componentes discretos, onde se verificou a capacidade de detecção das falhas injetadas através do método proposto.

Esse capítulo também apresenta resultados do uso de conversores analógico-digitais de baixa resolução para o teste de circuitos analógicos, onde se conclui que para dadas especificações de teste e relação sinal-ruído existe uma escolha ótima da resolução de

um conversor AD, relacionada a trocas entre custo (resolução) do conversor e tempo e sensibilidade do teste.

O capítulo 4 apresenta um novo digitalizador, chamado amostrador estatístico (*statistical sampler*), que utiliza um comparador possuindo ruído como sinal de referência. Embora esse digitalizador não seja capaz de reproduzir o sinal analógico de sua entrada (salvo sob condições especiais), ele é capaz de adquirir as estatísticas do sinal de entrada (em especial, a autocorrelação). Como a densidade espectral de potência (PSD) é a transformada de Fourier da autocorrelação, este conversor pode ser usado para a implementação prática do método de teste proposto no capítulo 3.

Diversos resultados práticos foram obtidos para a implementação de teste on-line de filtros utilizando o amostrador estatístico e o método de teste baseado em PSD. A técnica propõe a estimação on-line da função de transferência do circuito sob teste, através da razão entre a PSD na saída do circuito pela PSD da sua entrada. A estimativa assim obtida é comparada com a função de transferência de referência previamente obtida e armazenada. Como todo o processamento é feito digitalmente, essa técnica é perfeitamente adequada ao uso em SoCs, já que permite o reuso de processadores e memórias já existentes.

A utilização do amostrador estatístico no contexto de teste com sinais pseudo-aleatórios (ruído) é aprofundado no capítulo 5. Uma vantagem desse contexto é o uso de uma referência fixa, ao invés de ruído (uma vez que o próprio sinal de entrada já é ruído), dispensando um gerador de ruído analógico adicional para os amostradores. A maior vantagem dessa abordagem é possibilitar a estrutura de teste mais barata possível, contendo conversores DA e AD de apenas 1 bit. O impacto do processamento de 1-bit na implementação de métodos de teste baseado na PSD é avaliado para o conversor DA e depois para o conversor AD. Finalmente, um exemplo de teste demonstrando o uso de conversores AD e DA de 1-bit é apresentado.

Com a disseminação de dispositivos eletrônicos portáteis atualmente, o uso de transceptores para comunicações sem fio é comum em SoCs. Estes transceptores em geral fazem uso de circuitos analógicos que trabalham em freqüências elevadas, na ordem de centenas de megahertz ou mesmo alguns gigahertz. O teste dessas interfaces apresenta dificuldades adicionais em relação aos circuitos analógicos convencionais, principalmente porque os circuitos de teste devem operar nas mesmas freqüências elevadas.

Técnicas para o teste dessa classe de circuitos são discutidos no capítulo 6. Uma abordagem usando a técnica de sub-amostragem com conversores AD de alta freqüência é apresentada. No entanto, devido ao elevado custo desses conversores, o emprego dessa técnica é deixado a casos específicos.

A aplicação do amostrador estatístico do capítulo 4 ao teste de circuitos de RF é apresentada, incluindo o caso de teste sob operação normal do circuito (*on-line*). São apresentados diversos resultados sinais analógicos na faixa de uma centena de megahertz. Os resultados demonstram a capacidade do amostrador em realizar aquisições de sinais de alta freqüência e possibilitar o teste dessas interfaces. O emprego do amostrador para o teste de circuitos analógicos não lineares também é exemplificado.

Neste capítulo também se discute a sobrecarga do método de teste, no contexto de uma aplicação baseada em DSP para medição de potência. É feita uma análise da

sobrecarga e impacto do teste sobre o processador e memória, bem como são avaliados fatores como tempo de resposta do teste na sobrecarga do sistema.

No capítulo 7 é apresentada uma metodologia para o uso do amostrador estatístico na medição de níveis de ruído, empregada na medição de Figura de Ruído. Este é um parâmetro importante na caracterização de sistemas analógicos de baixo ruído e de sistemas de comunicação. Nesse capítulo discutem-se métodos que poderiam ser utilizados para a medição embarcada da figura de ruído. É também proposto um método de medição de figura de ruído usando o amostrador estatístico e um gerador de ruído analógico. São apresentados resultados práticos obtidos com diversos amplificadores operacionais discretos demonstrando a capacidade do método.

O método proposto é capaz de melhorar a testabilidade de projetos que utilizam circuitos de sinais mistos, sendo adequado ao uso no ambiente de SoCs usado em muitos produtos atualmente.

Como principais contribuições desse trabalho, pode-se citar:

- o desenvolvimento de um método de acesso a circuitos analógicos com saída digital, onde apenas a estatística do sinal é adquirida, com mínima área analógica e capacidade de atingir freqüências elevadas (na faixa de centenas de megahertz ou mais);
- um método de teste de circuitos analógicos baseado em PSD, que pode ser aplicado para teste embarcado (BIST) e para teste sob-operação normal do circuito ("on-line");
- uma célula de teste (amostrador estatístico) que pode ser empregada na automação de estratégias de teste analógico;

Embora muito esforço tenha sido dispendido no desenvolvimento desse trabalho, alguns pontos ainda precisam de desenvolvimento futuro:

- a aplicação do amostrador estatístico em circuitos integrados, ao invés de circuitos prototipados em bancada (nesse caso, métodos para inserção de falhas e validação devem também ser desenvolvidos);
- utilização do amostrador estatístico em transceptores operando em gigahertz;
- aplicação do amostrador estatístico para o teste de circuitos específicos em RF, bem com a avaliação de *jitter*;
- aspectos teóricos adicionais são apresentados por outro trabalho desenvolvido pelo grupo (SOUZA, 2004-a; SOUZA, 2004-b). Para o caso de teste em RF com ruído de banda limitada inferior ao sinal de interesse, ainda é necessário mais desenvolvimento teórico.