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FULLY NON-VOLATILE FULL ADDER DESIGN USING MEMRISTORS

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Graduation Project presented to Department of Electrical Engineering of Federal University of Rio Grande do Sul in partial fulfillment of the requirements for the degree of Electrical Engineer.

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This Project was considered adequate for obtaining the credits of the course Projeto de Diplomação of Department of Electrical Engineering and and approved in its final form by the Advisors and the Examination Committee.

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ABSTRACT

Given the increasingly challenging technical obstacles posed by the approaching limits of CMOS technology scaling, emerging devices have been considered as an alternative to break this paradigm. The memristor has garnered significant attention from the scientific community in recent years as a potential device to play a leading role in the next generation of integrated circuits. In this context, this work presents the design of a fully non-volatile memristive full adder. The designed circuit features a hybrid CMOS/memristor architecture, using CMOS transistors from the XFAB 180 nm technology and the JART VCM v1b memristor model. The proposed topology employs a majority voter as a non-volatile core, along with a magnitude comparator circuit, a multiplexer, and a non-volatile latch. By simulating the proposed circuit through the Virtuoso tool, it was confirmed that the circuit operates as expected, with input data stored in a non-volatile manner as resistances in memristors, even in the absence of a power supply. Also, through simulation, the circuit delay was found to be $132\mu s$.

Keywords: Memristor, full adder, non-volatile, CMOS.

RESUMO

Diante dos desafios técnicos cada vez mais difíceis impostos pela aproximação dos limites de exploração do escalonamento da tecnologia CMOS, os dispositivos emergentes têm sido considerados como uma alternativa para quebrar este paradigma. O memristor tem atraído a atenção da comunidade científica nos últimos anos como um potencial dispositivo para desempenhar um papel de liderança na próxima geração de circuitos integrados. Nesse contexto, este trabalho apresenta o projeto de um somador completo memresistivo inteiramente não volátil. O circuito projetado possui arquitetura híbrida CMOS/memristor, usando transistores CMOS de tecnologia XFAB de 180 nm e o modelo de memristor JART VCM v1b. A topologia proposta utiliza um votador majoritário como um núcleo não volátil, além de um circuito comparador de magnitude, um multiplexador e um latch não-volátil. Simulando o circuito proposto, através da ferramenta Virtuoso, foi possível verificar que o mesmo funciona conforme o esperado já que os dados de entrada são armazenados de forma não volátil como resistências em memristores, mesmo na ausência da fonte de alimentação. Também por meio de simulação, o *delay* obtido para o circuito foi de $132\mu s$.

Palavras-chave: memristor, somador completo, não-volátil, CMOS.

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LIST OF ABBREVIATIONS

AE	Active Electrode
ALU	Arithmetic and Logic Unit
CMOS	Complementary Metal-Oxide Semiconductor
HRS	High Resistive State
LRS	Low Resistive State
MIM	Metal-Insulator-Metal
MO	Metal Oxide
MOSFET	Metal-Oxide Semiconductor Field-Effect Transistor
MTJ	Magnetic Tunnel Junction
MUX	Multiplexer
NMOS	N-channel Metal-oxide Semiconductor
OE	Ohmic Electrode
PCSA	Pre-Charge Sense Amplifier
PDN	Pull-Down Network
PMOS	P-channel Metal-Oxide-Semiconductor
PUN	Pull-Up Network
PWL	Piecewise Linear
SOC	System On Chip
STT	Spin Transfer Torque
TG	Transmission Gate
VCM	Valence Change Mechanism

CONTENTS

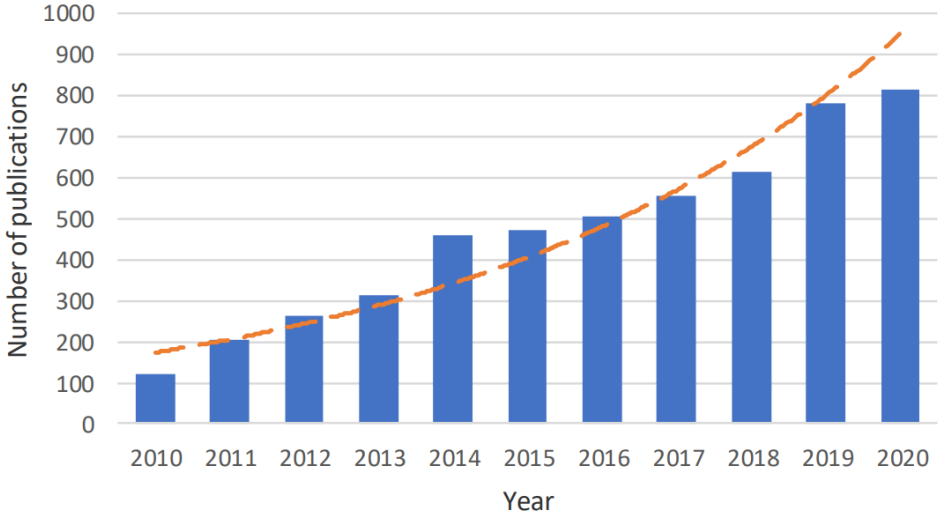
1 INTRODUCTION

Much of the progress in electronics is due to the miniaturization of CMOS technology. This technology scaling enables performance improvements, increased transistor density, and reduced power consumption (BORKAR, 1999). However, this miniaturization is reaching its limits, with contributing factors including the minimum possible manufacturing dimensions, reduced switching performance/efficiency, and current leakage or static power consumption (DANIEL, 2005).

In this context, memristors can serve as an alternative for advancing electronics. A memristor is a nanoscale, two-terminal passive device capable of changing its resistance based on the voltage across its terminals. This property enables memristors to store logical levels '0' and '1' through their maximum and minimum resistance limits (STRUKOV et al., 2008). These devices are non-volatile, exhibit low power consumption (ISAH; BILBAULT, 2022), are compatible with CMOS technology, and offer good scalability (ALI et al., 2021). While commonly used as memory devices, memristors can also be implemented in logic circuits (ROSE et al., 2012). Memristor-based logic circuits pave new avenues for exploring computational architectures, presenting promising alternatives to conventional integrated circuit technologies (VOURKAS; SIRAKOULIS, 2016).

Due to all these characteristics, memristors have become popular and widely researched worldwide. Their popularity can be observed in the number of papers published between 2010 and 2020, as shown in Figure 1

Figure 1: Number of publications on memristor technology from 2010 to 2020.



Source: (VLASOV et al., 2020).

The integration of memristive nano-devices with traditional CMOS technology proves to be a powerful and realistic approach for the post-CMOS era (PI et al., 2014). This hybrid method combines the maturity of CMOS with the unique functionalities of memristors, offering enhanced circuit performance without relentless CMOS scaling and expanding possibilities in this field. Thus, to explore this hybrid CMOS/memristor architecture, this work aims to investigate the application of memristors in logic circuits by designing and simulating a fully non-volatile full adder.

In digital circuits, adders are among the most commonly used components, playing a crucial role in arithmetic and logic units (ALUs) within microprocessors and microcontrollers. They are responsible for performing various arithmetic and logical operations, such as addition and multiplication. The performance of these adders directly influences the overall performance of the ALU, as well as the microprocessors, microcontrollers, and the applications dependent on them.

Non-volatility is an important feature for full adders, where data or intermediate states must be preserved even in the absence of power. In memory and non-volatile computing, non-volatile full adders can be used in memory technologies like MRAM, ReRAM, or FeRAM, allowing arithmetic operations to be performed directly within memory without losing data during power interruptions. In low-power systems, such as IoT devices or solar-powered sensors, non-volatility ensures that intermediate states are retained during energy interruptions. In high-reliability computing, like aerospace, medical, or industrial systems, non-volatility guarantees that arithmetic or logical operations are not lost during unexpected power failures.

Additionally, in data persistence systems, computational states must be preserved for fault recovery or historical data analysis. In neuromorphic computing, non-volatile adders play a role in hardware inspired by biological neural systems, where state persistence without continuous energy consumption is critical. Non-volatility in full adders is essential for ensuring state retention, energy efficiency, and fault resilience, making it a crucial factor for system performance and reliability in various applications.

Nowadays, there is a growing demand for digital circuit designs that prioritize low power consumption, high speed, cost efficiency, and minimal area usage. CMOS adders are the conventional architecture used, and various optimizations have already been implemented on these circuits (MANJUNATH et al., 2015). Therefore, the proposed solution aims to explore a new full adder architecture that incorporates memristors, bringing the non-volatility characteristic to the circuit, in addition to other contributions.

To compose the full adder, transistors from the XFAB 180 nm technology and the JART VCM v1b memristor model with its standard parameters will be used. To test and validate the circuit, transient simulations will be carried out using the Virtuoso tool. All analyses will be based on the simulations performed. This work does not encompass any type of physical implementation.

This work begins with a literature review on the concepts necessary to understand the implemented solution, in Chapter 2. Chapter 3 discusses the latch and majority voter circuits originating from previous works, which will serve as the foundation for the developed circuit. Chapter 4 presents the implemented solution of the fully non-volatile full adder, including the memristor model used and characterizing the chosen transistor technology. In this chapter, the proposed circuit is described, along with its logical sequence of operation and circuit sizing. Chapter 5 presents the results obtained, including the identified limitations and suggested improvements, while Chapter 6 provides the final considerations and conclusion of the work.

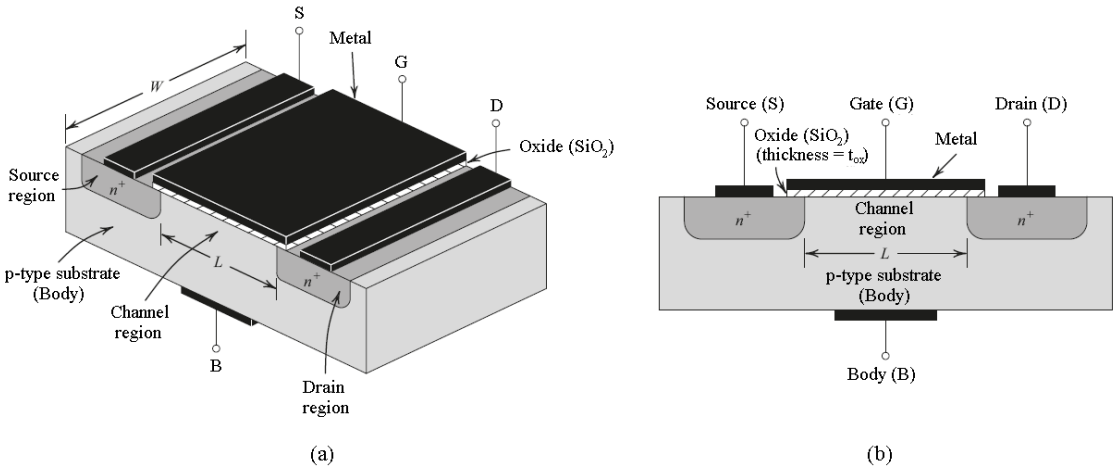
2 THEORETICAL FRAMEWORK

In this chapter, the fundamental concepts necessary for understanding this work will be presented. The first section will discuss the MOSFET transistor, one of the key components of the proposed solution. Next, the CMOS technology, which utilizes these transistors to compose various logic circuits, will be addressed, and the circuits used in this technology will be characterized. The following section will introduce the primary device used in the solution: the memristor. Finally, the MTJ device, which is used in the reference circuits of this project, will be discussed.

2.1 MOSFET

In this work, the enhancement mode metal-oxide-semiconductor field-effect-transistor (MOSFET) will be addressed. The n-channel enhancement mode MOSFET physical structure can be seen in Figure 2(a). This transistor is embedded in a p-type substrate, also known as the body (B). In the substrate are diffused two heavily doped n-type regions, named as source (S) and drain (D), as indicated in the figure. On the surface of the substrate, a thin layer of silicon dioxide (SiO_2) with thickness tox is grown, covering the area between the source and drain regions. On top of the oxide layer, a metal is deposited to form the gate electrode of the device, known as the gate terminal. Also, metal contacts are made to the source, drain and body regions.

Figure 2: N-channel enhancement mode MOSFET physical structure: (a) perspective view and (b) cross section.



Source: Adapted, (SEDRA et al., 2023).

Therefore, the MOSFET transistor has four terminals: gate - G; drain - D; source - S; and body - B. As can be easily seen in Figure 2(b), the MOSFET is a symmetrical device, which means that the source and drain can swapped without changing this transistor characteristics. Furthermore, its possible to observe that the gate terminal is electrically isolated from the body terminal, by the oxide layer. Because of this electrical isolation, the gate terminal current is extremely small, on the order of 10^{-15}A (SEDRA et al., 2023).

Another observation is that the body forms a pn junction with the source and the drain regions, and in normal operation, these pn junctions are kept inversely polarized. Assuming that the drain will have a positive voltage relative to the source,the pn junctions can be put on cut-off state by connecting the body and source terminals. Therefore, the substrate will be considered to have no effect on the device operation. For the MOSFET operation, a voltage will be applied to the gate terminal, controlling the current flow between the source and drain. This current will flow in the longitudinal direction from D to S, in the region with length L and width W, known as "channel region". This way, L and W are two important parameters for the characterization of the MOSFET transistor.

When there is no bias voltage applied to the gate terminal, there are two face-to-face diodes in series between the drain and the source. These diodes prevent the current flow from the drain to the source when a voltage v_{DS} is applied.

To create a channel that enables current flow, a voltage must be applied between the source and gate terminals. Considering that the source and drain terminals are grounded, a positive voltage, denoted as v_{GS}, is applied to the gate. This positive voltage at the gate terminal repels the positively charged free holes in the substrate region directly beneath the gate, referred to as the channel region. As a result, these holes are pushed deeper into the substrate, leaving behind a region depleted of charge carriers. This depletion region is filled with covalent bonds of negative charges associated with the acceptor atoms. These charges become exposed due to the holes that were pushed into the substrate.

In addition, the positive voltage at the gate terminal attracts electrons from the source and drain n_+ regions to the channel region. When a sufficient number of electrons accumulate near the substrate surface below the Gate, an n-type region forms, connecting the Source and Drain areas. The n-type induced region serves as a conductive pathway, allowing current to flow when a voltage is applied between the drain and source terminals. This region is denoted as channel region because it forms a channel for the current to flow form de drain to the source. In an NMOS transistor, the channel is n-type and is formed within a p-type substrate, while in a PMOS transistor, the channel is p-type and is formed within an $n - type$ substrate.

The threshold voltage (V_T) is the value of v_{GS} needed for a sufficient number of electrons to accumulate in the channel region to form a conduction channel in a field-effect transistor (FET). For an n-channel FET, V_T is positive and for a p-channel FET, this value is negative.

The MOSFET forms a parallel-plate capacitor, with the oxide layer acting as the dielectric. The positive voltage on the gate accumulates positive charges on the top plate of the capacitor, while the corresponding negative charge is made up of electrons in the channel. This vertical electric field controls the number of charges in the channel, determining its conductivity and the current flowing through it when a v_{DS} voltage is applied. The effective voltage or overdrive voltage, the difference between v_{GS} and V_T, is represented as v_{OV}, as shown in Equation 1 and is responsible for the charge in the channel.

$$v_{OV} = v_{GS} - V_T \tag{1}$$

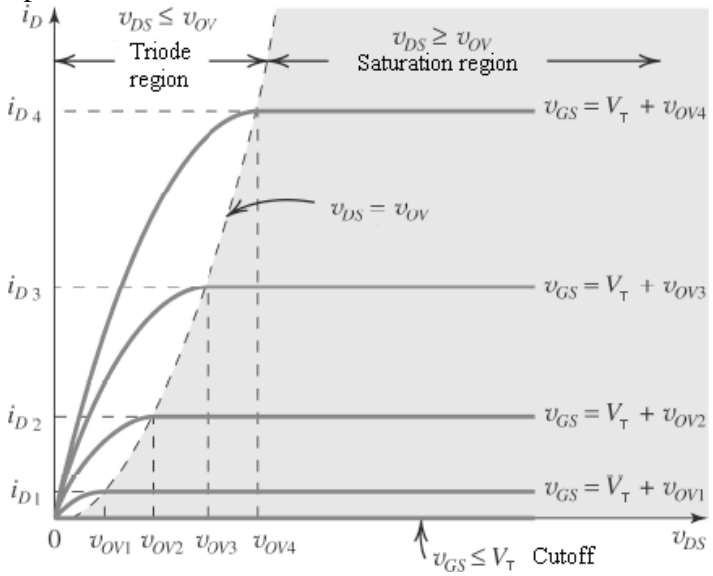
After a channel is induced, a positive voltage v_{DS} is applied between the drain and the source. This voltage causes the current i_D to flow through the induced n-channel. The current is carried by free electrons moving from the Source to the drain (hence the names "source" and "drain"). By convention, the direction of the current flow is opposite to that of the flow of negative charges. Therefore, the current in the channel, i_D, always flows from the drain to the source.

When v_{DS} is increased, while keeping v_{GS} constant and greater than V_T, the MOSFET operates with an overdrive voltage v_{OV}. As v_{DS} is applied, it causes a voltage drop along the channel, increasing from zero at the source to v_{DS} at the drain. The voltage between the gate and points along the channel decreases, resulting in a non-uniform channel depth: it is deeper at the source end (proportional to v_{OV}) and shallower at the drain end (proportional to $v_{OV} - v_{DS}$). As v_{DS} increases, the channel becomes narrower and its resistance correspondingly increases.

When v_{DS} is increased beyond v_{OV}, it no longer affects the shape or charge of the channel. The current flowing through the channel remains constant, reaching the value that corresponds to $v_{OV} = v_{DS}$. At this point, the drain current is said to saturate, and the MOSFET enters the saturation region, or the saturation mode of operation. The voltage at which saturation occurs is referred to as $v_{DS_{sat}}$.

The $i_D - v_{DS}$ curve of an NMOS transistor can be obtained by setting the v_{GS} to a constant desired value, varying v_{DS}, and measuring the corresponding i_D current. Figure 3 shows a set of $i_D - v_{DS}$ curves, where each graph is obtained by setting v_{GS} above v_T by a specific value of overdrive voltage, indicated as v_{OV_1}, v_{OV_2}, v_{OV_3}, and v_{OV_4}. These values of v_{OV} determine the saturation point of the corresponding graph, and the resulting saturation current value is directly determined by the value of v_{OV}. In this type of characteristic curve, it is possible to observe the three operation regions of the transistor.

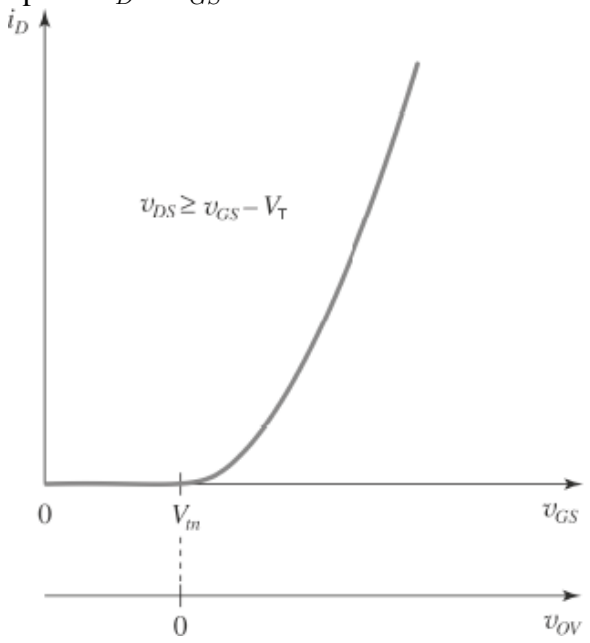
Figure 3: Examples of $i_D - v_{DS}$ characteristic curves of a NMOS transistor.



Source: Adapted, (SEDRA et al., 2023).

The $i_D - v_{GS}$ curve shows the behavior of the transistor in saturation. In this case, the drain current is a constant determined by v_{GS} (or v_{OV}) and is independent of v_{DS}. This means that the MOSFET operates as a constant current source, with the value determined by v_{GS}. An example of this characteristic curve is shown in Figure 4.

Figure 4: Example of $i_D - v_{GS}$ characteristic curve of a NMOS transistor.



Source: Adapted, (SEDRA et al., 2023).

The structure of PMOS transistors resembles that of NMOS devices, with the key difference being that the substrate for PMOS is of type n, and the source and drain regions are p+. This results in an inversion of the polarity of all semiconductor regions compared to those in the NMOS counterpart. PMOS and NMOS transistors are considered complementary devices. The operating principle of a p-channel MOSFET is analogous to that of the NMOS device, with the primary distinction being the inversion of all voltages.

In silicon, electron mobility (in NMOS transistors) is significantly higher than hole mobility (in PMOS transistors), typically by a factor of 2 to 3. This allows NMOS transistors to conduct more current under the same conditions of channel size and applied voltage. To ensure balanced operation in CMOS circuits, such as inverters, the width (W) of PMOS transistors is increased. By enlarging the PMOS width, it compensates for the reduced hole mobility, enabling it to drive a current comparable to that of the NMOS transistor. This adjustment is crucial for achieving uniform rise and fall times in signals, ensuring that the circuit performs efficiently with balanced propagation delays, enhanced speed, and reduced power waste (RABAEY; ANANTHA; BORIVOJE, 2003).

2.2 CMOS Technology

The complementary metal-oxide-semiconductor (CMOS) is a type of metal-oxide-semiconductor field-effect transistor (MOSFET) fabrication process that uses complementary and symmetrical pairs of p-type and n-type transistors to design logic circuits. CMOS digital circuits use NMOS and PMOS transistors operating as switches. A MOS transistor functions as an on/off switch by utilizing the gate voltage to operate the transistor in the triode region ("on" position) or in the cutoff region ("off" position). In this work, this technology will be applied in the design of parts of the proposed non-volatile full adder circuit.

An NMOS transistor behaves like a closed switch, exhibiting a very small resistance (r_{DS}) between its drain and source terminals when its gate voltage is high, typically at the

supply voltage V_{DD}, representing a logic '1'. Conversely, when the gate voltage is low, i.e., close to or equal to the ground voltage, representing a logic '0', the transistor is cut off, conducting no current and acting like an open switch. The PMOS transistor operates in a complementary manner: for the transistor to conduct, its gate voltage must be low, close to or equal to the ground voltage (logic level '0'). Raising the gate voltage to V_{DD} (logic level '1') turns off the PMOS transistor.

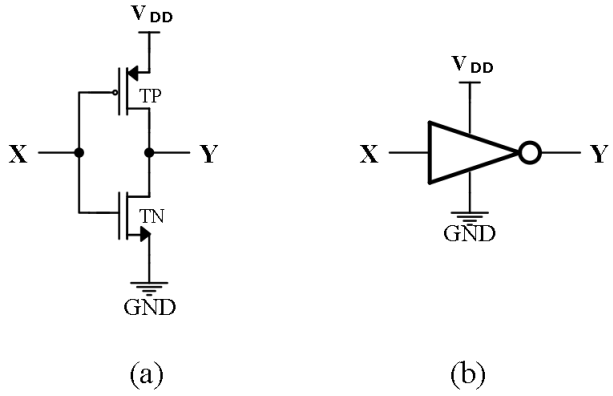
2.2.1 CMOS Inverter

The logic inverter inverts the logical value of its input signal. Thus, for a logical input of '0', the output will be a logical level of '1', and vice versa. The logical function of the inverter is represented by the Boolean expression shown in Equation 2.

$$Y = \overline{X} \tag{2}$$

The implementation of a CMOS inverter can be visualized in Figure 5(a), and its block diagram symbol in Figure 5(b). It consists of an NMOS transistor TN and a PMOS transistor TP, with the gate terminals connected to form the input terminal of the inverter, to which a logical input X is applied. Additionally, the drain terminals are connected to form the output terminal of the inverter, where the output logical variable Y appears.

Figure 5: CMOS inverter (a) implementation and its (b) block representation.



Source: Author, 2024.

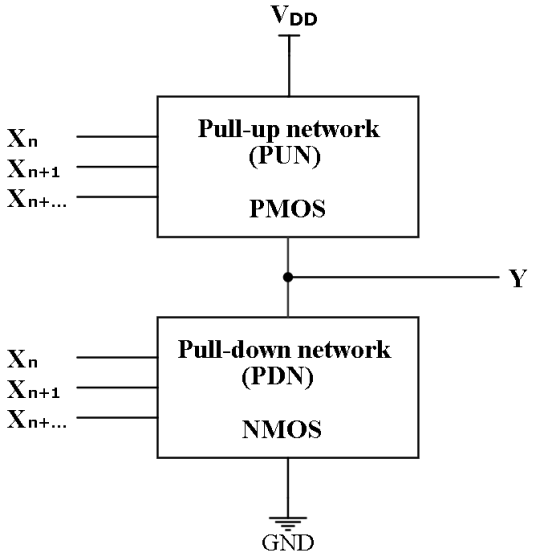
When $X = 1$ – that is, $V_X = V_{DD}$ – the PMOS transistor TP will be off, while the NMOS transistor TN will be on and will connect the output terminal of the inverter to ground through the small resistance of r_{DS}. Thus, the output voltage will be zero and $Y = 0$. When $X = 0$, i.e., $V_X = 0$, the NMOS transistor will be off, while the PMOS transistor will be on and will connect the output terminal to V_{DD} through the small resistance of r_{DS}. Thus, the output voltage will be equal to V_{DD} and Y will be '1'.

2.2.2 Static CMOS Logic Gates

The gate terminal of the MOSFET serves as the control node and is therefore typically one of the input terminals of the CMOS logic circuit. The CMOS logic circuit consists of two networks: the pull-down network (PDN), implemented with NMOS transistors, and the pull-up network (PUN), implemented with PMOS transistors, as shown in Figure 6.

Since the PDN is composed of NMOS transistors, and an NMOS transistor conducts when the signal at its gate is high, the PDN is activated—i.e., it conducts—when the

Figure 6: CMOS circuit representation, with its pull-down network (PDN) and pull-up network (PUN).



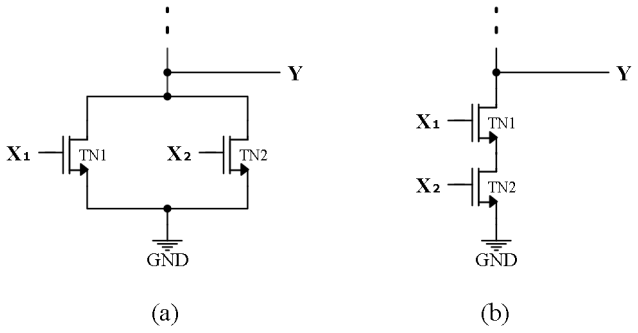
Source: Author, 2024.

inputs are high. Conversely, the PUN is composed of PMOS transistors, and a PMOS transistor conducts when the input signal at its gate is low. Therefore, the PUN conducts when the inputs are low.

The PDN uses parallel devices to form an OR function and series devices to form an AND function, and the same applies to the PUN. Here, the OR and AND notations refer to the flow or conduction of current. Figure 7 shows examples of PDNs. For the circuit in Figure 7(a), for instance, TN1 will conduct when X_1 is high ($V_{X_1} = V_{DD}$) and will then pull the output node to ground ($V_Y = 0, \text{V}$, $Y = 0$). Similarly, TN2 will conduct and pull Y down when X_2 is high. Thus, Y will be low when X_1 is high or $X2$ is high, as expressed in Equation 3.

$$Y = \overline{X_1 + X_2} \tag{3}$$

Figure 7: Examples of CMOS pull-down networks.



Source: Author, 2024.

The PDN in Figure 7(b) conduct only when X_1 and X_2 are both high simultaneously. Therefore, Y will be low when X_1 is high and X_2 is high, as expressed in Equation 4.

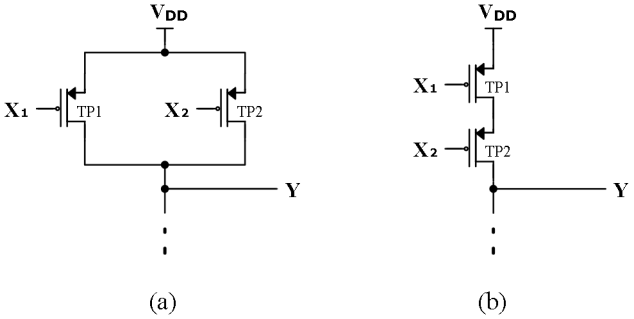
$$Y = \overline{X_1 X_2} \tag{4}$$

The PUN shown in Figure 8(a) will conduct and pull Y up to V_{DD} ($Y = 1$) when X_1 is low or X_2 is low, as per Equation 5. In contrast, the PUN in Figure 8(b) will conduct and produce a high output ($V_Y = V_{DD}$, $Y = 1$) only when X_1 and X_2 are both low, as per Equation 6.

$$Y = \overline{X_1} + \overline{X_2} \tag{5}$$

$$Y = \overline{X_1}\,\overline{X_2} \tag{6}$$

Figure 8: Examples of CMOS pull-up networks.



Source: Author, 2024.

With an understanding of the structure and operation of PUNs and PDNs, it is possible to construct various CMOS circuits, such as logic gates. Logic gates are basic digital devices that implement Boolean functions, which take one or more binary inputs and produce a single binary output (HARRIS; HARRIS, 2016). They serve as fundamental building blocks for countless digital circuits. Each logic gate has a unique symbol, typically drawn with inputs on the left and the output on the right. The relationship between a gate's inputs and its output can be expressed using a Boolean equation or a truth table.

2.2.2.1 NOR and OR Logic Gates

A two-input NOR gate implements the Boolean function described in Equation 7 and represented in Table 1.

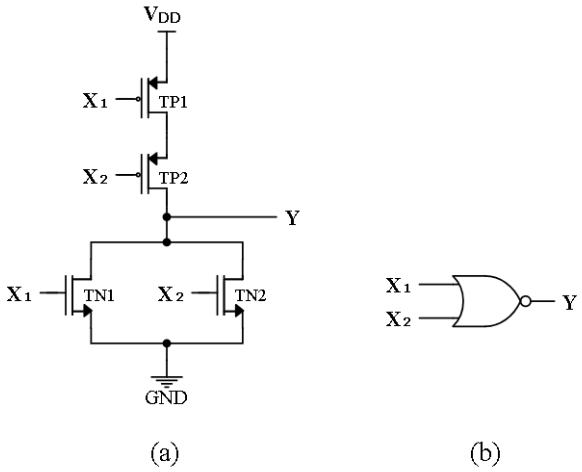
$$Y = \overline{X_1 + X2} \tag{7}$$

Table 1: NOR truth table.

X_1	X_2	Y
0	0	1
0	1	0
1	0	0
1	1	0

For the CMOS NOR gate implementation, it is possible to notice, through Table 1, that the output Y must be at logical '0' when the inputs X_1 or X_2 are at logical '1'. Thus, the PDN will be composed of two NMOS transistors in parallel, as discussed before. Using the same principles, Y will be at logical '1' only when both inputs are at logical '0', so the PUN must be composed of two PMOS transistors in series. This implementation is shown in Figure 9(a), and the NOR gate symbol is shown in Figure 9(b). To increase the number of inputs of the gate, for any new input, an NMOS transistor is added in parallel with the others on the PDN, and a PMOS transistor is added in series with the others on the PUN.

Figure 9: CMOS NOR (a) implementation and its (b) symbol.



Source: Author, 2024.

To implement a CMOS OR gate, an inverter is connected to the NOR gate output, as shown in Figure 10. The OR Boolean function is presented in Equation 8 and represented in Table 2.

$$Y = X_1 + X2 \tag{8}$$

Table 2: OR truth table.

X_1	X_2	Y
0	0	0
0	1	1
1	0	1
1	1	1

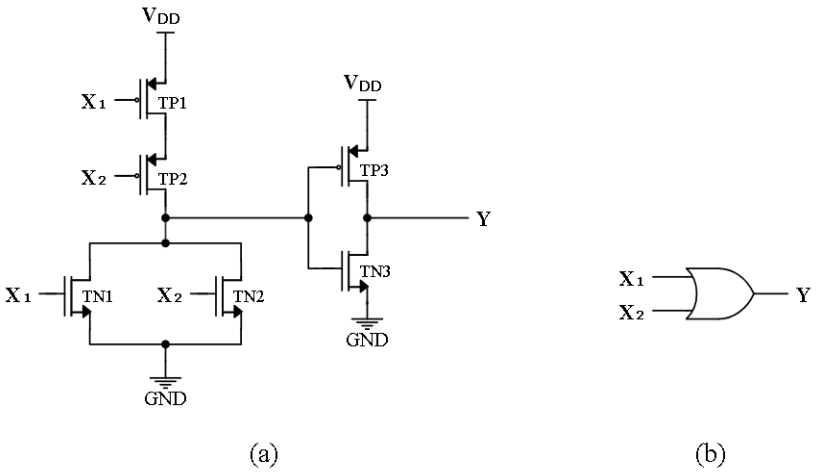
2.2.2.2 NAND and AND Logic Gates

A two-input NAND gate implements the Boolean function described in Equation 9 and represented in Table 3.

$$Y = \overline{X_1 X2} \tag{9}$$

For the implementation of a CMOS NAND gate, it is possible to notice in its truth table, shown in Table 3, that the output Y must be at logical '0' only when the inputs X_1

Figure 10: CMOS OR (a) implementation and its (b) symbol.



Source: Author, 2024.

Table 3: NAND truth table.

X_1	X_2	Y
0	0	1
0	1	1
1	0	1
1	1	0

and X_2 are at logical '1'. Thus, the PUN will be composed of two NMOS transistors in series. By the principles, Y will be at logical '1' when one or both inputs are at logical '0', so the PUN must be composed of two PMOS transistors in parallel. This implementation is shown in Figure 11(a), and the NAND gate symbol is shown in Figure 11(b). To increase the number of inputs of the gate, for any new input, an NMOS transistor is added in series with the others on the PDN, and a PMOS transistor is added in parallel with the others on the PUN.

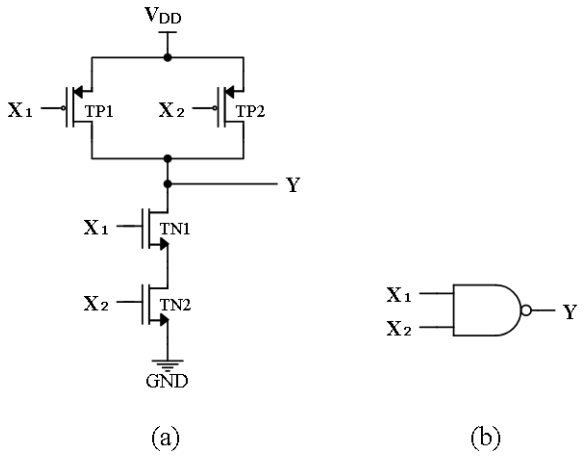
Consequently, to implement a CMOS AND gate, an inverter is connected to the NAND gate output, as shown in Figure 12. The AND Boolean function is presented in Equation 10 and represented in Table 4.

$$Y = X_1X2 \tag{10}$$

Table 4: AND truth table.

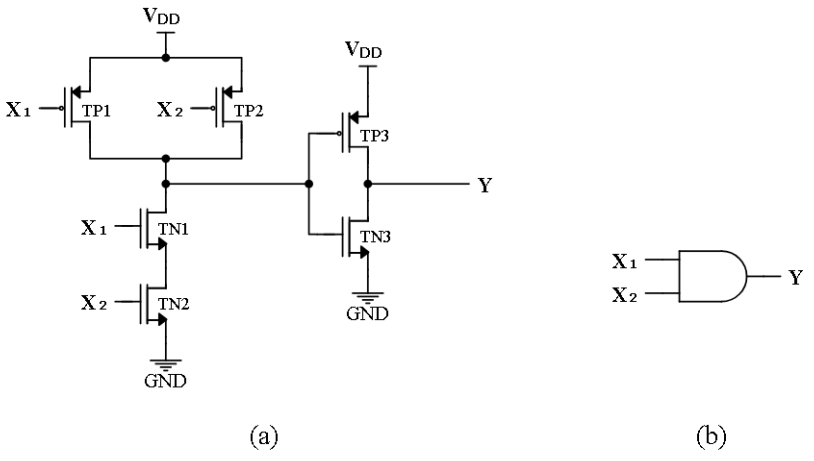
X_1	X_2	Y
0	0	0
0	1	0
1	0	0
1	1	1

Figure 11: CMOS NAND (a) implementation and its (b) symbol.



Source: Author, 2024.

Figure 12: CMOS AND (a) implementation and its (b) symbol.



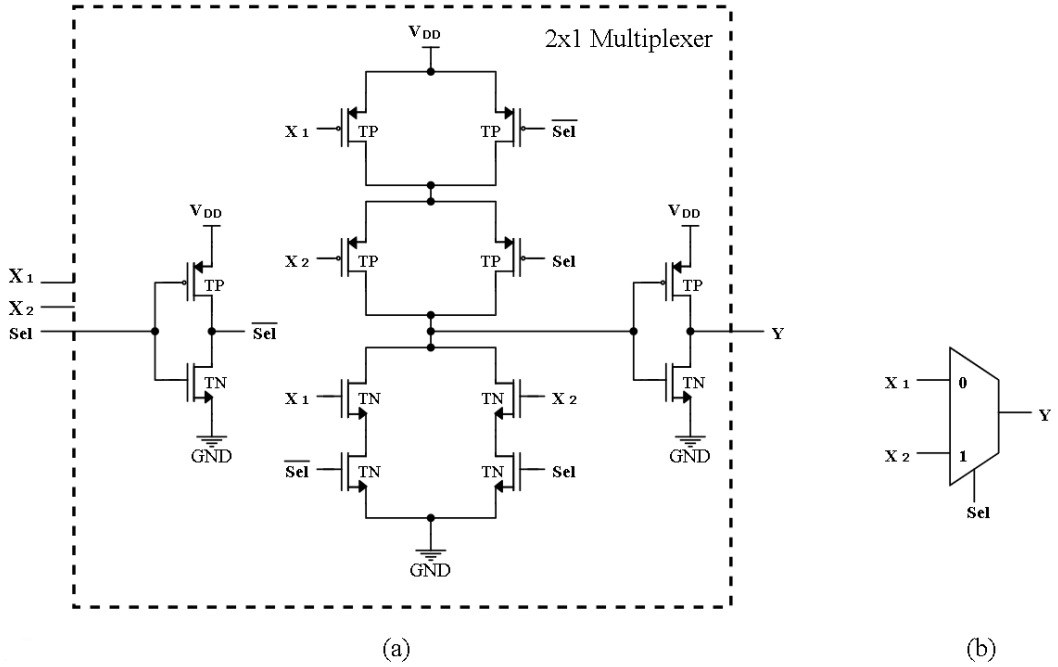
Source: Author, 2024.

2.2.2.3 *Multiplexer*

A multiplexer (MUX) is an electronic circuit that selects one input from two or more available inputs and connects it to a single output based on a binary selection signal (HAUPT; P. DACHI, 2016). The number of bits in the selection signal N, is determined by the number of inputs 2^N. For example, two inputs require a 1-bit selection signal, while four inputs require a 2-bit selection signal.

The smallest implementable multiplexer has two inputs and one output (MUX 2x1). The Boolean function of this MUX is presented in Equation 11, and its truth table is shown in Table 5. A MUX can be constructed using different combinations of logic gates. Another approach to implementing a multiplexer is through CMOS technology. An example of a CMOS implementation of a 2x1 MUX is depicted in Figure 13(a), along with its symbol in Figure 13(b). Additionally, it is possible to cascade multiplexers to increase the number of inputs to be multiplexed.

Figure 13: CMOS Multiplexer (a) implementation and its (b) symbol.



Source: Author, 2024.

$$Y = (\overline{Sel}\ X_1) + (Sel\ X2) \tag{11}$$

2.2.3 Transmission Gate

A transmission gate is an electronic circuit that controls the flow of signal levels between its input and output (ACD, 2024). It functions as a solid-state switch, consisting of a PMOS and an NMOS transistor to support both high and low logic states. These transistors operate in complementary fashion, with their gates biased oppositely to ensure that both are either turned on or off at the same time. Transmission gates are typically bidirectional, allowing signals to pass freely in either direction when the gate is enabled.

In a transmission gate, besides the input In and output Out, there is a control input En that enables the signal flow. For the implementation, the PMOS and NMOS transistors

Table 5: MUX truth table.

Sel	X_1	X_2	Y
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	1

are connected in parallel. An inverter is used to provide complementary enable voltages, since a NMOS transistor turns on when its gate is at logical one while a PMOS transistor turns on when its gate is at logical zero. With the same configuration, but only changing what transistor receives the En and the $\overline{En}$ control signals, it is possible to implement two types of transmission gates, as shown in Figure 14.

The transmission gate shown in Figure 14(a) is activated when the enable signal (En) is at '0', which means that when the enable signal is low, both the PMOS and NMOS transistors are biased to conduct. This happens because the En signal is applied to the PMOS while $\overline{En}$ is applied to the NMOS. Thus, when En is high, both transistors are in a cutoff state, resulting in an open switch. Conversely, the transmission gate shown in Figure 14(b) is activated when En is at '1', as both transistors are biased to conduct when the enable signal is high, and are cutoff when the enable signal is low. In this second configuration, the En signal is applied to the NMOS while $\overline{En}$ is applied to the PMOS.

When the transmission gate is acting as an open switch, the connection between In and Out is interrupted, placing the output in a high-impedance state ($High-Z$) where the resistance of the Out node is very high, effectively isolating it electrically. Conversely, when acting as a closed switch, the transmission gate allows the signal In ('0' or '1') to pass through to Out. Table 6 presents the truth table for TG_0 and TG_1, illustrating these three possible states.

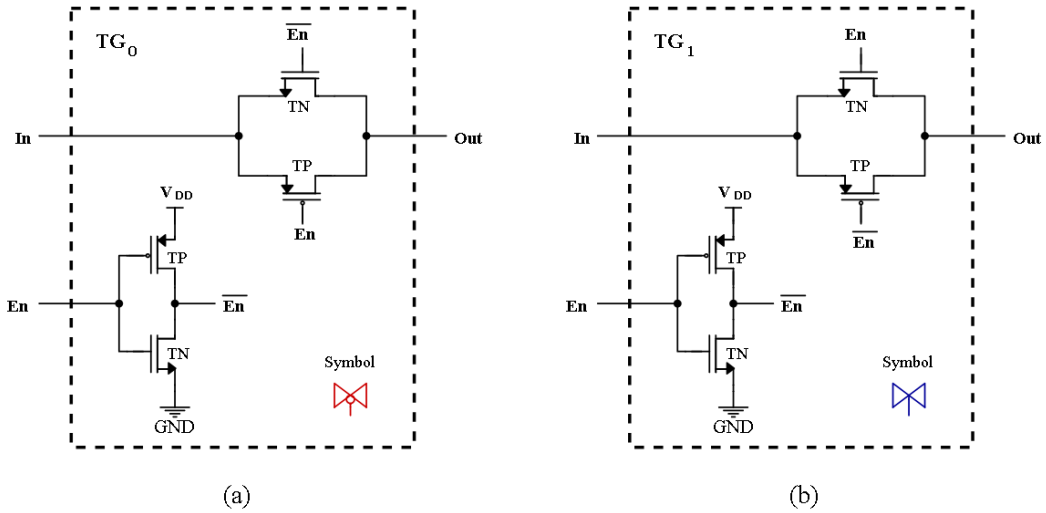
Table 6: Transmission gates truth table.

En	In	Out	
		TG_0	TG_1
0	0	0	High-Z
0	1	1	High-Z
1	0	High-Z	0
1	1	High-Z	1

2.3 Latch

The latch is considered the basic memory element (SEDRA et al., 2023), consisting of two cross-coupled logic inverters, G1 and G2, which form a positive feedback loop, as shown in Figure 15(a). By breaking the loop and applying an input signal (Figure 15(b)),

Figure 14: Implementation of CMOS transmission gate (a) activated at '0' (TG_0) and (b) activated at '1' (TG_1), with its symbols.



Source: Author, 2024.

the voltage transfer characteristic of the loop can be plotted (Figure 15(c)), revealing three possible operating points: A, B, and C. Points A and C are stable, allowing the circuit to operate indefinitely, while point B is unstable.

At the unstable point B, a voltage increase causes a regenerative effect, amplifying the signal until the circuit moves to point A or C, where the loop gain is low enough to prevent further amplification. This behavior illustrates the positive feedback characteristic of the inverters and underscores the importance of stable points for the proper latch operation.

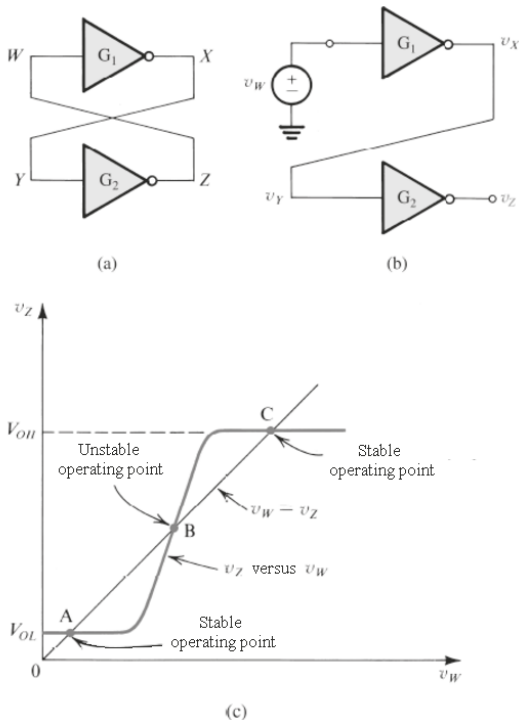
In summary, the latch is a bistable circuit, meaning it has two stable operating points with two complementary outputs. The stable state in which the latch operates depends on the external excitation that forces it into a particular state. The latch then memorizes this external action, remaining indefinitely in the acquired state. As a memory element, the latch can store one bit of information. Since the latch is sensitive to the input signal level, the state with a high level can be arbitrarily designated as corresponding to a stored logical '1'. The complementary state is then designated as a stored logical '0'. There are different ways to reproduce this behavior, whether by using CMOS logic gates or various other technologies and devices.

2.4 Memristor

The resistor, the capacitor, and the inductor are known as the three fundamental passive circuit elements. However, in 1971, Leon Chua proposed, based on symmetry arguments, the existence of a fourth fundamental circuit element, which he termed the memristor, as an abbreviation for "memory resistor" (CHUA, 1971). In this work, the memristor is the main component of the proposed full adder circuit, and it is this device that provides the non-volatility characteristic to the circuit.

Chua noted that there are six different mathematical relations connecting pairs of the four fundamental circuit variables: electric current i, voltage v, charge q and magnetic flux φ. Out of the six possible combinations of these four variables, five have led to well-known relationships. Two of these relationships are: the charge is the time integral of the

Figure 15: (a) Basic latch structure, (b) latch with open feedback loop and its (c) operation points.



Source: (SEDRA et al., 2023).

current, and the flux is the time integral of the electromotive force, or voltage (Faraday's law of induction) (STRUKOV et al., 2008). Three other relationships are given, respectively, by the axiomatic definition of the three classical circuit elements: the relationship between v and i of the resistor, the relationship between φ and i of the inductor, and the relationship between q and v of the capacitor. This considerations are illustrated in Figure 16. Only the relationship between φ and q remained undefined; thus, there should be a fourth basic circuit element described by this relationship: the memristor, with memristance M.

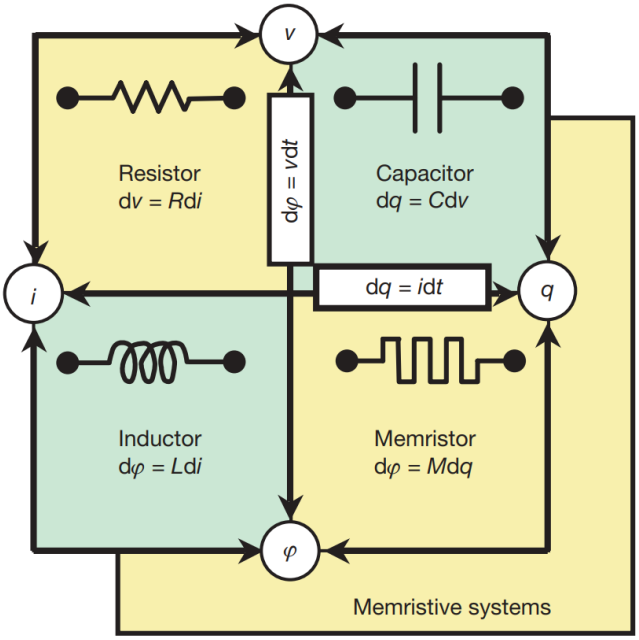
The mathematical relation describing the memristor is shown in Equation 12. Since magnetic flux and charge can be expressed as the time integrals of voltage and current, respectively, as shown in Equations 13 and 14, the memristor exhibits a resistance that depends on the historical behavior of the current passing through it or the voltage drop across its terminals. This resistance can increase or decrease, depending on the direction of the current flow. Once the electrical stimulus is removed, the component retains its final resistance value (GARCíA-REDONDO; LóPEZ-VALLEJO; ITUERO, 2014). For this reason, the memristor is classified as a non-volatile device.

$$d\varphi = M\, dq \tag{12}$$

$$\varphi = \int_{-\infty}^{\tau} v(\tau)\, d\tau \tag{13}$$

$$q = \int_{-\infty}^{\tau} i(\tau)\, d\tau \tag{14}$$

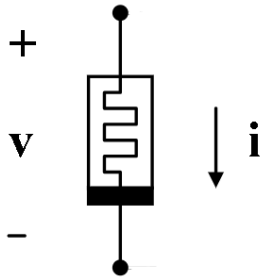
Figure 16: The four fundamental circuit elements: resistor, capacitor, inductor and memristor, and the mathematical relations between the four fundamental circuit variables.



Source: (STRUKOV et al., 2008).

For linear elements, where M is constant, memristance is identical to resistance. However, if M is a function of q, creating a nonlinear circuit element, no combination of nonlinear resistive, capacitive, or inductive components can replicate the unique properties of this nonlinear memristor. The $i - v$ characteristic curve of this nonlinear relationship between q and φ typically forms a frequency-dependent Lissajous figure. The memristor electrical symbol and the adopted polarity for electrical stimulus application are shown in Figure 17.

Figure 17: Memristor electrical symbol and adopted polarity.



Source: Author, 2024.

The mathematical definition of a current-controlled memristor for circuit analysis is expressed in the differential form represented in Equations 15 and 16 (STRUKOV et al., 2008). In these equations, w represents the state variable of the device, corresponding to q, while R denotes the generalized resistance that depends on the device's internal state.

$$V = R(w)\, i \tag{15}$$

$$i = \frac{dw}{dt} \tag{16}$$

Later, (CHUA; KANG, 1976) generalized the memristor concept to a broader class of nonlinear dynamical systems called memristive systems, which are described by Equations 17 and 18. In these equations, w can represent a set of state variables, and both R and f can generally be explicit functions of time.

$$V = R(w, i)\, i \tag{17}$$

$$f(w, i) = \frac{dw}{dt} \tag{18}$$

2.5 Magnetic Tunnel Junction - MTJ

A device with similar properties to memristors, but with a different functional mechanism, is the magnetic tunnel junction (MTJ). This device is introduced here only to provide the foundation for the reference circuits used in this work, as it serves as their main component. It is important to highlight that the devices used to design the proposed non-volatile full adder are memristors, not MTJs.

A MTJ is a device that enables electrical conduction through electron tunneling across a thin insulating barrier. A spin transfer torque magnetic tunnel junction (STT-MTJ) device consists of two thin ferromagnetic films separated by an oxide barrier. It presents two resistance values depending on the relative magnetization orientation of the two ferromagnetic layers: parallel R_P or anti-parallel R_{AP}, as shown in Figure 18.

Figure 18: Magnetic tunnel junction (MTJ) structure and the two possible states of relative magnetization orientation.

Source: (SLIMANI et al., 2016)

A STT-MTJ can switch between two resistance values through spin transfer torque mechanism, when a bidirectional current i is higher than its critical current. The difference between the two resistances values is explored in Hybrid CMOS-MTJ logic circuits to provide the correct logic output. This resistance difference is characterized by Tunnel Magneto Resistance ratio TMR, in Equation 19.

$$TMR = \frac{R_{AP} - R_P}{R_P} \tag{19}$$

In hybrid CMOS-MTJ logic circuits, the MTJs serve both as memory and functional inputs. These circuits are usually composed of three parts: a current comparator, also known as a pre-charge sense amplifier (PCSA), a writing circuit, and two logic networks constructed by MTJs and CMOS transistors. The circuit functionality is based in two stages: write and read. The write circuit is responsible to set a pair of MTJs (one in each

logic network) in opposite configuration. The circuit uses a pair of complementary inputs to properly set the current flow based on the desired value to be stored. This difference in the resistance causes different discharge currents in each branch during reading mode. The PCSA is used to sense the current difference of the two pull-down networks.

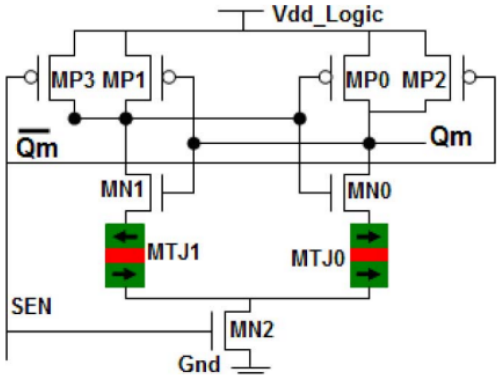
3 PREVIOUS WORK

The implemented solution uses a non-volatile majority voter as its core to generate the outputs of the full adder, along with a non-volatile latch to bring this crucial characteristic to the developed circuit. Both are based on circuits implemented using MTJs, whose operation and features will be presented in this chapter.

3.1 Latch Reference Circuit

In this work, the latch circuit used as a reference (VERMA; PAUL; SHUKLA, 2022) is based on a pre-charged sense amplifier (PCSA), as shown in Figure 19. This circuit consists of two inverters—composed of MP0 and MN0, and MP1 and MN1—two PMOS transistors (MP2 and MP3) in parallel with MP0 and MP1, respectively, and one NMOS transistor (MN2) connecting the circuit to ground. The memory and non-volatility of the circuit are provided by two MTJs.

Figure 19: Hybrid CMOS-MTJ latch.



Source: (ZHAO et al., 2009).

The PCSA operates in two phases, determined by the control signal SEN. When SEN is set to '0', the PCSA pre-charges the polarization voltages of the two MTJs. However, since MN2 remains closed, no stationary current flows through the circuit. As SEN transitions from '0' to '1', the pre-charged voltages begin to discharge. Due to the differing resistances of the two MTJs, the discharge rates of each branch vary. For example, if the ferromagnetic layers of MTJ1 are anti-parallel while those of MTJ0 are parallel, then R_{MTJ1} is greater than R_{MTJ0}, and the discharge current I_{MTJ0} will be higher than I_{MTJ1}. During this rapid discharge process, Qm will decrease faster than $\overline{Qm}$, and when Qm drops below the threshold switching voltage of the inverter amplifier

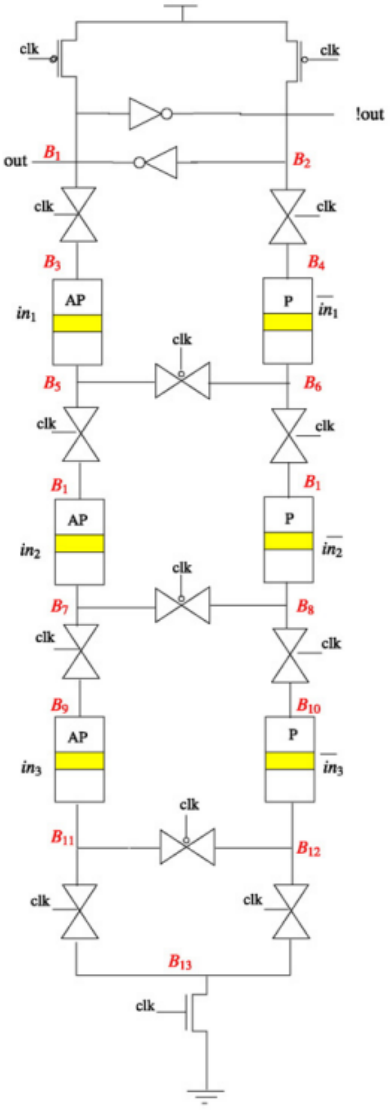
made up of MP0 and MN0, $\overline{Qm}$ will be charged to Vdd_Logic (logic '1'), while Qm continues discharging to '0'.

There is never any stationary current flow in the circuit, only the charging or discharging of capacitors, which consumes negligible power, along with the leakage current. Thus, it is possible to consider that the power consumption is nearly zero. This characteristic is a key feature of the circuit's low power consumption, as there are practically no continuous currents that would otherwise dissipate energy as heat.

3.2 Voter Reference Circuit

The majority voter is a circuit that outputs '1' if the majority of its inputs are logic high, and '0' if the majority are logic low. A significant application of this circuit is in generating the carry output in full adders. In this work, the majority voter circuit used as a reference (SLIMANI et al., 2016) for the implemented solution is a Hybrid CMOS-MTJ majority voter, as shown in Figure 20 (SLIMANI et al., 2016).

Figure 20: Hybrid CMOS-MTJ majority voter.



Source: Adapted, (SLIMANI et al., 2016)

The reference majority voter circuit utilizes transmission gates (TGs) to isolate the two operational stages. The TGs in the resistive branches are in a conducting state during the reading period and in an isolation state during the writing stage. Conversely, the TGs between the resistive branches are configured complementarily. They are in a conducting state during the writing period and in an isolation state during the reading stage.

The writing operation occurs when the control signal clk is low. Based on each input value, a current flows through the corresponding pair of MTJs, and its direction determines the stored values. The pairs of MTJs—MTJ1 and MTJ11, MTJ2 and MTJ22, and MTJ3 and MTJ33—are always configured oppositely. The majority voter read operation takes place when the clk signal is high. During this phase, a pre-charge sense amplifier (PCSA) detects the resistance difference between the two branches to generate the correct logical level at the output (ZHAO et al., 2009), as explained in Section 2.3.

4 NON-VOLATILE FULL ADDER

A full adder is a digital circuit that adds three single-digit binary bits. The first two inputs are the bits A and B, and the third input is the C_{in}, known as the carry in. The outputs are two single-digit binary bits: the Sum, that gives the value of the least significant bit of the sum, and the C_{out}, the output carry bit. The full adder truth table is shown in Table 7. When two or more full adders are connected in cascade, the C_{in} pin of a full adder is connected to the C_{out} pin of the previous adder, receiving its carry out bit, hence its names.

Table 7: Full adder truth table.

A	B	Cin	Sum	$Cout$
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

The implemented solution uses a hybrid architecture of CMOS technology with memristors to build a fully non-volatile full adder. The non-volatility characteristic is given by the memristor, which has the ability to store its logical state in the form of electrical resistance, even when de-energized, as discussed in Section 2.4.

In the first section of this chapter, the operation and characterization of the memristor model used in this work will be discussed. Following that, the chosen transistor technology will be addressed. The subsequent sections will focus on the implemented solution, describing the proposed circuit, its logical sequence of operation, and the circuit's sizing.

4.1 JART VCM v1b Memristor Model

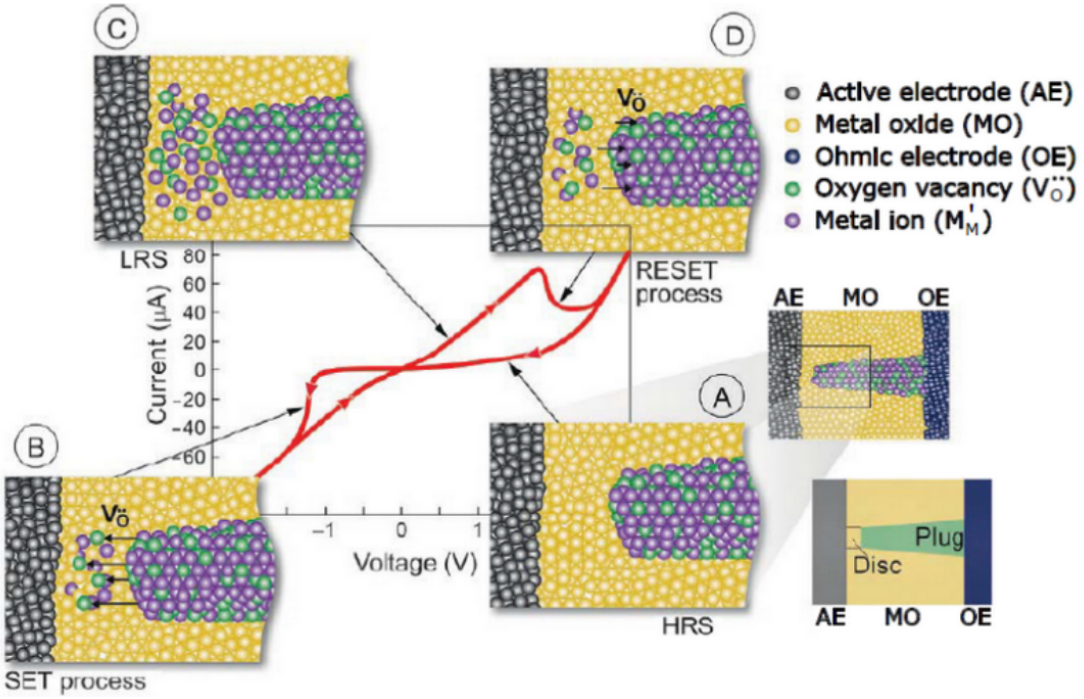
To develop this work, a real memristor model was selected. The Electronics Material Research Laboratory (WASER, 2024) was chosen as the source due to its provision of freely available models for research, accompanied by user manuals. The JART VCM v1b memristor model was selected, based on its principles and mechanisms of operation, and the information available about it. Furthermore, this memristor model had already been

used in other solutions researched and developed by the author, making it familiar and supporting the reasons for its choice. This model is not an MTJ; it is a memristor.

The JART VCM v1 memristor model simulates the switching characteristics of devices based on the Valence Change Mechanism (VCM). This mechanism consists of a metal-insulator-metal (MIM) system, where the insulator is typically a transition metal oxide (MO). The electrode materials are different concerning their oxygen affinity and work function. As a result, at the interface between the electrically active electrode (AE), which exhibits a high work function and a low oxygen affinity, a Schottky barrier is formed. On the other hand, a metal with a low work function and high oxygen affinity is chosen for the counter electrode. Due to the ohmic contact formed with the metal oxide, this electrode is referred to as the ohmic electrode (OE).

Figure 21 illustrates the switching mechanisms in a VCM device, showing the transition between a high resistive state (HRS) and a low resistive state (LRS). During the initial forming step, the metal oxide undergoes reduction, resulting in the formation of a highly n-conductive filament enriched with oxygen vacancies that function as mobile donors. This structure typically consists of two distinct regions: the disc region and the plug region, as depicted in the bottom-right corner of the figure. The switching occurs within the disc region, a confined area near the interface between the AE and the MO. In this region, localized redox (reduction-oxidation) processes (CARTER, 1995) during switching, that can be expressed as an ionic motion of the oxygen vacancies, modulate the Schottky barrier. This modulation directly influences the conductivity of the VCM cell.

Figure 21: Switching mechanism in a bipolar switching VCM cell. Schematic I-V-curve with illustrations of the different switching stages. The green and purple spheres indicate the mobile oxygen vacancies and the immobile metal ions in a lower valence state, respectively. (A) High resistive state (HRS); (B) SET process; (C) low resistive state (LRS) and (D) RESET process.



Source: (BENGEL et al., 2024).

The plug region contains the primary oxygen-deficient filament and remains highly n-conductive throughout the switching process. When a voltage is applied to the active electrode with the ohmic electrode grounded, it is possible to obtain a typical characteristic I-V-curve, illustrated in Figure 21. In the HRS, depicted in Figure 21(A), the disc region is fully oxidized, leading to low conductivity in the VCM device. Applying a negative voltage to the AE initiates the SET process, illustrated in Figure 21(B), during which positively charged oxygen vacancies (represented by green spheres) within the plug are drawn into the disc. This movement induces a valence change in the metal ions (represented by purple spheres) and reduces both the width and height of the Schottky barrier.

After the SET, the device is in the LRS, represented in 21(C). The RESET process occurs when a positive voltage is applied to the active electrode. In this step, oxygen vacancies are driven back into the plug region, as illustrated in Figure 21(D), restoring the original width and height of the Schottky barrier. The I-V characteristics, along with the observed switching behavior, are classified as bipolar switching, since the RESET and SET processes occur at opposite voltage polarities. Additionally, the switching mechanism, which relies on the redistribution of oxygen vacancies within the filament, is often referred to as counter-clockwise (c8w) switching. This term originates from the shape of the I-V curve, which resembles a tilted, inversely written "8" (WASER, 2012).

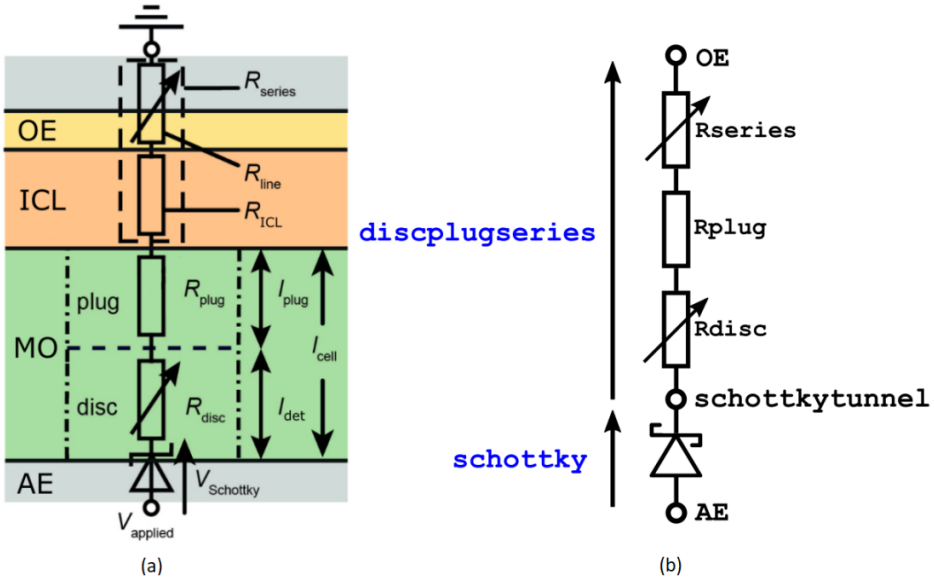
In short, a negative voltage applied to the AE leads to the SET process, where the memristor switches between a HRS to a LRS. In contrast, a positive voltage applied to the AE leads to the RESET process, where the resistance changes from LRS to HRS. The resistances in LRS and HRS can be called respectively R_{ON} and R_{OFF}, and the voltages that trigger the switching on the SET and RESET process can be referenced as V_{ON} and V_{OFF}, respectively.

The JART VCM v1b model represents an improvement of the JART VCM v1a model (BENGEL et al., 2024). In this second version, some of the equations and parameters have been modified to describe the switching dynamics of HfO_x based ReRAM (Resistive Random Access Memory) devices, maintaining the same operating principle. The model incorporates the SET and RESET kinetics, emphasizing the initial states preceding the SET and RESET processes. This update improves the alignment of the SET and RESET behaviors with the observed I-V characteristics, as well as the transitions between the HRS and the LRS, offering a better match compared to the JART VCM v1a model.

The description code of this memristor model is made available in Verilog-A. Figure 22(a) shows the equivalent circuit diagram of the electrical model. The VCM cell described in the JART VCM v1b model incorporates an additional inherent conduction layer (ICL), which is reported to positively influence the reduction of variability in both the SET process and the high resistive state (HRS) (HARDTDEGEN et al., 2018). The Verilog-A electrical model is illustrated in Figure 22. Three electrical nodes are defined: AE, schottkytunnel, and OE. The *schottky* branch connects the AE and schottkytunnel nodes, whereas the *discplugseries* branch connects the schottkytunnel and the OE nodes.

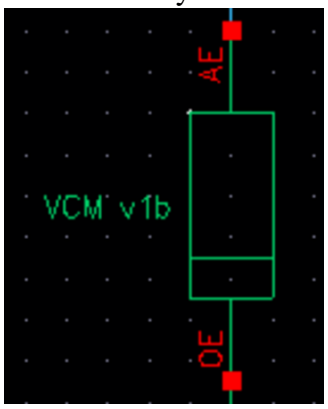
The JART VCM v1b Verilog-A code is deterministic and describes the memristor model with parameters and physical equations. To use this memristor in the simulations for the implemented solution, the model was inserted in a personal Virtuoso library, creating a component from the Verilog-A code with its own symbol, as shown in Figure 23. With this, it is possible select this component in the personal library and use it in schematic circuits and projects, having access to change parameters that can be configured. No model parameters were changed via the tool for any simulation and experiment. All parameters were kept at their default value (BENGEL et al., 2024).

Figure 22: (a) Equivalent circuit diagram of the JART VCM v1b model and (b) its electrical model in Verilog-A.



Source: (BENGEL et al., 2024).

Figure 23: JART VCM v1b symbol created on Virtuoso.

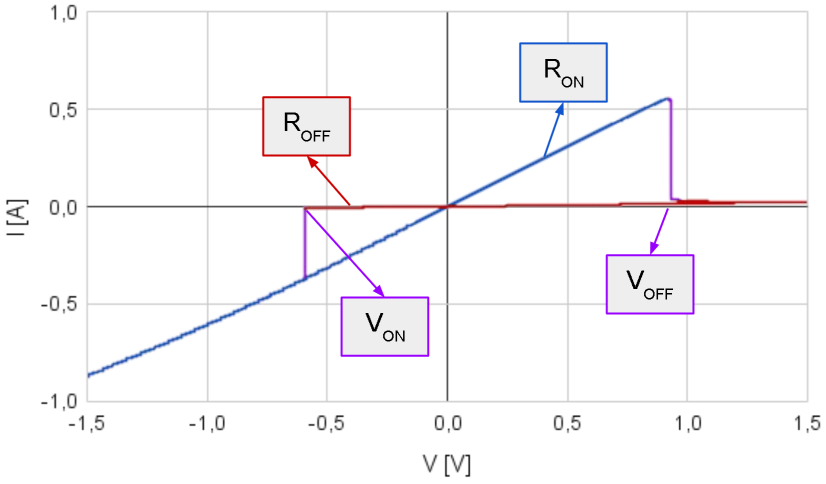


Source: Author (2024).

The values of R_{ON}, R_{OFF}, V_{ON}, and V_{OFF} do not have their value defined directly in the code, but depend on a series of parameters predefined, including thermal and material characteristics parameters. To obtain these values, that need to be considered in the design of the solution, the I-V-curve of this model was traced via simulation. The curve was obtained by applying a triangular voltage wave with maximum values of -1.5V and 1.5V in the AE terminal, while the OE terminal was grounded. A piecewise linear (PWL) source, that constructs a waveform from a series of straight line segments connecting the defined points, was used. The source was configured with four points following the pattern $(time[s], voltage[V])$, which were: $(0, 0)$, (1.5,-1.5), $(4.5, 1.5)$ and $(6, 0)$.

In Figure 24, it is possible to identify the shape of two lines with different steepness. The less steep line, in red, represents the HRS (R_{OFF}), while the steeper one, in blue, represents the LRS (R_{ON}). By choosing two distinct points on each line, it is possible to calculate the approximate resistance of each state through the application of Ohm's Law. In the $I - V$ curve, it is also possible to identify the transition points between LRS and HRS, and vice versa. The voltage at which the memristor switches from R_{OFF} to R_{ON} is the threshold voltage V_{ON}, while the voltage at which the memristor switches from R_{ON} to R_{OFF} is the threshold V_{OFF}. The resistances and threshold voltage values found in this procedure are listed in Table 8.

Figure 24: I-V-characteristic curve of JART VCM v1b memristor model.



Source: Author (2024).

Table 8: JART VCM v1b memristor model parameters.

Parameter	Value
V_{ON}	-0.60 V
V_{OFF}	0.90 V
R_{ON}	1.61 kΩ
R_{OFF}	63.1 kΩ

4.2 X-FAB 180nm Transistor Technology

The XC018 series is X-FAB 0.18 micron modular logic and mixed signal technology. Its main applications include standard logic/controller circuits, mixed signal embedded systems, systems on a chip (SOC), high precision mixed signal circuits and low power mixed signal circuits. It is a node of 0.18-micron single polycrystalline silicon, up to six-metal N-well CMOS basic process. The technology also features modules for metal-insulator-metal capacitors, high resistive poly, dual gate oxide transistors.

The chosen devices were the 1.8V NMOS and PMOS, named as ne and pe in the XC018 series, respectively. These devices parameters can be seen in Table 9.

Table 9: XC018 ne and pe devices parameters.

Device	Name	V_{th} [V]	Max. V_{DS}, V_{GB} [V]
$1.8VNMOS$	ne	0.60 V	1.98 V
$1.8VPMOS$	pe	0.65 V	1.98 V

4.3 Proposed Circuit

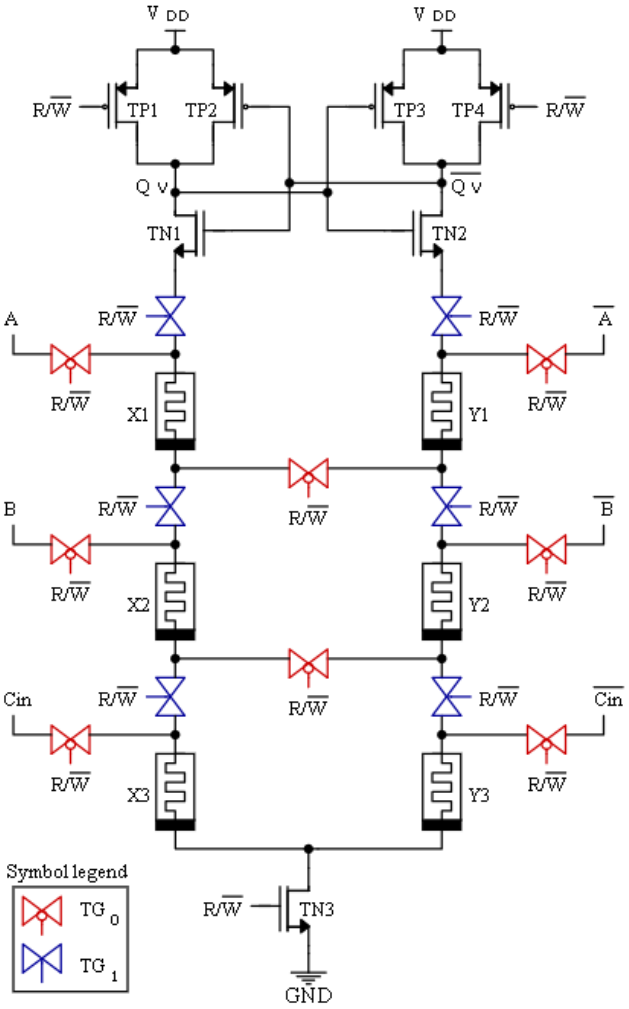
The proposed circuit uses the majority voter detailed in Section 3.2 as its main component, replacing the MTJs for memristors, as shown in Figure 25, and maintaining its operating characteristics. No MTJs were used in this project; only the JART VCM v1b memristor model was utilized. By comparing the truth tables of the full adder and the majority voter, as shown in Table 10, it is evident that the C_{out} bit of the full adder is identical to the voter output for all input combinations. However, the Sum output matches the voter output only when the logic levels applied to the A, B, and C_{in} inputs are identical. If one of the inputs differs from the others, the Sum equals the majority voter output complement.

Table 10: Comparison between the full adder and the majority voter truth tables.

A	B	C_{in}	Full adder		Majority Voter
			Sum	C_{out}	
0	0	0	0	0	0
0	0	1	1	0	0
0	1	0	1	0	0
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	0	1	1
1	1	0	0	1	1
1	1	1	1	1	1

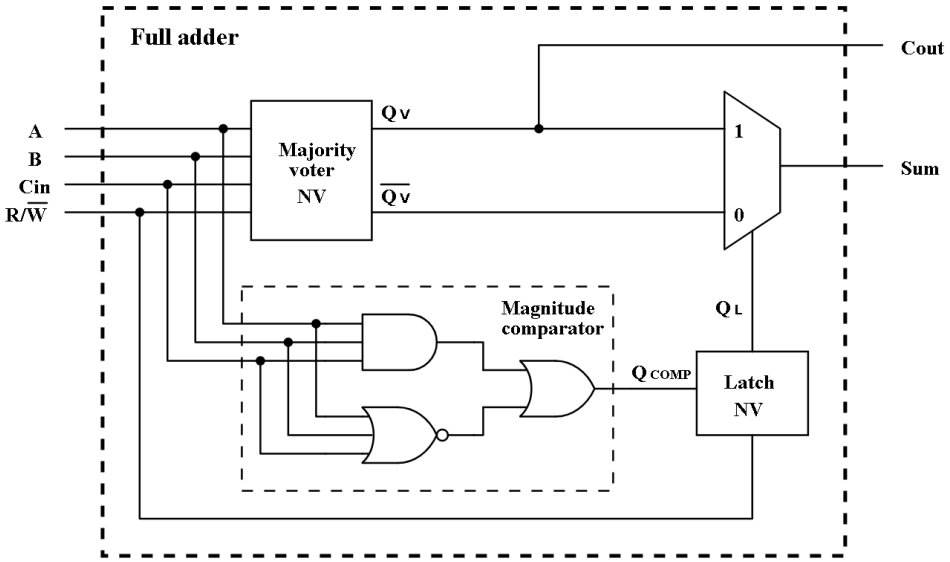
To compose the full adder, its C_{out} output was directly connected to the voter output, Q_V. On the other hand, its necessary to add other circuit elements to determine the Sum output based on the adder inputs (A, B and C_{in}) and the voter outputs (Q_V and $\overline{Q_V}$). This addition must select the voter output Q_V to be connected to the Sum output when the input combination is "000" or "111". For any other combination, the $\overline{Q_V}$ voter output must be selected. The block diagram for the proposed circuit can be seen in Figure 26.

Figure 25: CMOS/memristor majority voter circuit.



Source: Author (2024).

Figure 26: Fully non-volatile full adder circuit.

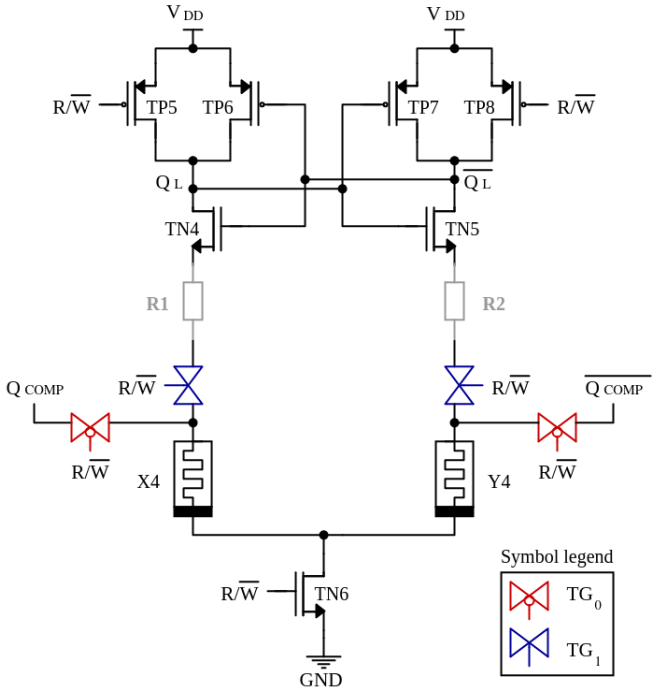


Source: Author (2024).

For the selection part, a two-input one-output multiplexer with CMOS architecture was used, following the implementation discussed in Section 2.2.2.3. The only difference is that the inverter for the control signal was not necessary, since the MUX control signal comes from a latch that already generates its complement, as shown in Figure 28. The MUX inputs are the voter outputs, and its output is the full adder output Sum.

The latch, with the same architecture and structure discussed in Section 3.1, but with all MTJs replaced by JART VCM v1b memristors, is used to assign the non-volatility characteristic to the circuit. This way, if the power supply is removed, the circuit is capable to select the right multiplexer input after its reestablishment. The latch schematic is shown in Figure 27. Two resistors, $R1$ and $R2$, are used in this circuit to ensure its proper functioning. Their purpose will be detailed further in Section 4.5.

Figure 27: Non-volatile Latch.



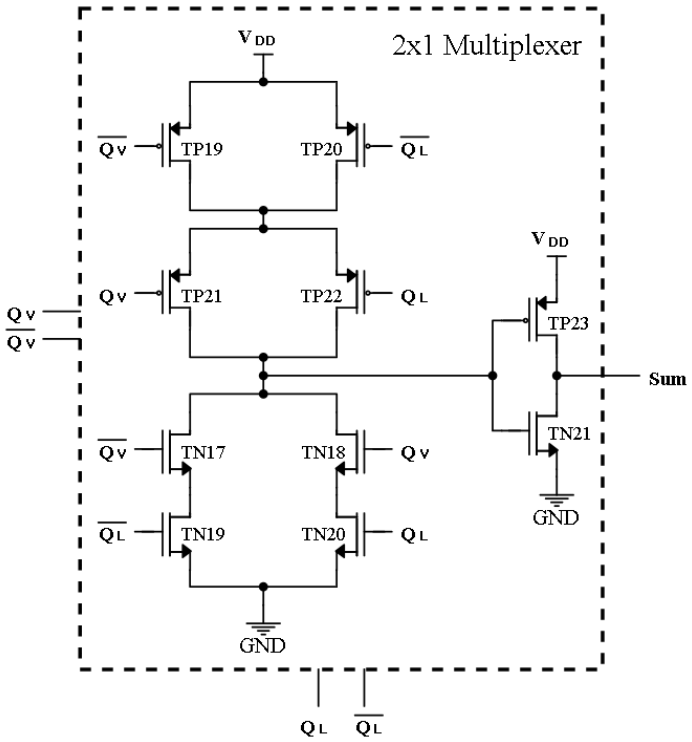
Source: Author (2024).

The latch input signal Q_{COMP}, that will later control the MUX, comes from a magnitude comparator circuit, composed by an AND, a NOR and an OR logic gates of CMOS architecture. The Boolean function of this circuit is presented in Equation 20 and its schematic is shown in Figure 29. This circuit is necessary to signal when all the inputs have the same magnitude, that is, when the input combination is "111" or "000", since these are the only combinations where the Sum output equals the voter output.

$$Q_{COMP} = (ABC) + \overline{(A + B + C)} \tag{20}$$

The AND gate is responsible to generate the logic '1' for the input combination "111", and the NOR gate for the "000" input combination. As described in Section 2.2.2, for all other combinations, both gates generate logic '0' as output, and the OR gate adds this two effects, generating the comparator output Q_{COMP}. From the magnitude comparator truth table, presented in Table 11, it is possible to notice that the circuit output is "1" when the inputs are the same, and '0' when they differ. Therefore, the Q_V voter output is connected

Figure 28: CMOS based 2x1 multiplexer circuit.



Source: Author (2024).

to the multiplexer ’1’ input, and the $\overline{Q_V}$ is connected to its "0" input, as represented in Figure 26.

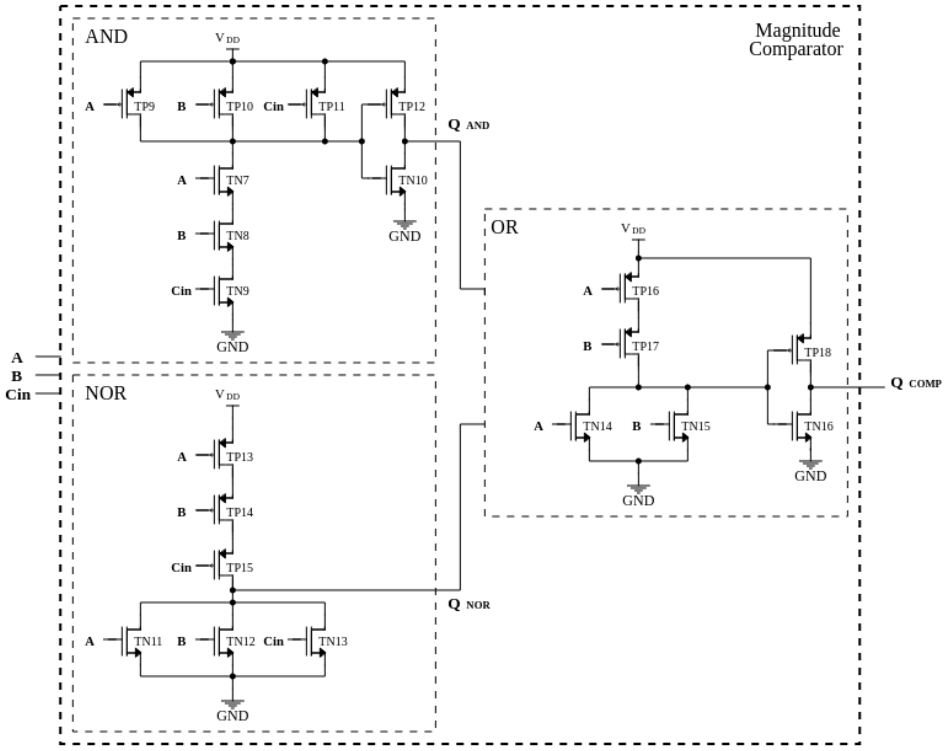
Table 11: Magnitude comparator truth table.

A	B	C_{in}	Q_{COMP}
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1

4.4 Logical Sequence of Operation

The circuit operation occurs in two stages, controlled by a *Read/Write* signal denoted by $R/\overline{W}$. The $Write$ stage receives this name because it is when the input voltages are applied to the memristors, and they may or may not switch their resistance state, depending on the input values. Alternatively, the $Read$ state involves obtaining the output signals from the circuit, namely the result of the sum. All the transistors and transmission gates play an important part in the circuit operation, since they are used to control what happens on both stages.

Figure 29: CMOS based magnitude comparator circuit.



Source: Author (2024).

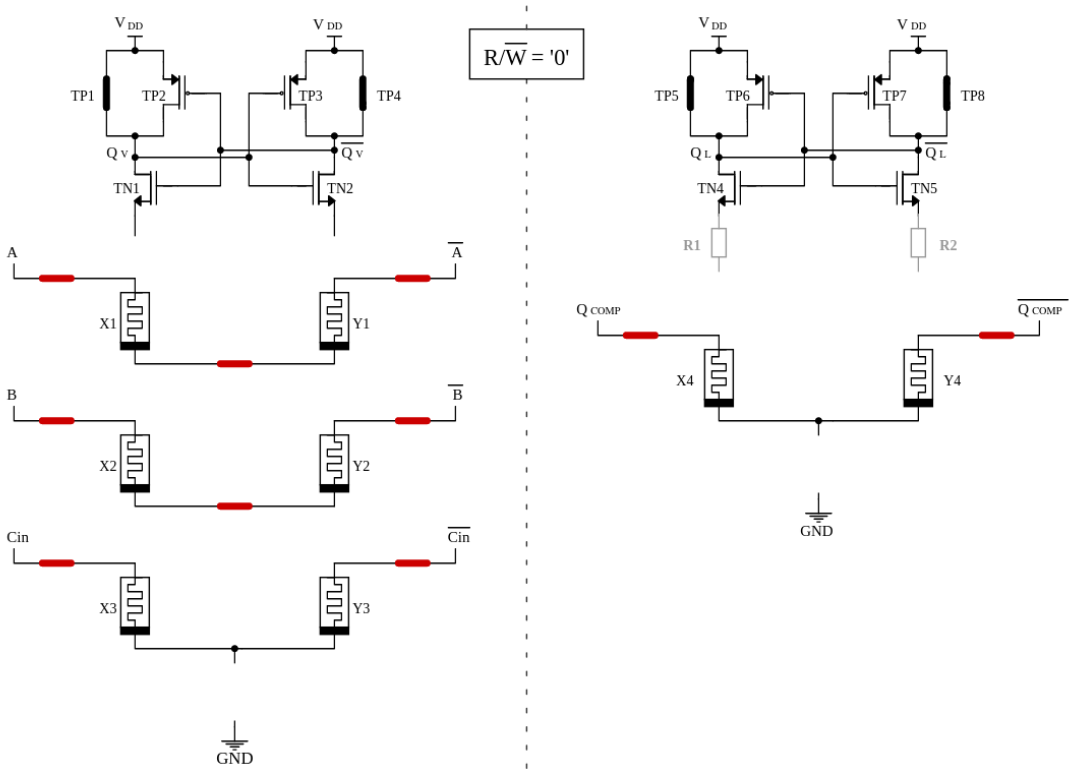
In the $Write$ stage, when the $R/\overline{W}$ signal is at logical zero, the inputs are applied to the magnitude comparator circuit, generating its Q_{COMP} output signal, that is the input to the non-volatile register. The low logical level at $R/\overline{W}$ pre-charges Q_L and $\overline{Q_L}$ on the latch circuit with the supply voltage V_{DD}, through the conduction path formed by transistors $TP5$ and $TP8$, respectively. The same pre-charge with V_{DD} happens on Q_V and $\overline{Q_V}$ at the voter circuit, through the conduction path formed by transistors $TP1$ and $TP4$.

Simultaneously, the transmission gates activated at '0' (TG_0) are on, forming conduction paths through the memristors at the voter and register circuits. There is no stationary current in both circuits as $TN3$ and $TN6$ are not conducting. Therewith, the input logical levels are stored as complementary/non-complementary resistance states in the devices Xn/Yn. For example, when A='1', $X1$ will be in the R_{OFF} state (logical zero) and $Y1$ will be in the R_{ON} state (logical one). An illustration of the $Write$ stage is shown in Figure 30.

When a rising edge occurs in the $R/\overline{W}$ signal, the TG_0 are disabled, while the transmission gates activated at '1' (TG_1), starts conducting. The voter and latch pass transistors $TN3$ and $TN6$, respectively, also starts conducting. Therefore, paths are created to discharge the pre-charged voltages in Q_L and $\overline{Q_L}$ on the latch, and in Q_V and $\overline{Q_V}$ on the voter. Since, for both circuits, the equivalent resistances of its two branches (X and Y) are different, the discharge speed will be different for each branch, which will result in these outputs being updated. The register Q_L output is connected to the multiplexer control signal and its value defines which of its inputs is taken to the Sum output. An illustration of the $Read$ stage is shown in Figure 31.

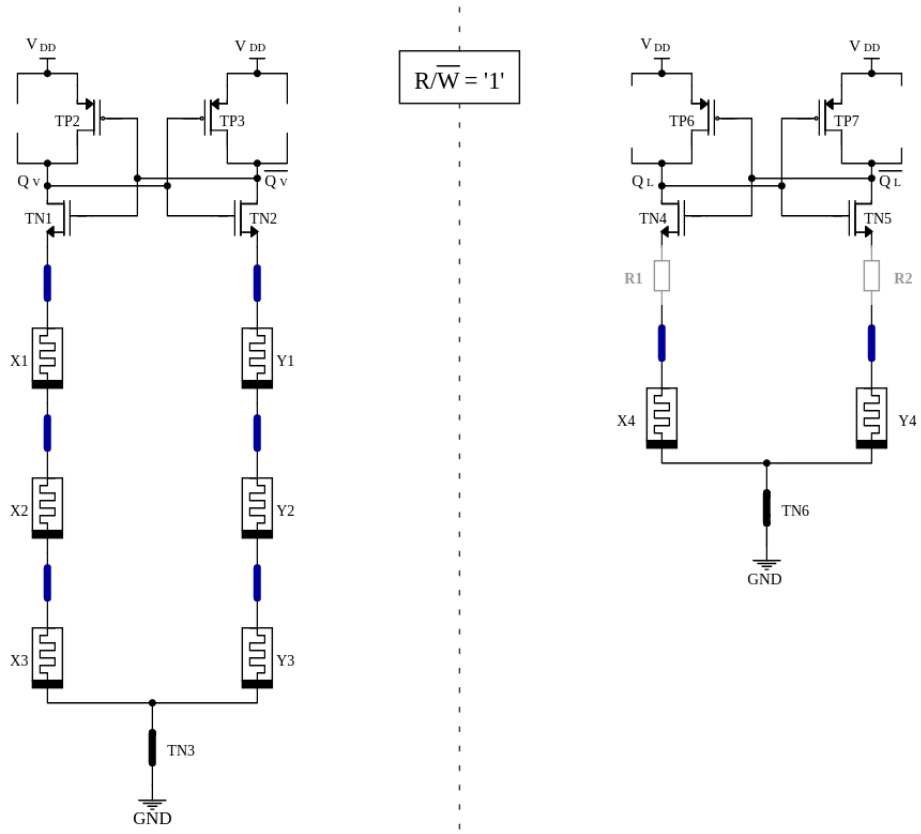
If the power supply is removed from the full adder, the written logical states remain

Figure 30: Illustration of the $Write$ stage of operation on majority voter and latch circuits.



Source: Author (2024).

Figure 31: Illustration of the $Read$ stage of operation on majority voter and latch circuits.



Source: Author (2024).

stored in the memristors in the form of resistance states. This insures the non-volatility characteristic of the implemented solution.

4.5 Constraints for Circuit Sizing

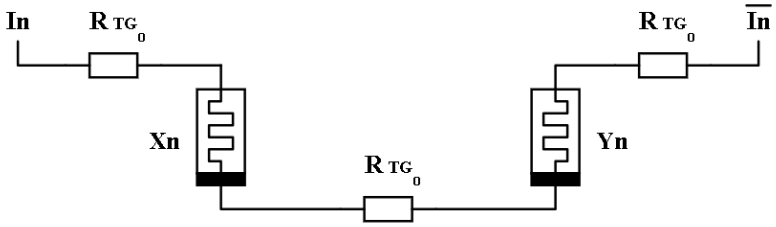
To ensure the correct operation of the circuit, it is essential that there is compatibility in the selection of the memristor parameters and the dimensions of the transistors. For this, the $Write$ and $Read$ stages on the memristors must be analyzed. In the voter circuit, when the signal $R/\overline{W}$ is at a low logic level, three electrically isolated paths are created, each consisting of two memristors and transmission gates active in '0', with resistance R_{TG_0}. For this stage of operation, the mentioned parameters must be adjusted so that the voltage drop across each of the memristors exceeds the threshold values associated with each resistance switching, as shown in table 8.

For this dimensioning, the input and power supply signals of the circuit have the same voltage level, so $In = V_{DD}$. Since the elements Xn and Yn of a memristor pair store complementary logical states in the form of resistances R_{ON} and R_{OFF}, the dimensioning aims to address the worst-case scenario, as shown in Figure 32. The device with resistance R_{OFF} will switch to R_{ON} first, as the voltage drop across it will be significantly higher. After this switching, the portion of the V_{DD} voltage remaining across the other memristor must increase above $|V_{OFF}|$ in paths with three gates, satisfying Equation 21. Thus, the restriction shown in Equation 22 applies, obtained through Kirchhoff's Circuit Laws. This analysis is also valid for the latch, since without a third transmission gate, the needed voltage drop is smaller.

$$V_{R_{ON}} \geq |V_{OFF}| \tag{21}$$

$$V_{DD} \cdot \frac{R_{ON}}{3 \cdot R_{TG_0} + 2 \cdot R_{ON}} \geq |V_{OFF}| \tag{22}$$

Figure 32: Illustration of the conduction path created in the $Write$ stage of operation on majority voter and latch circuits, for the wort case scenario.



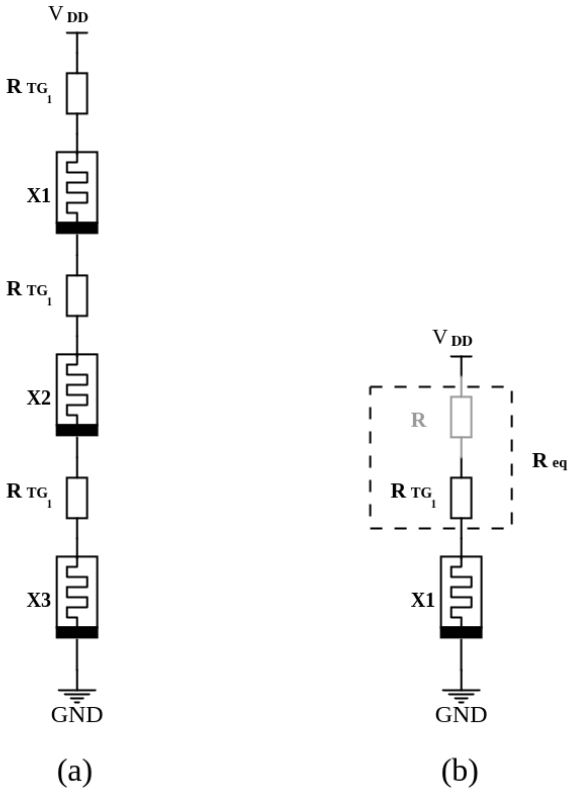
Source: Author (2024).

The second analysis included in the design focuses on the moment when a $Read$ stage is executed. In this circumstance, considering the adopted polarity, the magnitude of the voltage drop across each memristor must not exceed $|V_{OFF}|$, to ensure that the action is non-destructive, i.e., that the resistance state of the memristors is not affected by the read operation. Consequently, the worst-case scenario for the voter occurs when all memristors are in the R_{ON} state. Since there are three transmission gates in each branch, as shown in Figure 33(a), the described situation is mathematically represented by Equations 23 and 24, where R_{TG_1} corresponds to the resistance of the transmission gates active in '1'.

$$V_{R_{ON}} < |V_{OFF}| \tag{23}$$

$$V_{DD} \cdot \frac{R_{ON}}{3 \cdot R_{TG_1} + 3 \cdot R_{ON}} < |V_{OFF}| \tag{24}$$

Figure 33: Illustration of the conduction path created in the $Read$ stage of operation on majority voter and latch circuit, for the wort case scenario.



Source: Author (2024).

For the latch circuit, there would only be one memristor and one transmission gate in the $Read$ path, if not for the $R1$ and $R2$ resistances, as shown in Figure 33. These resistances are used to ensure that the $Read$ action is non-destructive, and must be dimensioned accordingly. Following Equation 23, the restriction for the latch is represented in Equation 25, where R_{eq} is the equivalent resistance of the series association between $R1$ and R_{TG_1}.

$$V_{DD} \cdot \frac{R_{ON}}{R_{eq} + R_{ON}} < |V_{OFF}| \tag{25}$$

5 RESULTS

This chapter will address the results obtained during the development of this work. The first section describes the experimental setup, and the second section presents the simulation results. Finally, the third section of this chapter discusses the limitations of the implemented solution and potential improvements to the project.

5.1 Setup Experiments

The functioning of the developed solution was proven through simulation experiments. All simulations were carried out using Cadence's Virtuoso tool, in the Analog Design Environment, using the Schematic Editing option. The simulations performed were transient, with stop time of $8s$, step time of $8ms$ and maximum step time of $80ms$. All the other simulation parameters were kept as default.

For the circuits implementation in Virtuoso, the majority of the utilized transistors maintained the default parameter $w = 2\mu m$. For complementary circuits, such as inverters, the compensation of W for the PMOS transistors, discussed in Section 2.1 was considered. The transistors that had its parameters changed are mentioned during the presentation of the results, in Section 5.2.

The supply voltage used as V_{DD} in the simulations was a DC voltage source. For the control signal and the inputs, pulse sources that generate rectangular pulses were used. The rise and fall time configured for this sources was $t_{rise} = t_{fall} = 1ms$. The period of waveform and the pulse width were configured according to the characterization of each signal.

5.2 Simulation Results

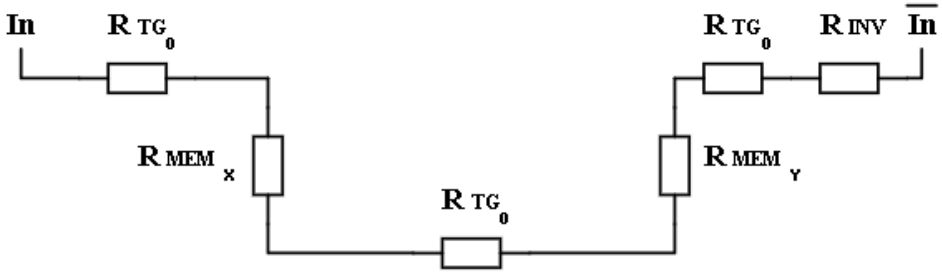
The first experiment aimed to verify the correct operation of the majority voter. For this, the circuit discussed in Chapter 4 and shown in Figure 25 was implemented in Virtuoso. Initially, all the memristor and transistor parameters were set to their default values, and the circuit was powered with $1.8V$. The results showed that this voltage level was insufficient to switch the memristors between their two resistance states.

To solve this problem, the path of each writing branch of the voting circuit was analyzed. The resistances of the memristors, the transmission gates, and the inverter were taken into account, as illustrated in Figure 34. Since, for the worse case scenario, each branch contains two memristors with complementary values, the combined voltage drop across these components will always be $1.5V$, as shown in Equation 26. With a supply voltage of $1.8V$, the remaining voltage drop to be distributed across the three transmission

gates and the inverter resistance was only $0.3V$, which was insufficient. Consequently, the supply voltage was increased to $2.2V$ to ensure proper operation.

$$V_{MEM_{\overline{W}}} = V_{MEM_X} - V_{MEM_Y} = V_{OFF} - V_{ON} = 0.90 - (-0.60) = 1.5V \tag{26}$$

Figure 34: Write path resistances.



Source: Author (2024).

Another point to consider was the current flowing through the transmission gates. The length (L) was kept as configured in the technology library at $180nm$. The width (W) of the TG_1 transistors was also kept at the value configured in the library, which is $2\mu m$ for NMOS and $4\mu m$, maintaining the $2:1$ ratio described in Section 2.1. However, since the transistors of TG_0 need to drive a greater current, their width was adjusted, as shown in Table 12.

Table 12: Transmission gates trnsistors width.

Transistor	W	
	TG_0	TG_1
NMOS	11μ m	2 μ m
PMOS	22μ m	4 μ m

With the supply voltage defined and the transmission gates sized, it is possible to use the constraint sizing Equations 22 and 24 to verify if the chosen values follow these constraints. For this purpose, the resultant resistances of the transmission gates were obtained via simulation, and their values are presented in Table 13. Substituting these values into the constraint equations, it is possible to derive the relation shown in Equation 27.

Table 13: Transmission gates resistances.

Parameter	Value
R_{TG_0}	120 Ω
R_{TG_1}	940 Ω

$$0.68V < |V_{OFF}| \leq 0.99V \tag{27}$$

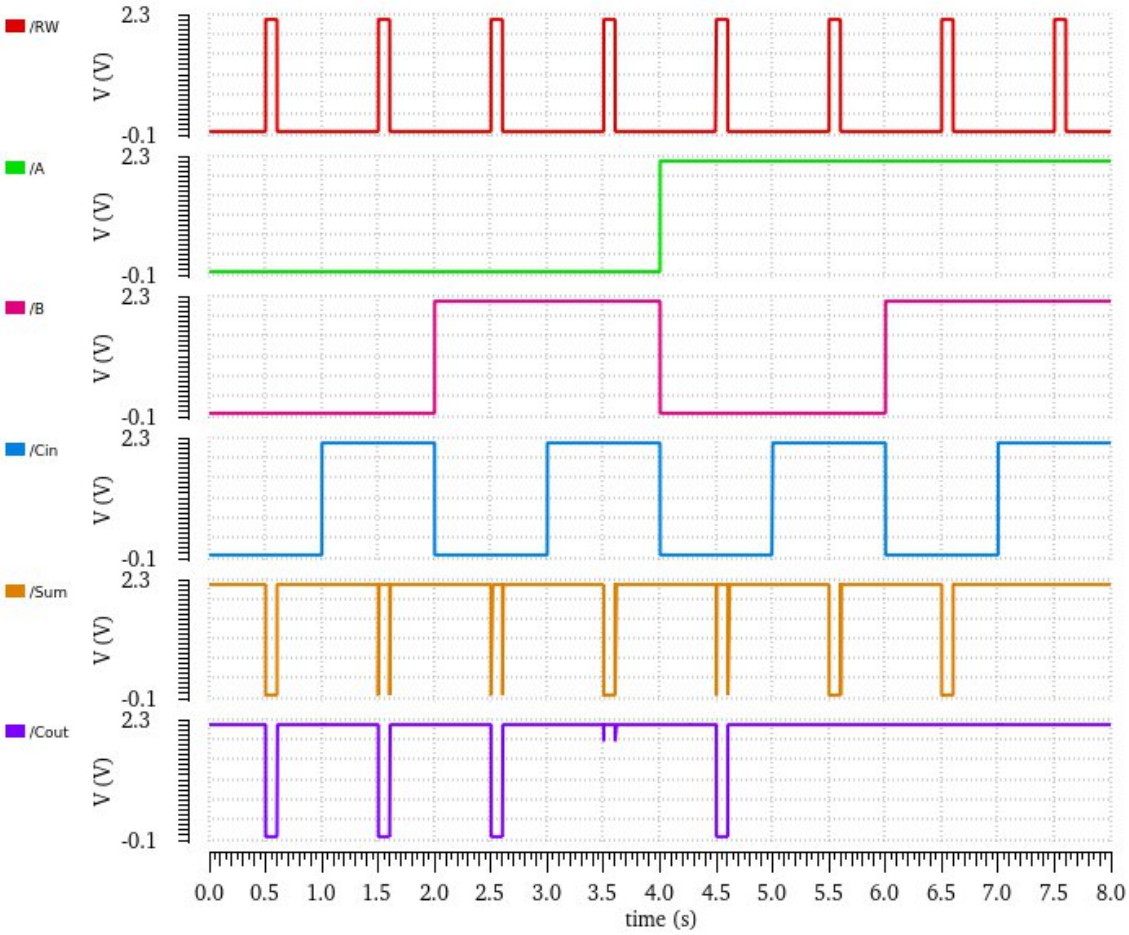
$$V_{DD} = V_{HIGH} = 1.8V \tag{28}$$

$$V_{DD} = V_{HIGH} = 2.2V \tag{29}$$

$$V_{LOW} = 0V \tag{30}$$

In the full adder simulation, all combinations of input signals were analyzed under different control signal commands. Figure 35 illustrates the temporal behavior of the circuit concerning the signals applied at the inputs.

Figure 35: Transient simulation results of the fully non-volatile full adder.



Source: Author (2024).

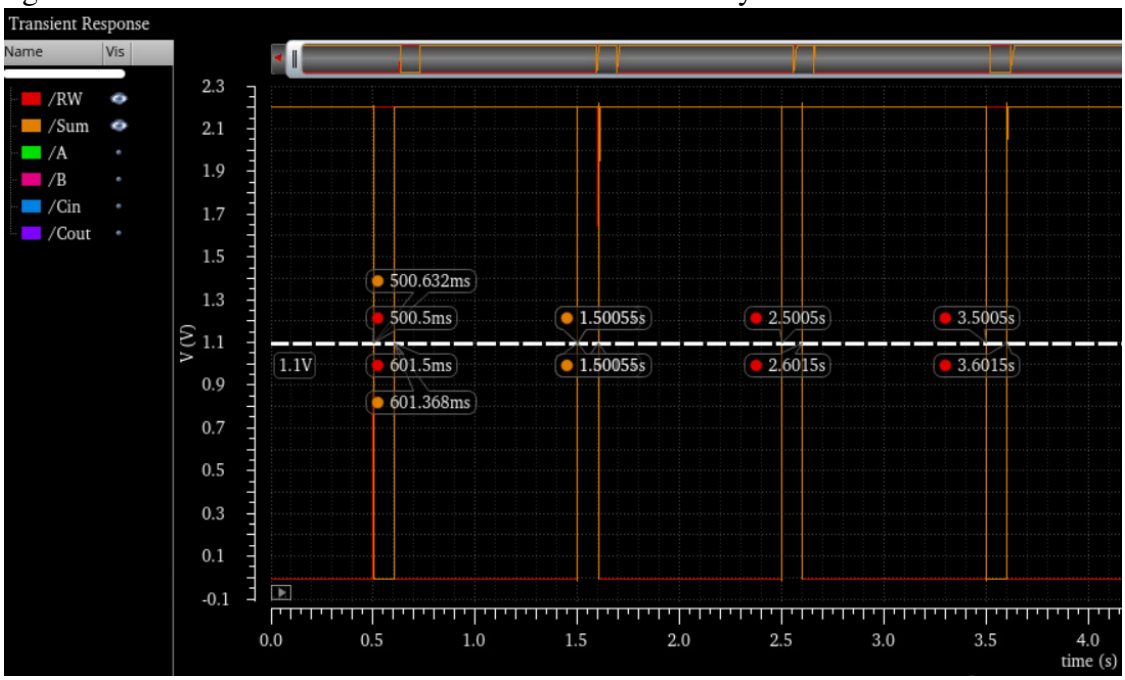
Based on the output signals obtained, it is evident that the circuit operates as expected. While the control signal $R/\overline{W}$ remains at a low logic level, the writing process occurs, the memristors switch states, and the output signals are maintained at a high logic level. When the control signal transitions to a high logic level, the sum result can be read, and this specific time period is observable in the graphs at times $0.5s$, $1.5s$, $2.5s$, and so on. By comparing the output signals Sum and $Cout$ shown in Figure 35 with the truth table of the full adder, presented in Table 7, it becomes clear that the circuit correctly performs the addition operation for all combinations of A, B, and Cin.

By observing the Sum signal in Figure 35, it is possible to notice transient voltage fluctuations (voltage spikes) in the output signal waveform. These fluctuations are caused by the simultaneous switching of the transmission gates but do not affect the logical operation of the circuit. As expected, the data is stored as resistance states in the memristors,

and once the write operation is complete, the circuit can retain its state without requiring continuous power. Therefore, the circuit has no static power consumption.

The circuit delay was measured considering the $R/\overline{W}$ signal switching from '0' to '1'. The time interval between the instant when $R/\overline{W}$ reaches 50% of its maximum value and the instant when the Sum signal reaches 50% was measured via simulation, as shown in Figure 36. The obtained value was $132\mu s$.

Figure 36: Transient simulation to measure the circuit delay of the non-volatile full adder.



Source: Author (2024).

In total, 116 transistors were used to compose the full adder circuit: 59 NMOS and 57 PMOS. Only 10 NMOS and 10 PMOS transistors had their widths increased (one pair for each TG_0 used).

5.3 Limitations and Improvements

A point to consider is the supply voltage used in relation to the chosen transistor technology. As discussed in Section 4.2, the selected transistors are rated for $1.8V$ with a maximum voltage of $1.98V$, but the supply voltage used in the simulations was $2.2V$. This voltage was chosen because of the voltage drop required in the memristor to enable it to switch resistances, as discussed in the previous section. Considering the positive results obtained, the time required for circuit design and implementation in the simulation tool, and the familiarity already acquired with this transistor technology, the decision was made to retain its use in the project.

As this is a simulation-based work that does not encompass any type of physical implementation, and since the main objective was to demonstrate that the circuit functions correctly while focusing on the properties introduced by memristors, this choice does not have a significant impact on this study. However, it is extremely important that, in projects intended for physical implementation, the tests conducted simulate real-world conditions as closely as possible. In such cases, an improvement to this project would involve re-

sizing the transistors used and making the necessary adjustments to the supply voltage to ensure the circuit operates correctly.

In physical implementations, using a voltage greater than the maximum recommended for a MOSFET transistor can cause issues, such as excessive heating, increased leakage current, accelerated degradation of the semiconductor material, channel deformation, damage to the oxide insulation, and, in extreme cases, electrical breakdown (TAKEDA; YANG; MIURA-HAMADA, 1995). These problems can degrade the performance, efficiency, and lifespan of the transistor, potentially leading to irreversible failure of the component. For these applications, it is essential to ensure that the applied voltage stays within the limits specified by the manufacturer to prevent damage to the transistor and ensure proper circuit operation.

Furthermore, increasing the width of the transistors in the transmission gates could directly impact the area occupied by the circuit. Therefore, employing other CMOS transistor technologies could help reduce the occupied area. Additionally, another possibility is to explore different memristor models that require lower currents.

6 CONCLUSION AND FINAL CONSIDERATIONS

Considering the increasing interest in memristor-related research and the potential of these devices to drive advancements in electronics, particularly in integrated circuits, this work aimed to design a circuit utilizing memristors. The circuit developed was a fully non-volatile full adder with a hybrid CMOS/memristor architecture. The core of the circuit is a non-volatile majority voter that directly produces the carry-out output of the adder. To generate the sum output, a magnitude comparator is used to control a latch, which, in turn, drives a multiplexer that selects either the voter's output or its logical complement.

Adders are among the most commonly used components in arithmetic logic units (ALUs) in processors and microcontrollers. Currently, there is an increasing demand for higher processing performance, as well as a push for low power consumption alternatives. In this sense, the solution implemented in this work presents an alternative in terms of power consumption, as the circuit is non-volatile and does not exhibit static power consumption.

Additionally, demonstrating the operation of a circuit with memristors using a real model represents a significant advancement in approaches involving this type of device. A future step would be to perform the layout and physical implementation of this circuit, conducting tests and performance evaluations. This would allow for the assessment of the actual area occupied by the circuit and enable a comparison of this solution with others available in the academic field.

Based on the simulations performed, it was possible to verify that the circuit operates as expected. Some voltage spikes were observed in the sum output signal, which are due to the simultaneous switching of the transmission gates. Therefore, for future work, it would be interesting to evaluate the use of two control signals to avoid this simultaneous switching.

REFERENCES

ACD. **Analog Circuit Design - Transmission gates**. 2024.

ALI, S. et al. Memristor Fabrication Through Printing Technologies: a review. **IEEE Access**, [S.l.], v.9, p.95970–95985, 2021.

BENGEL, C. et al. **EMRL - JART VCM v1 Verilog-A Compact Model**: user guide. Online. Available at: <https://www.emrl.de/JART.html#Artikel_3>. Last accessed 15 Nov. 2024.

BORKAR, S. Design challenges of technology scaling. **IEEE Micro**, [S.l.], v.19, n.4, p.23–29, 1999.

CARTER, D. E. Oxidation-Reduction Reactions of Metal Ions. **Environmental Health Perspectives**, [S.l.], v.103, n.1, p.17–19, 1995.

CHUA, L. O. Memeristor - The Missing Circuit Element. **IEEE Transactions on Circuit Theory**, [S.l.], v.18, n.5, p.507–519, 1971.

CHUA, L. O.; KANG, S. M. Building Memristor Applications: from device model to circuit design. **Proceedings of the IEEE**, [S.l.], v.64, n.2, p.209–223, 1976.

DANIEL, R. Limits of CMOS technology scaling and technologies beyond-CMOS. **Unpublished, IEEE Inc.**, [S.l.], 2005.

GARCíA-REDONDO, F.; LóPEZ-VALLEJO, M.; ITUERO, P. Building Memristor Applications: from device model to circuit design. **IEEE Transactions on Nanotechnology**, [S.l.], v.13, n.6, p.1154–1162, 2014.

HARDTDEGEN, A. et al. Improved switching stability and the effect of an internal series resistor in HfO_2/TiO_x bilayer ReRAM cells. **IEEE transactions on electron devices**, [S.l.], v.65, n.8, p.3229–3236, 2018.

HARRIS, D.; HARRIS, S. **Digital Design and Computer Architecture**. [S.l.]: Morgan Kaufmann, 2016.

HAUPT, A.; P. DACHI Édison. **Eletrônica digital**. [S.l.]: Blucher, 2016.

ISAH, A.; BILBAULT, J.-M. Review on the Basic Circuit Elements and Memristor Interpretation: analysis, technology and applications. **Journal of Low Power Electronics and Applications**, [S.l.], v.12, n.3, p.44, 2022.

MANJUNATH, K. M. et al. Analysis of various full-adder circuits in cadence. **International Conference on Emerging Research in Electronics, Computer Science and Technology**, [S.l.], p.90–97, 2015.

PI, S. et al. Device Engineering and CMOS Integration of Nanoscale Memristors. **IEEE International Symposium on Circuits and Systems (ISCAS)**, [S.l.], p.425–427, 2014.

RABAEY, J. M.; ANANTHA, C.; BORIVOJE, N. **Digital integrated circuits**: a design perspective. [S.l.]: Pearson, 2003.

ROSE, G. S. et al. Leveraging Memristive Systems in the Construction of Digital Logic Circuits. **Proceedings of the IEEE**, [S.l.], v.100, n.6, p.2023–2049, 2012.

SEDRA, A. S. et al. **Circuitos Microeletrônicos**. [S.l.]: LTC, 2023.

SLIMANI, M. et al. Reliability analysis of hybrid spin transfer torque magnetic tunnel junction/CMOS majority voters. **Microelectronics Reliability**, [S.l.], v.64, p.48–53, 2016.

STRUKOV, D. B. et al. The missing memristor found. **nature**, [S.l.], v.453, n.7191, p.80–83, 2008.

TAKEDA, E.; YANG, C. Y.; MIURA-HAMADA, A. **Hot-carrier effects in MOS devices**. [S.l.]: Academic Press, 1995.

VERMA, S.; PAUL, R.; SHUKLA, M. Non-Volatile Latch Compatible With Static and Dynamic CMOS for Logic in Memory Applications. **IEEE Transactions on Magnetics**, [S.l.], v.58, n.4, p.1–8, 2022.

VLASOV, A. I. et al. Market for memristors and data mining memory structures for promising smart systems. **Entrepreneurship and sustainability issues**, [S.l.], v.8, n.2, p.98, 2020.

VOURKAS, I.; SIRAKOULIS, G. C. Emerging Memristor-Based Logic Circuit Design Approaches: a review. **IEEE Circuits and Systems Magazine**, [S.l.], v.16, p.15–30, 2016.

WASER, R. Redox-based resistive switching memories. **Journal of nanoscience and nanotechnology**, [S.l.], v.12, n.10, p.7628–7640, 2012.

WASER, R. **EMRL - Electronic Materials Research Laboratory**. Online. Available at: <https://www.emrl.de/. Last accessed 17 Nov. 2024.

ZHAO, W. et al. High Speed, High Stability and Low Power Sensing Amplifier for MTJ/CMOS Hybrid Logic Circuits. **IEEE Transactions on Magnetics**, [S.l.], v.45, p.3784–3787, 2009.