Probabilistic Approach for Yield Analysis of Dynamic Logic Circuits

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***Abstract*—In deep-submicrometer technologies, process variability challenges the design of high yield integrated circuits. While device critical dimensions and threshold voltage shrink, leakage currents drastically increase, threatening the feasibility of reliable dynamic logic gates. Electrical level statistical characterization of this kind of gates is essential for yield analysis of the entire die. This work proposes a yield model for dynamic logic gates based on error propagation using numerical methods. We study delay and contention time in the presence of process variability. The methodology is employed for yield analysis of two typical wide-NOR circuits: one with a static keeper and another without the keeper. Since we use a general numerical approach for the calculation of derivatives and error propagation, the proposed yield analysis methodology may be applied to a wide range of dynamic gates (for instance pre-charge dynamic gates using dynamic keeper). The proposed methodology results in errors less than 2% when compared to Monte Carlo simulation, while increasing computational efficiency up to 100×.**

***Index Terms*—Design for yield, Monte Carlo methods, probabilistic analysis, process variability, VLSI, yield estimation.**

I. Introduction

PERFORMANCE and reliability of deep-submicrometer technologies are being increasingly affected by process variations and leakage current [1]. These variations are statistical in nature, and predicting the percentage of manufactured circuits that will achieve a given performance becomes a major problem for the circuit designer. Therefore, the use of statistical methods in circuit design assumes great relevance. When considering electric level simulations, the statistical characterization of circuits must be related to the microscopic features that cause device performance variability and affect circuit yield.

Electrical parameters variability may be decomposed into parameters that present spatial correlation (SC) and parameters that do not present spatial correlation (NSC) [2], [3]. NSC parameter variability may originate from different sources, for instance the discreteness of matter and energy (dopant atoms, photo resist molecules, and photons). A well known example of NSC parameter is threshold voltage (Vt) variability due to the random Dopant fluctuations (RDFs) [4]. RDF are mainly caused by the irregular distribution of doping atoms above the channel, and this effect nowadays represents one of the greatest challenges for the industry [5]. Consider σ_{vt0}, the standard deviation in threshold voltage for minimum-sized transistors. The dependence of σ_{vt} on transistor size is given by [6]

$$\sigma_{vt} = \sigma_{vt0}\sqrt{\frac{L_{\min} \times W_{\min}}{L \times W}} \tag{1}$$

where L is the channel length and W is the channel width. $L_{\min}$ and $W_{\min}$ refer to the minimum geometries of these dimensions.

The spatially correlated parameters can be subdivided into an inter-die systematic component and an intradie systematic component. Inter-die systematic variation may originate from equipment asymmetries (such as asymmetries in chamber gas flows, thermal gradients and so on) or imperfections in equipment operation and process flow. These asymmetries and imperfections affect the mean value of a parameter from die to die, wafer to wafer and lot to lot. Intradie systematic variations are due to pattern or layout induced deviation of a parameter from its nominal value. Parameters such as oxide thickness, transistor channel length and channel width may show systematic variations [7]. In the case of a SC parameter k, transistors close to each other are affected by the same constant fluctuation δk.

Typical topology for a dynamic gate consists of a pull-down network implementing the Boolean function and one single pMOS transistor connected to $V_{\rm DD}$. Fig. 1 shows the schematic of a typical dynamic wide-NOR gate with N inputs. The gate of the pMOS transistor is connected to the clock signal ϕ. According to the state of ϕ, the dynamic gate has 2 phases: pre-charge and evaluation. When $\phi = 0$ V, the gate is in pre-charge phase, and the dynamic output is charged to $V_{\rm DD}$. By definition, in this phase there is no path from the dynamic output to GND. After the pre-charge phase, ϕ is switched to

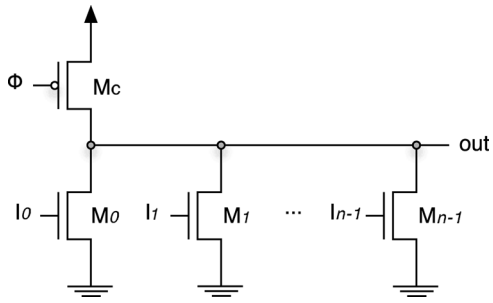

Fig. 1. Dynamic NOR.

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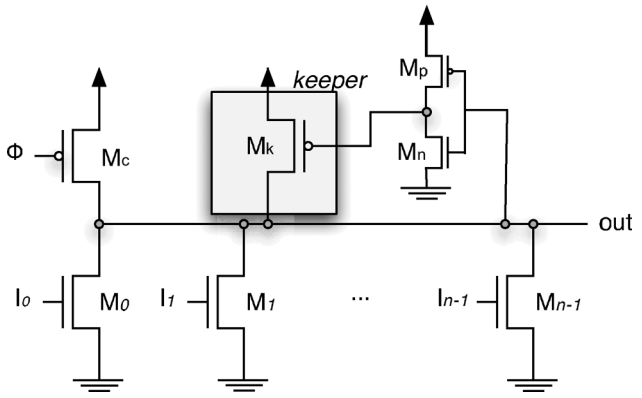

Fig. 2. Dynamic NOR with keeper.

$V_{\rm DD}$, and the gate is in the evaluation phase. During the evaluation phase, if the inputs are such that the computed output is logical one, the dynamic output is maintained at $V_{\rm DD}$, and in this case there is no power consumption. Otherwise, the output node is discharged to GND.

MOSFET subthreshold leakage currents are increasing exponentially across successive technology generations, due to threshold voltage and channel length reduction [8]. Furthermore, with decreasing device dimensions and supply voltages, the amount of charge at the circuit nodes used to store information reduces. In addition, measures in [9] indicate that the spread in the leakage current ($[\mu_{I\rm off} - 3\sigma_{I\rm off}, \mu_{I\rm off} + 3\sigma_{I\rm off}]$) can be up to 20× in a recent technology node. These effects impact negatively the robustness and feasibility of wide (high fan-in) domino logic gates [10]. High fan-in dynamic logic gates often lead to fewer logic levels, resulting in compact circuits with better performance and lower power consumption, when compared to their counterparts in static logic. These wide gates have been used extensively in the design of the access circuitry of memory elements and in the control and arithmetic units of high-performancee processors [11].

In order to increase the circuit noise margin (reducing sensitivity to leakage current, charge sharing effect and coupling noise), pre-charge dynamic gates can be designed using the traditional static keeper [12], as shown in Fig. 2. This circuit is composed of the dynamic NOR of Fig. 1, a static inverter and a static keeper transistor. If the output is at $V_{\rm DD}$, the keeper provides a path from the power supply to the output preventing the output to be discharged by leakage currents. Although, as the keeper transistor drives a contention current to the output node while output contains $V_{\rm DD}$, this approach implies a significant performance penalty when an input signal switches.

When a transition occurs, the keeper and pull-down network transistors compete to determine the logical state of the dynamic node. The time delay of a transition is inversely proportional to the keeper transistor size, while the noise margin is directly proportional to it. In the last few years, dynamic keeper technique emerged as an important research area. Kursun [13] proposes a technique where a body-bias generator dynamically varies the threshold voltage of keeper transistor, reducing contention current in the evaluation phase. In [10] a design is presented where the keeper is turned on only if after a given time $T_{\rm MAX}$ there is no transition on the dynamic output. Circuit proposed in [14] consists of a 3-bit programmable keeper, where a set of fuses is set during the test phase of the chip. Although recent researches in this area point to self-adaptive dynamic keeper techniques, static keeper is still an industry-standard and largely employed.

At gate level, statistical static timing analysis (SSTA) provides quantitative risk management for the design as a function of circuit parameters, topology and gate variability [15]. In order to obtain both delay average and delay variance using SSTA, logic gates must be statistically characterized at electrical level. The present methodology is an alternative to Monte Carlo simulation when computing statistical response of logic gates at electric level. This methodology provides accuracy equivalent to Monte Carlo while reducing running time. Furthermore, the methodology presents as advantage over Monte Carlo the capability to compute the variance sensitivity to each random variable, leading to further yield optimization.

In this work, we propose a probabilistic model to compute yield of a pre-charge dynamic gate. The methodology presented in this paper is intended to be generic enough to model response (e.g., delay, contention time, power and leakage) variability of any kind of pre-charge circuits, including circuits employing dynamic keeper. The proposed methodology shows this potential for wide applicability because we employ numerical techniques based on electric simulation for the computation of variance.

This paper is organized as follows. Section II exposes the theoretical foundations of error propagation and numerical derivatives for computing yield of logic gates. Section III presents the methodology applied to the problem of computing statistical delay and contention time of dynamic gates—with and without the static keeper. Next, Section IV presents results obtained with the proposed method, which is compared to Monte Carlo on both accuracy and performance. Finally, our conclusions are provided in Section V.

II. Yield Analysis Methodology

Consider an electric circuit denoted by ω, composed by n transistors represented as components of the vector $\overrightarrow{\tau} = (\tau_1, \ldots, \tau_n)$, interconnected according to a topology Γ. By definition, the circuit response is given by the function $F(\overrightarrow{\alpha}_1, \ldots, \overrightarrow{\alpha}_n, \overrightarrow{\beta}_1, \ldots, \overrightarrow{\beta}_n, \omega)$, where the vectors $\overrightarrow{\alpha}_i = (\alpha_i^{(1)}, \ldots, \alpha_i^{(p)})$ and $\overrightarrow{\beta}_i = (\beta_i^{(1)}, \ldots, \beta_i^{(q)})$ represent, respectively, the NSC and SC parameters of transistor i, p is the number of NSC parameters and q the number of SC parameters. For instance, the case $\overrightarrow{\alpha}_3 = (V_t)$ and $\overrightarrow{\beta}_3 = (T_{\rm ox}, L, W)$ represents typical input parameters for transistor τ_3, including oxide thickness $(T_{\rm ox})$, threshold voltage (V_t) and dimensions (L and W) of the transistor.

In the presence of variability in the fabrication process, electrical characteristics and physical dimensions of the circuit can be considered random variables and consequently the output is a random variable. Consider, without loss of generality, that parameters (for instance, $T_{\rm ox}$, V_t, L, W) are Gaussian variables with mean (μ) and variance (σ^2), i.e, $\alpha_i^{k_1} = N(\mu(\alpha_i^{k_1}), \sigma^2(\alpha^{k_1}))$ and $\beta_i^{k_2} = N(\mu(\beta_i^{k_2}), \sigma^2(\beta^{k_2}))$, where $i = 1, \ldots, n$, $k_1 = 1, \ldots, p$ and $k_2 = 1, \ldots, q$.

The circuit statistical response S is a function that depends on $N = n \times (p+q)$ random variables (including NSC and SC parameters), given by the functional relation

$$S = F(\overrightarrow{\alpha}_1, \ldots, \overrightarrow{\alpha}_n, \overrightarrow{\beta}_1, \ldots, \overrightarrow{\beta}_n, \omega). \quad (2)$$

A. SC and NSC Random Variables

In order to model the impact of process variations on the electric circuit response, SC and NSC are treated differently. By definition, for a SC parameter, exactly the same fluctuation affects all nearby transistors, although their absolute value can be different because they can have distinct average values.

Other random variables are modeled as Gaussian random variables, which are denoted in this work as NSC parameters. A NSC variable assumes a random value for each transistor, although it can be subject to covariance coefficients (σ_{ij}).

Notice that both SC and NSC parameters are random variables. The difference between them is the randomness context: each instance of a NSC variable assumes a different random value, while a SC parameter has a single random increment for a set of devices.

1) SC Parameters: Spatial correlation impels the SC electrical parameter of all transistors to change in a synchronized way. For instance, if the dimension W is assumed to present SC variations and W_1 of transistor τ_1 changes by a quantity δW, the dimension W_2 of a transistor τ_2 changes by the same quantity δW although their mean ($\mu(W_1)$ and $\mu(W_2)$) in the standard sampling process can be different. The parameter W is then defined as a variable that presents:

1) exactly the same variation δW inside an single electrical block;
2) but different variation in different electrical blocks, for instanced variation δW_1 in block 1 and variation δW_2 in block 2.

Parameters that present SC variations can be modeled as

$$\beta_i^j = \mu\left(\beta_i^j\right) + \xi_j \cdot \sigma(\beta^j)$$

where $\xi_j = N(0,1)$ is a standard normal variable which is independent of the transistor $1 \le i \le n$. It means that the same variable j will have the same shift of magnitude $\xi_j \cdot \sigma(\beta^j)$ independent of the transistor to which it is applied. In other words, the variables $\beta_1^j, \ldots, \beta_n^j$ are the same random variable except by their mean values. Looking at the contribution of this variables for error estimation, it is important to define the general variable $\beta^j = \mu(\beta^j) + \xi_j \cdot \sigma(\beta^j)$, where $\mu(\beta^j)$ is a transistor-independent constant. Then it can be written as

$$\beta_i^j(k) = \mu\left(\beta_i^j\right) + \xi_j \cdot \sigma(\beta^j) = \mu\left(\beta_i^j\right) + \beta^j - \mu(\beta^j) \quad (3)$$

which leads to suitable simplification $F(\overrightarrow{\alpha}_1, \ldots, \overrightarrow{\alpha}_n, \overrightarrow{\beta}_1, \ldots, \overrightarrow{\beta}_n, \omega) = F(\overrightarrow{\alpha}_1, \ldots, \overrightarrow{\alpha}_n, \beta^1, \ldots, \beta^q, \omega)$ and using the chain rule the computation of partial derivatives becomes

$$\frac{\partial F}{\partial \beta^j} = \sum_{i=1}^{n} \frac{\partial F}{\partial \beta_i^j} \frac{\partial \beta_i^j}{\partial \beta^j} = \sum_{i=1}^{n} \frac{\partial F}{\partial \beta_i^j} \quad (4)$$

because according to (3) it is true that $\partial \beta_i^j / \partial \beta^j = 1$, for all $i \in \{1, \ldots, n\}$.

B. Error Propagation

A frequent question when working on data analysis is how to estimate the uncertainty of a quantity which is function of many variables whose uncertainties are known. The classical error propagation formula [16] provides means to compute such uncertainty estimate. When computing uncertainty of logic gates electrical characteristics (delay, leakage, etc.) as modeled on (2), the variance in S can be computed as follows:

$$\begin{aligned}
\sigma_S^2 = & \sum_{i=1}^{n}\sum_{j=1}^{p} \left(\left.\frac{\partial F}{\partial \alpha_i^j}\right|_{\alpha_i^j = \mu\left(\alpha_i^j\right)} \right)^2 \sigma^2(\alpha^j) \\
& + \sum_{j=1}^{q} \left(\sum_{i=1}^{n} \left.\frac{\partial F}{\partial \beta_i^j}\right|_{\beta_i^j = \mu\left(\beta_i^j\right)} \right)^2 \sigma^2(\beta^j) \\
& + 2\sum_{i=1}^{n}\sum_{j=1}^{p}\sum_{k=j}^{p} \left(\left.\frac{\partial F}{\partial \alpha_i^j}\right|_{\alpha_i^j = \mu\left(\alpha_i^j\right)} \left.\frac{\partial F}{\partial \alpha_i^k}\right|_{\alpha_i^k = \mu\left(\alpha_i^k\right)} \right) \\
& \times \sigma(\alpha^j, \alpha^k) \\
& + 2\sum_{i=1}^{n}\sum_{j=1}^{q}\sum_{k=j}^{q} \left(\left.\frac{\partial F}{\partial \beta_i^j}\right|_{\beta_i^j = \mu\left(\beta_i^j\right)} \left.\frac{\partial F}{\partial \beta_i^k}\right|_{\beta_i^k = \mu\left(\beta_i^k\right)} \right) \\
& \times \sigma(\beta^j, \beta^k) \\
& + 2\sum_{i=1}^{n}\sum_{j=1}^{p}\sum_{k=1}^{q} \left(\left.\frac{\partial F}{\partial \alpha_i^j}\right|_{\alpha_i^j = \mu\left(\alpha_i^j\right)} \left.\frac{\partial F}{\partial \beta_i^k}\right|_{\beta_i^k = \mu\left(\beta_i^k\right)} \right) \\
& \times \sigma(\alpha^j, \beta^k). \quad (5)
\end{aligned}$$

For this particular case, the SC as given by (4) is assumed, as well as the hypothesis of $\{\alpha^j\}_{i=1}^{p}$, $\{\beta^j\}_{j=1}^{q}$ being random Gaussian variables deriving from systematic and statistical sources. Gaussian parameters is widely accepted [17] for such circuits.

The reader should notice that covariances between electrical parameters do not imply overhead in the number of simulations. Nonbiased sampling estimator to the standard deviation computed from a sample of n_{sample} experimental measures of S, denoted as $S_1, S_2, \ldots, S_{nsample}$, is calculated by the expression $\delta_S = (\sum_{i=1}^{n_{\text{sample}}} (S_i - \langle S_i \rangle)^2)/(n_{\text{sample}} - 1)$ and we expect $\delta_S \approx \sigma_S$ for a n_{sample} sufficiently large, where $\langle S_i \rangle = (1/n_{\text{sample}}) \sum_{i=1}^{n_{\text{sample}}} S_i$.

Such statistical estimates of electric characteristics of digital and analog circuits are often obtained by Monte Carlo simulations [18] considering a large sample of simulations at electric level [19]. In this case one needs a suitable number of runs to obtain reasonable approximation for variance and error estimates (confidence intervals, relative errors), once this error is nonrigorously estimated by $O(1/\sqrt{n_{\text{sample}}})$.

The error propagation (EP) method is a suitable way to compute variance of an electrical response avoiding the huge number of simulations required by sampling techniques once

it works by computing the variance having as input: standard deviation of random parameters, correlation between random parameters and the sensitivities of the circuit response to the random parameters. Standard deviations and correlation coefficients are technology dependent and are given by the foundry. Sensitivities can be computed numerically as suggested in Section II-C.

C. Numerical Derivatives

Suppose $f(k_1,\ldots,k_N)$ is an arbitrary function which can be computed by electrical simulation, the numerical estimates for derivatives $(\partial f/\partial k_i)|_{k_i=\overline{k_i}}$ also can be computed by electrical simulation. From these derivatives, the variability at the output can be computed.

In order to present a generic methodology independent of circuit topology, sensitivities are computed numerically. Thus, one can calculate the sensitivity at point $f(\overline{k_1},\ldots,\overline{k_i}+\varepsilon,\ldots,\overline{k_N})$ using an $O(\varepsilon)$ approximation

$$\frac{\partial f}{\partial k_i}(\overline{k_1},\ldots,\overline{k_i},\ldots,\overline{k_N}) = \frac{f(\overline{k_1},\ldots,\overline{k_i}+\varepsilon,\ldots,\overline{k_N})-f(\overline{k_1},\ldots,\overline{k_i},\ldots,\overline{k_N})}{\varepsilon}+O(\epsilon). \tag{6}$$

In order to obtain a more precise approximation, algebraic manipulations over Taylor expansion results in a formula with accuracy $O(\varepsilon^2)$. Consider Taylor expansions around the points $f(\overline{k_1},\ldots,\overline{k_i}+\varepsilon,\ldots,\overline{k_N})$ and $f(\overline{k_1},\ldots,\overline{k_i}-\varepsilon,\ldots,\overline{k_N})$, and a better approximation for $(\partial/\partial k_i)f(\overline{k_1},\ldots,\overline{k_i},\ldots,\overline{k_N})$ can be computed according to

$$\frac{\partial}{\partial k_i}f(\overline{k_1},\ldots,\overline{k_N}) = \frac{f(\overline{k_1},\ldots,\overline{k_i}+\varepsilon,\ldots,\overline{k_N})-f(\overline{k_1},\ldots,\overline{k_i}-\epsilon,\ldots,\overline{k_N})}{2\varepsilon} + O(\varepsilon^2). \tag{7}$$

For the first case, two electrical simulations are required to compute each partial derivative: one is required to compute $F(\overline{k_1},\ldots,\overline{k_i}+\varepsilon,\ldots,\overline{k_N})$ and another one for $F(\overline{k_1},\ldots,\overline{k_i},\ldots\overline{k_N})$. However, as $F(\overline{k_1},\ldots,\overline{k_i},\ldots\overline{k_N})$ is the same for all partial derivatives, it is computed only once. Thus, computation of all partial derivatives using first order approximation requires $N+1$ runs. Similarly in the second case we can conclude that $2N$ runs are required.

D. Sensitivity of the Variance to the Electrical Parameters

When dealing with the challenges imposed by design for manufacturability, it is essential to have a methodology capable of identify which parameters contribute most to the circuit variability. Error propagation is a good solution for variability analysis at electrical level because by using it one can compute the quantitative contribution of each parameter to the circuit variance. This information points out what parts of the circuit may be redesigned in order to optimize yield.

Error propagation uncovers the quantitative contribution of each transistor to the variability in circuit performance. Revisiting (5), the sensitivity of the circuit response variance to a within-die parameter α^k is given by

$$K(\alpha^k)=\left(\frac{\partial F}{\partial \alpha^k}\right)^2\sigma^2_{\alpha^k}. \tag{8}$$

For SC components, a re-weighted function can be defined as

$$p_{ik}=\left(\frac{\left|\partial F/\partial \beta_i^k\right|}{\sum_{j=1}^{m}\left|\partial F/\partial \beta_j^k\right|}\right) \tag{9}$$

where $\sum_{i=1}^{m} p_{ik}=1$ for m synchronized variables. For a parameter β_i^k that presents SC variation the sensitivity is given by

$$K\left(\beta_i^k\right)=p_{ik}\times\left(\frac{\partial F}{\partial \beta^k}^2\sigma^2_{\beta^k}\right). \tag{10}$$

III. Dynamic Logic

The generic applicability of error propagation using numerical derivatives to the statistical analysis of logic gates was shown in the previous section. This section presents the framework to analyze:

1) delay variance of a pre-charge dynamic NOR with or without a static keeper;
2) contention current variability of dynamic-NOR without keeper.

A. Formulas for Delay Variance of the Dynamic Logic Circuit

In the case of a dynamic gate without keeper (see Fig. 1), we can write the delay as a function of the parameters associated to the $(n+1)$ transistors labeled Mc and $\{Mi\}_{i=0}^{n-1}$. The threshold voltages are represented by Vt_{Mc} and $\{Vt_{Mi}\}_{i=0}^{n-1}$. Variability in the respective channel lengths of these transistors, e.g., L_{Mc} and $\{L_{Mi}\}_{i=0}^{n-1}$, is divided into two components: one SC and another NSC.

Here, it is important to notice that spatially correlated components, represented by L_{Mc}^{sc} and $\{L_{Mi}^{\text{sc}}\}_{i=0}^{n-1}$ are synchronized random Gaussian variables, such that

$$L_x^{\text{sc}}=\alpha_x\overline{L}+\xi\cdot\sigma \tag{11}$$

where x denotes the indexes Mc or Mi with $i=0,\ldots,n-1$. The α_x's and σ are constants while ξ is the standard normal variable $N(0,1)$. In other words, it means that these variables are the same random variables, even if they present different mean values. From that, defining $L^{\text{sc}}=\overline{L}+\xi\cdot\sigma$ we have $L_x^{\text{sc}}=(\alpha_x-1)\overline{L}+L^{\text{sc}}=\text{constant}+L^{\text{sc}}$.

The delay of the circuit is defined as the maximum time required to propagate a transition in the input to the output. At the beginning of evaluation phase ($\phi=1$) the dynamic output is V_{DD}, and every transition $0\rightarrow 1$ in at least one input will cause a transition $1\rightarrow 0$ at the output. It is important to notice that

all inputs are symmetric, i.e., for a n-input circuit, probability of the maximum delay to be given by the input i is $1/n$.

Consider, without loss of generality, a transition $000\ldots0 \rightarrow 100\ldots0$ at the dynamic gate input. In order to analyze the variability of a dynamic gate, first we have to study the mean value and standard deviation for the delay time of this transition. So, we can write the time delay to this transition as a function of the random variables of interest

$$t = t\left(L^{\mathrm{sc}}, L^{\mathrm{nsc}}_{Mc}, \{L^{\mathrm{nsc}}_{Mi}\}^{n-1}_{i=0}, Vt_{Mc}, \{Vt_{Mi}\}^{n-1}_{i=0}\right) \quad (12)$$

and the variance in t, using error propagation [16] taking into account circuit symmetry, is given by

$$\begin{aligned}\sigma_t^2 = &\left(\frac{\partial t}{\partial L^{\mathrm{sc}}}\right)^2 \sigma^2_{L^{\mathrm{sc}}} + \left(\frac{\partial t}{\partial L^{\mathrm{nsc}}_{Mc}}\right)^2 \sigma^2_{L^{\mathrm{nsc}}} \\ &+ \left(\frac{\partial t}{\partial Vt_{Mc}}\right)^2 \sigma^2_{Vt} + \left(\frac{\partial t}{\partial L^{\mathrm{nsc}}_{M0}}\right)^2 \sigma^2_{L^{\mathrm{nsc}}} \\ &+ \left(\frac{\partial t}{\partial Vt_{M0}}\right)^2 \sigma^2_{Vt}. + (n-1)\left(\frac{\partial t}{\partial L^{\mathrm{nsc}}_{M1}}\right)^2 \sigma^2_{L^{\mathrm{nsc}}} \\ &+ (n-1)\left(\frac{\partial t}{\partial Vt_{M1}}\right)^2 \sigma^2_{Vt}. \end{aligned} \quad (13)$$

On the other hand, applying the chain rule, we can conclude by synchronism of variables that $\partial t/\partial L^{\mathrm{sc}} = \partial t/\partial L^{\mathrm{sc}}_{Mc} + \sum_{i=0}^{n-1}(\partial t/\partial L^{\mathrm{sc}}_{Mi})$, provided that $\partial L^{\mathrm{sc}}_{Mc}/\partial L^{\mathrm{sc}} = \partial L^{\mathrm{sc}}_{Mi}/\partial L^{\mathrm{sc}} = 1$ for all $i = 0, \ldots, (n-1)$ what leads to

$$\begin{aligned}\sigma_t^2 = &\left(\frac{\partial t}{\partial L^{\mathrm{sc}}_{Mc}} + \frac{\partial t}{\partial L^{\mathrm{sc}}_{M0}} + (n-1)\frac{\partial t}{\partial L^{\mathrm{sc}}_{M1}}\right)^2 \sigma^2_{L^{\mathrm{sc}}} \\ &+ \left(\frac{\partial t}{\partial L^{\mathrm{nsc}}}\right)^2 \sigma^2_{L^{\mathrm{nsc}}} + \left(\frac{\partial t}{\partial Vt_{Mc}}\right)^2 \sigma^2_{Vt} \\ &+ \left(\frac{\partial t}{\partial L^{\mathrm{nsc}}_{M0}}\right)^2 \sigma^2_{L^{\mathrm{nsc}}} + \left(\frac{\partial t}{\partial Vt_{M0}}\right)^2 \sigma^2_{Vt}. \\ &+ (n-1)\left(\frac{\partial t}{\partial L^{\mathrm{nsc}}_{M1}}\right)^2 \sigma^2_{L^{\mathrm{nsc}}} \\ &+ (n-1)\left(\frac{\partial t}{\partial Vt_{M1}}\right)^2 \sigma^2_{Vt}. \end{aligned} \quad (14)$$

Then, evaluation of transition delay variance for a dynamic-NOR without keeper requires the computation of 9 partial derivatives. These derivatives can be numerically computed using an electrical simulator, according to formulations presented in the Section II-B. The automation tool for yield analysis generates the points where function t must be evaluated, and the electric simulator gives the responses of the circuit, which are employed in the computation of derivatives. Also, notice that the number of simulations is independent of the number of inputs because pull-down transistors are symmetric.

Introducing a keeper device in accordance to Fig. 2, we have three new transistors: Mp, Mn and Mk. Then, the delay from one input to the output can be written as

$$\begin{aligned}t = t\Big(&L^{\mathrm{sc}}, L^{\mathrm{nsc}}_{Mc}, L^{\mathrm{nsc}}_{Mp}, L^{\mathrm{nsc}}_{Mn}, L^{\mathrm{nsc}}_{Mk}, \{L^{\mathrm{nsc}}_{i}\}^{n-1}_{i=0}, \\ &Vt_{Mc}, Vt_{Mp}, Vt_{Mn}, Vt_{Mk}, \{Vt_{Mi}\}^{n-1}_{i=0}\Big). \end{aligned} \quad (15)$$

So in this case variance of time delay is given by

$$\begin{aligned}\sigma_t^2 = &\left(\frac{\partial t}{\partial L^{\mathrm{sc}}_{Mc}} + \frac{\partial t}{\partial L^{\mathrm{sc}}_{M0}} + (n-1)\frac{\partial t}{\partial L^{\mathrm{sc}}_{M1}}\right. \\ &\left. + \frac{\partial t}{\partial L^{\mathrm{sc}}_{Mn}} + \frac{\partial t}{\partial L^{\mathrm{sc}}_{Mp}} + \frac{\partial t}{\partial L^{\mathrm{sc}}_{Mk}}\right)^2 \sigma^2_{L_{\mathrm{sc}}} \\ &+ \left(\frac{\partial t}{\partial L^{\mathrm{nsc}}_{Mc}}\right)^2 \sigma^2_{L^{\mathrm{nsc}}_{Mc}} + \left(\frac{\partial t}{\partial Vt_{Mc}}\right)^2 \sigma^2_{Vt} \\ &+ \left(\frac{\partial t}{\partial L^{\mathrm{nsc}}_{M0}}\right)^2 \sigma^2_{L^{\mathrm{nsc}}} + \left(\frac{\partial t}{\partial Vt_{M0}}\right)^2 \sigma^2_{Vt}. \\ &+ (n-1)\left(\frac{\partial t}{\partial L^{\mathrm{nsc}}_{M1}}\right)^2 \sigma^2_{L^{\mathrm{nsc}}} + (n-1)\left(\frac{\partial t}{\partial Vt_{M1}}\right)^2 \sigma^2_{Vt}. \\ &+ \left(\frac{\partial t}{\partial L^{\mathrm{nsc}}_{Mn}}\right)^2 \sigma^2_{L^{\mathrm{nsc}}} + \left(\frac{\partial t}{\partial Vt_{Mn}}\right)^2 \sigma^2_{Vt}. \\ &+ \left(\frac{\partial t}{\partial L^{\mathrm{nsc}}_{Mp}}\right)^2 \sigma^2_{L^{\mathrm{nsc}}} + \left(\frac{\partial t}{\partial Vt_{Mp}}\right)^2 \sigma^2_{Vt}. \\ &+ \left(\frac{\partial t}{\partial L^{\mathrm{nsc}}_{Mk}}\right)^2 \sigma^2_{L^{\mathrm{nsc}}} + \left(\frac{\partial t}{\partial Vt_{Mk}}\right)^2 \sigma^2_{Vt}. \end{aligned} \quad (16)$$

Then, the dynamic-logic NOR with a static keeper requires the computation of 18 partial derivatives, regardless the number of inputs or keeper size. For instance, to obtain σ_t^2 for a circuit with a static keeper using 1 point around mean for numerical derivatives, only 19 electrical simulations are required.

From these formulas we build the Gaussian probability density function (PDF) provided that we have the necessary parameters $\overline{t}$ (delay calculated at the nominal values) and σ_t [computed using formulation (14) or (16)].

B. Variance in Contention Time of Dynamic Circuit

For recent and future technologies, dynamic gates designed as in Fig. 1 require special attention because leakage current may lead to output discharge. If the output is at V_{DD}, leakage currents lead to output discharge in a finite contention time t_c in the case of input $i_0 = 0, i_1 = 0, \ldots, i_n = 0$. In the following, a statistical model for contention time variability in dynamic gates will be provided.

Let the contention time t_c be a function of random variables as

$$tc = tc\left(L^{\mathrm{sc}}, L^{\mathrm{nsc}}_{Mc}, \{L^{\mathrm{nsc}}_{i}\}^{n-1}_{i=0}, Vt_{Mc}, \{Vt_{Mi}\}^{n-1}_{i=0}\right) \quad (17)$$

then variance in contention time is given by

$$\begin{aligned}\sigma^2_{tc} = &\left(\frac{\partial tc}{\partial L^{\mathrm{sc}}_{Mc}} + n\frac{\partial tc}{\partial L^{\mathrm{sc}}_{Mi}}\right)^2 \sigma^2_{L_{\mathrm{sc}}} + \left(\frac{\partial tc}{\partial L^{\mathrm{nsc}}_{Mc}}\right)^2 \sigma^2_{L^{\mathrm{nsc}}_{Mc}} \\ &+ n\left(\frac{\partial tc}{\partial L^{\mathrm{nsc}}_{Mi}}\right)^2 \sigma^2_{L^{\mathrm{nsc}}_{Mi}} + \left(\frac{\partial tc}{\partial Vt_{Mc}}\right)^2 \sigma^2_{Vt_{Mc}} \\ &+ n\left(\frac{\partial tc}{\partial Vt_{Mi}}\right)^2 \sigma^2_{Vt_{Mi}}. \end{aligned} \quad (18)$$

In this case, only numerical derivatives for transistors Mc and Mi , for an arbitrary $0 \leq i \leq (n-1)$, need to be computed. This occurs because: 1) the dynamic-NOR is symmetric;

2) during transient simulation of the contention time, we have no transition in the input, i.e., $i_0 = 0, i_1 = 0, \ldots, i_n = 0$.

C. Probabilistic/Statistical Analysis of Logic Gates

In order to characterize VLSI circuits variability, the design for yield methodology must consider the probability of gate delay T to be less than a given $\tau_{\max}$ and gate delay PDF. Considering the circuits represented in Figs. 1 and 2, t_i denotes the time delay of a transition $I_i = 0 \rightarrow 1$ being i arbitrary, i.e., $0 \leq i \leq (n-1)$. We can write that the probability of the time delay of a transition in the input I_i to be less or equal to $\tau_{\max}$ is the cumulative PDF $f_i(t_i \leq \tau_{\max}) = \int_{-\infty}^{\tau_{\max}} p_{\overline{t}_{Mi},\sigma_{Mi}}(t_i)dt_i$, where $p_{\overline{t}_i,\sigma_i}(t)$ is a Gaussian PDF with average $\overline{t}_i$ and standard deviation σ_i.

Such parameters may be obtained by Monte Carlo simulations considering many runs, or directly by error propagation. For the former case $\overline{t}_i$ is the sampling average of delay for the input Mi while in the later it is the nominal delay value, i.e., the delay computed using the nominal values: $\overline{t}_i = t(\overline{L}^{\text{sc}}, \overline{L}^{\text{nsc}}_{M0}, \overline{Vt}_{M0}, \ldots)$. Supposing that all inputs t_i are independent random variables we arrive that the probability of the dynamic logic gate time delay to be less than $\tau_{\max}$ is

$$P(T < \tau_{\max}) = f_0(t_0 \leq \tau_{\max}) f_1(t_1 \leq \tau_{\max}) \ldots f_{n-1}(t_{n-1} \leq \tau_{\max}).$$

At this time we can ask more precise questions about the delay of the dynamic gate. We are interested in the probability of gate delay to belong to interval $[\tau_{\max} - d\tau_{\max}, \tau_{\max}]$ that here we denote as $F(\tau_{\max})d\tau_{\max}$. In first approximation, for a small value of h this probability is calculated as

$$\begin{aligned} F(\tau_{\max}) &\approx \text{Prob}\,(t_0 \leq \tau_{\max}, t_1 \leq \tau_{\max}, \ldots, t_{n-1} \leq \tau_{\max} | \\ &\qquad \text{at least one } t_i \in [\tau_{\max}, \tau_{\max} - h]) \\ &= \text{Prob}\,(\max\{t_i\} \in [\tau_{\max}, \tau_{\max} - h]) \\ &= \text{Prob}\,(\{t_0 \leq \tau_{\max}, t_1 \leq \tau_{\max}, \ldots, t_{n-1} \leq \tau_{\max}\} \\ &\qquad / \{t_0 \leq \tau_{\max} - h, t_1 \leq \tau_{\max} - h, \ldots, \\ &\qquad\quad t_{n-1} \leq \tau_{\max} - h\}) \\ &= \text{Prob}\,(\{t_0 \leq \tau_{\max}, t_1 \leq \tau_{\max}, \ldots, t_{n-1} \leq \tau_{\max}\}) \\ &\quad - \text{Prob}\,(\{t_0 \leq \tau_{\max} - h, t_1 \leq \tau_{\max} - h, \ldots, \\ &\qquad\quad t_{n-1} \leq \tau_{\max} - h\}) \\ &= P(T < \tau_{\max}) - P(T < \tau_{\max} - h). \end{aligned}$$

However, in the case which all inputs are symmetric, i.e., $\overline{t}_i = \overline{t}$ and $\sigma_{Mi} = \sigma$ for all $i = 0, \ldots, (n-1)$, we conclude that

$$P(T < \tau_{\max}) = f(T \leq \tau_{\max})^n = \left(\int_{-\infty}^{\tau_{\max}} p_{\overline{t},\sigma}(\tau)d\tau \right)^n \quad (19)$$

and from this we conclude that the distribution for maximum delay (delay of the dynamic gate), in a first approximation and for $h \ll 1$, is given by

$$F(T) = \left(\int_{-\infty}^{\tau_{\max}} p_{\overline{t},\sigma}(T)dT \right)^n - \left(\int_{-\infty}^{\tau_{\max}-h} p_{\overline{t},\sigma}(T)dT \right)^n. \quad (20)$$

For a suitable study, we must compare the distribution of $F(T)$ with the experimental distribution (histogram for maximum values of delay obtained over n_{sample} runs in Monte Carlo simulation)

$$H(T) = \frac{1}{n_{\text{sample}}} \# \left\{ \max \left\{ t_i^{isample} \right\} \in [\tau_{\max} - h, \tau_{\max}], i = 0, \ldots, n-1 \right\}$$

and for a sufficiently large number of runs we expect $H(T) \sim F(T)$ for $h \ll 1$.

IV. Results

In this section, we apply the methodology exposed in the previous sections to the analysis of variability of a pre-charge dynamic NOR. In the first subsection the delay of a dynamic NOR designed without the static keeper is studied. The variability in circuit behavior computed using our semi-analytical approach is compared to traditional Monte Carlo approach. Next we analyze contention time variability in the circuit without keeper, comparing Monte Carlo (MC) simulations to error propagation. The last subsection is dedicated to the analysis of delay variability in a dynamic NOR designed with a static keeper. There, we: 1) look at fits of data obtained by our probabilistic approach compared to MC ; 2) show that the static keeper has an optimal channel width for delay variance.

We use the commercial electric simulator HSPICE [19] to obtain numerical derivatives needed for variability analysis in delay and contention time. The transistor model employed is Berkley BSIM3 Predictive Technology Model for the 70-nm node (BPTM70) [20].

We consider the transistor parameters threshold voltage (V_t) and channel length (L) as random variables with Gaussian distribution. For each transistor i, L_i is assumed to have one spatially correlated component and one spatially uncorrelated component, i.e., $L_i = L_{\text{sc}} + L_{r_i}$ so that $L_{\text{sc}} = N(70\text{ nm}, 5\text{ nm})$ and $L_{\text{nsc}} = N(0, 5\text{ nm})$. Transistor threshold voltage are random variables given by $Vt_{\text{pMOS}} = N(-0.22\text{ V}, 13.3\text{ mV})$ and $Vt_{\text{nMOS}} = N(0.2\text{ V}, 13.3\text{ mV})$. These values are in accordance to ITRS [21] and [22].

A. Delay Variability in a Dynamic NOR Without Keeper

In this subsection we present analysis of delay variability using both the error propagation approach and Monte Carlo simulation, for dynamic logic with 2, 4, 8, 16, 32, and 64 inputs. Consider the pre-charge dynamic NOR given in Fig. 1. Let W_{Mi}, where $i \in \{0, \ldots, n-1\}$, be the channel width of the n pull down transistors, and $W_{M_{\text{clk}}}$ the channel width of transistor M_{clk}. For our experiments, $W_{M_0} = \ldots = W_{M_{n-1}} = 1\ \mu$m and $W_{M\text{clk}} = 2.5\ \mu$m.

In order to analyze circuit delay variability, at this first moment consider the delay for a transition $00\ldots00 \rightarrow 10\ldots00$ (a transition $0 \rightarrow 1$ in one input), which causes a transition $1 \rightarrow 0$ at the output. The delay can be written according to (12), and (14) gives its variance using error propagation. To obtain a delay histogram of one input using Monte Carlo simulation, we run a large number of electrical simulations in which V_t, L_{nsc}, and L_{sc} are random Gaussian variables. Fig. 3 exposes the histogram and PDF of the delay of the transition at one input in an

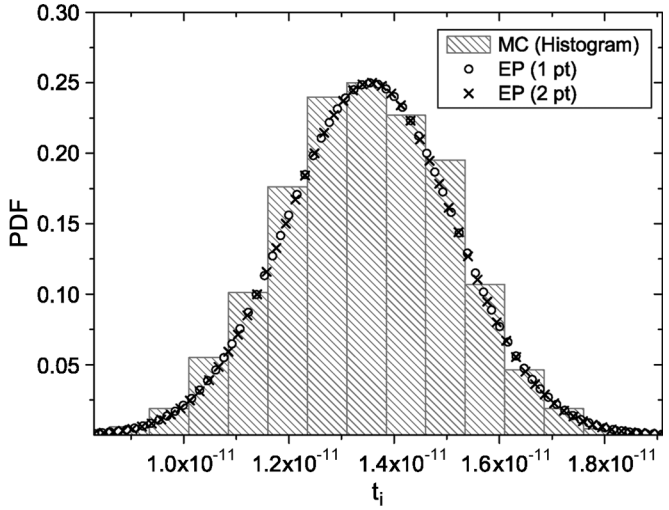

Fig. 3. PDF (using EP) and histogram (using MC) for the delay of a transition in one of the inputs of the dynamic-NOR without keeper.

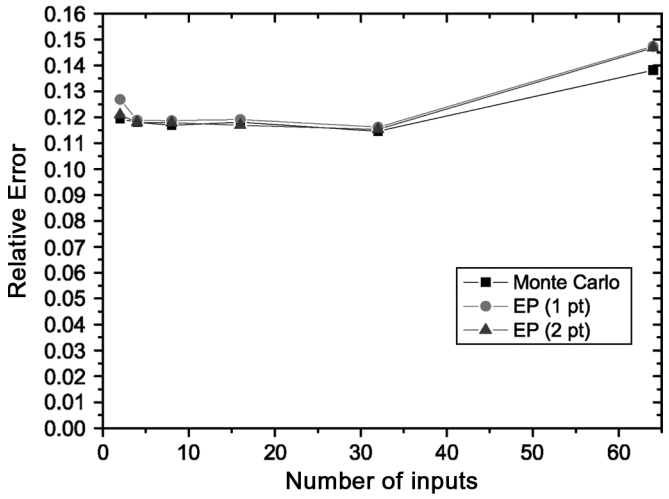

Fig. 5. Comparison of σ/μ obtained by MC and EP as a function of the number of inputs.

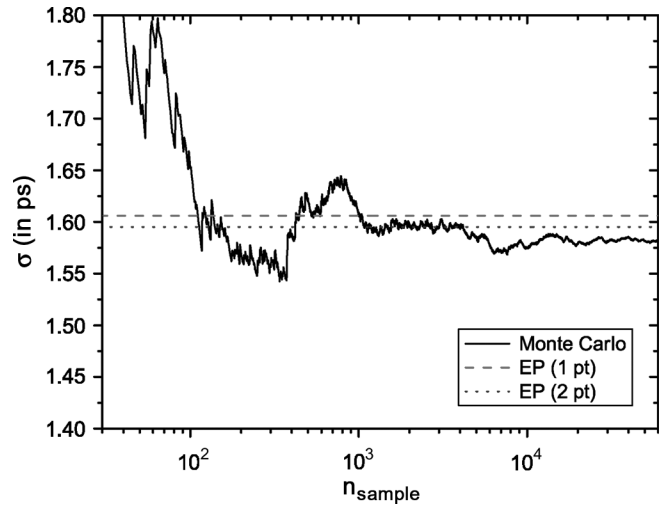

Fig. 4. Convergence of σ as a function of the number of MC simulations compared to EP using 1 and 2 points for derivative.

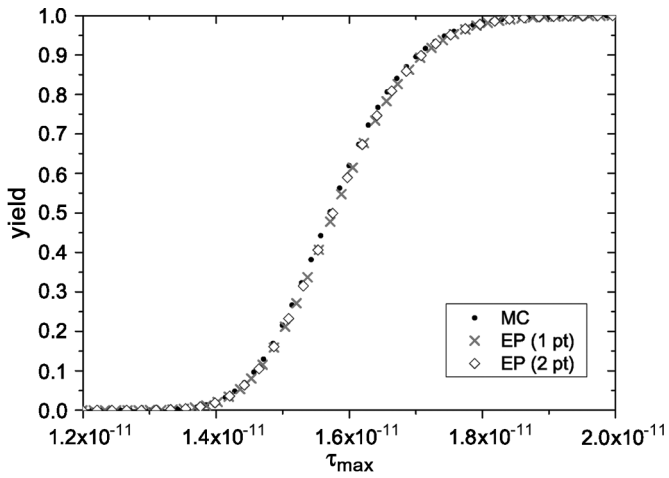

Fig. 6. Yield of an 8-input dynamic-NOR without keeper computed by MC and EP.

8-input dynamic-NOR. The histogram was obtained by MC simulation with 1000 runs, while the PDF was obtained using $\overline{t_0}$ computed by simulation with nominal values and σ_{t0} given by error propagation. The figure shows how EP, using 1 or 2 points around mean for numerical derivatives, compares to MC.

The convergence of the MC method can be verified by analyzing σ_S as a function of the number of runs. Fig. 4 shows the values obtained by EP using 1 and 2 points with the convergence of σ_T of an 8-input dynamic-NOR computed by MC. These simulations show that the MC method requires more than 10^3 runs to obtain a result with accuracy similar to EP. Error propagation using 1 point presents error of 1.5% in comparison to a MC run with 6×10^4 simulations. EP with 2 points for derivative presents an error of only 0.8% in comparison to MC. For a statistical process, this small difference is not significant.

Fig. 5 shows the standard deviation of the pre-charge dynamic-NOR delay considering 2, 4, 8, 16, 32 and 64 inputs. The standard deviation obtained by EP using 1 and 2 points for derivatives is compared with Monte Carlo using up to 6×10^4 runs. The relative standard deviation computed by EP (δ_{t_0}/μ_{t_0}) minus the relative standard deviation given by MC $(\sigma_{t_0}/\mu t_0)$ is less than 2% in all cases. Although we performed MC with 6×10^4 runs, only 10 electrical simulations are required for EP using 1 point around mean and 19 runs using 2 points around mean. This allows comparable results in terms of accuracy while improving running time by orders of magnitude.

The probability of the delay of a transition not being greater than a design constraint $\tau_{\max}$ tells the yield of the gate. Considering the symmetry of pre-charge dynamic-NOR circuit, this probability is given by (19). To apply this formula to the design, consider that $\tau_{\max}$ is a design constraint and $p_{\overline{t},\sigma}(t)$ is computed using error propagation or MC. Fig. 6 presents this formula applied to an 8-input dynamic-NOR, where yield (probability of all inputs having time delay less than $\tau_{\max}$) is a function of $\tau_{\max}$. The figure compares $p_{\overline{t},\sigma_t}(t)$ using average and standard deviation computed using EP (1 or 2 points around mean for numerical derivatives) with the ones obtained by MC.

Once the gate delay is given by the greatest transition delay and considering the symmetry in the pull-down transistors, (20)

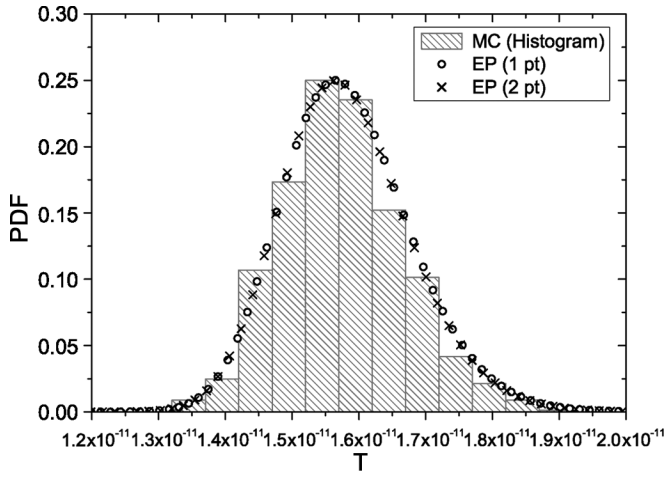

Fig. 7. Delay PDF (using EP) and histogram (using MC) of the dynamic-NOR without keeper.

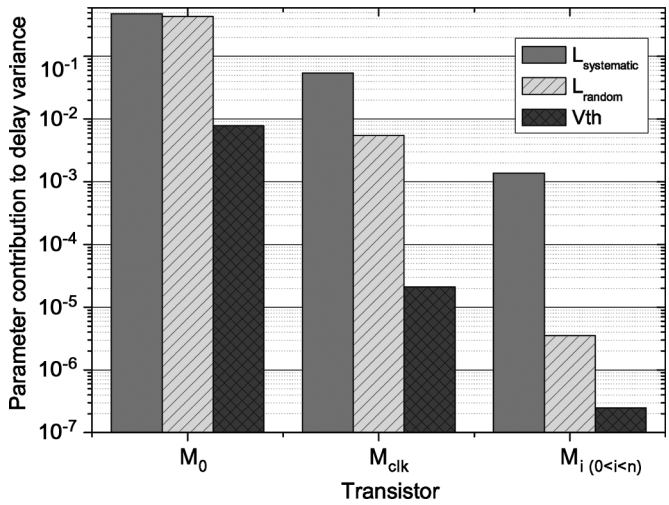

Fig. 8. Contribution of the parameters to the delay variability of the dynamic-NOR without keeper.

gives PDF of the gate delay. This formula computes the probability of the gate delay to be within the range $[\tau - h, \tau]$. Fig. 7 presents the Gaussian PDF obtained using EP with 1 and 2 points for derivatives compared to the histogram obtained by MC simulation with 10^3 runs. Again EP fits the data obtained using MC, with a running time speedup of 100× (approach using 1 point for derivative) or 50× (approach using 2 points for derivative).

Our methodology is suitable for a design-for-yield synthesis flow because it allows the study of the individual contribution of each electric parameter to the circuit variability, as exposed in the Section II-D. The Fig. 8 exposes the individual contribution of each parameter: Vt, $L_{\rm sc}$ and $L_{\rm nsc}$, considering (1) the pull-down transistor which switches from 0 to 1, (2) clock transistor and (3) the pull-down transistors that remain 0. Actually, we verify that more than 80% of the delay variability comes from the SC and NSC components of the channel length of the transistor that is switching.

Pre-charge dynamic-NOR delay variability computed using error propagation is equivalent to the results achieved by the

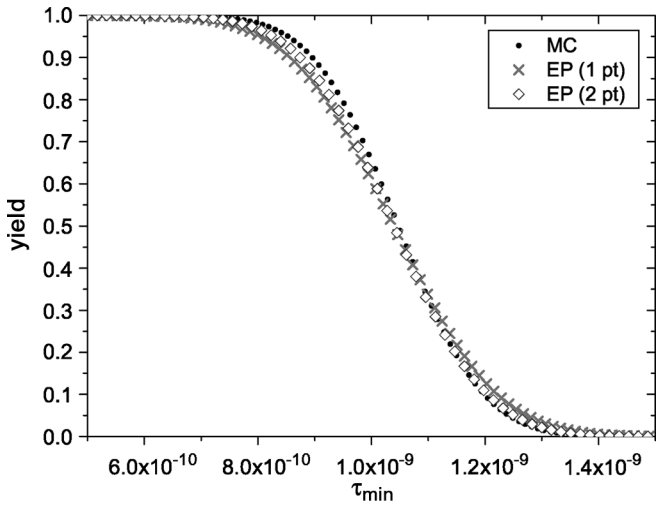

Fig. 9. Yield of the dynamic-NOR as a function of $\tau_{\rm min}$: distribution of the time required to discharge the dynamic-NOR without static keeper.

widely employed Monte Carlo simulation at electric level, featuring a speedup up to 100× (compared to MC using 10^3 runs). As the yield analysis using error propagation requires 10 or 19 electrical simulations for approaches using 1 or 2 points for the derivatives, respectively, an improvement of 50× is achieved. The difference of the standard deviations computed using MC and EP is less than 2%.

B. Contention Time of a Dynamic NOR

Transistors designed in deep-submicron technology nodes suffer of increasing leakage currents. Dynamic logic gates designed as in Fig. 1 present the problem of the output node discharging if all inputs keep at logical 0 during the evaluation phase. As discussed in the Section III-B, there is a finite contention time t_c for which the dynamic output signal is discharged to below $V_{\rm DD}/2$.

Variance in contention time of a dynamic-NOR can be computed using EP, as given by (18). The probability of the contention time to be greater than a given constraint $\tau_{\rm min}$ gives the probability of the dynamic-NOR to work properly. The formula for probability of contention time to be greater than the constraint $\tau_{\rm min}$ is given by

$$P(\mathrm{tc} > \tau_{\rm min}) = \int_{\tau_{\rm min}}^{\infty} p_{\overline{tc},\sigma_{tc}}(t)dt \tag{21}$$

Fig. 9 presents comparison of yield as a function of $\tau_{\rm min}$ computed by EP using 1 and 2 points around mean in comparison to statistical values obtained by MC with $n_{\rm sample} = 10^3$. In this case, semi-analytical approach requires only 7 or 12 simulations for numerical derivatives using 1 or 2 points, respectively. The speedup of EP over MC is up to 140×, while the difference of the standard deviations is less than 1%.

C. Delay Variability in a Dynamic-NOR *With Static Keeper*

In this subsection, we discuss error propagation and variability analysis for dynamic-NOR gates with a static keeper.Con-

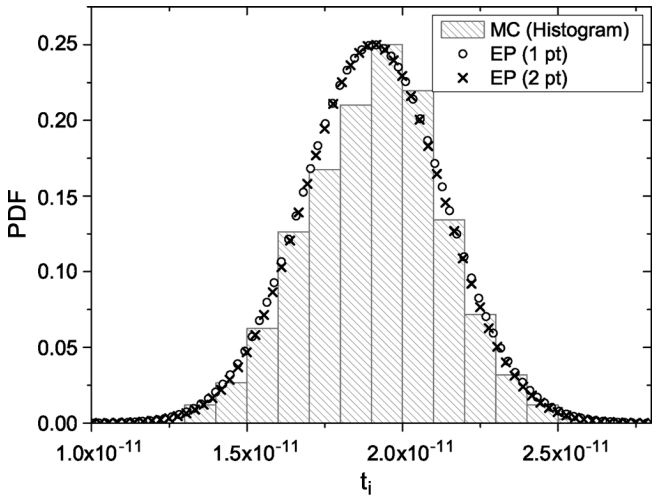

Fig. 10. PDF (using EP) and histogram (using MC) for the delay of a transition in one of the inputs of the dynamic-NOR with keeper.

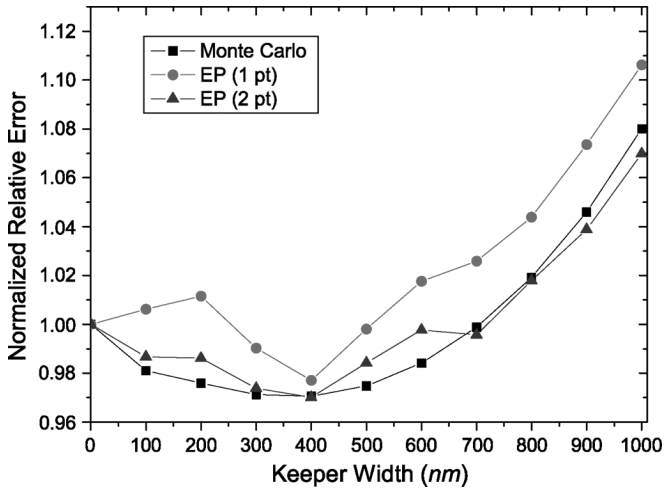

Fig. 11. Relative error of the 8-input dynamic-NOR as a function of the keeper width.

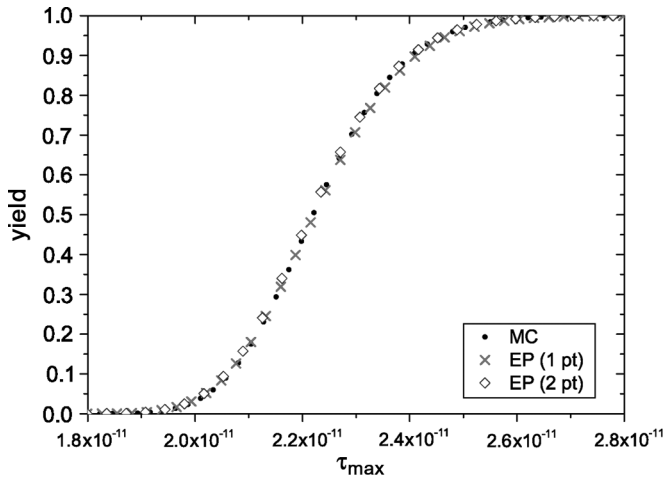

Fig. 12. Yield of an 8-input dynamic-NOR with keeper computed by MC and EP.

sider the pre-charge dynamic-NOR shown in Fig. 2. Let W_{Mi} be the channel width of the pull-down transistors, $W_{M_{\rm clk}}$ be the channel width of transistor $M_{\rm clk}$, W_{Mp}, W_{Mn} and W_{Mk} be the width of transistors M_p, M_n and M_k, respectively. Consider $W_{Mi} = W_{M_n} = 1\ \mu$m and $W_{M_{\rm clk}} = W_{M_p} = 2.5\ \mu$m.

The (16) computes the variance of a dynamic-NOR with a static keeper using error propagation. This simulation represents the variability of the delay when a transition $00\ldots00 \rightarrow 10\ldots00$ occurs, i.e., a transition $0 \rightarrow 1$ in one input (without loss of generality, we consider transition on input I_0, because inputs are symmetric). The partial derivatives of the 6 transistors computed numerically. Since each transistor has 3 random parameters (Vt, $L_{\rm sc}$ and $L_{\rm nsc}$), 18 partial derivatives must be computed. Fig. 10 presents how the PDF computed by EP using 1 or 2 points for partial derivatives compares to the histogram obtained by MC using 10^3 samples. The circuit in consideration is an 8-input dynamic-NOR with $W_{Mk} = 500$ nm. Error propagation using 1 point around mean for derivative evaluation requires 19 Spice simulations, while the approach using 2 points requires 36 Spice simulations.

Fig. 11 presents the relative standard deviation (σ/μ) of the delay of the 8-input dynamic-NOR with static keeper as a function of the keeper strength. Error propagation using 1 and 2 points for numerical derivatives was performed, as well as MC simulation with $n_{\rm sample} = 3 \times 10^4$. The relative standard deviation is normalized by the relative standard deviate of the 8-input dynamic-NOR without keeper shown in the previous subsection. The curve indicates that there is one keeper strength that minimizes the variability. In our case study, the dynamic-NOR designed with $W_{Mk} = 400$ nm presents a 3% decrease in variability compared to a dynamic-NOR without keeper, while a design using $W_{Mk} = 1\ \mu$m presents a 6% increase in delay variability. Also, this figure again shows that EP obtained results statistically equivalent to MC with a high improvement in simulation efficiency. Error propagation using 1 point around mean for numerical derivatives presents an error up to 2% compared to MC, while the approach using 2 points for derivatives presents an error smaller than 1%.

From the standard deviation computed using EP and the average approximated by the simulation using the nominal values, the probability of the gate delay T to be smaller than a constant $\tau_{\rm max}$, i.e., the yield of the gate, is computed using (19). Fig. 12 shows the yield of an 8-input dynamic-NOR with static keeper $(W_{Mk} = 500\,{\rm nm})$ in function of the time constraint $\tau_{\rm max}$. Once again the plot produced using the values computed by EP fits well with the one computed using MC.

PDF of the gate delay is computed using (20), where σ_τ can be computed using EP and $\overline{\tau}$ is approximated by the simulation using nominal values. The Fig. 13 exposes the Gaussian PDF of the delay of the dynamic-NOR with static keeper. The plot developed using the proposed methodology fits well to the histogram computed using MC. In order to draw the PDF using EP, we run 19 simulations in the case of derivatives using 1 point around mean, and 36 electrical simulations when using 2 points. This represents an improvement in the running time up to 50× compared to MC using 10^3 runs.

Fig. 14 presents the contribution of each parameter to the delay variability. They were computed according to the Section II-D. As in the case of the dynamic-NOR without keeper,

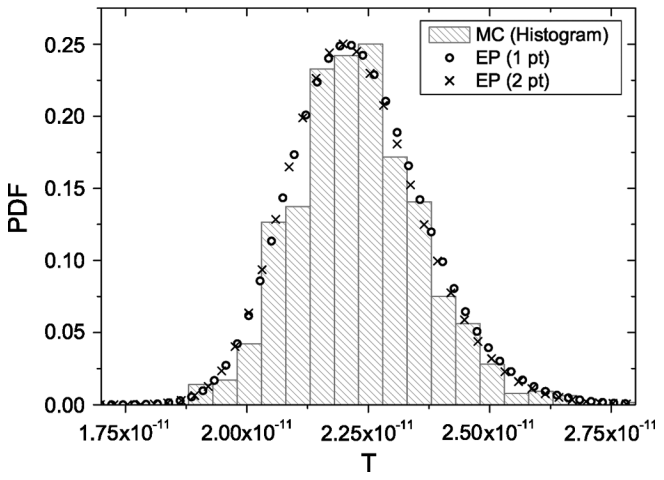

Fig. 13. Delay PDF (using EP) and histogram (using MC) of the dynamic-NOR with keeper.

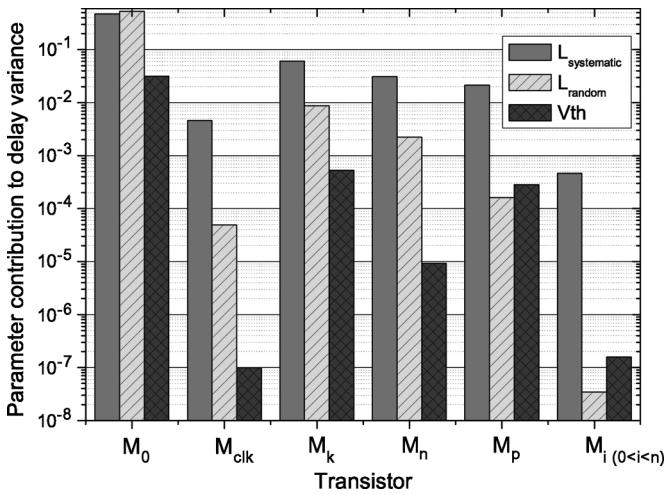

Fig. 14. Contribution of the parameters to the delay variability of the dynamic-NOR with keeper.

the contribution of L^{nsc} and L^{sc} are orders of magnitude more significant than the contribution of the other parameters.

V. Conclusion

A novel methodology for variability analysis in dynamic logic is presented. The methodology shows results statistically equivalent to usual sampling techniques like Monte Carlo simulation, while reducing simulation time by orders of magnitude. Our theoretical approach is generic and can be extended to gates which implement other Boolean functions as well as other kinds of dynamic and static gates with minor changes.

The proposed methodology allows quantifying the contribution of each component to the variability in circuit behavior. The components that contribute more to the circuit variability may then be selected for optimization. In our simulations the contribution of channel length is orders of magnitude more relevant than threshold voltage. These results are important for an yield enhancement phase.

Also, we identify an optimal strength for the static keeper transistor, which leads to diminishing the variance of the time delay by correctly sizing the static keeper.

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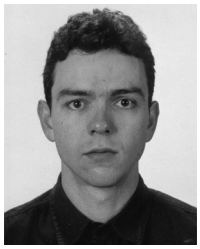

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