Timing and Power Consumption in High-Speed Very Deep Sub-Micron On-Chip Interconnects

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***Abstract*— With continuously increasing on-chip frequencies and shortening signal rise times, inductance effects pose severe difficulties on efficient timing analysis. This work analyzes the effects of inductive coupling in conjunction with capacitive coupling on power consumption and different timing parameters in high-speed on-chip parallel interconnects. We show that crosstalk, noise, signal integrity, signal rise and fall times, as well as power consumption strongly depend on the data toggling pattern. We also point out that the worst and best case switching patterns are different in the case of lines dominated either by capacitive coupling or by inductive coupling. In order to notice and analyze these variations, various scenarios are considered, such that different combinations of the two types of coupling are obtained. We show that classically employed figures of merit developed for line inductance do not hold when inductive coupling becomes important and simple models that take into consideration only line inductance and capacitive coupling fail to accurately predict those toggling patterns. In order to assess the accuracy of our results, we have carried out numerous parameter extraction steps with 3D field solvers and extensive experiments with SPICE simulations.**

***Index Terms*— On-Chip Interconnects, Capacitive and Inductive Coupling, Timing, Power Consumption.**

I. Introduction

During the last decade, the influence of the on-chip interconnect structure on performance, area, and power dissipation increased steadily. Interconnect-related latency and energy dissipation issues have become so stringent that numerous design and research engineers even claim that interconnects have replaced transistors as the main determinants of chip performance [1]. Moreover, it is generally predicted that in upcoming technologies, interconnects will be responsible for the majority of the signal degradation in high-speed systems [2].

With every new technological node, power dissipation in interconnects scales up due to increasing coupling capacitance between neighboring lines [3]. Furthermore, the need for performance rapidly pushes operating frequencies in the GHz domain, thereby dramatically reducing rise and fall times. In addition, inductive effects also became significant in global and intermediate lines due to a reduction in their wire resistance. Consequently, line and mutual inductive as well as capacitive effects cannot be neglected anymore, and resulting variations in delay, power consumption, overshoots, and inductive crosstalk become critical bottlenecks in integrated circuit performance [4], [5].

In contrast to capacitive coupling, which is a short-range effect, self and mutual inductance are difficult to extract and to simulate as they are functions of closed current loops [6]–[8]. The determination of such current paths is a rather tedious task, and as an alternative approach, the PEEC (Partial Equivalent Elements Circuit) method emerged [9]–[11]. In addition to the extensive research done in inductance extraction and modeling, the effects of on-chip inductance on various aspects of integrated circuit performance have also been often highlighted [11], [12]. Furthermore, in order to mitigate capacitive and inductive coupling effects, techniques like shielding, buffer insertion, line widening, wire separation, and net ordering have been proposed [13]–[15].

In this work, we focus on the capability of several electrical interconnect models to accurately predict crosstalk, signal delay, rise and fall times, and power consumption in on-chip parallel buses. The performed simulations and analyses show that power consumption and timing parameters like crosstalk, noise, signal integrity, signal rise and fall times, strongly depend on both geometric wire parameters and data toggling patterns, and do not obey general rules as mentioned in previous work. Furthermore, we point out that the worst and best case switching patterns are different in the case of lines dominated either by capacitive coupling or by inductive coupling and that this significant difference appears mainly because of two reasons: first, due to the distinct nature of the coupling, which is of long range for inductance and of short range for capacitance; and second, because of their opposite effects when aggressor and victim toggle synchronously in the same direction, i.e. a slower transition for inductive coupling and a faster switching for the capacitive one.

Another contribution of this work is the outcome that worst and best case switching patterns for those parameters differ significantly as a function of the employed interconnect model and that simple models including only coupling capacitances and line inductances fail to accurately predict the worst and best cases for the toggling patterns. Additionally, another main contribution of this work is the outcome that the classically employed figures of merit developed for line inductance do not hold when inductive coupling becomes important. Consequently, the selection of the right model is extremely critical and more conservative rules should be used for the inclusion of mutual inductances. Further, because of the different possible magnitude of the two couplings, the worst case and best case toggling patterns vary in a very complex manner. For this purpose, we consider various scenarios, such that different combinations of the two types of coupling can be observed. Based on these scenarios, we explain the way inductive and capacitive

coupling interact to produce different worst and best case toggling patterns. The different possible relations between the effects of self- and mutual inductance and the effects of capacitive coupling is determinant in finding the best and worst case pattern. The accuracy of the results has been assessed by means of extensive SPICE simulations and parameter extraction procedures with 3D solvers.

This paper is organized as follows. First, section II highlights the most important interconnect-related scaling issues in Very Deep Sub-Micron (VDSM) technology nodes. Here, the focus lies on indicating the different types of coupling occurring in local, intermediate and global interconnects. Afterwards, section III gives a brief overview on on-chip interconnect modeling and model selection. The main point is twofold: on the one hand, to give an overview on how to choose the model of least complexity; and on the other, to discuss the figures of merit proposed for the inclusion of line inductance. Further, based on the previous two sections, Section IV goes into details on the simulation environment, i.e. the employed electrical interconnect models and the corresponding parameter extraction procedure. Section V is dedicated to the analysis of crosstalk and timing parameters (delay and rise time), while section VI discusses the effects of capacitive and inductive coupling on power consumption. The paper ends with some concluding remarks.

II. Interconnect Scaling

Technological issues form the underlying background for every analysis related to on-chip interconnects. In order to provide a solid foundation for an understanding of interconnect-related VDSM effects, this section discusses interconnect scaling and its influence on performance and power consumption. The goal is twofold: to show that both capacitive and inductive coupling will play increasingly important roles in nanometer high-speed IC design and that depending on the type of buses, i.e. local, intermediate, or global, the two types of coupling will play different roles.

Technology scaling refers to the systematic rules employed to miniaturize devices while maintaining or improving their characteristics in terms of speed, power-efficiency and reliability. Those methodologies, together with advances in device integration and lithography, have resulted in a steady reduction of device feature sizes over the past years. We will focus on the interconnect scaling trends in the following.

At first glance, the theory of MOS device scaling suggests that signal wires should be scaled down by the same factor as active devices, so that the chip area can be reduced. However, as the wire cross section shrinks, the conducting characteristics of the wires degrade. In order to address these two conflicting requirements, interconnect scaling in sub-micrometer technologies can be split into two distinct components: *local* and *global* wire scaling. Note, that sometimes also a third component, i.e. the *intermediate* wire scaling, is considered. Local wires refer to lower metalization layers, which are normally used to connect nearby gates within a given digital module. On the opposite, global wires are used for connections among blocks, and for power and clock routing. The fundamental differences between these two types of wires suggest different scaling strategies. Two typical scenarios [8] are depicted in Table I, where α represents the scaling factor.

A major concern for the scaling of local wires is how to maintain the high integration density provided by the smaller device features. In order to accomplish this goal, both wire width and thickness are scaled down. Consequently, the wire cross-section is reduced, as well as its conductance per unit length. Since the capacitance per unit length is kept almost constant and the mean wire length decreases, the RC delay is not strongly altered by scaling. The main drawback of this approach is the increase in the current density of the wires, which reduces the reliability of the system. To cope with this problem, the wire thickness is reduced by a smaller factor in the so-called *quasi-ideal scaling*. Thus, the RC delay is improved by a factor of $\sqrt{\alpha}$, and the current density does not increase as rapidly as in the previous scenario.

Despite these valuable advantages, the technique suffers from a major drawback related to the increased aspect ratio of the wires. As the wire thickness gets larger than the width, the manufacturing process requires deep and narrow trenches which are difficult to produce. Furthermore, the capacitance between neighboring wires increases dramatically and becomes the dominant factor of the total wire capacitance. The consequence is higher crosstalk noise that degrades the signal integrity and modifies the power consumption of the bus line drivers [3]. Because local wires are generally very short, self and mutual inductance will not play an important role, and thus, local lines will be characterized almost exclusively by capacitive coupling.

If the ideal or quasi-ideal scaling methodologies previously discussed were applied to global wires, an unacceptable performance loss would occur. The reason is the different mean wire length behavior for local and global wires. Since global wires connect blocks, their length depends on the chip area, and increases with a factor of approximately $\sqrt{\alpha}$. The consequence is an unacceptable increase in the RC delay. To palliate this problem, *constant dimension scaling* may be applied. In this case, the dimensions of upper layer wires are not modified, and, thus, an improved RC delay can be achieved (see Table I). Obviously, the drawback is a drop in the routing resources at the upper levels. Moreover,

TABLE I
Wire scaling scenarios for local and global interconnect.

	Local wiring		*Global wiring*	
	Ideal Scaling	*Quasi-ideal Scaling*	*Ideal Scaling*	*Constant Dimensions*
Wire width	$1/\alpha$	$1/\alpha$	$1/\alpha$	1
Wire thickness	$1/\alpha$	$1/\sqrt{\alpha}$	$1/\alpha$	1
Wire length	$1/\alpha$	$1/\alpha$	$\sqrt{\alpha}$	$\sqrt{\alpha}$
Resistance	α^2	$\alpha^{3/2}$	α^2	1
Capacitance	1	≈ 1	1	1
RC delay	1	$1/\sqrt{\alpha}$	α^3	α
Current density	α	$\sqrt{\alpha}$	α	$1/\alpha$

with increasing wire length and rise times inductive effects cannot be neglected anymore [8]. Therefore, inductive coupling will play an important role in global as well as intermediate wires. However, an interesting observation can be added at this point. Being a long-range effect, inductive coupling allows neighbors of order higher than two to become inductive aggressors. In the case of neighbors of order one, one cannot know *a priori* whether they are inductive or capacitive aggressors. This is decided by wire geometries, propagation time, and rise times. Basically, for one line we expect to have three major cases when inductive and capacitive coupling appear: first, the very inductive case when the first-order neighbor is an inductive aggressor; second, the medium inductive case for which the first-order neighbor is a capacitive aggressor but overall, the cumulated effect of all inductive aggressors dominates the effect of the capacitive ones; and third, the less inductive case when the capacitive effect of the first-order neighbors outweighs the added effect of all inductive aggressors. As a first order approximation, we can expect the first and second case to show up more in global buses and the second and third to be typical for intermediate wires.

III. Interconnect Models

In this work, we want to model typical scenarios for global and intermediate parallel buses. First, our goal is to choose the most appropriate interconnect model. In this section, we therefore briefly discuss interconnect models of varying complexity and give an overview of basic criteria to choose among them. For very detailed expositions on this topic, the interested reader is referred to [2], [4], [16], [17].

In a wide sense, *high-speed interconnects* can be defined as interconnects in which signals propagate in a very short time. Though, small propagation times require very fast rise times, and when the rise times become comparable to the propagation times or the line losses are not negligible, the line actually electrically isolates the driver from the receiver. Within the transition time, the interconnect functions as the load to the driver and as the input impedance to the receiver. Thus, various transmission line effects, such as reflection, crosstalk, and overshoot have to be taken into consideration [2]. Depending on the structure, signal rise time, and operating frequency, interconnects can be modeled as lumped, distributed, or full-wave models.

The most important criterion employed for classifying an interconnect is based on its *electrical length*. A wire is considered to be electrically short if, at the highest operating frequency of interest, the interconnect is much shorter than the corresponding wavelength [2]. In general, the highest operating frequency is determined by the rise and fall times of the propagated signal. Even though the frequency spectrum of a trapezoidal pulse is infinite, the energy of the signal is concentrated in the lower part of the spectrum and rapidly decreases with increasing frequencies. Hence, the signal spectrum can be considered finite without affecting the signal waveform. For this purpose, the concept of *significant frequency*, f_s, has been proposed to reduce the complexity of the required information. For a trapezoidal pulse, f_s is defined as $0.34/t_r$, where t_r represents the pulse ramp time. Less than 15 % of the spectral components are at higher frequencies than f_s, and their overall magnitude is very small [4]. In some cases, the more conservative limit of $1/t_r$ may be used [2].

At low frequencies, wires are electrically short, and electromagnetic phenomena descriptions can be reduced to electric models. Thus, interconnects can be accurately modeled with lumped RC or RLC circuit models. However, due to faster rise times and longer interconnect lengths, the electrical length of interconnects becomes a significant fraction of the operating wavelength and transmission line effects must be taken into account. Lumped models become inadequate and cannot accurately predict crosstalk, rise time, or delay [4], [17]. Consequently, transmission line models based on the transverse electromagnetic mode (TEM) assumption are required. Moreover, when dimensions are electrically large, the structure can be broken into a set of electrically small substructures, each of them equivalent to a lumped model based on the so-called *per-unit length (PUL) parameters*. The PUL parameters of inductance, capacitance and conductance are governed by the fields external to the conductor and are determined as a static solution to the Laplace equation in the transversal plane of the line. In contrast, the entries in the PUL resistance matrix are governed by the interior fields [17], [18]. Thus, the PUL parameters contain the entire cross-sectional structural dimensions of the interconnect.

The main assumption made to derive the so-called *telegrapher's equation* [17] is that no field components exist in the direction of propagation, which is the case when there are losses neither in the conductors nor in the dielectric material. Nevertheless, both conductors and dielectrics are imperfect and small losses captured by the PUL resistance parameter do exist. The medium may be lossy and not violate the TEM assumption as long as it is homogeneous [18]. Lossy conductors invalidate the TEM field structure assumption, but if conductors are characterized by "small" losses, it is still possible to find an approximate interpretation in terms of quasi-static voltage and current in the orthogonal plane, and therefore, an electrical model [17]. This assumption is referred to as *quasi-TEM*. In practical situations, the interconnects may need to be modeled as nonuniform lines, and in this case, the PUL parameters are functions of the distance [2]. Details about different analytical and numerical methods for determining the PUL parameters can be found in [17], [18].

In the PEEC approach, the interconnects are subdivided into small surface and volume elements. Partial inductances and capacitances are computed from these elements and the resulting circuit elements are combined with each other into a complete PEEC circuit. For interconnect structure sizes which are much smaller than the smallest wavelength of interest, one can assume that the field instantly travels through space from one point to another. The assumption of quasi-stationarity allows a description of time dependent fields from static field calculations. Thus, PEEC models are RLC circuits where individual elements are extracted from

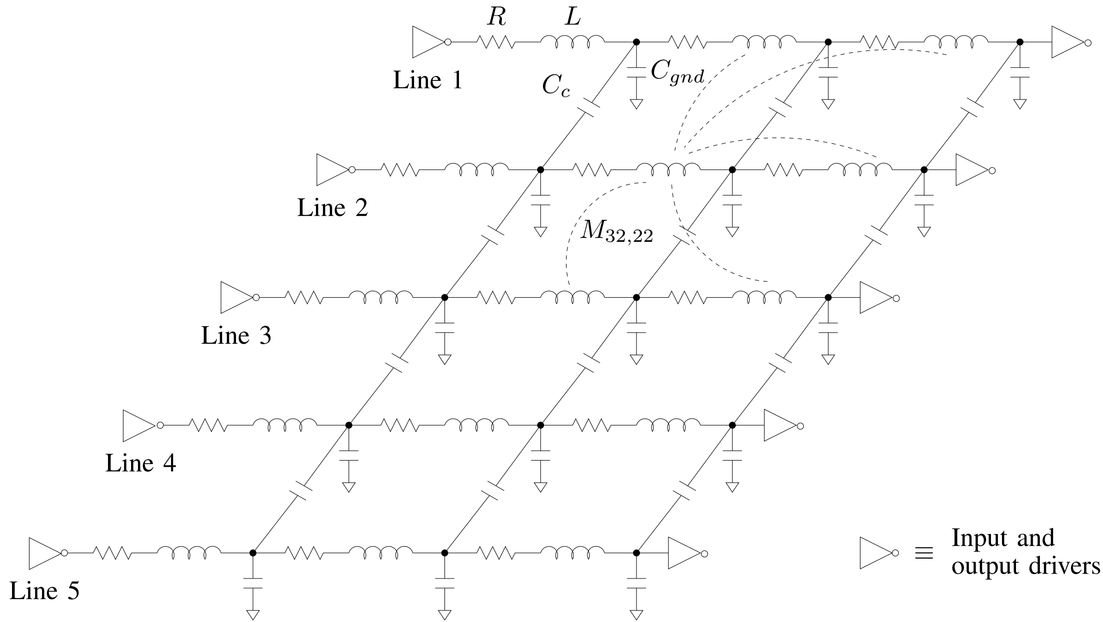


Fig. 1. Distributed full $RLMC$ interconnect model with resistance R, ground capacitance C_{gnd}, coupling capacitance C_c, self-inductance L, and mutual inductance $M_{ij,kl}$ indicated by a dashed line, where i and k denote the wire and j and l the segment. So, $M_{32,22}$ is the mutual inductance between the second segment ($j = 2$) of the third wire ($i = 3$) and the second segment ($l = 2$) of the third wire ($k = 2$). For illustration purposes, device symbols are given only for the first segment of the first wire and mutual inductances are only indicated for the first two segments of the first three wires.

the geometry using a quasi-static (non-retarded) solution of Maxwell's equations [2]. However, at very high frequencies the PEEC model is inaccurate as it does not consider the effect of the finite speed of light, i.e. retardation. Therefore, the PEEC approach has been extended to geometries where the size of the critical coupling distances is no longer short compared to the wavelength. The retarded PEEC (rPEEC) models include the retardation effect and provide a full-wave solution [16], [19].

In order to efficiently and accurately determine the signal characteristics of a bus, it is of utmost importance to choose the most appropriate model for on-chip interconnects. Even though a full-wave model would always give the correct solution, such approaches are extremely computationally extensive. There are several works in literature proposing and dealing with qualitative and quantitative methods for choosing the most appropriate interconnect model, i.e. an accurate model of least complexity [2]–[5], [11], [16]–[24]. In the following, we present some of the most used methods and figures of merit.

When the line capacitance becomes comparable to the load capacitance, signal delay propagation cannot be neglected anymore for a correct delay analysis. Additionally, in the case of longer lines, signal propagation is worsened due to the increasing line resistance, and therefore RC models have to be employed. However, simple lumped RC models can only be efficiently used if the interconnect induced propagation delay is considerably smaller than the rise time of the signal propagating through the interconnect. Thus, the distributed nature of the line impedance would not be modeled and the line has to be split into several cascaded lumped segments. The propagation delay induced by each of those segments $t_{p,seg}$ must be much shorter than the rise time [2], [25], [26]. A typical acceptable delay through a segment is $t_{p,seg} \leq t_r/10$.

As mentioned in Section II, global lines are generally wide and exhibit low resistance. The increase in clock frequencies pushes the rise and fall times to steadily decreasing values. Thus, the significant frequency is pushed into the GHz domain. Therefore, the line inductance affects even more the timing characteristics of on-chip interconnects and has to be included into a precise model. The rise time to be compared with the propagation time, t_p, is the one for the signal after the driver. Therefore, the input rise time is not necessarily a well-suited parameter for selecting the line model. Nevertheless, when the input rise time is much greater than the propagation time, non-inductive models can be used to simulate and check the value of the rise time at the driver output. The inductive model is not to be used if this approximate rise time is still greater than the propagation time. Note that the rise time is often compared to $2t_p$ in order to consider reflection [17].

Apart from the ration between signal rise time and time-of-flight, there is another important factor in correctly determining the interconnect model to be employed: the damping of the interconnect line [20]. The damping factor of an RLC line is given by:

$$\xi = \frac{\tau_{RC}}{2\tau_{LC}} = \frac{R_t C_t}{2\sqrt{C_t L_t}} = \frac{Rl}{2}\sqrt{\frac{C}{L}}\,,$$

where R, L, and C are the resistance, inductance, and capacitance per unit length respectively, l is the length of the line, R_t, L_t, and C_t are the total resistance, inductance, and capacitance of the line, respectively, and τ_{RC} and τ_{LC} are the RC and LC time constants of the line, respectively. When ξ decreases, which actually means that the effects due

to reflections increase, the RC model becomes inaccurate.

In order to assess the possibility of ringing and thus the need of an inductive model, one also has to compare the driver impedance, Z_d, with the characteristic impedance of the line, Z_l. The output impedance, Z_o, of a line is usually capacitive and, thus, very small compared to the line impedance, $Z_o < Z_l$. Consequently, the condition for ringing is $Z_d < Z_o$, and, thus, lower impedance drivers are candidates which may need an inductive interconnect model [17].

In [20], the following figures of merit, based on transmission line analysis, have been proposed. For an interconnect of length l, inductance has to be considered if:

$$\frac{t_r}{2\sqrt{LC}} < l < \frac{2}{R}\sqrt{\frac{L}{C}}. \tag{1}$$

This range depends upon the parasitic PUL impedances of the interconnect and the rise time of the signal. This range may be nonexistent in certain cases, namely if:

$$t_r > 4\frac{L}{R}. \tag{2}$$

When this condition holds, inductance is not important for any interconnect length [20].

Basically, the abovementioned condition 1 is the conjunction of two rules. The rule on the right side ensures that the equivalent RLC circuit is underdamped. The rule on the left side has been introduced to ensure the waveform agreement between the analytical solutions of the characteristic impedance of the transmission line and its RC approximation [4], [20]. Also, note that the term on the left side, $2\sqrt{LC}l$, is equal to twice the time required by the electromagnetic wave to travel from one end of the line to the other, that is twice the time-of-flight [4]. The process for the selection of an inductive or non-inductive line model can be found in form of an algorithmic scheme in [17], while a more detailed method is presented in [4].

Briefly, we can also say that if the signal propagation delay is much less than the rise time and long lines are too lossy, inductance need not be taken into consideration. In the case of short lines, the propagation time is too small compared to the transition time, and, in general, inductance is not important for any length if the effect of attenuation comes into play before the effect due to the rise time vanishes [20]. Nevertheless, the aforementioned rules are rather loose, and when mutual inductance plays an important role, finding such figures of merits is a very tedious task and still under research.

IV. Simulation Environment

In this section we choose some typical scenarios for global and intermediate buses and we will refer to the previous section in order to choose the most appropriate model. It is of utmost importance to choose an accurate model, however of least possible complexity. We will see in Sections V and VI that the choice of less complex but not accurate enough model can finally lead to completely different results and conclusions.

At high frequencies, each interconnect line exhibits not only an associated self-inductance but also a corresponding mutual inductance to all near and far neighboring lines. Thus, interconnect models evolved from being ignored, to the trivial lumped capacitive model, to the widely used distributed RC model (resistance - capacitance) and later to the distributed RLC model (RC with self-inductance). Nowadays, the mutual inductances are also included in what we call full RLC or $RLMC$ models (RLC with mutual inductance).

In Figure 1, a 3-segment $RLMC$ model for a 5-bit wide interconnect topology is shown. We can observe that for the full $RLMC$ model, we require $N \cdot S$ resistances, $N \cdot S$ self-capacitances, $(N-1) \cdot S$ mutual capacitances, $N \cdot S$ self-inductances, and $N \cdot S(N \cdot S - 1)/2$ mutual inductances, or more precisely, inductive coupling coefficients, where N denotes the number of conductors and S the number of segments, which is increased with increasing wire length to maintain sufficient accuracy. In order to reduce the order of the $RLMC$ model, several methods for making the inductance matrix sparse have been proposed [12]. Nevertheless, in order to avoid stability problems, one has to make sure that the sparsified matrix is positive definite. Since our goal is to employ a precise but not necessarily fast model, Model Order Reduction (MOR) techniques and automatic generation of reduced accurate circuit models for interconnects [27] are beyond the scope of this work. Consequently, we employ the full $RLMC$ model. Eventually, we will show based on the rules of Section III that for the chosen scenarios, this model is the one of least complexity and also high accuracy.

Because of the symmetry of the 5-bit bus structure with respect to the central signal wire, the “first” line may either

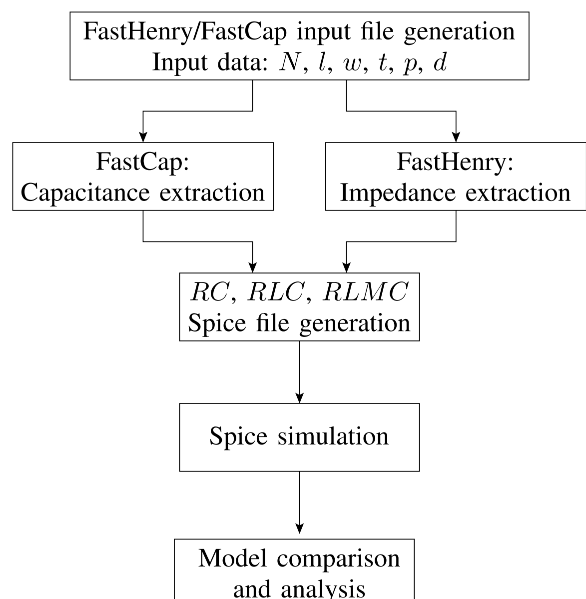


Fig. 2. Parameter Extraction Flow. In addition to material constants for metal (copper) and dielectric (SiO_2) and discretization values for the interconnect structure under consideration, the input data is specified by the number of wires N, wire length l, wire width w, wire thickness t, wire pitch p, and distance between two metal layers d.

be the leftmost or rightmost bit. For convenience, however, the first line will refer to the leftmost bit throughout our discussions.

Classically, the analysis of the total delay induced by a buffer driving an interconnect network has been addressed by splitting the problem into two simpler ones: computation of buffer delay and intrinsic delay through the wire (also referred to as time-of-flight). In order to determine the equivalent delay of a buffer, the complete network is abstracted as an equivalent load. The delay is then a function of the input transition time and that equivalent load. Key elements of this methodology are the estimation of the equivalent (or effective) capacitance and the delay of the wire. When inductive effects appear, this methodology becomes much more complex and is still a matter of research for the CAD community. Some efforts have been put into characterizing the intrinsic delay of a buffer when loading lines are dominated by inductive coupling [21], [28]. In this work, we focus only on the intrinsic delay of the wire.

The inductance of on-chip wires is not scalable with length and no good approximation formula exists for the mutual inductance between two parallel lines of unequal length. Therefore, it is necessary to use a field solver, such as FastHenry, in order to determine the inductive coupling more accurately than with closed-form equations [29].

In this work, we model a 500 µm and a 1000 µm long 5-bit wide bus. Every line has been split into 10 segments. The thickness, width, and spacing of the lines as well as the distance to the lower and upper metal layers are all considered to be 1 µm. The values have been chosen according to the upper layers characteristics of a typical 130 nm 1.8 V technology. They represent typical scenarios for parallel buses in global and intermediate parallel buses, as there can appear, depending on the rise times, significant capacitive and inductive coupling effects (see Section II). Note that, the employed transistor models used to implement the buffers also correspond to such a technological node.

Figure 2 illustrates the parameter extraction flow. FastHenry [30] was used to extract the total resistances and inductances. In order to obtain the required distributed parameter values, the input file for FastHenry has been adapted by splitting the five wires ($N = 5$), each of 1 mm length, into 10 segments ($S = 10$) closely spaced to one another. Thus, 50 resistances, 50 line inductances, and 1225 mutual coupling coefficients have been extracted and written into a SPICE netlist.

The total ground and coupling capacitances have been computed with FastCap [31]. A total of 50 self-capacitances and 40 mutual capacitances have been extracted and afterwards used to complete the aforementioned SPICE netlist.

An approximate range for the driver impedance is of 50 to 300 Ω, as indicated in [17] The lines in our simulations are driven by inverters with 75 Ω output resistance. Note that for lower impedance drivers, there may be a greater need to employ an inductive interconnect model which will become even more apparent in smaller-size VDSM technologies.

At frequencies corresponding to rise times in the order of picoseconds, there may be significant skin depth to be considered [4]. We have therefore performed FastHenry simulations which show the error in extracted interconnect parameters as a function of frequency at increasing values for volume discretization parameters. From these results, it can be seen that for frequencies leading to rise times larger than approximately 25 ps, the influence of the skin effect on extracted interconnect parameters can be neglected—apart from geometry and material constants, this value for the rise times also depends on the desired accuracy of extracted parameters. We have therefore restricted our simulations to rise times larger than 25 ps and present results for 25 ps, 50 ps, 75 ps, and 100 ps, which correspond to significant frequencies of 13.6 GHz, 6.8 GHz, 4.53 GHz, and 3.4 GHz respectively. Note that the highest significant frequency, 13.6 GHz, has a corresponding wavelength of $\lambda = 22.059$ mm, which is much bigger than the maximum simulated interconnect length of 1 mm. Thus, based on the qualitative and quantitative measures given in Section III, we can assume quasi-stationarity without any loss of accuracy and employ the non-retarded PEEC method.

The error involved with various discretizations of conductors into segments was observed in further FastHenry simulations to find the optimal trade-off between accuracy and computation time. From these simulations we have found the number of segments necessary for extracted impedance parameters to converge to their final values within a specified range. As an example, for a simulation in which the number of segments is increased from 1 to 25, the errors in the signal delay computed with the three investigated interconnect models for an input rise time of 25 ps are referenced to the case of an $RLMC$ model with the largest number of segments, considered to be the most precise model in this case. Now, if we specify a maximum value of 1 % for these errors, we find that, modeling the topologies discussed in this text, 7 segments provide sufficient accuracy and may be used for simulation. Because there is not much additional computational overhead involved and above errors can be further reduced, we have chosen 10 segments per wire of 1000 µm length for the scenarios discussed. In this case, we observe a maximum error of 0.6 %.

Nonetheless, the figures of merit proposed for line inductance (see Section III) cannot be directly applied when taking into account inductive coupling. Therefore, we performed SPICE simulations that allow to compare three cases of modeling an interconnect line, namely: a distributed RC line, a distributed simple RLC line without mutual inductances, and a distributed full $RLMC$ line including inductive coupling.

V. Crosstalk and Timing

The electromagnetic fields surrounding each interconnect wire interact with each other and induce undesired signals in all the neighboring lines. When dealing with this unintended interference designers refer to *crosstalk* or *signal integrity*.

A. Coupling Effects

The capacitive coupling effect is a “short-range” effect as only the mutual capacitances between adjacent bus lines

have a significant influence on crosstalk. On the contrary, mutual inductance decays only slowly with bus-line spacing making the inductive effect a “long-range” one [3], [32], [33]. The inductive far-coupling effect can be observed in Figure 3, which depicts the normalized inductive and capacitive coupling between the first and all other lines of a 20-bit wide signal bus for the distributed $RLMC$ model (due to the symmetry of the bus the first may be the leftmost or rightmost bit). This figure clearly shows the rapid drop in capacitive coupling between neighbors of higher order compared to inductive coupling.

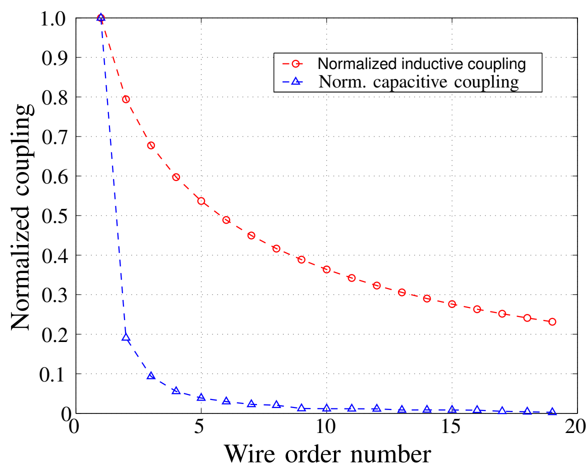
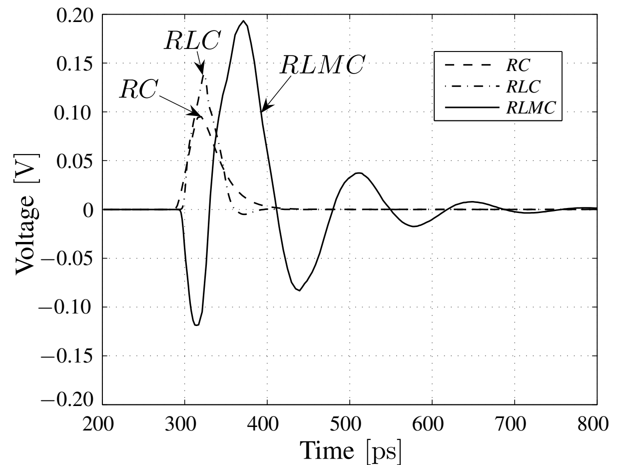


Fig. 3. Long-range effect of inductive coupling versus short-range effect of capacitive coupling. Normalized coupling coefficients illustrated are between the first wire and all neighboring wires.

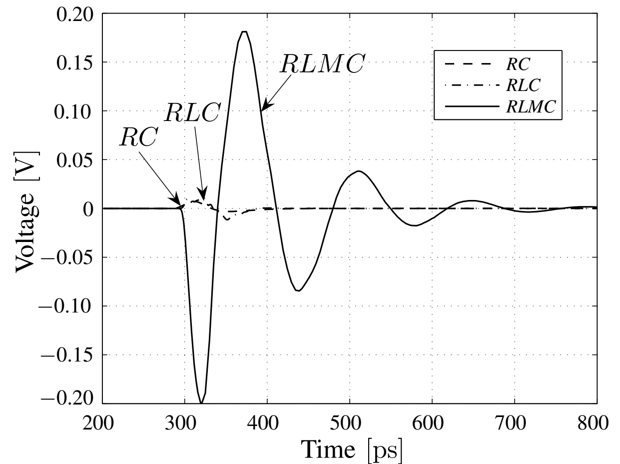
Figure 4 shows simulations of a 5-bit signal bus with four lines held at ground and the remaining neighboring line (aggressor) switching from 0 to 1. The voltage at the far end of the quiet first (leftmost) line is then plotted as a function of time and order of neighboring wire for the three interconnect models investigated. The main conclusion that can be drawn from Figures 4 a), b), and c) is that the simple RLC model cannot accurately estimate crosstalk. Additionally, it can be seen that the influence of capacitive coupling is comparable to that of inductive coupling when the first-order aggressor toggles. Nevertheless, for several transition activity patterns, in the case of a toggle in the fourth-order neighbor, the voltage glitch predicted by inductive coupling may be even more than one order of magnitude larger than the one predicted by the RLC and RC models. More details about crosstalk noise for quiet and switching lines can be found in [4], [34].

B. Signal Delay

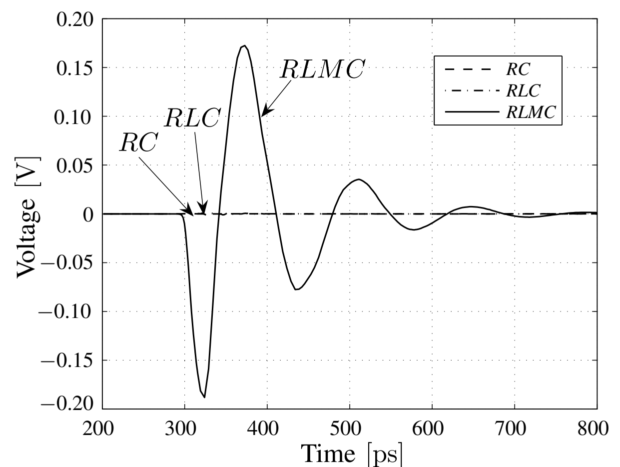
Tables II and III show simulation results for the signal delay in a 5-bit wide bus for the discussed interconnect models as a function of rise times and several switching patterns. From all possible switching patterns we selected only the most representative for different types of overlay between inductive and capacitive coupling, and for the three employed interconnect models. Note that the patterns



(a) Transition from ”00000” to ”01000”.



(b) Transition from ”00000” to ”00100”.



(c) Transition from ”00000” to ”00001”.

Fig. 4. Crosstalk at the far end of the quiet first line (leftmost bit) for a toggling in neighbors of different order with an input signal rise time of 25 ps.

TABLE II

SIGNAL DELAY IN LINE 3 FOR VARIOUS SWITCHING PATTERNS AND RISE TIMES WHEN WIRE LENGTH $l = 500\ \mu\mathrm{m}$.

Rise time	Transition	RC Delay	RLC Delay	$RLMC$ Delay	RC Error		RLC Error	
25 ps	00↑00	8.8 ps	10.3 ps	11.2 ps	−2.4 ps	−21.4 %	−0.9 ps	−8.1 %
	↑↑↑↑↑	7.2 ps	8.6 ps	16.0 ps	−8.8 ps	−55.1 %	−7.4 ps	−46.6 %
	↓↓↑↓↓	10.7 ps	12.4 ps	6.0 ps	4.7 ps	78.8 %	6.4 ps	107.0 %
	↓↑↑↑↓	7.3 ps	8.8 ps	10.0 ps	−2.7 ps	−26.8 %	−1.2 ps	−12.3 %
	↑↓↑↓↑	10.6 ps	12.1 ps	12.7 ps	−2.0 ps	−16.2 %	−0.5 ps	−4.2 %
50 ps	00↑00	9.8 ps	10.1 ps	11.2 ps	−1.4 ps	−12.3 %	−1.1 ps	−9.5 %
	↑↑↑↑↑	7.7 ps	7.7 ps	13.0 ps	−5.3 ps	−40.9 %	−5.3 ps	−40.7 %
	↓↓↑↓↓	11.9 ps	12.5 ps	7.7 ps	4.2 ps	54.2 %	4.7 ps	61.1 %
	↓↑↑↑↓	7.8 ps	7.9 ps	9.5 ps	−1.7 ps	−17.9 %	−1.6 ps	−17.2 %
	↑↓↑↓↑	11.8 ps	12.4 ps	12.9 ps	−1.1 ps	−8.3 %	−0.5 ps	−3.7 %
75 ps	00↑00	10.0 ps	10.1 ps	10.2 ps	−0.2 ps	−2.2 %	−0.1 ps	−1.4 %
	↑↑↑↑↑	7.8 ps	7.7 ps	9.3 ps	−1.5 ps	−16.1 %	−1.6 ps	−16.9 %
	↓↓↑↓↓	12.3 ps	12.4 ps	12.3 ps	−0.1 ps	−0.7 %	0.1 ps	0.7 %
	↓↑↑↑↓	7.8 ps	7.8 ps	8.3 ps	−0.4 ps	−5.3 %	−0.5 ps	−6.1 %
	↑↓↑↓↑	12.2 ps	12.4 ps	12.3 ps	0.0 ps	−0.4 %	0.2 ps	1.3 %
100 ps	00↑00	10.1 ps	10.1 ps	9.5 ps	0.5 ps	5.6 %	0.6 ps	5.9 %
	↑↑↑↑↑	7.8 ps	7.8 ps	5.8 ps	2.0 ps	34.8 %	2.0 ps	35.0 %
	↓↓↑↓↓	12.4 ps	12.4 ps	14.4 ps	−2.0 ps	−14.1 %	−2.0 ps	−14.0 %
	↓↑↑↑↓	7.8 ps	7.7 ps	7.3 ps	0.5 ps	6.7 %	0.4 ps	6.0 %
	↑↓↑↓↑	12.3 ps	12.4 ps	11.8 ps	0.6 ps	4.8 %	0.7 ps	5.6 %

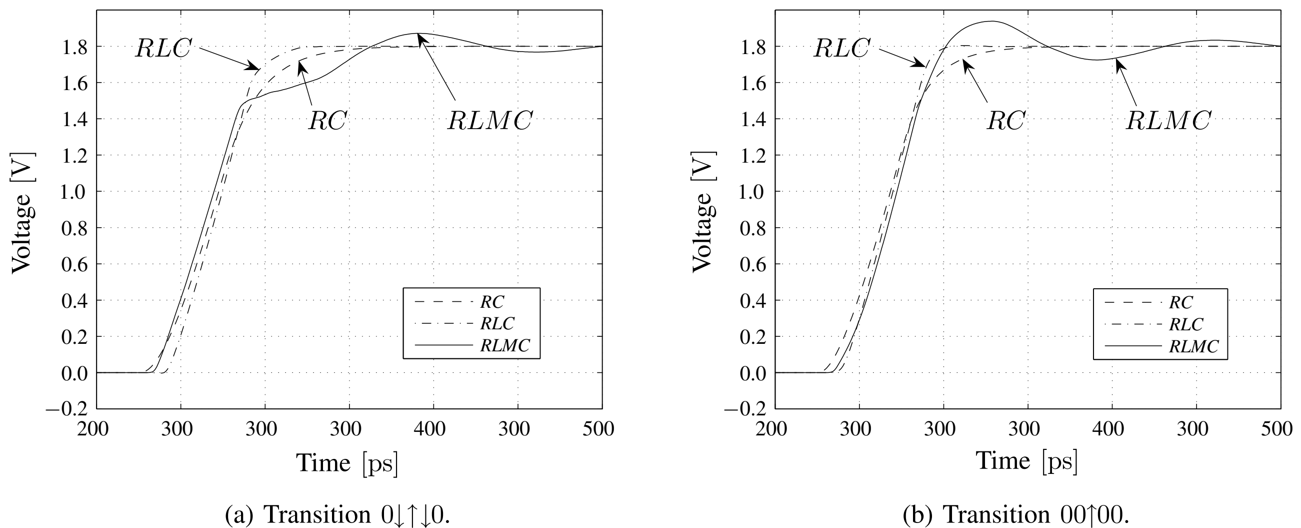
TABLE III

SIGNAL DELAY IN LINE 3 FOR VARIOUS SWITCHING PATTERNS AND RISE TIMES WHEN WIRE LENGTH $l = 1000\ \mu\mathrm{m}$.

Rise time	Transition	RC Delay	RLC Delay	$RLMC$ Delay	RC Error		RLC Error	
25 ps	00↑00	13.5 ps	17.0 ps	18.4 ps	−4.9 ps	−26.7 %	−1.4 ps	−7.5 %
	↑↑↑↑↑	10.5 ps	14.0 ps	27.9 ps	−17.4 ps	−62.2 %	−13.9 ps	−49.9 %
	↓↓↑↓↓	17.4 ps	20.8 ps	9.1 ps	8.4 ps	92.7 %	11.7 ps	129.6 %
	↓↑↑↑↓	11.0 ps	14.4 ps	16.1 ps	−5.1 ps	−31.8 %	−1.7 ps	−10.5 %
	↑↓↑↓↑	16.8 ps	20.1 ps	21.1 ps	−4.3 ps	−20.3 %	−1.0 ps	−4.7 %
50 ps	00↑00	15.4 ps	17.1 ps	19.5 ps	−4.0 ps	−20.7 %	−2.3 ps	−11.9 %
	↑↑↑↑↑	11.7 ps	13.0 ps	26.3 ps	−14.6 ps	−55.5 %	−13.3 ps	−50.6 %
	↓↓↑↓↓	19.7 ps	22.0 ps	9.8 ps	9.9 ps	101.6 %	12.2 ps	125.0 %
	↓↑↑↑↓	12.1 ps	13.6 ps	16.5 ps	−4.4 ps	−26.6 %	−2.9 ps	−17.6 %
	↑↓↑↓↑	19.3 ps	21.5 ps	22.8 ps	−3.5 ps	−15.5 %	−1.4 ps	−5.9 %
75 ps	00↑00	16.3 ps	17.0 ps	19.3 ps	−2.9 ps	−15.3 %	−2.2 ps	−11.5 %
	↑↑↑↑↑	12.0 ps	12.1 ps	23.0 ps	−11.0 ps	−47.7 %	−10.9 ps	−47.3 %
	↓↓↑↓↓	20.8 ps	22.0 ps	12.4 ps	8.5 ps	68.5 %	9.6 ps	78.1 %
	↓↑↑↑↓	12.3 ps	12.5 ps	15.8 ps	−3.4 ps	−21.8 %	−3.3 ps	−21.2 %
	↑↓↑↓↑	20.6 ps	21.8 ps	22.9 ps	−2.4 ps	−10.3 %	−1.1 ps	−4.7 %
100 ps	00↑00	16.7 ps	17.0 ps	18.4 ps	−1.7 ps	−9.0 %	−1.3 ps	−7.2 %
	↑↑↑↑↑	12.1 ps	12.0 ps	18.9 ps	−6.8 ps	−35.8 %	−6.9 ps	−36.5 %
	↓↓↑↓↓	21.4 ps	22.0 ps	17.0 ps	4.3 ps	25.4 %	4.9 ps	28.8 %
	↓↑↑↑↓	12.4 ps	12.2 ps	14.6 ps	−2.2 ps	−15.2 %	−2.4 ps	−16.5 %
	↑↓↑↓↑	21.2 ps	21.9 ps	22.3 ps	−1.1 ps	−4.9 %	−0.4 ps	−1.9 %

correspond to the cases indicated in Section II. The absolute and relative delay error for the RC and RLC models were referenced to the delay obtained by the $RLCM$ model. For further discussions on signal delay and output rise time, Figure 5 shows two particular cases from this set of simulations where the waveform of the voltage at the far end of the third signal wire is plotted against time for all three interconnect models.

The inclusion of line inductance brings to light not only overshoots and undershoots, which introduce large crosstalk noise on neighboring lines, but also the increase of signal delay [4], [11]. Disregarding line inductance generally results in underestimating the delay [11]. Nevertheless, as seen in Figure 5 and in Tables II and III, the propagation delay may increase or decrease compared to the RC model prediction. Moreover, those delays are strongly correlated to the input data pattern [33], [35], [36] and models are required at higher levels of abstraction to include these effects. For this purpose, we have developed a simple linear delay model which accurately predicts signal delay in both



(a) Transition 0↓↑↓0.

(b) Transition 00↑00.

Fig. 5. Effects of switching patterns 0↓↑↓0 and 00↑00 on signal delay and rise and fall times in the third line for RC, RLC, and $RLMC$ modeling.

inductively and capacitively coupled VDSM interconnects in [37].

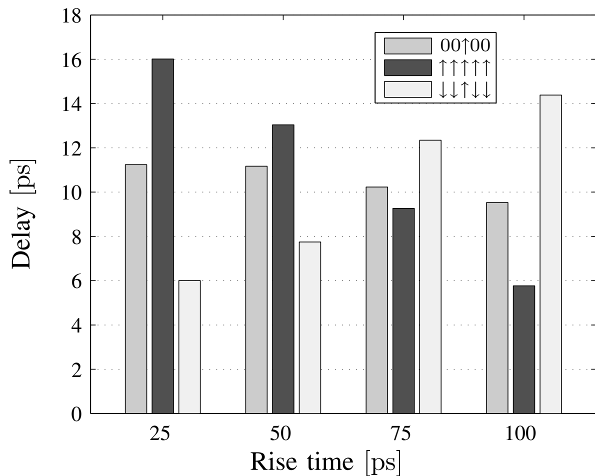
Cao et al. [35] concluded that when taking into account inductive coupling, worst case delay and noise are dominated more by the switching pattern ↑↓↑↓↑ than of the ↓↓↑↓↓ one. Furthermore, Tu et al. [36] showed that the former switching pattern becomes the worst case scenario with increasing wire capacitance. However, for smaller coupling capacitance the worst case pattern was reported to change to ↑↑↑↑↑.

Tables II and III show that, for our simulation settings, the best case switching patterns for the RC model are the worst case patterns for the $RLMC$ model and vice-versa. Depending on the switching pattern, the simple RLC model is closer to either the RC or $RLMC$ model. The signal delay is predicted by the RC model with an error varying between –55.1 % and 78.8 % for $l = 500$ µm and between –62.2 % and 101.6 % for $l = 1000$ µm with respect to the $RLMC$ model.

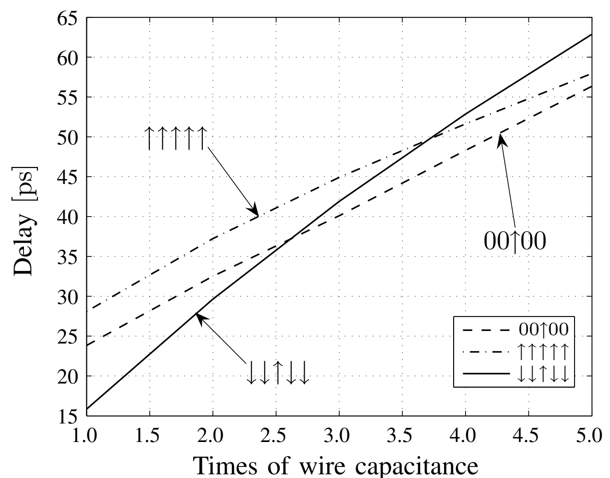
In the case of capacitively dominated coupling, a transition in an aggressor in the opposite direction increases the total capacitance that the victim has to charge and the transition is thus slowed down. On the contrary, in inductively coupling dominated lines, a transition of an aggressor in the same direction induces a current flowing in the opposite direction to the one in the victim line. Consequently, the effective current decreases and the delay increases.

Using data from Table II, Figure 6 a) shows a bar plot of the signal delay for three different values for the input rise time. The three patterns depicted were chosen based on the following reasoning: the first pattern, 00↑00, included as a reference, is considered to be a "neutral" case which does not have a significant impact on signal delay. The second pattern, ↑↑↑↑↑, is the best case pattern for the signal delay predicted by the RC model, but the worst case for a highly inductive $RLMC$ interconnect system. The opposite holds for the switching pattern ↓↓↑↓↓, which is the best case for the $RLMC$ model, but the worst case for the RC model. For the sake of completeness, it is also important to mention here, that the value of the far-end load capacitance may significantly influence the inductive behavior of the line as indicated in Section III.

Because inductance effects generally become less important with decreasing signal frequencies, one would expect a change in the worst case switching patterns for the $RLMC$ model with varying frequencies. This situation is indicated in Figure 6 a). In this figure, we can observe a decrease in the signal delay caused by the pattern ↑↑↑↑↑ and an increase in the signal delay due to the pattern ↓↓↑↓↓ with increasing rise times and, thus, decreasing significant frequencies. A different approach to show this change in worst case patterns for the $RLMC$ model is indicated by Figure 6 b). In this figure, the input rise time is held at a constant value while the ground and coupling capacitances in the netlist used for SPICE simulations are successively increased from their original values up to five times that value. On the one hand, one can observe the expected general increase in signal delay with increasing capacitances. On the other hand, one can see that the delay caused by the pattern ↓↓↑↓↓ takes over the delay caused by ↑↑↑↑↑ at a certain point, thus clearly showing the greater impact of capacitance than inductance on timing from this point onward. The technological reason behind such an increase in capacitance, particularly in the case of coupling capacitance, is the aforementioned interconnect scaling. Because scaling has a more significant influence on the lateral dimensions of interconnects, the aspect ratio between adjacent signal wires tends to increase and, thus, does the capacitive coupling between these wires for local interconnect. However, for global wires the width tends to be increased, thereby reducing their resistance and resulting in a more inductive behavior. As already discussed in Section II, one can basically differentiate between three different cases in terms of strength and nature of coupling for global and intermediate interconnects, and Figures 6 a) and b) are also shown to provide more insight into this issue.



(a) Bar plot illustrating the change in the worst case pattern with increasing rise time.



(b) Delay versus wire capacitance for different worst case signal patterns.

Fig. 6. Effects of rise time and wire capacitance on worst case switching patterns and signal delay for the $RLMC$ model.

C. Rise and Fall Times

Previous work showed that when including in the employed interconnect models only line inductances, the rise and fall times of the signal waveforms improve as the inductance effects increase [11]. Nevertheless, when taking into account the coupling inductance, the statement does not hold. The rise time has been computed as the difference between the time instances when the signal reaches 90% and 10% of the final value, respectively.

Table IV and Figure 5 show opposite effects with respect to different lines in the case of the same data toggling context. For instance, in the first case, the rise time in line 3 is predicted with an error of 17.42% by the RC model while in the second case, the introduced error is –31.40%. Thus, rise and fall times (and hence short-circuit induced power consumption) strongly depend on the data toggling pattern. It is important to add that RLC models generally fail to accurately predict rise and fall times and introduce significant errors. Consequently, the inclusion of inductive coupling in the interconnect model is of paramount importance for accurate rise time estimation.

VI. Power Consumption

According to the dependency on the temporal variation of the input signals, power consumption in digital CMOS circuits can be classified in two main categories, namely dynamic power consumption and static power consumption. Dynamic power consumption arises from the transient behavior of the input signals and is associated with two main phenomena: the capacitive switching current caused by the loading and unloading of internal capacitances, and the short-circuit current generated when a direct path between the supply voltage and ground appears. Moreover, VDSM CMOS technologies exhibit a steady leakage current even when transitions do not occur [38]. Nonetheless, this component of power consumption is still small in the case of interconnects in a 130 nm technological node, so it is not taken into consideration in this work.

TABLE IV
Output rise times for line 3 for input rise times of 50 ps.

Transition	RC	RLC	$RLMC$
00↑00	54.6 ps	41.1 ps	46.5 ps
0↓↑↓0	61.4 ps	43.7 ps	89.5 ps
↓↓↑↓↓	60.6 ps	43.2 ps	11.0 ps
↓↑↑↑↓	46.9 ps	38.2 ps	41.6 ps
↑↓↑↓↑	62.3 ps	44.2 ps	50.9 ps
↑↑↑↑↑	47.2 ps	38.3 ps	32.4 ps

The switching component of power dissipation corresponds to the amount of energy needed to completely charge the parasitic capacitors and is given by fCV_{dd}^2, where f is the switching frequency, C indicates the parasitic capacitors, and V_{dd} denotes the power supply. However, this is true only when the transient state is over. Otherwise, there is still a current flowing through the inductances when the next transition occurs, the voltage on the capacitors is not necessarily settled, and therefore some energy is stored in these elements. Simulations showed, that in the case of an $RLMC$ interconnect model, very small differences in the switching power dissipated exclusively in the lines may appear. Nevertheless, those discrepancies are getting important only when switching occurs very fast. In those situations, our simulations showed that the signals are degraded to such an extent which makes them unacceptable anyway. In brief, we can say that switching power consumption does not depend on inductive effects, but only on the ground and coupling capacitance [3].

For the purpose of analyzing the power consumption in interconnects, inductive effects can be neglected. Let us therefore consider, an interconnect structure modeled by an RC network. Assuming that the wires toggle synchronously with a complete swing of the supply voltage, V_{dd}, the mean

energy consumption, $\hat{E}_i$, in line i can be written as:

$$\hat{E}_i = \frac{V_{dd}^2}{2}\big(C_{gnd}lt_t + 2C_clt_s\big), \quad (3)$$

where l is the length of the lines and

$$t_t = 2E\big[b_i^+\Delta b_i\big] \quad (4)$$

$$t_s = E\big[b_i^+(2\Delta b_i - \Delta b_{i-1} - \Delta b_{i+1})\big] \quad (5)$$

are, as defined in [39], the temporal transition activity responsible for charging and discharging the PUL capacitance C_{gnd} and the spatial equivalent activity which is responsible for charging and discharging the PUL capacitance C_c respectively. Basically, because of the capacitive coupling, more capacitance needs to be charged and discharged than just the ground capacitance when a toggle occurs. However, depending on the toggling or non-toggling on the line itself and on the first order neighbors, a driver of a line could consume a maximum of energy for charging four times the coupling capacitance or receive an energy equivalent to charging two times the coupling capacitance. As mentioned in [3], the power consumption due to capacitive coupling in non-synchronously toggling interconnects is slightly smaller because of the induced dynamic delay.

The switching component of power consumption is independent of the rise and fall times of the input waveforms. However, direct current paths between V_{dd} and ground appear exactly during the rise and the fall of input signals. The short-circuit power can be approximated in first term by:

$$P_{sc} = \frac{\beta}{12}\,(V_{dd} - V_{THn} - |V_{THp}|)^3\,\tau\,\frac{t_t}{T}\,, \quad (6)$$

where T is the clock period, τ is the transition time of the input signal at the load gate, V_{THn} and V_{THp} are the threshold voltages of the NMOS and the PMOS transistors, respectively, and β is a technological parameter which has a very small dependence on τ [5], [38]–[42].

For interconnects modeled only by line inductances, previous work showed that the rise and fall times of signal waveforms improve as the inductance effects increase [11]. Nevertheless, when taking into account the coupling inductance, the statement does not remain true. As previously mentioned, Table IV and Figure 5 show opposite effects with respect to different bus models in the case of the same data toggling context.

Because of important overshoots and undershoots, simulations proved that the overall short-circuit power consumption does not necessarily have to decrease, as spurious short-circuit currents can appear whenever a sufficiently big spike opens the complementary transistors [33].

In order to assure high performance, long resistive interconnects are driven by repeaters. Those repeaters are generally large gates and are responsible for a notable part of the total power consumption. When not taking into account the mutual inductances, as line inductance effects increase, the optimum number of repeaters for minimum propagation delay decreases [5], [11]. Moreover, fewer and smaller repeaters result in a significant reduction of the dynamic power consumption in the repeaters. Nonetheless, as seen in section V, the worst case signal delay predicted by an $RLMC$ interconnect model degrades dramatically compared to the signal delay resulted in simulations of an RLC model. Thus, in inductively coupled on-chip interconnects, the optimum number of repeaters is generally higher than the number predicted by an RLC model and the expected savings in area and power consumption are therefore too optimistic.

VII. Concluding Remarks

This paper analyzed the effects on timing and power consumption in typical global and intermediate parallel buses when taking into account both inductive and capacitive coupling between the lines of the bus. We compared the results of three sets of simulations for three different distributed bus models: RC, RLC, and $RLMC$. For the third set of simulations, a full $RLMC$ model was used, allowing thus to run very accurate simulations.

For parameters like crosstalk, signal delay, rise and fall times serious errors of the RC and RLC models with respect to the $RLMC$ one have been reported. Those models introduce important errors in predicting the most important crosstalk and timing related parameters, which strongly depend on the transition activity pattern. Moreover, the worst case and best case switching patterns are not only different for the three models, but also depend on the geometrical interconnect structure. The power consumption however, is barely affected by inductive coupling effects with the exception of short-circuit power consumption, which actually represents a small fraction of the total switching power.

The worst and best case switching patterns for those parameters differ significantly as a function of the employed interconnect model and that simple models including only coupling capacitances and line inductances fail to accurately predict the worst and best cases for the toggling patterns. Because of the different possible magnitude of the two couplings, the worst case and best case toggling patterns vary in a very complex manner. Hence, we considered various scenarios, such that inductive and capacitive coupling can interact in several ways and produce therefore different worst and best case toggling patterns. The characteristics of this overlay is decisive in finding the best and worst case pattern. In addition, we have shown that the figures of merit developed for line inductance do not hold when inductive coupling becomes important and more conservative rules should be used in this case for the selection of an accurate model.

References

[1] J. D. Meindl, "Beyond Moore's Law: The Interconnect Era," *Computing in Science & Engineering*, vol. 5, no. 1, pp. 20 – 24, Jan.-Feb. 2003.

[2] R. Achar and M. S. Nakhla, "Simulation of High-Speed Interconnects," *Proceedings of the IEEE*, vol. 89, no. 5, pp. 693–728, May 2001.

[3] A. García Ortiz, T. Murgan, L. D. Kabulepa, L. S. Indrusiak, and M. Glesner, "High-Level Estimation of Power Consumption in Point-to-Point Interconnect Architectures," *Journal of Integrated Circuits and Systems*, vol. 1, no. 1, pp. 23–31, March 2004.

[4] C.-K. Cheng, J. Lillis, S. Lin, and N. Chang, *Interconnect Analysis and Synthesis*. New York: John Wiley & Sons, 2000.

[5] Y. I. Ismail and E. G. Friedman, *On-Chip Inductance in High Speed Integrated Circuits*. Boston: Kluwer, 2001.

[6] W. H. Kao, C.-Y. Lo, M. Basel, and R. Singh, "Parasitic Extraction: Current State of the Art and Future Trends," *Proceedings of the IEEE*, vol. 89, no. 5, pp. 729–739, May 2001.

[7] D. Sylvester and C. Hu, "Analytical Modeling and Characterization of Deep-Submicrometer Interconnect," *Proceedings of the IEEE*, vol. 89, no. 5, pp. 634–664, May 2001.

[8] D. Sylvester and K. Keutzer, "Impact of Small Process Geometries on Microarchitectures in Systems on a Chip," *Proceedings of the IEEE*, vol. 89, no. 4, pp. 467 – 489, April 2001.

[9] A. E. Ruehli, "Inductance Calculation in a Complex Integrated Circuit Environment," *IBM Journal on Research and Development*, vol. 16, pp. 470–481, September 1972.

[10] K. Gala, V. Zolotov, R. Panda, B. Young, J. Wang, and D. Blaauw, "On-Chip Inductance Modeling and Analysis," in *Design Automation Conf. (DAC)*, Los Angeles, California, June 2000, pp. 63 – 68.

[11] Y. Massoud and Y. Ismail, "Grasping the Impact of On-Chip Inductance," *IEEE Circuits & Devices Magazine*, vol. 17, no. 4, pp. 14–21, July 2001.

[12] K. Gala, D. Blaauw, J. Wang, V. Zolotov, and M. Zhao, "Inductance 101: Analysis and Design Issues," in *Design Automation Conf. (DAC)*, Las Vegas, Nevada, June 2001, pp. 329–334.

[13] Y. Massoud, S. Majors, J. Kawa, T. Bustami, D. MacMillen, and J. White, "Managing On-Chip Inductive Effects," *IEEE Trans. on Very Large Scale Integration (VLSI) Systems*, vol. 10, no. 6, pp. 789–798, December 2002.

[14] H. Kaul, D. Sylvester, and D. Blaauw, "Performance Optimization of Critical Nets Through Active Shielding," *IEEE Trans. on Circuits and Systems I: Regular Papers*, vol. 51, no. 12, pp. 2417–2435, December 2004.

[15] J. Nurmi, H. Tenhunen, J. Isoaho, and A. Jantsch, Eds., *Interconnect-Centric Design for Advanced SoC and NoC*. Dordrecht: Kluwer, 2004.

[16] A. E. Ruehli and A. C. Cangellaris, "Progress in the Methodologies for the Electrical Modeling of Interconnects and Electronic Packages," *Proceedings of the IEEE*, vol. 89, no. 5, pp. 740–771, 2001.

[17] F. Moll and M. Roca, *Interconnection Noise in VLSI Circuits*. Dordrecht: Kluwer, 2004.

[18] C. R. Paul, *Analysis of Multiconductor Transmission Lines*. New York: John Wiley & Sons, 1994.

[19] A. E. Ruehli and H. Heeb, "Challenges and Advances in Electrical Interconnect Analysis," in *Design Automation Conf. (DAC)*, Anaheim, California, June 1992, pp. 460–465.

[20] Y. Ismail, E. G. Friedmann, and J. L. Neves, "Figures of Merit to Characterize the Importance of On-Chip Inductance," *IEEE Trans. on Very Large Scale Integration (VLSI) Systems*, vol. 7, pp. 442–449, December 1999.

[21] M. Celik, L. Pileggi, and A. Odabasioglu, *IC Interconnect Analysis*. Boston: Kluwer, 1996.

[22] H. B. Bakoglu, *Circuits, Interconnections, and Packaging for VLSI*. Addison Wesley, 1990.

[23] J. A. Davis and J. D. Meindl, Eds., *Interconnect Technology and Design for Gigascale Integration*. Boston: Kluwer, 2003.

[24] A. Deutsch, P. W. Coteus, G. V. Kopcsay, H. H. Smith, C. W. Surovic, B. L. Krauter, D. C. Edelstein, and P. J. Restle, "On-Chip Wiring Design Challenges for Gigahertz Operation," *Proceedings of the IEEE*, vol. 89, no. 5, pp. 529–555, May 2001.

[25] D. Pamunuwa, "Modelling and Analysis of Interconnects for Deep Submicron Systems-on-Chip," Ph.D. dissertation, Royal Inst. of Technology, Stockholm, Sweden, 2003.

[26] M. A. El-Moursy and E. G. Friedman, *Interconnect-Centric Design for Advanced SoC and NoC*. Dordrecht: Kluwer, 2004, ch. 4 - Design Methodologies for On-Chip Inductive Interconnects, pp. 85–124.

[27] M. Kamon, N. A. Marques, L. M. Silveira, and J. White, "Automatic Generation of Accurate Circuit Models of 3-D Interconnect," *IEEE Trans. on Components, Packaging, and Manufacturing Technology - Part B*, vol. 21, no. 3, pp. 225–240, August 1998.

[28] S. Sapatnekar, *Timing*. Boston: Kluwer Academic Publishers, 2004.

[29] S. Lin, N. Chang, and S. Nakagawa, "Quick On-Chip Self- and Mutual-Inductance Screen," in *Intl. Symp. on Quality Electronic Design*, San Jose, California, March 2000, pp. 513–520.

[30] M. Kamon, M. Tsuk, and J. White, "FastHenry: A Multipole-Accelerated 3D Inductance Extraction Program," *IEEE Trans. on Microwave Theory and Techniques*, vol. 42, no. 9, pp. 1750–1758, September 1994.

[31] K. Nabors and J. White, "FastCap: A Multipole-Accelerated 3D Capacitance Extraction Program," *IEEE Trans. on Computer-Aided Design (CAD) of Integrated Circuits and Systems*, vol. 10, no. 11, pp. 1447–1459, November 1991.

[32] L. He, N. Chang, S. Lin, and O. S. Nakagawa, "An Efficient Inductance Modeling for On-Chip Interconnects," in *IEEE Custom Integrated Circuits Conf.*, San Diego, CA, May 1999, pp. 457–460.

[33] T. Murgan, A. García Ortiz, C. Schlachta, H. Zimmer, M. Petrov, and M. Glesner, "On Timing and Power Consumption in Inductively Coupled On-Chip Interconnects," in *Intl. Workshop on Power and Timing Modeling, Optimization and Simulation (PATMOS)*, Santorini, Greece, September 2004, pp. 819–828.

[34] J. Chen and L. He, "Determination of Worst-Case Crosstalk Noise for Non-Switching Victims in GHz+ Interconnects," in *Asia and South Pacific Design Automation Conf. (ASPDAC)*, Kitakyushu, Japan, January 2003, pp. 162–167.

[35] Y. Cao, X. Huang, N. H. Chang, S. Lin, O. S. Nakagawa, W. Xie, D. Sylvester, and C. Hu, "Effective On-Chip Inductance Modeling for Multiple Signal Lines and Application to Repeater Insertion," *IEEE Trans. on Very Large Scale Integration (VLSI) Systems*, vol. 10, no. 6, pp. 799–805, December 2002.

[36] S.-W. Tu, J.-Y. Jou, and Y.-W. Chang, "RLC Effects on Worst-Case Switching Pattern for On-Chip Buses," in *Intl. Symp. on Circuits and Systems (ISCAS)*, vol. 2, Vancouver, Canada, May 2004, pp. 945–948.

[37] T. Murgan, A. García Ortiz, M. Petrov, and M. Glesner, "A Linear Model for High-Level Delay Estimation in VDSM On-Chip Interconnects," in *Intl. Symp. on Circuits and Systems (ISCAS)*, Kobe, Japan, May 2005.

[38] A. P. Chandrakasan and R. W. Brodersen, *Low Power Digital CMOS Design*. Norwell, Massachusetts: Kluwer, 1995.

[39] A. García Ortiz, "Stochastic Data Models for Power Estimation at High-Levels of Abstraction," Ph.D. dissertation, Darmstadt Univ. of Technology, Germany, 2003.

[40] M. A. El-Moursy and E. G. Friedman, "Inductive Interconnect Width Optimization for Low Power," in *Intl. Symp. on Circuits and Systems (ISCAS)*, vol. 5, Bangkok, Thailand, May 2003, pp. 273–276.

[41] Y. I. Ismail, E. G. Friedman, and J. L. Neves, "Dynamic and Short-Circuit Power of CMOS Gates Driving Lossless Transmission Lines," *IEEE Trans. on Circuits and Systems I: Fundamental Theory and Applications*, vol. 46, no. 8, pp. 950–961, August 1999.

[42] W. Nebel and J. Mermet, Eds., *Low Power Design in Deep Submicron Electronics*. Kluwer, 1997.