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System-in-Package for IoT Sigfox Applications

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“I have not failed...

I’ve just found 10,000 ways that won’t work.”

— Thomas A. Edison

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ABSTRACT

In this work, the System-in-Package (SiP) electronic circuit manufacturing technology is presented as an economically viable alternative for implementing solutions where circuits processed in different technologies need to be integrated into a single, compact device. This technology is explored here through the development of a complete hardware platform designed for implementing devices for the Internet of Things (IoT) in the SigFox standard. The platform consists of an RF front-end module, a sub-GHz radio transceiver capable of operating in any global SigFox configuration, and an ARM M0+ microcontroller with 64 Kbytes of Flash memory, 8 Kbytes of RAM, a 2Kbyte EEPROM, a 12-bit 1.14Msps analog-to-digital multi-channel interface, a 12-bit digital-to-analog interface, ultra-low-power comparators for implementing a wake-up system, and a complete set of digital communication peripherals. In addition to this SiP, only a power source (e.g. two AAA batteries) and an antenna are required to implement applications on the SigFox network.

The system integrates an MCU, a radio transceiver, and an RF front-end module, enabling global operation of this device through Sigfox Monarch technology. The SiP operates from a supply voltage of 2.7-3.6 V, and its RF output power is programmable in the range of -30 dBm to 26 dBm. Operating at a supply voltage of 3.3V, it consumes 188.5 mA or 23 mA for RF output power of 22 dBm or 12.8 dBm, at 902.2MHz and 868.13 MHz, respectively. The device also offers a current consumption of 3 μ A in deep sleep mode. The proposed SiP design has successfully met all the requirements for Sigfox Verified certification, enabling the Sigfox Monarch function as well. Currently, it represents the solution with the smallest dimensions approved for Sigfox in the global market, measuring only 13 mm $\times$ 13 mm $\times$ 1.1 mm.

Keywords: Packaging. System-in-Package. Internet of Things. Sigfox.

RESUMO

Neste trabalho é apresentada a tecnologia de fabricação de circuitos eletrônicos System-in-Package (SiP), que se oferece como uma alternativa economicamente interessante para a implementação de soluções, onde circuitos processados em tecnologias diversas devem ser integrados em um único dispositivo de tamanho mínimo. Esta tecnologia é aqui explorada através do desenvolvimento de uma plataforma completa de hardware, voltada à implementação de dispositivos para a Internet das Coisas (IoT) no padrão SigFox. Esta plataforma é composta por um módulo *front-end* de RF, um rádio transceptor sub-GHz, capaz de operar em qualquer configuração global do padrão SigFox, além de um microcontrolador ARM M0+, com 64 Kbytes de memória Flash, 8 Kbytes de memória RAM, uma EEPROM de 2Kbytes, interface multi-canal analógico-digital de 12 bits e 1.14Msps, interface digital-analógico de 12 bits, comparadores ultra-low-power para implementação de um sistema de wake-up e linha completa de periféricos de comunicação digital. Além deste SiP, é necessário apenas a conexão de uma fonte de energia (bateria ou 2 pilhas AAA) e de uma antena, para implementar aplicações ma rede SigFox.

O sistema integra uma MCU, um rádio transceptor e um módulo *front-end* de RF, que habilita a operação global deste dispositivo através da tecnologia Sigfox Monarch. O SiP trabalha a partir de uma tensão de alimentação de 2.7-3.6 V e sua potência de saída de RF é programável na faixa de -30 dBm até 26 dBm. Operando com uma tensão de alimentação de 3.3V, ele consome 188.5 mA ou 23 mA para a potência de saída de RF de 22 dBm ou 12.8 dBm, em 902.2MHz e 868.13 MHz respectivamente. O dispositivo também oferece um consumo de corrente de 3 μA no modo *deep sleep*. O *design* de SiP proposto, atingiu todos os requisitos da certificação Sigfox Verified com sucesso, habilitando também a função Sigfox Monarch, representando atualmente a solução com as menores dimensões homologada para SigFox no mercado mundial, com apenas 13 mm $\times$ 13 mm $\times$ 1.1 mm.

Palavras-chave: Encapsulamento, System-in-Package, Internet das Coisas, Sigfox.

LIST OF ABBREVIATIONS AND ACRONYMS

SiP	System-in-Package
IoT	Internet of Things
IC	Integrated Circuit
PCB	Printed Circuit Board
THT	Through Hole Technology
TO	Transistor Outline
DIP	Dual-in-Line Package
SMT	Surface Mount Technology
SMD	Surface Mount Devices
SOT	Small Outline Transistor
SOP	Small Outline Package
PLCC	Plastic Leaded Chip Carrier
QFP	Quad Flat Package
QFN	Quad Flat No-Lead Package
BGA	Ball Grid Array
WL-CSP	Wafer-Level Chip-Scale Package
CSP	Chip-Scale Package
MCM	Multi-Chip Modules
RF	Radio Frequency
MEMS	Micro-Electro-Mechanical Systems
SoP	System-on-Package
SoC	System-on-Chip
NRE	Non-Recurring Engineering
R&D	Research and Development

LGA	Land Grid Array
CTE	Coefficient of Thermal Expansion
BT	Bismaleimide Triazine
FR4	Flame-Retardant 4
SMA	Surface Mount Assembly
UV	Ultraviolet
CMP	Chemical and Mechanical Polishing
DI	Deionized
KGD	Known Good Dies
RoHS	Restriction of Certain Hazardous Substances
EFO	Electronic Flame Off
EMC	Epoxy Mold Compound
MAP	Molded Array Packages
FDA	Food and Drug Administration
AiP	Antenna-in-package
OPA	Optical Phased Arrays
ASIC	Application-Specific Integrated Circuit
LiDAR	Light Detection and Ranging
TIA	Trans-Impedance Amplifier
SPAD	Single-Photon Avalanche Diode
DAF	Die Attach Film
LCP	Liquid Crystal Polymer
LPWAN	Low Power Wide Area Network
ISM	Industrial, Scientific and Medical
GSM	Global System for Mobile Communications
LTE	Long Term Evolution

CSS	Chirp Spread Spectrum
UNB	Ultra Narrouw Band
RC	Radio Configuration
M2M	Machine-to-Machine
QoS	Quality of Service
PoC	Proce of Concept
LVS	Layout-Versus-Schematic
BOM	Bill Of Materials
OEM	Original Equipment Manufacturer
SO	Sigfox Operator
MOQ	Minimum Order Quantity
ETSI	e European Telecommunications Standards Institute
LBT	Listen Before Talk
EIRP	Effective Isotropic Radiated Power
PER	Package Error Rate
OOK	On-Off Keying
ID	Device Identifier
ECC	Error Correcting Code
FCS	Frame Check Sequence
PA	Power Amplifier
LNA	Low Noise Amplifier
FEM	Front-End Module
XTAL	Crystal Oscillator
GPIO	General Purpose Input/Output
SPI	Serial Peripheral Interface
NSMD	Non Solder Mask Defined

LSB	Least Significant Bit
ADC	Analog to digital converter
DAC	Digital to Analog converter
HP	High Power
BALUN	Balanced-Unbalanced
VNA	Vector Network Analyzer
APD	Allegro Package Design
CPWG	Grounded Coplanar Waveguide
ADS	Advanced Design System
GSG	Ground-Signal-Ground
IF	Intermediate Frequency
SMU	Source and Measure Unit
DUT	Device Under Test
ANATEL	National Agency of Telecommunications

LIST OF SYMBOLS

T_g	Glass Transition Temperature
ε	Dielectric Constant or Permittivity
ε_r	Dielectric Constant in relation to the permittivity of a vacuum
ε_o	Permittivity of a Vacuum
$\tan\delta$	Dissipation Factor or Loss Tangent
TS_{UL}	Duration of an uplink symbol
Z_0	Transmission Line Characteristic Impedance

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1 INTRODUCTION

In the last decades, semiconductor devices enabled the continuous development of technologies that improve the quality of life for the whole world population (WAC et al., 2015). Today is hard to imagine our lives without a computer, a piece of information that does not travel the world in seconds, or a surgeon on a surgical intervention without the support of its specific equipment. The need for improvement in the quality of life made the semiconductor industry develop intensely during this period, and consequently, as packaging technologies. This work will discuss the System-in-Package (SiP) technology and the design of a product based on it.

1.1 The need for Advanced Packaging Technologies

A business case commonly drives new semiconductor product development, and the expected large volumes for Internet of Things (IoT) devices have been driving the electronics devices market (LEA, 2018) and consequently the semiconductor industry. In this market, it is always desirable to have low-cost end devices to enable most high-volume applications.

Since the first transistor was developed in 1947 (SHOCKLEY, 1984), semiconductors rapidly evolved into a key enabler for technology in our society. In 1965, Gordon Moore conducted a study predicting that the number of transistors on a silicon chip would double approximately every two years. This study was known as Moore's Law (MOORE et al., 1965). After that, referred to as scaling, the transistor size is reduced in each successive generation of process technology and has been used to set targets in the semiconductor industry for integrated circuits (ICs) over the last six decades (TUMMALA, 2019). However, this paradigm is ending for technical and economic reasons. The physical limitations of feature size down to a few nanometers and approaching atomic dimensions makes the cost of processing a Si wafer rocket. The semiconductor industry has concluded that beyond 14 nm (Fig. 1.1), there was minimal or no cost reduction as the next technology node was introduced (KEYES, 2005). Fig. 1.1 shows the transistor relative cost for different CMOS technologies nodes.

A new industry trend rises where the added value to devices is provided by incorporating functionalities (generally non-digital) that do not necessarily scale according to "Moore's Law". It may complement digital signal and data processing, including in-

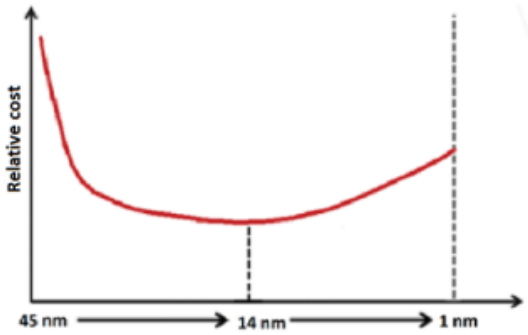

Figure 1.1 – Relative transistor manufacturing cost. **Source:** (TUMMALA, 2019)

teracting with the outside world through sensors, actuators, and subsystems for powering the product or enabling wireless capabilities. These functions may incorporate passive, high-voltage, micro-mechanical components, etc. This new direction, named "More than Moore" (ZHANG; ROOSMALEN, 2010), combines the heterogeneous integration of devices lying outside the chips. This feature has attracted more attention in recent years and has become widely used in industry (LI, 2017). It adds value to the product from a different perspective, and the packaging solutions play an essential role.

1.2 Packaging Solutions

There are many kinds of packaging. Considering the material, it could be a ceramic package, metal package, or plastic package. Ceramic and metal packages are primarily used in aerospace and military industries. In contrast, the plastic package is used for typical applications with lower cost (providing market advantage) and relatively lower reliability. The package forms electrical and mechanical connections between the microelectronic devices and the external peripherals. The package pins connect the chips to other devices using the traces, or copper, in the printed circuit boards (PCBs) for electronic system. Providing environment protection to the chips and components, dissipating heat, guaranteeing power supply, and signals proper operation are the main functions of an electronic package (TUMMALA, 2001).

The history of electronic packaging starts with the through hole technology (THT), which requires drilling a hole for each package pin. At this time, each pin occupies space on both sides of the PCBs. The first package developed dates back to 1955 (BOTTI, 2006), was the Transistor Outline (TO) package. Dual-in-Line Packages (DIP) appeared right after the ICs in the 1960s, providing the traditional THT pin space of 2.54mm. In the

80s, surface-mount technology (SMT) had drastically changed electronic products. Devices are mounted directly onto the PCB surface, called surface-mount devices (SMD). The SMT allows higher manufacturing automation, lower costs, improved quality, and lower area usage for electrical components (TUMMALA; RYMASZEWSKI; KLOPFENSTEIN, 2013). By the 1990s, the SMT had gained popularity and was used in most high-tech electronic products. There were developed a lot of different types of SMD packages as the small outline transistor (SOT), the small outline package (SOP), the plastic leaded chip carrier (PLCC), quad flat package (QFP), etc. In order to reduce the parasitic effect of pins and improve high-frequency signals performance, the leads were removed, evolving to the quad flat no-lead (QFN) package (LI, 2017). As semiconductor technologies advance, the package pin density increases, and the number of pins increases, leading to the ball grid array (BGA) package. A BGA can provide more interconnection pins since the whole bottom surface of the device can be used. The package pins replaces the pads on the bottom of the package, each with a tiny solder ball. Figure 1.2 gives a visual representation of some common packages types.

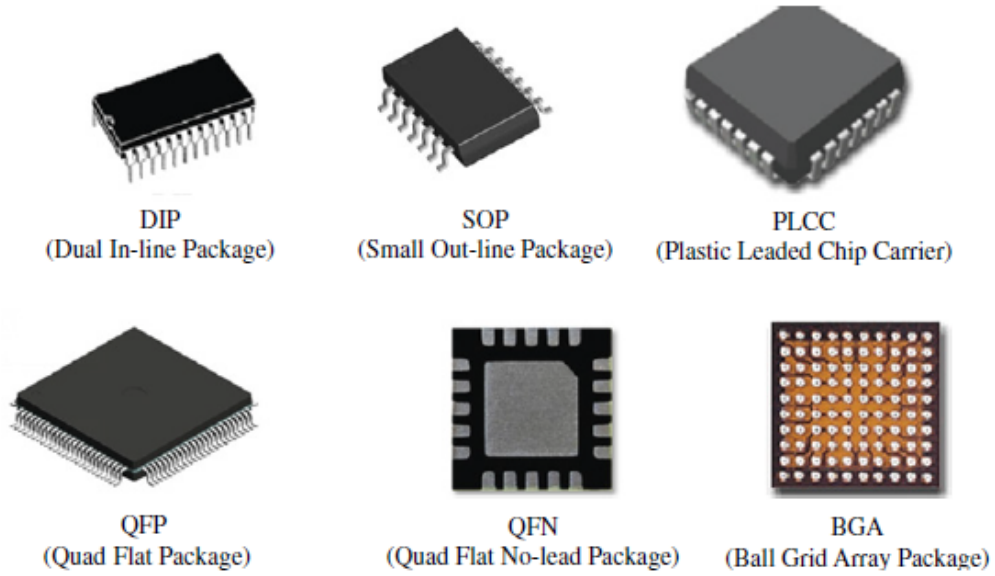

Figure 1.2 – Common Packages Types. **Source:** (LI, 2017)

Following the BGA trend, in the wafer-level chip-scale package (WL-CSP or simply CSP), the die is mounted on an interposer upon which pads or balls are formed. The pads may also be etched directly onto the silicon wafer, resulting in a package very close to the dimensions of the silicon die (it must have an area no greater than 1.2 times the die's). The CSP technology had been in development since the 1990s, but only in early 2000 that several companies begin the volume production (YOUNG, 1999).

Up to this point, single package solutions were presented, but in the 1980s, multi-

chip modules (MCM), integrating more than one die into a package, gave rise to the System-in-Package (SiP) concept (DAI, 2016). It allows chips manufactured using different technologies to be integrated into a single package (also called heterogeneous integration). The functionality of an entire system such as digital, analog, memories, Radio Frequency (RF), optical, and Micro-Electro-Mechanical Systems (MEMS) functions (ZHANG; ROOSMALEN, 2010). There are different SiP technologies, categorized into three levels for (ZHANG; GRAEF; ROOSMALEN, 2006):

- Level 1 SiP is composed of a wide variety of hybrid electronic components and multiple dies mounted in a high-density multi-layer interconnection substrate constituting a complete system that can work independently.
- Level 2 SiP refers to sub-systems built up using more than just one IC process, such as passive integration on a substrate.
- Level 3 SiPs are built up using heterogeneous technologies and placed or stacked in three-dimensional space, making use of advanced packaging technologies such as chip stacking, embedded components, substrate cavity, integrated passive devices (IPD), through silicon vias (TSV), and Package-on-Package (PoP).

The Level 3 SiP cited by (ZHANG; GRAEF; ROOSMALEN, 2006), its very similar to the system-on-package (SoP) concept, presented on (MADISETTI, 2006) and (TUMMALA; SWAMINATHAN, 2007), from Georgia Institute of Technology. These terms are interchangeably used in this work. Figure 1.3 helps us to understand the technologies that could be used in the Level 3 SiPs.

1.3 What is a System-in-Package?

The System-in-Package is a packaging technology that enables the miniaturization of functional systems into what looks like a single component (Fig.1.4). The size, functionalities, development time, and costs are the main drivers for a SiP product design (TUMMALA, 2001). This kind of device is different from the RF modules that can be easily found on the market and are often composed only of a small printed circuit board (PCB) enclosed by an electromagnetic shield. SiPs take advantage of using integrated circuits (especially bare dies) closer together along with their passive devices, enabling higher area efficiency. In addition, the packaging processes lead to higher system reliability, reduced overall volume, weight, and the complexity of the final system development

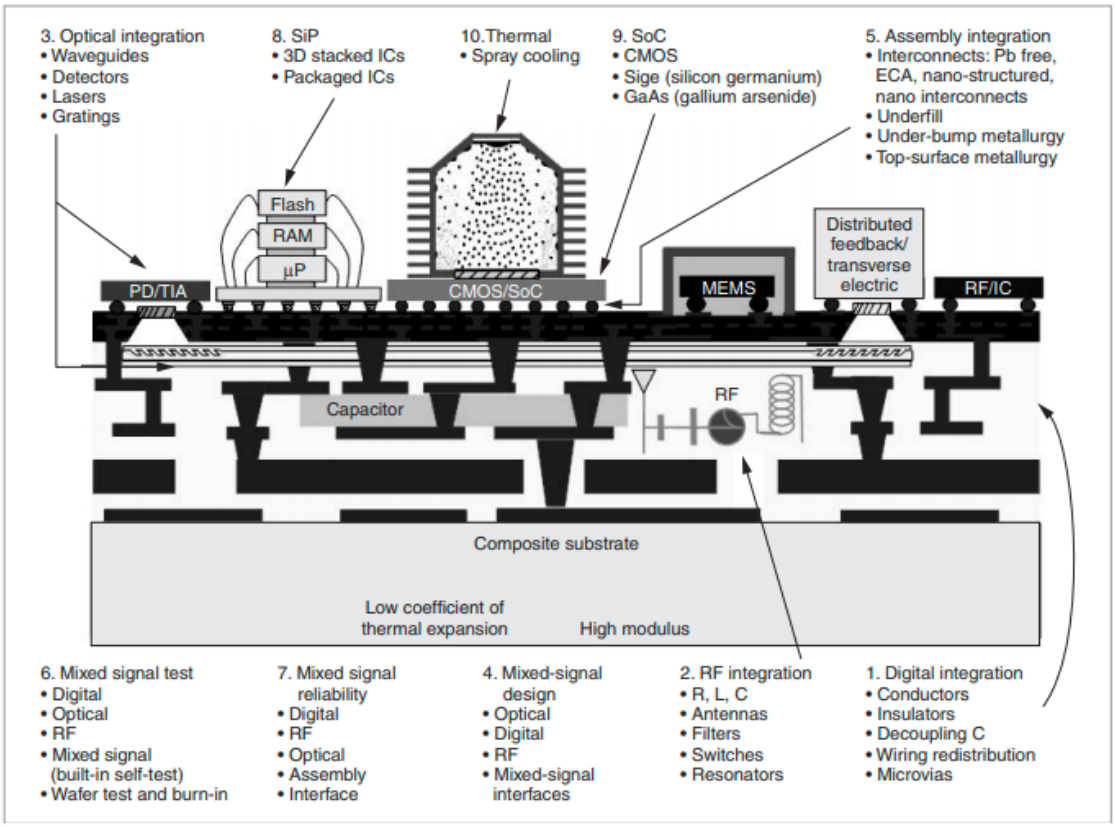

Figure 1.3 – Level 3 SiP representation. **Source:** (MADISETTI, 2006)

(TSUJIMURA, 2020). A great attribute of this technology is the integration of heterogeneous IC technologies, enabling the selection of the best individual processes optimized for the different system blocks such as digital, memory, power, analog, and RF into one single package.

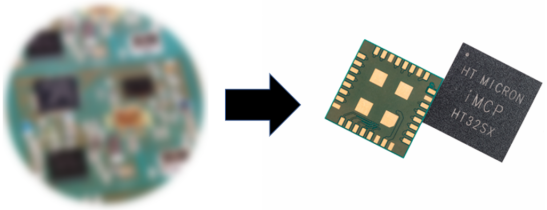

Figure 1.4 – System-in-Package device. **Source:** Author

The SiP technology and concepts help surpass some limits of the System-on-Chip (SoC) design, having a shorter development cycle, time to market, and much lower non-recurring engineering (NRE) costs compared to an SoC design (TUMMALA; SWAMINATHAN, 2007). Compared to SoC, the SiP development cycle could be 1/6 to 1/10 shorter than the SoC development cycle, and the development costs 1/5 to 1/10 lower than SoC development costs (LI, 2017). Using SiP technology, all modules can be certified in advance, so it is only necessary to put the required modules together to form a

multi-function chipset. That makes its use easier for the end-user since it can abstract the system design complexity, focusing on the features that will add more value to their customers.

1.4 Brazil and the Semiconductor Industry

The semiconductor industry encompasses the latest technologies abroad different disciplines, fostering intensive knowledge development. It is frequently pushing the science limits and using the technology edge. These characteristics demand massive investments, is hard to sustain, and is one of the main reasons to have only a few companies producing chip around the world (FILHO, 2004). This causes a growing dependency on technology, on a continental scale, around these companies (INTARAKUMNERD; CHAIRATANA; CHAIYANAJIT, 2016). Due to the industry complexity and costs, governmental programs are common in different countries to foster this technology and the industry local development (CHANG; AMSDEN, 1994).

The Brazilian trade balance deficit in electronic products achieved U$ 14.02 billion in the year 2021 (ABINEE, 2021), but efforts are being made to reduce this value. The Support to Development of Semiconductor's Industry Program (PADIS) was created to foster the industry in the country. To enjoy tax benefits, companies shall invest part of their gross annual earnings in activities focused on research and development (R&D) (FILHO, 2004). Another example was the IC Brazil Training Program, part of the Microelectronics National Plan, to develop specialized resources to design integrated circuits using the industry tools, techniques, and technologies (CARVALHO, 2018).

Despite the deficit in the semiconductor industry, there are some companies in Brazil willing to change this situation. HT Micron Semicondutores is a packaging company that used to act only in the final semiconductor fabrication cycle and saw an opportunity to develop a new line of products. This work aims to describe the design of its first product using the System-in-Package (SiP) technology, resulting from PADIS R&D incentives and the IC Brazil Training Program internship phase, where the author had the opportunity to participate. At the end of this development, the company's know-how on advanced packaging processes was used in conjunction with the IC design knowledge acquired by a team formed by graduates of the program to put a new product on the market.

1.5 Organization

This work started with a brief overview of the System-in-Packaging technology to give a clear view of the product proposed and the semiconductor packaging technology used. The next chapter will bring more details about the packaging, processes, the state-of-the-art, and its history. Chapter 3 discusses the Internet of Things concept and compares technologies for the Low Power Wide Are Networks such as NB-IoT, LoRa, and Sigfox. Chapter 4 starts proposing a design methodology, discusses the system specification, presents the system architecture, the package and circuit design, and the layout implementation to finally show the simulation results. Chapter 5 brings the package assembly results and the device's performance measurement. Chapter 6 closes this work with the author's conclusions.

2 SYSTEM-IN-PACKAGE TECHNOLOGY

The following sections of this chapter will discuss some fundamental packaging processes that help understand the basic packaging specifications. This section is followed by a review of the state-of-the-art applications enabled by advanced packaging solutions and System-in-Package technology.

2.1 Packaging Processes

This work will explore the design of a Land Grid Array (LGA) SiP as a solution for the Internet of Things device, and the simplified LGA package production process using wire bonding is described in Fig.2.1. The surface mount technology (SMT) process puts the discrete electrical components on the substrate, welding it in a soldering reflow furnace, followed by using cleaning agents to wash the substrate and remove residual solder particles and fibers in the package body substrate. In parallel,, the wafer thinning and dicing are done, making wafer cutting easier and reducing the final package's thickness. Die attach uses silver-filled epoxy adhesive to attach the IC chip to the substrate. Wire bonding uses pure gold wire to connect chip pins to bond pads on the substrate, and then molding encapsulation is done using the compression mold technique. The remaining steps include laser marking, singularization, testing, packing, and warehousing.

This chapter will discuss the critical elements of a SiP, starting with the package substrate in section 2.1.1, going through the SMT components assembly and wafer processing, and attaching in sections 2.1.2 e 2.1.3 respectively. The section 2.1.4 brings topics on sealing and encapsulation to finally review some reliability considerations.

2.1.1 Package Substrate

One of the SiP's advantages is the area reduction because the bare chips can be placed much closer together than chips in single packages, leading to better electrical performance since there is a reduced substrate wiring length. It is possible due to the multilayer board structures, made up of a laminated organic structure, using copper foil tracks on its inner and outer layers, with plated through-holes or vias interconnecting the layers.

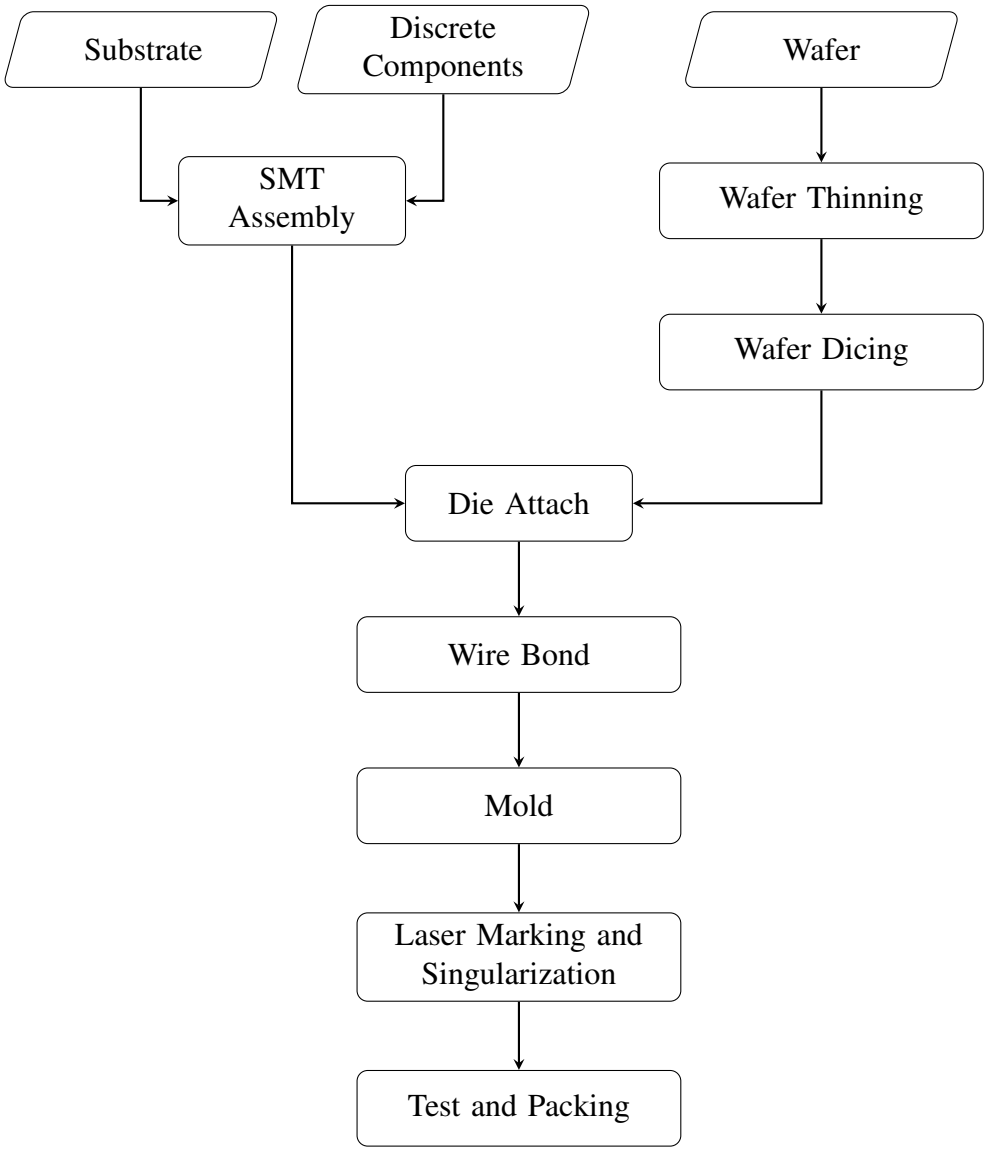

Figure 2.1 – Packaging assembly flow. **Source:** Author.

2.1.1.1 Mechanical Characteristics

The modern high-speed, high density, complex ICs, and components had their wiring complexity increased, needing advanced processing techniques for fabricating the substrate. Providing higher trace and vias density, different insulators, and dielectric characteristics. The incorporation of vias increases the wiring density. Blind vias extend only part way through the board, while buried vias connect between layers only within the board. Conductor trace width and spacing can be small as 30μm in advanced substrate technologies. The rigid laminated substrate type is typically epoxy-based polymer resin dielectric reinforced with fiberglass. There are two types of dielectric layers in the SiP construction: cores and prepregs. The core material is fully cured and usually clad with

copper on both sides. In contrast, the prepreg material is partially cured and is used between layers as a bonding agent to hold them together. The copper thickness is specified by a measure of its weight, in ounces, a 1 oz. copper foil is about 35 μm in thickness. The major limitation of the SiPs applications is the lack of wiring density, due in larger part to the need for the plated vias (TUMMALA, 2001), the standard drilled holes are relatively large (200-450 μm). It explains why the drilling costs rise rapidly below the diameter of 8mils (200 μm) in Fig.2.2. Microvias are an alternative to connecting layers using laser, plasma etching, or photo processing. Their diameter is typically less than 150 μm.

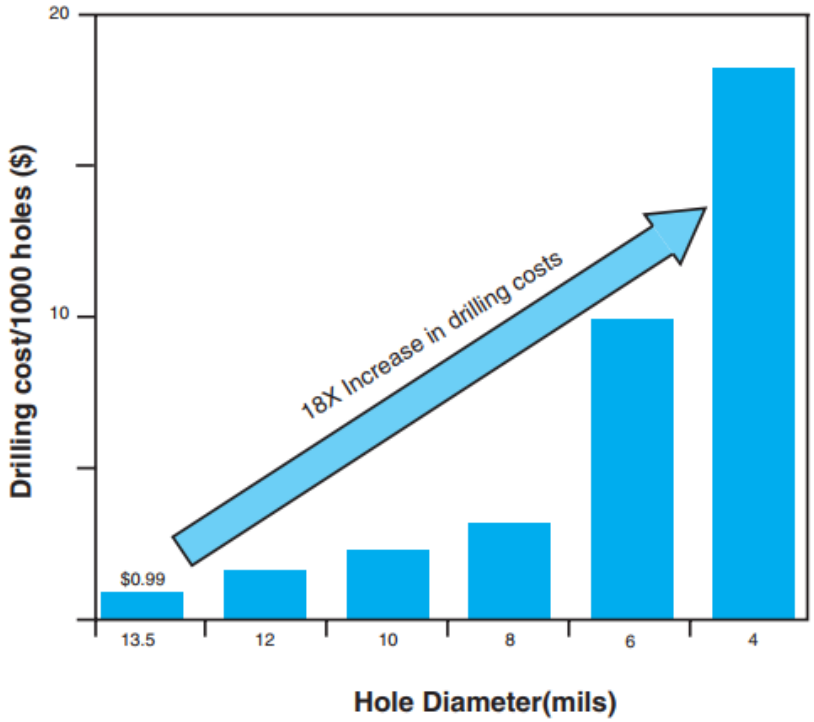

Figure 2.2 – Drilling cost of holes in organic laminate material as a function of hole diameter.
Source: (TUMMALA, 2001)

The insulator laminate material used in the sandwich structure of conductors and dielectrics must have good mechanical strength, low water absorption, not degrade at process temperatures, be able to drill enough, low expansion in Z-direction at process temperatures and be able to dissipate heat in product use (HOLDEN; BARR; POWELL, 2001). The main parameters include the glass transition temperature (T_g), which is defined as the temperature at which the polymer material changes from a hard and relatively brittle condition to a viscous or rubbery condition (CLARK, 2012), significantly changing many physical properties of the material after this transition. The coefficient of thermal expansion (CTE) describes the material expansion (over the temperature) in the x-y-z directions and the dimensional stability. A large majority of laminates are produced using

epoxy resins with reinforcing materials or fillers. As a result, this combination provides unique characteristics. The epoxy/glass flame-retardant 4 (FR4) is a low-cost and widely used material because of its acceptable CTE, heat resistance, good adhesion, and large processability. Despite of its lowest cost, FR4 does not meet some high-performance requirements of the packaging process, especially its transition temperature of (T_g) 130^oC, below the surface mount assembly or molding temperatures requirement. However, using high-temperature resins such as Bismaleimide Triazine epoxy (BT-epoxy) in the material composition provides a higher T_g of 180^oC and more stable CTE values (CLARK, 2012). The T_g of 180^oC is the best cost-effective balance for high technology boards, providing good mechanical resistance required for wire-bonding and SMT assembly (TUMMALA, 2001). Also, BT-epoxy has improved reliability thermal cycling with less pad lifting, less impact to the via plating, and voiding occurrences (TUMMALA, 2001). All these benefits make the BT-epoxy material the choice for this project.

2.1.1.2 Electrical Characteristics

Important electrical characteristics of the substrate laminate are the dielectric constant and the dissipation factor. The dielectric constant (ε), also referred to as permittivity, quantifies the ability of an insulating material to store electrostatic energy in an electric field. The laminate substrate manufacturer provide the value of the insulator relative dielectric constant (ε_r) (KHANDPUR, 2005). For BT-epoxy ε_r common values ranging between 3.5 and 5.

The dissipation factor or loss tangent ($\tan\delta$) is directly related to the resistive power loss in a laminate. The insulator material has charge carriers, naturally polarized dipoles, that realign themselves by rotation in the direction of the applied field. When an alternating field is applied, the total recoverable energy depends on the ability of charge carriers to re-orient themselves as the polarity of the field changes. As a result of this rotation, part of the electrical energy is converted into heat and is lost (CHEN et al., 2004). This make the laminate substrates and their interfaces critical for determining the circuit performance, specially in relation to the system frequency.

Expressed in another way, is the out-of-phase component ϵ'' (lost energy) in relation to ϵ', the in-phase component (Eq.2.1) (TUMMALA, 2001). This relation is depicted in Fig.2.3. Note that, in general, substrate materials have lower $\tan\delta$ values, ranging from 0.01 to 0.0001.

$$\tan \delta = \frac{\epsilon''}{\epsilon'} \tag{2.1}$$

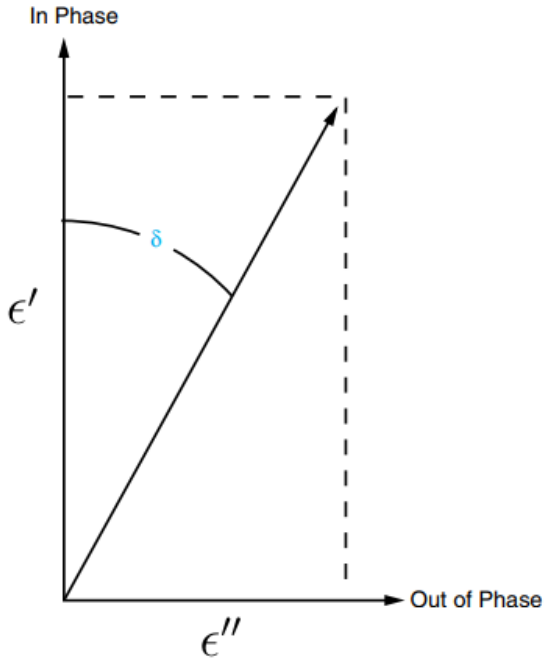

Figure 2.3 – Dissipation factor, or loss tangent, schematic representation. **Source:** (TUMMALA, 2001)

2.1.2 Surface Mount Technology

The use of a PCB as the electrical and mechanical platform for assembly has been a successful concept since the introduction of semiconductors in the 1950 (TUMMALA, 2001). The assembly process typically involves mounting components on a package substrate and soldering their leads. There are some differences between the abbreviations SMT, SMD, and SMA. SMA is the surface mount assembly, SMD is the device, and SMT is the entire technology. This technology has dominated electronic manufacturing since the late 1990s.

Compared to the through-hole assembly, that the compromisse area in all the board's layers, the SMT provides an excellent size reduction because the components only use external layers to connect to the board. Another important factor is the production gain provided by the components assembly with totally automated equipments (PRASAD, 2013). Surface mount assembly is done following the main process steps:

- Solder-paste printing

- Pick and Place
- Reflow soldering

In order to assemble the SMDs, solder paste is applied to a board substrate by the stencil-printing, components are placed on the board, and then the entire assembly is heated until the solder melts and forms solder joints. The flux is already mixed in with the solder paste, providing the necessary stickiness to hold the components in their correct positions until the solder joints are created (STRAUSS, 1994).

2.1.2.1 Solder-Paste Printing

For the solder-paste printing process, a stencil is used as a screen with openings through which a squeegee pushes the solder-paste onto the desired places on the substrate, generally the components pads. Solder-paste printing is one of the most critical steps to control the entire surface mount process. It is also the process step where the most errors occur (HWANG, 2012). The solder paste is a homogeneous combination of metal spheres in a flux medium.

2.1.2.2 Pick and Place

Component assembly is almost always automated. The equipment used is commonly called pick-and-place machines. The accuracy of the mechanical alignment of the board is not good enough for the assembly of today's small or fine-pitch components; that is why a camera is needed to find the marks used for optical alignment and inspection. These marks are commonly called fiducials. Component placement starts with the board being transported into the machine and fixed in its position. A board should have two or three fiducials widely separated in X and Y directions to allow optimal alignment (PRASAD, 2013). After the alignment, a vacuum nozzle is used to get the component up from its feeder and transport it to the correct position on the substrate. Since the pick-up position is not very accurate, there is a need for aligning the center of the component with the center of the nozzle to finally put the component in the correct substrate coordinates.

2.1.2.3 Reflow Soldering

The soldering provides an electrical, mechanical, and thermal connection between the components and substrate through a good solder joint with the proper intermetallic

build-up. The solder joint is created based on solder and flux. The flux reduces the oxides on the substrate surfaces, usually activated at higher temperatures ($150 - 160^{o}$C) (STRAUSS, 1994).

The reflow soldering is done after the solder paste is deposited into the pads and the components are in place. The process uses a conveyorized reflow oven (Figure 2.4). The reflow temperature profile and stages directly impact the product yield, solder integrity, and assembly reliability.

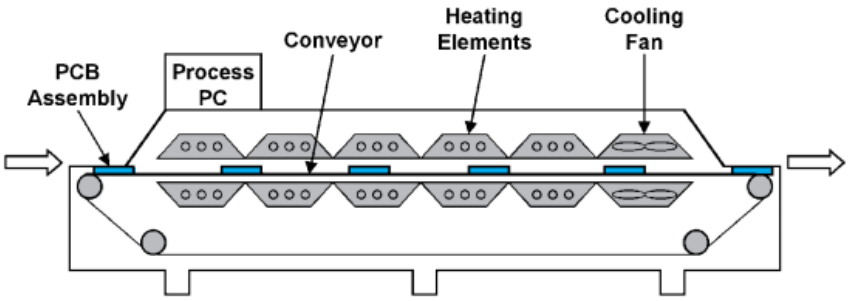

Figure 2.4 – Reflow oven. **Source:** (TUMMALA, 2001)

At the end of this process, the package IC substrate has all the SMDs mounted, and afterward, packaging processes advance through the die assembly.

2.1.3 Die Assembly

In the die mounting process, before being put all together in the package substrate, the wafer height must be reduced to fit within the package's requirements and get smaller electrical paths. Next, the wafer is singulated, and the chip is mounted onto the substrate using a die attach process. Finally, the wire bonding connects the chip to the substrate.

2.1.3.1 Wafer Thinning

Wafer thinning is an essential process that enables chip stacking and package area reduction through height reduction. The back side grinding is the most efficient way of thinning wafers until 100μm. At this limit, the wafer warpage and fragility are not acceptable (TUMMALA; SWAMINATHAN, 2007). It is composed of four steps:

- Tape mount
- Coarse grinding
- Fine grinding

- Tape removal

After the wafer is mounted in tape (to protect its surface against damage and contamination), the coarse grinding starts. It mechanically removes silicon faster, inducing wafer damage, and that is what limits the minimum thickness achieved in this step to 200μm. Also, it is recommended to keep at least a 20μm layer above the desired thickness (TUMMALA; RYMASZEWSKI; KLOPFENSTEIN, 2013). In the fine grinding step, the grinding wheel is changed, giving a safe and better wafer finishing achieving the final thickness. The tape removal step exposes the wafer to ultraviolet (UV) light to reduce the tape film adhesion. It should be noted that back-side grinding produces wafer warpage because of the damaged layer created during the process.

In some cases, after grinding, an additional step is needed: polishing. It is required to reduce the damage produced by fine grinding, providing enhancements on wafer strength and warpage. Several polishing methods have been employed, including chemical and mechanical polishing (CMP), dry and wet polishing, and dry (downstream plasma) and wet etching (WU; CHAN; HSIAO, 2003) (SANDIREDDY; JIANG, 2005).

2.1.3.2 Wafer Dicing

The conventional wafer dicing process cuts the wafer with a fully automatic dicing saw using a diamond-bonded wheel. The result is the individual chips. This process is divided into the follow steps:

- Tape and frame mount
- Wafer saw
- Cleaning and inspection

The wafer is mounted on an elastic dicing tape, secured to a mounting ring, and used to affix the wafer to the dicing saw. The wafer saw or dicing can be done in more than one step to smooth some problems. Usually, the scribe line (or scribe lane) width has 1/3 of the wafer thickness, and the blade thickness has 40% of the scribe line width (TUMMALA; RYMASZEWSKI; KLOPFENSTEIN, 2013). The mechanical dicing method induces such problems as chipping on the front and back surfaces of the die, delamination of mechanically brittle dielectric layers, and the formation of micro-cracks. The use of deionized (DI) water and CO_2 in the sawing process helps remove heat and reduce the blade's mechanical resistivity of the blade (TUMMALA; RYMASZEWSKI; KLOPFENSTEIN, 2013) and remove residuals.

2.1.3.3 Die attach

In this process, each die is attached (bonded) onto a package substrate. In some cases, before this process, plasma cleaning is needed to remove oxides and surface impurities. Die attach processes influence thermal management and stress isolation. The process resumes with these steps:

- Adhesive application
- Die attach
- Cure

Die attach film adhesives are used in controlled amounts on the die pad, which characteristics include: good adhesion, low creep, low moisture absorption, low cure temperature, low T_g, high electrical conductivity, and fatigue resistance. The die for mounting is ejected from the wafer, and a vacuum pick-up tool (also known as collet) retrieves and positions it on the adhesive based on a known good dies (KGD) map. The adhesive cure generally takes from 30 minutes to 1 hour at a temperature of 150^oC-180^oC into the oven. Common problems are delamination caused by contamination, low cure time or lack of adhesive film, broken chips, and short circuits caused by an excess of adhesive film.

2.1.3.4 Wire-Bonding

SIPs traditionally were interconnected by wire bonding. This technique is economical for interconnecting densities of up to 300 pads (TUMMALA; SWAMINATHAN, 2007). This technology bonds a fine wire (common materials are Al or Au) using thermosonic bonding between the IC pad and the substrate bond pad. To ensure good wire bondability, special care must be taken concerning the substrate surface finish. Cooper plated with nickel, and immersion gold is ubiquitous. An alternative is ENEPIG: Electroless Nickel (Ni $3 - 5\mu$m), followed by Electroless Palladium (Pd $0.05 - 0.1\mu$m) and an Immersion Gold (Au $0.03 - 0.051\mu$m). ENEPIG presents a better reliability performance (FU et al., 2008) and is also compliant with the Restriction of Certain Hazardous Substances (RoHS) directive (DENNIS; YEE, 2007).

The most common wire bonding technique is ball bonding. A significant advantage of ball bonding is that the capillary bonding tools are round so that the wire can be pulled through the capillary at any angle of the bonding head. The basic steps of thermosonic ball bonding are shown in Fig.2.5. The process involves forming a ball bond un-

der a controlled capillary bonding force at moderate temperature (between 150^o˘200^oC) using an ultrasonic excitation. Next, the wire is removed from the capillary to form the wire loop. The bond is formed between the wire and the package substrate bond pad. The tail is broken, and the electronic flame off (EFO) fires to form the ball for the next bond. It is the process cycle, and it can be less than 20ms (TUMMALA, 2001).

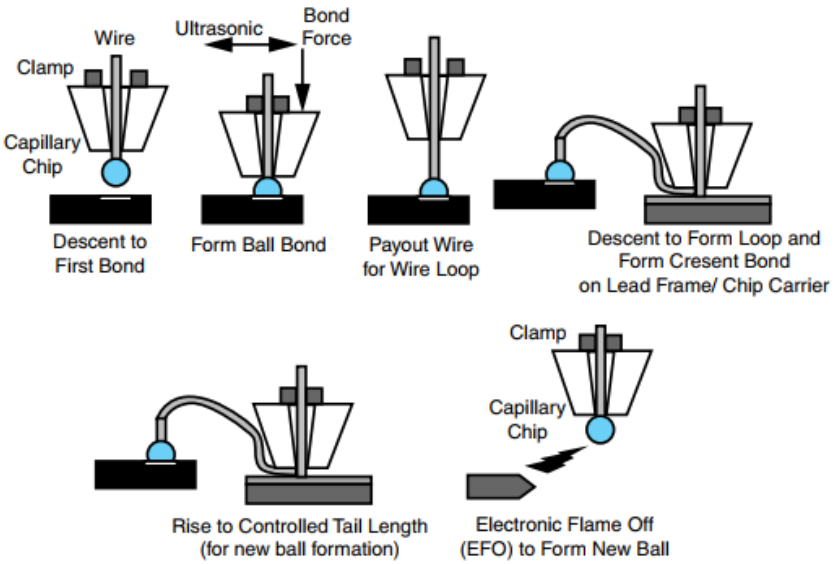

Figure 2.5 – Thermosonic ball bonding process. **Source:** (TUMMALA, 2001)

Another common wire bonding technique is wedge bonding. It has demonstrated the finest pitch bonding capabilities since the wire deformation is only 25–30% beyond the original wire diameter. The major disadvantage of wedge bonding is that the package bonding pad must be aligned along the axis between the chip pad and substrate pad to prevent wire fracture (TUMMALA, 2001).

These techniques can be used in different manners: forward and reverse bonding. Forward bonding allows long wire lengths, and higher-speed assembly starts on the die pad and ends at the substrate. Reverse bonding (or stitch bonding) starts at the substrate pad and goes to the die, creating a low wire loop height over the last and a higher loop height at the former.

2.1.4 Encapsulation

Encapsulation protects device packages isolating the devices within from environmental pollutants, offering mechanical protection, and presenting a cooling surface for heat transfer and structural coupling of the epoxy mold compound (EMC) to the package

substrate. The machinery and the tooling used in this process are dimensioned for molded array packages (MAP) instead of single package units. The MAP comprises a substrate panel containing several units and process alignment fiducials.

The primary encapsulating process in the IC packaging market is the transfer molding (TUMMALA; SWAMINATHAN, 2007). Applying pressure, the heated molten molding compound is transferred from a pot (plunger) into the mold cavities (Fig.2.6(a)). However, the transfer molding method faces difficulties in molding advanced packages since it requires a resin flow path with high injection pressure. Aa different encapsulation process is introduce to overcome this issued: the compression mold (MIURA, 2016).

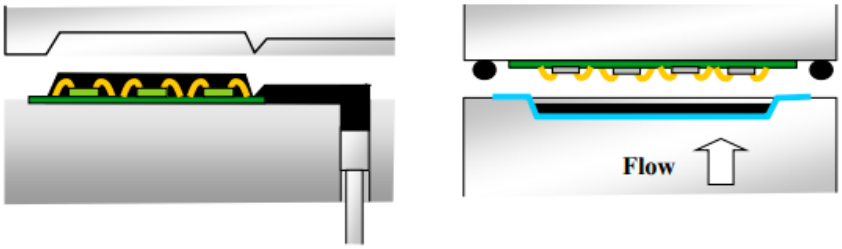

Figure 2.6 – Mold processes: a) Transfer Mold b)Compression Mold. **Source:** (MIURA, 2016)

Compression mold is used to mold packages with the minimum compound flow. The granule EMC is first deposited on the foil clamped onto the bottom mold chase at the required temperature. Then the top and bottom chases are brought into contact, the substrate is chucked, and the compression is started (JULIEN et al., 2020).

Encapsulants must have the required mechanical and thermal properties. However, these properties are not present in a single epoxy, and a formulation comprising a mixture of resin, hardener, catalyst, mold release agent, additives, and a filler generally silica (60% to 90%), is needed. Spherical silica fillers help the MAP to minimize defects such as wire sweep and void traps. The encapsulation can be a major contributor to overall module reliability. The EMC with CTE in the desirable range of 10–15$ppm/^o$C and with T_g outside of reliability testing window (65^oC–150^oC), are essential for robust encapsulated packages (TUMMALA, 2001).

After a curing time (typically 1 hour at 150^oC), the packages are singulated from the MAP substrate, marked with a laser, and finally packaged.

2.2 Review of state-of-the-art in SiP Applications

From simple metal to complex multi-layer ceramic or organic structures, the packaging design and fabrication processes become increasingly complex and challenging as the semiconductor technology progresses towards higher levels of performance and functionality. At this moment, the advanced packaging technologies bring alternatives for new electronics devices, exploring different semiconductors technologies integration and providing broader system functionalities into single chips. This section presents applications of these innovative packaging technologies, gathering some of the latest trends in medical, wireless, and sensor-based devices.

2.2.1 Implantable Electronic Systems

Implantable electronic systems should combine bio-compatibility, hermeticity and extreme system miniaturization to provide an interface with the human body (MCLAUGHLIN; IMRAN, 2012). These systems can be used to obtain data through embedded package sensors (CHEN; YOUNG, 2016) or to affect biological functions. Packaging plays an essential role in biomedical applications, and key innovations are driven by the hermetic titanium case supporting highly-integrated 3D electronics modules. Low power applications with few data channels, low current, low duty cycle, and long-term use expectations, such as pace-makers, could be battery-driven. Batteries using lithium polycarbon monofluoride (Li-CFx) chemistry have been gaining acceptance. It is reliable, does not generate gas, has a low self-discharge rate, and is capable of providing a modest amount of current, enabling the minimum and limited pace-maker operation life of 5 years. Power demanding applications have been using energy harvesting techniques (CHEN; YOUNG, 2016) or Power Telemetry (e.g., inductive link) to supplement finite battery capacity. Power Telemetry could be used to drive photonic sensors, fluorescence spectroscopy detects pressure, glucose concentration, blood oxygenation for hemodynamics, or several other markers and wirelessly communicates to an external reader(ABDAL; HASSAN; RAJ, 2021).

The trends described above drive several packaging technologies with advanced materials and processes to improve functional density, reliability, and heterogeneous integration of system components in the required device geometries. Faster time to clinical use is met using the Food and Drug Administration (FDA) agency-approved materials

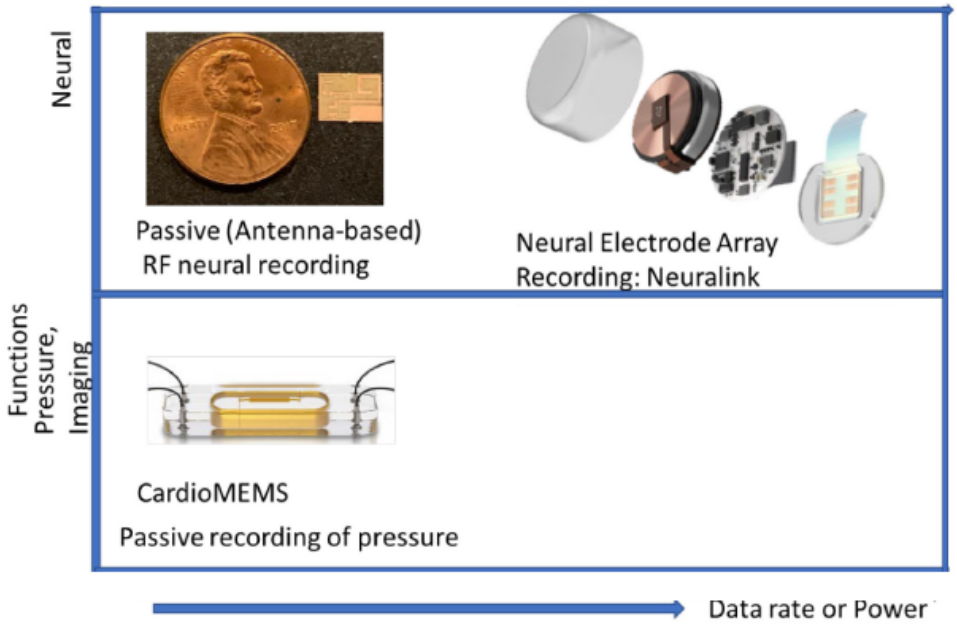

Figure 2.7 – Biomedical devices for health-monitoring, imaging, spectroscopy and neural recording. **Source:** (MARKONDEYA; NEDUMTHAKADY; TUMMALA, 2019)

and technologies. The most sophisticated electronic systems injected into the body are the wireless camera pills that can collect images, process them and communicate to outside (MARKONDEYA; NEDUMTHAKADY; TUMMALA, 2019). Wireless cameras are a 3D system packaged into a cylindrical pill with electromagnetically and optically transparent walls. The Figure 2.7 system comprises an antenna and RF transmitter on one end, lens and CMOS camera on the other hand, with a battery in the middle. This 3D package pill can communicate images to an external reader. Emerging 3D heterogeneous-integrated 3D package architecture details of these systems are illustrated in Figure 2.7.

2.2.2 Antenna-in-Package Technology

The Antenna-in-package (AiP) technology integrates an antenna with a radio transceiver into a package, considering performance, size, and cost. There are different challenges in the AiP design; for example: at 2.4 GHz, a key challenge is how to miniaturize the antenna size, while at 60 GHz, it is how to minimize the interconnect losses between the chip and antenna. For microwave and millimeter-wave (mmWave) applications, AiP technology is more of a need than an option since the most common way to minimize the transmission losses in higher frequencies is to reduce the overall distance between the signal source and radiator (ZHANG, 2019). The author in (HO et al., 2019) discusses the

challenges faced by packaging engineers minimizing the transmission losses from chip to package, where the transceiver chip is embedded in a mold compound at the 77GHz automotive radar systems (Figure 2.8).

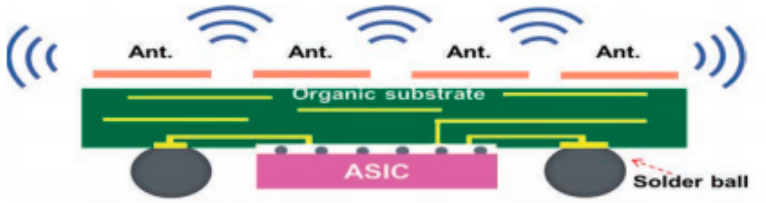

Figure 2.8 – Cross-section view of the mmWave transceiver on flip antenna in package. **Source:** (HO et al., 2019)

A commercial gesture radar was developed using the AiP technology (NASR et al., 2016). It presents a highly integrated 57–64 GHz transmitter for short-range sensing. The chip is mounted in a wafer-level ball grid array package, with six patch antennas realized at the metal redistribution layer. The receiver patch antennas have a combined antenna gain of around 10 dBi, and each transmitter antenna has a gain of around 6 dBi. Figure 2.9 the AiP and the antennas details.

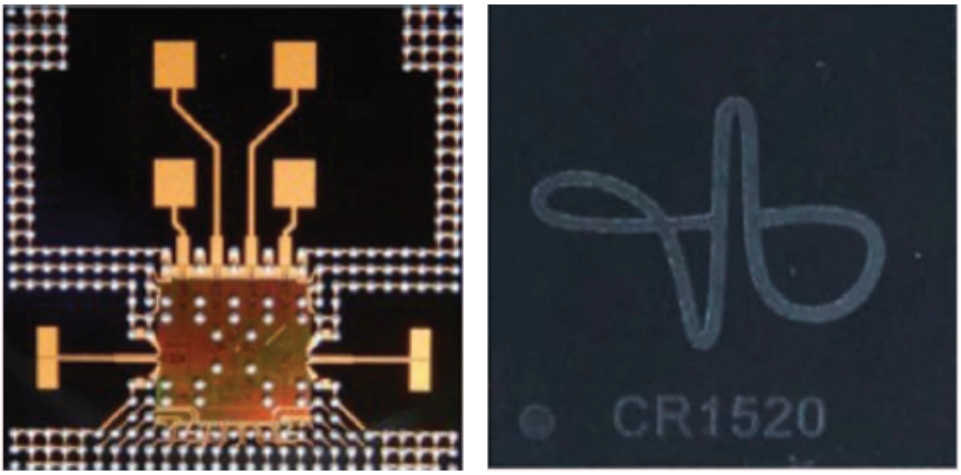

Figure 2.9 – Top and bottom view of an AiP for a 60 GHz gesture radar. **Source:** (NASR et al., 2016)

AiP is now a mainstream antenna technology, dominating antenna solutions for mmWave wireless devices and RF IoT devices (LU; CHO; CHANG, 2021). It represents an important achievement in antenna and packaging technologies and has proved to offer excellent antenna solutions for radio and radar technologies.

2.2.3 Automotive light Detection and Ranging (LiDAR) Applications

LiDAR is a method for determining ranges (with variable distance) by targeting an object with a laser and measuring the time for the reflected light to return to the receiver. A narrow laser beam can map physical features with very high resolutions. It uses ultraviolet, visible, or near-infrared light to image objects. It also targets a wide range of materials, including non-metallic objects, rocks, rain, chemical compounds, aerosols, clouds, and even single molecules (BEHROOZPOUR et al., 2017). According to the scanning sensor mechanism, LiDAR can be divided into flash, mechanical, MEMs, and optical phased arrays (OPA).Following the recent integration trends, it has been applied on 3D imaging. It is essential for autonomous-driving cars to find the distance of multiple points on an object or in a scene creating a point cloud of those range measurements.

At this moment, LiDAR package solutions do not have a standardized process due to the customers' varying requirements. Without scale, it becomes inherently expensive (SAPONARA; GRECO; GINI, 2019).

Using standardized MEMS sensors processes, (SATTU et al., 2021), a cost reduction was achieved with cavity and molded cavity LGA/BGA packages. Typical laser diode and detector packaging use high-cost ceramic substrates, which feeds the industry's continued development of laminates and mold compounds to ensure low-cost and high-reliability materials. These technologies target product categories such as biometric authentication, human interfaces, and automotive.

Common building blocks for a LIDAR system consist of an emitter (for scene illumination), a detector (to capture the reflected light), an application-specific integrated circuit (ASIC) to process the signal, and a processing unit to analyze the data. With SiP modules successfully reaching automotive applications, an integrated trans-impedance amplifier (TIA), an integrated single-photon avalanche diode (SPAD) with an ASIC can be packaged in a side-by-side solution.

Molded-cavity structures can be modified, including flip-chip/copper pillar bonds instead of a wire bond, LGA instead of BGA, and varying glass attach epoxies for different applications. Different wavelengths for a clear die attach film (DAF) solution adhesive offer over 93% transparency in the infrared spectrum (SATTU et al., 2021). Figure 2.10, structure B, utilizes a clear DAF to attach the glass, while Figure 2.10, structure A, uses an ultraviolet (UV) curable epoxy to attach the glass to create an air gap. Utilizing similar technologies, multiple sensors can be integrated into one package Figure 2.10, structures

C, D, and E show three different solutions for combo-sensors. Structure C uses a ceramic substrate with a stacked die solution on top, recommended for high-power applications. Structures D and E both utilize wire-bond interconnects with a laminate substrate, one with a molded solution (E) and the other (D), a liquid crystal polymer (LCP) lid. Both solutions, (D) and (E), are optimal for lower power applications.

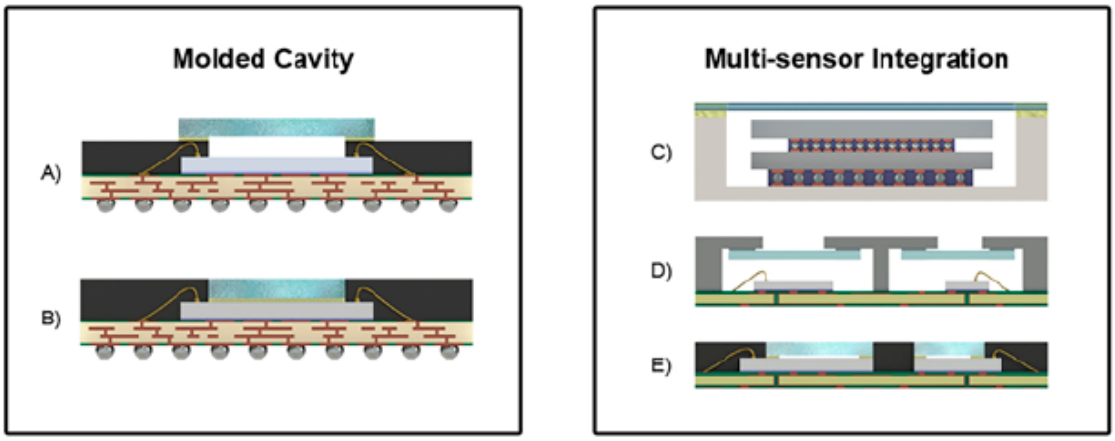

Figure 2.10 – Advanced packaged solutions for LiDAR sensors. **Source:** (SATTU et al., 2021)

2.3 Status of the Technology

This chapter presents the fundamental manufacturing processes and some applications on the edge of the packaging technologies. All of these cases have something in common: the materials technology dictates the majority of limitations, from the device energy source to its dimensions or its bio-compatibility.

The SiP technology has a unique advantage where the size is critical. Today's AiP technologies implemented on SiP modules achieve a complete RF front-end. Due to its high integration, the RF design, tune, and test iterations are reduced for RF systems, enabling an accelerated time-to-market. It is perfect for the Internet of Things products, where different companies and technologies are racing for this new market.

3 INTERNET OF THINGS

It has been a long time since the internet plays a significant role as an information interface for our society, and the technology is moving towards data collection, analysis, and remotely controlling devices rather than just sharing the information (BĂLĂU; UTZ, 2017). This advance results in the Internet of Things (IoT) technology. The concept is not new; as soon as the internet started to spread worldwide, people became delighted to imagine how multiple electronic devices could be integrated into our lives in a manner in which no one could notice their presence (WEISER, 1995). IoT is an emerging paradigm that includes many technologies, enabling the internet to reach the real world of physical objects. The result is an interconnected smart world where humans and devices interact, establishing an environment where the exchange of data and services is continuous.

In contrast to the computing platforms, such as desktop and handheld devices, IoT devices receive data through sensors (often highly miniaturized) and send information through wired or wireless interfaces to cloud computers. It enables the placement of IoT devices in multiple new applications where computing was previously absent (GOURSAUD; GORCE, 2015). It presents a considerable challenge to the electronics and semiconductor industry but also is an opportunity where the expected volume may exceed all previous computing classes (LIU; HAN; LI, 2020).

An encouraging factor for spreading the IoT paradigm is that many industry-leading manufacturers, service providers, and software and systems developers are investing in the IoT future world vision (CRUZ et al., 2018). The number of internet-connected devices is expected to be 75.44 billion (Figure 3.1), and the economic growth of IoT technology will range from 2.7 to 6.2 trillion by 2025 (SWAMY; KOTA, 2020).

Bluetooth Low Energy, Zigbee, and Wi-Fi are some examples of conventional IoT technologies commonly used for short-range communications (PALATTELLA et al., 2016). Still, recently, the IoT requirements have led to the development of the Low Power Wide Area Networks (LPWANs) (CENTENARO et al., 2016).

3.1 Low Power Wide Area Networks

Low power wide area networks are a novel communication paradigm that complements traditional cellular and short-range wireless technologies, focusing on long-range communication and low energy consumption applications. It represents approx-

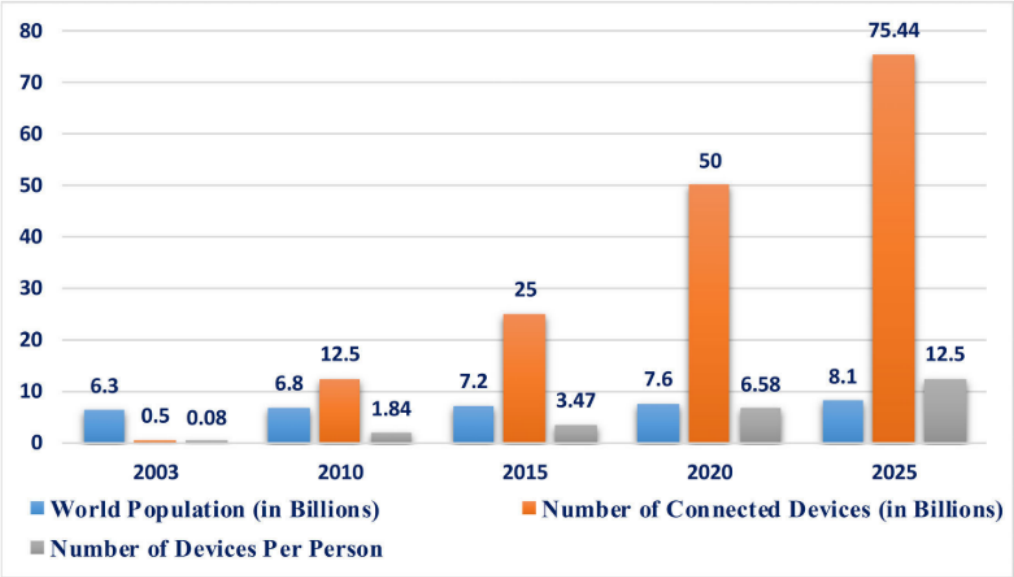

Figure 3.1 – Estimated number of devices connected to the internet by 2025. **Source:** (SWAMY; KOTA, 2020)

imately one-fourth of the overall IoT Market (RAZA; KULKARNI; SOORIYABANDARA, 2017). It provides long-range communication up to 10–40 km in rural, and 1–5 km in urban zones (CENTENARO et al., 2016). The term LPWAN doesn't even exist in early 2013 (SINHA; WEI; HWANG, 2017). Long-range wireless communications must have a significant link budget; otherwise, they will lose the signal power along the way it propagates. Receiver sensitivities of more than -130 dBm are common (compared with the -90 to -110 dBm seen in traditional wireless technologies). The Shannon-Hartley theorem states that the energy per symbol or energy per bit is the main lever to change the possibility of a message being "heard" (LATHI, 1990). Slowing the modulation rate by half, there is twice as much energy in each symbol, increasing the receiver sensitivity by double, i.e., 3 dB. It explains the data rate values used in these technologies. Most LPWANs operate in the unlicensed Industrial, Scientific, and Medical (ISM) bands, centered at 868MHz, 915MHz, and 433MHz, providing better indoor coverage. Sigfox, LoRa, and NB-IoT are some examples of leading emergent LPWANs (PALATTELLA et al., 2016) (CENTENARO et al., 2016), each of these new technologies differing in data rates, coverage, security, power consumption, and scalability.

3.1.1 NB-IoT

NB-IoT is an IoT technology specified by 3GPP as a part of Release 13 in June 2016. It coexists with a global system for mobile communications (GSM) and long-

term evolution (LTE) technologies under licensed frequency bands of 700MHz, 800MHz, and 900MHz. One of the significant advantages of NB-IoT is that it can be supported with only a software upgrade in addition to the existing LTE infrastructure (WANG et al., 2017). It occupies a frequency bandwidth of 200 kHz and employs BPSK and QPSK modulation. NB-IoT uses 12 subcarriers of 15 kHz in downlink using OFDM and 3.75/15 kHz in uplink using SC-FDMA. There are different frequency band deployments, which are stand-alone, guard-band, and in-band deployments, as shown in Fig. 3.2. Stand-alone deployment can also use the GSM frequency bands, the guard-band scheme utilizes the unused resource blocks within an LTE carrier's guard band, and the in-band utilizes resource blocks within an LTE carrier.

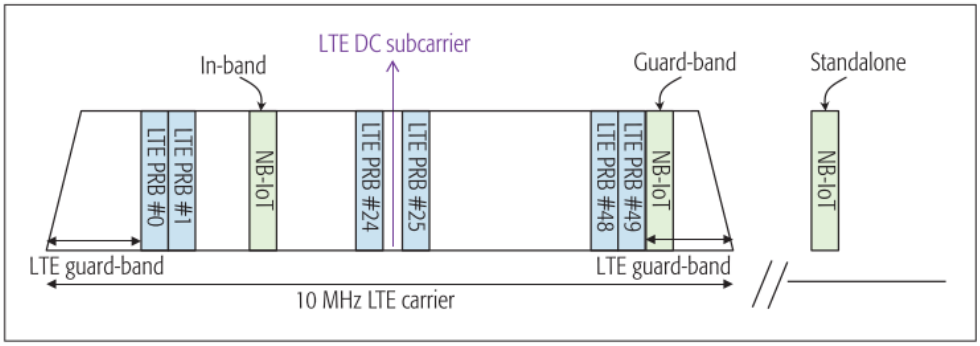

Figure 3.2 – NB-IoT stand-alone deployment and LTE in-band and guard-band deployments.
Source: (WANG et al., 2017)

3.1.2 LoRa

LoRa was developed by a start-up in 2009, purchased later by Semtech, and standardized by LoRa-Alliance in 2015. The bidirectional communication modulates signals in the unlicensed sub-GHz ISM band using a proprietary chirp spread spectrum (CSS) technique with configurable data rates from 300 bps up to 50 kbps, depending on the spreading factor and channel bandwidth (SFORZA, 2013). Despite LoRaWAN being offered at least three classes of operation, class-A end devices are preferred for application developers. It allows bidirectional communications where two short downlinks follow each end-device uplink transmission receive windows. In this mode, the end device must wait until the following uplink message to receive data from the base stations. Class-B uses short scheduled receive windows while class-C has continuously open receive windows, only closed when transmitting. The class-A operation has a lower power requirement.

3.1.3 Sigfox

Sigfox was founded in 2010 and had been growing very fast as a service provider for IoT. The network is laid out in a star topology, operating in unlicensed frequency bands worldwide. The patented ultra narrowband (UNB) technology uses time and frequency diversity, i.e., each message is resent three times on three random carrier frequencies, with 100Hz or 600Hz of bandwidth, depending on the region. Using different radio configurations (RCs), the global operation is organized into seven geographical zones, radio configuration (RC) 1 to RC7, and each zone has its own set of parameters (SIGFOX, 2021a), defining the device requirements and guiding the hardware implementation.

The end devices are connected to Sigfox Cloud via its proprietary base stations operating in unlicensed frequency bands, ranging from 862 to 928MHz. The patented technology uses time and frequency diversity, i.e., each message is resent three times on three random carrier frequencies.

At the physical level, the Sigfox protocol uses the binary phase shift keying (BPSK) modulation scheme and a data rate of 100bps or 600bps, depending on the region. The number of messages for the uplink is limited to 140 per day, with a maximum payload length of 12 bytes (excluding headers). The downlink uses the Gaussian frequency shift keying (GFSK) modulation, is limited to 4 messages per day, and has a maximum payload length of 8 bytes (excluding headers). The end device must request the downlink message, with a delay of 20 seconds between the first frame transmitted and the reception window that lasts for 25 seconds maximum.

3.2 Technologies Characteristics Comparison

In recent years we have seen the emergence of IoT as a promising paradigm to accommodate massive machine-to-machine (M2M) connections within licensed, or unlicensed spectrum (PALATTELLA et al., 2016), using existing standards and infrastructures or developing new proprietary standards. All these connected devices can acquire data from the environment in which they are placed (monitoring) and provide different information to other devices that could even act in this context. Such behavior generates a distributed network, in which heterogeneous data sources can cooperate by querying different information (ZHOU et al., 2018).

A variety of applications can exploit the Low Power Wide Area Network (LP-

WAN) technologies to connect their end devices. These sectors include but are not limited to smart cities, smart metering, logistics, industrial monitoring, agriculture, etc. (LEA, 2018). Each application is unique to the characteristics of each technology. It is essential to understand the differences between the available LPWANs to choose the best fit for each application. The author in (MEKKI et al., 2019) compares these technologies in terms of the IoT success factors such as scalability, range, coverage, deployment, cost efficiency, battery life, quality of service (QoS), payload length, and latency (Fig.3.3).

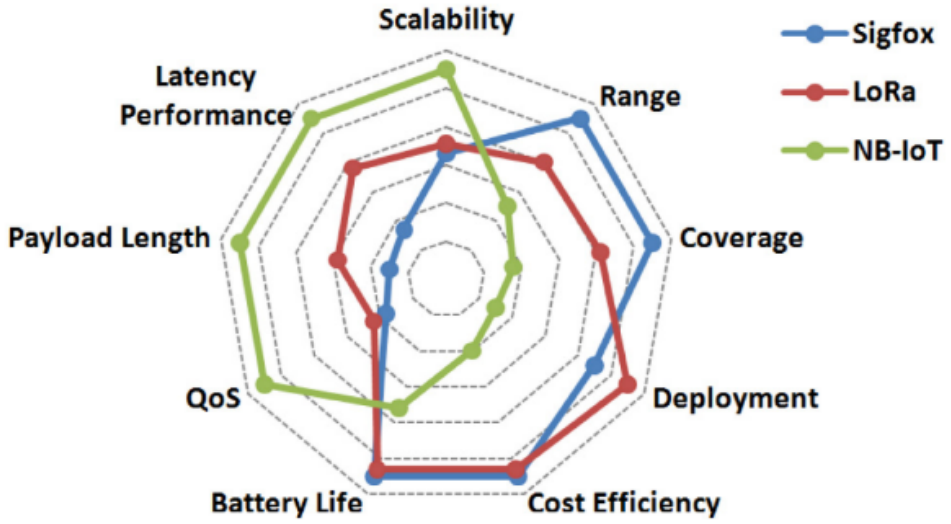

Figure 3.3 – NB-IoT, Sigfox and LoRa IoT factors comparison. **Source:** (MEKKI et al., 2019)

Table 3.1 presents a technical comparison among the technologies discussed in this section to better understand the LPWAN network characteristics. Each technology has its place in the IoT market (MEKKI et al., 2019). Sigfox and LoRa are preferred for a lower-cost device, long range (high coverage), infrequent communication, and long battery lifetime. By contrast, NB-IoT serves the higher-value IoT markets willing to pay for low latency and high quality of service.

Table 3.1 – LPWAN technologies: Sigfox, LoRa, and NB-IoT. **Source:** (MEKKI et al., 2019)

	Sigfox Network	**LoRa**	**NB-IoT**
Modulation	BPSK	CSS	QPSK
Frequency	Unlicensed ISM bands: 868-915 MHz	Unlicensed ISM bands: 868-915 MHz	Licensed LTE frequency
Bandwidth	100 Hz and 600Hz	125 kHz and 250 kHz	200 kHz
Max. data rate	600 bps	50 kbps	200 kbps
Bidirectional	Limited / Half-duplex	Yes / Half-duplex	Yes / Half-duplex
Messages/day	Uplink: 140; downlink: 4	Unlimited	Unlimited
Max. payload length	Uplink: 12 bytes; downlink: 8 bytes	243 bytes	1600 bytes
Range	10 km (urban); 40 km (rural)	5 km (urban); 20 km (rural)	1 km (urban); 10 km (rural)
Interference immunity	Very high	Very high	Low
Authentication and encryption	Yes (AES-ECB)	Yes (AES 128b)	Yes (LTE encryption)
Adaptative data rate	No	Yes	No
Handover	End-devices do not join a single base station	End-devices do not join a single base station	End-devices join a single base station
Localization	Yes (RSSI)	Yes (TDOA)	Under specification
Allow private network	No	Yes	No
Standardization	Sigfox Company	LoRa-Alliance	3GPP

6 CONCLUSIONS

This work presented an overview of the challenges in designing a System-in-Package product as a compact solution for the Internet of Things applications using the Sigfox technology. The results are very satifatory, it meets all the Sigfox Verified certification requirements enabling the Monarch feature in a 13 mm $\times$ 13 mm $\times$ 1.1 mm total package size. This reduction reaches 65% when compared to the smaller market competitor, maintaining the device's competitive performance (especially efficiency at RC1, where it has the highest value of 25.1%, almost double of the lowest competitor value) and functionality for global operation. Moreover, this device stands out among some limited options available in the market by providing a programmable MCU (32bits Arm M0+) and a programable output power. Consequently, it is not merely an AT-command module (despite its ability to operate as such), but rather a programmable module that enhances IoT applications with intelligence and local processing capabilities.

The impedance target value (section 5.2.2) unfortunately was not met because the design simulation was not performed before the substrate fabrication, but the simulation was validated with measurements and the module first prototype maintain a competitive performance. These results demonstrated that the VNA's measurement procedure was performed correctly. The presented solution for the network achieved a satisfactory transmitter performance compared with market competitors.

The proposed SiP was probably the first reported product made and designed in Brazil using this technology. The design of a SiP working in the sub-GHz frequency shows the multidisciplinary nature of the challenges, remarking the way assembly processes and the design choices are interdependent. Starting from the product requirements, going further through the SiP design, supporting the packaging assembly until finally validating the device performance had presented a broad product design perspective. Not only the technical aspects of a product were considered, but a complex relationship between stakeholders' expectations and interests, costs, and time takes place.

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LIST OF PUBLICATIONS

The authors were awarded as the best paper at industrial category for the work listed bellow.

KALINSKI, F. et al. Compact System-in-Package Design for IoT Sigfox Applications. **In: 11th Symposium on Integrated Circuits and Systems Design (WCAS).** 2021.

APPENDIX A — RF AND MICROWAVES FUNDAMENTALS

The radio frequency (RF) and microwave engineering fields deal with high-frequency alternating current signals. Because of these short wavelengths, the voltages and currents no longer remain spatially uniform compared to the circuit elements' size. Traditional circuit theory cannot be used to solve network problems in these cases. They have to be treated as propagating waves.

This chapter brings the fundamentals, closing the gaps concerning the topics presented in the text.

A.1 General Considerations

The voltage and power gain are expressed in decibels (dB).

$$A_V = 20 \log \left(\frac{V_{out}}{V_{in}} \right) \tag{A.1}$$

$$A_P = 10 \log \left(\frac{P_{out}}{P_{in}} \right) \tag{A.2}$$

A.2 Transmission Line Theory

A transmission line is a *distributed parameter network*, where voltages and currents can vary in magnitude and phase along with length. Standard circuit theory deal with *lumped elements*, where voltage and current do not vary over the circuit elements' physical dimension. Figure A.1 shows an equivalent circuit for an infinitesimal section of a transmission line (Δz).

Note that voltages and currents depend on both time (t) and position (z) since they are treated as propagating waves. R, L, G, and C are per-unit-length quantities, where:

- R = series resistance, in Ω/m
- L = series inductance, in H/m
- G = conductance, in S/m
- C = shunt capacitance, in F/m

This model is robust. A cascade of these sections is considered to represent a

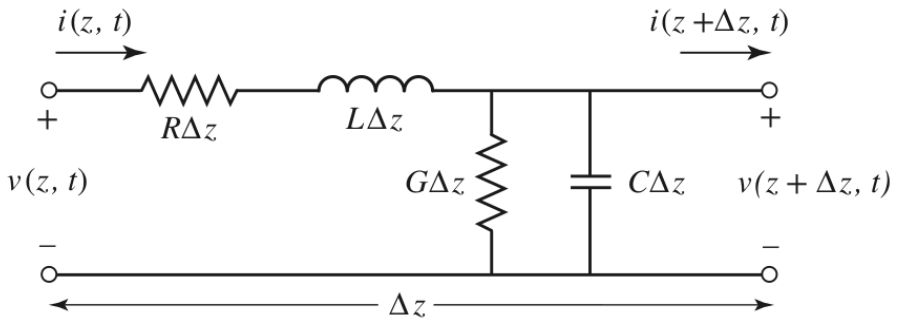

Figure A.1 – Transmission line lumped element equivalent circuit.
Source: (POZAR, 2011).

finite-length transmission line.

A.2.1 Transmission Line Wave Equations

Applying the Kirchhoff's laws to the Figure A.1 circuit, we get the Equations A.3a and A.3b.

$$v(z+\Delta z,t)-v(z,t)=-R\Delta z i(z,t)-L\Delta z\frac{\partial i(z,t)}{\partial t}, \tag{A.3a}$$

$$i(z+\Delta z,t)-i(z,t)=-G\Delta z v(z+\Delta z,t)-C\Delta z\frac{\partial v(z+\Delta z,t)}{\partial t}, \tag{A.3b}$$

Dividing both by Δz and taking the limit as Δz $\to$0

$$\lim_{z\to 0}\frac{v(z+\Delta z,t)-v(z,t)}{\Delta z}=-Ri(z,t)-L\frac{\partial i(z,t)}{\partial t}$$

$$\lim_{z\to 0}\frac{i(z+\Delta z,t)-i(z,t)}{\Delta z}=-Gi(z,t)-C\frac{\partial v(z+\Delta z,t)}{\partial t}$$

Equations A.4a and A.4b becomes the *Telegrapher's Equations* by definition of derivative.

$$\frac{\partial v(z,t)}{\partial z}=-Ri(z,t)-L\frac{\partial i(z,t)}{\partial t}, \tag{A.4a}$$

$$\frac{\partial i(z,t)}{\partial z}=-Gv(z+\Delta z,t)-C\frac{\partial v(z+\Delta z,t)}{\partial t}, \tag{A.4b}$$

For the sinusoidal, steady-state condition: $v(z,t)$ = Re$\{V(z)e^{j\omega t}\}$ and $i(z,t)$ = Re$\{I(z)e^{j\omega t}\}$, the *Telegrapher's Equations* can be simplified as shown in Equations A.5a

and A.5b.

$$\frac{\partial V(z)}{\partial z} = -(R + j\omega L)I(z), \tag{A.5a}$$

$$\frac{\partial I(z)}{\partial z} = -(G + j\omega C)V(z), \tag{A.5b}$$

The functions V(z) and I(z) are complex and describe the magnitude and phase of the $e^{j\omega t}$ sinusoidal time function for voltage and current along the transmission line as a function of position z. To find a solution for $V(z)$ and $I(z)$ that satisfy both *Telegrapher's Equations* we first take the derivative of Equation A.5a as shown in Equation A.6.

$$\frac{\partial^2 V(z)}{\partial z^2} = -(R + j\omega L)\frac{\partial I(z)}{\partial z} \tag{A.6}$$

Combining the Equation A.6 and A.5b we get an equation involving one function only (Eq. A.7). In a similar way the differential equation for the current $I(z)$ is given in Equation A.8.

$$\frac{\partial^2 V(z)}{\partial z^2} = (R + j\omega L)(G + j\omega C)V(z) = \gamma^2 V(z) \tag{A.7}$$

$$\frac{\partial^2 I(z)}{\partial z^2} = (R + j\omega L)(G + j\omega C)V(z) = \gamma^2 I(z) \tag{A.8}$$

γ (in Eq. A.9) is known as *propagation constant*, which is a complex value function of frequency.

$$\gamma = \alpha + j\beta = \sqrt{(R + j\omega L)(G + j\omega C)} \tag{A.9}$$

Considering a solution for Equations A.8 and A.8, the functions $V(z) = e^{+j\gamma z}$ and $V(z) = e^{-j\gamma z}$ has the characteristic of the double derivative results in the original function weighted by a constant. Since we are working with a linear differential equation, the superposition will be a solution. Accordingly to this analysis, the solution to this equations are described by Equations A.10a and A.10b.

$$V(z) = V_0^+ e^{-j\gamma z} + V_0^- e^{+j\gamma z}, \tag{A.10a}$$

$$I(z) = I_0^+ e^{-j\gamma z} + I_0^- e^{+j\gamma z}, \tag{A.10b}$$

For example, the two terms, $V_0^+ e^{-j\gamma z}$ and $V_0^- e^{+j\gamma z}$, in each solution describe two waves propagating in the transmission line width in different directions. In addition, this is a significant result because the functions that describe the current and voltage waves at all points along a transmission line can be completely described with four complex constants: V_0^+, V_0^-, I_0^+ and I_0^-.

A.2.2 The Characteristic Impedance of a Transmission Line

Also known as *natural impedance*, it represents the equivalent impedance of an infinite transmission line. Based on Equation A.5a and A.10a, a new expression for $I(z)$ can be found in Equation A.11.

$$I(z) = \frac{\gamma}{R + j\omega L}(V_0^+ e^{-j\gamma z} + V_0^- e^{+j\gamma z}) \tag{A.11}$$

Considering impedance as the ratio between voltage and current waves, the Equation A.12 shows the relation that defines the Characteristic Impedance of a transmission line.

$$Z_0 = \frac{V(z)^+}{I(z)^+} = \frac{-V(z)^-}{I(z)^-} = \frac{\sqrt{R + j\omega L}}{\sqrt{G + j\omega C}} \tag{A.12}$$

Note that the Characteristics Impedance of a transmission line is constant with the position z. It is not dependent on boundary conditions and is determined by the transmission line's parameters (R, L, G and C).

A.2.3 The Propagation Constant

The propagation constant is a parameter that describes how much the amplitude and phase of an electromagnetic wave change as it propagates. It is described by the Equation A.9, where $\alpha = Re\{\gamma\}$ and $\beta = Im\{\gamma\}$.

$$\gamma = \alpha + j\beta = \sqrt{(R + j\omega L)(G + j\omega C)}$$

The real part expresses the magnitude of the signal, α it is also known as **attenuation constant**, because $|e^{-\gamma z}| = e^{-\alpha z}$. A similar relation states that: $|e^{-j\beta z}| = 1$, what makes β known as the **phase constant**, since the relative phase $(\phi(z))$ (from Euller's

equation in Equation A.13).

$$e^{-j\beta z} = e^{-j\phi(z)} = \cos(\beta z) + j\sin(\beta z) \tag{A.13}$$

β has the units of radians/meter, and considering that the wavelength λ is the distance where the relative phase value is 2π, λ and β are related by the Equation A.14.

$$\beta = \frac{2\pi}{\lambda} \tag{A.14}$$

The time relation arises with the wave **propagation velocity** in Equation A.15.

$$v_p = \frac{\omega}{\beta} = \frac{\omega\lambda}{2\pi} = \lambda f \tag{A.15}$$

Where f is the frequency in Hertz.

A.2.4 The Reflection Coefficient

The Reflection Coefficient is just a way of representing the activity of a transmission line in terms of the incident and reflected waves. It is defined as the amplitude ratio of the voltage reflected wave to the incident voltage wave.

$$\Gamma(z) = \frac{V_0^- e^{-j\gamma z}}{V_0^+ e^{-j\gamma z}} \tag{A.16}$$

Now considering a transmission line of characteristic impedance Z_0 feeding a load impedance Z_L, the input impedance seen by the feed line is Z_L, and the reflection coefficient Γ is given by the Equation A.17.

$$\Gamma = \frac{Z_L - Z_0}{Z_L + Z_0} \tag{A.17}$$