Reliability Analysis of 0.5µm CMOS Operational Amplifiers under TID Effects

Guilherme S. Cardoso[1, 2], Tiago R. Balen[1], Marcelo S. Lubaszewski[1, 3] and Odair L. Gonçalez[4]

[1]UFRGS - Porto Alegre, RS, Brazil; [2]IFSul - Pelotas, RS, Brazil; [3]CEITEC-SA - Porto Alegre, RS, Brazil;
[4]Instituto de Estudos Avançados- (IEAv) São José dos Campos, SP, Brazil
gscardoso@inf.ufrgs.br, tiago.balen@ufrgs.br, luba@ece.ufrgs.br, odairl@ieav.cta.br

ABSTRACT

Analog integrated circuits operating in radiation environments. In previous irradiation experiments performed on a switched-capacitor filter, implemented in a programmable analog array, it was observed a sudden recovery of the device performance during the irradiation, while increasing the accumulated dose. In some cases the considered performance parameters (such as the total harmonic distortion) may even be enhanced if compared to the pre-irradiation measurements, in specific accumulated dose intervals. This behavior is associated to partial inactivity windows in the internal components of the device. Spice simulations considering two complementary architectures of a simple CMOS Operational Amplifier (OpAmp) are performed, aiming to understand the origins of this effect. Results indicate that shifts on the operating point of the amplifier building blocks are responsible for the degradation and recovery of the OpAmp performance. Results also show that specific architectures, as well as, application constraints (such as the external feedback and the input signal amplitude and frequency) may result in different robustness levels related to the linear applications of the OpAmps in radiation environments.

Index Terms: CMOS Operational Amplifiers, Total Ionizing Dose, Radiation Effects, Inactivity Windows.

I. INTRODUCTION

Electronic systems operating in radiation environments, such as in space applications and nuclear facilities, are exposed to significant radiation doses. Frequently, constraints associated to the budget and development time of a giving project or mission, lead to the adoption of COTS (Commercial Off-The-Shelf) devices and standard CMOS process in the developing of electronic systems to be employed in such applications [1], associated with design or system-level mitigation techniques. Moreover, with the technology scaling of standard CMOS process, the performance related to Total Ionizing Dose (TID) effects is naturally being improved due to the thinner isolation oxides of newer technologies, which reduces the charge trapping induced by ionizing radiation [2-4].

On the other hand, the scaling of analog circuits is not as aggressive as it is for the digital parts. Therefore, it is common to find commercial available analog and mixed-signal (MS) devices fabricated in older CMOS technologies as, for example, 0.5µm technology node. Moreover, these technologies are still being offered as low cost production alternatives by several foundries around the world, and represent a significant part of the semiconductor market [5], mainly when considering analog or RF applications [6]. However, the devic-

es fabricated in such technologies are more sensitive to TID effects, since some of these effects are more severe in thicker oxide technologies [7, 8].

Total Ionizing Dose (TID) is a class of cumulative radiation effects that, in electronic systems, causes the degradation of electrical characteristics of the circuit devices. Electrical degradation in MOS transistors exposed to ionizing radiation is mainly caused by the buildup of trapped charges in the isolation oxides of the integrated circuit [7]. The main consequences of oxide and interface charge buildup are shifts in the threshold voltage (V_{th}) of transistors and current leakage [7, 8].

Several works have been developed addressing important issues in the context of TID effects on analog circuits. In [2-4] the performance under radiation effects of individual parameters of CMOS analog circuits, such as the transistors drive current, transconductance, and threshold voltage, were studied. In [9, 10] experimental radiation data regarding the output offset and open loop gain of bipolar and CMOS commercial Operational Amplifiers (OpAmps) were presented. Considerations on the impact of transistors sizing on the TID effects and radiation-hardening-by-design approaches using ELT (Enclosed Layout Transistor) are discussed in [11, 12].

In a previous work of our group the effects of TID in a 0.6µm switched-capacitor (SC) programma-

ble analog device were investigated [13]. In that work it was observed a sudden recovery of the device performance during a specific interval of the irradiation phase (after significant signal degradation was established). This recovery may be associated to partial inactivity windows in the analog switches of the device as well as in the device OpAmps, as described in [13] and firstly observed in [14] on irradiated commercial analog switches.

With this in mind, this work aims to investigate the behavior of analog building-blocks of operational amplifiers under cumulative radiation effects. The main goal is to enhance the understanding of the contribution of these important subsystems in the performance degradation of the operational amplifiers exposed to ionizing radiation, and their contribution to the inactivity window effect. Two counterpart architectures of a two-stage OpAmp are considered as case study due to the inherent difference between the behavior of the NMOS and PMOS devices under cumulative radiation effects. Threshold deviations are injected into the transistors of the OpAmps' building-blocks by means of *Spice* simulations. The simulations were focused both on the behavior of intrinsic OpAmp parameters (such as the biasing currents, DC operating points and small signal transfer characteristics) and, also, on performance parameters related to the application (frequency response, harmonic distortion, and dependence on the external feedback).

This paper is organized as follows: Section II presents the previous works that motivated this study and a brief discussion on the effects of TID in MOS devices. Section III presents the simulation models employed in this work, while section IV shows the obtained results and discussions. Section V concludes this paper.

II. RELATED WORKS

A. Previous work

In a recent work of our research group, the effects of TID in a switched-capacitor (SC) programmable analog device were investigated [13]. In that work the THD (Total Harmonic Distortion) of the signal processed by a second order analog SC filter, programmed into the device, was monitored during the device irradiation with a Cobalt-60 gamma ray source. It was observed a sudden recovery of the THD during a specific window of the irradiation phase. This fail-recovery pattern may be associated to partial inactivity windows in the analog switches of the device as well as in the device OpAmps, as described in [13] and firstly observed in [14] on irradiated commercial analog switches.

In order to discard the possibility of any mea-

surement error or environmental interference, we repeated the experiment with another sample of the device. However, a different analog hardware was programmed into the Field Programmable Analog Array (FPAA) under study. Similarly to the first experiment, we programmed two band-pass filters into the device. In addition, we also tested a continuous anti-aliasing filter that is available in the I/O cells of this FPAA.

This new experiment produced very similar results to those of the first experiment. The THD of the signals at the output of the monitored filters presented a significant variation in respect to the accumulated dose. At the beginning of the experiment, the THD was near 2%, reaching approximately 20% few minutes before the complete failure of the device. However, between these two extremes, the harmonic distortion did not show a monotonic behavior. As depicted in Fig 1, the THD started to increase, with an exponential trend, when the dose reached approximately 12krad. Then, when the total accumulated dose reached 17.5krad, the harmonic distortion suddenly decreased and started to increase again with the same trend presented before. At 22.5krad the circuit lost its functionality.

B. Effects of TID on MOS transistors

As one will see in the remainder of this paper, the behavior observed on the irradiation experiments is associated to the degradation of the electrical characteristics of the device transistors.

Electrical degradation in MOS transistors exposed to ionizing radiation is mainly caused by the buildup of trapped charges in the isolation oxides of the integrated circuit [7]. The main consequences of oxide and interface charge buildup are shifts in the threshold voltage (V_{th}) of transistors and current leakage [7, 8].

The complementary transistors (NMOS and PMOS) present different characteristics regarding the TID-induced charge buildup at the oxide and at
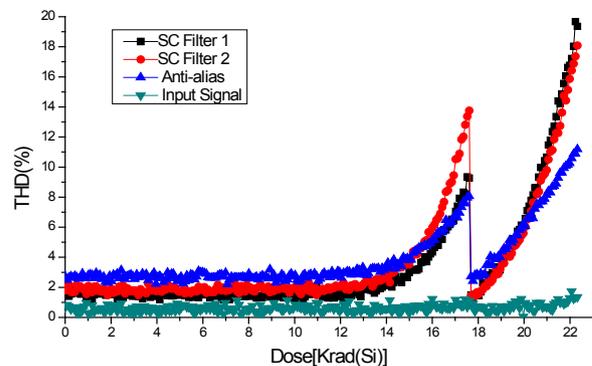
Figure 1. Total Harmonic Distortion evolution of output signals of three analog Filters programmed in an SC-FPAA, as function of the accumulated dose, in a practical TID experiment [13].

the oxide-silicon interface. The oxide-trapped charges are usually positive for both devices while the interface-trapped charges are typically positive for PMOS transistors and negative for NMOS transistors [7]. For this reason, while the net charge accumulated in PMOS transistors is always positive, leading to negative deviations of the threshold voltage, the net charge accumulated in NMOS transistors may be positive, neutral or negative. Therefore, the threshold voltage shifts of irradiated NMOS transistors may be positive or negative. Moreover, for moderate dose rates and exposure times the contribution of each mechanism on the deviations of the threshold voltage (ΔV_{it} and ΔV_{ot}) is significant [7]. In addition, according to [15] the interface charge buildup is slower than the buildup of oxide trapped-charges buildup. This behavior is taken into account in the simulations performed in this work as it will be presented in section III.

III. SIMULATION SETUP

Considering this different characteristic regarding the TID-induced threshold deviations on NMOS and PMOS transistors, we selected two counterpart operational amplifiers as case study. Both architectures consist in a two stage amplifier with miller compensation, as can be seen in Fig 2. The configuration depicted in Fig 2(A) comprises a PMOS differential amplifier as input stage (M1(A) and M2(A)) and the second stage is composed by a common-source amplifier (M6(A)). From here on, this configuration will be referred as PMOS Differential Amplifier (PMOS-DA). Fig 2(B) shows the counterpart architecture, in which the first stage is now composed of an NMOS differential pair (M1(B) and M2(B)) and the output stage is composed of a PMOS transistor (M6(B)). This configuration is referred, in this work, as NMOS Differential Amplifier (NMOS-DA).

In order to understand the role of each OpAmp stage on the observed behavior of the irradiated circuits (fail-recover-fail), each OpAmp was partitioned in two building blocks, as can be seen in Fig 2. Fig 2(C) and 2(E) show the input and output stages of the PMOS-DA architecture, respectively. The NMOS-DA building blocks are depicted in Figs 2(D) and 2(F).

The sizing of the OpAmp components considered in this work is summarized in Table I. Both designs have similar specifications, as follows:

- $Iss=10\mu A$,
- Gain-Bandwidth=1MHz,
- CL=20pF
- CMR from -2V to +1V (PMOS-DA) and from -1V to +2V (NMOS-DA).

On the functional point of view, these two complementary amplifiers have no significant difference.
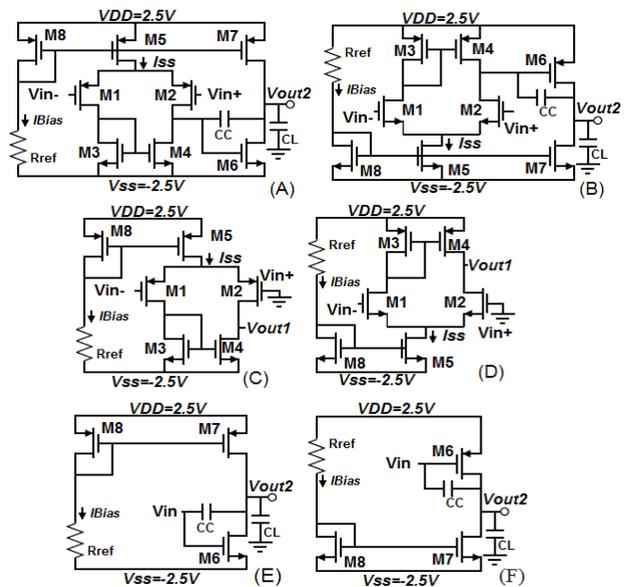
Figure 2. Schematic of the investigated architectures: (A) PMOS-DA OpAmp; (B) NMOS-DA OpAmp; (C) PMOS-DA Input stage; (D) NMOS-DA Input stage; (E) PMOS-DA Output stage; (F) NMOS-DA Output stage.

Table I. Sizing of the components of both OpAmps.

Transistors	PMOS-DA(W/L)[μm]	NMOS-DA(W/L)[μm]
M1, M2	4/1	1.5/1
M3, M4	1/1	5/1
M5	2.5/1	1.5/1
M6	24/1	60/1
M7	30/1	9/1
M8	2.5/1	1.5/1
Capacitor CC	4.4pF	4.4pF
I_{Bias}	10μA	10μA

However, it is important to take care to achieve a good matching between M1-M2 and M3-M4 (Figure 2 (A or B)). This can be accomplished by employing layout techniques, especially on the differential pair stages.

Regarding Radiation Hardened-By-Designed (RHBD) techniques, a popular layout technique applied to digital circuits to cope with TID is the Enclosed *Layout Transistor* (ELT) [11, 12]. However, design of analog circuits with this technique is not a very simple task, since it does not allow arbitrary W/L ratios required in analog designs. For this reason, investigation of architectural implications in radiation hardness of analog blocks, while using conventional transistors, is also important to the design phase of an analog or mixed-signal system.

The effects of charge buildup due to TID were simulated by injecting threshold shifts in the transistors model, directly in the model cards of the considered technology (AMI 0.5μm). The injected deviations

were carried out according to the typical behavior of the threshold voltage shifts (according to [14]) for the dose rate applied in the practical experiment previously performed by the authors (1krad/h), whose results have motivated this investigation [13]. This behavior is depicted in Fig. 3. Therefore, 124 spice files modeling different V_{th} deviations were generated. Considering also the nominal condition, 125 files were individually simulated using HSpice®. One additional Matlab® code was used to compute the results from the 125 *Spice* output files.

Several analyses were carried out through these simulations. DC analyses were performed to check the linearity of the OpAmp stages and the mobility of operating point due to the threshold deviations. At this point, Monte Carlo simulations were carried out to investigate the combined effect of TID-induced V_{th} shifts with mismatches of this parameter between the transistors of the input differential pair. The biasing current was also evaluated in these simulations. Finally, transient analyses were performed to investigate the behavior of the OpAmp when used in an inverter amplifier configuration, with different closed loop gains (external feedback factor) and frequencies of the input signal.

IV. SIMULATION RESULTS

More than one hundred of V_{th} combinations (for PMOS and NMOS transistors) were injected, to simulate the threshold voltage degradation caused by TID. However, in order to simplify the results presentation, seven points representing important V_{th} combinations were selected to be displayed. These combinations represent different values of accumulated dose, and are highlighted in 3 (markers 1 to 7).

The first point simulates the *pre-rad* situation (nominal values of V_{thN} and V_{thP}). Between the second and forth points V_{thN} goes negative, configuring
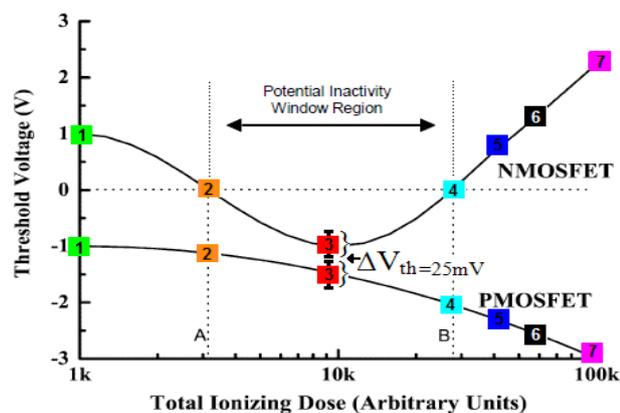
a potential inactivity window, into which it is expected the partial or total failure of the OpAmps or some of their components. Samples 5 to 7 represent the most aggressive situation, when the transistors present high shifts in their threshold voltages.

It is important to point out that in our previous experiments, the transistors threshold voltage could not be measured and the exact correspondence of this parameter to the accumulated dose is unknown. Also, there is no comprehensive available data on the literature concerning TID induced threshold deviations for this technology. For this reason we adopted the qualitative degradation pattern depicted in Fig 3. This figure represents the threshold deviation behavior versus the accumulated dose.

In this case the dose is shown in arbitrary units, since the exact V_{th} behavior depends on several factors, such as the fabrication technology, transistors' sizing, DC operating point, external operation conditions and also the dose rate to which the devices are exposed. However, as one will see on the results of this work (in the following sub-sections) this degradation model for the V_{th} parameter produced similar simulation results to that observed in the practical experiments previously performed. As an example, in one of our experiments the partial inactivity window occurred nearly from 13krad up to 17.5krad, as can be noticed in Fig 1.

A. Input stage DC analysis

Fig 4 shows the behavior of the bias current (Iss) for NMOS-DA and PMOS-DA architectures. The nominal value of the bias current is 10μA. During the potential inactivity window the bias current of the NMOS-DA amplifier increases. Conversely, the PMOS transistor presents negative V_{th} shifts, decreasing the bias current of the PMOS-DA configuration. Nevertheless, during the potential inactivity window, for both topologies the biasing current is not interrupted. This occurs only in point 6 for PMOS-DA and near point 7, for NMOS-DA, as can be noticed in Fig 4.

Figs 5 and 6 show the DC analysis results for the differential amplifier architectures, from which the small signal behavior of these blocks may be obtained. The curves highlighted with the number 1 (on both figures), represent the nominal response of the differential amplifier blocks. It is possible to see that both PMOS-DA and NMOS-DA present a high and linear gain near 0V on the "V_{in-}" axis. When V_{thN} is negative (situation 3), the operating point of the PMOS-DA amplifier is pushed to a strongly non-linear region, seriously degrading the OpAmp performance.

The same did not occur with the NMOS-DA differential amplifier, to which the operating point remains in the linear range with an adequate linear voltage swing possibility. An exception is observed to the worst
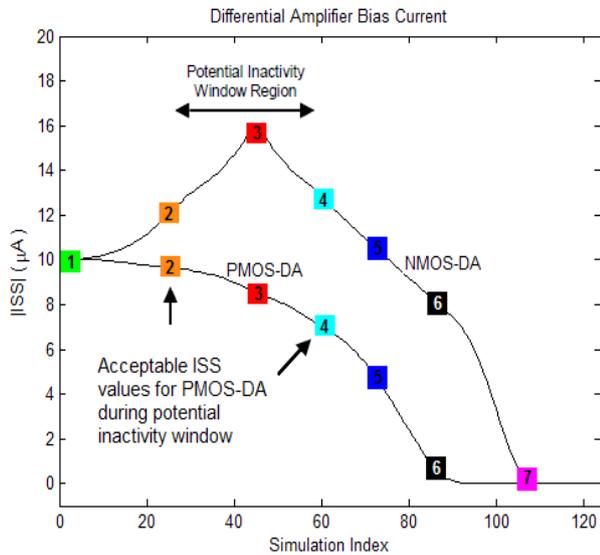
Figure 3. V_{th} deviation behavior considered in the simulations (adapted from [14]).

Figure 4. Behavior of bias current (*Iss*) for the PMOS-DA and NMOS-DA due to the injected threshold deviations.
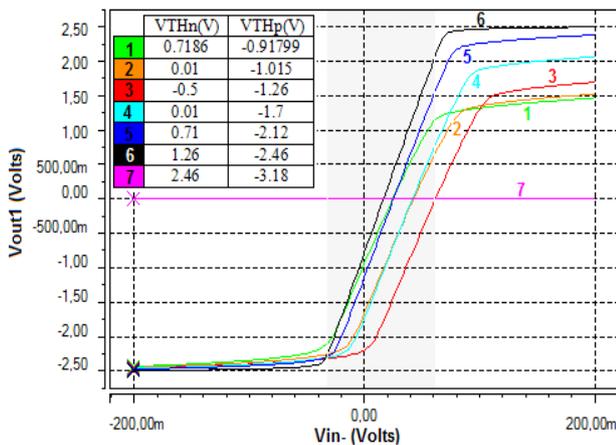

Figure 5. Small signal characteristic of the PMOS-DA differential amplifier.
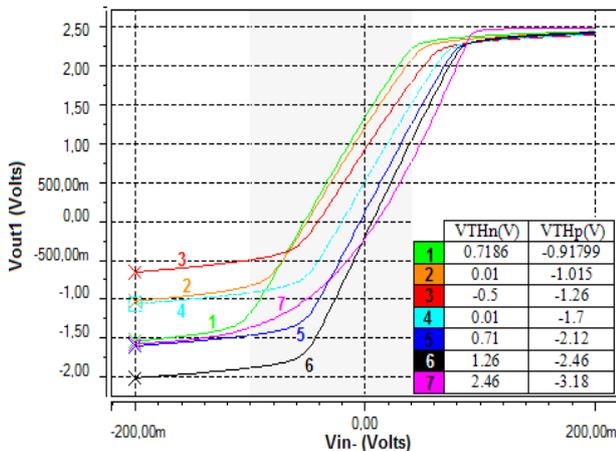

Figure 6. Small signal characteristic of the NMOS-DA differential amplifier.

case condition (situation 7) when the threshold voltages of NMOS transistors are near V_{DD} and PMOS transistors are below V_{SS}. In this situation the behavior of the NMOS-DA is no longer linear and the PMOS-DA is no longer functional, as can be seen in Figs 5 and 6. This occurs because the drain voltage of M5 assumes the maximum allowed voltage (V_{DD}), thus, in this case $|V_{DS}|$ of M5 is 0V. Even if $|V_{GS}|$ exceeds V_{thP}, $|V_{DS}|$ is always 0V and no current flows through the drain of M5. The same occur with the NMOS-DA architecture, when V_{thN} is beyond V_{DD}, M5 is off and there is no current flowing.

The nominal DC operating point of NMOS and PMOS differential amplifiers are highlighted (with a black dot) on Figs 5 and 6. One can notice that PMOS-DA operating point tends to be negative while the NMOS-DA OP is positive. Although the NMOS-DA OP is closer to V_{DD} if compared to the distance of PMOS-DA OP from V_{SS}, the NMOS input stage is more robust compared to its counterpart, considering the OP mobility. This is because the voltage V_{out1} tends to move towards V_{SS}, while for NMOS-DA input stage this voltage moves away from V_{DD}, as the V_{th} of the transistors are shifted.

Fig 7, shows the behavior of the OP of both input amplifier architectures. It is possible to see that the shifts on NMOS-DA OP follow the same trend of the threshold shifts injected in PMOS transistors, while the operating point of PMOS-DA vary similarly to the NMOS threshold deviations considered (according to the pattern depicted in Fig 3). The reason for that is because the main responsible to set the DC OP voltage (V_{out1}) are the active loads of both architectures (M3 and M4) that are composed of PMOS transistor on the NMOS-DA stage and NMOS transistors on the PMOS-DA block.

One can conclude from these analyses that the design specifications of the OpAmp can influence the circuit robustness. It occurs because the performance
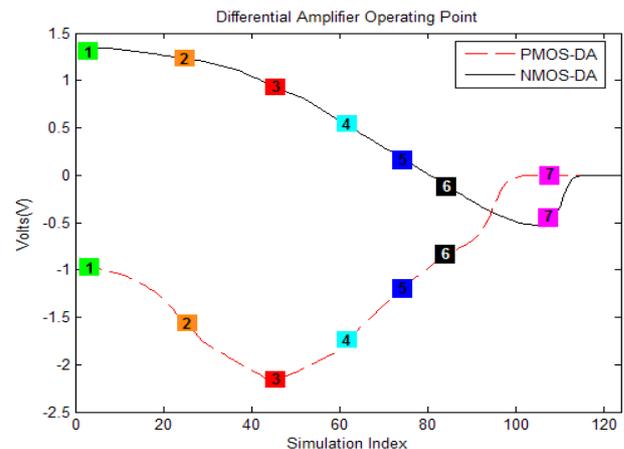

Figure 7. Input stage operating point tendency for both NMOS-DA and PMOS-DA architectures, during the V_{th} shifts simulation.

requirements define the transistors sizing, which, in turn, defines the operating point of the circuit.

Thereby, it is intuitive to think that the OP must be allocated far from power supply voltage rails to increase the robustness regarding TID effects. Considering symmetric power supply, it could be convenient to set 0V for the OP voltage, especially for PMOS-DA configuration. It may be achieved by correct adjust of transistors M1-M5 aspect ratio. However, the tradeoff of this arbitrary adjustment is the systematic offset that may appear at the output stage. For this reason, this condition is not always possible to achieve, due to design constraints.

B. Monte Carlo analysis of differential pair

Monte Carlo (MC) simulations were also performed, in order to investigate the influence of V_{th} mismatches among transistors M1, M2, M3 and M4 (input stage). These analyses were performed, specifically, for V_{th} values inside the potential inactivity window (as highlighted in Fig 3), with a maximum deviation from the central value of 25mV (3σ) [16]. Figs 8 and 9 show the results of 1000 MC iterations for both OpAmp architectures. The central curves represent the responses with zero mismatch (V_{thN}=-0.5V and V_{thP}=-1.26V, for all transistors).

Taking into account the same pattern simulated for both architectures, it is possible to observe that, for the NMOS-DA block, the non-linear regions of the differential amplifier were not achieved in any case inside this window, as can be seen in Fig 9. The same did not occur with the PMOS-DA topology, to which in most MC iterations the operating point is shown to be in a non-linear region as can be observed in Fig 8 (near marker 2). It is possible to conclude from these analyses that mismatches between the threshold voltage of input transistors play an important hole on the performance of the amplifiers under radiation, since, for a given radiation induced threshold deviation (mean) the random factor can define between the functionality or inactivity of the block. An appropriate layout of the differential pairs may also be relevant to the robustness of this block.

C. Output amplifier DC analysis

The individual behavior of output stages was also investigated. These building-blocks comprise transistors M6 – M8, as depicted in Figs 2(E) and 2(F). A DC analysis was carried out with the input voltage (V_{in}) varying from -2.5V to 2.5V. Considering the complete OpAmps, the output signal of the differential amplifier, V_{out1} (Figs 2(C) and 2(D)), drives the input of the output stage (V_{in} in Figs 2(E) and 2(F)). The operating point of this building block is the input voltage to which the amplifier presents a high and linear
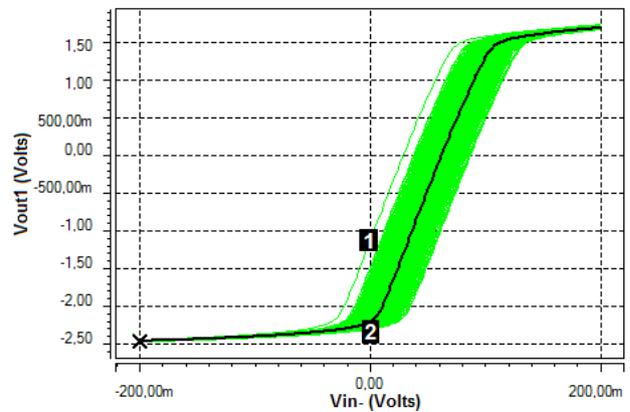

Figure 8. Monte Carlo simulations of the differential amplifier in the PMOS-DA architecture, considering Vth mismatches among the input transistors.
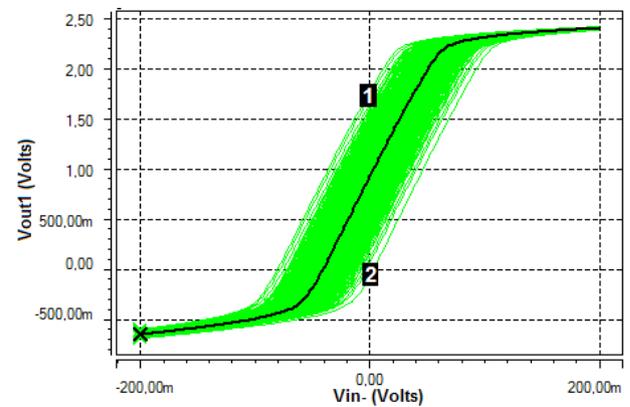

Figure 9. Monte Carlo simulations of the differential amplifier in the NMOS-DA architecture, considering V_{th} mismatches among the input transistors.

gain. In the nominal combination of threshold voltage (fault-free condition), for PMOS-DA output stage, the operating point is close to -1.2V in 'V_{in}' axis, as depicted in Fig 10 (curve 1).

The critical situation occurs when V_{th} parameter of NMOS transistors goes negative, which means that M6 (Fig 3(A)) is operating in strong inversion, and therefore, any voltage between drain and source is sufficient for M6 to present a high drain current. In this situation the NMOS transistor pull down the output to V_{ss}, as can be observed in Fig 10 (curve 3). The evolution between situations 3 and 4 (V_{thN} from -0.5V to 0.01V and V_{thP} from -1.26V to -1.7V) is depicted in curves 3.D to 3.A, which shows the recovery of the output stage of the PMOS-DA architecture. A similar behavior is observed when the V_{th} deviation goes from sample 2 to 3 i. e., entering in the partial inactivity window, but, in this case, the evolution is in the opposite direction (3.A to 3.D), degrading the transfer characteristic of the output stage.

Fig 11 shows that the operating point of the NMOS-DA output stage also presents a variation around the nominal value, but not strong enough to degrade its linearity. This shift can lead to an increase in the output systemic offset if the shift in the OP of the input stage does not vary in the same way.

D. Frequency performance on a closed loop configuration

Both counterpart amplifiers were designed to achieve 1MHz Gain-Bandwidth (GBW) parameter. Fig 12 shows the simulated frequency response of the PMOS-DA OpAmp, employed in an inverter configuration with a closed loop gain equal to 10 and considering the same V_{th} deviations adopted on the DC analysis. No significant change in the frequency response is observed until the threshold deviations achieve the values of situation 2 (marker 2 on the related figures). However, inside the considered inactivity window (situation 3), it is possible to notice a degradation in

the frequency response. The GBW of the PMOS-DA OpAmp is recovered when considering threshold voltage deviations higher than the upper limit of the window (situation 4). The NMOS-DA OpAmp remains fully operational for all combinations of V_{th} until the situation 6, as can be observed in Fig 13.

One can notice that, for both counterpart amplifiers, TID induced threshold voltage deviation did not change the rolloff factor of the frequency response. On the other hand, the frequency of the first pole can be slightly modified, as can be seen in Figs 12 and 13.

The numerical value of the GBW parameter is shown in Fig14, as a function of the simulated evolution of threshold shifts. Regarding the PMOS-DA architecture, the inactivity window effect is well evidenced near marker number 3. With the corresponding threshold deviations within this window the output signal is always fully attenuated, thus the GBW parameter was not evaluated. On the other hand, the NMOS-DA topology shows an improvement of the
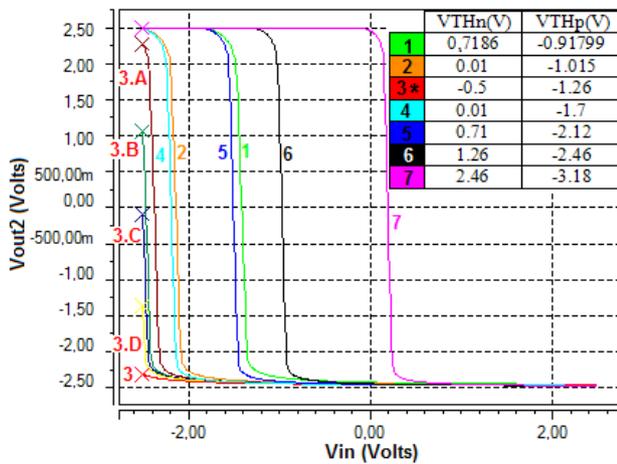

	VTHn(V)	VTHp(V)
1	0,7186	-0.91799
2	0.01	-1.015
3 ★	-0.5	-1.26
4	0.01	-1.7
5	0.71	-2.12
6	1.26	-2.46
7	2.46	-3.18

Figure 10. Behavior of the output stage of the PMOS-DA OpAmp.

	VTHn(V)	VTHp(V)
1	0.7186	-0.91799
2	0.01	-1.015
3	-0.5	-1.26
4	0.01	-1.7
5	0.71	-2.12
6	1.26	-2.46
7	2.46	-3.18
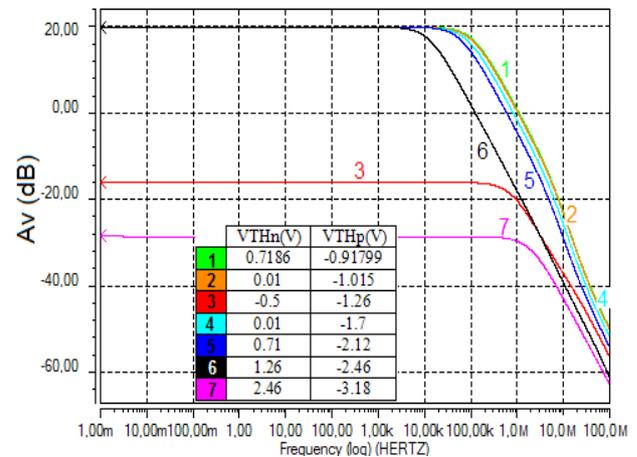
Figure 12. Frequency response of the PMOS-DA OpAmp.

	VTHn(V)	VTHp(V)
1	0.7186	-0.91799
2	0.01	-1.015
3	-0.5	-1.26
4	0.01	-1.7
5	0.71	-2.12
6	1.26	-2.46
7	2.46	-3.18
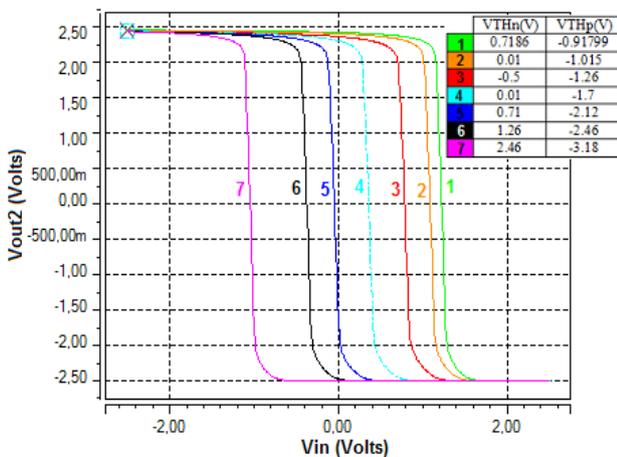
Figure 11. Behavior of the output stage of the NMOS-DA OpAmp.

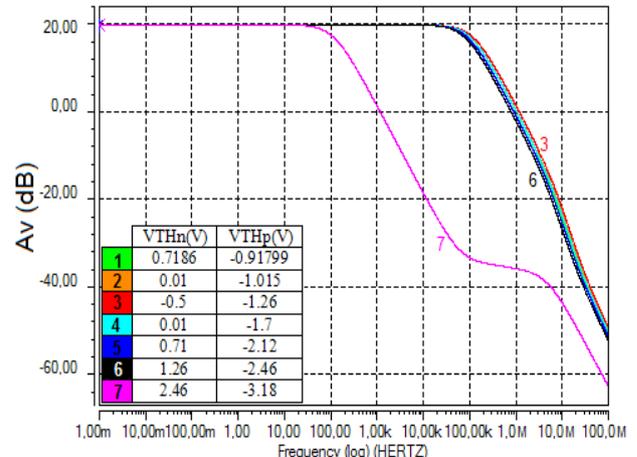|	VTHn(V)	VTHp(V)
1	0.7186	-0.91799
2	0.01	-1.015
3	-0.5	-1.26
4	0.01	-1.7
5	0.71	-2.12
6	1.26	-2.46
7	2.46	-3.18

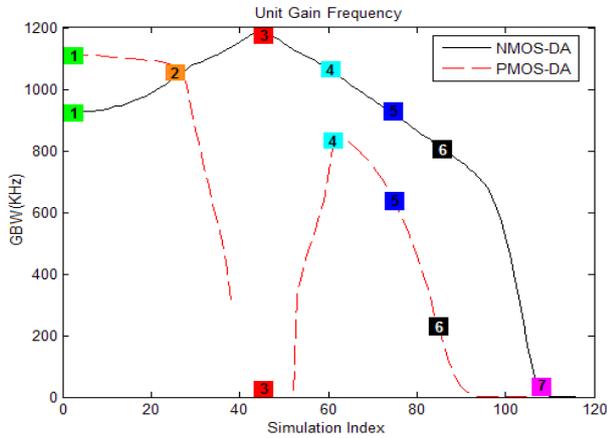**Figure 13.** Frequency response of the NMOS-DA OpAmp.

Figure 14. Gain-Bandwidth behavior of both OpAmp architectures.

GBW parameter until the situation 3, comparing to the *pre-rad* performance. It can be explained due to the increasing of the bias current (I_{SS}), as can be noticed in Fig 3, since the GBW is directly proportional to this current [17].

The influence of the input frequency and the external feedback were also briefly investigated by means of transient simulations. For this purpose, three configurations concerning the input frequency (f_i) and closed loop gain (G) of an inverter amplifier were considered: 1) $G=1$ and $f_i = 10kHz$; 2) $G=1$ and $f_i = 1MHz$; 3) $G=20$ and $f_i = 10kHz$. Figs 15 to 17 show the output signal for each condition with superimposed signals representing 3 distinct situation of threshold deviations: **before** the partial inactivity (27 iterations of injected V_{th} shifts between situations 1 and 2), **during** the partial inactivity (36 iterations) and **after** the in-
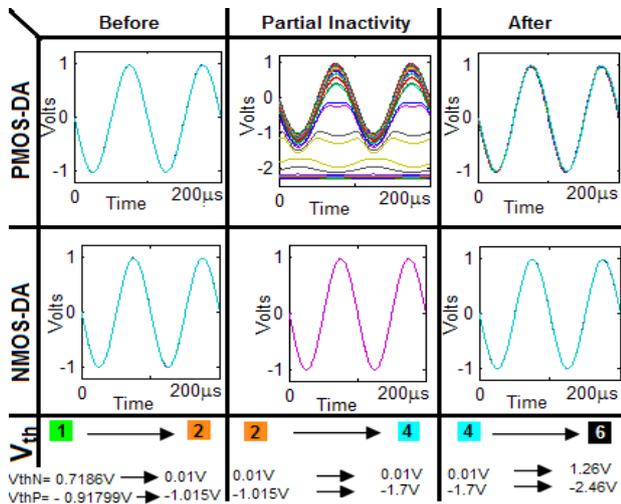

Figure 16. Time domain behavior of both OpAmp architectures in an inverter configuration with unit gain and 1MHz as input frequency, considering 89 combinations of threshold deviation following the trend presented in Fig 3.
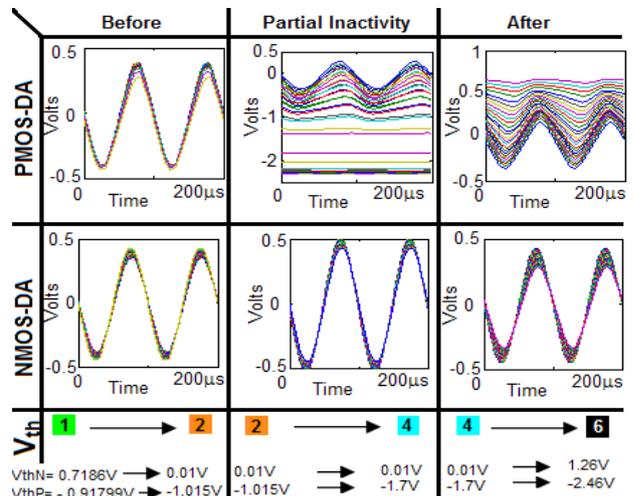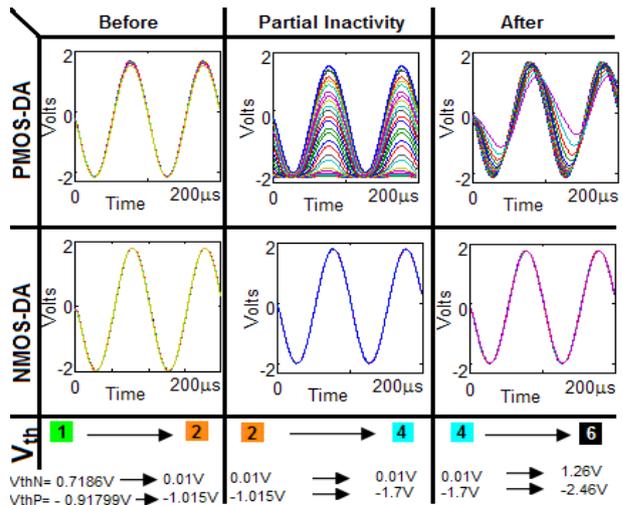

Figure 17. Time domain behavior of both OpAmp architectures with close loop gain equal to 20 (inverter configuration) and 10KHz as input frequency, considering 89 combinations of threshold deviation following the trend presented in Fig 3.

Figure 15. Time domain behavior of both OpAmp architectures in an inverter configuration with unit gain and 10KHz as input frequency, considering 89 combinations of threshold deviation following the trend presented in Fig 3.

activity window (26 iterations). The total number of superimposed curves is 89.

When the input frequency and/or closed loop gain are increased (reducing the feedback factor), the differential voltage at the OpAmp is increased, forcing it to work in a wider range of the differential and inverter amplifiers voltage swing. This increases the possibility that the non-linear regions of the transfer curve of the amplifier stages (Figs 5 and 6, for example) be reached by the internal signals. As a result, it may affect the robustness of the OpAmps related to TID-induced threshold voltage deviations. This dependency can be noticed in Figs 15 to 17.

Fig 18 illustrates the increase of the amplitude signal at the OpAmp differential input when increasing the closed loop gain (reducing the negative feedback) and the signal frequency, considering the PMOS-DA topology. For the NMOS-DA OpAmp, no catastrophic change was observed at the output signal to all the 89 simulated iterations of each combination (gain and amplitude).

The OpAmp DC gain is inversely proportional to I_{SS} [17], whose tendency during the inactivity window is depicted in Fig 4. Regarding the PMOS-DA architecture, the DC gain during the inactivity window is well evidenced, as can be seen in Fig 19.

The THD of the output signal was also evaluated in the simulations, considering 100 harmonics. Results are shown in Fig 20, in which the inactivity windows for the PMOS-DA architecture can be noticed. A similar behavior was observed in our practical radiation experiments [13].
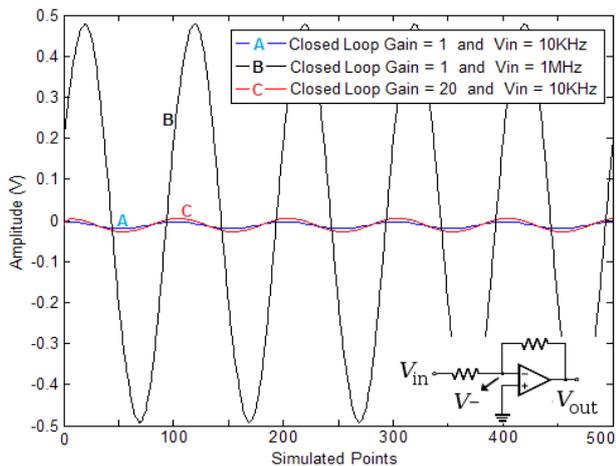
Figure 20. THD of the signals at the output of both OpAmps.

E. Output offset analysis

Finally, the OpAmp output offset voltage was also monitored considering an inverter configuration with unit gain. Taking into account the threshold voltage deviation simulated in this work for both amplifiers, it is possible to observe the effect of partial inactivity window in PMOS-DA architecture (between markers 2 and 4 of Fig 21). In this window the OpAmp fails, reducing the DC level of the output to near VSS. After this window the PMOS-DA recovers its normal operation condition, showing a similar offset of that presented in nominal situation.

Considering the NMOS-DA topology, no important modification was observed on the offset voltage until its complete failure, near situation 7 (final iterations of the injected threshold deviations).

Figure 18. Inverter input signal (V-) of the PMOS-DA OpAmp with the non-inverter input connected to ground, in an inverter amplifier configuration.
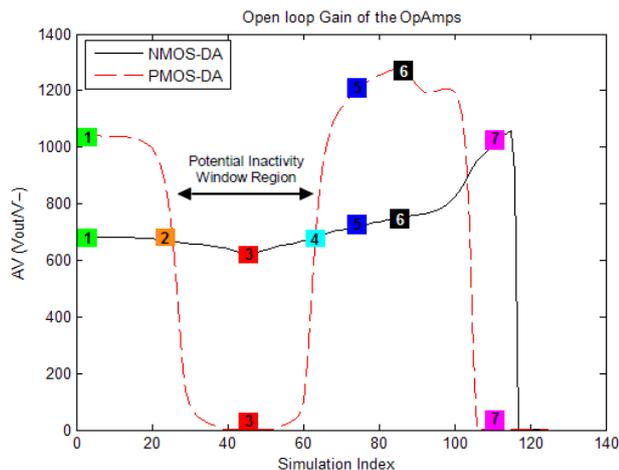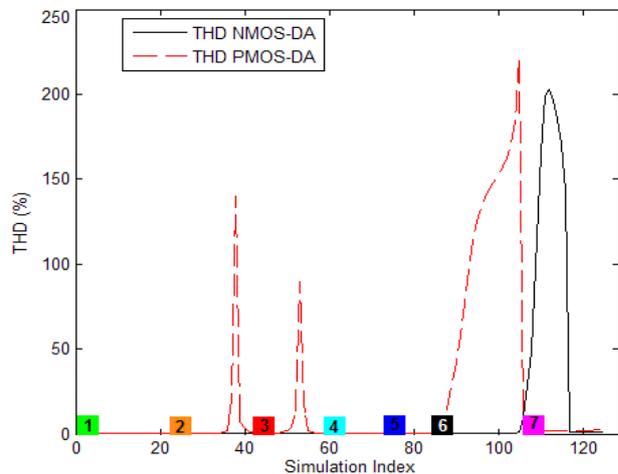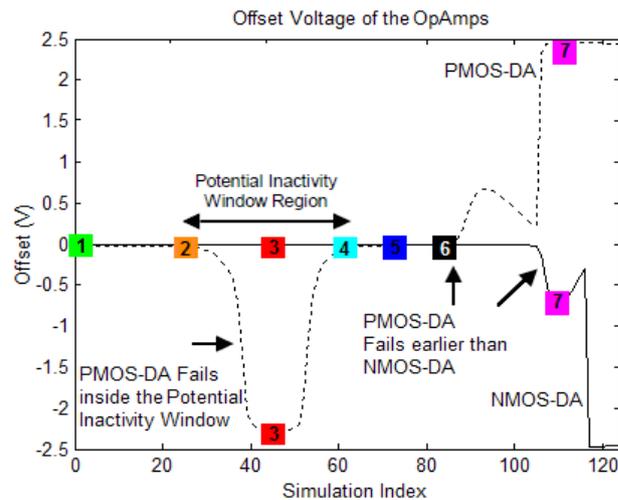
Figure 19. Behavior of DC gain for PMOS-DA and NMOS-DA architectures.

Figure 21. Offset voltage of the complete OpAmp with PMOS-DA and NMOS-DA architecture.

V. CONCLUSIONS

In this work the impact of TID-induced threshold deviations on the building-blocks of two complementary OpAmp topologies was studied. Results help to understand the inactivity window effect observed in previous radiation experiments. The threshold shifts induced by TID alter the biasing current and the transistors electrical characteristics, tending to pushing them to an operation condition outside the saturation region. This may lead to shifts on the operating point of the internal stages, in a way that the linearity of the OpAmp building blocks is no longer guaranteed. Additionally, some operation conditions related to the feedback factor and the input signal frequency and amplitude, may evidence the inactivity window effect.

Considering the radiation-induced threshold deviation pattern simulated in this work, the PMOS-DA amplifier clearly showed the partial inactivity window effect. No catastrophic effect was observed, into the same window, to NMOS-DA architecture, indicating that the NMOS differential amplifier architecture may present an improved robustness in radiation environments, since it can maintain its functionality for the same degradation conditions to which the PMOS architecture fails.

Finally, despite the OpAmps that were investigated in this work are simple 2-stage configurations, their building blocks are the same that are used in more complex architectures. This way, it is expected these results can be extended to such architectures.

ACKNOWLEDGMENTS

REFERENCES

[1] Johnston, A.H.; Lee, C.I.; Rax, B.G.; Shaw, D.C.; "Using commercial semiconductor technologies in space", Radiation and its Effects on Components and Systems – RADECS -, pp 175-182, 1995.

[2] Re, V.; Manghisoni, M.; Ratti, L.; Speziali, V.; Traversi, G.; "Total ionizing dose effects on the analog performance of a 0.13μm CMOS technology", IEEE Radiation Effects Data Workshop, pp. 122 – 126, 2005.

[3] M. Manghisoni, L. Ratti, V. Re, V. Speziali, G. Traversi,; A. Candelori, "Comparison of ionizing radiation effects in 0.18 and 0.25 μm CMOS technologies for analog applications", IEEE Transaction on Nuclear Science, vol. 50, No. 6, pp. 1827-1833, 2003.

[4] Osborn, J.V.; Lacoe, R.C.; Mayer, D.C.; Yabiku, G.. "Total dose hardness of three commercial CMOS microelectronics foundries", Radiation and its Effects on Components and Systems – RADECS- pp. 265-270, 1997.

[5] Leibson. S. "Where is the mainstream IC process technology today? 28nm? 40nm? 65nm?", 2011. Available-on line in: <http://eda360insider.files.wordpress.com/2011/09/foundry-capacity-by-technologies.jpg>, Accessed on Sept. 2013.

[6] Goering, R. "GTC Panel: Getting Best Use From Older IC Process Nodes", 2011. Available on-line in: <http://www.cadence.com/Community/blogs/ii/archive/2011/09/05/gtc-panel-older-ic-process-nodes-deserve-some-respect.aspx?CMP=home>, Accessed in Sept. 2013.

[7] J. R. Schwank, M. R. Shaneyfelt, , D. M. Fleetwood, J. A. Felix, P. E. Dodd, P. Paillet and V. Ferlet-Cavrois. "Radiation Effects in MOS Oxides". IEEE Trans. Nuclear Science, Vol. 55, No. 4, pp. 1833-1853, August, 2008.

[8] R. D. Schrimpf. "Radiation Effects in Microelectronics" In: Velazco, R; Fouillat; P; Reis, R. (Org.). "Radiation Effects on Embedded Systems". Springer, 2007, p. 11-29.

[9] Hiemstra, D.M. "High total dose performance of various commercial off the shelf operational amplifiers during irradiation", IEEE Radiation Effects Data Workshop, pp. 32-38, 2000.

[10] Guckenberger,D.; Hiemstra,D.M. "Simultaneos cryogenic temperature (77K) and total dose ionizing radiation effects on COTS amplifiers", IEEE Radiation effecs Data Workshop, pp. 14-18, 2001.

[11] Verbeeck,J.; Leroux, P.; Steyaert, M.; "Radiation effects upon the mismatch of identically laid out transistor pairs", IEEE international Conference on Microelectronic Test Structures, pp- 194-197, 2011.

[12] Djezzar, B.; Smatti, A.; Amrouche,A.; Kechouane, M.. "Channel-Length impact on radiation–induced threshold-voltage shift in N-MOSFET devices at low gamma ray radiation doses", IEEE Transaction on Nuclear Science. Vol 47, N°1, pp. 1872-1878, 2000.

[13] T. R. Balen, R.G. Vaz, G. S. Cardoso, O. L. Gonçalez and M.S. Lubaszewski, "TID in a Switched-Capacitor FPAA: Degradation and Partial Inactivity Windows due to Compensating Effects in MOS Transistors". IEEE Trans. Nuclear Science, Vol. 58, N. 5, 2011.

[14] F. J. Franco; Y. Zong; J. A. Agapito. "Inactivity windows in irradiated CMOS analog switches". IEEE Trans. Nuclear Science, v. 53, n. 4, p. 1923-1930, 2006.

[15] Shaneyfelt, M.R.; Schwank, J.R.; Fleetwood, D.M.; Winokur, P.S.; Hughes, K.L.; Hash, G.L.; Connors, M.P.; , "Interface-trap building rates in wet and dry oxides". IEEE Trans. Nuclear Science , vol.39, no.6, pp.2244-2251, Dec 1992.

[16] Lacoe, R.C.; Osborn, J.V.; Mayer, D.C.; Brown, S.; Hunt, D.R.; , "Total-dose radiation tolerance of a commercial 0.35 μm CMOS process". Radiation Effects Data Workshop, 1998. IEEE , pp.104-110, 24 Jul 1998.

[17] P Allen and D. Holberg, "CMOS analog circuit design". New York: Holt-Rinehart and Winston, 1987.