Testing a Fault Tolerant Mixed-Signal Design Under TID and Heavy Ions

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Abstract— **This work presents results of three distinct radiation tests performed upon a fault tolerant data acquisition system comprising a design diversity redundancy technique. The first and second experiments are Total Ionizing Dose (TID) essays, comprising gamma and X-ray irradiations. The last experiment considers single event effects, in which two heavy ion irradiation campaigns are carried out. The case study system comprises three analog-to-digital converters and two software-based voters, besides additional software and hardware resources used for controlling, monitoring and memory management. The applied Diversity Triple Modular Redundancy (DTMR) technique, comprises different levels of diversity (temporal and architectural). The circuit was designed in a programmable System-on-Chip (PSoC), fabricated in a 130nm CMOS technology process. Results show that the technique may increase the lifetime of the system under TID if comparing with a non-redundant implementation. Considering the heavy ions experiments the system was proved effective to tolerate 100% of the observed errors originated in the converters, while errors in the processing unit present a higher criticality. Critical errors occurring in one of the voters were also observed. A second heavy ion campaign was then carried out to investigate the voters reliability, comparing the the dynamic cross section of three different software-based voter schemes implemented in the considered PSoC.**

Index Terms— **Design Diversity Redundancy; Mixed-Signal; Radiation; Single Events; Soft Errors; Fault Tolerance; Analog-to-Digital Converters; Programmable device; PSoC.**

I. Introduction

Ionizing radiation effects in integrated circuits (ICs) significantly affects the reliability of electronic systems exposed to such environmental condition. Although soft errors caused by Single Event Effects (SEEs) in modern electronics configure a significant reliability problem [1], [2], and may even be destructive in some cases [3], Total Ionizing Dose (TID) effects are determinant to the system lifetime, when operating in radiation environments [4].

Electronic systems applied to control, instrumentation and communication tasks comprise mixed-signal interfaces that include Analog-to-Digital Converters (ADCs). These circuits are crucial in satellites, spacecrafts and data acquisition systems of nuclear facilities and particle accelerators, for instance. Therefore, as important as the correct functioning of computing units and digital system parts, is the reliability of analog-to-digital (AD) and digital-to-analog (DA) system interfaces. Examples of works in which reliability to radiation effects and mitigation techniques were evaluated in such blocks can be found in [5, 6, 7, 8, 9, 10, 11].

In a previous work of our research group a fault-tolerant data acquisition system (DAS) was proposed to cope with radiation effects and other environmental degradation sources [7, 12, 13, 14]. The system was designed and programmed in a Commercial Programmable System-on-Chip (PSoC) from Cypress Semiconductor (now Infineon Technologies) [15] fabricated in a 130 nm CMOS process. The adopted fault tolerance strategy is based on diversity redundancy, with hardware and time redundancy, in a way that the DAS is composed of three ADCs operating in parallel and two voters. In previous works, we firstly performed an intensive fault injection campaign, by using a fault injection system based on a pseudo-random number generator implemented in an auxiliary board, to select the memory and bit positions, to insert the faults, and software interruption to perform the bit-flip injection routine [16].

In fact, a PSoC device was already tested under fault injection in a related work [17]. However, the experiment was directed to a device from the first generation of the PSoC family (comprising a simple 8-bit processor). The target application in that work was purely digital (matrix multiplication), to which no mitigation technique was applied.

In the current work, the studied device pertains to the third generation of PSoC family from Cypress Semiconductor (comprising a 32 bit ARM processor). Additionally, the application is a fault tolerant mixed-signal system based on design diversity, comprising

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three ADCs, besides digital hardware and software resources for controlling the converters and the direct memory access, as well as to perform the voting. Therefore, this design implements a Mixed-Signal Design Diversity Triple Modular Redundancy (MS-DTMR) technique.

In this work we compile results of several radiation experiments we performed upon the above mentioned system prototyped in the PSoC device [12, 13, 18]. Results include TID (Cobalt-60 and X-ray) experiments, as well as two heavy ion campaigns. This way, this work presents significant results showing the effectiveness of the radiation tolerance technique proposed, with the design under test operating under radiation, as well the susceptibility of the tested component to different radiation sources. Discussions upon relevant references concerning radiation test in data converters and mixed-signal devices are also presented along this manuscript.

II. Device and Design Under Test

The architecture tested in all the experimentes herin presented is a fault tolerant data acquisition system (DAS), proposed by our research group in [7]. The system was fully implemented in a commercial Programmable SoC (PSoC 5 from Cypress Semiconductor - now Infineon) manufactured in a 130 nm CMOS technology. Such device has a 32-bit ARM Cortex-M3 processor, several memory resources, digital peripherals, such as communication interfaces and programmable logic devices.

The device also comprises analog peripherals, such as ADCs, DACs, comparators, operational amplifiers, and configurable analog blocks. The general architecture of the PSoC is presented in Fig. 1.

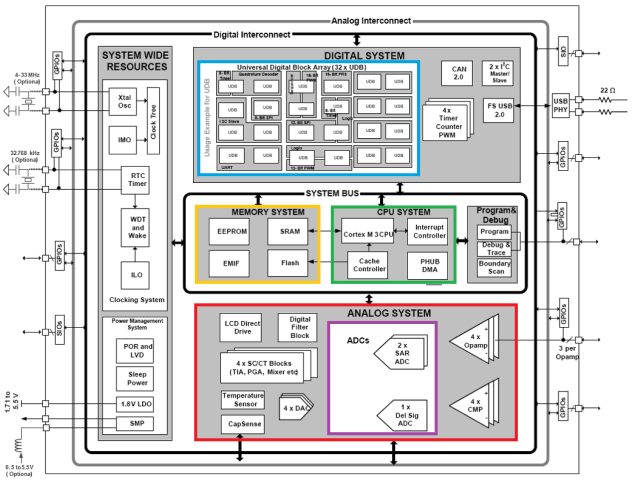


Fig. 1 PSoC block diagram.

The available Analog-to-Digital converters of PSoC 5 are a Sigma-Delta (ΣΔ) AD converter and two Successive Approximation Register (SAR) converters. In this implementation both SAR converters were programmed to operate with different sampling rates and 8-bit wide output. A temporal voter and a synchronizer bock are used to synchronize the system [7]. The block diagram of the redundant DAS, prototyped into the PSoC device, is depicted in Fig. 2. Besides both SAR converters studied in this work the system also comprises a ΣΔ converter, two voters, sample-and-hold blocks, direct memory access (DMA) blocks, a synchronizer and a status register block, which allows monitoring the converters during the experiments. The status register is composed by 5 circular buffers that continuously monitor the output of the 3 converters and both voters. In TID tests, its content is sent to the external computer (by an UART interface) periodically, and, in SEE tests, whenever an error is detected by the voters, as detailed in the experiments description, in next sections.

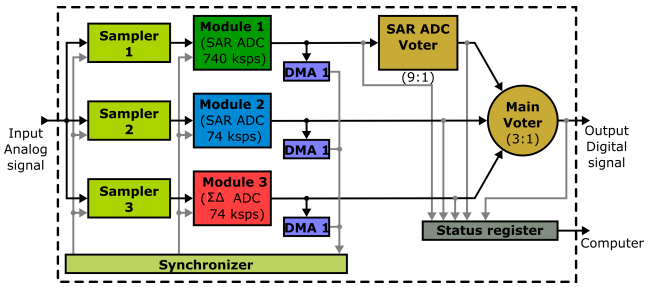


Fig. 2 Block diagram of the DAS programmed into the PSoC device.

The system also comprises two voters: one main voter, which performs the voting between the converted words of the three ADCs and a special voter (called here SAR ADC voter), which performs the voting between the samples generated by the SAR ADC that runs at 740 ksps. Since the sampling frequency of this ADC is ten times higher than the frequency of the other converters, there is an equivalent oversampling. In this way, a "temporal" voter performs the majority voting upon 9 of the 10 generated samples of this converter, adding additional temporal redundancy at the same time that the coarse synchronization is performed.

The fine synchronization is performed by using hardware and software resources. Synchronization is a key issue of the diversity schemes [19], because different copies may present distinct latencies and delays in performing the same task. Therefore, a synchronizer block is needed to guarantee the correct voting. Fig. 2 shows the overall system block diagram of the Device Under Test (DUT).

Majority voting presents a challenge when applied to mixed-signal or approximate TMR systems due to the intrinsic difference of output results of each module. In the digital domain, the implementation of a majority voting can be done by using bit-by-bit voting or word voting, each with proper advantages and drawbacks [19, 20].

The main voter of the tested architecture is based on the concept of word voting [19]. This voter consists of three comparators, which perform mutual subtractions between the signals, generating three error signals. Based on the magnitude of the error signals (considering a tolerance window) a decision element

with multiplexing capability selects the voted signal to be the current system output. The part of the code which implements the main voter is show in Fig. 3. The adopted tolerance window in this case is 4 (decimal), which represents an error of approximately 1.5% of the converter full scale for an 8-bit resolution. One can refer to Fig. 19, in section V.C. to see an schematic representation of the voters.

The SAR ADC temporal voter was implemented using the bit-by-bit voting technique, which is easier to implement in the case of many inputs [19]. The part of the software implementing this voter is depicted in Fig. 4. The voter considers 9 of the 10 samples generated in a voting cycle (one is discarded from voting in order to avoid a tie) and counts the number of ones in each bit position of each word. If there is 5 or more ones in a given position the respective bit of the final voted word is filled with one, otherwise with zero.

```
void main_voter()
{
    error1 = abs (SAR_ADC_voter_data - module2Data[1]);
    error2 = abs (module2Data[1] - module3Data[1]);
    error3 = abs (module3Data[1] - SAR_ADC_voter_data);

        if (error1 <= 4)
            system_output = SAR_ADC_voter_data;
        else if (error2 <= 4)
            system_output = module2Data[1];
        else if (error3 <= 4)
            system_output = module3Data[1];
        else
            system_output = SAR_ADC_voter_data;

        if ((error1 > 4) || (error2 > 4) || (error3 > 4))
            main_voter_error_det = 1;
}
```

Fig. 3 Main voter code.

```
void SAR_ADC_voter_data
{
    bits = 0;
    SAR_ADC_voter_data = 0;
    for (i = 0; i < 8; i++) bit_counter[i] = 0;
    for (i = 0; i < 8; i++)
    {   for (j = 1;j < 10; j++)
        {  bits = (module1Data[j] & mask[i]) != 0;
        // mask is an aray of bytes previosly defined:
        // mask[8] = {128, 64, 32, 16, 8, 4, 2, 1}
            if (bits == 1)
                bit_counter[i] = bit_counter[i] + 1;
        }
    }
    for (i = 0; i < 8; i++)
    {       if (bit_counter[i] > 4)
            SAR_ADC_voter_data = SAR_ADC_voter_data + mask[i];
    }
}
```

Fig. 4 SAR ADC voter code.

The diversity paradigm employed in this system may increase the design complexity and area overhead, compared with traditional redundancy schemes, impacting also in the limits of the operating frequency, due to timing and synchronization issues. By considering triplicated devices, area overhead may be similar to the traditional TMR (> 200%). However, considering the application of the technique to MS programmable devices, the resources that would not be used in the original design can be employed to add an extra degree of reliability with virtually zero area overhead, though, with the expense of the increase in power consumption and system complexity. A detailed analysis of advantages and drawbacks of design diversity applied to MS systems and details about thiss specific case study may be found in [7].

III. Experiment 1: Cobalt-60 Gamma Irradiation

A. Test Setup

The system was exposed to ionizing radiation using a Cobalt-60 gamma radiation source from Atomic Energy of Canadian Limited (model Eldorado 78) with a dose rate of 0.28 rad(Si)/s (1 krad(Si)/h), following the European Space Agency (ESA) Basic Specification 22900s [21]. Fig. 5 shows the experimental setup applied in the experiment. A 120 Hz signal was applied to the converters input, alternating between a sinusoidal and a ramp signal, both oscillating between the full-scale limits of the converters (0 to 2V).

To allow monitoring the system during the experiment, the output of the converters are stored in internal buffers. The buffers content is sent to an external computer every 3 minutes by means of an UART/RS232 interface. The collected data is then used to calculate important parameters, such as Total Harmonic Distortion (THD), Effective Number of Bits (ENOB) and Integral Non-Linearity (INL).

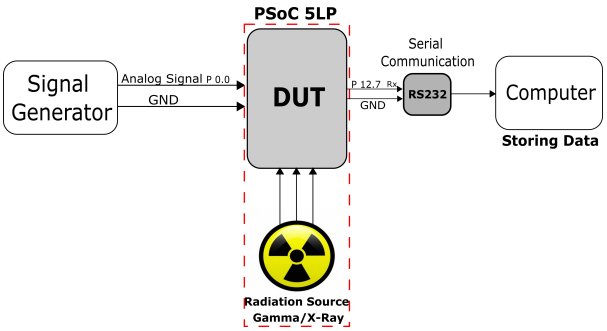


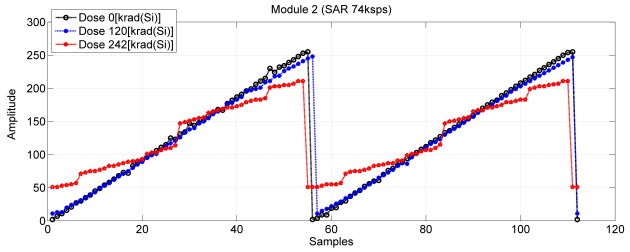
Fig. 5 Experimental setup for gamma irradiation.

B. Test results and considerations

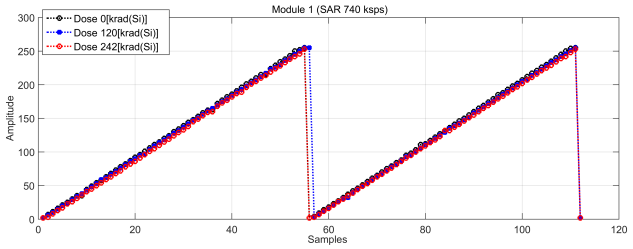
Concerning the behavior of the converters under study, results showed no significant degradation to the SAR ADC operating at 740 *ksps* (from here on referred to as SAR@740). For this converter, the THD at the end of experiment (accumulated dose of 242 krad(Si)) was approximately the same of the pre-rad situation (near 1%).

On the other hand, the THD of SAR@74 (SAR converter operatin at 74 *ksps*) reached near 10% after irradiation. This linearity degradation can be observed by visual inspection in Fig. 6(a), which shows the converted signals for three values of accumulated dose, considering the ramp input stimulus. Conversely, negligible degradations is observed on SAR@740 block for the same dose values (Fig. 6(b)).

The Total Harmonic Distortion (THD) is a good metric to evaluate the correct functionality of data converters, since it measures the high order distortion imposed on a single tone signal [22]. This dynamic parameter is also correlated to static ones as DNL (Differential Non-Linearity) and INL (Integral Non-Linearity) [23]. The



(a)



(b)

Fig. 6: Output of SAR@74 (a) and SAR@740 (b) for different accumulated doses during gamma irradiation.

THD may be calculated both in in decibels (dB) or in percent (%) as follows as:

$$THD_{[\%]} = \left(\frac{\sqrt{{V_2}^2 + {V_3}^2 + ... + {V_N}^2}}{V_1} \right) \times 100\% \quad (1)$$

where, V_1 is the Root Mean Square (RMS) value of the fundamental harmonic of the signal and V_2 to V_N are the RMS value of second to the N^{th} harmonic of interest. The IEEE Standard for Terminology and Test Methods for Analog-to-Digital Converters [22] recommends to use 10 harmonics to characterize THD on ADCs. For this carachterization the test signal must be a single tone sinusoidal signal with the highest possible spectral purity.

In this experiment, the sinusoidal test signals started presenting degradation for doses higher than 100 krad(Si). As can be seen in Fig. 7, the module with higher degradation is the SAR converter operating at 74 *ksps*. The non-monotonic behavior of the THD in respect to the dose is probably related to the rebound (or super recovery) effect [24], which was already observed and explained in details in previous irradiation experiments with programmable analog devices [25, 26].

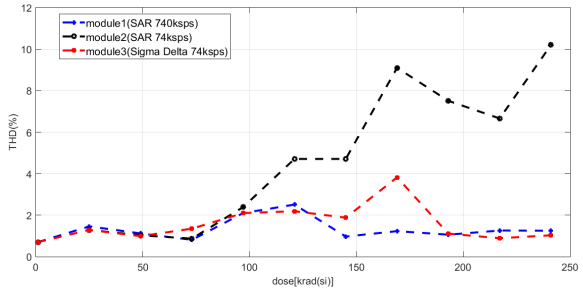


Fig. 7 THD of converter signals at each DTMR module.

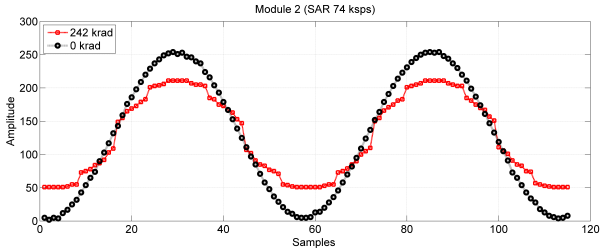


Fig. 8 SAR ADC (74 ksps) degradation.

Fig. 8 shows the degradation observed at the output of module 2 (SAR@74) for the sinusoidal signal, which explains the increase on the THD. This segment-dependent variation on the signal slew rate is explained because the converter is based on a Programmable Capacitor Array (PCA), since it is a charge redistribution SAR. This behavior is associated with the malfunction and failure of the transistors that compose the switches of the PCA, as explained in more detail in [18].

Besides degradation on linearity, it can be observed from Fig. 6 that the radiation caused the SAR@74 to present gain and offset errors. This behavior is due to the appearance of entire ranges of missing codes and changing in the code occurrence probability, as detailed in [13]. Fig. 9 compares the INL (calculated using measured data) of the converter, before and after irradiation.

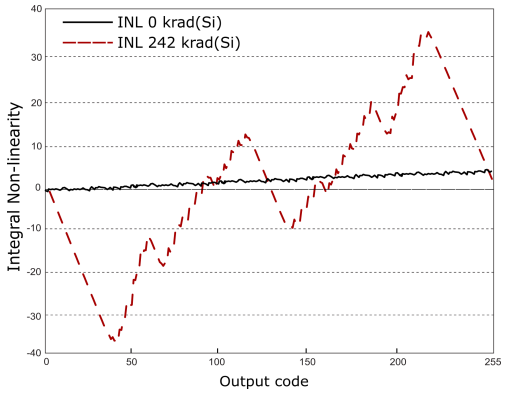


Fig. 9: Comparison of measured pre- and post- irradiation (gamma) INL for SAR@74 ADC.

Similar to the SAR@740, no significant linearity degradation was observed for the ΣΔ converter as can be seen in Fig. 10, that show the converted signals before and after the irradiation (0 and 242 krad(Si)). Considering this converter, the different radiation performance may be attributed to the distinct working principle (comparing to SAR ADCs). The influence of sampling frequency on the performance of both SAR ADCs is detailed in [18], in which the observed effect was reproduced by electrical simulations and the main failure mechanism was elucidated.

C. *Effectiveness of Voting Scheme*

One of the main concerns in fault tolerant redundant system is the voter reliability. In the considered system, the voting is performed by software (implement-

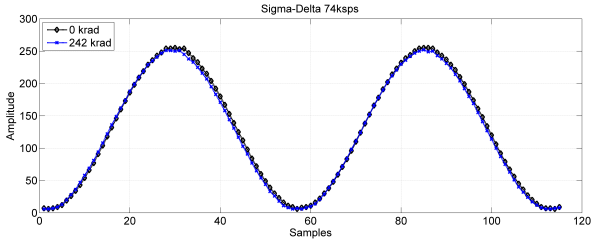


Fig. 10 Sigma-Delta converter pre- and post-rad signals.

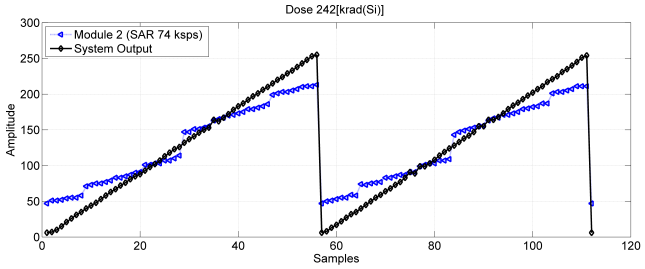


Fig. 11: Module 2 (74 ksps SAR) and system output at 242 krad(Si) accumulated dose.

ing also domain level diversity [7]), though running in the system processor. The voter was able to select the signal of a correct DTMR domain during the whole irradiation. In Fig. 11 it is observed that the voter is able to select a healthy signal, despite the linearity failure of module 2 at the highest accumulated dose.

The radiation impacts in dynamic parameters of the converters, such as the Signal to Noise and Distortion Ratio (SNDR) and Effective Number of Bits (ENOB) were also evaluated with the sinewave test signals. The SNDR (also known as SINAD) is the ratio between the RMS value of the signal (fundamental frequency) and the root-sum-square of the harmonic components plus noise (excluding DC) [23]. With harmonic distortion taken into account, the effective number of bits may be calculated as:

$$ENOB = \frac{SNDR - 1.76}{6.02} \quad (2)$$

Fig. 12 shows the evolution of the SNDR and ENOB for some selected values of dose during the irradiation for the most degraded converter (SAR@74ksps) and the voter output (which follows the SAR@740ksps up to 100 krad(Si) and then switch to the Sigma-Delta ADC). The initial measured ENOB of the converters is between 5 and 5.5 since a not negligible third harmonic component and some noise are already present even before the irradiation. It is possible to see in the figure that both SNDR and ENOB of the system, after voting, are kept near the values of the pre-rad ones (despite a slightly decrease), even at the higher values of dose achieved in this experiment. Additionally, no missing codes were observed at the voted system output during the irradiation.

IV. Experiment 2: X-Ray Irradiation

In order to confirm the sampling frequency dependency of the converters degradation due to TID, a

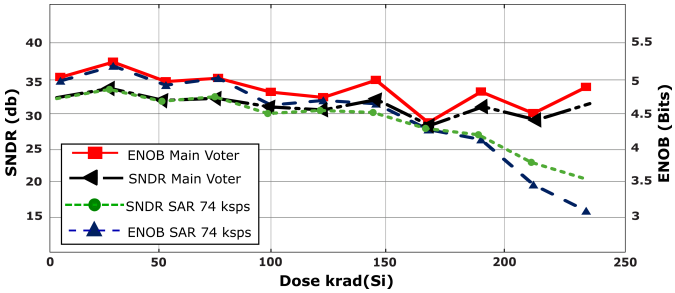


Fig. 12: SNDR (left axis) and ENOB (right axis) evolution during irradiation for ADC module 2 and overall voted output.

second radiation experiment was performed using an XRD-6100 (Shimadzu) X-ray diffraction setup.

X-ray sources are very versatile for studying radiation effects in electronic devices since it is possible to modify the X-ray tube current, bias and the source-device distance, in order to choose an adequate dose rate. The radiation dose was determined using an ionization chamber considering the exposure measure and transformed into an absorbed dose in silicon [27]. The effective energy was measured using aluminum foils of different thickness and calculating the half-attenuation Al layer [28, 29].

A. Test Setup

A voltage of 20 kV was applied on a cooper X-ray source, generating a 10-keV effective energy X-ray beam. A current of 10 mA was applied on the X-ray tube terminals with a distance of 7 cm from the DUT. In this condition, the radiation dose rate was 30.3 rad(Si)/s (109 krad(Si)/h). For this experiment (different from the gamma irradiation) the DUT board was prepared by removing the top package of the PSoC 5 IC. The applied test signals were the same used in the Cobalt test, with the same setup depicted in Fig. 5. The monitoring signals, in this experiment, were sent every 2 minutes to the external computer.

B. Results

In this X-ray test, the experiment was ended when the PSoC system failed completely, with an accumulated dose of 30.6 krad(Si). Details on the adopted X-ray dosimetry methodology can be found in reference [30].

An important factor to be considered in the performed TID experiments (gamma and X-ray) is the different dose rates applied. High dose rates may lead to saturation of short half-life charge traps, because, at high dose rates, the charge trapping rate is much higher than the trap decay rate. At low dose rates, the escaping of charges from these traps is faster than the velocity of charge trapping. Therefore, in low dose rate irradiations, it can be expected the buildup of trapped charges being dominated by long-life traps. Thus, different charge buildup, and the consequent electrical degradation, may be observed for different dose rates. This process is also known as self-annealing. It is worth mentioning that lower dose rates are suitable to better reproduce the radiation of the space environment.

Table I.: Accumulated dose and experiment time until the failure of the tested converters and PSoC system.

Module	Time in minutes	Accumulated dose (krad/Si)
SAR 74 ksps	10.0	18.1
SAR 740 ksps	12.0	21.8
Sigma - Delta	14.3	25.8
PSoC device	17.0	30.6

The fabrication process variability may also contribute, in some degree, to the failure behavior in both experiments, since the devices used in each experiment are not from the same fabrication batch. However, given to the high observed difference on the failure doses, and considering our previous experience in similar experiments, it is possible to affirm that variability is not the dominant effect in this case.

It is worth noticing that a second gamma experiment was performed with the studied device, in which a 13% variation in the failure dose was observed, compared with the first experiment (with the same trend observed for individual converters failure). Additionally, we have also observed, in past experiments of our group, and in literature data, variations in dose of failure that may be greater than this, tough within the same order of magnitude. The observed variation (between gamma and X-ray experiment) was near one order of magnitude (10×), indicating that another effect may be dominating this difference on results.

Uncertainties in X-ray dosimetry could also be a source of discrepancy. However, as already mentioned, a careful calibration setup was carried out, eliminating the possibility of this issue to be one of the main contributors. Future works are being considered in order to investigate the observed dose rate effects in this specific DUT.

With this in mind, one can conclude that the difference in dose rates is the main cause of the distinct values of total dose reached before failure in both experiments. Nevertheless, the trend related to the sampling frequency is the same.

Table I shows the time of experiment and correspondent accumulated doses in which the converters and the whole system have failed. The failure of the converters, in this experiment, was considered when the signals harmonic distortion presented values higher than 20%. The whole system failure was characterized when all the communication and status signals where lost. It can be observed in Table I that the SAR converter operating with lower sampling frequency failed with a lower accumulated dose than the faster SAR, confirming the dependency on the sampling frequency observed in the previous gamma irradiation. The ΣΔ converter showed to be more robust to TID.

Figure 13 shows the waveform of the sawtooth signal at the converters output, for different accumulated doses, evidencing the sequence of converters failure shown in Table I. The degradation starts to become visible for the slower SAR at an accumulated dose of 14.5 krad(Si) (Fig 13(a)) whose failure was registered at 18.1 krad(Si) (Fig 13(b)), while the faster SAR failed at 21.8 krad(Si) (Fig 13(c)). The ΣΔ converter was able to tolerate a 25.9 krad(Si) dose.

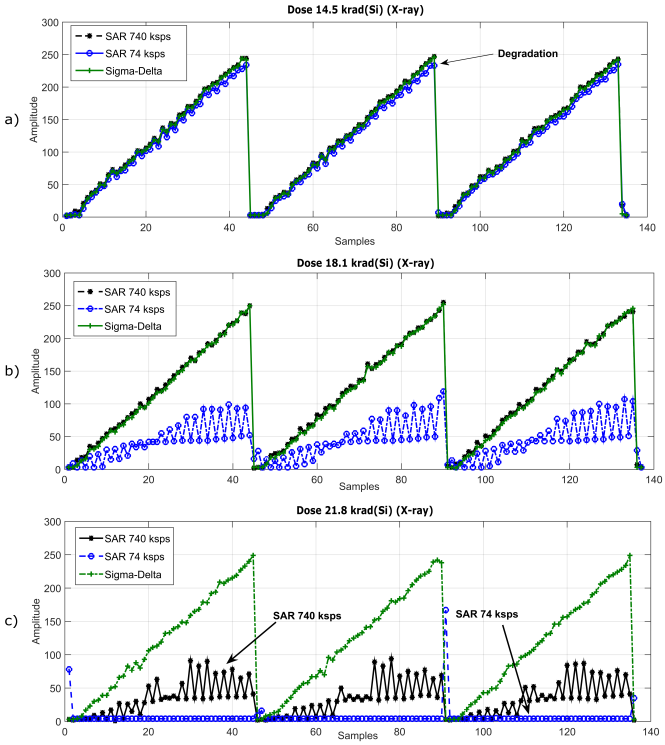


Fig. 13: Output of the tested converters, with the ramp signal as input, for different doses, during X-ray irradiation.

Due to the very high dose rate employed in this experiment and given the interval time in which the logs with the signal status were sent to the computer (2 minutes), failures were observed already in an advanced degradation state. For this reason, in this experiment it was not possible to verify the intermediate linearity degradation as in the gamma irradiation experiment. On the other hand, it was possible to witness the failure of all ADC modules and the complete system failure, differently from the previous experiment.

V. Experiment 3: Heavy Ion Irradiations

A. Test setup

Two heavy ion irradition campains were performed on the fault tolerant DAS at the *Laboratório Aberto de Física Nuclear* at the *Universidade de São Paulo* (LAFN-USP), Brazil [31], with ion beams produced and accelerated by the São Paulo 8UD Pelletron Accelerator, generating a ^{16}O ion beam with 22 μm penetration into the silicon. The heavy-ion beam was accelerated up to 36 MeV and reduced its intensity to hundred particles/s/cm² (as recommended by the European Space Agency (ESA) for SEU tests [32]) using magnetic defocusing techniques and two thin gold foils (near 1 mg/cm²) in the SAFIIRA system [33]. This new system was built to study heavy-ion beam effects in electronic components. SAFIIRA is a Portuguese acronyms for Ion-beam Application and Irradiation System.

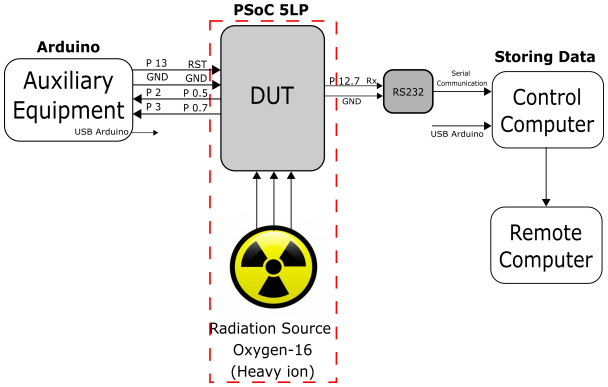


Fig. 14 Experimental setup block diagram for heavy ion tests.

The DUT (with top package removed) was irradiated at 0^o angle, producing an effective LET at the active region of 5.5 $MeV/mg/cm^2$. The average flux of each experiment was 350 and 430 $particles/s/cm^2$, during 246 and 288 min resulting in fluences of 5.08 $\times$ 10^6 $particles/cm^2$ and 7.32 $\times$ 10^6 $particles/cm^2$, respectively.

The overall experiment setup is described in Fig. 14. The auxiliary equipment acts as a watchdog, monitoring the DUT activity and resetting it if a hang is identified. The Control and remote computer are used for controlling and data storage.

B. *Results of Heavy Ion Experiments*

Two well known system level effects of single events in computing systems are Single Event Functional Interrupt (SEFI) and Silent Data Corruption (SDC). When considering mixed-signal systems in which the analog function may be assisted by digital circuits and configured by means of control registers, a deviation on a given register value may affect the "analog" behavior of the system. For this reason, a new system level error classification is needed. We then propose to use the term "Single Event Functional Deviation" (SEFD), to classify the conditions in which a "semipermanent" or lingering error [34, 35, 36] is caused by a single event, in such a way that the system is still operating similarly to the nominal case, but with a deviated output.

While examples of SDCs in the converters are given in Fig. 15 and SEFI examples are shown in Fig. 16, SEFD examples may be observed in Fig. 17. The SDCs may be related to an error in a data register of the converter or in the memory position in which the current sample is stored (before the voting is completed), while SEFI and SEFD in the converters may be associated to control registers and auxiliary control circuits used to assist the analog part of the converters.

All errors shown in the figures were recorded during the heavy ion irradiation. The reason for the error to appear always in the sample number 51 in the figures is due to the adopted continuous buffering strategy, which is able to store 50 samples before and 50 after the error occurrence.

The data acquisition system under study is prototyped in a microprocessor-based programmable SoC with the voting and processing performed by software.

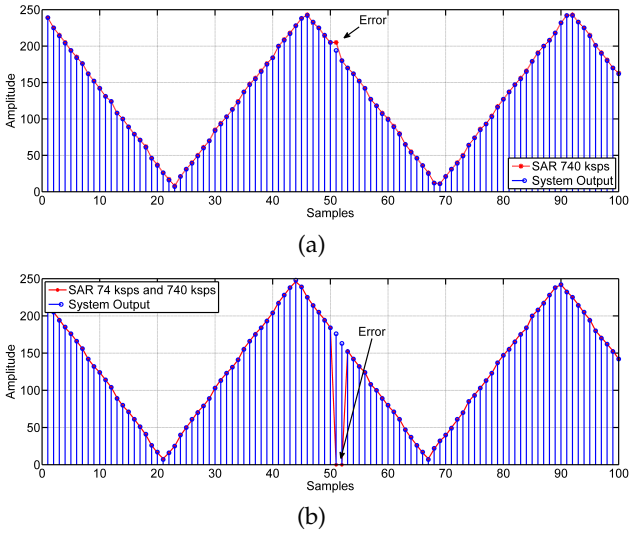


Fig. 15: Examples of SDCs in the SAR @740 ksps module: small (a) and high (b) magnitude errors.

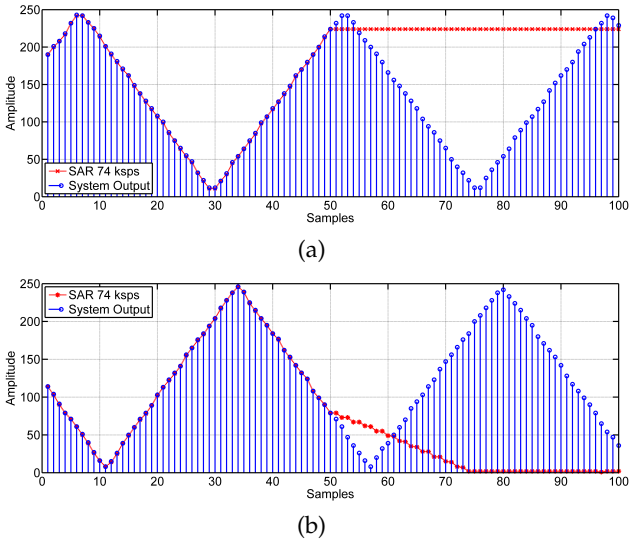


Fig. 16: Examples of SEFIs in the SAR @74 ksps module: stuck at current sample (a) and decay to zero (b).

This way, the fault-free condition of the overall system depends also on the processor correct functioning. Besides the above described errors in the converters, system level SEFIs, from here on called *hangs*, were also observed.

Considering both heavy ion experiments, 353 errors were observed. From these errors, 211 are system hangs and 98 are SDC, SEFI or SEFD at the converters. Most of the hangs were detected by the external watchdog and the system was automatically reset. There were 44 errors that were detected and treated manually. For this reason we classified these errors as critical hangs. We can explain this behavior because, in this experiment, the alive signal sent by the DUT is generated by a clock generator from the hardware peripherals of the PSoC device that may still be functional even if the program is not running normally. If we consider an interaction of the main program with the watchdog

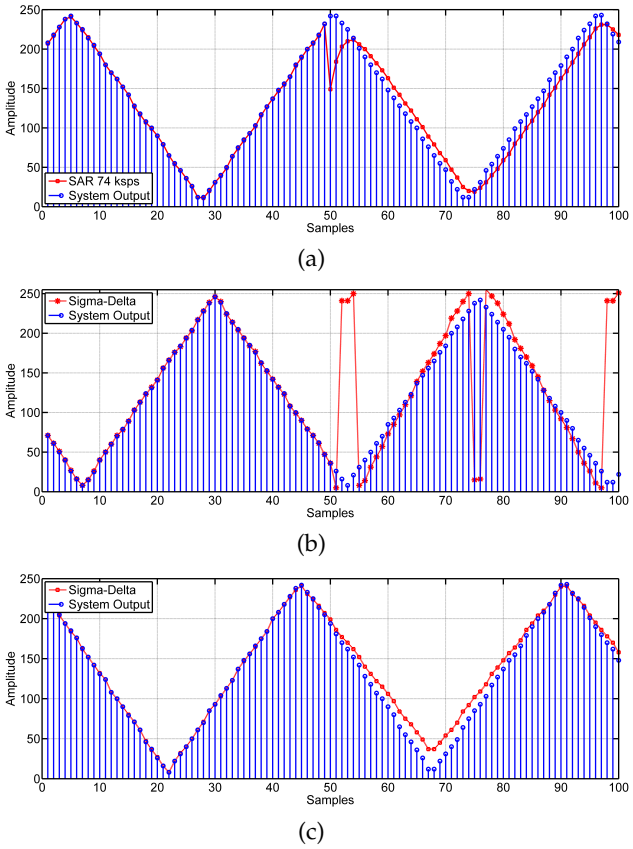


Fig. 17: Examples of SEFDs in the SAR @74 ksps (a) and Sigma-Delta ((b) and (c)) modules.

timer, it is expected that these critical hangs can be also treated accordingly. Some of these critical errors were identified in the communication interface (experiment monitoring), with no data sent trough the UART, despite the system was normally ruining.

With the experiment time, ion flux, and the recorded errors, we are able to calculate the dynamic cross section of the system, as well as the individual cross section of each converter lane. Table II summarizes the calculated cross-section for each case, which can be also individually calculated for the different error nature (hangs and SDC/SEFI/SEFD). To calculate the cross sections, the uncertainties were calculated considering a Poisson distribution for the error occurrence.

Table III summarizes the number and percent of errors according to the affected system part, along with the uncertainties (where (353 ± 19) means an uncertainty of 19 in a total of 353 errors, for instance). The unknown errors are errors that triggered the data sending from the DUT to the computer, but were not identified in the post-experiment analysis (no observed signal deviation). These errors may be related to malfunction of the serial communication interface and bit inversions in the error flag of the voters. Actually some other communication errors were identified, with garbage data sent through the serial channel. These errors were not computed to generate the cross section data presented in this paper.

Errors were also observed in the SAR ADC temporal voter (as depicted in Fig. 18), even when no error occurred at the 9 voted samples originated by the SAR@740 module. On the other hand, no error was observed in the main voter, which means that 100% of the observed SDC/SEFI/SEFD occurring in the converters were tolerated by the proposed system, as one can see in Figs. 15 to 17.

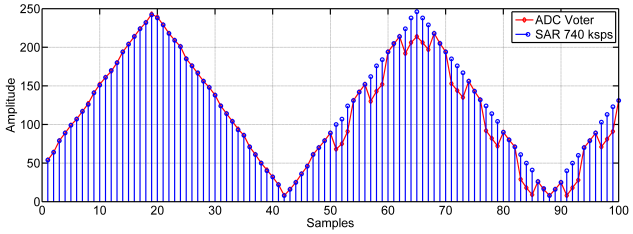


Fig. 18 SEFD in the temporal voter.

Table II.: Dynamic cross section of the whole system and individual converters.

System Cross Section (cm^2)	
Total	$(4.98 \pm 0.26) \times 1 \times 10^{-5}$
SDC/SEFI/SEFD (ADCs)	$(1.38 \pm 0.13) \times 1 \times 10^{-5}$
System hangs (processor)	$(2.97 \pm 0.20) \times 1 \times 10^{-5}$
Converters Cross Section (cm^2)	
SAR @740 ksps	$(3.95 \pm 0.74) \times 1 \times 10^{-6}$
SAR @74 ksps	$(1.83 \pm 0.50) \times 1 \times 10^{-6}$
$\Sigma\Delta$	$(3.38 \pm 0.69) \times 1 \times 10^{-6}$

Table III. Summary of error occurrence results at the DAS.

Total Events	(353 ± 19)	**100%**
Hangs	(211 ± 15)	60%
Critical Errors	(44 ± 7)	12%
SDC/SEFI/SEFD (converters)	(98 ± 10)	28%
SAR @740 ksps	(28 ± 5)	8%
SAR @74 ksps	(13 ± 4)	4%
$\Sigma\Delta$ Converter	(24 ± 5)	7%
Temporal Voter	(22 ± 5)	6%
Main voter	0	0%
Unknown errors	(11 ± 3)	3%

C. *Voter Reliability Analysis*

The second heavy ion irradiation campaign was idealized in order to allow an investigation on the voters reliability, since the first experiment showed that the both tested voter present very distinct relaibility levels.

In this second experiment a new temporal voter architecture to the SAR@740 was implemented. This way,in both experiments, 3 distinct software-based voter architectures were tested. Figure 19 shows the schematic representation of the tested voters. Fig. 19(a) depicts the main spatial voter, based in mutual subtraction and comparison, whose software code was already presented in Fig. 3. The first version of the SAR ADC Temporal voter (software code depicted in Fig. 4) is illustrated in Fig. 19(b). This bit-by-bit voter consists on a counter and a decision element for each bit position,

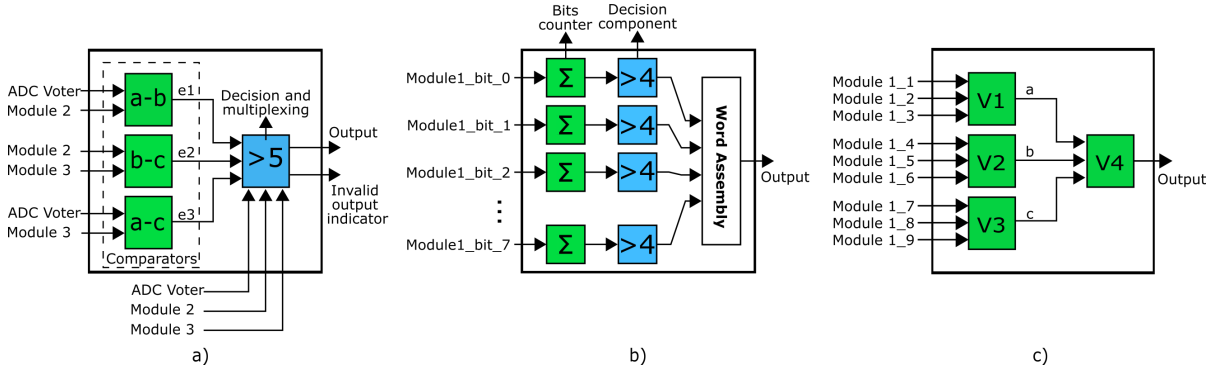


Fig. 19: Architecture of the studied voters: (a) main word voter; (b) bit-by-bit temporal voter (first version) and (c) second version of temporal voter with a cascade of word voters identical to (a).

Table IV. Experiment details and results for each tested voter.

	Bit-by-Bit voter	**Cascade of word voters**	**Main voter**
Errors	(18 ± 4)	(4 ± 2)	Zero
Voting time	95μ sec.	11.75μ sec.	3.75μ sec.
Cross Section ($\times 10^6 cm^2$)	(5.3 ± 1.2)	(1.09 ± 0.54)	——-
Fluence (part./cm^2)	5.08×10^6	7.32×10^6	12.40×10^6
Irrad. time	246 *min*	288 *min*	534 *min*

as well as a single word assembler. For each bit position the number of ones among all words is counted, and this information is taken to the decision element, that votes upon each bit position. The word assembler generates the output word, based on the voting results.

The second version of the SAR temporal voter was built with a cascade of word voters (V1 to V4), identical to the main voter, as depicted in Fig. 19(c).

In this specific analysis the errors originated in the voters are computed and compared, considering the different voter architectures. While the main word voter showed no error in both experiments (even experiencing the higher total fluence), 4 errors were recorded at the temporal voter built with 4 word voters (Fig. 19(c)), while 18 errors were observed in the bit-by-bit version (Fig. 19(b)), as shown in Table IV. The uncertainties were calculated considering a Poisson distribution of the observed errors. This table also shows the calculated dynamic cross section for each voter (number of errors divided by fluence), the fluence (integral of flux over time), the experiment time, and the time each voter takes to perform the voting task.

Finaly, it is important to mention that no errors were observed in multiple modules of the DTMR or both voters at the same time. Therefore, as no error occurred at the main system voter, 100% of the observed errors, including those occurring in the temporal voter, were tolerated by the proposed system.

VI. Conclusions

In this work results of three distinct radiation tests performed upon a fault tolerant data acquisition system comprising a design diversity redundancy technique were presented. The system is composed of three analog-to-digital converters, with different architectures and sampling rates, along with a synchronizing and voting scheme, implementing hardware and temporal diversity redundancy. The MS-DTMR case study design was prototyped in a commercial programmable system on-chip (PSoC). Results of two TID tests (Cobalt-60 gamma and X-Ray) were discussed and compared.

In the Cobalt-60 Irradiation, considering the final accumulated dose to which the system was exposed (242 krad(Si)) only one of the three diversity modules presented a significant degradation, which points to the advantage of using diversity in redundant schemes. This increased tolerance of the other two modules would be responsible for increase the system lifetime, if considering a real scenario of a mission, in which this design would be exposed to ionizing radiation, reaching the doses tested in this experiment. Though diversity may increase the design complexity and area overhead, if compared to traditional redundancy schemes, implementing it using programmable mixed-signal devices may be a feasible alternative.

Even concluding in this TID experiment that operating the SAR converter with a higher sampling frequency, or using the Sigma-Delta ADC, would be the best choice to implement the DAS (if considering using a single converter or traditional redundancy), this conclusion was achieved after an expensive radiation test. Going further, the designers and system integrators usually do not have the information regarding the reliability level of all implementation possibilities against all reliability threats (to make an optimal decision, selecting the most reliable architectures and schemes). Thus, diversity redundancy may be a good choice to enhance reliability of redundant schemes whenever it is allowed.

Considering the voters, the implemented schemes were able to select the copies with less degradation to provide the system overall output, contributing to have a functional system even for the higher dose values tested in this experiment.

Another experiment, with a high dose rate X-ray source, also showed that the linearity degradation starts to occur for a lower dose value in the slower SAR converter. In addition, the lifetime under X-ray radi-

ation of the slower converter was lower, if compared with the converter operating at higher sampling rate, confirming the trend observed in the first TID experiment.

Two havy ion irradiation campaings were also performed. Considering the converters operating at the same sampling frequency, the ΣΔ showed a cross section higher than the charge redistribution SAR, given to its increased complexity. When comparing the same architecture (SAR), the dynamic cross section of the copy which operates at higher sampling frequency is also higher, as expected, but still lower than the cross section observed for the ΣΔ converter, with lower sampling rate.

The application of DTMR technique to the analog-to-digital interface of the PSoC device showed effective to tolerate 100% of the errors originated in the converters. However, the temporal voter at the output of the faster SAR converter showed to be very sensitive to single events, specially if compared with the main voter. Despite this fact, in all occurrences the main voter was able to correct the error originated by the SAR voter.

To investigate the voters reliability, a second heavy ions irradiation campaign was performed considering a new architecture for the temporal voter. These results showed that different software-based voting schemes present distinct reliability, with voting time and algorithm complexity being responsible for this behavior. The voting time depends on the number of inputs and algorithm complexity and impacts the voter reliability. The higher is this time, the higher is the probability of this task being affected by an ion impact for a given fluence. The software-based word voter tested in the heavy ion campaigns showed to be more reliable than the bit-by-bit voter counterpart, with a significant difference in the obtained cross-sections.

Finally, the overall system is also prone to hangs due to errors in the processor. These errors may be mitigated with existing watchdog methods, besides other techniques usually employed to cope with soft errors in control path elements of processors, when applicable.

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