Memristors: A Journey from Material Engineering to Beyond Von-Neumann Computing

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Abstract—Memristors are a promising building block to the next generation of computing systems. Since 2008, when the physical implementation of a memristor was first postulated, the scientific community has shown a growing interest in this emerging technology. Thus, many other memristive devices have been studied, exploring a large variety of materials and properties. Furthermore, in order to support the design of practical applications, models in different abstract levels have been developed. In fact, a substantial effort has been devoted to the development of memristive based applications, which includes high-density nonvolatile memories, digital and analog circuits, as well as bio-inspired computing. In this context, this paper presents a survey, in hopes of summarizing the highlights of the literature in the last decade.

Index Terms—memristors, devices, models, applications.

I. Introduction

In 1971, Leon Chua postulated the existence of the fourth fundamental electrical circuit element [1]. This element establishes a relationship between the electric charge and the magnetic flux. It demonstrates the hysteresis property of a memory and the dissipative characteristics of a resistor. For this reason, this hypothetical nonlinear device was named memristor (memory + resistor). A few years later, this concept has been generalized to a broader class of nonlinear, dynamical systems called memristive devices [2]. In 2008, a research group at HP announced the fabrication of a nanoscale device, which they claimed to be the first practical implementation of the memristor predicted by Chua [3].

Since then, extensive literature related to memristors have been produced. Other devices, which also have the memristive behavior, have been developed [4-6]. They explore different materials and different physical properties. Although there is some disagreement in the literature regarding the nomenclature of these devices [7, 8], in this paper, as a matter of simplicity, the terms "memristor" and "memristive device" are used interchangeably.

Furthermore, memristors may be explored in several areas of integrated circuit design and computing. In terms of applications, the non-volatile memories are the most intuitive due to the small physical area consumed and the nonvolatile characteristic [9]. Recently, its scalability potential was demonstrated through a crossbar array with 2 nm feature size and a single layer density up to 4.5 terabits per square inch [10]. In addition, memristors have also been used to perform analog and digital logic [11, 12]. Finally, new possibilities, as bioinspired systems [13, 14], are one of the most promising aspects to the future of semiconductor industry.

In this context, in order to explore practical applications and validate them, computational models are needed. Hence, there is a large effort to provide these solutions in several abstract levels [15-17].

This paper presents a constructive discussion in three important aspects: device engineering, memristor models, and main applications. Each of these topics is presented in a specific section. Materials and devices are introduced in Section II. Section III discusses the models proposed in the literature. The applications are presented in Section IV, while Section V contains the final considerations.

II. Materials and Devices

After the announcement of the manufacture of the TiO_2 memristive device by HP Labs in [3], the research interest in this promising area was intensified, including the search for novel chemical compounds with memristive behavior.

Since then, several materials with these properties have been studied, such as binary transition metal oxides, perovskites, chalcogenides, polymers, carbon nanotubes, manganites, graphene and organic materials. Different resistance switching phenomena have also been observed in emerging devices developed from these materials. In this context, memristors have been classified into different technologies, which differ in the switching mechanisms, switching time, resistance variation range, energy consumption, retention time, endurance, among others. A broad review of the literature on the different resistance switching mechanisms, their peculiar properties and potential applications was presented by Wang et al. [18]. Next, we will briefly address each of these technologies.

A. Filament-Type Devices

These devices consist of an insulating layer sandwiched between two metal electrodes, in a structure also known as MIM (Metal – Insulator - Metal), as shown Fig. 1. The resistance switching mechanism in these devices is based on the formation and rupture of a conductive filament (CF) within the insulating layer. The existence of filaments connecting the electrodes leads the device to a low resistance state (LRS), while the absence or rupture of these conductive paths characterizes a high resistance state (HRS). The transition from HRS to LRS is often called SET operation whereas the transition from LRS to HRS is called RESET operation. In general, these resistance changes can occur either abruptly or gradually [19]. In addition, resistive switching can be classified as a bipolar or unipolar (also called nonpolar). In

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bipolar switching, SET and RESET operations occur with voltages of different polarities, while in unipolar switching these operations are triggered by voltages of the same polarity, but with different magnitudes [20]. However, before switching can be achieved, the insulating layer must go through a soft breakdown, where initially conductive channels are created. This is also known as forming process and can be performed through electrical operations [21] or fabrication processes [22].

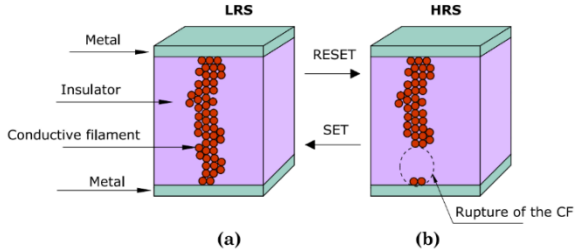


Fig. 1. Filament-type memristor in (a) LRS and (b) HRS.

According to the insulator and electrodes materials, filament-type memristors are categorized as valence change memories (VCM) and electrochemical metallization memories (ECM). In VCM devices, electric field and thermal effects resulting from the application of an appropriate voltage will cause movement of the anions. This migration of anions will result in the formation and rupture of the conductive filament. The insulating material in VCM devices includes a wide range of binary metal oxides such as TiO_x [23], HfO_x [4] and AgO_x [24], perovskites, such as $SrTiO_3$ [25] and $BiFeO_3$ [26], some complex metal oxides, e.g. InGaZnO, some non-metal oxides such as SiO_x [27] and GO [28] , metal nitrides such as ZrN [29], among others.

In ECM devices, the switching mechanism is very similar to that observed in VCM. A fingerprint of ECM memristors is that an electrochemically active (EA) material, such as Cu and Ag [18], constitutes one electrode and the other electrode is usually made from an inert material, such as Pt and Au. Thus, the conductive filament usually forms via the movement of dissolved metal cations from the EA electrode towards to the inert electrode. In bipolar devices, a polarity reversal will cause the dissolution of the filament.

The insulator material in ECM includes oxides such as AlO_x [30] and ZnO [31], chalcogenides such as GeS_x [32], halides such as AlN [33] and organics such as [34].

B. Interface-type Devices

The interface-type (or barrier-type) memristor is usually built in a capacitor-like structure, which is often composed by insulating and/or semiconducting oxides sandwiched between metal electrodes. Usually, an ohmic contact is formed at one interface between metal and oxide, and a Schottky barrier is formed at the other interface. In this group of memristive devices, modulating the height or width of the Schottky barrier causes resistance changes in the device. As the barrier can be shifted gradually between a maximum and minimum position, an analog resistance switching can be achieved according to an applied voltage or current. This important feature makes this type of device an interesting alternative for applications such as neuromorphic computing and multilevel storage.

One of the possible mechanisms for adjusting the barrier is related to the electrochemical migration of oxygen vacancies [35]. To illustrate this phenomenon, Fig. 2 shows the behavior of a device made up of a n-type oxide in two distinct moments. In Fig. 2a, a negative voltage is applied to the top electrode, forcing vacancies to drift towards that terminal.

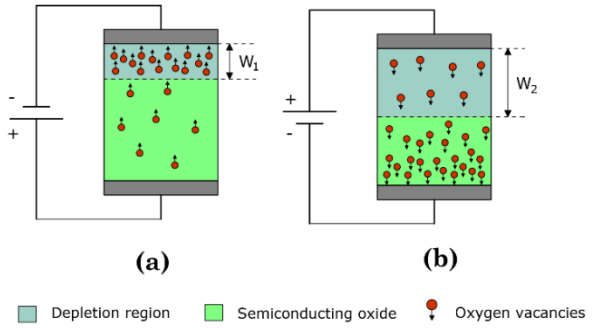


Fig. 2. Redistribution of oxygen vacancies according to the voltage polarity in n-type material. (a) A negative voltage applied to the top electrode narrows the depletion region to a width W_1 and reduces the resistance. (b) A positive voltage causes the opposite effect, widening the depletion region to a width W_2 and increasing the resistance.

The accumulation of ions at the interface will increase the density of donors, narrowing the depletion region and, consequently, causing a decrease in resistance. If the polarity is reversed (Fig. 2b), vacancies will move away from the top electrode, which causes the widening of the depletion region and the increasing of the resistance.

Regarding the materials used in the middle layer, there are implementations based on numerous compounds that include binary oxides such as TiO_x [36], some complex perovskite oxides such as $Pr_{0.7}Ca_{0.3}MnO_3$ (PCMO) and $CaMnO_3$ [37] selenides such as CdSe [38] and others.

C. Phase-Change Devices

This technology explores the properties of chalcogenide phase-change materials, such as $Ge_2Sb_2Te_5$ (GST) or GeTe [39], which are able to switch between the amorphous and crystalline solid phases [6]. Typically, a PCM device is built as the structure shown in Fig. 3.

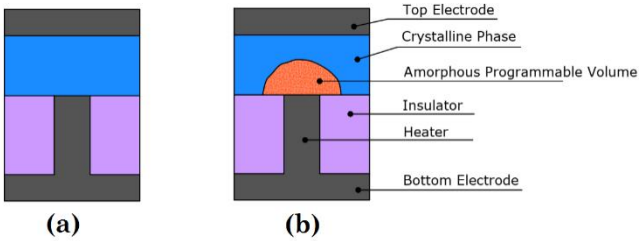


Fig. 3. Schematic of a PCM device in (a) low resistance state, characterized by the fully crystalline active layer and (b) high resistance state, with an amorphous volume blocking the heater pillar.

In Fig. 3a, the phase change material on the active layer is entirely crystalline (low resistance). For a binary operating mode, the switching between the crystalline and amorphous phases is performed with single pulses. For this case, if a relatively high amplitude and short duration current pulse is applied to the device, Joule heating causes a portion of material to melt in the active layer. The short pulse duration causes fast cooling of the molten material, leading it to the amorphous phase (high resistance) [6]. The pillar-like heater

results in a mushroom shape of the molten volume shown in Fig. 3b. This area needs to completely cover the heater interface so that the current path is fully blocked and the reset is achieved. A lower amplitude and longer duration current pulse is applied to switch it back to the crystalline, low resistive state. Alternatively, the pulses applied to these devices can be tuned in amplitude and/or duration so that the amorphous region can be progressively crystallized from a predetermined number of pulses, taking advantage of the characteristic accumulation property of this technology.

D. Spintronic Devices

Magnetic Tunnel Junction (MTJ) is a promising spintronic memristive device, whose electrical resistance is dependent on their state of magnetization. This component is composed of a thin insulating layer disposed between two ferromagnetic (FM) layers. Fig. 4a shows the schematic of the MTJ presented by [5], where the insulating layer is constituted by MgO and the ferromagnetic layers are formed by CoFeB.

These devices are built using a pinned ferromagnetic layer, whose magnetization cannot be easily reversed and a free layer whose magnetization can be reversed by an external input. The operation of this device is based on the Tunnel Magnetoresistance effect (TMR), so that its resistance depends on the relative orientation of the magnetization in the two ferromagnetic layers [40]. If the magnetization directions of the two layers are parallel, the resistance of the MTJ will be minimal (R_P). On the other hand, if they are antiparallel, the MTJ resistance will be maximum (R_{AP}). The relative change of resistance, also called magnetoresistance ratio, typically ranges between 250 - 600% at room temperature, depending on the manufacturing technology [18]. The resistance switching in MTJs can be performed through mechanisms such as spin-transfer torque (STT), voltage-controlled magnetic anisotropy (VCMA) and spin-orbit torque (SOT). Among these, the most technically mature is the STT. In this mechanism, the resistance variation is triggered when an electric current I with a magnitude higher than a critical current (I_{C0}) flows through the MTJ. In Fig. 4b, the orientation of the electronic spins of the ferromagnetic layers are parallel, which keeps the MTJ in a state of low electrical resistance. To change the resistance, an electric current directed downwards is applied to the device, changing the orientation of the free layer electronic spins. Thus, the magnetization directions of the ferromagnetic layers become antiparallel, leading the MTJ to a state of high resistance. To reverse this situation and return the device to the low resistance state, a current with the opposite direction of the one previously applied must run through the memristive element, as can be seen in Fig. 4c.

Among the important advances in this technology, are reports of devices with switching times ~ 200ps [41], minimum switching energy < 10fJ [42] and high endurance above 10^{14} cycles [43].

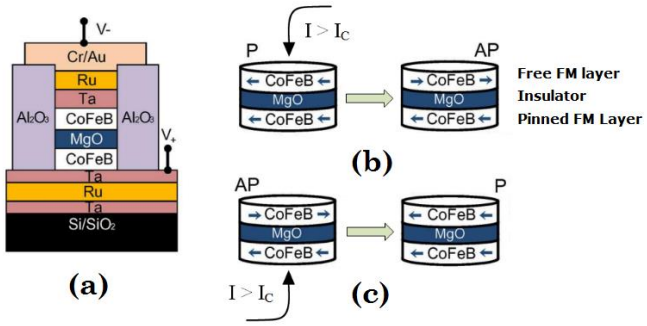


Fig. 4 (a) Schematic of the MTJ presented by Ikeda et al. in [5]. (b) Switching from R_P to R_{AP}. (c) Switching from R_{AP} to R_P.

E. Ferroelectric Devices

In the last years, memristive properties have been intensively investigated in ferroelectric materials. In this research field, there are several efforts focused on the study and the enhancement of a device called Ferroelectric Tunnel Junction (FTJ). This device consists of an ultra-thin ferroelectric barrier disposed between two electrodes.

In these devices, electric-field-induced polarization reversal in the ferroelectric material can modulate height and/or width of the barrier, causing non-volatile resistance switching of the device between high and low resistance states. This resistance variation in the ferroelectric barrier is a phenomenon known as Tunneling Electroresistance (TER) effect [44]. Fig. 5 illustrates the simplified schematic of a FTJ built on a conventional Metal/Ferroelectric/Metal structure, where the direction of polarization in the ferroelectric layer determines a HRS or a LRS in the device.

In the literature, there is a wide variety of structures and materials used in the manufacturing of FTJs, such as $Cr/BaTiO_3/Pt$ [45], $Pt/Co/BiFeO_3/Ca_{0.96}Ce_{0.04}MnO_3$ [46] and $Cu/Pb(Zr_{0.2}Ti_{0.8})O_3/La_{0.7}Sr_{0.3}MnO_3$ [47]. In recent years, Metal/Ferroelectric/Semiconductor (MFS) FTJs have attracted more attention due to reports of promising results achieved in experiments conducted with these devices. For instance, a $Ag/BaTiO_3/Nb:SrTiO_3$ FTJ implemented in [48] can reach giant TER values in the order of 10^6. In addition, further studies with this family of memristors reveal other promising features. Recently, the development of a FTJ with subnanosecond (600 ps) operating speed was presented [49]. This device has also writing current density as low as 4×10^3 A cm^{-2} and is capable to store 32 distinct resistive states (or 5 bits).

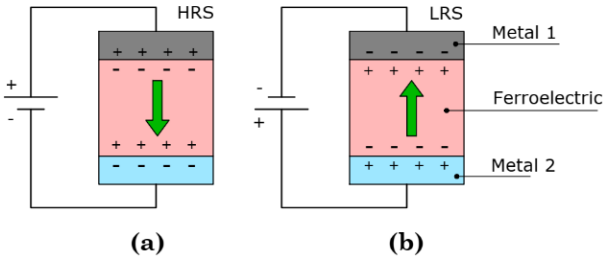


Fig. 5 Schematic of a conventional FTJ built in a Metal/Ferroelectric/Metal stack. Ferroelectric polarization orientation is linked to the switching between (a) high and (b) low resistance states.

III. MEMRISTOR MODELS

Several memristor models have been proposed in the literature. In this section, we present a review of the most common ones. We start with the linear ion drift model, passing through an extensive list of propositions, which explore different devices and abstract levels, and finally conclude highlighting other relevant approaches.

A. Linear ion drift model

The first claim for the practical design of a memristor occurred in 2008, by researchers of HP Labs [3]. The physical structure of this device consists of a thin semiconductor film of thickness D, sandwiched between two platinum contacts. This semiconductor layer is divided into two regions: one, with width *w*, has a high concentration of dopants and, therefore, has a low resistance value, called R_{ON}; the other has a low concentration of dopants and a much higher resistance value, called R_{OFF}. Fig. 6a shows this structure.

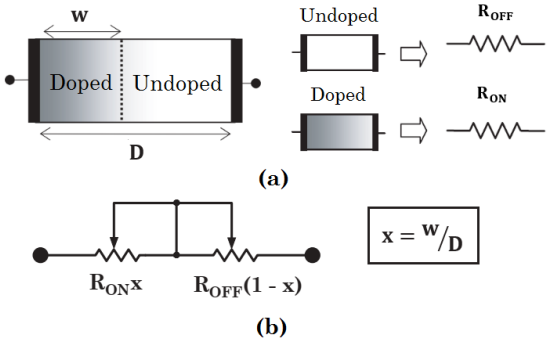


Fig. 6. (a) Physical structure of the memristive device built in the HP Labs, with a thin semiconductor layer sandwiched between two platinum electrodes. The semiconductor film is composed by a doped region with low resistance (R_{ON}) and a undoped region with high resistance (R_{OFF}). (b) Equivalent circuit of the linear ion drift model.

In this device, the non-doped layer consists of insulating TiO_2, while the doped layer is formed by oxygen-poor TiO_{2-x}. In this structure, the oxygen vacancies in the active layer drift in response to the applied electric field, shifting the dividing line between the layers. To represent this behavior, the equivalent circuit shown in Fig. 6b was used, where the resistance of the doped region and the undoped region are connected in series. Considering ohmic electronic conduction and linear ionic drift in a uniform field with average ion mobility μ_V, the mathematical modeling is accomplished according to the expressions (1)-(3):

$$\frac{dw}{dt} = \mu_V \frac{R_{ON}}{D} i(t), \tag{1}$$

$$v(t) = \left(R_{ON}x + R_{OFF}\,(1 - x)\right) i(t), \tag{2}$$

$$x = \frac{w}{D} \in [0,1], \tag{3}$$

where *x* is the normalized state variable. In nanoscale devices, small voltages can yield enormous electric fields, which in turn can produce significant nonlinearities in ionic transport. These nonlinearities manifest themselves particularly at the thin film edges, where the speed of the boundary between the doped and undoped regions gradually decreases to zero [50]. This phenomenon can be modeled, in terms of the normalized variable *x*, as

$$\frac{dx}{dt} = \mu_V \frac{R_{ON}}{D^2} i(t) f(x), \tag{4}$$

where the function *f(x)* adopted is

$$f(x) = x - x^2. \tag{5}$$

B. Nonlinear ion drift model

After the memristive behavior has been correlated to a practical device in [3], different window functions were proposed in the literature aiming to better describe its nonlinear dopant drift. Joglekar and Wolf [51] have proposed the following window function:

$$f(x) = 1 - (2x - 1)^{2p}, \tag{6}$$

where *p* is a positive integer. As the values of *p* are increased, the window function shape approximates to a rectangular window function, and the nonlinear ion drift phenomenon decreases.

However, if *w* reaches one of the bounds, the internal state of the device will not be able to change, since the derivative of *w* will be forced to zero. This issue is referred in the literature as boundary lock. To avoid this problem, a different window was proposed by [50],

$$f(x) = 1 - \left(x - stp(-i)\right)^{2p}, \tag{7}$$

where *p* is an integer number, *i* is the memristive device current and *stp(i)* is a step function, described as

$$stp(i) = \begin{cases} 1, & i \geq 0 \\ 0, & i < 0. \end{cases} \tag{8}$$

The window functions proposed by [51] and [50] do not have a scale factor. Therefore, the maximum value of *f(x)* cannot be greater than one. Motivated by this limitation, a new function was proposed in [52]. It was described as

$$f(x) = j[1 - ((x - 0{,}5)^2 + 0{,}75)^p], \tag{9}$$

where $p \in \mathbb{R}^+$ and j is a control parameter that defines the maximum value of *f(x)*. However, this approach cannot handle the boundary lock problem. A few years later, an improved window function was presented, in order to simultaneously provide a boundary lock solution, full scalability and nonlinear ionic effects [53]. This novel formulation was designed as

$$f(x) = j[1 - (0.25(x - stp(-i))^2 + 0.75)^p], \tag{10}$$

where $p \in \mathbb{R}^+$. In [54] a general window function is proposed, assuming the form

$$f(w) = \alpha(1 - \beta((2x - 1)^2 + \gamma stp(-i))^p), \tag{11}$$

where γ decides the degree of *f(x)* affected by *i*, and β determines the degree of nonlinear drift. The parameter α controls the magnitude of the window function and *p* determines the rate of decrease of the window function when *x* approaches its bounds. In the same work, the authors also provide a set of constraining conditions to facilitate the parameters fitting.

All of these models with nonlinearity introduced by window functions can be computationally implemented using the SPICE macromodel proposed by Biolek et al. [50], whose equivalent circuit is shown in Fig. 7. The operation of the circuit can be summarized as follows. In the second loop, a 1F capacitor integrates the current from the dependent current source G_x, which is given by the expression on the right side of (4). The resulting voltage V_x is numerically equivalent to the normalized width *x* of the doped region. This voltage is used at the dependent voltage source G_{MEM} on the first mesh to ensure that the equivalent resistance between points a and b is consistent with (2).

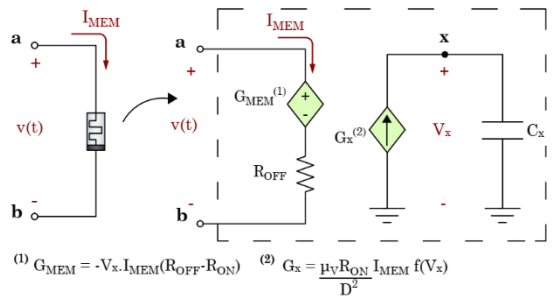


Fig. 7. Equivalent circuit of the model proposed by Biolek et al. [50].

Despite contributions from the models based on window functions presented so far, these works do not fully model nonlinear ion drift behavior since they do not consider the dependence of the state variable derivative on the current.

C. Lehtonen and Laiho Model

An improved version of the model described in [36] was proposed in [55]. As in [36], the *I-V* relationship is given by

$$I = \underbrace{w^n \beta sinh(\alpha V)}_{T1} + \underbrace{\chi[exp(\gamma V) - 1]}_{T2}, \quad (12)$$

where α, β, γ and χ are fitting constants. Here, the state variable w is normalized to have values between 0 (OFF) and 1 (ON). The exponent n of the state variable is used as a free parameter in the model and it affects the switching between ON and OFF states.

In (12), the term T1 is the approximation adopted for the current when the device is in the ON state, which represents essentially the electron tunneling through a thin residual barrier. When the memristive device is on the OFF state, the current will be dominated by the second term T2, which is similar to the ideal diode equation.

The state variable w depends nonlinearly on the voltage over the memristor, i.e.,

$$\frac{dw}{dt} = a\, f(w) v(t)^q, \quad (13)$$

where a is constant and q is an odd integer. As effect of this nonlinear relationship, a programming threshold is inserted into the behavior of the model. A similar model, more complex state drift derivative, is proposed in [56].

D. Pickett's Model

A nonlinear memristive model of bipolar switching was proposed in [16], based on experimental results from a Pt – TiO_2/TiO_{2-x} – Pt device. Unlike the structure shown in Fig. 6b, the device schematic uses a resistor in series with an electron tunnel barrier, as shown in Fig. 8.

In this model, there is a highly nonlinear and asymmetric dynamical response for off and on transitions, as a consequence of an exponential dependence of the drift velocity of ionized dopants on the applied current or voltage and the competing or cooperative behavior of ionic drift and diffusion, depending on the switching voltage polarity.

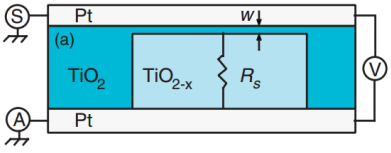


Fig. 8. Schematic of the memristive device described in [16].

The state variable w corresponds to the Simmons Barrier tunnel width. The derivative of the state variable w is interpreted as the speed of the oxygen vacancy, and is represented by the following analytical expressions:

$$\frac{dw}{dt} = f_{OFF} sinh\left(\frac{|i|}{i_{OFF}}\right) \times exp\left[-exp\left(\frac{w - a_{OFF}}{w_c} - \frac{|i|}{b}\right) - \frac{w}{w_c}\right], \quad (14)$$

for $i > 0$ (off switching) and

$$\frac{dw}{dt} = -f_{ON} sinh\left(\frac{|i|}{i_{ON}}\right) \times exp\left[-exp\left(\frac{a_{ON} - w}{w_c} - \frac{|i|}{b}\right) - \frac{w}{w_c}\right], \quad (15)$$

for $i < 0$ (on switching).

The current i through the device is described by the Simmon's formula introduced in [57]:

$$i = \frac{j_0 A}{\Delta w^2}\left\{\phi_1 e^{-B\sqrt{\phi_1}} - (\phi_1 + e|v_g|)e^{-B\sqrt{\phi_1 + e|v_g|}}\right\}, \quad (16)$$

where

$$j_0 = \frac{e}{2\pi h}, B = \frac{4\pi\Delta w\sqrt{2m}}{h}, \lambda = \frac{e^2 \ln(2)}{8\pi\kappa\varepsilon_0 w}, \quad (17)$$

$$\Delta w = w_2 - w_1, w_1 = \frac{1.2\lambda w}{\phi_0}, \quad (18)$$

$$w_2 = w_1 + w\left(1 - \frac{9.2\lambda}{3\phi_0 + 4\lambda - 2e|v_g|}\right), \quad (19)$$

$$\phi_1 = \phi_0 - e|v_g|\left(\frac{w_1 + w_2}{w}\right) - \left(\frac{1.15\lambda w}{\Delta w}\right)\ln\left(\frac{w_2(w - w_1)}{w_1(w - w_2)}\right), \quad (20)$$

where A represents the junction area, e is the elementary electronic charge, v_g is the voltage across the tunnel barrier, m is the mass of the electron, h is the Planck constant, κ is the dielectric constant, ε_0 is the vacuum permittivity and ϕ_0 is the barrier height. Based on the physical model description presented in [16], a SPICE model was presented in [58]. Although this physical model accurately describes the static and dynamic behavior of the TiO_2 memristor, its complexity leads to a computationally inefficient implementation. Moreover, depending on the voltage applied to the device, simulations can present numerical problems, from convergence problems up to finding unphysically solutions [59]. These issues manifest themselves, especially, in large scale simulations, such as crossbar arrays and neuromorphic applications.

E. Eshraghian's Model

Eshraghian et al. [60] introduced a modeling approach based on modified Simmons tunneling relation, which includes the concept of programming threshold. The model is based on the same Metal-Insulator-Metal (MIM) structure introduced in [16] and exhibited in Fig. 8. However, this new proposition explores a different approach for the memristor dynamics, by using simpler equations that simplify its SPICE adaptation. The state equation in this model is given by

$$\frac{dw}{dt} = \begin{cases} f_{on}\left(1 - \frac{v}{2\varphi_0}\right) e^{p(w)\varphi_0\left(1 - \sqrt{1 - \frac{v}{2\varphi_0}}\right)}, & v > 0, w < w_{max} \\ -f_{off}\left(1 + \frac{v}{2\varphi_0}\right) e^{p(w)\varphi_0\left(1 - \sqrt{1 + \frac{v}{2\varphi_0}}\right)}, & v < 0, w > w_{min} \\ 0, & \text{Otherwise.} \end{cases} \quad (21)$$

where f_{on} and f_{off} are fitting constants to identify on and off

switching speeds in a normalized distance. The constant φ_0 is the equilibrium barrier height in eV and *p(w)* is called shape factor function, which is defined as

$$p(w) = \delta + \eta\,(1 - (2w-1)^{2p}), \tag{22}$$

where δ is an offset constant (positive) related to the monotonically increasing condition in (21) and η is a positive constant used to adjust the nonlinearity of *p(w)*. The term $1-(2w-1)^{2p}$ is the window function proposed in [51], and serves to model the nonlinearities at the boundaries.

The tuning of the shape factor allows the programming of different thresholds, which can be specified in a certain range of voltages. In addition, the exponential terms in (22) can be used symmetrically or asymmetrically for negative and positive voltages. The current/voltage relationship uses the same modelling introduced by [36], which is given in (12).

F. Yakopcic's Model

Yakopcic et al. [17] presented a generalized memristive SPICE model based on a set of equations previously presented in [61] . The main goal of this proposal is to reproduce accurately the behavior of several memristive devices for different types of voltage stimulus. In particular, the importance of accurate modeling the memristive response for repetitive dc sweep signals is emphasized, as this is an important requirement for neuromorphic systems development, since neural spikes are similar to this kind of signal.

The generality of the model is supported by its correlation with characterization data from multiple physical devices composed by different materials, such as a-Si and Ag [14], Ag chalcogenide [62], TaO_x [63] and TiO_2 [64]. The I-V relationship is the same proposed in [65], i.e.

$$\mathrm{I(t)} = \begin{cases} a_1 x(t)\sinh\big(bV(t)\big), & V(t) \geq 0 \\ a_2 x(t)\sinh\big(bV(t)\big), & V(t) < 0, \end{cases} \tag{23}$$

where *a1*, *a2* and *b* are constants and *x* is the state variable of the memristor, whose value is constrained between zero and one. The hyperbolic sinusoid shape is typical of electron tunneling. This characterization establishes an increase in conductivity when a specific threshold voltage is surpassed.

The derivative of the state variable is based on the functions *g(V(t))* and *f(x(t))*

$$\frac{dx}{dt} = \eta g(V(t)) f(x(t)), \tag{24}$$

where *g(V(t))* is implemented so that there may be different thresholds depending on the polarity of the voltage

$$\mathrm{g(V(t))} = \begin{cases} A_P\big(e^{V(t)} - e^{V_p}\big), & V(t) > 0 \\ -A_n\big(e^{-V(t)} - e^{V_n}\big), & V(t) < -V_n \\ 0, & -V_n \leq V(t) \leq V_p. \end{cases} \tag{25}$$

In (25), the parameters V_p and V_n represent the positive and negative thresholds, respectively. The constants A_p and A_n correspond to the magnitude of the exponentials. These constants represent how fast the state changes when the voltage across the device is exceeds the threshold. The constant η in (24) defines the direction of the motion of *x* according to the voltage polarity. If $\eta = 1/\eta = -1$, applying a positive voltage above the threshold will increase/decrease the value of *x*.

The function *f(x(t))* is modeled in such a way that the variation in *x* slows down as the state variable approaches the boundaries. Moreover, it is possible to describe the motion of *x* in different ways, according with the polarity of the input voltage.

$$f(x) = \begin{cases} e^{-\alpha_p (x - x_p)} w_p(x, x_p), & x \geq x_p \\ 1, & x < x_p, \end{cases} \tag{26}$$

$$f(x) = \begin{cases} e^{\alpha_n (x + x_n - 1)} w_n(x, x_n), & x \leq 1 - x_n \\ 1, & x > 1 - x_n. \end{cases} \tag{27}$$

In the function *f(x(t))*, the variable motion will be constant until it reaches the points x_p or x_n. After these points are surpassed, the motion of the state variable will be reduced by a decaying exponential function at a rate of α_p and α_n, for x_p and x_n, respectively. In (26)-(27), $w_p(x, x_p)$ and $w_n(x, x_n)$ are window functions that nullify *f(x)* it reaches its boundary values:

$$w_p(\mathrm{x}, x_p) = \frac{x_p - x}{1 - x_p}, \tag{28}$$

$$w_n(\mathrm{x}, x_n) = \frac{x}{1 - x_n}. \tag{29}$$

These four fitting constants allow to adequate the motion of the state variable according with the dynamic of different memristive devices.

In [66], it was proposed a model whose mathematical description of the state variable is very similar to (24)-(29), but its I-V relationship is based on (2), which is a much simpler approach than (23). The characteristics of this alternative proposition aim to meet the requirements of applications with complementary resistive switches (CRS).

G. TEAM and VTEAM Models

A generalized model called TEAM (Threshold Adaptive Memristor Model) was presented in [15]. This model represents the same physical behavior presented in [16], but with simpler mathematical functions and with flexibility to characterize a variety of different practical memristive devices.

This model assumes that there is no change in the state variable below a certain threshold, and a polynomial dependence on the current is adopted. The derivative of the state variable for the proposed model is

$$\frac{dx}{dt} = \begin{cases} k_{off}\left(\dfrac{i(t)}{i_{off}} - 1\right)^{\alpha_{off}} f_{off}(x), & 0 < i_{off} < i \\ 0, & i_{on} < i < i_{off} \\ k_{on}\left(\dfrac{i(t)}{i_{on}} - 1\right)^{\alpha_{on}} f_{on}(x), & i < i_{on} < 0, \end{cases} \tag{30}$$

where k_{off}, k_{on}, α_{off} and α_{on} are fitting constants, i_{off} and i_{on} are the threshold currents, and *x* is the internal state variable, which represents the effective electric tunnel width. The functions $f_{off}(x)$ and $f_{on}(x)$ acts as window functions which ensures that $x \in [x_{on}, x_{off}]$. If a linear variation of memristance as a function of *x* is considered, then the *I-V* relationship becomes

$$v(t) = \left[R_{ON} + \frac{R_{OFF} - R_{ON}}{x_{OFF} - x_{ON}}(x - x_{ON})\right] i(t). \tag{31}$$

However, in order to fit the behavior of some practical devices, such as [16], where the memristance change is dependent on a highly nonlinear tunneling effect, a different expression is proposed:

$$\mathrm{v(t)} = \mathrm{R_{ON}} e^{\frac{\lambda}{(\mathrm{x_{off}} - \mathrm{x_{on}})}(\mathrm{x} - \mathrm{x_{on}})} \mathrm{i(t)}, \tag{32}$$

where λ is a fitting parameter

$$e^{\lambda} = \frac{\mathrm{R_{OFF}}}{\mathrm{R_{ON}}}. \tag{33}$$

In the same work, the authors prove the flexibility of the model by fitting the Simmons Tunnel Barrier model. Besides the result is sufficient accurate, the simplicity of TEAM improves the computational efficiency in the simulations.

Since the characterization data of many physical devices exhibits a threshold voltage [3, 67, 68], a voltage-controlled model analogous to TEAM was developed to support this kind of behavior, which was named VTEAM [69]. VTEAM also provides the parameter setting to fitting some particular models, such as [61, 67, 70]. Both TEAM and VTEAM models have been implemented in Verilog-A.

H. Pershin, Di Ventra Model

Pershin and Di Ventra introduced in [71] a generic memristor model whose resistance switching mechanism is based on the existence of a threshold voltage. Mathematically, the authors propose a memristive system described by the following set of equations:

$$\mathrm{I_{MEM}} = \mathrm{R_{MEM}}^{-1}\mathrm{V_{MEM}}, \tag{34}$$

$$\frac{d(R_{MEM})}{dt} = \begin{cases} f(V_{MEM}), & V_{MEM} > 0 \text{ and } R_{MEM} < R_{OFF} \\ f(V_{MEM}), & V_{MEM} < 0 \text{ and } R_{MEM} > R_{ON} \\ 0. & \text{Otherwise.} \end{cases} \tag{35}$$

$$f(V_{MEM}) = \beta V_{MEM} + 0.5(\alpha\text{-}\beta) \times (|V_{MEM} + V_T| - |V_{MEM} - V_T|). \tag{36}$$

In (34) , R_{MEM} represents the resistance of the device, which relates the instantaneous voltage V_{MEM} over its terminals and the instantaneous current I_{MEM} flowing through it. Equation (35) describes the resistance variation rate of the device according to $f(V_{MEM})$, when $|V_{MEM}| > 0$ and $\mathrm{R_{ON}} < R_{MEM} < \mathrm{R_{OFF}}$. Otherwise, there will be no resistance variation. $\mathrm{R_{ON}}$ and $\mathrm{R_{OFF}}$ are parameters related to the minimum and maximum resistance boundaries, respectively.

The function $f(V_{MEM})$ uses some important parameters of the model, one of which is the threshold voltage V_T. Exceeding this voltage level can trigger the start of the resistance switching or significantly increase a switching already started, which will depend on the configuration of the parameters α and β. These parameters characterize the rate of growth or decrease of the resistance variation, when $|V_{MEM}| < V_T$ and $|V_{MEM}| > V_T$, respectively. A SPICE implementation of this model was presented in [72]. Based on this work, we proposed a new model for threshold current controlled memristors in [73]. In this implementation, naturally, all the variables and the parameters expressed as electrical voltages in the reference material were replaced by the corresponding electric currents. Moreover, a new function (dependent on the resistance itself) called proportionality factor has been added to the mathematical modelling, so that the rising ($R_{ON} \rightarrow R_{OFF}$) and falling ($R_{OFF} \rightarrow R_{ON}$) transitions can be handled differently. In addition, the adopted approach increases the non-linearity of the transitions as they approach the intended values, which also favors the convergence of simulations.

I. Spintronic Memristor Model

Zhang et al. [74] presented a compact model of CoFeB/MgO/CoFeB PMA MTJ [5, 75] based on the STT switching mechanism. In this proposition, the resistance of the MTJ is calculated through a simplified equation obtained from the physical model introduced by [76], i.e.,

$$R_P = \frac{t_{OX}}{F \times \bar{\varphi}^{1/2} \times Area} \times \left(1.025 \times t_{OX} \times \bar{\varphi}^{1/2}\right), \tag{37}$$

where R_P is the resistance of the MTJ in the parallel state, $\bar{\varphi} = 0.4$ is the potential barrier height of crystalline MgO, t_{OX} is the thickness of the oxide barrier, and *Area* is the MTJ area. *F* is a factor calculated from the resistance–area product (R-A) value of the MTJ, which depends on the material composition of the three thin layers.

Another important aspect of the model is the description of the TMR ratio. This variable is calculated considering the influence of the bias voltage V_{bias}, according to the theory evidenced in [77], resulting in

$$TMR_{real} = \frac{TMR(0)}{1 + \frac{{V_{bias}}^2}{{V_h}^2}}, \tag{38}$$

where TMR_{real} is the real value of the TMR ratio during simulation, *TMR(0)* is the TMR ratio with 0-V bias voltage, and V_h is the bias voltage as $TMR_{real} = 0.5 \times TMR(0)$. The default values of *TMR(0)* and V_h are set to 120% and 0.5 V, respectively. Thus, the resistance of the MTJ in the anti-parallel state (R_{AP}) can be calculated as

$$R_{AP} = R_P \times (1 + TMR_{real}). \tag{39}$$

The threshold or critical current I_{C0} involved in the STT mechanism is defined as:

$$I_{C0} = \alpha \frac{\gamma e}{\mu_B g} (\mu_0 M_S) H_K V = 2\alpha \frac{\gamma e}{\mu_B g} E, \tag{40}$$

where *E* is the barrier energy, H_K is the effective anisotropic field, μ_0 is the vacuum magnetic permeability, M_S is the saturation magnetization, α is the magnetic damping constant, γ is the gyromagnetic ratio, *e* is the elementary electrical charge, μ_B is the Bohr magnet and *V* is the volume of the free ferromagnetic layer. The variable *g* is a function of the spin polarization percentage of the tunnel current and the angle between the magnetization of the free and reference layers.

The switching dynamics relates the writing current and the time required to perform this operation, based on the equation presented by [75]:

$$\frac{1}{\langle\tau\rangle} = \left[\frac{2}{C + \ln\left(\frac{\pi^2 \xi}{4}\right)}\right] \frac{\mu_B \mathrm{P_{ref}}}{em(1 + \mathrm{P_{ref}P_{free}})} (\mathrm{I_w} - \mathrm{I_{c0}}), \tag{41}$$

where $\langle\tau\rangle$ is the average switching time, *C* is Euler's constant, P_{ref} and P_{free} are the tunneling spin polarizations of the reference and free layers (the model assumes $P_{ref} = P_{free} = P$), m is the magnetic moment of the free layer, I_w is the writing current and I_{c0} is the zero temperature threshold current; $\xi = E/k_B T$ is the activation energy, k_B is the Boltzmann constant and *T* is the temperature.

The compact model was implemented in Verilog-A and its was validated through the simulation of a writing circuit and a nonvolatile flip-flop. In order to facilitate the configuration of the model, the authors provide a list of default parameters and variables.

J. Other models and correlated works

In addition to the models covered in this Section, there is a wide variety of works focused on different aspects of the memristive devices modeling. Regarding models related to practical implementations, Zhang et al. [78] proposed a model consistent with experimental data from different devices intended for the development of electronic synapses. Bayat et al. [79] presented a general phenomenological approach for deriving mathematical equations for modeling real memristive devices. Lupo et al. [80] reported a model for oxide-based filamentary memristors, and the simulation results showed excellent match with HfO_2 devices.

Extending the discussion, Naous et al. [81] presented an study where stochasticity phenomenon are incorporated into the behavior of different threshold-based memristors models. There is also a concentration of efforts in the modification of computationally complex models, which may present several numerical problems, mainlly in large scale simulations[82].

Another alternative for the design and testing of memristive systems are the emulator circuits. These tools allow us to build circuits based on memristors at the hardware level. Emulators can be designed in different ways. Pershin and Di Ventra [83] combined a digital potentiometer, an analog-to-digital converter and a microcontroller to create a circuit for this purpose. Implementations based on components such as operational amplifiers, voltage multipliers, MOSFETs, resistors and capacitors are also common [84, 85].

IV. APPLICATIONS

Memristors provide the unique opportunity to either supplement or replace CMOS technology. In this section we explore the potential of memristors in several applications. Digital applications are the first aspect explored, following to the analog ones. Resistive memories are discussed together with nonvolatile Flip-Flops. The neuromorphic computation closes this Section.

A. Digital Applications

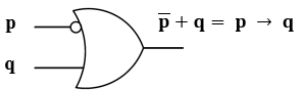
There is a large amount of memristor-based methods and circuits focused on performing logic operations. This broad spectrum of propositions includes different philosophies for the implementation of Boolean functions, some with universal coverage and others limited to some specific operations. This Section intends to give an overall insight of the main contributions in this field of research.

1) Imply Logic

Material implication is a logical operation represented as p → q or p IMP q, meaning “p implies q” or “if p then q”. By observing the truth table of this function, in Fig. 9a, it is possible to note that the operation p → q is logically equivalent to the expression $\overline{p} + q$. For this reason, this function can be represented by the symbol shown in Fig. 9b. An important feature of the IMP function is that, along with the FALSE operation (that always yields logic value ‘0’), it composes a complete computational set that can be used to perform any logic operation. The implementation of this function can be performed by the circuit shown in Fig. 10.

p	q	p → q
0	0	1
0	1	1
1	0	0
1	1	1

(a)



(b)

Fig. 9. (a) Truth table of p → q. (b) Symbol of IMPLY logic gate.

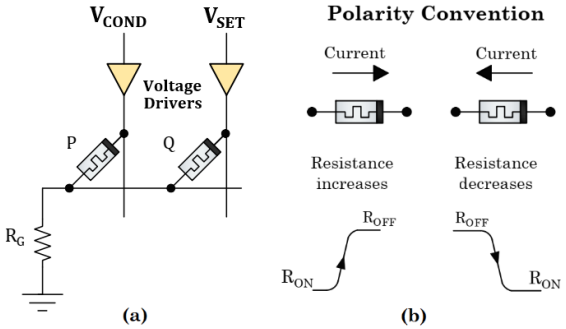


Fig. 10. (a) Circuit proposed in [86] for the implementation of memristive material implication. (b) Polarity convention for increasing/decreasing resistance.

The logical variables of this structure are the resistances of P and Q, so that a logic level '1' corresponds to a low resistance state R_{ON} and a level '0' corresponds to a high resistance value R_{OFF}. The computation of the imply operation is performed by applying voltages V_{COND} and V_{SET} to P and Q, respectively. It should be noted that the input memristors at the beginning of the operation are P and Q, and the output memristor at the end of the operation is Q (the input value of Q may be destroyed). In addition, the following conditions must be met to ensure the operation of a material implication:

$$V_{COND} < V_C < V_{SET}, \quad (42)$$

$$(V_{SET} - V_{COND}) < V_C, \quad (43)$$

$$R_{ON} < R_G < R_{OFF}, \quad (44)$$

where V_C is the critical voltage, a minimum value required to change the state of the memristor. The polarity shown in Fig. 10b is assumed. When computing an implication, the current direction in the memristors can only be from top to bottom. So, whenever Q starts at ‘1’, that state will remain unchanged (combinations “01” and “11”). When P = ‘0’ and Q = ‘0’, most of the V_{COND} and V_{SET} voltages will fall on their respective memristors, switching Q to ‘1’ and keeping P at ‘0’. Lastly, when P = ’1’ and Q = ’0’, V_G will be approximately V_{COND} and the voltage over Q will be V_{SET}-V_{COND}, which is insufficient to cause a resistance switching in this device. Laiho and Lehtonen [87] showed the extension of this operation to multiple input memristors. Later, the concept of multi-memristor implication was proposed as a generalization of this approach [88].

2) MAGIC

An important memristor-only logic family was proposed in [89]. In this method, called MAGIC (Memristor-Aided logic), a logic gate is built with an individual memristor for each of its inputs and an additional memristor for the output. As in the imply logic, logical values are stored through resistance states. The schematic circuits corresponding to the implementation of the AND, NAND, OR, NOR and NOT gates in this logic family are shown in Fig. 11.

The description of the operation of a MAGIC gate will be based on the same polarity convention shown in Fig. 10b and divided into two steps. The first step consists in the initialization of the output memristor to a specific logical state. In the second step, a voltage V_0 is applied to the circuit (see in Fig. 11) and is divided between its components. For some input combinations, the voltage drop across the output memristor will be sufficient to surpass a certain threshold value and, consequently, change its logical state. For other input combinations, this will not happen and the output memristor remains at its pre-established state.

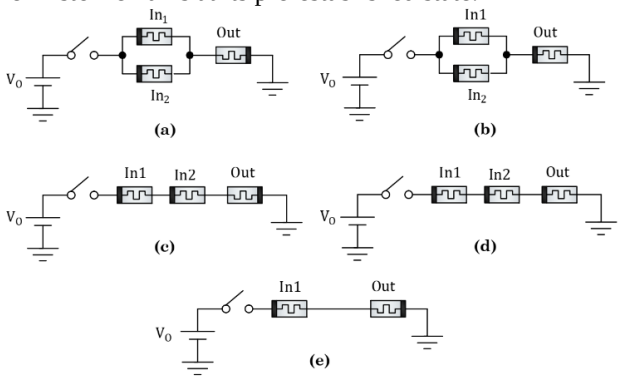


Fig. 11. (a) MAGIC logic gates of (a) NOR, (b) OR, (c) NAND, (d) AND and (e) NOT.

The description of the operation of a MAGIC gate will be based on the same polarity convention shown in Fig. 10b and divided into two steps. The first step consists in the initialization of the output memristor to a specific logical state. In the second step, a voltage V_0 is applied to the circuit (see in Fig. 11) and is divided between its components. For some input combinations, the voltage drop across the output memristor will be sufficient to surpass a certain threshold value and, consequently, change its logical state. For other input combinations, this will not happen and the output memristor remains at its pre-established state.

For a NOR gate, for example, the first step is to write logic level '1' on the output memristor and, if necessary, write the input values on the memristors In_1 and In_2. After that, the computation is performed by applying a voltage V_0 to the circuit, as shown in Fig. 11a. Assuming $R_{OFF} >> R_{ON}$, when the input combination is "00", the equivalent resistance of $In_1 \parallel In_2$ is $R_{OFF}/2$, causing the voltage (current) over (across) the output memristor to be lower than the threshold voltage (current). Hence, the logical state of the output memristor does not change and remains at logical one. For other input combinations, the voltage/current is greater than the memristor threshold voltage/current. The logical state of the output memristor for these input combinations switches to logical zero.

MAGIC and Imply Logic are memristive-based design approaches that can be integrated within a crossbar array and enable in-memory-computing, i.e., simultaneous processing and storage of data by the same circuit [11, 90].

3) MRL

MRL (Memristor Ratioed Logic) family [91] combines memristive and CMOS technologies. In this logical family, the AND and OR gates are implemented with memristors. These gates are combined with a CMOS inverter to form the NAND and NOR gates, which are universal Boolean functions. The NOT gate also serves to restore degraded signals. An overview of such implementations is provided in Fig. 12. The following explanation regarding the operation of these gates is based on the polarity convention depicted in Fig. 10b and covers AND/OR gates. When the inputs have identical logic levels, there is no current flowing through the memristors and, therefore, there is also no resistance variation in these devices. Thus, V_{OUT} follows the input values in these cases. However, when the inputs are different, there will be a current flow from the V_{HIGH} voltage terminal (level '1') to the V_{LOW} terminal (level '0'), ensuring complementary resistance states in the devices. The output voltage will be determined by a voltage divider. Assuming $R_{OFF} \gg R_{ON}$, if the grounded memristor is in the R_{OFF} state, then $V_{OUT} \cong V_{HIGH}$. If it is in the R_{ON} state, then $V_{OUT} \cong 0$ V. The number of inputs can be extended by connecting more memristors to the common node, similar to a logic with diodes.

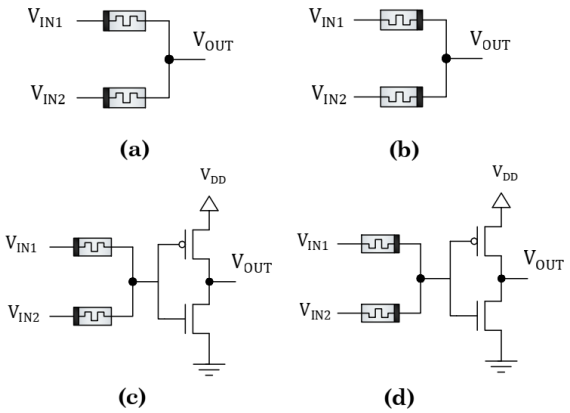


Fig. 12. Schematic of the MRL gates. a) OR gate. b) AND gate. c) NOR gate. d) NAND gate.

4) Other implementations

The scope of alternatives for the design of memristive logic circuits also includes other notable techniques such as Programmable CMOS/Memristor Threshold Logic [92], CMOS-like Memristor Complementary Logic [93], Parallel Input-Processing Memristor Logic [94] and Memristors-As-Drives Gate Design [95]. In addition, several works employ memristive devices in the development of alternative versions of classic circuits, including full-adders [96, 97], Look-Up Tables (LUTs) [98], sense amplifiers [99], majority voters [100], etc.

B. Analog Applications

Memristors with gradual resistance variation can be exploited in several analog circuit implementations. Pershin and Di Ventra presented in [83] a few examples of memristive-based programmable analog circuits, including a voltage comparator, a non-inverting amplifier and a Schmitt trigger. There are also reports of the use of memristors in different types of oscillators, such as Wien bridge oscillator [101], phase-shift oscillator [102] and reactance-less oscillator [103]. Ascoli et al. [104] bring an insight on adaptable filtering design with memristors, presenting a first-order low-

pass filter with tunable cutoff frequency and a second-order band-pass filter with tunable quality factor. Potrebić et al. [105] analyze the application of memristors in several RF/microwave circuits, such as the Wilkinson power dividers, antennas, frequency selective surfaces, and others.

By exploring cumulative resistance variations in phase-change memristors, Wright et al. [12] demonstrated that analog computation is able to carry out the full set of arithmetic operations (addition, subtraction, multiplication, division), besides being able to handle other complex tasks such as parallel factorization and fractional division. There is also in the group of analog implementations a primary application for computational systems, which is the vector-by-matrix multiplication. This task can be performed in a single step from a memristive crossbar array [106], as shown in Fig. 13.

In a simplified way, this operation can be described using the following multiplication as an example:

$$B_{1xM} = x_{1xN} \times A_{NxM} \tag{45}$$

To perform this operation, the elements of vector **x** will be converted into a set of input voltage signals and the elements of matrix **A** will be mapped as conductances of the memristors in the crossbar. Then, by applying the voltage vector to the matrix rows, these components will be intrinsically multiplied by the column elements (memristor conductances) following Ohm's law, and the sum of the currents through each column will naturally be computed according to the KCL rule. For an arbitrary column α, the current is given by:

$$I_\alpha = \sum_{k=1}^{N} V_k^{in} \times G_{k,\alpha}\,, \tag{46}$$

where V_k^{in} is the voltage input vector and $G_{k,\alpha}$ is the conductance vector for the column α. The output current vector can be applied to transimpedance amplifiers (TIA), for example, to perform the conversion to voltage values. This technique provides essential support for the development of several applications involving neuromorphic computing, the subject of the next subsection.

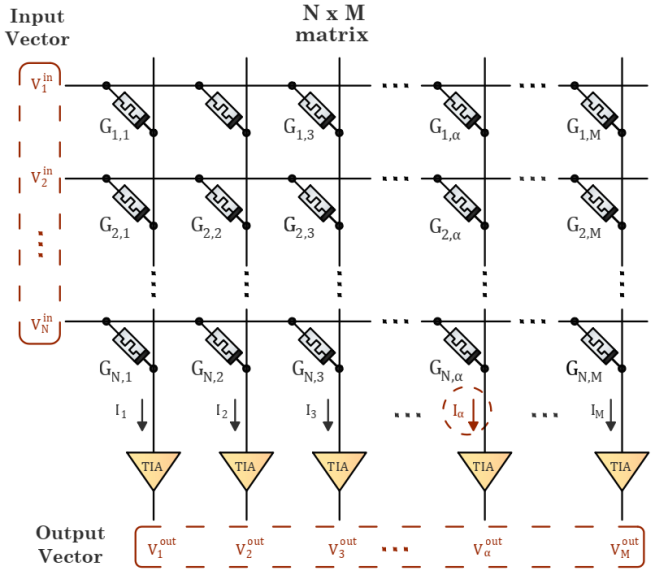


Fig. 13. A memristor crossbar array for vector-by-matrix multiplication.

C. Memory Applications

Memory circuits may be considered one of the most promising applications involving memristive devices. They challenge the traditional memory hierarchy, where nonvolatile memories are at the bottom of the hierarchy and are large and slow. The small memristor dimension allows high storage density. The data is stored as resistance rather than electric charge, which allows longer data retention and no leakage currents. This feature makes memristors potential candidates to replace the current mainstream memory.

There are two main RRAM memory architectures: crossbar [90, 107-109] and grid [110-113]. The crossbar approach does not have access transistors in its memory cell topology. The cell is the memristor itself or the memristor and a diode-selector. Fig. 14 exemplify both structures. This characteristic makes it attractive to intense high density. However, the crossbar structure faces issues in terms of switching, access and writing time, array size, and operating voltage, which are caused by the wire resistance and sneak paths [107, 108]. Furthermore, several techniques have been proposed to deal with those aspects [109, 114].

The grid architecture, illustrated in Fig. 15, is more energy efficient and presents superiority in access time when compared to the crossbar solution. However, grid architecture presents higher size and consequently lower density and higher cost. Even so, RRAM grid architecture, when compared to traditional 6T SRAM, presents significant higher density associated to low power consumption.

As in traditional SRAM architecture, the memory cell is also explored in RRAM grid to improve specific aspects. The smaller memory cell is the one composed by one transistor and one memristor [111]. It is called 1T1M. Emara et al. [110] introduces the 1T2M differential memory cell to deal with single and multi-bit data storage. The 2T2M cell is presented to offer higher stability and noise margins when compared to the previous ones [113]. Fig. 16 illustrates all this three RRAM memory cells.

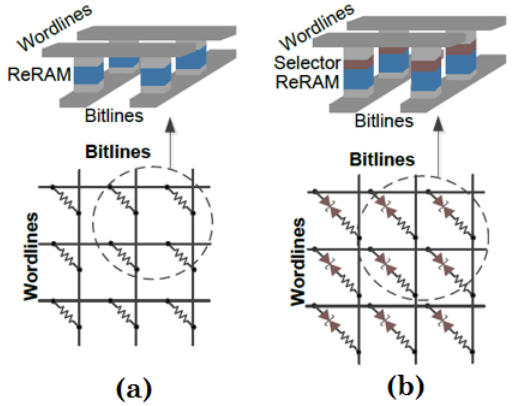


Fig. 14. Crossbar RRAM structure (a) without selector and (b) whit diode-selector [108].

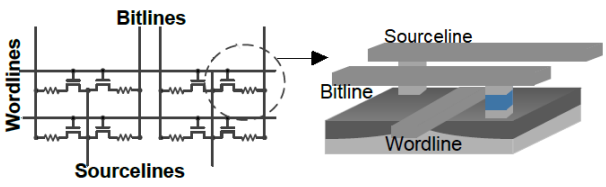


Fig. 15. Grid RRAM structure with 1T1R memory cell [108].

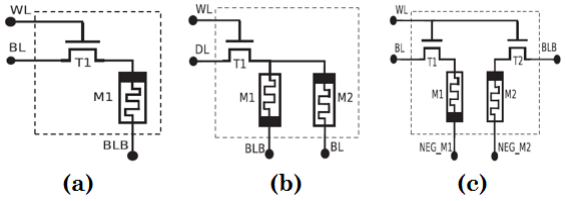


Fig. 16. Topologies of memristor-based RRAM cells. (a) 1T1M, (b) 1T2M, and (c) 2T2M [112].

Some memristors have continuous resistance change. This characteristic has been explored to design memory cell that are able to store more than a single bit [115]. This multi-level memory cells increase even more the memory capacity. In this solution, more issues beyond the ones already mentioned have to be solved. One of the more important is related to the nonlinear nature of memristor dynamic behavior. To deal with this, the voltage application to define the resistance value explore different types of programming strategies [116, 117].

In addition to high-density memories, memristors are also being explored in the design of nonvolatile latches and flip-flops (NVFF). These components can transform traditional processors into fully nonvolatile circuits by storing permanently all the data. They are vital elements for fast and energy efficient hibernation in nonvolatile processors (NVPs). The non-volatility enables NVPs to decrease the start-up latency from some micro seconds down to some hundreds of pico-seconds [118].

Fig. 17 presents complete schematic of a non-volatile flip-flop (NVFF). This solution is only one of several existing in the literature. The design uses two complementary MTJs per bit to achieve higher robustness. In addition to the two MTJ, the schematic contains the sense amplifier used to read the data and the bidirectional current source responsible to write the information in the MTJs. The presented schematic performs the storing data in a single-phase. There are other solutions that uses an initial reset operation in both devices, and later set the specific memristor according to the data to be stored [119]. Comparing both solutions, the two-phase reduces the minimum time and energy required in the operation. However, the reset operation in all cycles compromise the cell endurance. The cell endurance (the maximum number of transitions between the high and low resistive states) may be considered the main limitation of NVFFs. This limited endurance can reduce the lifetime of NVPs and is receiving special attention in the community [120].

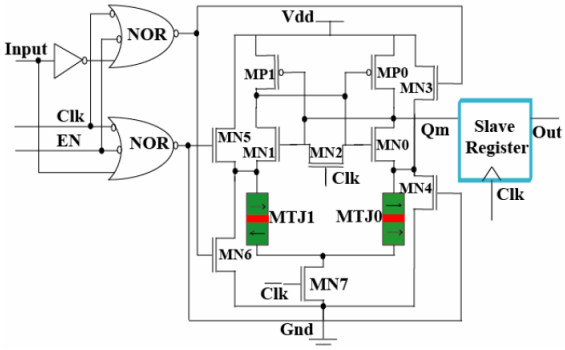


Fig. 17. Complete Schematic of MTJ-based non-volatile FF [118].

D. Neuromorphic Computing

The memory bottleneck has been an important barrier to the advance of conventional Von Neumann computing systems, once this issue leads to high power consumption and performance degradation [121]. In order to overcome these limitations, novel architectures and emerging technologies have been studied. In this context, one of the most promising alternatives consists of neuromorphic computing. This concept, introduced by Mead in [122], describes the use of VLSI systems to mimic the nervous system in the brain. This system is fundamentally composed by neurons and synapses, and the interconnections between these elements form the so-called neural networks. A neuron can be roughly described as a processing unit that integrates the inputs coming from other neurons and generates action potentials (spikes) as a result. The synapses are adaptive memory elements that change their connection strength (or weight) as a result of neuronal activity, which is known as synaptic plasticity [123]. This mechanism is believed to underlies learning and memory of the biological brain. In order to mimic the massive parallelism inherent to the nervous system, which have $\sim 10^{11}$ neurons and $\sim 10^{15}$ synapses, scalability and ultra-low power consumption are key factors for neuromorphic computing.

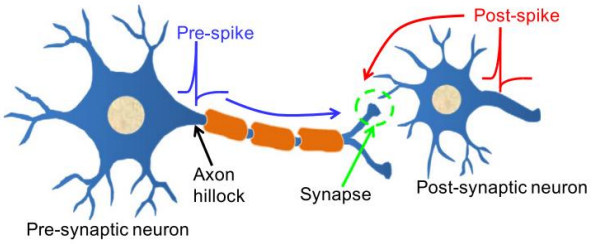


Fig. 18. Illustration of the interconnection between two neurons [123].

Each neuron is mainly composed by a cell body called soma, branched projections called dendrites and a long terminal called axon. The contact areas where the information is transmitted from one cell to another are called synapses [123].

This area of research has shown great interest in memristive technology, since these devices not only meet these requirements but also have a programmable resistance quite similar to the plasticity of a biological synapse. The neuromorphic computing is usually implemented in a crossbar configuration, as shown in Fig. 19a. In this structure, every neuron in the pre-neuron layer (vertical lines) is connected to every neuron in the post-neuron layer (horizontal lines) with individual memristive synaptic weights (resistance). These spiking neural networks (SNNs) can be trained to perform several tasks, using a set of different learning rules/algorithms. Learning rules describe changes in synaptic plasticity, that is, they determine when the strength of the connections increases or decreases. There is a considerable amount of learning rules, divided as supervised, unsupervised and reinforcement learning [124]. An experimentally demonstration of the Spiking-Time Dependent Plasticity (STDP) learning rule was presented in [14]. In this mechanism, the synapse weight changes according to an exponentially decaying

function of the delay time between the pre-synaptic and pos-synaptic spikes, as shown in Fig. 19b. When a pre-spike precedes a post-spike, Δt = tpost - tpre is positive and the weight increases (see in Fig. 19c). when this sequence is reversed, Δt is negative and the weight decreases.

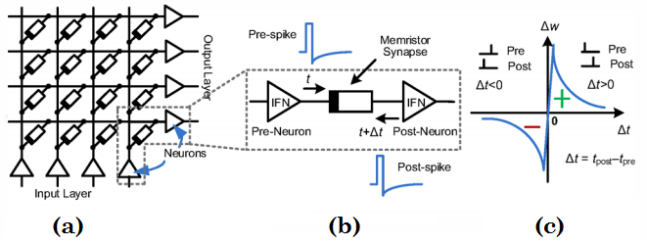


Fig. 19. (a) Typical crossbar architecture of a SNN with memristor synapses connecting neurons. (b) Excitation of a matrix synapse by pre and post spikes separated by a Δt interval. (c) STDP learning curve [125].

Another topic with special emphasis in studies related to this area of interest is neural behavior. Although there is a large amount of CMOS implementations of artificial neurons [125-127], these circuits usually require a large number of transistors. Thus, memristor-based neurons have been proposed to simplify the circuits. For instance, the electrical circuit of the classic Hodgkin-Huxley model [128] was redesigned in [129], replacing two variable resistors in the potassium and sodium channels with first and second order memristors, respectively (see Fig. 20a). In [130], a scalable neuristor, an electronic device with properties similar to the Hodgkin–Huxley axon, was built from two nanoscale Mott memristors.

Other notable contributions based on memristors adapt in hardware the behavior of classic models like Morris-Lecar [131], FitzHugh-Nagumo [132] and Hindmarsh-Rose [133]. In addition, there is also reports of memristive-based integrate-and-fire (I&F) neurons [134, 135]. As an example, Cobley et al. [13] presented a simple self-resetting I&F spiking neuron model based on the exploitation of the accumulation property of PCM devices. The schematic of this implementation is shown in Fig. 20b. Initially, the memristive device is in an amorphous state (high resistance) and is excited by postsynaptic pulses. After a certain number of pulses, the PCM cell switches to the crystalline state (low resistance), causing the voltage at non-inverting input of the comparator to rise above V_{REF} (through the low-pass filter composed of R_{LPF} and C_{LPF}). As a consequence, the comparator output switches to high level and a spike is generated. The output is fed back through a delay block, which forces the PCM device back to the amorphous state. Further insight regarding this subject can be found in [136], where a comparative analysis in different aspects is made between several CMOS and memristive-based neuron models.

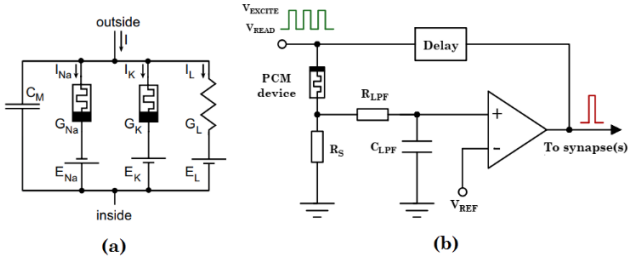


Fig. 20. (a) Memristive Hodgkin-Huxley axon membrane circuit proposed by [129]. (b) Self-resetting spiking phase-change neuron [13].

Interesting applications have been exploited in neuromorphic computing. Prezioso et al. [137] realized the pattern classification of 3x3 pixel black/white images into three classes, while Yao et al. [138] showed a more complex gray scale face classification. Based on the same concepts, Truong et al. [139] developed a system for speech recognition of five vowels and Jeong et al. [140] proposed an accurate method for calculating the Euclidean distance. In addition, Choi et al. [141] used a memristive network to perform feature extraction and analyze sensory data from a standard breast cancer screening database.

V. FINAL CONSIDERATIONS

In this paper, we discussed several aspects related to memristors. They represent one of the most promising emerging alternatives to replace or complement the standard CMOS. We described the current state of the art in memristor devices, models and applications. We examined how memristors can be used as building blocks for on-chip memory and many other digital and analog circuits. Additionally, we showed that its features conveniently meet the requirements for the implementation of neuromorphic computing. While many challenges remain to be addressed, we believe that memristors can enable computing paradigms in beyond-CMOS era. We consider memristors an active and vibrant field of research, with extensive efforts under way. Advances are continuously presented in the literature, and we tried to summarize part of them in this paper.

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