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Single-Trimming Resistorless CMOS Sub-Bandgap Voltage References for High Precision Applications

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“Al fin y al cabo, somos lo que hacemos para cambiar lo que somos.”
— EDUARDO GALEANO

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ABSTRACT

A voltage reference is a relevant circuit class since its output voltage should generate an accurate reference for many analog, mixed-signal, and digital applications. This type of circuit works based on the mutual compensation of the temperature dependencies of two electrical quantities. Considering that these quantities also depend on the fabrication process, the voltage reference performance is heavily affected by fabrication variability. The reduction or compensation of the variability impact on the reference performance is a considerable design challenge, required to increase its precision and robustness. Hence, this work proposes two sub-bandgap voltage references that are designed to reduce the variability impact on the reference voltage to enhance its precision. A BJT biasing circuit, a self-cascode MOSFET, an unbalanced differential pair and a high-slope PTAT structure were analyzed to understand how to minimize the main error sources, such as fabrication variability and intrinsic non-linearities. From this investigation, a sheet specific current (I_{SQ}) source was implemented for biasing a BJT to reduce the variability of its generated base-emitter voltage. Also, the self-cascode MOSFET and the unbalanced differential pair architectures were chosen to form the proposed voltage references. A single-point trimming strategy was presented to reduce the temperature sensitivity of the circuits. The voltage references topologies are analytically described and the UICM model was used to design the circuits. The circuits are resistorless and were designed in a 180 nm process. Also, the performance of the voltage references were evaluated through post-layout simulation. Then, the proposed sub-bandgap reference with self-cascode MOSFETs (SBSCM) presented a 592 mV reference voltage with a typical temperature coefficient (TC) of 3.6 ppm/°C, while consuming just 40.8 nW under 1.8 V of power supply. The sub-bandgap reference with an unbalanced differential pair (SBDF) resulted in a 607 mV reference voltage with a typical TC of 8.3 ppm/°C and consuming 40 nW under 1.8 V of supply voltage. Monte-Carlo simulations demonstrated the sensitivity of the implemented design to fabrication variability. Considering the variability impact and the trimming scheme, the SBSCM and the SBDF presented an average TC of 6.9 ppm/°C and 11 ppm/°C, respectively. The circuit's performance presented low power consumption and TC with an accurate output voltage while occupying a small silicon area.

Keywords: CMOS analog design, voltage reference, high precision, trimming, low power.

Referências de Tensão Sub-Bandgap CMOS sem Resistores com um Único Ajuste para Aplicações de Alta Precisão.

RESUMO

A referência de tensão é uma classe de circuito relevante já que sua tensão de saída deve gerar uma referência precisa para muitas aplicações analógicas, de sinais mistos e digitais. Esse tipo de circuito funciona baseado na compensação mútua de dependências de temperatura de duas grandezas elétricas. Considerando que essas grandezas também dependem do processo de fabricação, o desempenho das referências de tensão são profundamente afetadas pela variabilidade de fabricação. A redução ou compensação do impacto da variabilidade no desempenho da referência é um desafio considerável de projeto, necessário para aumentar sua precisão e robustez. Por isso, esse trabalho propõe duas referências de tensão do tipo sub-bandgap que são projetadas para reduzir o impacto da variabilidade na referência de tensão para aumentar a precisão. Um circuito de polarização de um transistor bipolar, um MOSFET self-cascode, um par diferencial desbalanceado e uma estrutura PTAT high-slope foram analisadas para identificar como minimizar as principais fontes de erros, como a variabilidade de fabricação e não-linearidades intrínsecas. A partir dessa investigação, uma fonte de corrente I_{SQ} foi implementada para alimentar um transistor bipolar e reduzir a variabilidade da tensão de base-emissor gerada. Além disso, as estruturas de MOSFET self-cascode e do par diferencial desbalanceado foram escolhidos para formar as referências de tensão propostas. Uma estratégia de calibração em um único ponto foi apresentada para reduzir a sensibilidade à temperatura do circuito. As topologias de referências de tensão são descrevidas analiticamente e o modelo UICM foi utilizado para projetar o circuito. Os circuitos não possuem resistores e foram projetados em um processo de 180 nm. Além disso, o desempenho dos circuitos é avaliado através de simulações feitas após o layout. Então, a referência sub-bandgap com MOSFET self-cascode (SBSCM) apresentou uma referência de tensão de 592 mV com um coeficiente de temperatura (TC) típico de 3.6 ppm/°C, consumindo 40.8 nW com uma fonte de alimentação de 1.8 V. A referência sub-bandgap com o par diferencial desbalanceado (SBDF) resultou em uma referência de tensão de 607 mV com um TC típico de 8.3 ppm/°C e consumindo 40 nW com 1.8 V de tensão de alimentação. Simulações do tipo Monte Carlo demonstraram a sensibilidade do projeto implementado à variabilidade. Considerando o impacto da variabilidade e a calibração proposta, as referências SBSCM e SBDF apresentaram um TC médio de 6.9 ppm/°C e 11 ppm/°C, respectivamente. O desempenho dos circuitos apresentou um baixo consumo de potência e coeficiente de temperatura com uma tensão de saída precisa, ocupando uma pequena área de silício.

Palavras-chave: projeto analógico CMOS, referências de tensão, alta precisão, calibração, baixo consumo.

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LIST OF ABBREVIATIONS AND ACRONYMS

AC	Alternating Current
ADC	Analog-to-Digital Converter
ASIC	Aplication Specific Integrated Circuit
BEVL	Base-Emitter Voltage Linearization
BGR	Bandgap Reference
BJT	Bipolar Junction Transistor
BVS	Battery Voltage Supervisor
CMOS	Complementary metal-oxide-semiconductor
CTAT	Complementary to Absolute Temperature
DAC	Digital-to-Analog Converter
DC	Direct Current
FoM	Figure of Merit
HOCCG	High-order Curvature Compensation Generator
IC	Integrated Circuit
IoT	Internet of Things
IMEC	Interuniversity Microelectronics Centre
LS	Line Sensitivity
MC	Monte Carlo
MOS	Metal-oxide-semiconductor
MOSFET	Metal-oxide-semiconductor Field Effect Transistor
MM	Mismatch
NMOS	N-channel MOSFET
NWE	Narrow-Width Effect
PC	Process
PMOS	P-channel MOSFET
PMU	Power Management Unit

PSR	Power Supply Rejection
PTAT	Proportional to Absolute Temperature
RF	Radio Frequency
RLSBCS	Resistorless Self-Biased Current Sources
RSCE	Reverse Short-Channel Effect
SBDF	Sub-bandgap with Unbalanced Differential Pair
SBSCM	Sub-bandgap with Self-Cascode MOSFETs
SCM	Self-Cascode MOSFET
SoC	System on Chip
TC	Temperature Coefficient
TSMC	Taiwan Semiconductor Manufacturing Company
UICM	Unified Current-Control Model
ULP	Ultra-low Power
VSC	Voltage Step Compensation
WI	Weak Inversion
WSN	Wireless Sensor Networks

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1 INTRODUCTION

In this chapter, we explore the importance and applications of voltage references in numerous electronic systems. First, the motivation for this work is defined as well as how the current performance requirements challenge the design of a voltage reference. Also, we discuss some necessities for circuits with low variability to increase the precision of a reference voltage. The concept of an ideal voltage reference is presented. Finally, we state the main objectives of this thesis and describe the work structure.

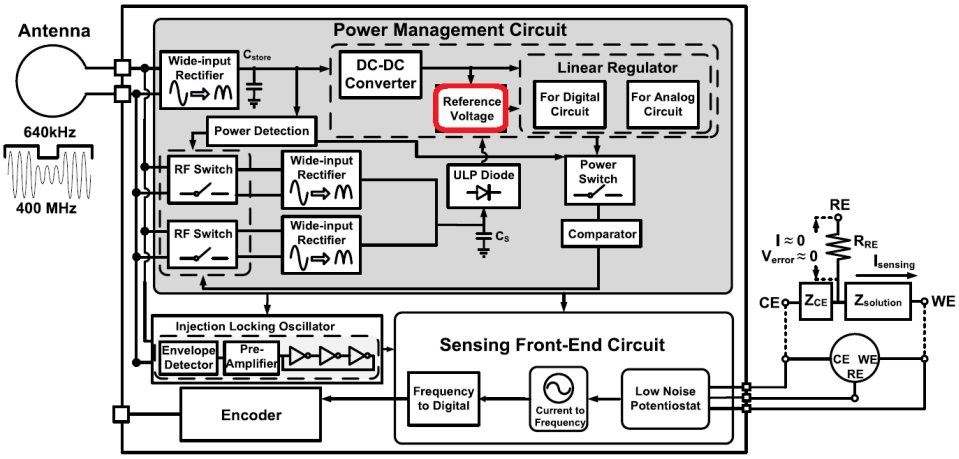
1.1 Motivation

The emergence of Internet of Things (IoT) systems and their advances increasingly demand low power, low cost, and high precision integrated circuits. Nowadays, the IoT market comprises implantable medical devices, wearable electronics, wireless sensors, and energy harvesting systems. As power consumption is a significant concern, IoT devices can be battery powered or include a self-powering solution such as a harvesting system.

Considering these market trends, a batteryless transceiver for wireless sensor networks (WSN) that allows a maintenance-free operation was developed by PAPOTTO et al. (2014). Another batteryless and self-powered device was proposed by HUANG et al. (2014), where a system on chip (SoC) was designed to monitor real-time multiple physiological parameters for a biomedical purpose. Moreover, for battery operated applications LEE et al. (2016) proposed a battery voltage supervisor (BVS) that monitors the energy transferred from the energy harvester to a battery and avoids permanent damage in the power system. Also, a power management unit (PMU) which can be connected to Li-ion batteries was presented by SHI et al. (2018). An application specific integrated circuit (ASIC) for power management of batteryless wireless sensors was implemented in FAN et al. (2018). This proposed ASIC integrates a power management system with a temperature sensor. Focusing on chemical sensing, TSAI et al. (2018) proposed a wirelessly-powered electrochemical readout interface circuit as shown in Fig. 1.1. The power management block delivers a stable power supply to the sensor considering the environmental variations that change RF power magnitude collected through a harvesting system. In wearable and mobile devices, sleep modes are commonly employed to avoid recharging the system battery several times a day. Therefore, an event-detector sensor is used in a watchdog circuit to wake up the device. For this purpose, HUSSAINI et al. (2019) proposed a readout circuit for capacitive touch sensors, as shown in Fig. 1.2. In CMOS image sensors, a temperature sensing for thermal management has been used to optimize the image sensor accuracy since the circuit can be thermal sensitive. Then, XIE; THEUWISSEN (2019) presented an on-chip smart temperature sensor for image sensors

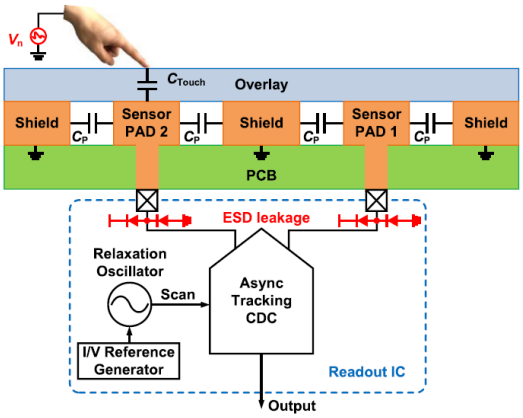
that can also be implemented for thermal sensing network.

Figure 1.1: Wireless electrochemical readout chip proposed by TSAI et al. (2018).



Source: TSAI et al. (2018).

Figure 1.2: System block diagram of the readout IC proposed by HUSSAINI et al. (2019).



Source: HUSSAINI et al. (2019).

In all these cited developments, a voltage reference circuit is needed. Therefore, it shows that voltage references are indispensable building blocks of many analog, mixed-signal, radio-frequency, and even digital circuits, providing references for on-chip power management systems, for smart sensors, for signal conditioning and signal measurement, or for build blocks such as analog to digital converters (ADCs) and digital to analog converters (DACs). Moreover, the reference voltage accuracy certainly determines the maximum achievable performance of its biased circuits, demonstrating that a high precision voltage reference is fundamental in a microelectronic system.

The reference voltage is required to be almost independent of supply voltage, temperature, and process variations. Therefore, considering the companies established priority to design reliable, low voltage and high precision integrated circuits (ICs), the development and improvements in voltage references blocks are extremely important nowadays. The voltage reference performance suffers from the limited controllability of the fabrication steps and the effect of variability on the reference signal sometimes is not discussed in

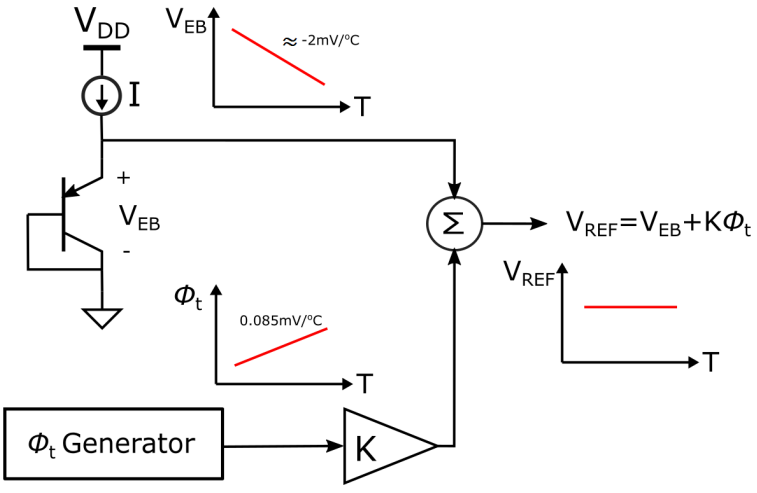
detail. However, it is relevant because these fabrication uncertainties produce significant variations in voltage reference circuits and degrade the reference accuracy. Therefore, it impacts on manufacturing cost by increasing trimming requirements, test time, circuit complexity, and decreasing yield. Then, the reduction or compensation of the fabrication variability impact on the reference performance is a great design challenge required to increase its precision and robustness.

There are several approaches to design voltage references in CMOS technology and throughout the years some solutions were proposed in order to improve the performances of these circuits. Amongst state-of-the-art circuits, one can find voltage references designed to meet the demanding low power consumption, low supply voltage and small area requirements. However, it is difficult to find strategies that combine low voltage and power consumption, low temperature sensitivity and low fabrication variability impact.

1.2 Ideal Voltage Reference

An ideal voltage reference is a circuit that generates an output voltage insensitive to variations in temperature, operating voltage, load current, and fabrication variability. The bandgap voltage reference (BGR) is a commonly applied voltage reference circuit, and its basic concept is shown in Fig. 1.3. Essentially, a voltage reference works based on the mutual compensation of temperature dependencies of two electrical quantities. The temperature-independence is achieved by adding a voltage proportional to absolute temperature (PTAT) with a voltage that is complementary to absolute temperature (CTAT). This bandgap voltage reference generates a reference voltage of approximately 1.23 V, that is approximately the extrapolated bandgap potential of Silicon.

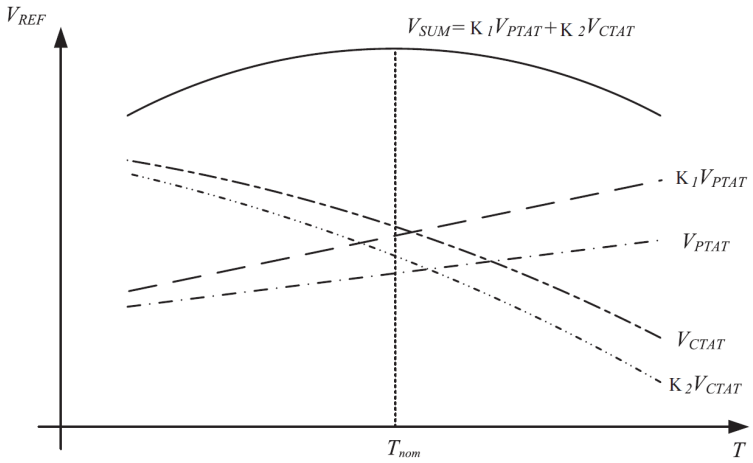
Figure 1.3: Basic concept of a bandgap voltage reference.



Source: Author.

The ideal behavior of a reference voltage is degraded by multiple sources of errors that affect the circuit. Hence, the nonlinear terms of the CTAT and PTAT voltages generate a curvature error resulting in a significant temperature coefficient, as shown in Fig. 1.4. Also, mismatches, offsets, second-order effects, supply voltages variations, and process deviations decrease the voltage reference accuracy.

Figure 1.4: Temperature variation of a voltage reference.



Source: KOK; TAM (2013).

1.3 Objectives

Considering the important role of voltage references for biasing IC blocks, this thesis primary purpose is to develop voltage reference circuits that present a high performance combining low power consumption and low fabrication variability to achieve the current precision and robustness requirements for microelectronics systems. This work also aims to study and analyze distinct circuit structures to propose performance improvements in the voltage reference design.

1.4 Organization

This work is organized as follows: a review on the evolution of integrated voltage references, followed by a chronological survey of recent developments, and a performance comparison between the state-of-art circuits are presented in Chapter 2. In Chapter 3, a detailed analysis of CTAT and PTAT voltage generators is discussed to explore the limitations of each studied structure. Then, Chapter 4 presents the proposed idea to develop two voltage references designs and a trimming technique to enhance circuit performance. Chapter 5 shows the post-layout simulation results of the proposed circuits and summarizes the performance of the voltage reference with other published works. Finally, Chapter 6 presents our main conclusions and explores future steps through this research topic.

2 INTEGRATED VOLTAGE REFERENCES EVOLUTION

This chapter presents a chronological review of earlier voltage references designs. Also, the main performance metrics of voltage reference circuits are presented. Then, we expose the most recent developments in the area and the last section evaluates recent advances.

2.1 Classic References

The concept of a bandgap reference was proposed by HILBIBER (1964) but the first practical implementation was presented by WIDLAR (1971). Widlar's reference did not use zener diode as previous discrete circuits employed (HILBIBER, 1964). Thus, the voltage reference proposed by Widlar implemented bipolar technology using the positive temperature coefficient of emitter-base differential voltage of two transistors operating at different emitter current densities, that is proportional to the thermal voltage ϕ_T, added to a negative temperature coefficient of a transistor emitter-base voltage. The idea is the mutual compensation of these temperature dependencies. Therefore, a simple weighted sum between these two voltages generates a low temperature coefficient reference voltage of 1.205 V (i.e., approximately the silicon bandgap voltage).

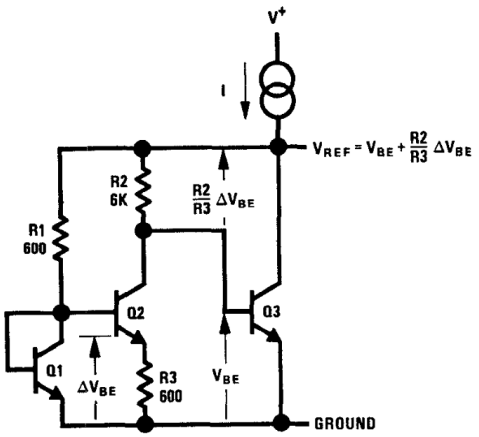
The BGR circuit is shown in Fig. 2.1. In this circuit Q_1 operates with a high current density, the current density of Q_2 is about 10 times lower, and the emitter-base voltage difference ΔV_{BE} between Q_1 and Q_2 appears across R_3. Q_3 is defined as a gain stage that regulates the output voltage formed by the Q_3 emitter-base voltage V_{BE} plus the drop across R_2, that is proportional to ΔV_{BE}, since currents in R_2 and R_3 are approximately the same.

Another topology for a bandgap voltage was proposed by KUIJK (1973), as shown in Fig. 2.2. This circuit uses two bipolar junction transistors (BJTs) connected as diodes and an operational amplifier. The emitter-base voltage difference ΔV_{BE} appears across R_3 and defines the emitter current I_2, which is proportional to absolute temperature. The BJT D_1 shows a proportional decrease with temperature. Thus, to provide a temperature independent output V_o the resistors values of R_1, R_2 and R_3 need to be adjusted.

One year later, BROKAW (1974) presented a BGR that uses two BJTs and collector-current sensing to establish the bandgap voltage. As shown in Fig. 2.3, the circuit regulates the transistors base voltage making the collector currents I_{C1} and I_{C2} match. The ΔV_{BE} between Q_1 and Q_2 appear across R_2 and current in R_1 is twice that in R_2. The voltage across R_1 varies directly with temperature. Then, this voltage is used to compensate the negative temperature coefficient of V_{BE}. The output voltage V_{OUT} is the sum of $V_{BE,Q1}$ and the voltage across R_1.

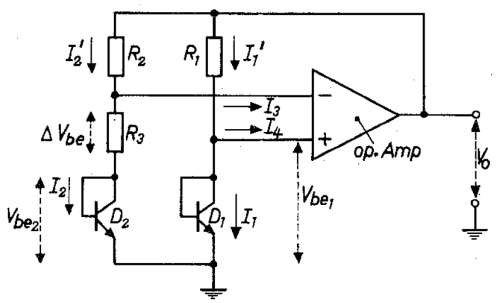
In 1977, Eric Vittoz established the weak inversion (WI) operation of MOS transistors

Figure 2.1: Schematic of the bandgap voltage reference proposed by WIDLAR (1971).



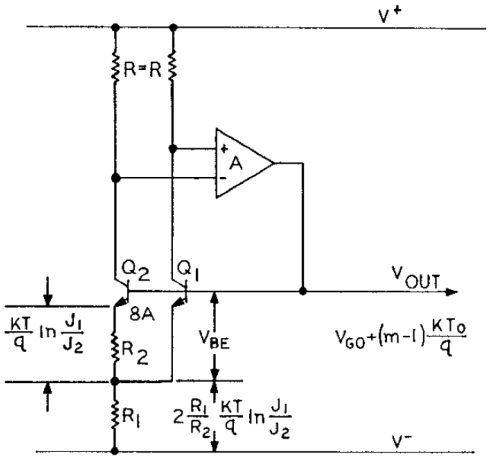
Source: WIDLAR (1971).

Figure 2.2: Topology of the bandgap voltage reference proposed by KUIJK (1973).



Source: KUIJK (1973).

Figure 2.3: Bandgap voltage reference reported in BROKAW (1974).

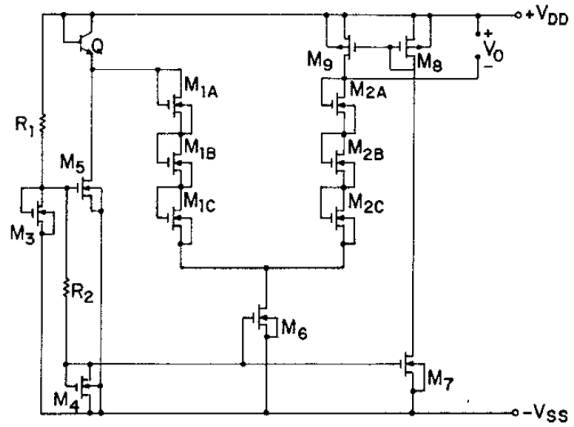


Source: BROKAW (1974).

for CMOS analog integrated circuits. The weak inversion (or subthreshold) operation was described by a model suitable for circuit design and also verified experimentally in VITTOZ; FELLRATH (1977). Circuits like current references, a quartz oscillator, and a bandpass amplifier were implemented using the WI operation and were able to prove the WI operation reliability.

The first CMOS voltage reference using WI operation was published by TSIVIDIS; ULMER (1978). In this work, a positive temperature coefficient was developed with a MOSFET unbalanced differential pair in WI. Then, the difference of the gate-to-source voltage (V_{GS}) of two MOS transistors (M_1 and M_2) in WI region and biased with different currents densities resulted in a PTAT voltage. For satisfactory temperature compensation, the PTAT voltage generators (M_1-M_2) were cascaded in series to achieve a higher voltage. The negative temperature coefficient voltage is generated through a bipolar transistor Q. The CTAT and PTAT voltages are added to form the output voltage V_O. The proposed bandgap voltage reference with transistors operating in WI is shown in Fig. 2.4.

Figure 2.4: Voltage reference proposed by TSIVIDIS; ULMER (1978).

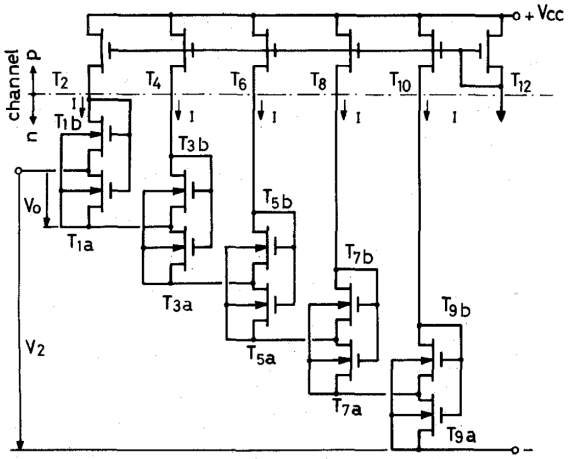


Source: TSIVIDIS; ULMER (1978).

Although TSIVIDIS; ULMER (1978) used transistors in WI, the need to sum up three gate-to-source voltages did not let the circuit operate with low supply voltages. Therefore, in 1979, Vittoz developed a novel PTAT voltage generator. This circuit is composed of stacked self-cascode PTAT voltage generators with transistors operating in WI as shown in Fig. 2.5. Employing this novel PTAT cell, a CMOS bandgap reference voltage was proposed (VITTOZ; NEYROUD, 1979). The reference voltage was generated by a base-emitter voltage of a bipolar transistor combined with the stacked self-cascode PTAT voltage generator. Results showed that the bandgap reference operated with a supply voltage as low as 1.3 V and a drain current below 1μA.

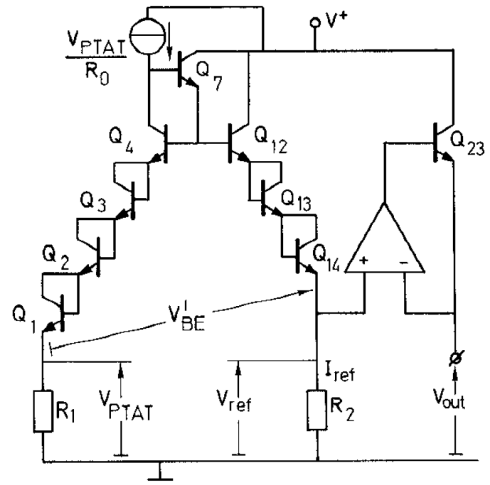
Seeking to reduce the temperature dependence of a bandgap reference output voltage, Meijer proposed a circuit configuration for compensating the thermal nonlinearity of the BJT base-emitter voltage (MEIJER; SCHMALE; ZALINGE, 1982). Meijer stated that for a BJT biased by a PTAT current, the thermal nonlinearity in V_{BE} is about 25% less than that of a BJT biased at a constant current. Then, the nonlinearity of V_{BE} is dependent on the bias current. So, the nonlinearity compensation can be optimized by properly choosing the bias current. The curvature-corrected bandgap circuit is shown in Fig. 2.6. In this topology the base-emitter junctions of Q_1-Q_4 are biased by a PTAT current and a temperature independent current (I_{ref}) biases the base-emitter junctions of Q_{12}-Q_{14}. Thus, subtracting V_{BE} of Q_{12}-Q_{14} from V_{BE} of Q_1-Q_4 resulted in a voltage V'_{BE} with a improved thermal linearity. The series resistor R_1 canceled the linear portion of V'_{BE} temperature dependence resulting in a reference voltage at the emitter of Q_{14}. The I_{ref} current is obtained when a temperature-independent resistor is employed for R_2. Finally, the output voltage (V_{out}) is regulated by the series transistor Q_{23} and the error amplifier.

Figure 2.5: Schematic of the PTAT cells proposed by VITTOZ; NEYROUD (1979).



Source: VITTOZ; NEYROUD (1979).

Figure 2.6: Bandgap voltage reference reported in MEIJER; SCHMALE; ZALINGE (1982).



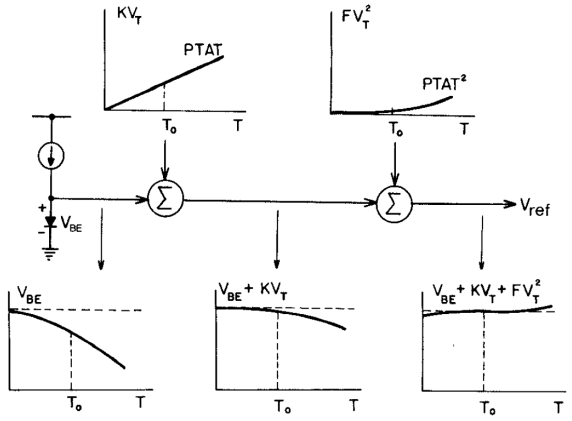
Source: MEIJER; SCHMALE; ZALINGE (1982).

In order to further improve the temperature stability of the bandgap reference, SONG; GRAY (1983) implemented a second-order temperature compensation. The proposed reference added linear and quadratic PTAT correction voltages to V_{BE}. Then, the reference voltage (V_{ref}) should drift only due to higher order temperature variations; this concept is shown in Fig. 2.7.

Through the years, the CMOS technology supply-voltage downscaling increased the demand for novel bandgap topologies to meet this requirement. Then, BANBA et al. (1999) proposed a sub-bandgap reference (Sub-BGR) circuit to operate with sub-1 V supply. As shown in Fig. 2.8, the reference voltage is determined mainly by the resistance ratio of R2, R3, and R4, indicating that this circuit can provide a wide range of output values. Therefore, the supply voltage for the proposed bandgap can be lowered according to V_{ref}, demonstrating the sub-1 V operation.

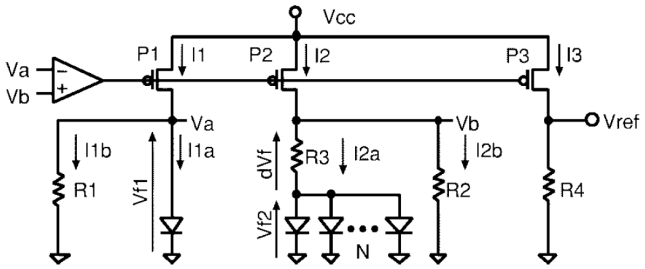
The use of resistors inevitably increases the chip size, and it also results in an increased cost of fabrication. To overcome these drawbacks, BUCK et al. (2002) presented a BGR without resistors. The proposed circuit is shown in Fig. 2.9. The difference between

Figure 2.7: Second-order temperature compensation proposed by SONG; GRAY (1983).



Source: SONG; GRAY (1983).

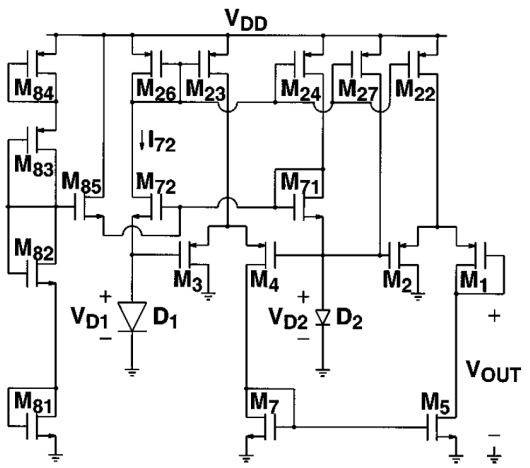
Figure 2.8: Sub-bandgap voltage reference reported in BANBA et al. (1999).



Source: BANBA et al. (1999).

the forward bias voltages across two diodes ($\Delta V_D = V_{D2} - V_{D1}$) is multiplied by a gain obtained by using ratioed transistors with the inverse function technique (TORRANCE; VISWANATHAN; HANSON, 1985) to generate the PTAT term. This term is compensated by the CTAT behavior of the diode D1, resulting in an output voltage that is equal to a reference voltage.

Figure 2.9: Schematic of the resistorless bandgap voltage reference proposed by BUCK et al. (2002).



Source: BUCK et al. (2002).

2.2 Performance and Metrics

The performance of a voltage reference circuit is quantified by many specification parameters, and one of the most important is the temperature coefficient (TC). Considering that the circuit physical characteristics vary with the temperature, the TC is a fundamental parameter that measures the maximum sensitivity of the reference voltage over a defined temperature range, and it is usually given in ppm/°C. The TC can be expressed as (GRAY; MEYER, 1993)

$$TC = \frac{V_{REFmax} - V_{REFmin}}{(T_{max} - T_{min})V_{REF27^oC}} \times 10^6 \tag{2.1}$$

where V_{REFmax} and V_{REFmin} are the maximum and minimum reference voltage values within the operating temperature range ($T_{max} - T_{min}$) and V_{REF27^oC} is the reference voltage at 27 °C.

Another relevant metric is the reference voltage sensitivity on supply voltage variations. This dependency is known as Line Sensitivity (LS) if related only to DC, and its unit is %/V. The LS can be written as

$$LS = \frac{\Delta V_{REF}}{\Delta V_{DD} \times V_{REF\mu}} \times 100\% \tag{2.2}$$

where ΔV_{REF} is the difference of the reference voltage within the supply voltage (V_{DD}) range considered, ΔV_{DD} is the operating V_{DD} range and $V_{REF\mu}$ is the mean value of the reference voltage within the ΔV_{DD}.

Power Supply Rejection (PSR) is the circuit ability to reject AC interferences coming from the supply voltage and measured in dB over a defined frequency range. The PSR is defined as

$$PSR = 20\ log\left(\frac{V_{REF,AC}(f)}{V_{DD,AC}(f)}\right) \tag{2.3}$$

where $V_{REF,AC}(f)$ is an AC coupled reference voltage at the output of the voltage reference circuit and $V_{DD,AC}(f)$ is the power supply with incoming noise at a frequency f (KOK; TAM, 2013).

Variability impacts the circuit performance and can be classified by two kinds of variations: process and mismatch. Process variation is defined as an uncertainty that affects similar devices of a circuit in the same way and then does not produce mismatch among these devices. It impacts only the performance parameters that depend on the absolute value of physical quantities. Mismatch variations can be explained as an uncertainty that affects each similar device of a circuit differently and then produces mismatch among these devices. It also impacts performance parameters that depend on the ratio of physical quantities.

Thus, the reference voltage variation due to fabrication variability or variability coefficient can be quantified by the standard deviation and mean value ratio (σ/μ) and is given in %. The variability also impacts the TC because, within several samples of voltage references, different temperature sensitivities are found. Hence, it is essential to evaluate the minimum, average, and maximum TC. Furthermore, classical specifications are important, such as: silicon area, power consumption, and minimum supply voltage.

A Figure of Merit (FoM) can be used to provide a comparative result that represents the overall performance of a voltage reference. Prof. Willy Sansen proposed a FoM that considers the main performance parameters, such as temperature range, TC, power

consumption, and silicon area, and can be defined as follows (SANSEN, 2015)

$$FoM_{Sansen} = \frac{(T_{max} - T_{min})^2}{TC.Power.Area} . \frac{1}{10^{16}} \tag{2.4}$$

However, this FoM does not consider the voltage reference deviation due to the variability impact. Additionally, the power consumption and silicon area have the same emphasis of TC on (2.4). Thus, for a better evaluation of a voltage reference considering high precision applications, we propose a similar FoM, expressed in (2.5), where $V_{REF}\ \sigma/\mu$ parameter is the reference voltage relative deviation considering fabrication variability.

$$FoM = \frac{T_{max} - T_{min}}{(TC)^2.Power.Area.(V_{REF}\ \sigma/\mu)^2} . \frac{1}{10^{23}} \tag{2.5}$$

In this new FoM, the TC and $V_{REF}\ \sigma/\mu$ are squared because theses parameters are a priority when generating an accurate reference voltage. The power consumption and silicon area are still present to meet the demanding low power consumption and small area requirements. The temperature range of the voltage reference is also a relevant parameter that is considered in this FoM. The division by 10^{23} was added for better visualization of the FoM values.

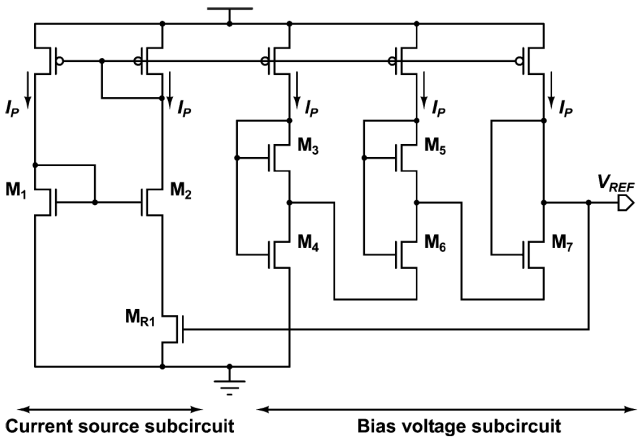
All these metrics are used to analyze voltage references designs and to evaluate the recent circuits presented in the next section.

2.3 Recent Developments on CMOS Voltage References

2.3.1 Self Cascode Cells and Diode-Connected NMOS

The circuit in UENO et al. (2009) consists of subthreshold MOSFETs and uses no resistors. The schematic of the voltage reference is shown in Fig. 2.10.

Figure 2.10: Voltage reference proposed by UENO et al. (2009).



Source: UENO et al. (2009).

A current source circuit generates a current I_P. Through a current mirror, the two self-cascode PTAT generators and the diode-connected NMOS are biased by I_P. The gate-source voltage V_{GS1} is equal to the sum of gate-source voltage V_{GS2}, and drain-source voltage V_{DSR1}. The drain-source voltage V_{DSR1} can be written as

$$V_{DSR1} = n\phi_T ln(\frac{S_2}{S_1}) \tag{2.6}$$

where n is the subthreshold slope factor, ϕ_T is the thermal voltage and S is the aspect ratio (W/L).

The bias current I_P in M1 and M2 are equal and is given by

$$I_P = S_{R1}\mu C_{OX}(V_{REF} - V_{TH})n\phi_T ln(\frac{S_2}{S_1}) \tag{2.7}$$

where μ is the carrier mobility, C_{OX} is the gate-oxide capacitance and V_{TH} is the threshold voltage of a MOSFET.

The gate-source voltages (V_{GS3}-V_{GS7}) form a closed loop and the reference voltage V_{REF} is given by

$$V_{REF} = V_{GS4} - V_{GS6} - V_{GS5} + V_{GS7} = V_{TH} + n\phi_T ln(\frac{3I_P}{S_4 I_0}) + n\phi_T ln(\frac{2S_3 S_5}{S_6 S_7}) \tag{2.8}$$

where $I_0 = \mu C_{OX}(n-1)\phi_T^2$.

The threshold voltage has a CTAT behavior and ϕ_T a PTAT behavior. Thus, from expression (2.8), the reference voltage can be obtained by adjusting the transistors ratios. A zero TC can be achieved by setting the aspect ratios S_i considering $\partial V_{REF}/\partial T = 0$. The authors stated that the generated reference voltage equals to the threshold voltage of MOSFETs at 0 K (V_{TH0}). The current I_P can be rewritten as

$$I_P = S_{R1}\mu C_{OX} kn\phi_T ln(\frac{S_2}{S_1}) \tag{2.9}$$

where k is the TC of V_{TH0}. This expression (2.9) demonstrate that the current is independent of V_{TH0}. The parameter k suffer less impact of process variability than V_{TH0}. Thus, I_P is less affected by process variations. However, since $V_{REF} = V_{TH0}$ the reference voltage is less accurate due to process variation. The authors designed the circuit using large values for W and L and appropriate layout techniques to reduce the mismatch impact, but the reference will still significantly deviate due to process variability.

The TC of the reference voltage depends on channel doping concentration (N_A), and this concentration is process-dependent. Although TC can change with process variation, this change is minimal because the authors calculated that TC is a logarithmic function of N_A. Moreover, computer simulations showed that the threshold voltage changes by $\pm 20\%$ with N_A and its TC by $\pm 2\%$

The authors fabricated the proposed circuit in a standard 0.35 μm CMOS process and measured 17 samples from the same wafer. Table 2.1 presents the performance summary of the prototype chip. Analyzing the measured results, one can confirm the impact of process variability in the reference voltage. Therefore, a trimming scheme can be useful to this topology to correct its deviation due to variability. It is also relevant to avoid an output voltage that depends on the threshold voltage of transistors due to its process variations.

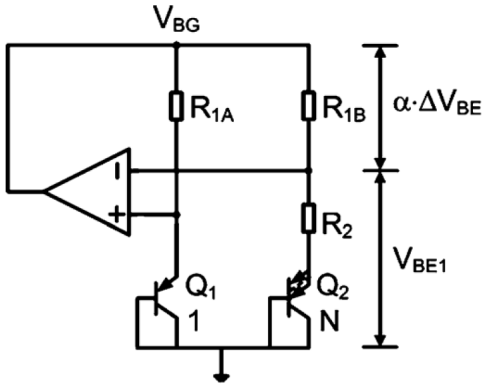
2.3.2 Bandgap Reference with a Single Trim

GE et al. (2011) proposed a BGR with a trimming circuit to compensate process variations and achieve an accurate reference. First, the authors studied error sources in a typical bandgap topology (KUIJK, 1973), as shown in Fig. 2.11. The nonlinear temperature dependence of the BJT base-emitter voltage V_{BE}, the opamp offset, and process variation of V_{BE} and V_{BE} difference (ΔV_{BE}) are factors that degrade the precision of a voltage reference.

Table 2.1: Reported Results Summary in UENO et al. (2009).

Specification	This work
Process	0.35 μm CMOS
Temp. Range	-20 - 80 °C
Supply Voltage	1.4 - 3 V
V_{REF}	745 mV
V_{REF} σ/μ	0.87 %
TC_{avg}	15 ppm/°C
TC_{min}	7 ppm/°C
TC_{max}	45 ppm/°C
Line Sensitivity	20 ppm/V
PSRR	-45dB(@100 Hz)
Power Consumption	0.3 μW(@1.4 V)
Silicon Area	0.055 mm^2

Figure 2.11: Typical bandgap voltage reference reported in KUIJK (1973).



Source: GE et al. (2011).

The V_{BE} is determined by its collector current I_C and saturation current I_S. Considering that I_S deviates from its nominal value, V_{BE} can be written as

$$V_{BE} = \phi_T ln \frac{I_C}{I_S + \Delta I_S} \tag{2.10}$$

where ϕ_T is the thermal voltage and ΔI_S the deviation of I_S. Therefore, the V_{BE} spread due to the saturation current spread is PTAT and can be removed by a PTAT trim. The collector current I_C can also deviate as a result of resistance variations of R_1 and R_2. Considering the resistance spread as a fractional deviation δ_R, V_{BE} can be rewritten as

$$V_{BE} = \phi_T ln \frac{\frac{I_C}{1+\delta_R}}{I_S}. \tag{2.11}$$

Assuming δ_R is temperature independent, expression (2.11) demonstrate that this V_{BE} variation is also PTAT. Finally, BJT current gain β_F impact V_{BE} and if β_F deviates from its nominal value, V_{BE} is given by

$$V_{BE} = \phi_T ln(\frac{I_E}{I_S} \frac{\beta_F + \Delta\beta_F}{1 + \beta_F + \Delta\beta_F}) \tag{2.12}$$

where I_E is the emitter current of the BJT, and $\Delta\beta_F$ is the deviation of β_F. All these PTAT deviations can be reduced by a single room temperature trim.

The PTAT term in a BGR is generated by two BJTs biased at different current densities and ΔV_{BE} can be written as

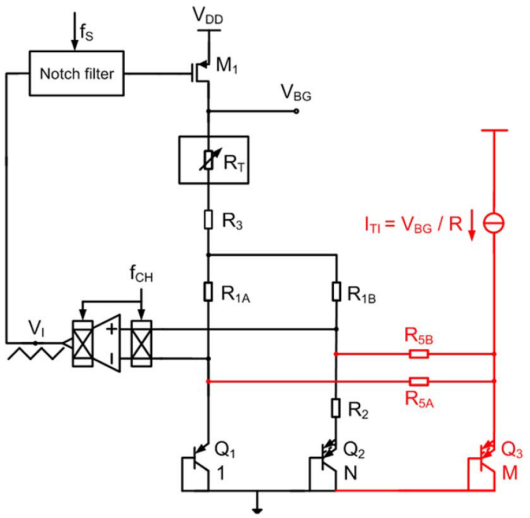
$$\Delta V_{BE} = \frac{R_1}{R_2}\phi_T ln(\frac{I_{C1}}{I_{C2}}N) \tag{2.13}$$

where I_{C1} and I_{C2} are collector currents of Q_1 and Q_2. Then, the temperature drift of these collector currents will degrade the bandgap voltage (V_{BG}) accuracy. To overcome this error, a matched resistor based topology was employed. The authors stated that the resistor mismatch is more stable over temperature.

The offset of an opamp is typically non-PTAT; therefore, it is difficult to reduce with a PTAT trim. Thus, the offset can be removed by a chopping technique. This chopping is better than the auto-zeroing technique in terms of noise performance and because the opamp output is continuously available. The curvature correction of V_{BE} follows MEIJER; SCHMALE; ZALINGE (1982).

The BGR is shown in Fig. 2.12, and it was fabricated in a standard 0.16 μm CMOS process and measured 61 samples from the two batches. Table 2.2 summarizes the performance of the proposed bandgap reference. This circuit achieved excellent results in terms of variability. However, the main drawback is the power dissipation. Such a high power consumption is due to the sophisticated strategies that were used to reduce variability deviations.

Figure 2.12: Schematic of the bandgap voltage reference proposed by GE et al. (2011).



Source: GE et al. (2011).

2.3.3 Bandgap with Cascaded Differential Pairs

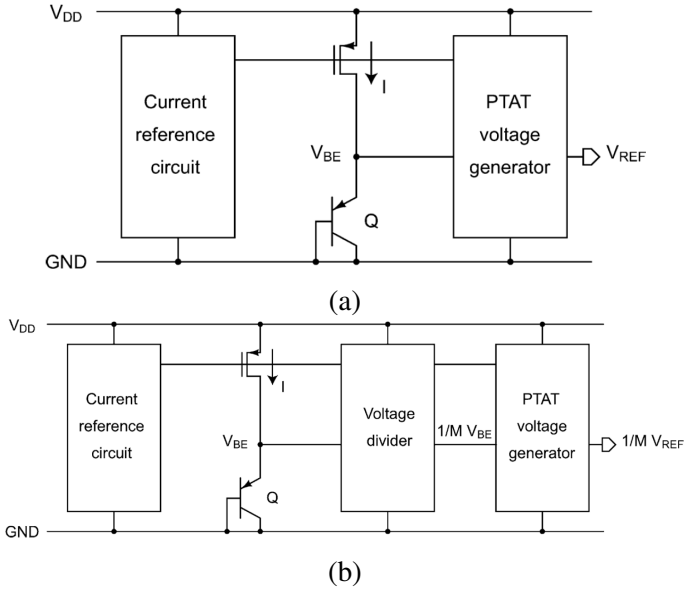
All-MOSFETs voltage references usually operate with low power consumption because of the WI operation of transistors. However, these circuits provide reference voltages based on the threshold voltage of MOSFETs. Classical bandgap topologies use BJT and resistors to generate a PTAT voltage, which impact on power consumption and silicon area. Then, OSAKI et al. (2013) implemented a topology employing a BJT to generate the CTAT voltage and cascaded MOSFETs unbalanced differential pairs as the PTAT term. The authors proposed a resistorless bandgap and a sub-bandgap circuit, and its architectures are shown in Fig. 2.13.

Table 2.2: Performance Summary GE et al. (2011).

Specification	This work
Process	0.16 μm CMOS
Temp. Range	-40 - 125 °C
Supply Voltage	1.8 V
V_{REF}	1.0875 V
V_{REF} σ/μ	0.05^a %
TC_{min}	5^a ppm/°C
TC_{max}	12^a ppm/°C
PSRR	74dB(@DC)
Power Consumption	99 μW
Silicon Area	0.12 mm^2

^{a}Trimmed;

Figure 2.13: Architectures of proposed (a) BGR and (b) sub-BGR circuits proposed by OSAKI et al. (2013).



Source: OSAKI et al. (2013).

The PTAT voltage is generated through a differential pair with a current mirror, illustrated in Fig. 2.14. Considering MOSFETs in WI operation, their gate-to-gate voltage V_{GG} can be expressed as

$$V_{GG} = V_{GS,D2} - V_{GS,D1} = n\phi_T ln(\frac{S_{D1}S_{M2}}{S_{D2}S_{M1}}) \tag{2.14}$$

where $V_{GS,D1}$ and $V_{GS,D2}$ are gate-source voltages of M_{D1} and M_{D2}, ϕ_T is the thermal voltage and S is the aspect ratio (W/L), and n is the subthreshold slope factor. Thus, the PTAT term can be adjusted by the aspect ratios of transistors M_{D1}, M_{D2}, M_{M1} and M_{M2}. To achieve a PTAT voltage that is able to cancel the V_{BE} temperature behavior, the differential pairs can be cascaded, resulting in a total gate-to-gate voltage V_{GG} given by

$$\sum_{i=1}^{N} V_{GG,i} = \sum_{i=1}^{N} n\phi_T ln(\frac{S_{D2i-1}S_{M2i}}{S_{D2i}S_{M2i-1}}) \tag{2.15}$$

where N is the number of differential pairs. So, the output voltage V_{REF} can be written as

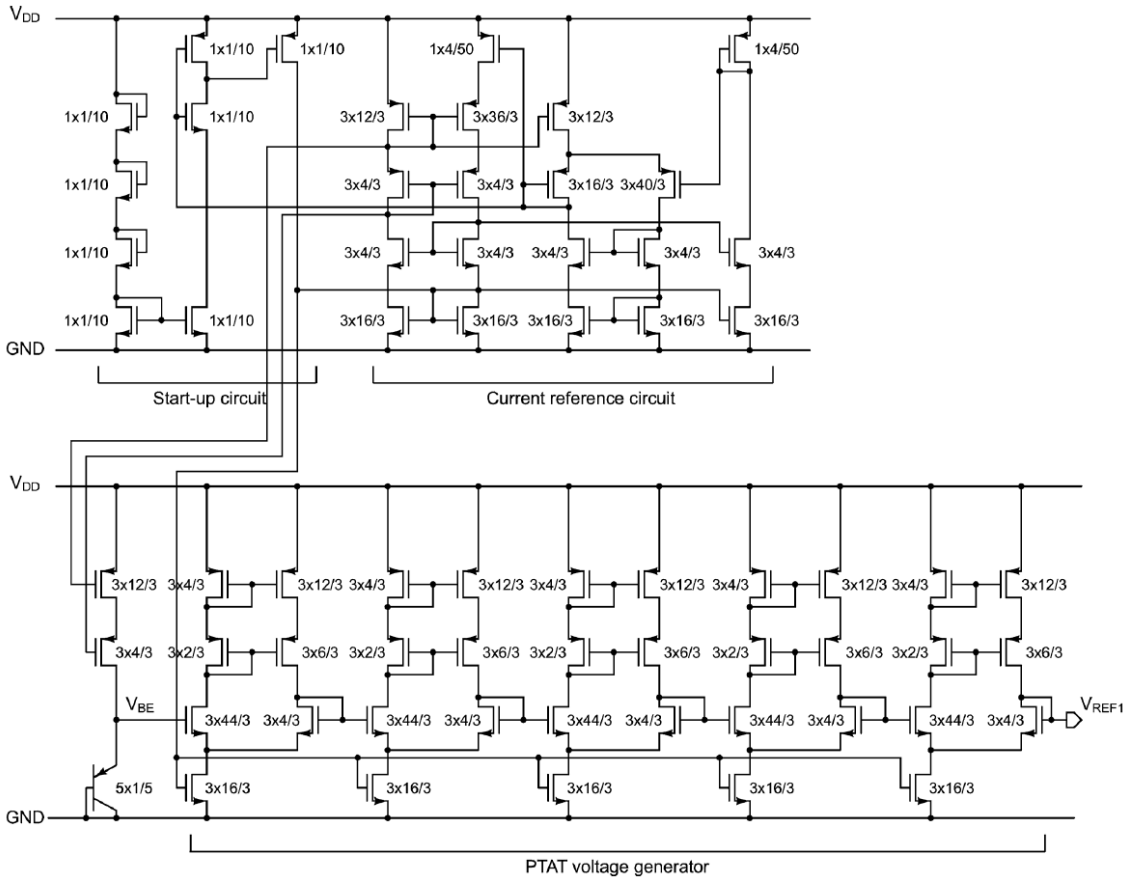
$$V_{REF} = V_{BE} + \sum_{i=1}^{N} n\phi_T ln(\frac{S_{D2i-1}S_{M2i}}{S_{D2i}S_{M2i-1}}) \tag{2.16}$$

and from expression 2.16 it is possible to achieve the bandgap voltage of the silicon by appropriate choice of N and aspect ratio os transistors.

A nano-ampere current reference circuit was used to bias the BJT and the PTAT term through current mirrors. This bias current also impacts on V_{BE} deviations. Then, it was chosen a reference current that generates a bias current tolerant with threshold voltage variations.

The schematic of the BGR is illustrated in Fig. 2.14, and it was fabricated in a standard 0.18 μm CMOS process and measured 9 samples from the same wafer. Table 2.3 summarizes the performance of the proposed reference. This topology obtained a good performance in terms of power consumption. Considering that V_{REF} does not depend on the threshold voltage and the bias current circuit was chosen to reduce the deviation on V_{BE} it was expected better results in terms of V_{REF} variability. Then, using a different current reference and employing larger transistors to reduce the mismatch could improve this performance. Moreover, the TC is not acceptable for a precision bandgap. Thus, a curvature compensation technique or a trimming strategy can be used to reduce this temperature dependence.

Figure 2.14: Bandgap voltage reference proposed by OSAKI et al. (2013).



Source: OSAKI et al. (2013).

Table 2.3: Measured Results Summary OSAKI et al. (2013).

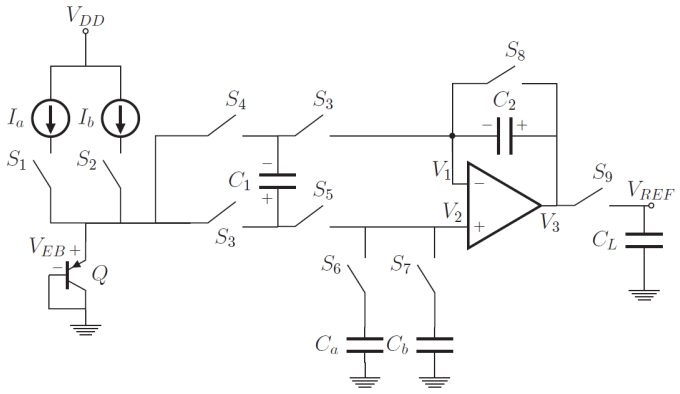
Specification	BGR	Sub-BGR
Process	0.18 μm CMOS	0.18 μm CMOS
Temp. Range	-40 - 120 °C	-40 - 120 °C
Supply Voltage	1.2 - 1.8 V	0.7 - 1.8 V
V_{REF}	1.09 V	0.548 V
V_{REF} σ/μ	0.737 %	1.05 %
TC_{avg}	147 ppm/°C	114 ppm/°C
PSRR	-62dB(@100Hz)	-56dB(@100Hz)
Power Consumption	0.1 μW	0.0525μW
Silicon Area	0.0294 mm^2	0.0246 mm^2

2.3.4 A Switched-Capacitor Bandgap

A novel switched-capacitor bandgap voltage reference was proposed by KLIMACH et al. (2013). In general, switched-capacitor bandgap references were used to remove the opamp offset voltage V_{OS} (CHEN; LI; CHENG, 2012). However, since capacitors present reduced variability aspects such as process spread and device mismatches, it is possible to improve the bandgap variability performance by employing these devices to generate the PTAT and CTAT voltages.

The topology is shown in Fig. 2.15, and it uses a single current mirror, a single BJT, and switched capacitors. The concept in this circuit it that the base-emitter voltage of a BJT that has a CTAT behavior is added with a difference of the junction voltages ΔV_{BE} of the same BJT biased by two different current densities. The switched-capacitors generate V_{BE} and ΔV_{BE}.

Figure 2.15: Schematic of the switched bandgap reference proposed by KLIMACH et al. (2013).



Source: KLIMACH et al. (2013).

The reference voltage is generated after 5 phases of switching. Considering a small mismatch in the current source, thus, $I_a = I + \delta I$ and $I_b = I - \delta I$. In phase 1, S_1 S_3, S_5, S_6, and S_8 are closed and the capacitor C_a is charged resulting in $V_{C_a} = V_{EB}(I_a)$. In phase 2, S_2 S_3, S_5, S_7, and S_8 are closed and the capacitor C_b is charged resulting in $V_{C_b} = V_{EB}(I_b)$. Phase 3 calculates the average of C_a and C_b by closing S_1 S_2, S_3, S_6, S_7 and S_8. Then, $V_2 = (V_{C_a} + V_{C_b})/2$ and $V_{C_1} = V_{EB}(2I) - V_{EB}(I) + V_{OS}$ in phase 3. Phase 4 represents the charge transferring from C_1 to C_2 by closing S_1 S_2, S_3, and S_5. So, $V_{C_2} = C_1/C_2(V_{EB}(2I) - V_{EB}(I))$ and V_{OS} remains in C_1. Finally, in phase 5 S_1 S_2, S_4, S_5, and S_9 are closed and C_1 is connected in series with V_2 and $V_{EB}(2I)$, removing

V_{OS} and defining the reference voltage as

$$V_{REF} = V_{EB}(2I) + (C_1/C_2)(kT/q)\ ln(2) \tag{2.17}$$

where k is the boltzman constant, T is the absolute temperature and q is the electron charge.

The circuit was simulated using 0.18 μm CMOS process. For the simulation, the ideal current sources were replaced by self-biased current reference (CAMACHO-GALEANO; GALUP-MONTORO; SCHNEIDER, 2005). To analyze the variability impact on V_{REF}, a Monte Carlo run of 200 samples combining process variation and mismatch was simulated. Therefore, Table 2.4 summarizes the characteristics of the proposed switched-capacitor bandgap. This solution presented a good performance in terms of V_{REF} variability and TC. The use of capacitors instead of resistors proved to be an interesting choice to overcome variability deviations. Interesting strategies such as using only one BJT, the reduction of current mirror mismatch, and the V_{OS} cancellation are relevant too. A significant concern is the power consumption of this topology. Moreover, line sensitivity and PSR results were not presented, and the circuit was not fabricated.

Table 2.4: Simulated Results Summary KLIMACH et al. (2013).

Specification	This work
Process	0.18 μm CMOS
Temp. Range	-40 - 85 °C
Supply Voltage	1.8 V
V_{REF}	1.29 V
V_{REF} σ/μ	0.26 %
TC_{avg}	14.51 ppm/°C
TC_{max}	28.8 ppm/°C
Power Consumption	77.4 μW
Silicon Area	0.015 mm^2

2.3.5 Voltage Reference with High-Slope PTAT Generator

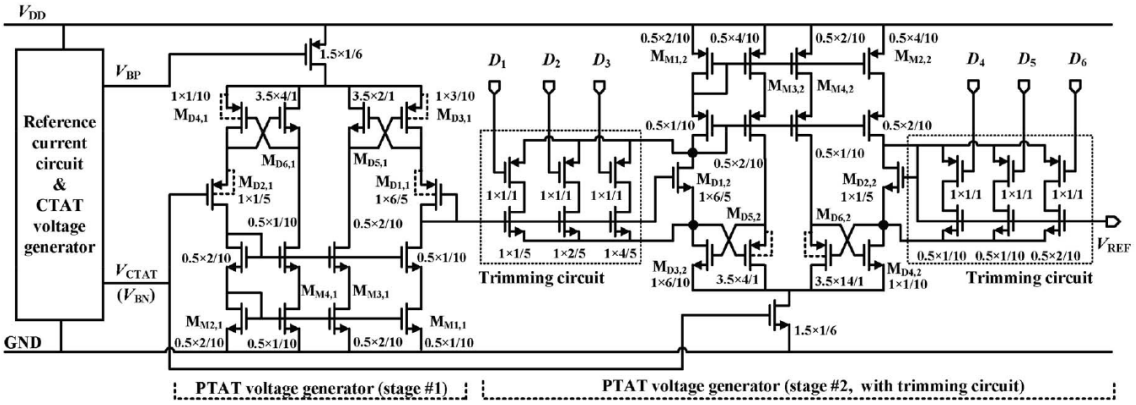
As reported in OSAKI et al. (2013), the slope of the PTAT voltage generated by a single cell is not sufficient to cancel the slope of the CTAT voltage; then, five cascaded stages were required in the proposed BGR. These cascaded PTAT generators increase silicon area and power dissipation. Therefore, the main contribution of ZHANG et al. (2018) is a MOSFET-only voltage reference with a novel PTAT voltage generator. In this topology, only two stages of PTAT generators are used since this architecture enhanced the slope of the PTAT output voltage, as illustrated in Fig. 2.16.

A nano-ampere current reference biases the PTAT cell, and the bias circuit generates the CTAT voltage to reduce chip area and power consumption. Fig. 2.17 shows that the gate-source voltage V_{GS} of M_{N2} is used as the CTAT voltage V_{CTAT}. Thus, V_{CTAT} can be expressed as

$$V_{CTAT} = V_{TH} + n\phi_T ln\left[\frac{I_{P0}T^{(m_N - m_P)}}{S_{N2}\mu_{n0}T_0^{m_N}C_{OX}(n-1)(k_B/q)^2}\right] \tag{2.18}$$

where V_{TH} is the MOSFET threshold voltage, n is the subthreshold slope factor, ϕ_T is the thermal voltage, I_{P0} is a current independent of temperature, T is the absolute temperature, m_N is the temperature exponent of electron mobility, m_P is the temperature

Figure 2.16: Voltage reference topology proposed by ZHANG et al. (2018).



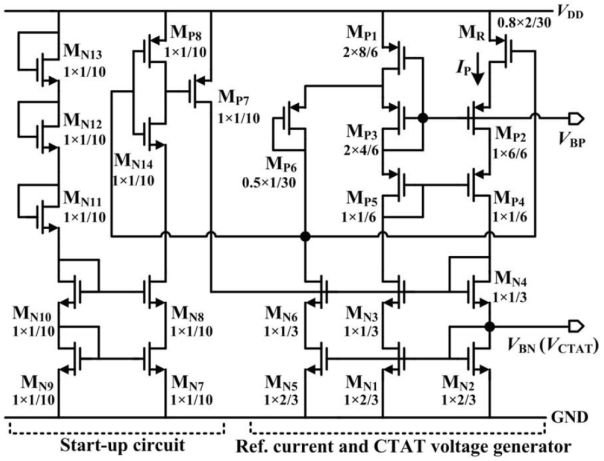
Source: ZHANG et al. (2018).

exponent of hole mobility, S is the aspect ratio (W/L) of the MOSFET, μ_n is the mobility at T_0, C_{OX} is the gate-oxide capacitance, k_B is the Boltzmann constant, and q is the elementary charge. The term in the logarithm operator in 2.18 is assumed to be constant independent of temperature. Then, the TC of V_{CTAT} can be obtained by its derivative and can be written as

$$TC_{V_{CTAT}} = \frac{\partial V_{CTAT}}{\partial T} = TC_{V_{TH}} + n\frac{k_B}{q} ln\left[\frac{I_{P0}}{S_{N2}\mu_{n0}T_0^{m_N}C_{OX}(n-1)(k_B/q)^2}\right] \quad (2.19)$$

where $TC_{V_{TH}}$ is the TC of V_{TH}. The absolute value of the second term in 2.19 is much less than $TC_{V_{TH}}$. So, simulated results showed that V_{CTAT} has a TC of -1.3 mV/°C.

Figure 2.17: Start-up circuit, reference current and CTAT generator reported in ZHANG et al. (2018).



Source: ZHANG et al. (2018).

As seen in Fig. 2.16, the PTAT voltage generator is an asymmetrical differential cell with two additional cross-coupled NMOS/PMOS pairs ($M_{D3,2}$/$M_{D5,2}$ and $M_{D4,2}$/$M_{6,2}$). The sizes of the transistors in this cell determine the current of each branch. The gate-to-gate voltage V_{GG} of this cell can be written as

$$V_{GG} = (V_{GS,D2} + V_{GS,D4} - |V_{GS,D6}|) - (V_{GS,D1} + V_{GS,D3} - |V_{GS,D5}|) \quad (2.20)$$

assuming a small V_{TH} difference between M_{D1} and M_{D2} caused by the body effect and neglecting the difference in n of PMOS and NMOS, V_{GG} can be rewritten as

$$V_{GG} = n\phi_T ln\left(\frac{S_{D1}S_{M2}}{S_{D2}S_{M1}}\frac{S_{D3}S_{M2}}{S_{D4}S_{M1}}\frac{S_{D6}S_{M3}}{S_{D5}S_{M4}}\right) + \Delta V_{TH,D21} \tag{2.21}$$

where $\Delta V_{TH,D21} = V_{TH,D2} - V_{TH,D1}$. The multiplication factors inside the logarithm term in (2.21) can provide a higher PTAT slope with a proper choice of aspect ratios. The second stage of the PTAT voltage generator presented in Fig. 2.16 achieved a PTAT slope of 0.82 mV/°C, showing an almost twice slope improvement compared to OSAKI et al. (2013), while consuming less power and area.

The proposed circuit was fabricated in a standard 0.18 μm CMOS process and measured 63 samples from the same wafer. Table 2.5 summarizes the performance of the circuit. This topology obtained a good performance in terms of power consumption and area. However, from expressions (2.18) and (2.21), V_{CTAT} and V_{PTAT} depend on the threshold voltage. Therefore, process variations could cause variations in the PTAT and CTAT voltages slopes, degrading the temperature sensitivity. Also, mismatch between the differential pairs is a concern. A trimming scheme is employed to reduce these variations, but it has little impact on the performances. Then, using a CTAT generator that does not depend on the V_{TH} and designing a better trimming circuit could be a solution to improve the circuit immunity to variability.

Table 2.5: Reported Results Summary in ZHANG et al. (2018).

Specification	This work
Process	0.18 μm CMOS
Temp. Range	-40 - 125 °C
Supply Voltage	1 - 1.8 V
V_{REF}	756 mV
V_{REF} σ/μ	0.95 %
TC_{avg}	49.6 ppm/°C
Line Sensitivity	0.524 %/V
PSRR	-52dB(@100 Hz)
Power Consumption	23 nW(@1 V)
Silicon Area	0.0162 mm^2

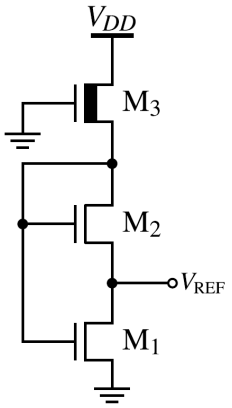
2.3.6 A 3-Transistor Voltage Reference

Ultra-low power (ULP) systems are emerging to comply with the Internet of Things (IoT) market. Therefore, OLIVEIRA et al. (2018) proposed an ULP voltage reference using only 3 transistors based on the self-cascode MOSFET (SCM). The schematic of the 3T voltage reference is illustrated in Fig. 2.18.

Transistors M_1 and M_2 compose the SCM and are biased by an NMOS transistor acting as a current source. Both transistors of the SCM operate in the subthreshold region, and their difference between gate-to-source voltages V_{GS} defines the reference voltage V_{REF}. According to the Unified Current-Control Model (UICM) (SCHNEIDER; GALUP-MONTORO, 2010), the drain current of a long channel NMOS transistor in WI can be expressed as

$$I_D = 2eI_S exp\left(\frac{V_G - V_{TH}}{n\phi_T}\right)\left[exp\left(\frac{-V_S}{\phi_T}\right) - exp\left(\frac{-V_D}{\phi_T}\right)\right] \tag{2.22}$$

Figure 2.18: Voltage reference proposed by OLIVEIRA et al. (2018).



Source: OLIVEIRA et al. (2018).

where e is the Euler's number, $I_S = I_{SQ}S$, S is the transistor aspect ratio (W/L), and W and L are the channel width and length, respectively. $I_{SQ} = \mu C'_{ox} n\phi_T^2/2$ is the sheet normalization current where μ represents the carrier mobility, n the subthreshold slope factor, C'_{ox} is the gate capacitance per unit area, and ϕ_T is the thermal voltage. V_G, V_S, and V_D are the gate, source and drain voltages, respectively, all referred to the bulk, and V_{TH} is the geometry-dependent threshold voltage.

Since $I_{D1} = I_{D2}$ and the authors are using the same type of transistors it is possible to assume $n_1 = n_2$. Then, an expression for V_{REF} can be written as

$$V_{REF} = \phi_T ln\left[1 + \frac{I_{S2}}{I_{S1}} exp\left(\frac{V_{TH1} - V_{TH2}}{n\phi_T}\right)\right] \tag{2.23}$$

Solving $\partial V_{REF}/\partial T = 0$, an S_2/S_1 value can be found for temperature compensation. Thus, the temperature compensated V_{REF} can be rewritten as

$$V_{REF} = \frac{V_{TH1}(T_0) - V_{TH2}(T_0)}{n} \tag{2.24}$$

where T_0 is the reference temperature. Thereby, the reference voltage is generated through the V_{TH} difference of M_1 and M_2. To achieve $V_{TH1} > V_{TH2}$, reverse short-channel effect (RSCE), and narrow-width effect (NWE) are explored.

The proposed voltage reference was fabricated in a standard 0.13 μm CMOS process. A total of 5 chips from the same wafer were package in ceramic and measured. Table 2.6 summarizes the performance of the circuit. The results presented excellent performances for power consumption and silicon area. Nevertheless, the output voltage dependency on the transistor threshold voltage impacts the accuracy of the voltage reference, degrading the TC and increasing the reference voltage deviation.

2.3.7 Bandgap Reference with Successive Voltage-Step Compensation

Conventional high-order curvature compensation usually employs resistors and is used to reduce the TC of a voltage reference. However, to reduce chip area MING et al. (2018) proposed a resistor-less curvature-compensated BGR, called voltage step compensation (VSC). Furthermore, this compensation does not depend on the threshold voltage of MOSFETs V_{TH} to decrease the impact of process variations.

The concept of the proposed bandgap is shown in Fig. 2.19 and it consists of two current references with different TC, a BJT, and two gate-to-source voltage difference

Table 2.6: Measured Results Summary OLIVEIRA et al. (2018).

Specification	This work
Process	0.13 μm CMOS
Temp. Range	-25 - 125 °C
Supply Voltage	0.3 - 1.2 V
V_{REF}	26 mV
V_{REF} σ/μ	3.4* %
TC_{avg}	208 ppm/°C
Line Sensitivity	0.188 %/V
PSRR	-67.3*dB(@100 Hz)
Power Consumption	40 pW
Silicon Area	0.0006 mm^2

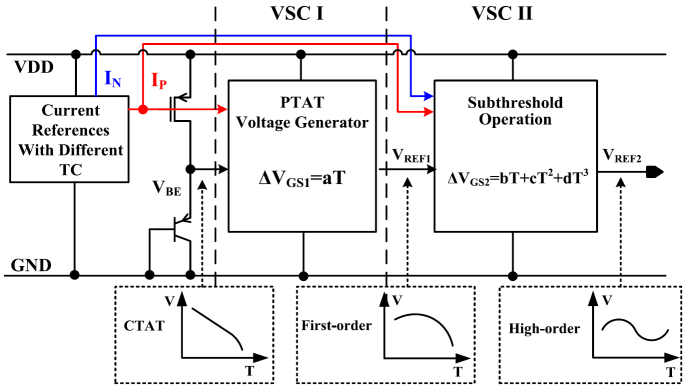
*Simulated;

(ΔV_{GS}) structures. The reference voltage output V_{REF2} can be expressed as

$$V_{REF2} = V_{BE} + \Delta V_{GS1} + \Delta V_{GS2} \tag{2.25}$$

where V_{BE} is the base-emitter voltage of a BJT.

Figure 2.19: Bandgap concept presented in MING et al. (2018).



Source: MING et al. (2018).

The complete schematic of the high-order curvature compensated BGR is shown in Fib. 2.20. The first-order temperature compensation is achieved by a PTAT term biased by a reference current I_P with a positive TC. Assuming electron mobility equals 2x hole mobility, $V_{TH17} = V_{TH18}$ and channel length modulation is neglected for long-channel devices, the first order reference output V_{REF1} can be given by

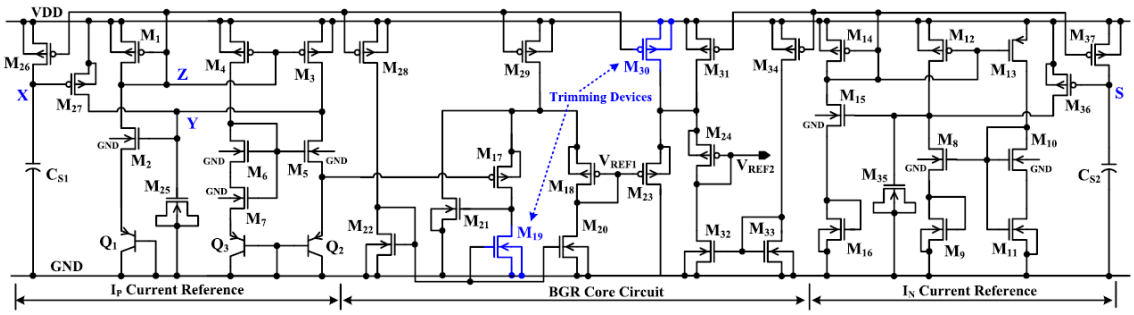
$$V_{REF1} = V_{BE} + \Delta V_{GS1} = V_{BE} + A_1 \phi_T \tag{2.26}$$

where ϕ_T is the thermal voltage. The term A_1 can be written as

$$A_1 = \sqrt{2\delta_1}\left(\sqrt{\lambda_3/(W/L)_{M17}} - \sqrt{1/(W/L)_{M18}}\right) \tag{2.27}$$

where W/L is the width length ratio of the MOSFET transistor channel, δ and λ are temperature independent constants ($\delta_1 = 12.6$). Therefore, by properly designing M_{17} and M_{18}, a first-order temperature compensated reference is achieved.

Figure 2.20: Schematic of the bandgap voltage reference proposed by MING et al. (2018).



Source: MING et al. (2018).

The high-order curvature compensation is obtained with a differential pair biased by two currents of different TC (I_P and I_N). Transistors M_{23} and M_{24} operate in the subthreshold region and have the same aspect ratios. The nonlinear differential voltage ($\Delta V_{GS2} = V_{REF2} - V_{REF2}$) can be expressed as

$$\Delta V_{GS2} = n\phi_T ln(\lambda_2 I_P / I_N). \tag{2.28}$$

The logarithm term has a positive concave relationship with respect to temperature and cancels residual first-order and high-order TC of V_{BE}.

Moreover, a trim scheme is used to reduce the variability impact by adjusting the bias currents to minimize the TC and decrease reference voltage deviation. The proposed BGR was fabricated in a standard 0.5 μm CMOS process and measured 10 samples from the same wafer. Table 2.7 summarizes the performance of the circuit. The voltage-step compensation concept proved to be an interesting choice to improve the TC performance of a BGR. Furthermore, design the VSC concept with advanced technology nodes could reduce power consumption and silicon area.

Table 2.7: Results Summary MING et al. (2018).

Specification	This work
Process	0.5 μm CMOS
Temp. Range	-5 - 125 °C
Supply Voltage	2.1 - 5 V
V_{REF}	1.196 V
V_{REF} σ/μ	0.625[a] %
TC_{avg}	5.87[a] ppm/°C
Line Sensitivity	0.19 mV/V
PSRR @100 Hz	-84 dB
Power Consumption	79.8 μW
Silicon Area	0.053 mm^2

[a]Trimmed;

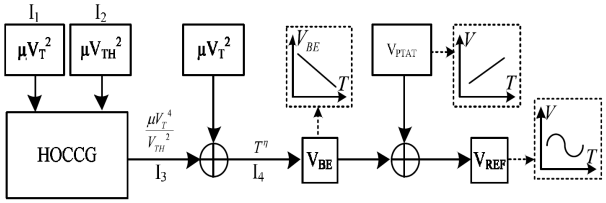
2.3.8 Bandgap Reference with Base-Emitter Voltage Linearization

The high-order nonlinearity of base-emitter voltage V_{BE} can be corrected through strongly temperature-dependent bias currents (MEIJER; SCHMALE; ZALINGE, 1982). Then, another resistorless high-order curvature compensation is implemented by ZHOU et al. (2019). The authors proposed a base-emitter voltage linearization (BEVL) technique

using two resistorless self-biased current sources (RLSBCS) to generate currents proportional to μV_{TH}^2 and $\mu\phi_T^2$, where μ is the carrier mobility of MOSFET, V_{TH} is threshold voltage, ϕ_T is thermal voltage.

The BEVL concept is shown in Fig. 2.21. The two RLSBCS (I_1 and I_2) are injected into a high-order curvature-compensation generator (HOCCG) block to perform mathematical operations and obtain a current I_3 proportional to $\mu\phi_T^4/V_{TH}^2$. Current I_4, a combination of I_1 and I_3, provides the bias current for BJT. This high-order compensated V_{BE} (CTAT term) is added to a PTAT voltage to generate a temperature-stable reference voltage V_{REF}.

Figure 2.21: Bandgap concept proposed by ZHOU et al. (2019).



Source: ZHOU et al. (2019).

The proposed high-precision compensated BGR is illustrated in Fig. 2.22, where all transistors are operating in strong inversion or cut-off region. The current I_3 is generated using a translinear loop technique and can be written as

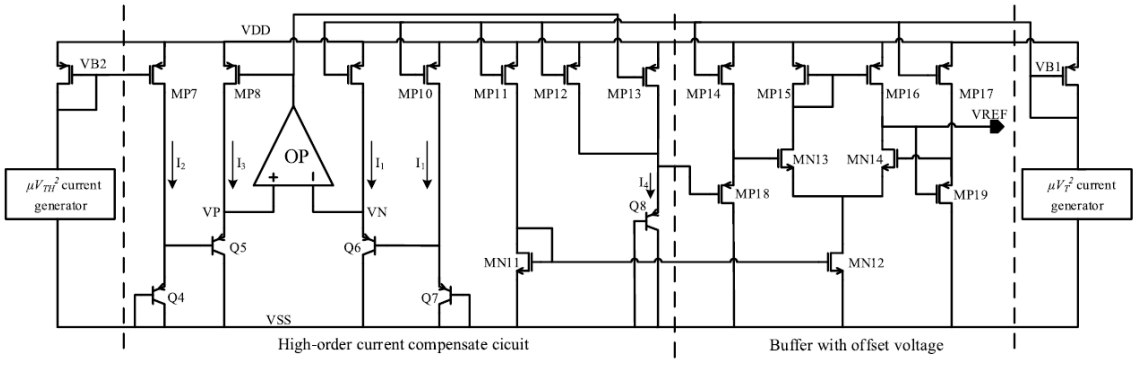
$$I_3 = \frac{I_1^2}{I_2} = \frac{A^2\mu^2\phi_T^4}{B\mu V_{TH}^2} = \chi\frac{T^{4-n}}{(1-\lambda T)^2} \tag{2.29}$$

where λ is temperature coefficient of threshold voltage with positive value, n is usually between 1.5 and 2 in semiconductor surface and, T is temperature. Also, parameters A, B, $\chi = A^2C/(BV_{TH0}^2)$ and C are temperature independent constants and V_{TH0} is the threshold voltage at 0 K. Considering $n = 1.5$, current I_3 can be rewritten as

$$I_3 \approx \chi T^{2.5}(1 + 2\lambda T + 3\lambda^2 T^2). \tag{2.30}$$

From expression (2.30), the current I_3 generate terms of $T^{2.5}$, $T^{3.5}$ and $T^{4.5}$ demonstrating the strong temperature dependence of the reference current. Thus, this current compensate the high-order non-linearity of V_{BE}.

Figure 2.22: Bandgap voltage reference reported in ZHOU et al. (2019).



Source: ZHOU et al. (2019).

The operational amplifier shown in Fig. 2.22. has an input offset voltage V_{OS} that is a PTAT voltage. Then, the reference voltage of the proposed circuit can be expressed as

$$V_{REF} = V_{EB(Q8)} + V_{OS}. \tag{2.31}$$

The circuit was fabricated in a standard 0.35 μm CMOS process and measured 30 samples from the same batch. A two-step trim strategy was used in this work. Table 2.8 summarizes the performance of the circuit. The BEVL technique compensated the thermal non-linearity of V_{BE} and improved the TC of this voltage reference. However, the power consumption of the reference voltage could be decreased. Also, the sensitivity to variability of the bias currents could be reduced by generating bias currents that do not depend on the V_{TH}.

Table 2.8: Measured Results Summary ZHOU et al. (2019).

Specification	This work
Process	0.35 μm CMOS
Temp. Range	-40 - 125 °C
Supply Voltage	2 - 5 V
V_{REF}	1.14055 V
V_{REF} σ/μ	0.97^a %
TC_{avg}	4.03^a ppm/°C
TC_{min}	1.01^a ppm/°C
TC_{max}	8.29^a ppm/°C
Line Sensitivity	2 mV/V
PSRR @100 Hz	-61 dB
Power Consumption	66 μW
Silicon Area	0.0396 mm^2

^{a}Trimmed;

2.4 Performance Summary of the State-of-The-Art

In Table 2.9 a comparison between recent voltage references considering its specifications is presented. MOSFET-only designs (UENO et al., 2009; ZHANG et al., 2018; OLIVEIRA et al., 2018) showed the best results considering power consumption and low supply voltage. These circuits consist of MOSFETs working in the subthreshold region to achieve a low power operation and do not use resistors. UENO et al. (2009) and ZHANG et al. (2018) generated a threshold voltage as the CTAT term and added with a ϕ_T generated by the difference between the gate-source voltages of two transistors operating in subthreshold. Seeking to reduce the power consumption further, the work proposed by OLIVEIRA et al. (2018) used MOSFETs with different threshold voltage, and the difference between these threshold voltages (ΔV_{th}) generated a reference voltage using only three transistors. However, the variability performance of these MOS-only architectures is degraded since the generated voltage depends on the V_{th} and it changes too much with process variation.

Bandgap designs (GE et al., 2011; OSAKI et al., 2013; KLIMACH et al., 2013; MING et al., 2018; ZHOU et al., 2019) tend to show a better performance in terms of variability because V_{BE} is more robust with respect to variability than V_{th}. This can be confirmed by the excellent result achieved in GE et al. (2011). The main drawback of this circuit

is the power dissipation because to improve accuracy performance, more sophisticated strategies are needed, which require more blocks, and it increases power consumption.

Analyzing the TC, one can conclude that bandgap circuits (GE et al., 2011; MING et al., 2018; ZHOU et al., 2019) showed better performance. Furthermore, MOSFET-only circuits not presented very high precision stability over temperature because devices biased in the subthreshold region are much more sensitive to temperature variations.

In regards to the above-mentioned design trends and limitations, it is possible to identify some open challenges. To improve the trade-off between power consumption and variability is a big one because a μW power consumption range is unacceptable for emerging nW microsystems. Moreover, improvements in the design to achieve a low TC combining with a low V_{REF} σ/μ are relevant too. Also, to propose a trimming technique with a fast and simple calibration procedure that can boost the circuit performance is a necessary research advance.

Table 2.9: Comparison of Recent Published CMOS Voltage References.

Specification	[1]	[2]	[3]	[4]^{s}	[5]	[6]	[7]	[8]
Process (μm)	0.35	0.16	0.18	0.18	0.18	0.18	0.5	0.35
Temp. Range (°C)	-20 - 80	-40 - 125	-40 - 120	-40 - 85	-40 - 125	-25 - 125	-5 - 125	-40 - 125
Measured Samples	17 1 batch	61 2 batches	9 1 batch	-	63 1 batch	5 1 batch	10 1 batch	30 1 batch
V_{DD} (V)	1.4 - 3	1.8	1.2 - 1.8	1.8	1 - 1.8	0.3 - 1.2	2.1 - 5	2 - 5
V_{REF} (V)	0.745	1.0875	1.09	1.29	0.756	0.026	1.196	1.14055
V_{REF} σ/μ (%)	0.87	0.05^{a}	0.737	0.26	0.95^{a}	3.4^{s}	0.625^{a}	0.97^{a}
TC_{avg} (ppm/°C)	15	-	147	14.51	49.6^{a}	208	5.87^{a}	4.03^{a}
TC_{min} (ppm/°C)	7	5^{a}	-	-	-	-	3.98^{a}	1.01^{a}
TC_{max} (ppm/°C)	45	12^{a}	-	28.8	-	-	8.29^{a}	-
LS (%/V)	0.002	-	-	-	0.524	0.188	0.19	0.02
PSRR@100Hz (dB)	-45	74*	-62	-	-52	-67.3^{s}	-84	-61
Power@V_{DDnom} (nW)	320	99000	100	77400	23	0.04	79800	66000
Silicon Area (mm^2)	0.055	0.12	0.0294	0.015	0.0162	0.0006	0.053	0.0396
FoM$_{Sansen}$ (°C^3/W mm^2)	3.8	0.046	5.9	0.093	150	450000	0.068	0.26
FoM (°C^3/W mm^2)	3.3	22.2	0.5	0.7	20	1250	0.2	0.4

^{a}Trimmed; ^{s}Simulated;*@DC

[1] UENO et al. (2009); [2] GE et al. (2011); [3] OSAKI et al. (2013); [4] KLIMACH et al. (2013); [5] ZHANG et al. (2018); [6] OLIVEIRA et al. (2018); [7] MING et al. (2018); [8] ZHOU et al. (2019);

3 CTAT AND PTAT VOLTAGE GENERATORS

The reduced temperature sensitivity of a VR is achieved by adding two voltages or currents that present opposite temperature sensitivity directions. The most usual solution combines PTAT and CTAT structures but it is possible to subtract two voltages or currents that present the same temperature sensitivity direction (both PTAT or both CTAT). Generally, the base-emitter voltage (V_{BE}) of a bipolar transistor or the threshold voltage (V_{T0}) of a MOSFET are used to produce a CTAT voltage. The PTAT term usually results from a circuit that generates an output voltage proportional to the thermal voltage (ϕ_T). In this chapter, the voltage variability of CTAT and PTAT generators are discussed and analyzed to understand the impact of these structures on the accuracy of a voltage reference.

CMOS PTAT and CTAT generator circuits usually operate with transistors in weak or moderate inversion since these conditions decrease power consumption. Then, a MOSFET model that continuously describes all device operation regions is needed. In this thesis, the Unified Current-Control Model (UICM) proposed by CUNHA; SCHNEIDER; GALUP-MONTORO (1998) is used to design the circuits. Appendix B shows the detailed UICM model.

Also, the results presented in this chapter were obtained for schematic simulations using the BSIM4 (V4.5) model performed by the Cadence Virtuoso™ Spectre™ electrical simulator. Schematic simulations present an interesting result since VR circuits are operated in a DC condition. Post-layout parasitic affects mainly the dynamic behavior of the circuit and only a few parameters (PSR, noise, and start-up time) are influenced by this simulation. The reference voltage, temperature coefficient, σ/μ or line sensitivity are not significantly affected by post-layout parasitic. The circuits were implemented in TSMC 180 nm process using standard threshold voltage NMOS and PMOS transistors.

3.1 CTAT Voltage Generators

In the traditional BGR, the temperature-independence is achieved by adding a voltage that is PTAT with a junction diode voltage that is CTAT. A p-n junction or the MOSFET threshold voltage are generally used to generate the CTAT voltage in a VR. Moreover, a CTAT structure can be self-biased or biased by an independent biasing circuit. The biasing current is important because it affects the accuracy of the generated CTAT voltage (AITA et al., 2013).

Voltage reference designs using V_{BE} as the CTAT term presents better performance in terms of accuracy because V_{BE} is less sensitive to fabrication variability than V_{T0} (TSIVIDIS, 1980; GE et al., 2011; LEE et al., 2015). However, the forward biased p-n junction requires higher supply voltages and has a slightly non-linear behavior over temperature. Then, to reduce the variation of reference voltage over a wide temperature range, high-

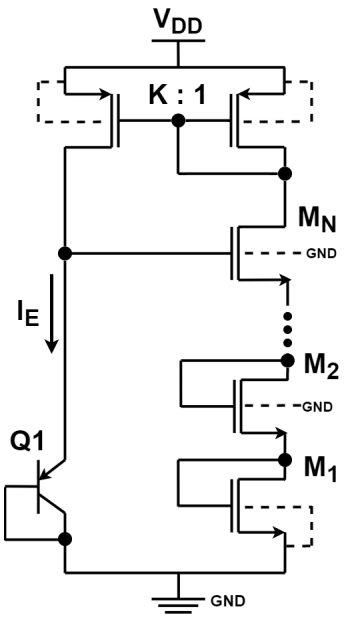
order temperature compensation techniques have been developed (MING et al., 2018; ZHOU et al., 2019), but they impact on power consumption and silicon area. Moreover, to achieve lower supply voltages, schottky barrier diodes (SBD) (LU et al., 2015; CAMPANA; KLIMACH; BAMPI, 2016) and voltage dividers (OSAKI et al., 2013; LIU; MU; ZHU, 2018) can be used to ensure sub-1V supply operation in CTAT generators.

In this section, a CTAT voltage generator composed of a self-biased BJT circuit which allows a V_{EB} voltage division is analyzed. The focus is to understand the fabrication uncertainties that produce significant variations in this type of circuit.

3.1.1 Resistorless BJT Bias Circuit

The emitter-base voltage of the BJT has a CTAT behavior when biased by a current. Then, we investigated a resistorless BJT bias proposed by MATTIA; KLIMACH; BAMPI (2014), because this topology resulted in a small silicon area, works in a nano-ampere current consumption range and comprises a voltage divider. In this work, the gate-source voltage of N stacked transistors is counterbalanced by the V_{EB} of the BJT, as shown in Fig. 3.1. The bipolar emitter current is defined by the resulting gate-source voltage through a feedback path that adopt a current mirror with gain K. When specifying values for K and N, the circuit reaches a non-zero equilibrium DC point, which reflects the current-voltage response of the BJT and the MOSFETs. The transistors drain current are heavily dependent on the number N and the temperature dependence of the generated emitter current can change the $\partial V_{EB}/\partial T$ derivatives. Thus, the author states that the V_{EB} voltage can be linearized through an almost cubic emitter current.

Figure 3.1: BJT bias circuit proposed by MATTIA; KLIMACH; BAMPI (2014).



Source: Author.

In this circuit, the emitter current I_E of transistor Q_1 can be expressed as:

$$I_E = KI_{D1} \tag{3.1}$$

where I_{D1} is the drain current of M_1. Considering the UICM model (CUNHA; SCHNEIDER; GALUP-MONTORO, 1998), the drain current I_D of a transistor in the subthreshold

region is given by:

$$I_D = 2I_{SQ}S\ exp\left(\frac{V_G - V_{T0}}{n\phi_T} - \frac{V_S}{\phi_T}\right)\left[1 - exp\left(-\frac{V_{DS}}{\phi_T}\right)\right] \tag{3.2}$$

where I_{SQ} is the is the sheet normalization current, $S = W/L$ is the transistor aspect ratio, W being the width, and L the length of the transistor, V_{T0} is the threshold voltage for zero bulk-source voltage, ϕ_T is the thermal voltage, V_{DS} is the drain-source voltage, V_G and V_S are the gate and source voltages referred to the substrate, respectively. The MOSFETs are in saturation under weak inversion level when $V_{DS} > 4\phi_T$.

From Fig. 3.1, $I_{D1} = I_{DN}$ and $V_{GN} = V_{EB}$. Assuming that M_1 and M_N are in the subthreshold region and saturated, have the same W, L, and slope factor n. According to (3.2), the emitter-base voltage can be written as (3.3), and the gate-source voltage is approximated by (3.4).

$$V_{EB} = V_{GS1} + nV_{GN-1} \tag{3.3}$$

$$V_{GS1} \approx \frac{V_{EB}}{1 + n(N-1)} \tag{3.4}$$

Moreover, according to SZE (1981) the I_E can be expressed by

$$I_E = I_{SE}\ exp\left(\frac{V_{EB}}{m\phi_T}\right) \tag{3.5}$$

where I_{SE} is the reverse saturation current and m is the slope factor of bipolar transistor.

From (3.1), (3.2), (3.4), and (3.5), the junction voltage V_{EB} can be obtained, as given by (3.6).

$$V_{EB} = \frac{m(nN - n + 1)}{n(nN - n + 1) - m}\left[n\phi_T\ ln\left(2KS_1\frac{I_{SQ}}{I_{SE}}\right) - V_{T0}\right] \tag{3.6}$$

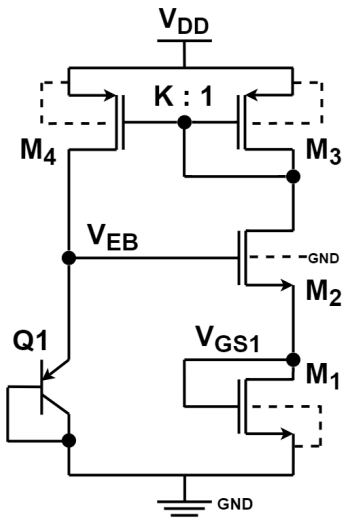
According to (3.6), it is possible achieve distinct $\partial V_{EB}/\partial T$ derivatives by modifying N and K. However, this generated CTAT voltage depends directly on V_{T0}, I_{SQ}, and I_{SE}, which impact on the V_{EB} variability.

From the methodology presented in COITINHO et al. (2001), the MOSFET parameters V_{T0} and I_{SQ} were extracted and its process deviations estimated by Monte Carlo simulations. Considering only process variability the σ/μ of V_{T0} is 2.37% and the σ/μ of I_{SQ} is 2.25%. The I_{SE} current spread of a BJT was estimated in GE et al. (2011) as σ/μ = 0.8%. Therefore, the main source of deviations is the V_{T0} because it varies more than the I_{SQ} and I_{SE} parameters. Also, I_{SQ} and I_{SE} are into a natural logarithm in (3.6), which attenuates the effects of these variations.

Thus, this resistorless self-biased BJT topology was designed to evaluate its performance and to understand this variability impact. The transistor dimensions were calculated using equations presented in this section and aiming an I_E of 3.5 nA at ambient temperature. The circuit shown in Fig. 3.2 was simulated considering N = 2, K = 1, W_{1-4} = 2 μm, L_{1-4} = 2 μm, and V_{DD} = 1.8 V.

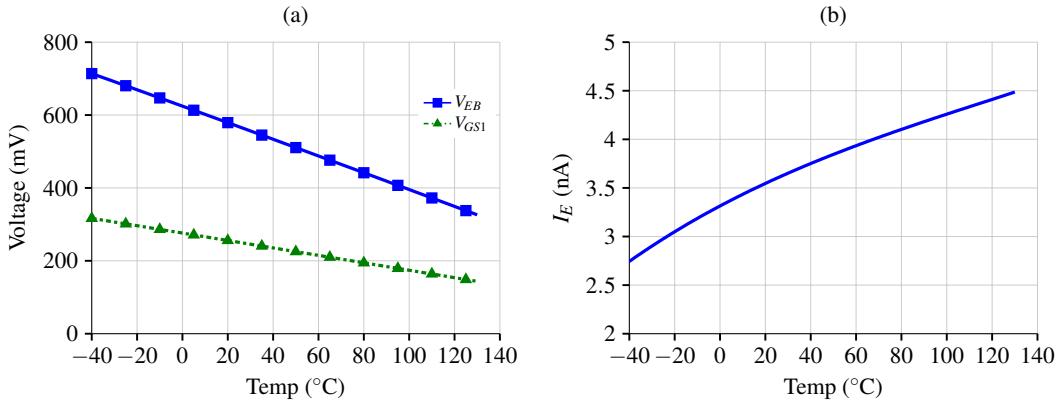
The temperature behavior of the generated V_{EB} and V_{GS1} are presented in Fig. 3.3(a), from -40 to 130 °C. According (3.4), $V_{GS1} \approx V_{EB}/(n+1)$ and this difference of slopes is confirmed by Fig. 3.3(a). The I_E current temperature dependence is shown in Fig. 3.3(b).

Figure 3.2: Simulated BJT bias circuit schematic (N = 2; K = 1).



Source: Author.

Figure 3.3: (a) V_{EB} and V_{GS1} voltages over temperature; (b) I_E current over temperature.



Source: Author.

The temperature coefficient of this generated CTAT voltage can be expressed by its derivative, as shown in (3.7). The TC of the CTAT voltages are presented in Fig. 3.4.

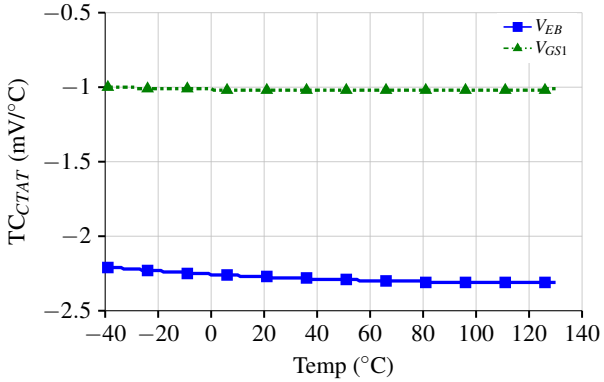
$$TC_{CTAT} = \frac{\partial V_{EB}}{\partial T} \tag{3.7}$$

To analyze the fabrication variability of the circuits, Monte Carlo (MC) simulations with 200 runs were performed for local mismatch effects (MM) and average process (PC) variations. The nominal V_{EB} voltage histograms at 27°C are presented in Fig. 3.5, where μ is the mean value and σ the standard deviation. Considering process variations only, the V_{EB} variability coefficient σ/μ resulted in 2.19%, considering mismatch only resulted in 0.45%, and both effects combined resulted in 2.25%.

Temperature coefficient histograms are presented in Fig. 3.6. MC simulations show the variability impact in the accuracy of the V_{EB} voltage slope. Considering process variations only, the TC variability coefficient resulted in 0.80%, considering mismatch only resulted in 0.028%, and both effects combined resulted in 0.80%.

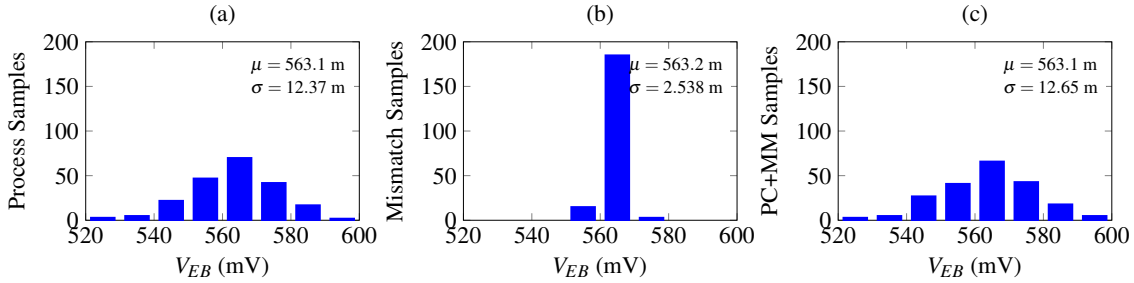
Table 3.1 shows the summary of the results considering the self-biased resistorless topology. As presented in the circuit analysis and according to (3.6), the circuit perfor-

Figure 3.4: V_{EB} and V_{GS1} derivatives over temperature.



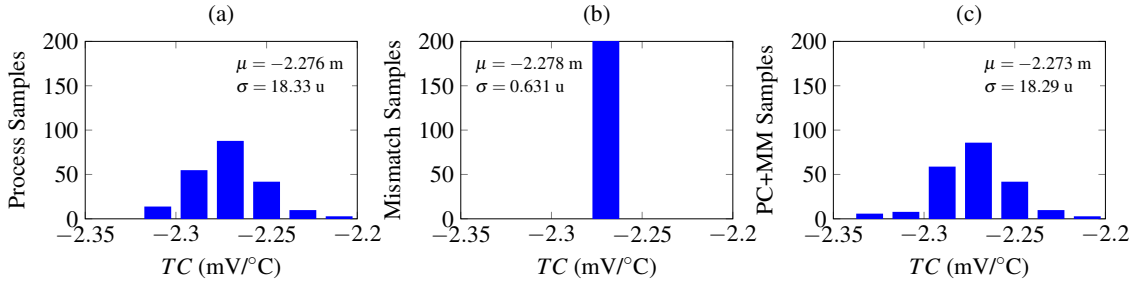
Source: Author.

Figure 3.5: MC simulations histograms of V_{EB} voltage at 27°C. Average process variation on (a); Local mismatch on (b); Combined on (c).



Source: Author.

Figure 3.6: MC simulations histograms of TC. Average process variation on (a); Local mismatch on (b); Combined on (c).



Source: Author.

mance is strongly dependent on process parameters as V_{T0}, I_{SQ}, and I_{SE}. Therefore, this CTAT generator is more sensitive to process variations than to mismatch.

Considering the presented variability analysis, in the next chapter, we propose a different BJT biasing circuit to generate a CTAT voltage and reduce the process variability impact on this signal.

3.2 PTAT Voltage Generators

The base-emitter voltage difference (ΔV_{BE}) between two bipolar transistor with different current density or the temperature dependence of the difference between the gate-

Table 3.1: Performance summary of the circuit in 180 nm CMOS at V_{DD} = 1.8V.

Parameter	BJT Bias	Unit
I_E	3.6	nA
Temp. Range	-40 - 130	°C
V_{EB}		
μ	563.1	mV
σ	12.65	mV
σ/μ	2.25	%
TC_{CTAT}		
μ	-2.273	mV/°C
σ	18.29	uV/°C
σ/μ	0.80	%

source voltages (ΔV_{GS}) of two MOSFETs operating in the subthreshold region are used to obtain the ϕ_T generator. This ΔV_{GS} can be generated by the association of two transistors that share the same gate connection, known as self-cascode MOSFET, or the same source connection, known as unbalanced differential pair.

The sensitivity to fabrication variability of the ϕ_T generators is relevant because these uncertainties can also degrade the reference accuracy. Thus, three usual MOS-only PTAT generator architectures were designed and analyzed here: the self-cascode MOSFET, the unbalanced differential pair, and the high-slope topology.

3.2.1 Self-Cascode MOSFET (SCM) Topology

The self-cascode MOSFET (SCM) shown in Fig. 3.7(a) is widely used as a PTAT generator and commonly applied on low-voltage analog blocks as presented in VITTOZ; NEYROUD (1979), SERRA-GRAELLS; HUERTAS (2003) and CAMACHO-GALEANO; GALUP-MONTORO; SCHNEIDER (2005). It consists of the series association of two transistors M_1 and M_2, where M_1 operates in triode or saturation regions and M_2 must be in saturation.

Following (B.1), the current in M_1 and M_2 can be expressed as (ROSSI; GALUP-MONTORO; SCHNEIDER, 2007)

$$I_{D_1} = I_{SQ} S_1 (i_{f_1} - i_{r_1}) \tag{3.8}$$

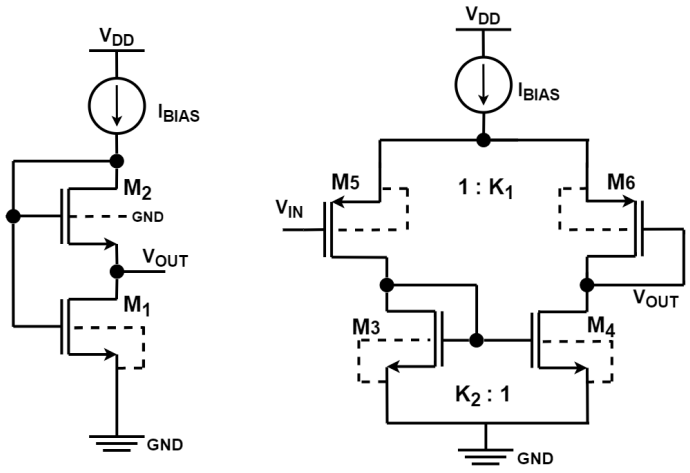
$$I_{D_2} = I_{SQ} S_2 i_{f_2}. \tag{3.9}$$

where parameters i_f and i_r are the normalized forward and reverse currents, related to the source and drain inversion charge densities, I_{SQ} is the sheet normalization current, I_D is the transistor drain current, $S = W/L$ is the transistor aspect ratio, W being the width, and L the length of the transistor.

Considering that the drain voltage of M_1 equals the source voltage of M_2 ($V_{D1} = V_{S2}$), then $i_{f_2} = i_{r_1}$, and therefore one can calculate the relationship between i_{f_1} and i_{f_2} as follows:

$$i_{f_1} = \left(1 + \frac{S2}{S1}\right) i_{f_2} = K_0 i_{f_2}. \tag{3.10}$$

Figure 3.7: (a) Self-Cascode MOSFET PTAT generator and (b) unbalanced differential pair schematic.



(a) (b)

Source: Author.

Applying the UICM, considering K_0 a constant design factor and V_P the pinch-off voltage, since $V_{P2} = V_{P1}$, solving for the output voltage V_{OUT} results in

$$\frac{V_{OUT}}{\phi_T} = F(i_{f_1}) - F(i_{f_2}) = F(K_0 i_{f_2}) - F(i_{f_2}) \tag{3.11}$$

Keeping V_{OUT} low (typically lower than $3\phi_T$) and M_2 in weak inversion, (3.11) can be approximated by (VITTOZ; NEYROUD, 1979)

$$V_{OUT} = \phi_T \ln K_0. \tag{3.12}$$

From (3.12), the generated PTAT voltage depends only on geometrical factors. This circuit also generates a PTAT voltage independent of the inversion region, as long as the inversion levels i_{f1} and i_{f2} are kept constant. Then, this is achieved by biasing this structure with a current I_{BIAS} proportional to I_{SQ}.

3.2.2 Unbalanced Differential Pair Topology

Another PTAT generator circuit is the unbalanced differential pair (TSIVIDIS; ULMER, 1978; OSAKI et al., 2013; MU et al., 2017), shown in Fig. 3.7(b). This topology is appropriate to achieve PTAT voltage slopes higher than the ones obtained with SCM. When the MOSFETs are in the saturation region, according to (B.3) for all inversion levels, the difference between gate-to-gate voltages ($V_{G6} - V_{G5} = V_{OUT} - V_{IN} = V_{DIFF}$) can be expressed by

$$\frac{V_{DIFF}}{n\phi_T} = F(i_{f_5}) - F(i_{f_6}). \tag{3.13}$$

In Fig. 3.7(b), M_3 and M_4 represent the NMOS-current mirror responsible for biasing M_5 and M_6, respectively. Moreover, K_1 and K_2 are the aspect ratio relations of $M_6 - M_5$ (i.e. $K_1 = (W_6/W_5)(L_5/L_6)$) and $M_3 - M_4$ (i.e. $K_2 = (W_3/W_4)(L_4/L_3)$), respectively, thus it is possible to verify that $i_{f_5}/i_{f_6} = K_1 K_2$ and $I_5 = (K_2 I_{bias})/(K_2 + 1)$, and

substituting it into (3.13) leads to

$$\frac{V_{DIFF}}{n\phi_T} = F\left[\left(\frac{(K_1K_2)I_{bias}}{(1+K_2)S_6I_{SQ}}\right)\right] - F\left[\left(\frac{I_{bias}}{(1+K_2)S_6I_{SQ}}\right)\right]. \tag{3.14}$$

Eq. (3.14) can be rewritten as (3.15) and (3.2) can be expressed by (3.16).

$$\frac{V_{DIFF}}{n\phi_T} = F\left(K_1K_2i_{f_6}\right) - F\left(i_{f_6}\right) \tag{3.15}$$

$$i_f = 2\,exp\left(F(i_f)\right) \tag{3.16}$$

Since M_5 and M_6 operate in weak inversion, considering (3.16), and making $K_1K_2 > 1$, (3.15) can be approximated as (3.17).

$$V_{DIFF} = n\phi_T \ln\left(K_1K_2\right) \tag{3.17}$$

From (3.17), the PTAT voltage depends on n and on transistors geometrical ratios. The inversion levels i_{f_5} and i_{f_6} will remain constant over temperature if the M_5 and M_6 pair is biased by a current source proportional to I_{SQ}.

3.2.3 High-Slope Topology

A high-slope PTAT generator structure is shown in Fig. 3.8 (ZHANG et al., 2018). It consists essentially of an asymmetrical differential cell with all MOSFETs operating in the subthreshold region, enhancing the PTAT voltage slope. The UICM model was used to extend this circuit operation to all inversion levels, as it was done for the SCM and the unbalanced differential pair. Assuming that all transistors are in saturation and using (B.3), the gate-to-gate voltage of the high-slope circuit ($V_{GG} = V_{OUT} - V_{IN}$) is given by

$$\frac{V_{GG}}{n\phi_T} = F(i_{f_7}) - F(i_{f_{16}}) + F(i_{f_8}) - F(i_{f_{13}}) + F(i_{f_{12}}) - F(i_{f_9}). \tag{3.18}$$

The current through M_8 is $K_3I_{bias}/(K_3+K_4+2)$, M_{10}, M_{11}, M_{14}, and M_{15} are NMOS-current mirror biasing M_7, M_8, M_9, M_{12}, M_{13}, and M_{16}. Considering $K_{16,7} = S_{16}/S_7$, $K_{13,8} = S_{13}/S_8$, $K_{12,9} = S_{12}/S_9$, and neglecting the small difference in n of NMOS and PMOS, (3.18) results in

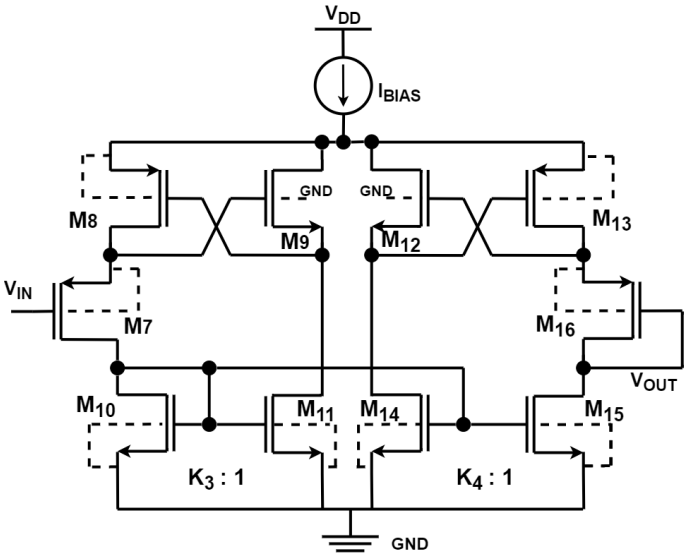
$$\begin{aligned}\frac{V_{GG}}{n\phi_T} = &F\left(\frac{(K_3K_{16,7})I_{bias}}{S_{16}I_{SQ}(K_3+K_4+2)}\right) - F\left(\frac{I_{bias}}{S_{16}I_{SQ}(K_3+K_4+2)}\right)\\ &+F\left(\frac{(K_3K_{13,8})I_{bias}}{S_{13}I_{SQ}(K_3+K_4+2)}\right) - F\left(\frac{I_{bias}}{S_{13}I_{SQ}(K_3+K_4+2)}\right)\\ &+F\left(\frac{(K_4K_{9,12})I_{bias}}{S_9I_{SQ}(K_3+K_4+2)}\right) - F\left(\frac{I_{bias}}{S_9I_{SQ}(K_3+K_4+2)}\right)\end{aligned} \tag{3.19}$$

Since M_7, M_8, M_9, M_{12}, M_{13}, and M_{16} operate in weak inversion, (3.19) can be derived as

$$V_{GG} = n\phi_T \ln\left(K_3K_{16,7}K_3K_{13,8}K_4K_{9,12}\right) \tag{3.20}$$

From (3.20), there are more multiplication factors in the logarithm operator than (3.12) and (3.17). Thus, this circuit can provide the higher PTAT slope compared to the SCM and the differential pair topologies. Also, as long as i_{f_7}, i_{f_8}, i_{f_9}, $i_{f_{12}}$, $i_{f_{13}}$, and $i_{f_{16}}$ are kept constant over temperature, they generate a PTAT voltage under any inversion level.

Figure 3.8: High-Slope PTAT generator schematic.



Source: Author.

3.2.4 Circuit Design and Performance Comparison

In this first analysis, the three topologies were designed with the same power consumption condition for performance comparison since this is a fundamental aspect of today ultra-low-power designs. The transistor dimensions were optimized to achieve maximum PTAT slopes with feasible sizes and multipliers. The circuits were designed following the inversion level model and the equations presented in this section. The ideal current sources were replaced by the current bias source proposed in CAMACHO-GALEANO; GALUP-MONTORO; SCHNEIDER (2005). The current I_{bias} is proportional to the specific current I_{SQ}, being designed to be 9.5 nA at ambient temperature. Table 3.2 presents the transistor sizes for the three topologies previously presented, as well as the inversion level of every MOSFET in the three designs.

The temperature behavior of the three PTAT voltage topologies is shown in Fig. 3.9, from -40 to 130 °C. From this figure, one can verify the different slopes of each architecture. The temperature coefficient of the PTAT voltage can be expressed by its derivative

$$TC_{PTAT} = \frac{\partial V_{OUT}}{\partial T} \tag{3.21}$$

where V_{OUT} is the PTAT output voltage, and T is the corresponding temperature range. The SCM topology presents a nominal TC around 196.5 μV/°C, the differential pair topology achieved a nominal TC of 417.13 μV/°C, and the high-slope topology showed a nominal TC of 798.24 μV/°C.

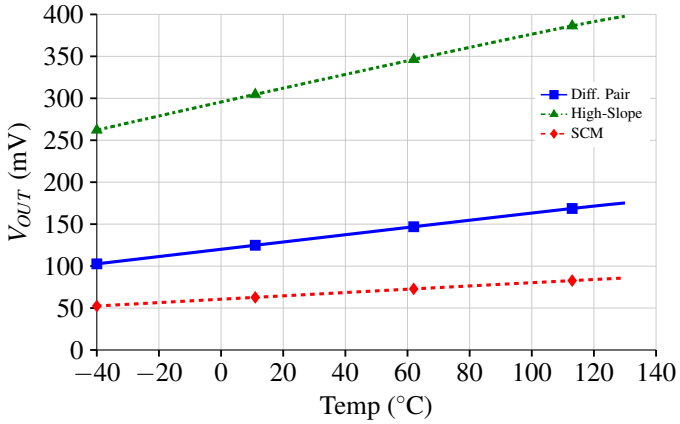
The temperature coefficient of the PTAT voltages are shown in Fig. 3.10. From this plot, it is noted that the non-linearities of the generated PTAT voltages over higher temperatures affect the three structures but mainly the high-slope circuit.

To make a fair comparison considering the fabrication variability performance, the SCM and the unbalanced differential pair topologies were cascaded seeking to achieve a similar TC compared to the high-slope type, as shown in Fig. 3.11. Each branch of the circuits was biased by same I_{bias} current, that is proportional to the specific current I_{SQ} and designed to be 9.5 nA at ambient temperature. The circuits were simulated considering

Table 3.2: Dimensions and i_f of the transistors.

Topology		i_f	$W(\mu m)$	$L(\mu m)$
SCM	M_1	0.06	2	2
	M_2	0.006	9*2	2
Diff. Pair	M_3	0.042	6*2	10
	M_4	0.042	2	10
	M_5	0.05	2.1	2
	M_6	0.011	7*2.1	2
High-Slope	M_7	0.08	1	3
	M_8	0.07	1.5	4
	M_9	0.002	6*1.2	4
	M_{10}	0.033	8*1	10
	M_{11}	0.033	1	10
	M_{12}	0.08	1.2	4
	M_{13}	0.002	4*1.5	4
	M_{14}	0.033	8*1	10
	M_{15}	0.033	1	10
	M_{16}	0.001	10*1	3

Figure 3.9: PTAT voltages vs temperature.



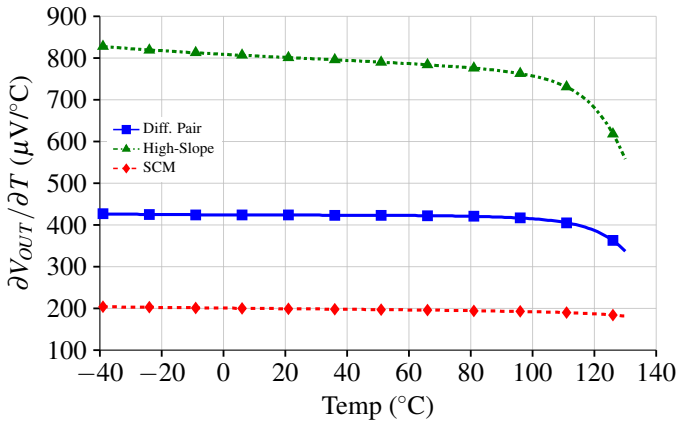
Source: Author.

1.8 V of supply voltage.

To analyze the fabrication variability of the circuits, Monte Carlo simulations with 200 runs for each topology were performed for local mismatch effects and average process variations. Temperature coefficient histograms are presented in Fig. 3.12, where μ is the mean value and σ the standard deviation. MC simulations show the variability impact in the accuracy of the PTAT voltage slope and that the high-slope topology has the highest variability coefficient $\sigma/\mu = 1.76\%$, followed by the differential pair topology with $\sigma/\mu = 1.44\%$, and SCM with $\sigma/\mu = 0.56\%$. Considering only process variations the TC variability coefficient achieved a result of 0.53%, 1.45%, and 1.73%, for mismatch only achieved 0.15%, 0.094%, and 0.12% in the SCM, differential pair, and high-slope structures, respectively.

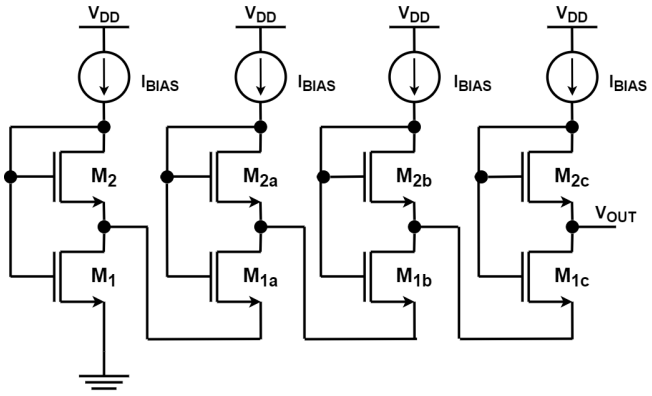
The nominal PTAT output voltage at 27°C was also simulated through an MC analy-

Figure 3.10: PTAT derivatives vs temperature.

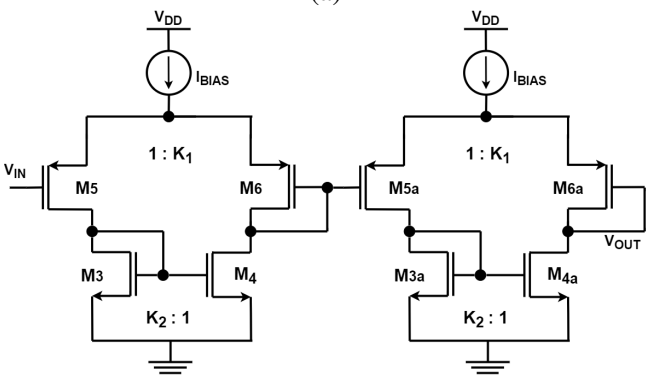


Source: Author.

Figure 3.11: Cascaded (a) SCM and (b) unbalance differential pair topologies.



(a)



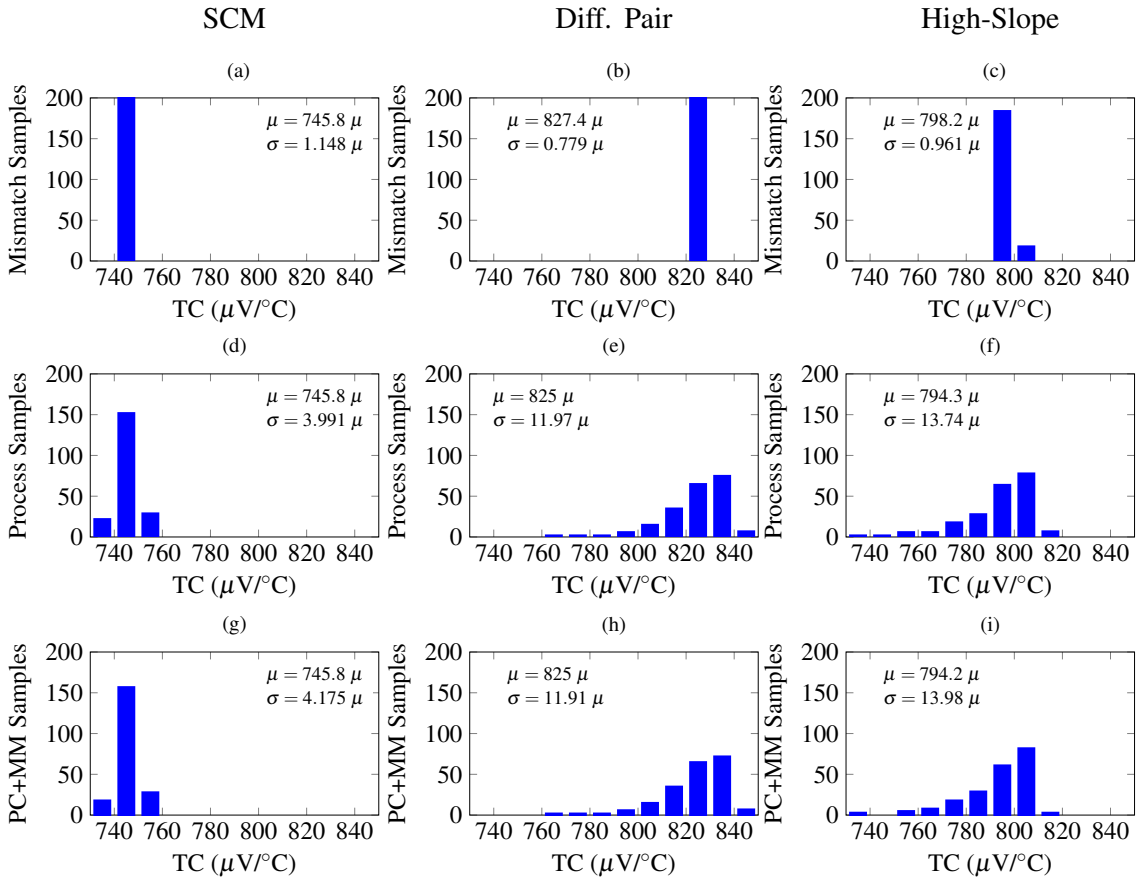
(b)

Source: Author.

sis (process and mismatch) and its histograms are presented in Fig. 3.13. The high-slope circuit has the worst variability coefficient again, with $\sigma/\mu = 4.22\%$, the SCM and the unbalanced differential pair topology achieved a similar one with $\sigma/\mu = 0.94\%$. Considering process variations only, the PTAT voltage variability coefficient resulted in 0.72%, 0.19%, and 4.05%, considering mismatch only resulted in 0.60%, 0.91%, and 0.75% in the SCM, differential pair, and high-slope structures, respectively.

Considering the analyzed parameters, a FoM that represents an overall performance

Figure 3.12: MC simulations histograms of TC. Local mismatch on (a), (b) and (c); Average process variation on (d), (e) and (f); Combined on (g), (h) and (f).



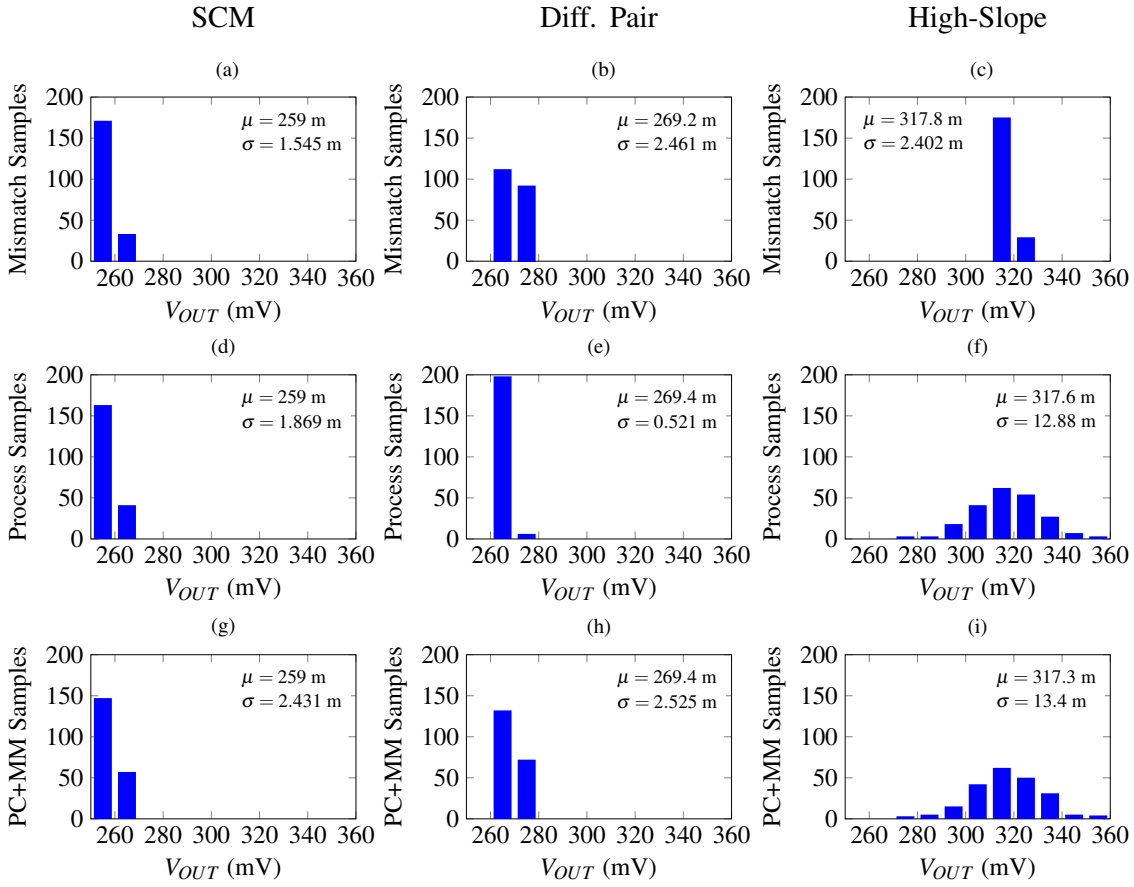
Source: Author.

of the PTAT voltage generators is described in (3.22).

$$FoM_{PTAT} = \frac{(T_{max} - T_{min})TC_{PTAT}}{Power.(V_{OUT}\ \sigma/\mu).(TC_{PTAT}\ \sigma/\mu)} \tag{3.22}$$

Table 3.3 shows a comparison of the results considering the simulated circuits. The SCM structure presented the best accuracy of PTAT voltage slope. The unbalanced differential pair and SCM topologies resulted in a similar nominal PTAT voltage variability, but the unbalanced differential pair suffered less from process variations. Both these designs showed a more accurate PTAT voltage and slope than the one generated by the high-slope architecture. Among these designs, the SCM structure and the differential pair structure are the ideal topology choice for a high precision voltage reference. However, the SCM topology must be cascaded to obtain the same PTAT slope as the other compared circuits, which can lead to more current consumption.

Figure 3.13: MC simulations histograms of a PTAT output voltage at 27°C. Local mismatch on (a), (b) and (c); Average process variation on (d), (e) and (f); Combined on (g), (h) and (f).



Source: Author.

Table 3.3: Performance comparison between PTAT circuits in 180 nm CMOS at V_{DD} = 1.8V.

Parameter	SCM	Diff. Pair	High Slope	Unit
I_{bias}	38	19	9.5	nA
Temp. Range	-40 -130	-40 -130	-40 -130	°C
TC_{PTAT}				
μ	745.8	825	794.2	μV/°C
σ	4.175	11.91	13.98	μV/°C
σ/μ	0.56	1.44	1.76	%
V_{OUT}				
μ	259	269.4	317.3	mV
σ	2.431	2.525	13.4	mV
σ/μ	0.94	0.94	4.22	%
FOM_{PTAT}	35.2	30.3	10.6	V/W

4 PROPOSED SUB-BANDGAP VOLTAGE REFERENCES

Considering the PTAT and CTAT structures previously analyzed, this chapter presents two sub-bandgap voltage references designs. The proposed circuits employ a bipolar transistor and two types of PTAT voltage generators. A BJT biasing is developed to reduce the CTAT voltage variability and improve the reference voltage accuracy. A resistorless structure is chosen to meet the present low power consumption requirements, occupy a small silicon area, and allow fabrication in standard digital CMOS process. Also, a trimming technique is proposed to obtain a low TC. The design methodology is based on the UICM model (Appendix B) and is detailed for each circuit.

4.1 BJT circuit with I_{SQ} current

As shown in the previous section, the resistorless BJT bias proposed by MATTIA; KLIMACH; BAMPI (2014) suffers from a high process variability due to the direct dependence of the V_{T0} in the V_{EB} voltage. The bipolar transistor must be biased by a current that is independent of the threshold voltage to suppress its variability deviations. Therefore, it is possible to achieve a CTAT voltage independent of the V_{T0} by biasing the BJT with a current proportional to I_{SQ}.

Considering that an I_{SQ} current source generates an output current I_{BIAS}. Then, the BJT is biased by this generated I_{BIAS} current. According to (3.5), the V_{EB} voltage is given by (4.1), showing that the V_{EB} voltage does not depend on the V_{T0}.

$$V_{EB} = m\phi_T ln\left(\frac{I_{BIAS}}{I_{SE}}\right) \tag{4.1}$$

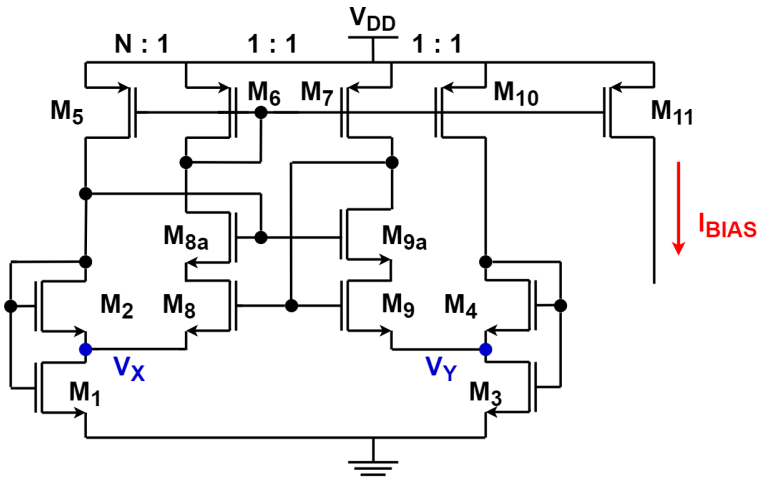
An I_{SQ} current generator needs to be implemented to bias the BJT. The self-biased I_{SQ} current source proposed by CAMACHO-GALEANO et al. (2008) is suitable for low power applications, presents low sensitivity to changes in the supply voltage, and has a good transistor matching to reduce mismatch effects. Thus, this topology was chosen for biasing the bipolar transistor.

The SCM structure is the core of this current source as shown in Fig. 4.1. In the previous chapter, the SCM was explored and the intermediate node V_X, presented in Fig. 4.2, is a PTAT voltage. The UICM model is used to design this I_{SQ} current generator, and considering (B.1) and (B.2), the relationship between M_1 and M_2 is expressed by

$$\alpha = \frac{i_{f1}}{i_{f2}} = \left[1 + \frac{S_2}{S_1}\left(1 + \frac{1}{N}\right)\right] \tag{4.2}$$

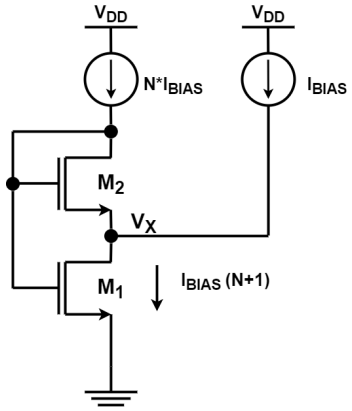
where factor N is the current gain of a PMOS current mirror and the provided I_{BIAS} is proportional to I_{SQ}.

Figure 4.1: I_{SQ} current source presented in CAMACHO-GALEANO et al. (2008).



Source: Author.

Figure 4.2: Biasing relations for the SCM.



Source: Author.

The design started by choosing the inversion level of M_2. The operation of M_2 under a weak inversion condition results in a current very sensitive to V_X, meaning that deviations in V_X due to M_1 and M_2 mismatch could lead to an inaccuracy of the generated current. Therefore, we choose to operate with the SCM composed by M_1 and M_2 in moderate inversion level with $i_{f2} = 9$. It was defined $S_1 = S_2$ to simplify the $M_1 - M_2$ transistor matching in the layout of the circuit. Considering $N = 1$ it is possible to calculate the relation between M_1 and M_2 presented in (4.2). Then, the M_1 and M_2 relation resulted in $\alpha = 3$.

The generated reference current is defined by an aspect ratio relation, as follows

$$NI_{BIAS} = I_{S2}i_{f2} = S_2 I_{SQ} i_{f2} \tag{4.3}$$

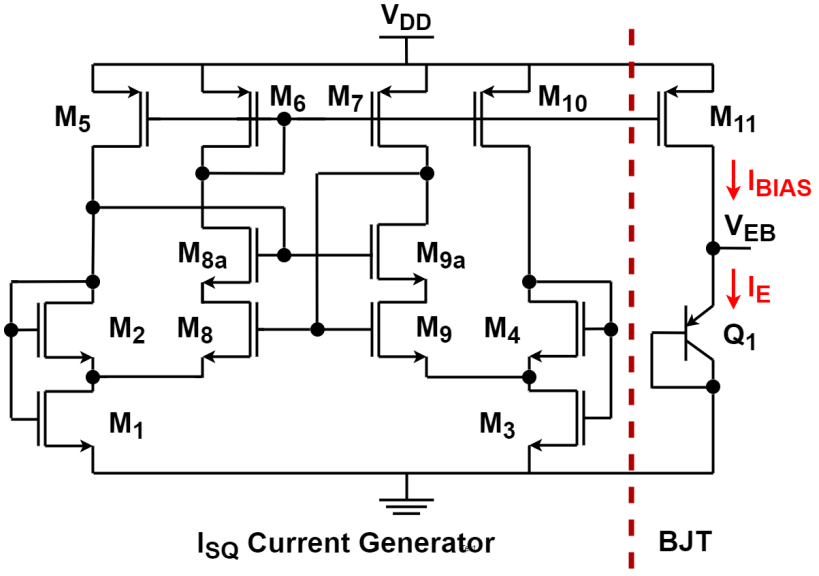
From (4.3) $I_{BIAS} = 9I_{SQ}S_2$ and according to (3.11) $V_X = 76mV$. The $M_1 - M_2$ pair needs to generate a PTAT voltage with 76 mV, and by choosing a value for I_{BIAS} it is possible to generate the desired current that is proportional to I_{SQ}. This 76 mV is applied into the intermediate node (V_Y) of the other SCM, composed by M_3 and M_4. Then, transistors $M_6 - M_7$ are a current mirror and $M_8 - M_9$ forms a self-biasing voltage-following current-mirror. $M_3 - M_4$ are under weak inversion operation and are designed

to generate a PTAT voltage of 76 mV, following (3.8) and (3.9). The current mirrors formed by M_5, M_6, M_7, M_{10}, and M_{11} are unity-gain to reduce the power consumption and the Q_1 transistor has a 2 x 2 μm^2 of emitter area. The self-biased current source was developed to achieve a $I_{BIAS} = 3.2\ n$A. Table 4.1 presents the transistors sizes of the circuit and Fig. 4.3 shows the proposed biasing BJT circuit.

Table 4.1: Dimensions of the MOSFETs.

Transistor	i_f	$W(\mu m)$	$L(\mu m)$
M_1	28	0.3	6*20
M_2	9.3	0.3	6*20
M_3	0.17	2*3	20
M_4	0.012	4*10	20
M_5	0.12	10	15
M_6	0.12	10	15
M_7	0.12	10	15
M_8	0.17	3*5	15
M_{8a}	0.17	3*5	15
M_9	0.17	3*5	15
M_{9a}	0.17	3*5	15
M_{10}	0.12	10	15
M_{11}	0.12	10	15

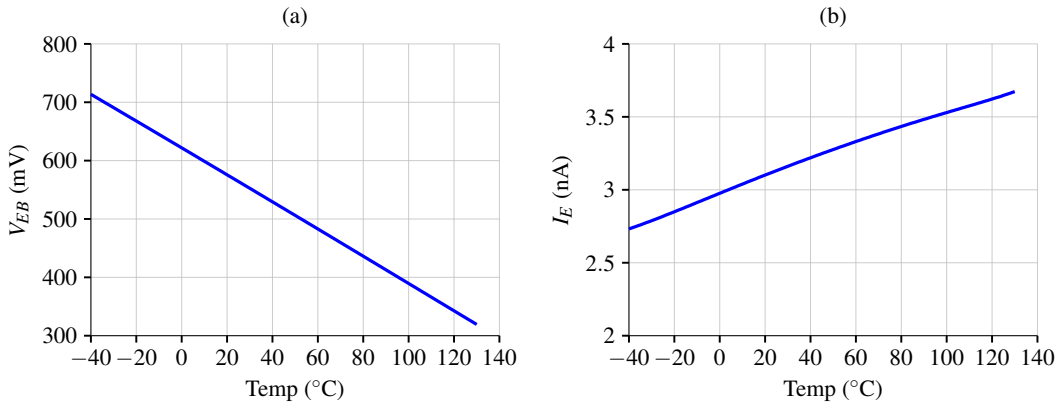
Figure 4.3: I_{SQ} current generator used to bias the Q_1 BJT.



Source: Author.

This I_{SQ} BJT biasing was implemented in TSMC 180 nm process and simulated to compare its performance with the BJT bias discussed in Chapter 3 that was proposed by MATTIA; KLIMACH; BAMPI (2014). The results presented here are from schematic only simulations with a $V_{DD} = 1.8V$. The temperature behavior of the generated V_{EB} is shown in Fig. 4.4(a), from -40 to 130 °C. The I_E current temperature dependence is shown in Fig. 4.4(b).

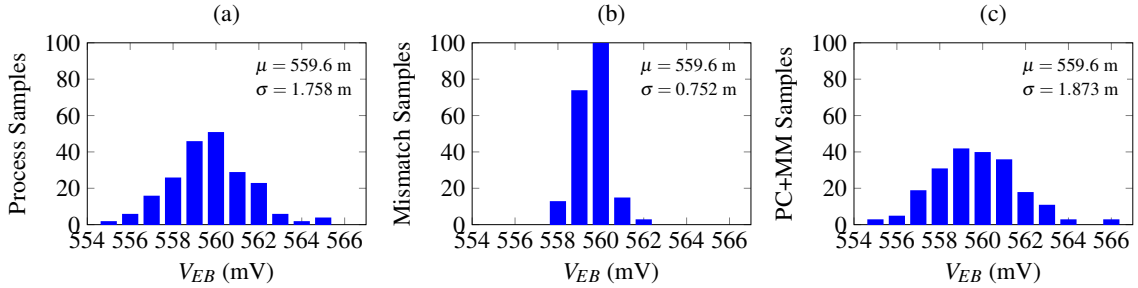
Figure 4.4: (a) V_{EB} voltage and (b) I_E current over temperature.



Source: Author.

To analyze the fabrication variability of this topology, Monte Carlo simulations with 200 runs were performed for local mismatch effects and average process variations. The nominal V_{EB} voltage at 27°C histograms are presented in Fig. 4.5, where μ is the mean value and σ the standard deviation. Considering process variations only, the V_{EB} variability coefficient σ/μ resulted in 0.31%, considering mismatch only resulted in 0.13%, and both effects combined resulted in 0.33%.

Figure 4.5: MC simulations histograms of V_{EB} voltage at 27°C. Average process variation on (a); Local mismatch on (b); Combined on (c).



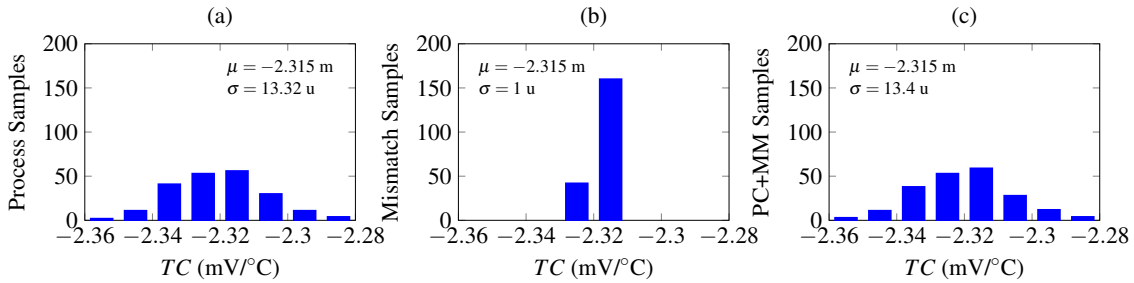
Source: Author.

The temperature coefficient histograms of this generated CTAT voltage are presented in Fig. 4.6. MC simulations show the variability impact in the accuracy of the V_{EB} voltage slope. Considering process variations only, the TC variability coefficient resulted in 0.57%, considering mismatch only resulted in 0.043%, and both effects combined resulted in 0.58%.

Table 4.2 shows a result comparison considering the two different structures for biasing the p-n junction. As presented in the circuit analysis and according to (4.1), the V_{EB} generated with the I_{SQ} current is independent of V_{T0}. Therefore, this CTAT generator with an I_{SQ} current source is less sensitive to process variations than the other biasing circuit.

This self-biased I_{SQ} current source has two DC operating points, one is the desired I_{BIAS}, and the other one is where all internal currents are zero. Then, a start-up circuit is needed to avoid the zero-current condition. A start-up circuit presented in GOMEZ et al. (2015) was implemented, as shown in Fig. 4.7.

Figure 4.6: MC simulations histograms of TC. Average process variation on (a); Local mismatch on (b); Combined on (c).



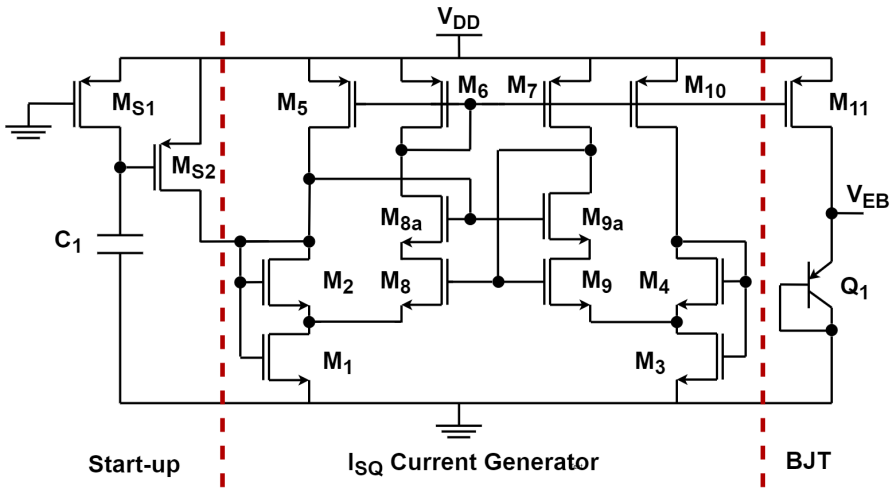
Source: Author.

Table 4.2: Performance comparison of BJT biasing in 180 nm CMOS at V_{DD} = 1.8V.

Parameter	BJT Bias [1]	I_{SQ} BJT Bias	Unit
I_E	3.6	3.2	nA
Temp. Range	-40 -130	-40 -130	°C
V_{EB}			
μ	563.1	559.6	mV
σ	12.65	1.873	mV
σ/μ	2.25	0.33	%
TC_{CTAT}			
μ	-2.273	-2.315	mV/°C
σ	18.29	13.4	uV/°C
σ/μ	0.80	0.58	%

[1] MATTIA; KLIMACH; BAMPI (2014);

Figure 4.7: BJT with I_{SQ} current source and start-up circuit.



Source: Author.

Considering that the capacitor C_1 discharged when the supply voltage starts to increase. Then M_{S2} drives current into the SCM composed by M_1 and M_2 to initialize the circuit. At the same time, M_{S1} delivers current to C_1 which leads to changing M_{S1} to deep triode operation and M_{S2} to the cut-off region. The currents through M_{S1} and M_{S2} are

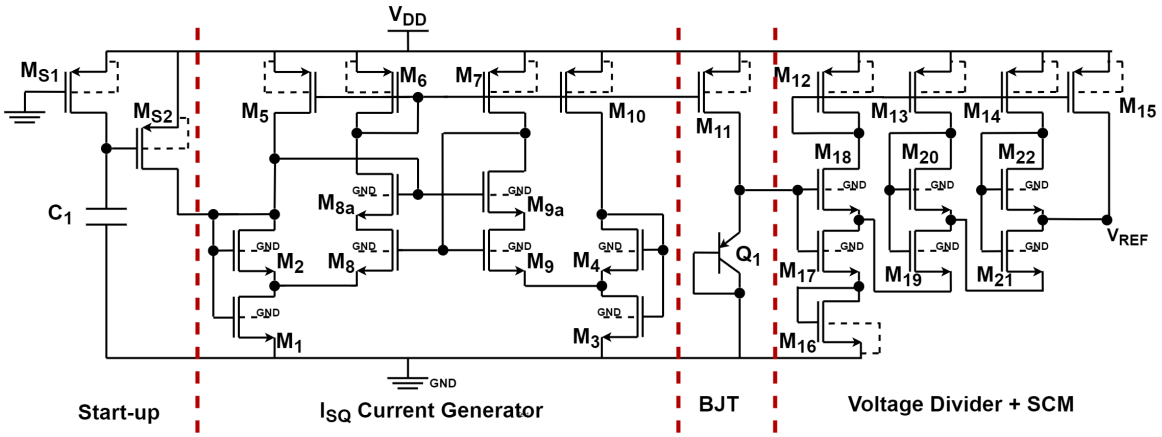
approximate zero during the circuit operation due to the loaded C_1 capacitance because it forces the drain voltage of M_{S1} and the gate voltage of M_{S2} to be zero. This is important because it does not result in extra current consumption.

In the next sections, two voltage references are proposed, considering the improvements in the CTAT voltage generator achieved by this I_{SQ} biasing BJT circuit.

4.2 Sub-Bandgap Reference with Self-Cascode MOSFETs

The proposed sub-bandgap reference with SCMs (SBSCM) schematic is shown in Fig. 4.8. The CTAT voltage is generated through a self-biased I_{SQ} current source that bias the BJT. Transistors $M_{16} - M_{22}$ form a voltage divider and a PTAT generator circuit. As presented in Fig. 4.8, the first stage of the SCM is combined with the voltage divider to reduce power consumption.

Figure 4.8: Schematic of the proposed SBSCM reference circuit.



Source: Author.

Analyzing Fig. 4.8, $V_{EB} = V_{G18} = V_{G17}$, $I_{D16} = I_{D17}$, considering S_{16} = S_{17}, and from (3.4), the gate-source voltage M_{16} is given by (4.4). Then, the CTAT voltage V_{EB} appears divided by approximately 2.3 ($n \approx 1.3$ for WI) at the gate of M_{16}.

$$V_{GS16} \approx \frac{V_{EB}}{n+1} \tag{4.4}$$

The PTAT voltage is generated through a cascaded SCM structure. Since each SCM cell of this topology presents different current densities and from (3.2), the SCM output voltage can be expressed as

$$V_{DS,lower} = \phi_T \, ln\left(\frac{I_{D,lower}}{I_{D,upper}}\frac{S_{upper}}{S_{lower}} + 1\right) \tag{4.5}$$

where the lower transistors are M_{17}, M_{19}, and M_{21}. M_{18}, M_{20}, and M_{22} are upper transistors.

The total PTAT voltage is the sum of the drain-source voltage of M_{17}, M_{19}, and M_{21}, as shown in (4.6). Therefore, to adjust the PTAT voltage of the cascaded structure, (4.6) can be rewritten as (4.7)

$$V_{PTAT} = V_{DS17} + V_{DS19} + V_{DS21} \tag{4.6}$$

$$V_{PTAT} = \phi_T \, ln \left[\left((K_{15,12} + 3)\frac{S_{18}}{S_{17}} + 1 \right) \left((K_{15,12} + 2)\frac{S_{20}}{S_{19}} + 1 \right) \left((K_{15,12} + 1)\frac{S_{22}}{S_{21}} + 1 \right) \right] \tag{4.7}$$

where $K_{15,12}$ is the aspect ratio relation of M_{15} and M_{12} (i.e. $K_{15,12} = (W_{15}/W_{12})$ (L_{12}/L_{15})).

The reference voltage V_{REF} , at the drain of M_{21}, is the sum of a CTAT term given by (4.4) and the PTAT term given by (4.7), thus:

$$V_{REF} = \frac{V_{EB}}{n+1} + V_{PTAT} \tag{4.8}$$

4.2.1 Design Methodology of the PTAT Voltage Generator

In the previous section the bipolar transistor with I_{SQ} current source was designed and the generated CTAT voltage is represented by (4.4). Thus, the temperature sensitivity of (4.8) can be calculated. The condition that reduces this sensitivity to zero provides the PTAT voltage slope, that is used to size the cascaded SCM structure. The CTAT voltage temperature sensitivity was estimated by simulation as -1 mV/°C, meaning that a PTAT voltage slope of approximately +1 mV/°C is necessary to counterbalance it. Thus, differentiating (4.7) with respect to temperature and then equating it to the desired PTAT voltage slope results in the aspect ratios values of the SCM circuit.

From (4.7), one can choose the constant design factors as $S_{17} = 1.5$ and $S_{18} = 40$ to provide a higher PTAT voltage slope in the first SCM stage, for $M_{17} - M_{18}$ pair to operate in weak inversion, and $M_{17} - M_{18}$ sizes to allow transistor splitting and interdigitation in the layout. The second and third SCM stages have equal sizing for simplicity and the design constants are $S_{19} = 0.17$, $S_{20} = 1.4$, $S_{21} = 0.17$, and $S_{22} = 1.4$ to generate the desired voltage slope of +1 mV/°C. $M_{19} - M_{20}$ and $M_{21} - M_{22}$ operate in weak inversion and are also sized to allow a good transistor matching. Following (4.7), the value of $K_{15,12} = 2$ was implemented to adjust the PTAT voltage to provide sufficient gain for the SCM cells to achieve the desired PTAT slope. Then, it is possible to estimate the W and L of the PTAT structure transistors. The aspect ratios of the PMOS current mirrors $M_{12} - M_{15}$ are designed to guarantee that all transistors are kept in saturation and for a low current consumption. Table 4.3 presents the transistors sizes of the circuit after simulation adjustments.

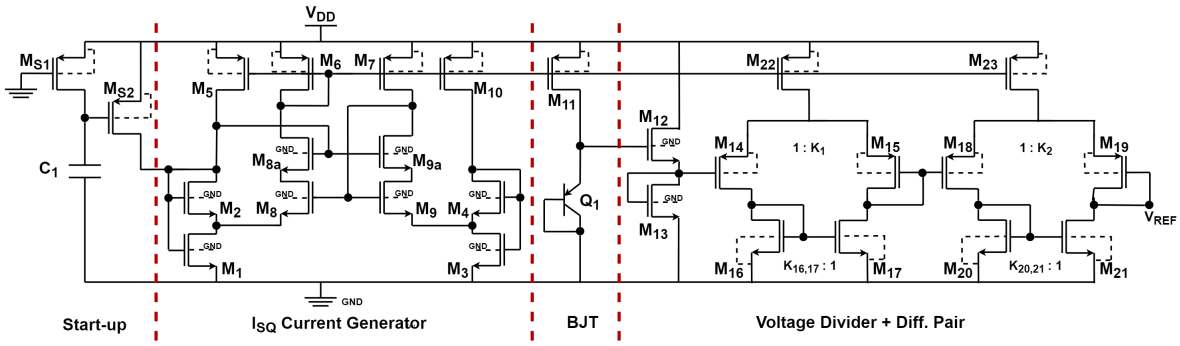
4.3 Sub-Bandgap Reference with Unbalanced Differential Pair

Another topology employing a different voltage divider and ϕ_T generator circuit was implemented. This circuit was designed for a comparison purpose, to understand which PTAT structures in a voltage reference circuit showed less voltage deviations due to variability. The proposed sub-bandgap reference with an unbalanced differential pair (SBDF) is shown in Fig. 4.9. The CTAT voltage is again produced through a self-biased I_{SQ} current generator that biases the BJT. Transistors $M_{12} - M_{13}$ form the V_{EB} voltage divider and $M_{14} - M_{23}$ the PTAT generator circuit. The I_{D10} current generated by the I_{SQ} current source is mirrored to bias the rest of the circuit through PMOS transistors M_5, M_6, M_7, M_{10}, M_{22}, and M_{23}.

Table 4.3: Dimensions of the MOSFETs.

Transistor	i_f	$W(\mu m)$	$L(\mu m)$
M_{12}	0.087	4	15
M_{13}	0.087	4	15
M_{14}	0.087	4	15
M_{15}	0.087	2*4	15
M_{16}	0.021	3	2
M_{17}	0.079	3	2
M_{18}	0.00016	13*6	2
M_{19}	0.0048	1	6
M_{20}	0.16	8*1	6
M_{21}	0.0048	1	6
M_{22}	0.12	8*1	6

Figure 4.9: Schematic of the proposed SBDF reference circuit.



Source: Author.

The output voltage of the voltage divider can be calculated as

$$V_{GS13} = \frac{V_{EB}}{M} \tag{4.9}$$

where M is the division ratio. $S_{12} = S_{13}$ is applied to obtain $M = 2$. Then, the CTAT voltage appears divided by approximately 2 at the gate of M_{13}.

The PTAT voltage is generated through a cascaded unbalanced differential pair structure. From (4.3), since $I_{D10} = I_{BIAS}$, and considering (3.14), the PTAT output voltage can be expressed as

$$V_{G15} = n\phi_T \left[F\left(\frac{K_1 K_{16,17} K_{22,10}}{(1+K_{16,17}) S_{15} S_2 i_{f2}} \right) - F\left(\frac{K_{22,10}}{(1+K_{16,17}) S_{15} S_2 i_{f2}} \right) \right] \tag{4.10}$$

$$V_{G19} = n\phi_T \left[F\left(\frac{K_2 K_{20,21} K_{23,10}}{(1+K_{20,21}) S_{19} S_2 i_{f2}} \right) - F\left(\frac{K_{23,10}}{(1+K_{20,21}) S_{19} S_2 i_{f2}} \right) \right] \tag{4.11}$$

where K_1, K_2, $K_{16,17}$, $K_{20,21}$, $K_{22,10}$, and $K_{23,10}$ are the aspect ratio relationships between $M_{15} - M_{14}$, $M_{19} - M_{18}$, $M_{16} - M_{17}$, $M_{20} - M_{21}$, $M_{22} - M_{10}$, and $M_{23} - M_{10}$, respectively.

Both of unbalanced differential pairs present the same sizing, then the generated PTAT voltage is two times the gate voltage of M_{G15} or M_{G19}. Therefore, the PTAT voltage of the cascaded structure can be rewritten as (4.12).

$$V_{PTAT} = 2n\phi_T \left[F\left(\frac{K_1 K_{16,17} K_{22,10}}{(1+K_{16,17}) S_{15} S_2 i_{f2}} \right) - F\left(\frac{K_{22,10}}{(1+K_{16,17}) S_{15} S_2 i_{f2}} \right) \right] \quad (4.12)$$

The reference voltage V_{REF}, at the gate voltage of M_{19}, is the sum of the CTAT term given by (4.9) and the PTAT term given by (4.12), thus:

$$V_{REF} = \frac{V_{EB}}{2} + V_{PTAT} \quad (4.13)$$

4.3.1 Design Methodology of the PTAT Voltage Generator

The temperature sensitivity of (4.13) can be expressed through its derivative. The condition that reduces this sensitivity to zero provides the PTAT voltage slope, which is used to size the unbalanced differential pair cell. The V_{EB}/2 voltage temperature sensitivity was estimated by simulation as -1.1 mV/°C, meaning that a PTAT voltage slope of approximately +1.1 mV/°C is necessary to counterbalance it. Thus, differentiating (4.12) with respect to temperature and then equating it to the desired PTAT voltage slope results in the aspect ratios values of the PTAT circuit.

From (4.12), one can choose the constant design factors as $K_1 = 13$ and $K_{16,17} = 10$ to provide a high PTAT voltage slope and to allow transistor splitting. $S_{15} = 0.7$ was implemented to adjust the voltage slope to +1.1 mV/°C. Also, a value of $K_{22,10} = 0.6$ was used to reduce the current consumption of the PTAT branches. Then, it is possible to estimate the sizing of each MOSFET in the design. Table 4.4 presents the transistors sizes of the circuit after simulation adjustments.

Table 4.4: Dimensions of the MOSFETs.

Transistor	i_f	$W(\mu m)$	$L(\mu m)$
M_{12}	0.051	1	10
M_{13}	0.051	1	10
M_{14}	0.80	1	18
M_{15}	0.0073	13*1	18
M_{16}	0.012	10*1	10
M_{17}	0.014	1	10
M_{18}	0.80	1	18
M_{19}	0.0073	13*1	18
M_{20}	0.012	10*1	10
M_{21}	0.014	1	10
M_{22}	0.125	6	15
M_{23}	0.125	6	15

4.4 Single-trimming Strategy

Voltage reference circuits are used as a reference for applications such as ADCs, DACs, and voltage regulators. These applications exhibit some level of overall error

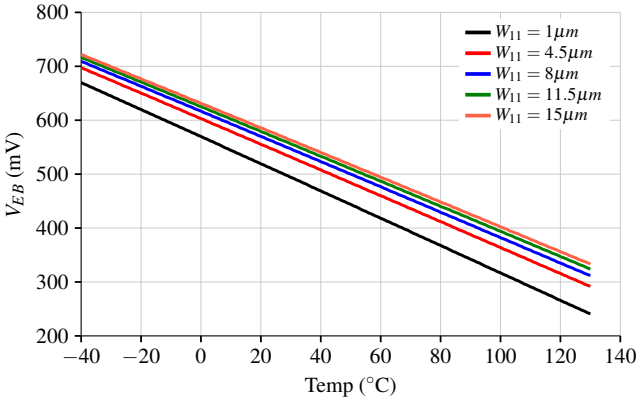
which requires, for example, zero-scale and full-scale calibrations. Then, it is possible to trim the V_{REF} voltage with these calibrations. However, it is also necessary to reduce the temperature sensitivity of the reference voltage. Thus, a trimming technique is proposed to reduce the TC of the reference voltage. From Fig. 4.9, Fig. 4.8, and (4.1), the V_{EB} voltage can be rewritten as

$$V_{EB} = m\phi_T \left[ln \left(\frac{K_{11,10} I_{SQ}}{I_{SE} S_2 i_{f2}} \right) \right] \tag{4.14}$$

where $K_{11,10}$ is the the aspect ratio relations of $M_{10} - M_{11}$ (i.e. $K_{11,10} = S_{11}/S_{10}$) and m is the bipolar slope factor. Thus, by modifying the current gain $K_{11,10}$ it is possible to change the V_{EB} voltage. Also, different $\partial V_{EB}/\partial T$ derivatives can be generated (TSIVIDIS, 1980).

To understand and visualize this relation between $K_{11,10}$ and the bipolar transistor, a simulation was done with the I_{SQ} BJT biasing circuit. Fig. 4.10 shows the V_{EB} voltage over temperature considering distinct sizes of W_{11}, since $K_{11,10}$ modifies with changes in W_{11}. Table 4.5 presents the V_{EB} and $\partial V_{EB}/\partial T$ values for W_{11} sizes, and Fig. 4.11 plots the V_{EB} voltage at $27°C$ over W_{11}.

Figure 4.10: V_{EB} voltage over temperature with different W_{11}.



Source: Author.

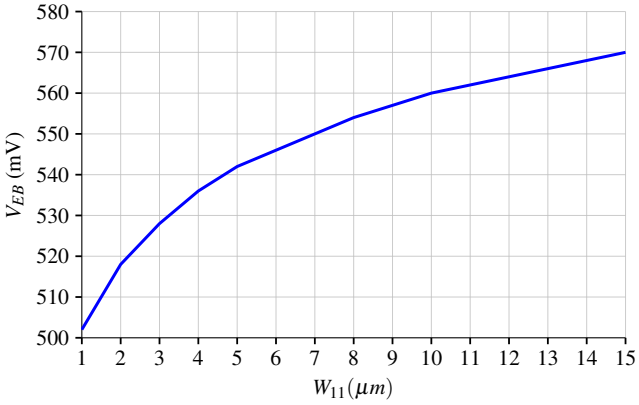
Table 4.5: V_{EB} and $\partial V_{EB}/\partial T$ comparison for different W_{11} sizes.

$W_{11}(\mu m)$	V_{EB} at $27°C$ (mV)	$\partial V_{EB}/\partial T$ (mV/$°C$)
1	501.63	-2.52
4.5	538.73	-2.38
8	553.71	-2.33
11.5	563.09	-2.30
15	569.90	-2.28

Complex trimming techniques generally increase the calibration time, leading to a high production cost of the circuit. Then, to develop a trimming scheme that can easily calibrate the device and with low power consumption is a fundamental strategy for a cost-efficient voltage references.

The idea of the proposed trimming circuit is to use the BJT biasing current to modify the CTAT voltage slope of the generated V_{EB} voltage. Then, the relation between the

Figure 4.11: V_{EB} voltage at 27°C over W_{11}.



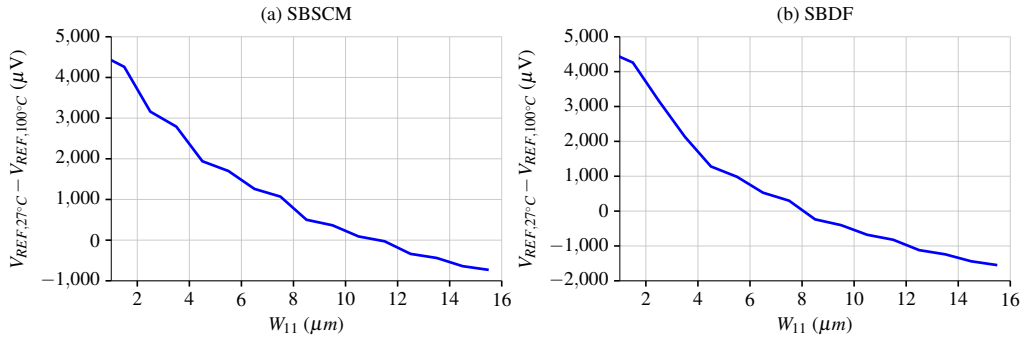
Source: Author.

current gain $K_{11,10}$ and the V_{EB} voltage is used to improve the temperature sensitivity performance of the sub-bandgap circuit. The strategy is to implement a **single-trim** because to trim the device the transistor M_1 is individually adjusted considering only two different temperatures (27 °C and 100 °C). Thus, this strategy represents a fast and simple calibration procedure.

Simulating both voltage references and modifying $K_{11,10}$, with changes in W_{11}, the V_{EB} voltage changes and, consequently, the reference voltage is modified. Then, there is a relation with the measured difference of the V_{REF} voltage at 27 °C and 100 °C ($\Delta V_{REF(27,100°C)} = V_{REF,27°C} - V_{REF,100°C}$) and the W_{11} value, as shown in Fig. 4.12. It is not a linear association however it can be approximated through a polynomial extrapolation of third order.

Considering changes in W_{11}, it was also analyzed that the voltage references TCs have an almost linear relation with the $\Delta V_{REF(27,100°C)}$, as shown in Fig. 4.13. Thus, by measuring the reference voltage in both temperatures, it is possible to estimate the TC and recognize which sample needs to be trimmed. Then, as shown in Fig. 4.12, with a polynomial equation and the $\Delta V_{REF(27,100°C)}$ it is possible to calculate the W_{11} value.

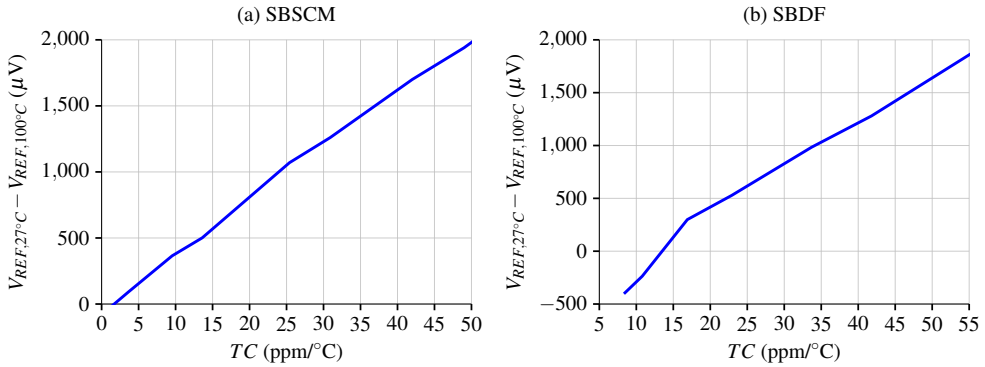
Figure 4.12: $\Delta V_{REF(27,100°C)}$ over W_{11}



Source: Author.

From 200 samples of MC simulations considering mismatch and process variability, the difference of the maximum and minimum $\Delta V_{REF(27,100°C)}$ achieved was approximately 2.4 mV and 3.4 mV for SBSCM and SBDF, respectively. As shown in Fig. 4.12(a), by changing W_{11} from 5 to 15 μm this range of 2.4 mV is reached. In Fig. 4.12(b), by modifying W_{11} from 3 to 15 μm this range of 3.4 mV is achieved. Thus, by increasing

Figure 4.13: $\Delta V_{REF(27,100°C)}$ over TC.



Source: Author.

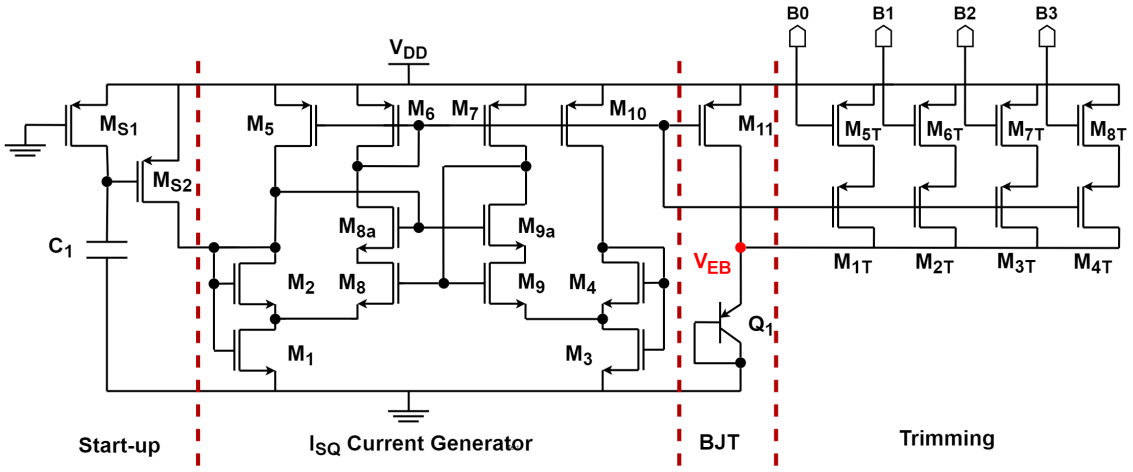
or decreasing 12 μm of W_{11} it is possible to cover the variations of the $\Delta V_{REF(27,100°C)}$ considering the worst-case range generated by the MC simulations of both circuits.

A digital controlled binary-weighted aspect ratio adjustment is implemented in parallel of M_{11} to modify W_{11}. The number of bits can be calculated by (4.15) (BRITO; BAMPI; KLIMACH, 2007)

$$Bits \geq \frac{ln\left(\frac{V_{FS}}{V_{LSB}}\right) + 1}{ln(2)} \tag{4.15}$$

where V_{LSB} is the least significant bit and V_{FS} is the full-scale voltage. V_{FS} equals 3.4 mV to cover both circuits entire voltage variation. Since a variation of at least 12 μm is needed and we choose each trimming code to vary 1 μm, the V_{LSB} equals 284 μV. Then, a 4 bit code is required to trim the circuit. Fig. 4.14 shows the BJT bias circuit with the proposed trimming scheme and Table 4.6 presents the transistors sizes of the trimming strategy.

Figure 4.14: BJT biasing circuit with a trimming structure.



Source: Author.

Table 4.7 shows the trimming codes of the circuit and its respective W_{11} modifications. To discover which trimming code must be inserted to calibrate the TC, it is necessary to use an equation that is generated through the polynomial fitting of the curves presented

Table 4.6: Dimensions of the MOSFETs.

Transistor	$W(\mu m)$	$L(\mu m)$
M_{11}	0.5	15
M_{1T}	1	15
M_{2T}	2	15
M_{3T}	4	15
M_{4T}	8	15
M_{5T-8T}	1	1

in Fig. 4.15. The equation of the sub-bandgap with SCM is presented in (4.16), and the equation for the SBDF is expressed in (4.17). From these equations, a Matlab code (Appendix C) was created to calculate the exactly binary code to apply on the digital bits.

$$T_{SBSCM} = 9.9{*}10^{-11}\Delta V^3_{REF(27,100°C)} - 1{*}10^{-6}\Delta V^2_{REF(27,100°C)} + 0.004\Delta V_{REF(27,100°C)} + 4.4 \tag{4.16}$$

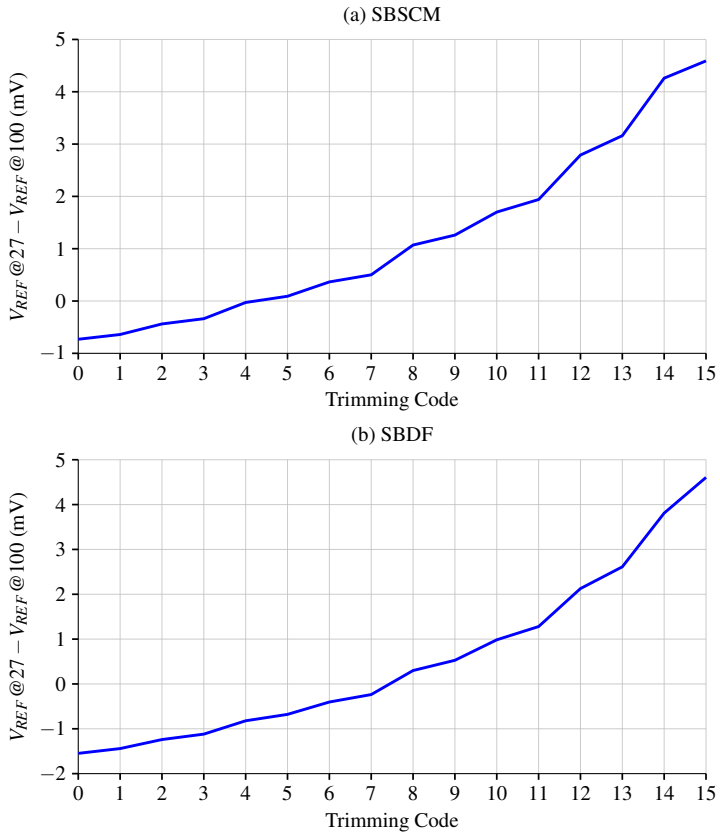
$$T_{SBDF} = 7.1{*}10^{-11}\Delta V^3_{REF(27,100°C)} - 7{*}10^{-7}\Delta V^2_{REF(27,100°C)} + 0.003\Delta V_{REF(27,100°C)} + 7.5 \tag{4.17}$$

Table 4.7: Trimming code associated to a binary word.

Trim Code	Binary Code (B3 B2 B1 B0)	W_{11} Equivalent Sizing (μm)
0	0 0 0 0	15.5
1	0 0 0 1	14.5
2	0 0 1 0	13.5
3	0 0 1 1	12.5
4	0 1 0 0	11.5
5	0 1 0 1	10.5
6	0 1 1 0	9.5
7	0 1 1 1	8.5
8	1 0 0 0	7.5
9	1 0 0 1	6.5
10	1 0 1 0	5.5
11	1 0 1 1	4.5
12	1 1 0 0	3.5
13	1 1 0 1	2.5
14	1 1 1 0	1.5
15	1 1 1 1	0.5

Finally, by measuring the V_{REF} at 27 °C and then at 100 °C, it is possible to estimate the TC of the sample and also define the digital bits for the calibration. The trimming procedures are detailed in a flowchart, presented in Appendix D. The proposed trimming strategy presents a fast and straightforward procedure to improve TC performance. More-

Figure 4.15: $V_{REF,27°C} - V_{REF,100°C}$ voltage versus trimming code.



Source: Author.

over, this trimming circuit offers a very low power consumption, which is exhibited in the next Chapter.

5 SIMULATION RESULTS

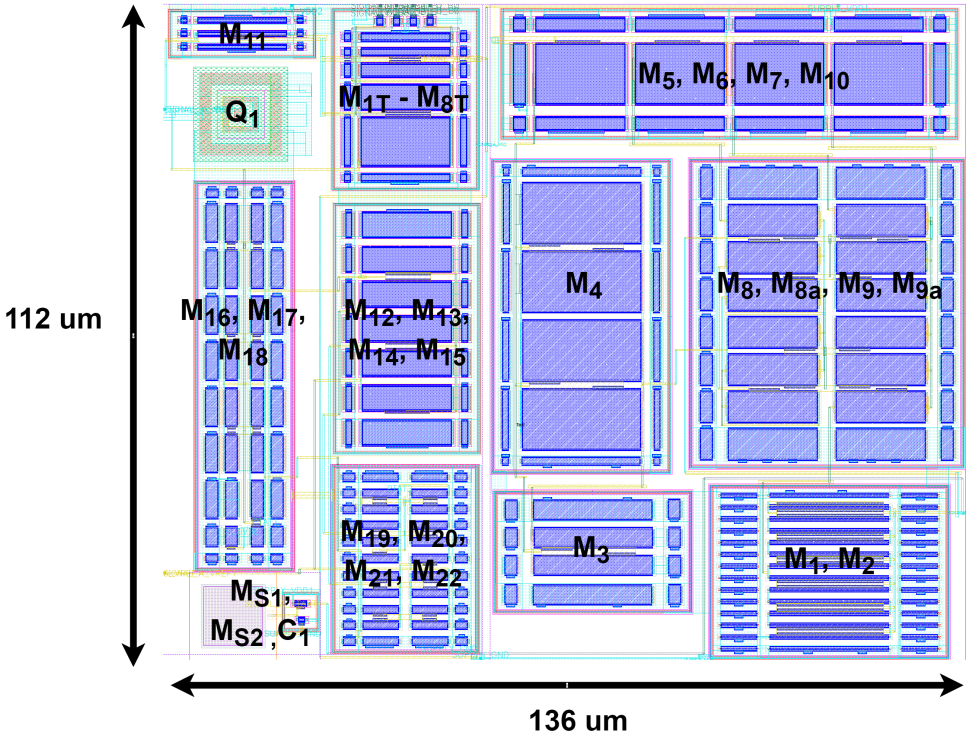
The results presented here were obtained for post-layout simulations performed by the Cadence Virtuoso™ Spectre™ electrical simulator. The circuits were implemented in TSMC 180 nm process using standard threshold voltage NMOS and PMOS transistors. The layout was done applying good layout practices, such as: creating a floorplan before implementing the layout, dummy structures, guard-rings, transistors splitting, and interdigitation of transistors.

The proposed sub-bandgap with SCMs was sent to fabrication through the IMEC/TSMC Mini@sic Incentive Program for Brazilian Universities. However, we expect to receive the chips only in the beginning of 2021.

5.1 Sub-Bandgap Reference with Self-Cascode MOSFETs

The layout of the sub-bandgap with SCMs is shown in Fig. 5.1. The occupied silicon area is 0.0154 mm^2.

Figure 5.1: Sub-bandgap with SCMs layout.

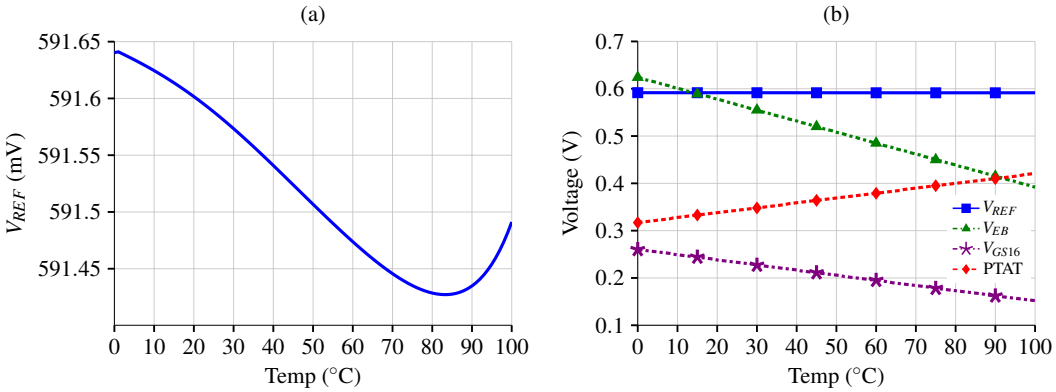


Source: Author.

The voltage reference obtained is around 591.6 mV, as shown in Fig. 5.2(a). The typical temperature coefficient, as given by (2.1), is 3.6 ppm/°C for the 0 to 100 °C temperature range, with a 1.8 V of supply voltage. The voltage reference temperature range was shortened compared to the PTAT and CTAT simulations because the previous analysis of those circuits showed that the generated PTAT and CTAT voltages suffer from non-linearities at temperature extremes.

The temperature behavior of the PTAT and CTAT voltages are shown in Fig. 5.2(b), both these voltages are added to form the temperature independent V_{REF}.

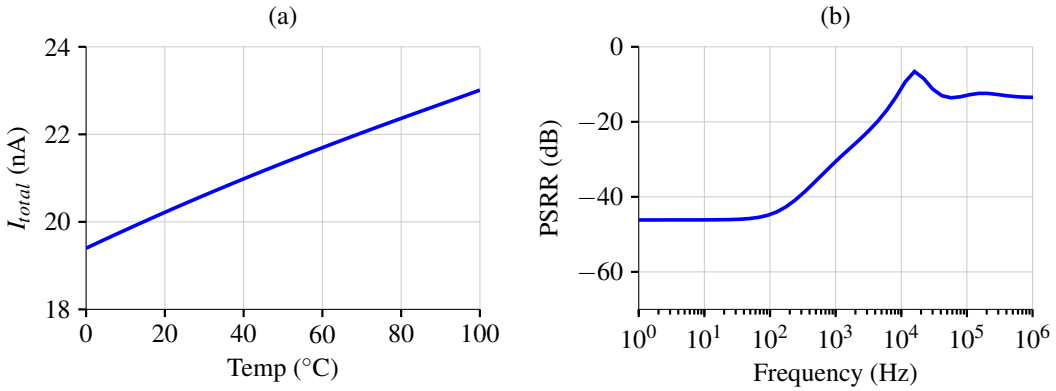
Figure 5.2: (a) V_{REF}; (b) V_{REF} , V_{EB}, V_{GS16}, and PTAT voltages over temperature.



Source: Author.

In Fig. 5.3(a) the total current (I_{total}) of the circuit over the 0 to 100 °C temperature range is presented. The current consumption at 27 °C for the whole circuit is 20.5 nA, reaching a maximum of 23 nA at 100 °C. This results in a power consumption of 36.9 nW and 41.4 nW respectively, for a 1.8 V supply.

Figure 5.3: (a) I_{total} over temperature; (b) PSRR over frequency.

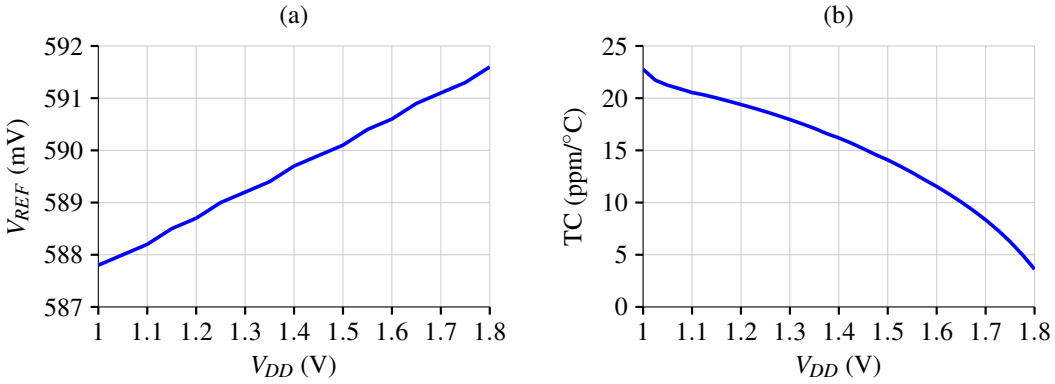


Source: Author.

The power supply rejection ratio is presented in Fig. 5.3(b) and shows -44.7 dB at 100 Hz for V_{DD} = 1.8 V. The line sensitivity obtained for V_{DD} ranging from 1 V to 1.8 V is 0.8 %/V at 27 °C, as shown in Fig. 5.4(a). Although the nominal supply voltage of the implemented process is 1.8 V, this circuit starts operating at 1 V with a voltage reference TC of 23 ppm/°C, as presented in Fig. 5.4(b).

The start-up behavior of the circuit was simulated to obtain the settling time of the reference voltage, as shown in Fig. 5.5. The circuit presents a settling time of approximately

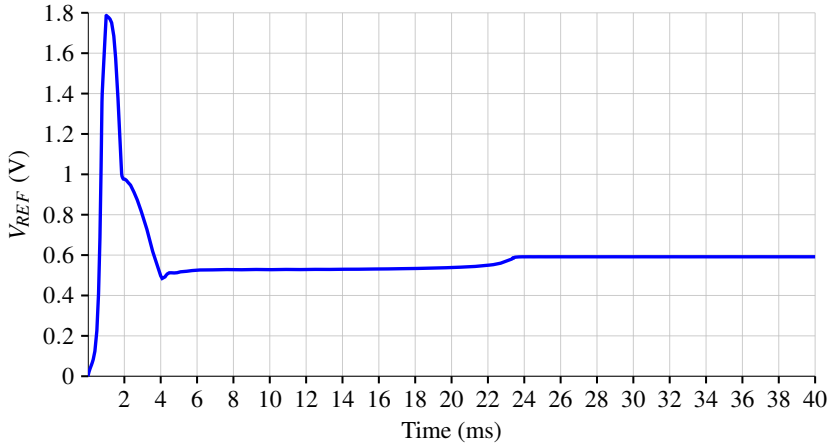
Figure 5.4: (a) LS; and (b) TC over power supply.



Source: Author.

24 ms, which is acceptable for this type of circuit.

Figure 5.5: Start-up behavior.



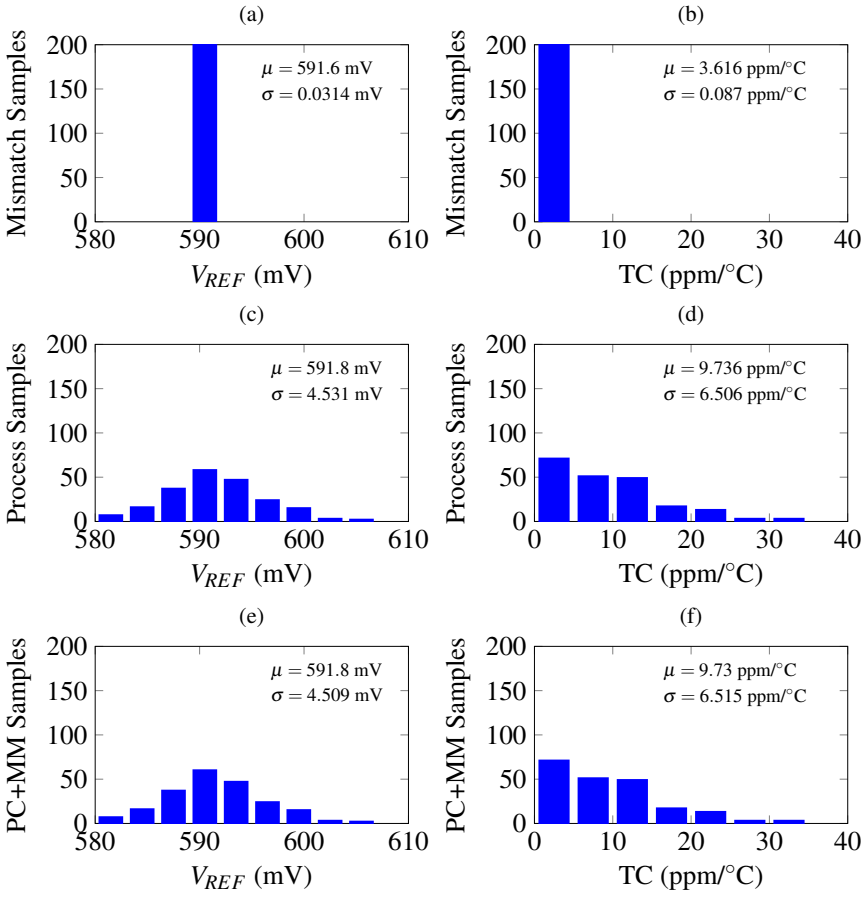
Source: Author.

The sensitivity of the proposed voltage reference to fabrication variability is evaluated through Monte Carlo simulations, where local mismatch effects and average process variations were simulated separately and combined with 200 runs each. The obtained results for V_{DD} = 1.8 V are shown in Fig. 5.6.

Fig. 5.6(a) exhibit the spread of the reference voltage with a $\sigma/\mu = 0.0053\%$ for local mismatch, while for mean process variation, shown in Fig. 5.6(c), yields $\sigma/\mu = 0.76\%$. In Fig. 5.6(e), both types are considered and resulted in a $\sigma/\mu = 0.76\%$. Another significant performance that is affected by fabrication spread is the temperature coefficient, as shown in Fig. 5.6(b), (d), and (f). When local mismatch and average process are considered, the temperature coefficient varies from 1.3 to 31.3 ppm/°C, with an average of 9.7 ppm/°C. Also, in the simulated TC for PC+MM variations, 95% of the runs yield a TC lower than 23.8 ppm/°C.

The circuit achieved a low TC but it is possible to improve the reference voltage temperature sensitivity through the proposed trimming strategy explained in the previous chapter. Considering 200 samples from the MC simulations, for each sample, its reference voltage V_{REF} was simulated at 27°C and 100°C to calculate $\Delta V_{REF(27,100°C)}$. From Fig. 4.13(a), samples with $\Delta V_{REF(27,100°C)} > 400\mu V$ do not present low TC and are the ones

Figure 5.6: V_{REF} and TC Monte Carlo results (untrimmed). Local mismatch on (a) and (b); Average process variation on (c) and (d); Combined on (e) and (f)



Source: Author.

that must be trimmed. Then, 50 among the 200 samples were selected to be trimmed.

Considering these 50 trimmed references within the 200 samples, 95% of the runs yield a TC lower than 13.5 ppm/°C. Moreover, 90% yield a TC lower than 12.2 ppm/°C while the untrimmed circuit reached only 69.5% of the samples with a TC lower than 12.2 ppm/°C.

A histogram comparing the spread of the TC considering the trimmed and untrimmed circuit is shown in Fig. 5.7. Also, Fig. 5.8 plots the reference voltage over the temperature range in 10 samples that reached the highest TCs before and after trimming.

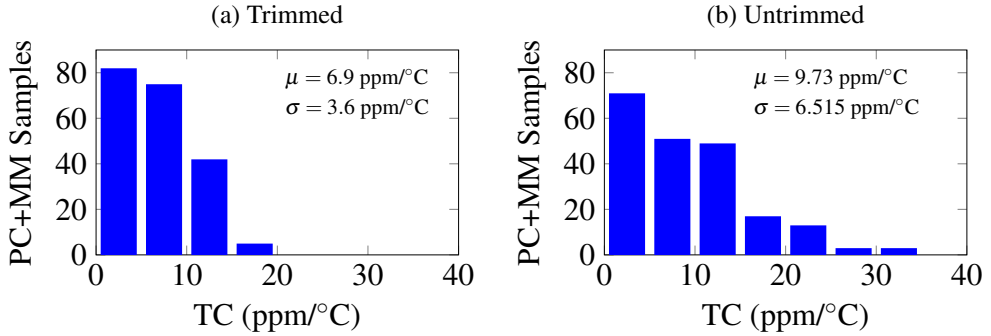
The results are summarized in Table 5.1. The TC is one of the most important metrics of a voltage reference and a very complex parameter to be trimmed. Then, the proposed trimming scheme allowed the circuit to achieve a low TC. The trimming technique improved TC performance while consuming only 3.9 nW. The V_{REF} σ/μ presented a small deviation but not compromising the excellent performance achieved by the reference voltage.

5.2 Sub-Bandgap Reference with Unbalanced Differential Pair

The layout of the sub-bandgap with unbalanced differential pair is shown in Fig. 5.9. The occupied silicon area is 0.022 mm^2.

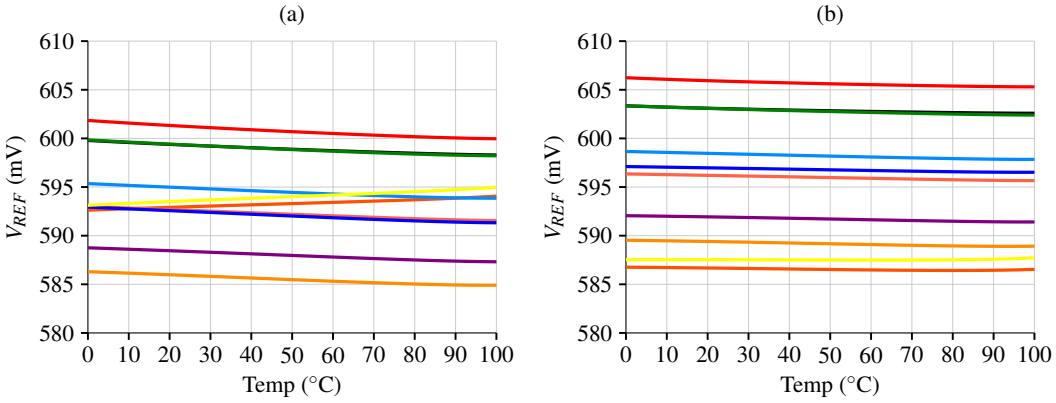
The voltage reference obtained is around 607.4 mV, as shown in Fig. 5.10(a). The

Figure 5.7: Monte Carlo results of TC considering process and mismatch for trimmed and untrimmed circuit.



Source: Author.

Figure 5.8: Temperature dependence of V_{REF} (a) before and (b) after trimming.



Source: Author.

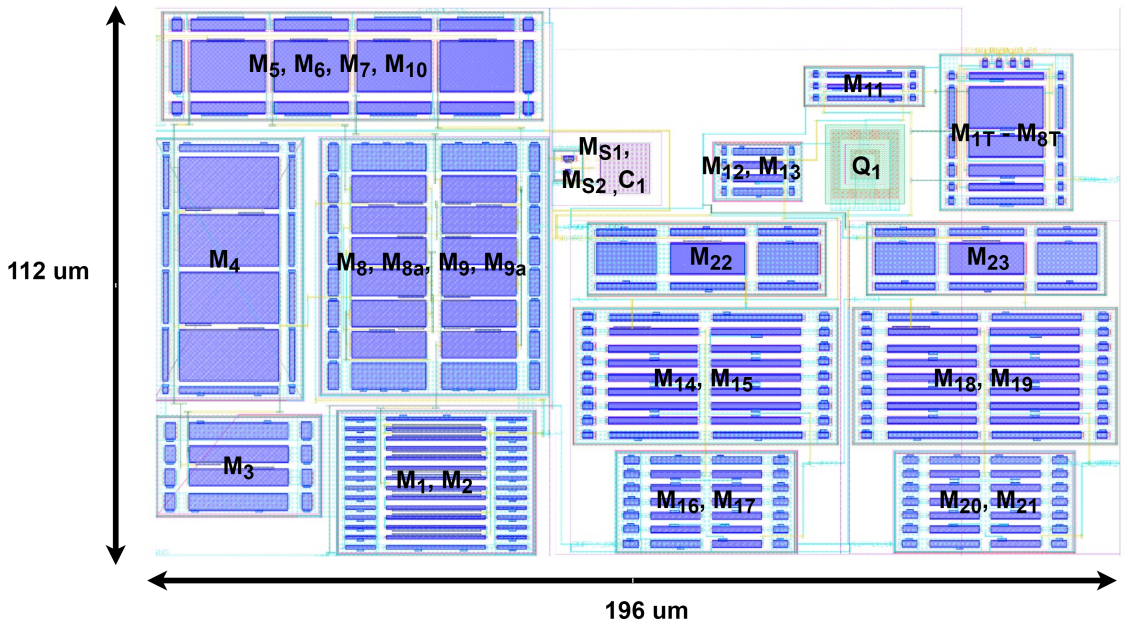
Table 5.1: Performance summary of SBSCM.

Specification	**Untrimmed**	**Trimmed**
Temp. Range (°C)	**0 - 100**	**0 - 100**
V_{DD} (V)	**1 - 1.8**	**1 - 1.8**
V_{REF} (V)	**592.6**	**592**
V_{REF} σ/μ (%)	**0.76**	**0.83**
TC_{avg} (ppm/°C)	**9.7**	**6.9**
TC_{min} (ppm/°C)	**1.3**	**1.3**
TC_{max} (ppm/°C)	**31.3**	**15.9**
LS (%/V)	**0.8**	**0.8**
PSRR@100Hz (dB)	**-44.7**	**-44.7**
Power@V_{DDnom} (nW)	**36.9**	**40.8**

typical temperature coefficient, as given by (2.1), is 8.3 ppm/°C for the 0 to 100 °C temperature range, with a 1.8 V of supply voltage. The temperature range was again reduced due to the CTAT and PTAT non-linearities over temperature. The temperature behavior of the PTAT and CTAT voltages are shown in Fig. 5.2(b).

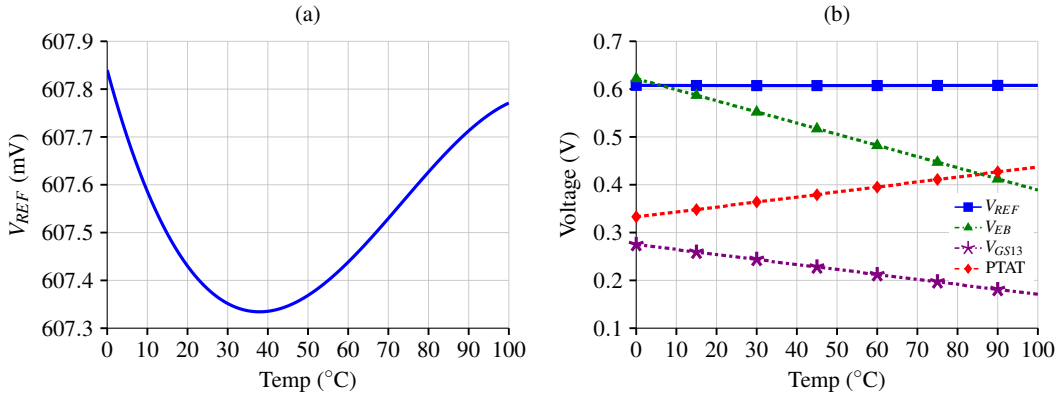
In Fig. 5.11(a) the total current (I_{total}) of the circuit over the 0 to 100 °C temperature range is presented. The current consumption at 27 °C for the whole circuit is 20.2 nA, reaching a maximum of 22.6 nA at 100 °C. This results in a power consumption of 36.4

Figure 5.9: Sub-bandgap with unbalanced differential pair layout.



Source: Author.

Figure 5.10: (a) V_{REF}; (b) V_{REF} , V_{EB}, V_{GS13}, and PTAT voltages over temperature.



Source: Author.

nW and 40.7 nW respectively, for a 1.8 V supply.

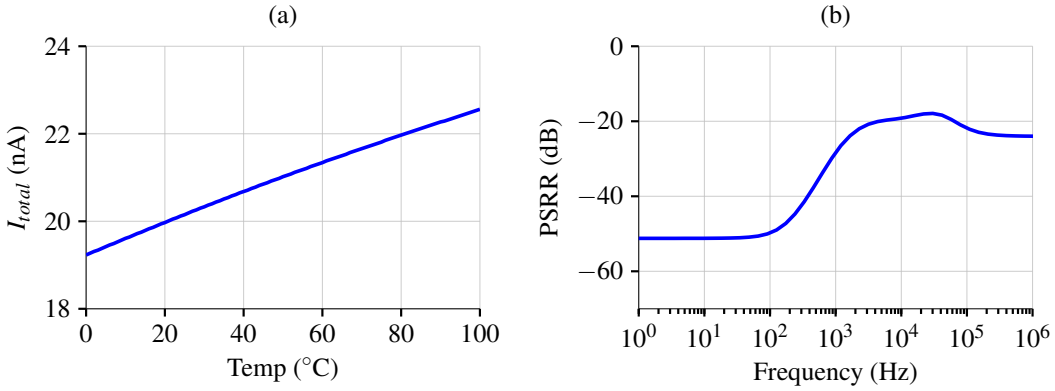
The power supply rejection ratio is reported by Fig. 5.11(b) and shows -49.7 dB at 100 Hz for V_{DD} = 1.8 V. The line sensitivity obtained for V_{DD} ranging from 0.9 V to 1.8 V is 0.46 %/V at 27 °C, as shown in Fig. 5.12(a). Although the nominal supply voltage of the implemented process is 1.8 V, this circuit starts operating at 0.9 V with comparable TC, as presented in Fig. 5.12(b).

The start-up behavior of the circuit was simulated to obtain the settling time of the reference voltage, as shown in Fig. 5.13. The circuit presents a settling time of approximately 25 ms.

The sensitivity of the proposed voltage reference to fabrication variability is evaluated through Monte Carlo simulations, where local mismatch effects and average process variations were simulated separately and combined with 200 runs each. The obtained results for V_{DD} = 1.8 V are shown in Fig. 5.14.

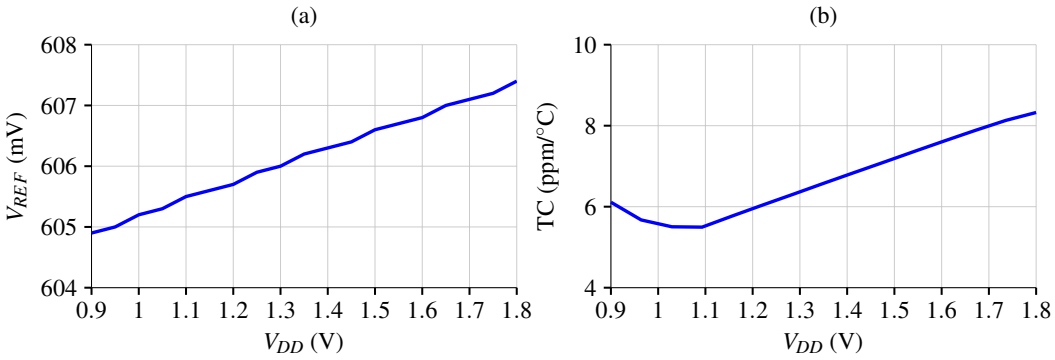
Fig. 5.14(a) exhibit the spread of the reference voltage with a σ/μ = 0.0043% for

Figure 5.11: (a) I_{total} over temperature; (b) PSRR over frequency.



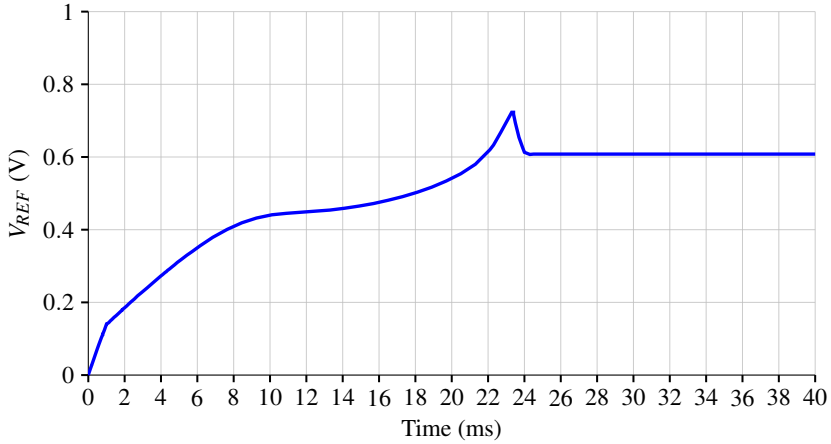
Source: Author.

Figure 5.12: (a) LS; and (b) TC over power supply.



Source: Author.

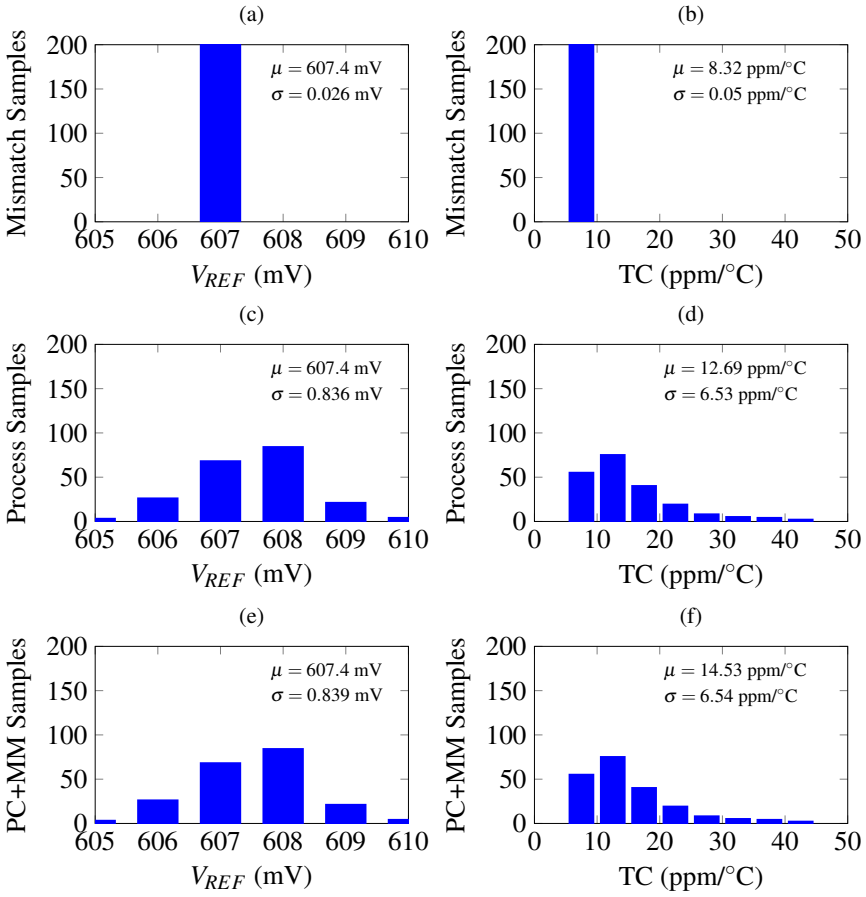
Figure 5.13: Start-up behavior.



Source: Author.

local mismatch, while for mean process variation, shown in Fig. 5.14(c), yields σ/μ = 0.14%. In Fig. 5.14(e), both types are considered and resulted in a σ/μ = 0.14%. Another significant performance that is affected by fabrication spread is the temperature coefficient, as shown in Fig. 5.14(b), (d), and (f). When local mismatch and average process are considered, the temperature coefficient varies from 6.5 to 41.5 ppm/°C, with an average of 14.5 ppm/°C. Also, in the simulated TC for PC+MM variations, 95% of the

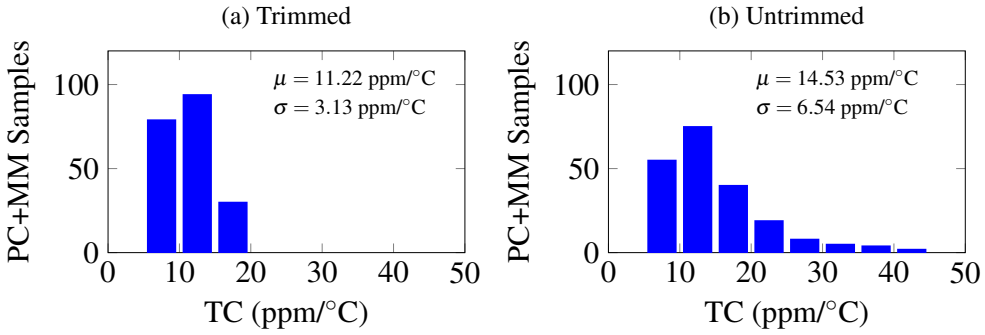
Figure 5.14: V_{REF} and TC Monte Carlo results. Local mismatch on (a) and (b); Average process variation on (c) and (d); Combined on (e) and (f)



Source: Author.

runs yield a TC lower than 29.3 ppm/°C.

Figure 5.15: Monte Carlo results of TC considering process and mismatch for trimmed and untrimmed circuit.



Source: Author.

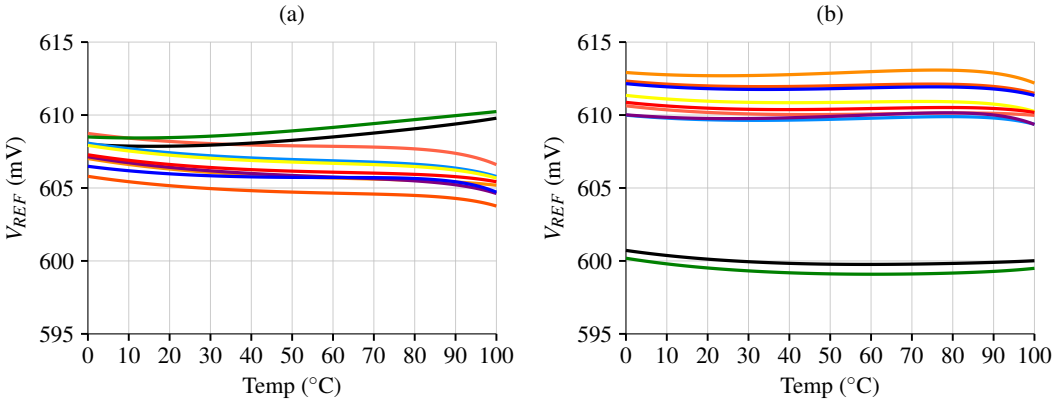
The circuit reached an adequate TC performance however with the proposed trimming scheme it is possible to improve the reference voltage temperature sensitivity. Considering 200 samples from the MC simulations, for each sample, its $\Delta V_{REF(27,100°C)}$ values were calculated. From Fig. 4.13(b), samples with $\Delta V_{REF(27,100°C)} > 200\mu V$ do not present low TC and are the ones that must be trimmed. Then, 50 among the 200 samples

were selected to be trimmed through the digital bits.

Considering these 50 trimmed references within the 200 samples, 95% of the runs yield a TC lower than 16.8 ppm/°C. Moreover, 90% yield a TC lower than 16 ppm/°C while the untrimmed circuit achieved only 68% of the samples with a TC lower than 16 ppm/°C.

A histogram comparing the spread of the TC considering the trimmed and untrimmed circuit is shown in Fig. 5.15. Also, Fig. 5.16 plots the reference voltage over the temperature range in 10 temperature coefficient worst-case samples before and after trimming.

Figure 5.16: Temperature dependence of V_{REF} (a) before and (b) after trimming.



Source: Author.

The results are presented in Table 5.2. The trimming scheme improved TC performance while consuming only 3.6 nW. From Fig. 5.16 the spread of the reference voltage increases with the trimming technique and resulted in a V_{REF} σ/μ = 0.33%, which is still a good performance because the deviation is low. The purpose of the trimming is to reduce the TC due to its importance and difficulty. The spread of the reference voltage is easier to trim and can also be done by other analog blocks inside a system.

Table 5.2: Performance summary of SBDF.

Specification	**Untrimmed**	**Trimmed**
Temp. Range (°C)	**0 - 100**	**0 - 100**
V_{DD} (V)	**0.9 - 1.8**	**0.9 - 1.8**
V_{REF} (V)	**607.4**	**607.4**
V_{REF} σ/μ (%)	**0.14**	**0.33**
TC_{avg} (ppm/°C)	**14.5**	**11**
TC_{min} (ppm/°C)	**6.5**	**5.6**
TC_{max} (ppm/°C)	**41.4**	**19.3**
LS (%/V)	**0.46**	**0.46**
PSRR@100Hz (dB)	**-49.7**	**-49.7**
Power@V_{DDnom} (nW)	**36.4**	**40**

5.3 Comparison with the State-of-The-Art

The comparison of the implemented designs with recently published voltage references is reported in Table 5.3. The SBSCM presented a lower TC compared to the SBDF

topology. This can be explained because the PTAT voltage slope generated by the SCM cell is less affected by variability than the one generated by the unbalanced differential pair. Also, the SCM structure generates a PTAT voltage that is less non-linear over temperature compared to the unbalanced differential pair.

As presented in the PTAT circuits analysis, the unbalanced differential pair topology generates an output voltage that suffers less from process deviations than the cascaded SCM cell. Then, regarding the reference voltage spread, the SBDF circuit shows a more accurate V_{REF} than the SBSCM.

Comparing the proposed circuits with other published voltage references, the SBSCM and SBDF designs present an excellent TC performance over a considerable temperature range. The circuits occupy a small silicon area with one of the lowest power consumption. Both topologies report low line sensitivity and a high PSRR. The proposed circuits present the best trade-off among TC, V_{REF} σ/μ, and power consumption over all other state-of-art references. Although the circuit of OLIVEIRA et al. (2018) presents a higher FoM, its TC and V_{REF} σ/μ performance are not suitable for high precision applications. Moreover, our circuits presented the second-best and third-best FoM.

Table 5.3: Comparison of Recent CMOS Voltage References.

Specification	[1]	[2]	[3]	[4]^s	[5]	[6]	[7]	[8]	**SBSCM**^{s}	**SBDF**^{s}
Process (μm)	0.35	0.16	0.18	0.18	0.18	0.18	0.5	0.35	**0.18**	**0.18**
Temp. Range (°C)	-20 - 80	-40 - 125	-40 - 120	-40 - 85	-40 - 125	-25 - 125	-5 - 125	-40 - 125	**0 - 100**	**0 - 100**
Measured Samples	17 1 batch	61 2 batches	9 1 batch	-	63 1 batch	5 1 batch	10 1 batch	30 1 batch	-	-
V_{DD} (V)	1.4 - 3	1.8	1.2 - 1.8	1.8	1 - 1.8	0.3 - 1.2	2.1 - 5	2 - 5	**1 - 1.8**	**0.9 - 1.8**
V_{REF} (V)	0.745	1.0875	1.09	1.29	0.756	0.026	1.196	1.14055	**592**	**607.4**
V_{REF} σ/μ (%)	0.87	0.05^a	0.737	0.26	0.95^a	3.4^s	0.625^a	0.97^a	**0.83**	**0.33**
TC_{avg} (ppm/°C)	15	-	147	14.51	49.6^a	208	5.87^a	4.03^a	**6.9**^{a}	**11**^{a}
TC_{min} (ppm/°C)	7	5^a	-	-	-	-	3.98^a	1.01^a	**1.3**^{a}	**5.6**^{a}
TC_{max} (ppm/°C)	45	12^a	-	28.8	-	-	8.29^a	-	**15.9**^{a}	**19.3**^{a}
LS (%/V)	0.002	-	-	-	0.524	0.188	0.19	0.02	**0.8**	**0.46**
PSRR@100Hz (dB)	-45	74*	-62	-	-52	-67.3^s	-84	-61	**-44.7**	**-49.7**
Power@V_{DDnom} (nW)	320	99000	100	77400	23	0.04	79800	66000	**40.8**	**40**
Silicon Area (mm^2)	0.055	0.12	0.0294	0.015	0.0162	0.0006	0.053	0.0396	**0.0154**	**0.022**
FoM (°C^3/W mm^2)	3.3	22.2	0.5	0.7	20	1250	0.2	0.4	**485**	**862**

^{a}Trimmed; ^{s}Simulated;* @DC

[1] UENO et al. (2009); [2] GE et al. (2011); [3] OSAKI et al. (2013); [4] KLIMACH et al. (2013); [5] ZHANG et al. (2018); [6] OLIVEIRA et al. (2018); [7] MING et al. (2018); [8] ZHOU et al. (2019);

6 CONCLUSIONS

From classic references to recent developments on CMOS voltage references, distinct works were discussed. This investigation of different circuits focused mainly on improving the trade-off between temperature coefficient, power consumption, and variability impact on the reference voltage.

An evaluation of CTAT and PTAT voltages generators were presented. Each topology was detailed and described considering the UICM model. The variability impact was estimated in these structures through Monte Carlo simulations and resulted in different outcomes. From this analysis it was possible to propose and implement voltage reference circuits combining precision and low power consumption.

Considering the PTAT voltage generators, the SCM and the unbalanced differential pair were the architectures that suffered less with process deviations. Then, both these structures were chosen to generate a PTAT voltage and implement two voltage references circuits. From the performance of the voltage references designs, it is possible to compare and verify the variability performance of each circuit.

A self-biased BJT circuit presented an interesting topology combining a voltage divider with the biasing structure. However, its biasing current depends on the threshold voltage which impacts on the process deviations of the generated CTAT voltage. Then, a different BJT biasing was introduced to generate a CTAT voltage and reduce the variability impact on this signal. Simulation results showed that the CTAT voltage variability reduced from 2.2% to 0.33% with the proposed I_{SQ} current source.

Focusing on reducing the variability impact to generate a precision reference voltage and based on these above-mentioned results and analysis, two sub-bandgap voltage references were proposed. Both circuits employed the same CTAT voltage but combined with distinct PTAT structures. Furthermore, considering the CTAT characteristics, a low power single-point trimming strategy was proposed to adjust the reference voltage TC. The relation between the biasing current and the generated V_{EB} voltage was used to modify the TC of the CTAT voltage. Then, the temperature coefficient of the reference voltage was adjusted by these CTAT voltage modifications. The trimming scheme was developed to facilitate the calibration procedure and to represent a cost-efficient solution. Moreover, the proposed trimming technique significantly reduced the reference voltage TC, consumed less than 4 nW of power, and proved to be an interesting solution to suppress fabrication variability deviations.

A sub-bandgap with SCMs was designed in TSMC 180 nm and from post-layout simulations generated a reference voltage of 592 mV with a power consumption of 40.8 nW under 1.8 V supply. The circuit works over the 0 to 100 °C temperature range with a typical temperature coefficient of 3.6 ppm/°C, with a silicon area of 0.0154 mm^2. The topology presented a 0.8 %/V of LS within the supply voltage range of 1 to 1.8 V and

a -44.7dB of PSRR. Monte Carlo simulations considering the trimming samples showed the design robustness to process and mismatch variations, resulting in a spread of the reference voltage of σ/μ = 0.83%. Also, in the MC simulations, the circuit achieves a TC as low as 1.3 ppm/°C and an average TC of 6.9 ppm/°C. The sub-bandgap with unbalanced differential pair was also implemented in TSMC 180 nm and generated a reference voltage of 607.4 mV from post-layout simulations. The circuit occupies 0.022 mm^2 of silicon area while consuming 40 nW under 1.8 V. The design presented a 0.46 %/V of LS within the supply voltage range of 0.9 to 1.8 V and a -49.7dB of PSRR. A typical temperature coefficient of 8.3 ppm/°C was found over the 0 to 100 °C temperature range. Monte Carlo simulations considering the trimming samples demonstrated the circuit robustness to process and mismatch variations, achieving a TC as low as 5.6 ppm/°C and an average TC of 11 ppm/°C. Also, this simulation resulted in a spread of the reference voltage of σ/μ = 0.33%.

The proposed topologies were compared with the state-of-the-art, and the sub-bandgap reference with self-cascode MOSFETs and the sub-bandgap reference with unbalanced differential pair presented a low temperature coefficient over the temperature range while consuming low power. Both circuits present a small silicon area and the best trade-off considering TC, $V_{REF}\sigma/\mu$, and power consumption compared to the state-of-the-art. The SBDF design showed the second-best FoM and the SBSCM the third-best. Then, considering the achieved performance, the proposed circuits are suitable for applications that require a high precision reference voltage.

6.1 Future Works

The implemented circuits presented attractive results; however the circuits were only tested through simulation. Since the SBSCM topology was sent to fabrication by TSMC/mini@sic program, it is essential to confirm the results by measuring the circuit. Below are listed future steps of this research and possible new topics to investigate:

1. Measurement of the sub-bandgap voltage reference fabricated by mini@sic program in TSMC 180 nm;
2. Publish in a relevant journal the measured results of the proposed circuit;
3. Optimization of the topologies for low supply voltage operation;
4. Improvement of the start-up circuit;
5. Improvement of the trimming techniques;
6. Design of voltage references in more advanced technological nodes (< 90 nm);
7. Study and develop novel topologies based on switched capacitors.

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APPENDIX A LIST OF PUBLICATIONS

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APPENDIX B UICM MOSFET MODEL

The Unified Current-Control Model (UICM) proposed by CUNHA; SCHNEIDER; GALUP-MONTORO (1998) is based on charge inversion levels and calculates the drain current I_D of a long-channel MOS transistor by

$$I_D = I_F - I_R = I_{SQ} S (i_f - i_r) \tag{B.1}$$

where I_F and I_R are the forward and reverse current components, $S = W/L$ is the transistor aspect ratio, W being the width, and L the length of the transistor. Parameters i_f and i_r are the normalized forward and reverse currents, related to the source and drain inversion charge densities, while I_{SQ} is the sheet normalization current

$$I_{SQ} = \frac{1}{2} n \mu C'_{ox} \phi_T^2, \tag{B.2}$$

where n is the subthreshold slope factor, μ is the effective channel mobility, C'_{ox} is the oxide capacitance per unit of area, $\phi_T (= k_B T/q)$ is the thermal voltage, k_B is the Boltzmann constant, T is the absolute temperature, and q is the electron charge. The forward and the reverse inversion levels are related to the terminal voltages as follows

$$\frac{V_P - V_{S(D)}}{\phi_T} = F(i_{f(r)}) = \sqrt{1 + i_{f(r)}} - 2 + \ln(\sqrt{1 + i_{f(r)}} - 1) \tag{B.3}$$

where $V_{S(D)}$ is the source (drain) voltage referenced to bulk, V_P is the pinch-off voltage, which can be approximated by $V_P \simeq (V_G - V_{T0})/n$ being V_{T0} the threshold voltage for zero bulk bias and V_G the gate voltage.

APPENDIX C MATLAB CODE

Matlab code for calculation of the trimming codes, as shown in C.1 and C.2.

Listing C.1: Code for trimming SBSCM.

```
% Varibles definition.

Vref_27 = 500;   % Insert here the measured reference voltage at 27C in mV.
Vref_100 = 501;  % Insert here the measured reference voltage at 100C in mV.
DVref = (Vref_27 - Vref_100)*1000;   % Difference between Vref at 27C and 100C.

p1 = 9.9593e-11    % Coefficients of the polynomial equation
p2 = -1.0142e-06
p3 = 0.0048334
p4 = 4.3992


bitscubic = p1*abs(DVref)^3 + p2*abs(DVref)^2 +  p3*abs(DVref) + p4;  % Polynomial eq.

if DVref > 0
       flag1 = bitscubic - 5;       % DVref > 0 increasing W11 sizing
       BITS_total = 5 - flag1 ;     % BITS_total is the trimm code that must be used
  else
       flag2 = bitscubic - 5;       % DVref < 0 reducing W11 sizing
       BITS_total = flag2 + 5 ;     % BITS_total is the trimm code that must be used
end
```

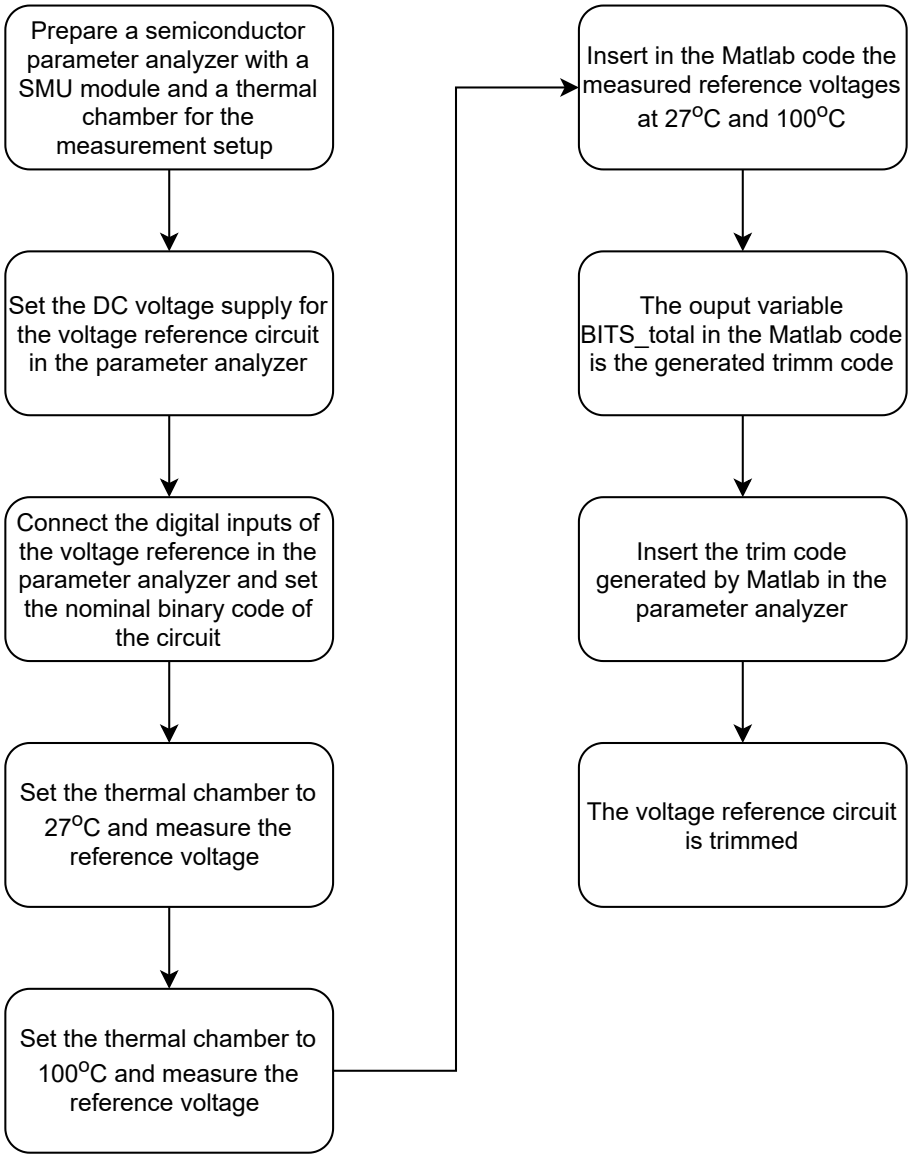
Listing C.2: Code for trimming SBDF.

```
% Varibles definition.

Vref_27 = 500;   % Insert here the measured reference voltage at 27C in mV.
Vref_100 = 501;  % Insert here the measured reference voltage at 100C in mV.
DVref = (Vref_27 - Vref_100)*1000;   % Difference between Vref at 27C and 100C.

p1 = 7.1352e-11     % Coefficients of the polynomial equation
p2 = -7.0739e-07
p3 = 0.0033825
p4 = 7.472

bitscubic = p1*abs(DVref)^3 + p2*abs(DVref)^2 +  p3*abs(DVref) + p4;  % Polynomial eq.

if DVref > 0
       flag1 = bitscubic - 6;       % DVref > 0 increasing W11 sizing
       BITS_total = 6 - flag1 ;     % BITS_total is the trimm code that must be used
  else
       flag2 = bitscubic - 6;       % DVref < 0 reducing W11 sizing
       BITS_total = flag2 + 6 ;     % BITS_total is the trimm code that must be used
end
```

APPENDIX D TRIMMING PROCEDURE

The flowchart in Fig. D.1 shows the trimming steps and procedures to properly trim the device.

Figure D.1: Trimming procedure flowchart.



Source: Author.