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Circuit-Level Design Impact on Variability and Soft Errors Robustness

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"Those who fall in love with practice without science are like
a sailor who enters a ship without a helm or a compass,
and who never can be certain whither he is going."

— Leonardo Da Vinci

ABSTRACT

Physical limitations were found in MOSFET devices with the advancement in microelectronics. To overcome these limitations, multigate devices, such as the FinFET technology, were introduced, allowing the continuity of the technology scaling below 22nm. The evolution in the manufacturing process of integrated circuits has resulted in increasingly smaller devices and made the lithography stage more complicated, which can lead to circuits operating outside their specification ranges. Moreover, integrated circuits are exposed to different sources of radiation, considering space or even terrestrial applications. All of these factors impact the reliability of the circuits and may cause a deviation in expected behavior. In that way, the study of new guidelines capable of dealing with the challenges posed by technological development is of utmost importance. Some circuits can be designed using different transistor arrangements. A specific transistor arrangement can influence the performance of logic cells; complex logic gates can be used to minimize area, delay and power consumption. However, with the increasing relevance of nanometric challenges, it is also necessary to consider the variability and radiation effects at the logic level design with the adoption of different topologies, as the multi-level logic. This work explores circuit-level techniques to mitigate the radiation and process variability effects at 7nm FinFET technology. The process variability impact, through the work-function fluctuations (WFF), and the Single Event Transient (SET) response under WFF are evaluated using different transistor arrangements for a set of logic functions, versions of C17 benchmark (ISCAS85) and majority voters. Results show the impact of different transistor arrangements in the radiation and process variability robustness. The multi-level logic topology is more robust to the radiation effects than complex topology; the Threshold Linear Energy Transfer (LET_{th}) values are, on average, 55% higher considering or not the process variability impact. The LET_{th} values of the different majority voter circuits can vary by up to 65%. All the analyzed circuits independently of the topology are more sensitive (LET_{th} values, on average, 20% smaller) to the SETs considering the process variability impact.

Keywords: FinFET technology. microelectronics. multi-level design. radiation effects. variability.

Impacto do projeto em nível de circuito na robustez à variabilidade e erros leves

RESUMO

Com o avanço da microeletrônica, limitações físicas foram encontradas em dispositivos MOSFET. Para superar essas limitações, foram introduzidos dispositivos multigate, como a tecnologia FinFET, permitindo a continuidade do dimensionamento tecnológico a abaixo de 22 nm. A evolução no processo de fabricação de circuitos integrados resultou em dispositivos cada vez menores e tornou a etapa de litografia mais complicada, podendo levar os circuitos a operarem fora de suas faixas de especificação. Ainda, os circuitos integrados são expostos a diferentes fontes de radiação, considerando aplicações espaciais ou mesmo terrestres. Todos esses fatores afetam a confiabilidade dos circuitos e podem causar um desvio no comportamento esperado. Dessa forma, o estudo de novas diretrizes capazes de lidar com os desafios colocados pelo desenvolvimento tecnológico é de extrema importância. Alguns circuitos podem ser projetados utilizando diferentes arranjos de transistores. Um arranjo de transistores específico pode influenciar o desempenho de células lógicas; portas lógicas complexas podem ser usadas para minimizar a área, o atraso e o consumo de potência. No entanto, com a crescente relevância dos desafios nanométricos, também é necessário considerar os efeitos de radiação e da variabilidade no design de nível lógico com a adoção de diferentes topologias, como a lógica multinível. Este trabalho explora técnicas em nível de circuito para mitigar os efeitos de radiação e da variabilidade de processo na tecnologia FinFET de 7nm. O impacto da variabilidade do processo, através das flutuações da função de trabalho (WFF), e a resposta de Eventos Únicos Transientes (SET) sob WFF são avaliados usando diferentes arranjos de transistores para um conjunto de funções lógicas, versões do benchmark C17 (ISCAS85) e votadores majoritários. Os resultados mostram o impacto de diferentes arranjos de transistores na robustez à radiação e variabilidade de processo. A topologia de lógica multinível é mais robusta aos efeitos de radiação do que a topologia complexa; os valores da Transferência Linear de Energia Limiar (LET_{th}) são, em média, 55% maiores considerando ou não o impacto da variabilidade de processo. Os valores de LET_{th} dos diferentes circuitos de votadores majoritários podem variar em até 65%. Todos os circuitos analisados, independentemente da topologia, são mais sensíveis (valores de LET_{th}, em média, 20% menores) aos SETs, considerando o impacto da variabilidade de processo.

Palavras-chave: FinFET, microeletrônica, design multinível, radiação, variabilidade.

LIST OF ABBREVIATIONS AND ACRONYMS

AOI	And-Or-Inverter
ARM	Advanced RISC Machine
ASAP7	7nm Arizona State Predictive Design Kit
BEOL	Back End Of Line
BTI	Bias Temperature Instability
CMOS	Complementary Metal-Oxide-Semiconductor
DD	Displacement Damage
DRC	Design Rule Check
DRAM	Dynamic Random Access Memory
EDA	Electronic Design Automation
EUV	Extreme Ultraviolet
FD-SOI	Fully Depleted Silicon On Insulator
FEOL	Front End Of Line
FET	Field Effect Transistor
GND	Ground
HFIN	Fin Height
IG	Independent Gate
INV	Inverter
IRPS	International Reliability Physics Symposium
L	Length
LELE	Litho-Etch Litho-Etch
LET	Linear Energy Transfer
LFIN	Gate Length
LVS	Layout Versus Schematic

MGG	Metal Gate Granularity
MOL	Middle of line
MOS	Metal Oxide Semiconductor
MUX	Multiplexer
NAND	Not AND
NFET	N-Channel FET
NIEL	Non-ionizing Energy Loss
NMOS	N-Channel MOSFET
NOR	Not OR
OAI	Or-And-Inverter
OPC	Optical Proximity Correction
PDK	Process Design Kit
PDP	Power-Delay-Product
PFET	P-Channel FET
PMOS	P-Channel MOSFET
RET	Resolution Enhancement Techniques
SAA	South Atlantic Anomaly
SADP	Self-Aligned Double Patterning
SAQP	Self-Aligned Quadruple Patterning
SCE	Short Channel Effects
SE	Soft Error
SEB	Single Event Burnout
SEE	Single Event Effects
SEGR	Single Event Gate Rupture
SEL	Single Event Latch-up
SET	Single Event Transient

SEU	Single Event Upset
SG	Shorted Gate
SHE	Single Hard Error
SOI	Silicon on Insulator
SPICE	Simulation Program with Integrated Circuit Emphasis
SRAM	Static Random Access Memory
TCAD	Technology Computer-Aided Design
TID	Total Ionizing Dose
TMR	Triple Modular Redundancy
TSI	Fin Width
UV	Ultraviolet Rays
VDD	Supply Voltage
VLSI	Very large-system Integration
W	Width
WFF	Work-Function Fluctuation
XOR	Exclusive OR

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1 INTRODUCTION

The evolution in the manufacturing process of the transistors has been happening with impressive speed. The reduction of the transistors dimensions, known as technology scaling, provides some advantages, such as: an increase in the integration capacity of the integrated circuits, the operating frequencies can be increasingly higher, and the circuits can operate with better performance and lower power consumption. However, some challenges are also introduced. The transistors shrinking ends up causing a series of side effects. Increasing the variability of the manufacturing process (ORSHANSKY; NASSIF; BONING, 2008), the Short-Channel Effects (SCE), the undesirable leakage current (TAUR et al., 1997) and the susceptibility to radiation effects. Integrated circuits play an important role in all of our daily tasks, which is one of the reasons that make them increasingly dense and complex.

Bulk CMOS technology is reaching its physical and geometric limits. The planar devices have been used in integrated circuits design for several decades, but in each new technological node, these devices suffer from the side effects previously mentioned, highlighting the increasing susceptibility to soft errors (SEs) (FRANK et al., 2001; KING, 2005). The use of multigate devices is an option to overcome these obstacles and to continue the technology scaling since these devices provide better control of the SCE, a reduction in the leakage currents and better yield (ITRS, 2011; AUTH et al., 2012). FinFET (Fin-Shaped Field Effect Transistor) technology is the main multigate device, replacing planar MOSFET devices on sub-22nm technology nodes (BROWN; WATLING; ASENOV, 2006).

The radiation-induced soft errors and the process variability are an essential reliability concern for nanotechnologies, affecting integrated circuits used for space or even terrestrial applications (BAUMANN, 2002; HEIDEL et al., 2009). Process variability is related to the random deviation, which causes an increase or decrease of typical design specifications. The primary variability issue is the uncertainty about the correct operation of the circuit. There is no guarantee that a circuit will behave as expected after the manufacturing process. Due to the process variability effects, each circuit can present a different electrical behavior such as abnormal power consumption, performance deviation, or both. The unexpected behavior due to variations can stimulate circuit degradation besides make it inappropriate for your initial purpose. On multigate devices, variability effects are mainly due to the work-function fluctuation (WFF) of the metal gate (BROWN;

WATLING; ASENOV, 2006; KLEEBERGER; GRAEB; SCHLICHTMANN, 2013). As previously mentioned, the radiation effects are also an essential reliability concern. Before observing the impact of these effects on the design of the integrated circuits, it is important to know their origins.

The Earth's atmosphere is a semi-permeable layer that allows the passage of light and heat; it acts as a natural filter reducing the intensity of radiation that hits the Earth and blocking ultraviolet rays. The intensity of the radiation increases according to the increase of altitude about the sea level; however, some regions suffer from a greater concentration of radiation, even if they are located in low altitudes. This fact occurs due to phenomena related to the Earth's magnetic field, such as the polar regions. There is a diverse range of radiation that can be found in space or in the atmosphere, which is classified into two broad groups: ionizing particles and non-ionizing particles. Cosmic rays, x-rays and radiations from radioactive materials are examples of ionizing radiation; that is, they produce the emission of electrons when interacting with some material. Ultraviolet light, radio waves and microwaves are examples of non-ionizing radiation, as they are not capable of ionizing any material. The main particles that can cause undesired effects in electronic circuits are electrons, protons, neutrons, alpha particles and heavy ions, as well as electromagnetic radiation, such as x-rays and gamma rays (STASSINOPOULOS; RAYMOND, 1988).

Space radiation consists of subatomic particles, which may originate from heavy ions present in the space environment or alpha particles emitted from radioactive isotopes. These particles travel in space at very high speeds, and the fastest ones can travel at speeds close to the speed of light, which allows them to easily traverse a material and cause various effects on it. The Earth constantly receives radiation from the space of three primary sources that can affect the electronic circuits: the Sun, Cosmic Rays and Trapped Radiation.

Electronic circuits operating in space, especially in harsh environments, may be exposed to significant radiation doses as well as to the incidence of heavy particles from the sun or outside the galaxy. From this exposure to radiation, changes and disturbances in the circuit, which impair its correct functioning, can occur with high probability. The effects related to the incidence of radiation in electronic components have been studied for a long time by the international scientific community, mainly for space and military applications. The integrated circuits that experience the interaction of ionizing particles basically suffer from two types of degradation: those of singular character, occurring due

to the incidence of a single particle, and those of a cumulative character, which, in turn, occur due to the accumulation of doses of ionizing radiation over the lifetime of the circuit (BOUDENOT, 2007; STASSINOPOULOS; RAYMOND, 1988).

Degradations that occur due to the incidence of a single particle are called Single Event Effects (SEE). These effects can be divided into two subgroups: Destructive Events (hard error) if it causes a permanent failure in the circuit. Single Event Transient (SET) or Non-Destructive (soft error), in case of an error in the system that does not cause permanent damage. The SET, the main focus of this work among the radiation effects, results in a current pulse at a given point in the circuit that can propagate by modifying the voltage of other nodes and the current elsewhere in the circuit (BAZE; BUCHNER, 1997) (SAVAGE et al., 2001).

Cumulative effects have their origin due to the dose of ionizing radiation accumulated over the life of the device and are classified as Total Ionizing Dose (TID). Prolonged exposure to ionizing radiation, due to accumulated (radiation-induced) electric charges, causes parts of the circuit to change in their electrical characteristics, such as a change in threshold voltage (V_{th}) and the increase in the leakage current of the device. These electrical changes impair the correct functioning of the device and may, depending on the amount of accumulated dose, permanently damage it.

For a long time, SETs were not considered a significant reliability concern. The logical, electrical and latching window masking present in digital logic, were enough to minimize the importance of considering the phenomenon. However, with technology scaling, lower supply voltages and reduced nodal capacitances, the minimum charge required to induce a transient pulse was decreased (HEIDEL et al., 2009; GADLAGE et al., 2010). Also, it is more likely that a SET generated in combinational logic will be captured at the storage element due to the higher operating frequencies. Thus, to overcome some of these problems, new device architectures and novel materials are being used.

The techniques to protect integrated circuits against radiation effects can be divided into three levels: process (hardening-by-technology), design (hardening-by-design) and system (hardening-by-system). The focus of this work is the device design-level techniques to mitigate SEs, but also the process variability effects. Modifying the transistor arrangement is a technique explored to design faster (BUTZEN et al., 2010) or low power circuits (HOSSAIN; ZHENG; ALBICKI, 1994), but also to deal with Bias Temperature Instability (BTI) (SILVA; REIS; RIBAS, 2009; YI et al., 2016) or to improve design robustness against permanent and transient faults (CHIANG et al., 2013). The adoption of

complex gates reduces the number of transistors, reducing the used area and also reducing the delay and power consumed. However, complex gates can present challenges related to regularity and reliability that can be avoided with more regular and basic cells.

The FinFET technology presents significant differences in structure compared to planar CMOS devices. FinFET devices have limited sensitive areas compared to planar devices, resulting in a reduced charge collection region (ARTOLA; HUBERT; ALIOTO, 2014; EL-MAMOUNI et al., 2011). So, FinFETs collect significantly less charge than mature technologies, showing a better response to radiation effects, even considering the technology scaling. However, the radiation effects are not negligible on multigate devices (FERLET-CAVROIS; MASSENGILL; GOUKER, 2013). With the constant increase in the circuits operating frequencies, the possibility of a memory element capturing an SE also increases. Also, other reliability challenges can interfere in the radiation effects susceptibility of FinFET devices. The proper estimation of Threshold Linear Energy Transfer (LET_{th}) along with the SET pulse width is of utmost importance for soft error mitigation and radiation-tolerant circuit design (ARTOLA; HUBERT; SCHRIMPF, 2013).

Few papers address the two reliability concerns presented together in circuit design, and few solutions are found in the literature to mitigate the impact of process variability at the circuit-level. In this context, this master dissertation investigates the radiation and process variability effects in robustness, using 7nm FinFET technology (CLARK et al., 2016). Circuit-level techniques are explored to try to mitigate these reliability challenges, considering only the process variability and both effects together.

1.1 Objectives

This research focuses on the robustness of different circuits to the radiation and process variability effects. The main contributions are related to circuit-level techniques to mitigate these reliability concerns using a 7nm FinFET technology. The key objectives:

1) To evaluate the process variability impact on complex and multi-level logic topologies using transistor reordering technique and different transistor sizing;
2) To investigate the SET response under process variability, through the WFF, using different transistor topologies;
3) To assess the impact of both effects on circuits with different complexities.

1.2 Organization

This work was organized to facilitate the reader's understanding. Chapter 2 introduces the main features of FinFET technology and the fault tolerance basic concepts and terms. The main sources of process variability and their effects are presented in chapter 3. The radiation effects on electrical circuits, with emphasis on the single event effects, are shown in chapter 4. Chapter 5 presents the primary works related to this dissertation. The chapters 6 and 7 present the methodology and the results obtained through different experiments. Finally, the conclusions are presented in chapter 8.

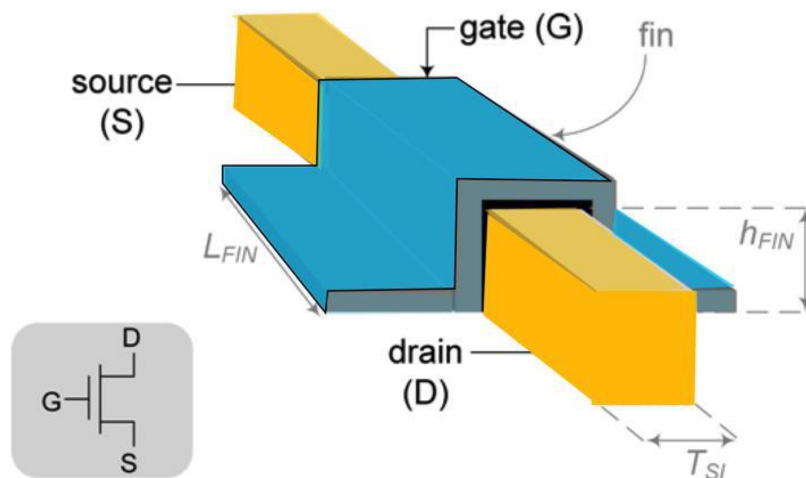
2 BACKGROUND

This chapter introduces initial concepts about FinFET technology and the fault tolerance area. Before presenting in detail the reliability challenges evaluated in this work, it is important to highlight parameters, terms and basic concepts of the technology and the effects explored in this dissertation.

2.1 FinFET Reliability Challenges

A FinFET device is composed of vertical silicon structures that form the channel region connecting the source and drain regions at each end (BROWN; WATLING; ASENOV, 2006). The gate region is wrapped around this vertical structure, which is known as **fin**. MOS channels are formed in the two side walls. The ON current (I_{on}) of these devices is a function of the sum of the drive currents contributed by the two side-gate transistors. This fin-like geometry, where the depletion regions arrive from the gates to the body region, implies that no free-charge conveyor is available, reducing the SCEs in FinFETs (HUANG et al., 1999). Figure 2.1, presents the main geometric parameters of a FinFET transistor (ALIOTO, 2011): gate length (L_g), fin height (H_{fin}) and the fin width/thickness (W_{fin}/T_{si}). It is important to remember that the FinFETs also have Bulk and SOI insulation; in this work was used Bulk FinFETs.

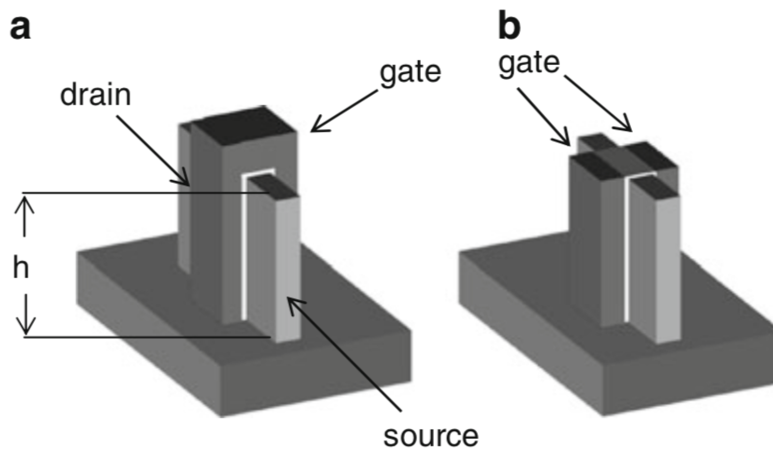
Figure 2.1: Structure and geometric parameters of a FinFET device.



Source: Alioto (2011).

FinFET devices can be designed in different configurations. Two main configurations are shown in Figure 2.2. In the shorted-gate (SG) configuration, the front-gate and the back-gate are connected together, leading to a three-terminal device. This can serve as a direct replacement for the conventional bulk CMOS devices. In the FinFETs of the independent-gate (IG) configuration, the top of the gate is removed, giving rise to two independent gates. Since the two independent gates can be controlled separately, FinFETs in the IG mode offers more options for design (MISHRA; MUTTREJA; JHA, 2011). This work uses the FinFET transistors in the SG configuration for all analysis.

Figure 2.2: Two configurations of FinFET devices: (a) SG - FinFET; (b) IG - FinFET.

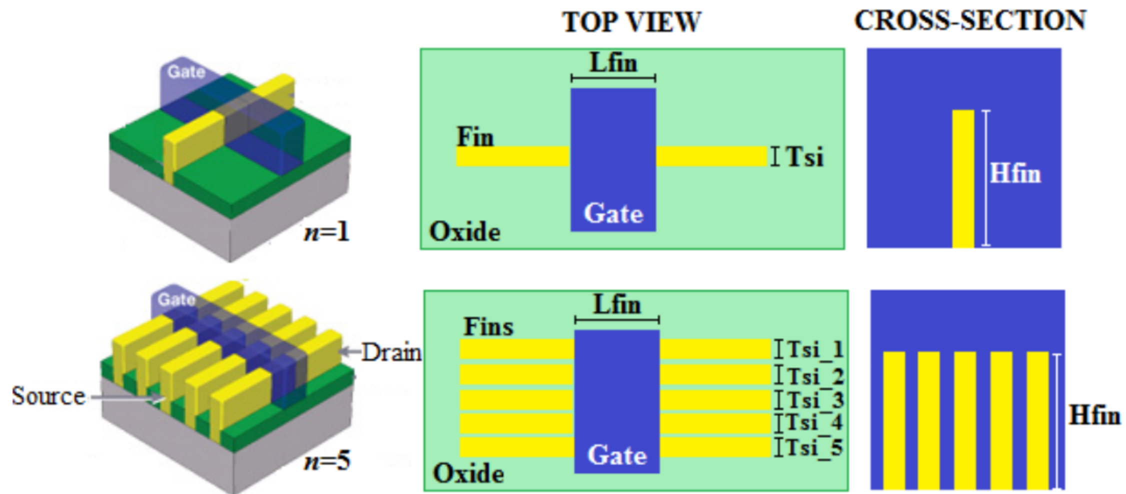


Source: Mishra, Muttreja and Jha (2011).

Another important feature of FinFET technology is transistor sizing. Unlike mature MOSFETs, to have an increase in the sizing of FinFETs transistors, multiple fins sharing common lateral diffusion are connected in parallel in the region between the source and the drain, as shown in Figure 2.3. Thus, the total width of the device is given by $W_{total} \approx W_{min} \times n$, where n is the number of fins (SWAHN; HASSOUN, 2006)(COLINGE et al., 2008) and W_{min} (minimum transistor size) is $W_{min} = 2 \times H_{fin}$.

Reliability challenges also affect FinFET devices. The significant differences in the structure of a FinFET transistor, compared to mature technologies, modify the circuit's robustness to the reliability aspects. These differences will be presented in detail in the following chapters.

Figure 2.3: Structure of a FinFET device with one fin and multi-fin.



Source: Christiansen (2015).

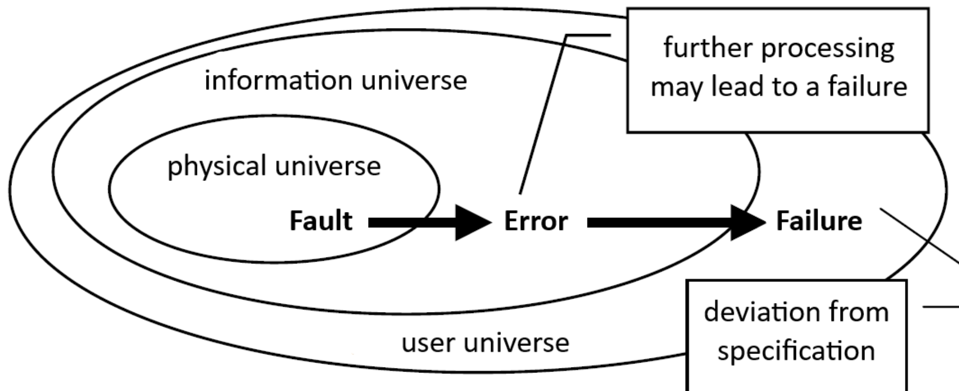
2.2 Fault Tolerance Basic Concepts and Terms

Before presenting the impact of radiation effects on electronic circuits, it is essential to present the main terms and concepts used in the fault tolerance area to characterize these effects. In the fault tolerance area, the most conflicting terms are fault, error, and failure. The concepts and terms presented in this work are used by the majority of the community (LAPRIE, 1985)(ANDERSON; LEE, 1981), highlighting the works of Pradhan et al. (1996) and Avizienis (1982).

The terms fault, error and failure, can be best explained using the Three-Universe model of Pradhan et al. (1996), shown in Figure 2.4. This model, an adaptation of the Four-Universe model introduced by Avizienis (1982), describes the different phases of evolution from fault to failure. The first universe is the physical universe, where faults occur.

A **fault** is an unwanted physical condition or imperfection that occurs in some hardware components. The faults may become dormant for a long time and will not influence component performance. When a fault is activated, the effects can be observed in the information universe. An **error** is the manifestation of a fault, that is, a change in the state of the system presenting inconsistency in the data generated by the functionality affected by the fault. **Failure** is a deviation from the circuit specification and therefore corresponds to the inability of a component to perform its predefined function. Failures cannot be tolerated, just avoided.

Figure 2.4: Three-Universe model proposed by Pradhan et al. (1996).



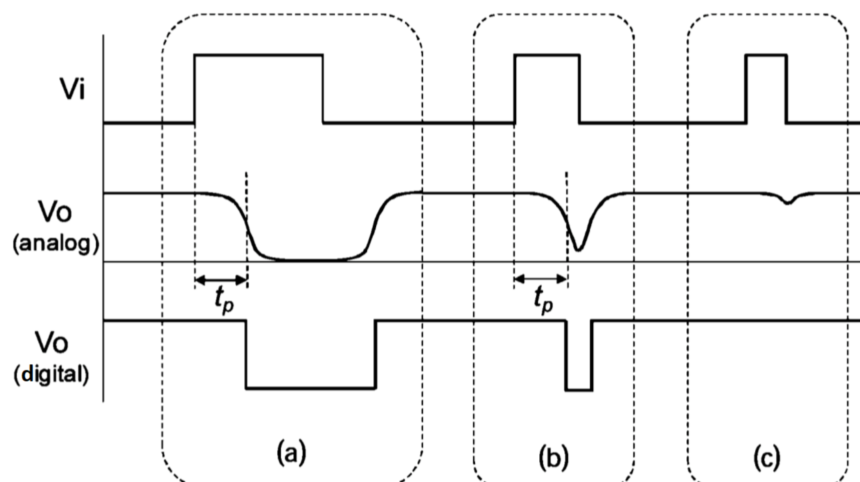
Source: Adapted from Pradhan et al. (1996).

2.2.1 Fault Masking

In the occurrence of transient faults caused by the radiation effects, some mechanisms are responsible for masking the effect of a fault and prevent it from being propagated to the next levels, avoiding that incorrect values reach the output of the circuit. The masking can be divided into three main types: electric, logical and latching window.

In the **electric masking**, the fault is not propagated until the output of the circuit due to electrical losses that attenuate its magnitude. In Figure 2.5, one can observe the degradation of the pulse, until its possible attenuation, characterizing the electric masking.

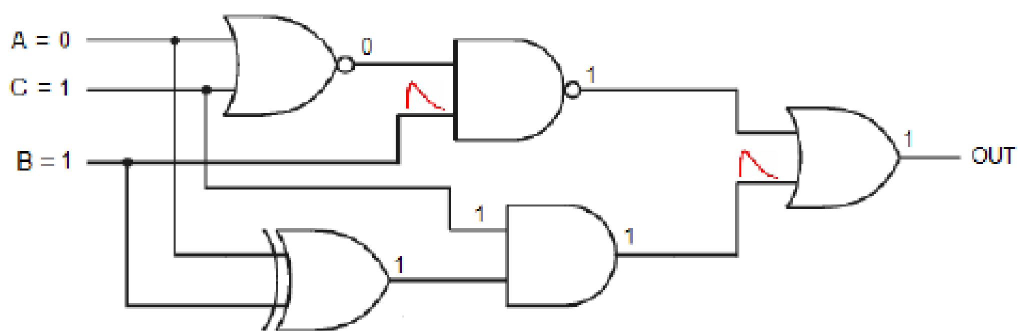
Figure 2.5: Degradation of a pulse by electric masking. Depending on the width of the generated pulse (a) this, when propagating through the circuit, can be attenuated (b) or filtered (c), characterizing the electric masking.



Source: Entrena et al. (2009).

Logical masking occurs when the fault affects a region of the circuit that is not determinant for the result obtained at its output at the time the fault occurred. Figure 2.6 presents two cases of logical masking present in a circuit. The first case would be the NAND2 logic gate, in which one of its inputs is set to '0'. Therefore, regardless of the value assigned in the other inputs, its output will always be '1'. Another case can be observed in the OR2 gate, in which a transient fault falls on one of its inputs, the other input being equal to '1'. Since the output of the circuit has already been determined by one of its inputs, the transient fault present in the other input will not affect the result, so it turns out that there was logical masking of the fault in question.

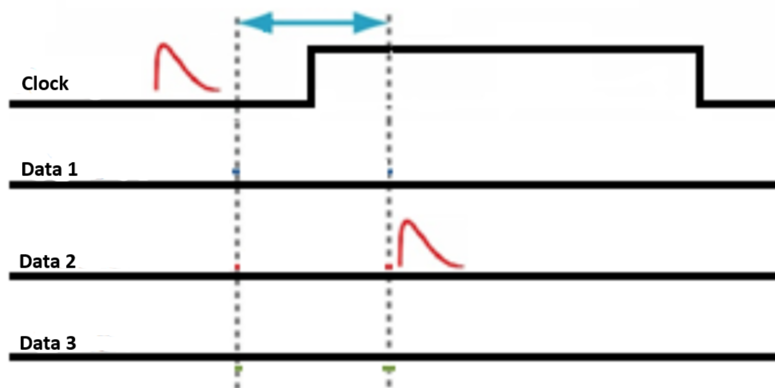
Figure 2.6: Logical masking example in combinational circuit.



Source: Zimpeck, Meinhardt and Butzen (2014).

The masking by **latching window** occurs when a transient pulse, not being masked logically or electrically, propagates through the circuit to a memory element. However, during its transition, there is no clock transition, i.e., the pulse reaches the data lines outside the latching window area, as can be seen in Figure 2.7. Thus, this pulse will not be stored in memory, not producing an error.

Figure 2.7: Latching Window masking.

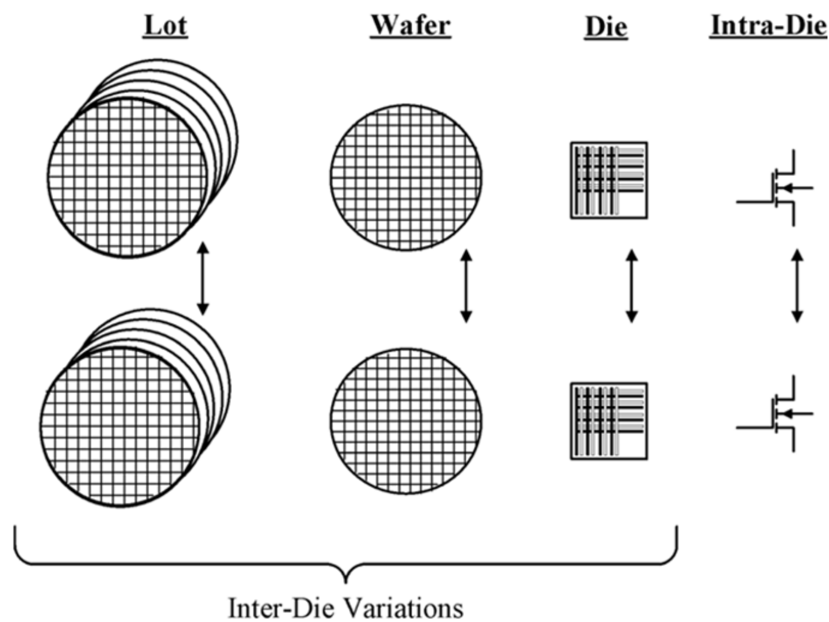


Source: Adapted from Zimpeck, Meinhardt and Butzen (2014).

3 VARIABILITY IN THE INTEGRATED CIRCUITS DESIGN

The advanced integrated circuits manufacturing process typically requires many steps. Despite the advances in fabrication techniques, systematic or random variations are still present during each manufacturing step. The number of mechanisms that lead to these variations seems to increase as processes become more complex (MUTLU; RAHMAN, 2005). From a circuit design perspective, process variations can be classified into inter-die and intra-die (MUTLU; RAHMAN, 2005; DOH et al., 2005), as shown in Fig 3.1.

Figure 3.1: Classification of variations observed at different phases of the manufacturing process.



Source: Mutlu and Rahman (2005).

Inter-die variations are characterized by lot-to-lot, wafer-to-wafer, or die-to-die fluctuations in the process. Inter-die variations affect all devices on a single chip equally (MUTLU; RAHMAN, 2005; DOH et al., 2005). In the circuit design, it is usually assumed that each component or contribution in inter-die variation is due to a different physical and independent source. The variation component can be represented by a deviation in the parameter mean of the circuit (COX et al., 1985).

Intra-die variations are deviations occurring within a die (MUTLU; RAHMAN, 2005) and refer to the device characteristics that vary from device to device (DOH et al., 2005). As a device scales down, intra-die variation has become as crucial as inter-die variation when analyzing circuit performance and predicting the yield of a chip (NASSIF, 1998). These variations may have a variety of sources that depend on the physics of the manufacturing steps (CHANDRAKASAN; BOWHILL; FOX, 2000).

3.1 Process Variability

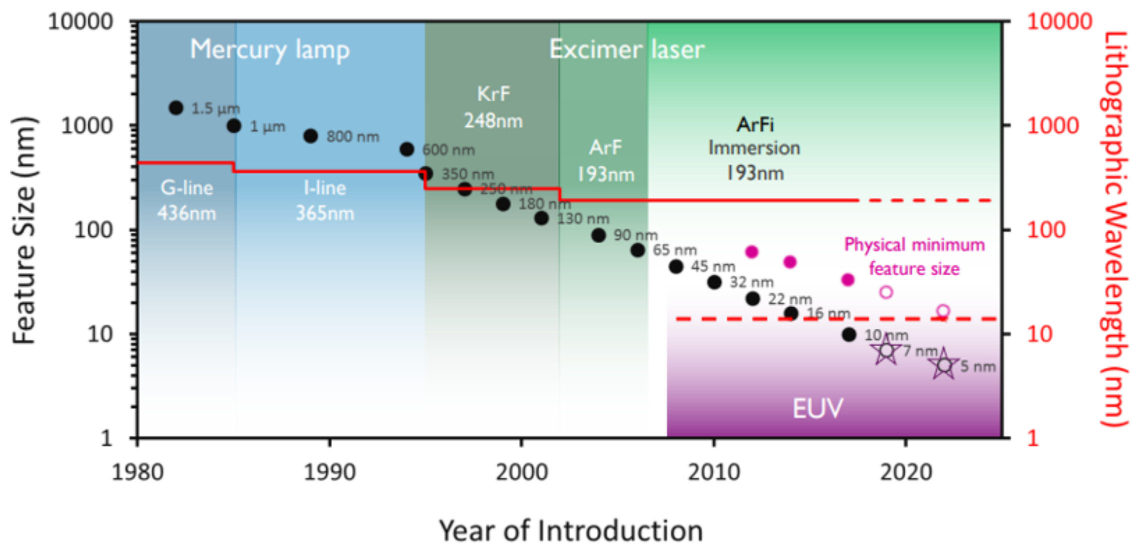
The variability in electronic circuits can be divided into three different factors: environmental, reliability and physical (NASSIF, 2008). Environmental factors appear during the circuit operation; variations in supply voltage and temperature are examples of environmental factors. Reliability factors are related to the transistor aging, due to the high electric fields presented in modern circuits. Finally, physical factors are associated with variations in electrical and geometrical parameters, which may occur due to the manufacturing process of the devices (NASSIF, 2008). The latter is best known for process variability and is the focus of this study.

The integrated circuits manufacturing process consists of several steps. Lithography is the primary tool used in the fabrication process to record a pattern on a layer of photosensitive material (photoresist) spun over a substrate, generally a semiconductor wafer (CERRINA, 2001). According to Thomas Caulfield, senior vice president and general manager of Global Foundries' Fab 8: "Lithography is the heart of the fab."

The semiconductor industry development has been following Moore's law in the last 50 years. The development of photolithography technology is the main factor that allows the continuous shrinking of devices (FOMENKOV, 2017), as shown in Figure 3.2. In the late 1970s, the first G-line (436nm wavelength) step-and-repeat system was created. This exposure system quickly has become mainstream and dramatically promoted the capability and efficiency of photolithography (MULKENS et al., 1995). Due to the Rayleigh diffraction effect, a smaller light wavelength needs to be adopted in order to get a reduced feature size with high resolution through a lens system, which makes a semiconductor device smaller. To get even smaller feature size, the light source adopted in photolithography has been continuing switching from excimer laser for i-line (365nm) (KATZ et al., 1993), to krypton fluoride (KrF) excimer laser for 248nm deep ultraviolet (MCCLEARY et al., 1988) and argon fluoride (ArF) for 193nm wavelength (KIM et al., 2001). In that way, 157nm wavelength of F2 excimer laser was supposed to be produced to reach a smaller half-pitch than 65nm (ISHIMARU et al., 2005).

The Extreme Ultraviolet (EUV) lithography was created at the beginning of the 21st century. Almost all key players from the industry and academic institutes have been involved in EUV light source development. The EUV scanners are equipped with a high power EUV light source, which can generate 13.5nm wavelength radiation at high power up to 250W. The EUV lithography system, together with the economic affordable multi-

Figure 3.2: Evolution of lithographic wavelength and technology nodes.



Source: Luong (2018).

patterning technologies, allows that the semiconductor technology nodes can advance to beyond 3nm and extend Moore's Law to the next decades (FUI et al., 2019).

3.1.1 Process Variability Effects on Device Geometry/Physics

Process variability affects the structure of the transistor, changing the electrical properties of a circuit. The main sources of process variability that affect the characteristics and performance of devices are:

1. **Line Edge Roughness (LER):** When variations in the width of a resist feature occur quickly over the length of the feature, this variation is called linewidth roughness. When examining these variations along just one edge, it is called line edge roughness (LER) (MACK, 2006). This effect occurs when the optical lithography stage uses light sources with much longer wavelengths than the minimum characteristics of the technology. When applied to the transistor gate, this variation in critical dimensions can change the channel size, varying the drain current and the threshold voltage. That is, considerably affecting the device's electrical properties and, consequently, the entire circuit's performance. LER becomes important for feature sizes on the order of 100nm or less and can become a significant source of linewidth control problems for sub-50nm devices. It is unclear which process or processes are the primary responsible source of the LER (MACK, 2006). This lithography limitation can be mitigated through new lithography technologies and techniques. Resolution

Enhancement Techniques (RET) are widely used techniques that modify original masks before printed on the wafer (FERLA; FLACH; REIS, 2014). RET utilizes lithography simulation to increase the layout resolution; the objective is to increase the coherence between the intended layout and the actual layout printed. A well-known and commonly applied RET is Optical Proximity Correction (OPC). OPC adds rectangles at locations where defects may occur (FERLA; FLACH; REIS, 2014).

2. **Metal Gate Granularity (MGG):** With the advent of multigate architecture and the adoption of high-k metal as the gate material, Metal Gate granularity (MGG) has become a significant source of variability. Local work-function fluctuations due to the polycrystalline structure of these metals imply variations in the potential surface (BROWN et al., 2010). This source of process variability is assessed in this work and will be better described in the next section.

3. **Oxide Thickness Variation:** The aggressive scaling of MOS devices has resulted in the use of ultrathin gate oxides, which in turn enhanced the device performance. For sub-90nm technologic nodes, the interface introduced between silicon/silicon dioxide and between silicon dioxide/polysilicon causes variations in the gate oxide thickness. As the oxide thickness is very thin in these technologies, any variation affects the entire circuit's performance (MANDAL; PANDIT, 2011), as static power consumption.

4. **Random Dopant Fluctuation (RDF):** With the continuous scaling of MOS dimensions, a radically different concern about Vth variation has emerged. Random dopant fluctuation (RDF) is a form of process variability resulting from variation in the implanted impurity concentration (ASENOV, 1998). Due to the discrete behavior of doping atoms, there is a random statistical fluctuation in the number of dopants with a given volume around the dopant's average (MIZUNO; OKUMTURA; TORIUMI, 1994). In planar MOSFET devices, RDF in the channel region can alter the transistors' properties, mainly the threshold voltage. RDF has a more significant effect on newer process technologies, such as FinFET devices. Besides the addition or removal of a few impurity atoms, the lower total number of dopants can significantly alter the transistor properties. RDF is a local form of process variability, meaning that two neighboring transistors may have significantly different dopant concentrations (ASENOV, 1998).

3.1.2 Process Variability Impact on FinFET Devices

From the beginning of the adoption of FinFET devices in digital circuits, many papers reinforce the relevance of considering the impact of variability on FinFETs. The goal is to estimate how this effect will affect the design of integrated circuits and ensure functional devices (KING, 2005; DADGOUR; DE; BANERJEE, 2008; ENDO et al., 2009; WANG et al., 2011). Initially, the works investigated only the impact on the V_{th} and the I_{on} and I_{off} currents of variations on the main geometrical parameters of the devices.

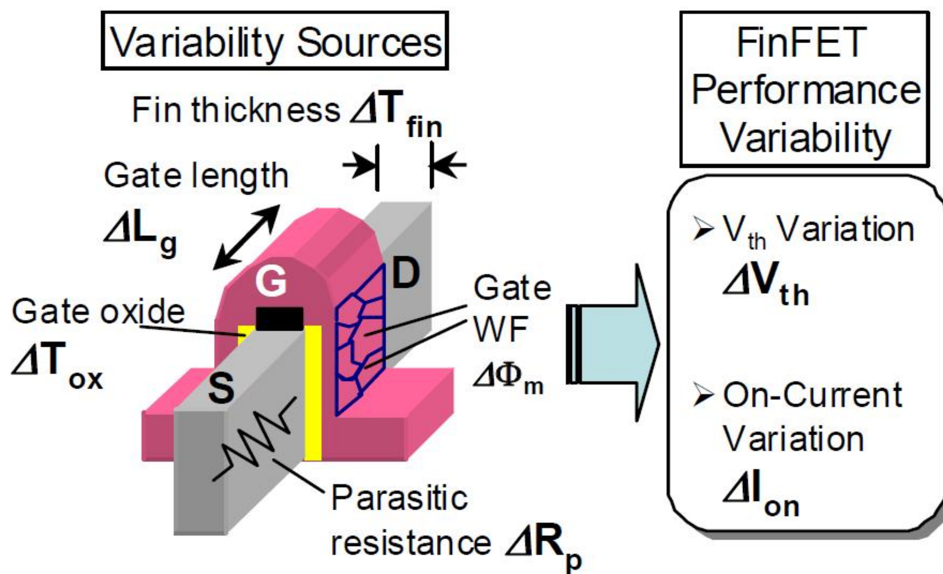
As previously mentioned, the primary sources of process variability at nanometric nodes are due to the sub-wavelength lithography (NASSIF, 2008; DADGOUR et al., 2010), and it is also considered for FinFET devices. The variability on geometric parameters due to lithography directly impacts the V_{th} of the transistor. These variations can compromise the entire blocks of cells or reduce the performance and energy efficiency of the chip.

The work of Topaloglu (2013) points to some expected sources of variability for FinFETs. Among the main sources, are highlighted: the influence of variations in the fins height, the width variations across the double-standard layers, the variations of the fin to fin, the dependent variations in the width of the pitch, the MOL (Middle of Line) resistance, and variations due to the overlap and the epitaxy.

Figure 3.3 summarizes the main FinFET parameters and the possible variability sources that affect the V_{th} and the I_{on} current on FinFET devices (ENDO et al., 2009). The gate oxide thickness is represented by T_{ox} and the parasitic resistance by R_p. The fin thickness and the gate work-function are represented in Figure 3.3 by T_{fin} and Φ_m, respectively. However, these parameters have already been presented and will be cited in work by W_{fin}/T_{si} and WF. Further studies point out that it is no longer sufficient to consider only the fluctuations in V_{th} in the development of EDA designs and tools that consider FinFET technology. It is necessary to consider all the electrical characteristics of these nanometric technologies (MEINHARDT; ZIMPECK; REIS, 2014).

For nanotechnology bulk CMOS devices, the geometric variability in the gate length has the greatest impact on the change of I_{on} current due to the random fluctuation in the dopants of the channel (MEINHARDT, 2014). However, in FinFET devices, another parameter has a more significant impact. As a result of the active format of the fins, the fin channel is weakly doped to minimize variations in V_{th}. As a consequence, the

Figure 3.3: Possible sources of FinFET variability.



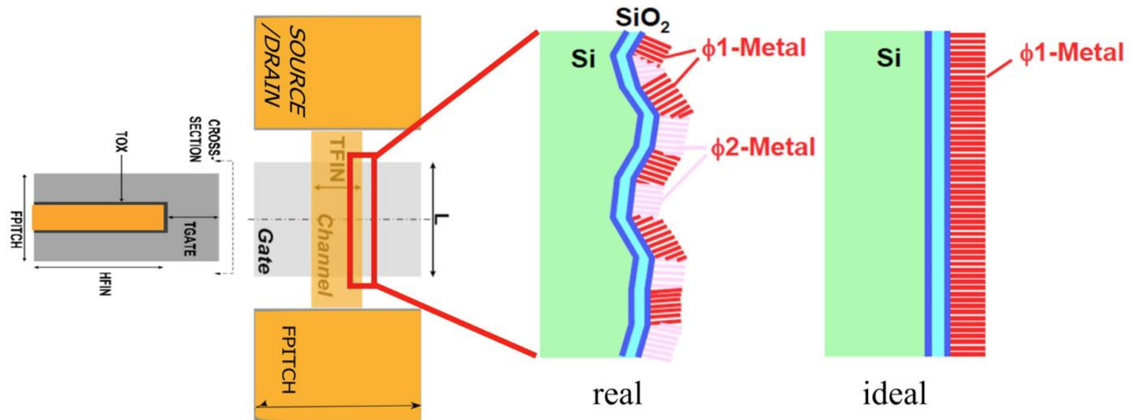
Source: Endo et al. (2009).

V$_{th}$ of weakly doped channels is mainly configured by the work-function of the metals adopted in the gate. The use of metal as gate material introduced some fluctuations in the work-function of the gate, mainly due to the presence of MGG (BROWN; WATLING; ASENOV, 2006; KLEEBERGER; GRAEB; SCHLICHTMANN, 2013).

In the ideal fabrication process, metal gates devices have the gates produced with a unique metal uniformly aligned and very lower work-function deviation. Nevertheless, in a real fabrication process, metal gate devices are generally produced with metals with different WF randomly aligned, which implies higher WFF. WFFs are locally induced due to the polycrystalline nature of the metal lead to potential surface variations, and it is caused by the dependency of metal WF on the orientation of its grains, as illustrates the Figure 3.4. The V$_{th}$ fluctuation due to MGG is close to a Gaussian distribution, and the standard deviation is almost linearly proportional to metal-grain size (DADGOUR et al., 2010; WANG et al., 2011).

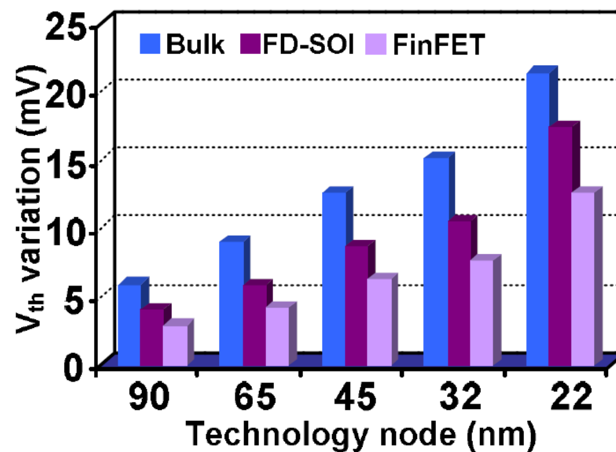
Dadgour, De and Banerjee (2008) evaluated the deviation level of the work-function on various types of CMOS devices with a metal gate. Figure 3.5 shows the comparison of the impact on the threshold voltage due to variations in the process parameters of different technological nodes in CMOS, FD-SOI and FinFET technologies. TiN is the material considered for the gate in the FD-SOI and FinFET technologies. FinFET technology has the least impact on the V$_{th}$.

Figure 3.4: FinFET devices: main geometric parameters and the random alignment of metal in real devices.



Source: Modified from Dadgour et al. (2010) and Meinhardt, Zimpeck and Reis (2014).

Figure 3.5: Variation in the threshold voltage of bulk CMOS, FD-SOI and FinFET devices in different technological nodes.

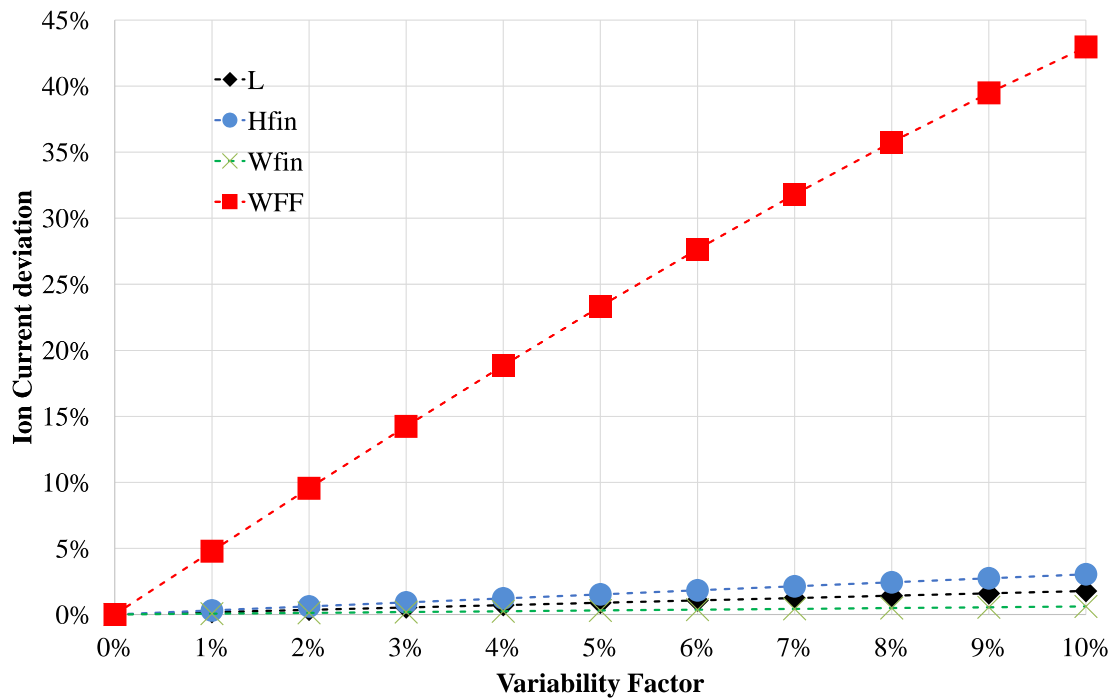


Source: Dadgour, De and Banerjee (2008).

Thus, although variations in gate length, fin height and fin width influence the electric behavior of FinFET devices, the fluctuations of the metal gate work-function are the main source of expected variability for FinFETs sub-20nm (HENDERSON, 2013; SAHA, 2010; MEINHARDT; ZIMPECK; REIS, 2014). Experimental results show that the ASAP7 model reproduces the same behavior, previously found for other multigate technologies (MEINHARDT; ZIMPECK; REIS, 2014), with the WFF effect highly dominating the impact on the I_{on} and I_{off} currents, as shown in Figure 3.6. The impact of the geometric parameters on the I_{on} current, even considering 10% of variability factor deviation, is minimal, reaching less than 5% of the impact. The WFF effect is considerable, even with low levels of work-function fluctuation, introducing about 5% of I_{on} current de-

viation considering a process with only 1% of WFF. The WFF impact grows linearly with the increase in the variability factor (BRENDLER et al., 2019c). Observing the impact of the different variability factors on the I_{on} current, the range between 3%-5% can be determined as the most representative in the I_{on} current deviations. In this range, the I_{on} current deviates between 15% and 25%, which are values according to other experiments in the literature.

Figure 3.6: Impact on I_{on} current due to work-function fluctuation.



Source: Brendler et al. (2019c).

4 RADIATION EFFECTS ON ELECTRONIC CIRCUITS

Anomalies induced by the radiation effects on electronic circuits are known from the beginning of space exploration. The research aimed at the study of the radiation effects on electronic circuits was initially considered a concern of utmost relevance only in projects developed for military or space applications. The first US artificial satellite, Explorer I, designed and built by the Jet Propulsion Laboratory, and launched on January 31, 1958, carried a Geiger counter proposed by J.A. Van Allen. When the spacecraft reached a certain altitude, the counter suddenly stopped counting cosmic rays. From this behavior, the existence of the Van Allen belts was discovered because the counter was in fact saturated by an extremely high particle count rate. The evidence of the existence of trapped particles in Earth's radiation belts can be considered, in this respect, as the very first scientific output of the Space Age (ECOFFET, 2007).

In 1962, the USA proceeded to a high altitude nuclear test in the Telstar telecommunications satellite, designed and built by the Bell Telephone Laboratories with AT&T funds and supported by NASA. The extremely high radiation levels induced by electrons injected in the radiation belts caused degradations of some electronic components (diodes in the command decoder) and, finally, the loss of the satellite in 1963. This was the first spacecraft loss due to radiation effects (ECOFFET, 2007). From this moment on, the effects of radiation (whether natural or man-made) on electronic circuits have come to be studied by the scientific community, space agencies and military agencies.

A new class of effects emerged, starting from first observations in 1978 when Intel Corporation discovered that anomalous upsets occurred at the ground level on dynamic random access memories (DRAMs) (MAY; WOODS, 1978). It was determined that the faults were caused by alpha particles emitted by the decay of the radioactive uranium and thorium elements, which contaminated the encapsulation material in the memory chip manufacturing process. This was the first study published in the International Reliability Physics Symposium (IRPS) and was the first work to define the anomalies as "soft errors". This term was used to differentiate from permanent faults and to characterize the random effects caused by radiation on memory elements.

Guenzer, Wolicki and Allas (1979) reported that the occurrence of SEs could also come from nuclear reactions where proton particles and high energy neutrons are produced. At that moment, the term "single event effects" was introduced, characterizing the effects that are triggered by only one particle. It was established that ions, protons and

neutrons could also produce single event effects, and it soon became one of the significant causes of component dysfunction in space (ECOFFET, 2007).

Most of the research in the 1980s was directed mainly to sequential circuits, such as DRAMs and SRAMs. This was due to the requirement to understand radiation effects and their mitigation to reliably provide data storage (DODD; MASSENGILL, 2003). However, studies focusing on combinational logic circuits began to emerge at the end of this decade in response to the Best Paper of the International Reliability Physics Symposium entitled "Dynamic fault imaging of VLSI random logic devices" by May et al. (1984).

The Earth is protected by the atmosphere, which acts as a semi-permeable "screen", to let throughout light and heat, while stopping radiation and ultraviolet rays (UVs) (BOUDENOT, 2007). The intensity of the radiation basically increases according to the increase in altitude relative to ground level. However, due to phenomena related to the Earth's magnetic field (the polar regions are an example), some regions suffer from a higher intensity of radiation even though they are located at low altitudes.

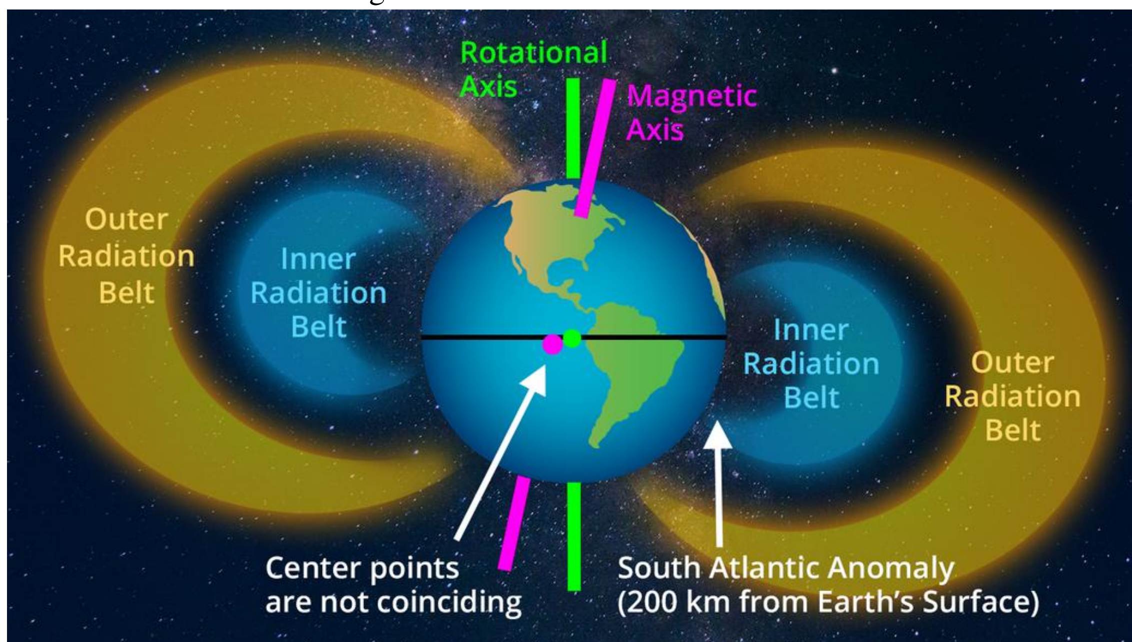
In space and the Earth's atmosphere, there is a diverse range of radiation, which is classified into two broad groups: ionizing particles and non-ionizing particles. Cosmic rays, x-rays and radiations from radioactive materials are examples of ionizing radiation. That is, they produce the emission of electrons when interacted with some material. Examples of non-ionizing radiation are ultraviolet light, radio waves and microwaves, as they are not capable of ionizing any material. The main particles that may cause unwanted effects in electronic circuits are electrons, protons, neutrons, muons, alpha particles and heavy ions, as well as electromagnetic radiation, such as x-rays and gamma rays (STASSINOPOULOS; RAYMOND, 1988). At sea level, muons are the most numerous terrestrial species (SIERAWSKI et al., 2010).

Space radiation consists of subatomic particles (e.g., protons, electrons, neutrons), which may originate from heavy ions present in the space environment or alpha particles emitted from radioactive isotopes. These particles travel in space at very high speeds (near the speed of light), which allows them to easily traverse a material and cause various effects on it. The main components of radioactive phenomena encountered in space can be classified into four categories by origin: Radiation belts, solar flares, solar wind and cosmic rays (BOUDENOT, 2007). These phenomena will be discussed in detail in the next subsections.

4.1 Radiation Belts

Radiation belts are formed in the terrestrial magnetosphere and contain trapped electrons and protons. A layer of charged energetic particles, which are trapped by the influence of a magnetic field, forms a radiation belt. Earth has two of these belts that are known as Van Allen Belts, as shown in Figure 4.1. Most of the particles that form the belts originate from solar flares, solar winds, and also cosmic rays (ALLEN; FRANK, 1959). The inner belt contains electrons whose energy is less than 5 MeV. The outer belt contains electrons whose energy may reach 7 MeV, furthermore in the case of the outer belt, the electron flux is both more variable and more intense than that of the inner belt. Like electrons and protons, heavy ions may also be trapped in the magnetosphere (BOUDENOT, 2007).

Figure 4.1: Van Allen radiation belt.



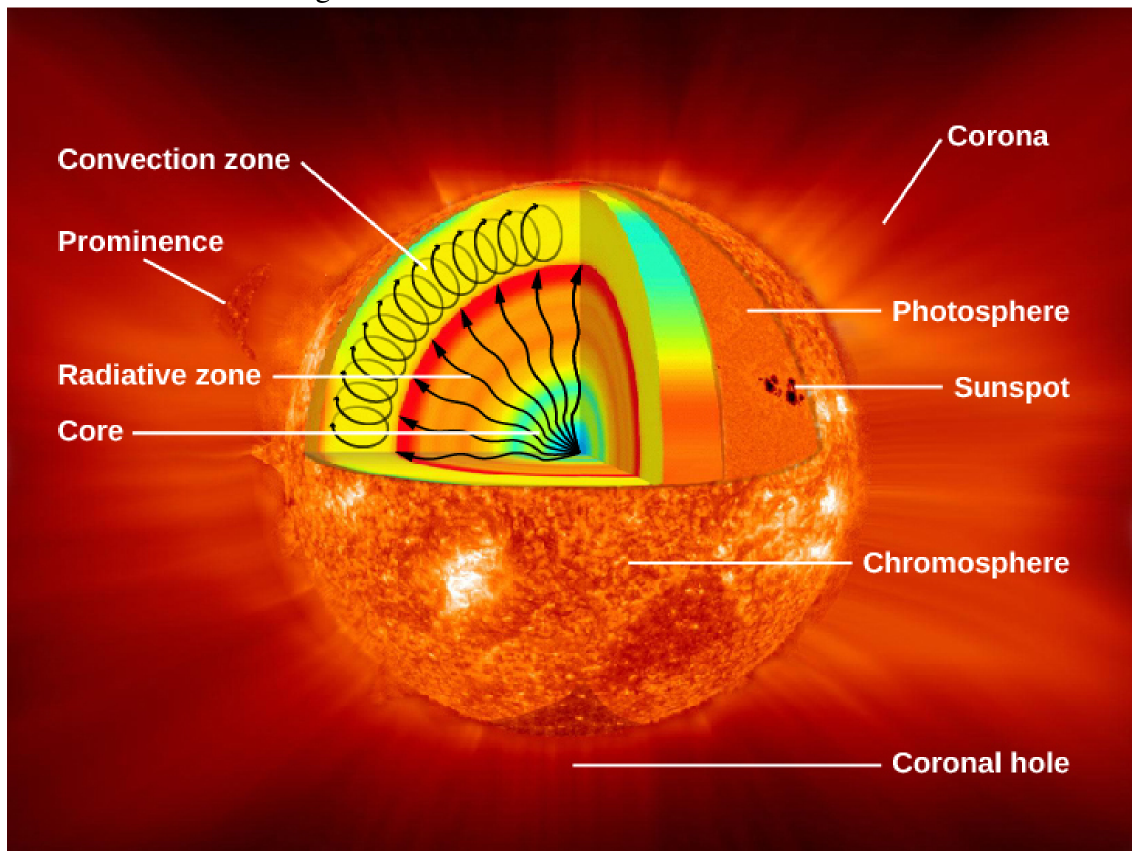
Source: Hamer (2017).

In space missions, Van Allen belts have always been a major concern because of their ability to interfere with the smooth operation of systems and possibly to permanently damage satellite electronics (WALT, 2005). Typical proton energies can reach several hundred MeV and are known to cause effects like TID, SEE and Displacement Damage (DD). Electrons, however, reach energies of some MeVs contributing to effects such as TID, DD and charging and discharging (CUMMINGS, 2010).

4.2 Sun

The Sun, formed over 4.6 billion years ago, is a gaseous sphere composed primarily of hydrogen and helium, in addition to a small amount of heavier elements such as iron, silicon, neon, oxygen, nitrogen, and carbon (LIOU, 2002). Almost all energy received by the planet and that feeds life in the Earth's atmosphere comes from the Sun, making its existence essential for the maintenance of life on Earth. The Sun's energy source comes from within, where due to high temperatures, fusion reactions occur by turning four hydrogen atoms into a helium atom and releasing energy. The solar atmosphere is known as the solar corona and is visible as a weak white halo during total solar eclipses. Through a cross-section, Figure 4.2 illustrates the interior of the Sun, where the reactions responsible for the release of particles of radiation to their atmosphere and the universe occur.

Figure 4.2: Cross-section of the Sun interior.

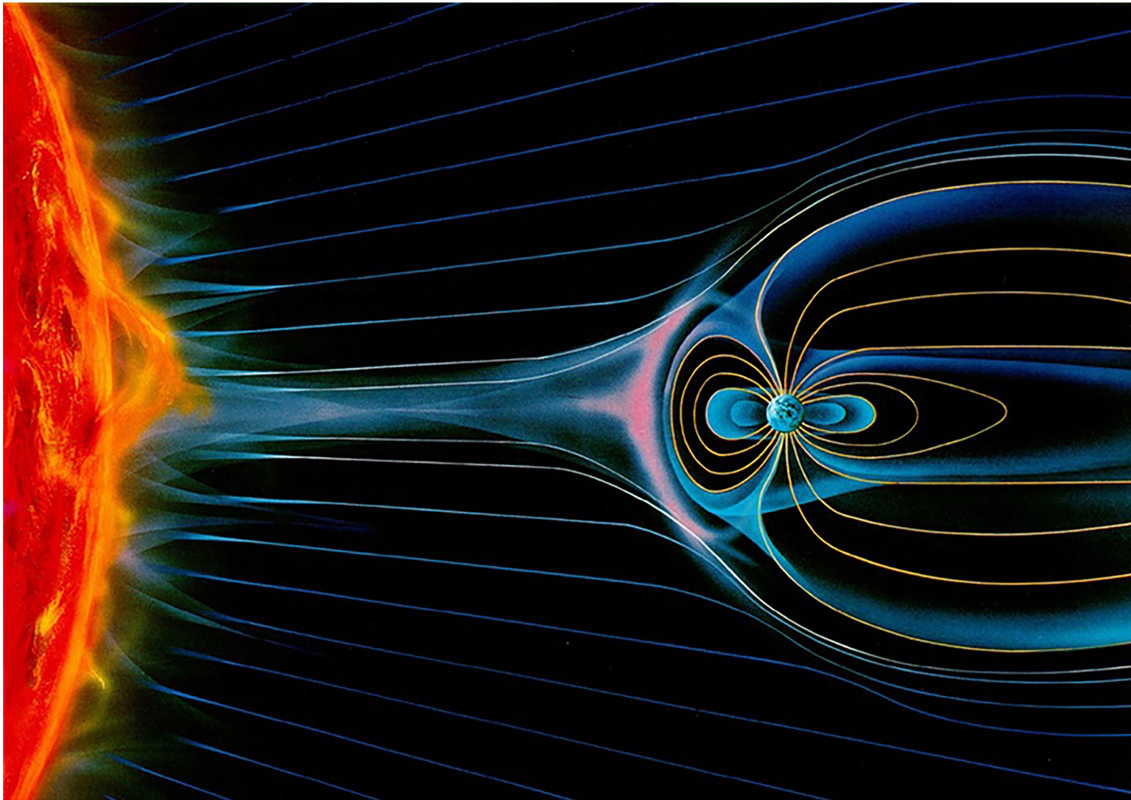


Source: NASA (2008).

4.2.1 Solar Wind

One of the most important events of solar activity is the Solar Wind, which occurs due to the phenomenon of the coronal mass ejection, shown in Figure 4.3. The high temperature of the Sun corona (about two million K) inputs sufficient energy to allow electrons to escape the gravitational pull of the Sun. The effect of the electron ejection's causes a charge imbalance resulting in the ejection of protons and heavier ions from the corona. The particles are homogenized into dilute plasma due to the high temperature of the ejected gas. The energy density of the plasma exceeds that of its magnetic field, so the solar magnetic field is "frozen" into the plasma (BOUDENOT, 2007).

Figure 4.3: Solar Wind.



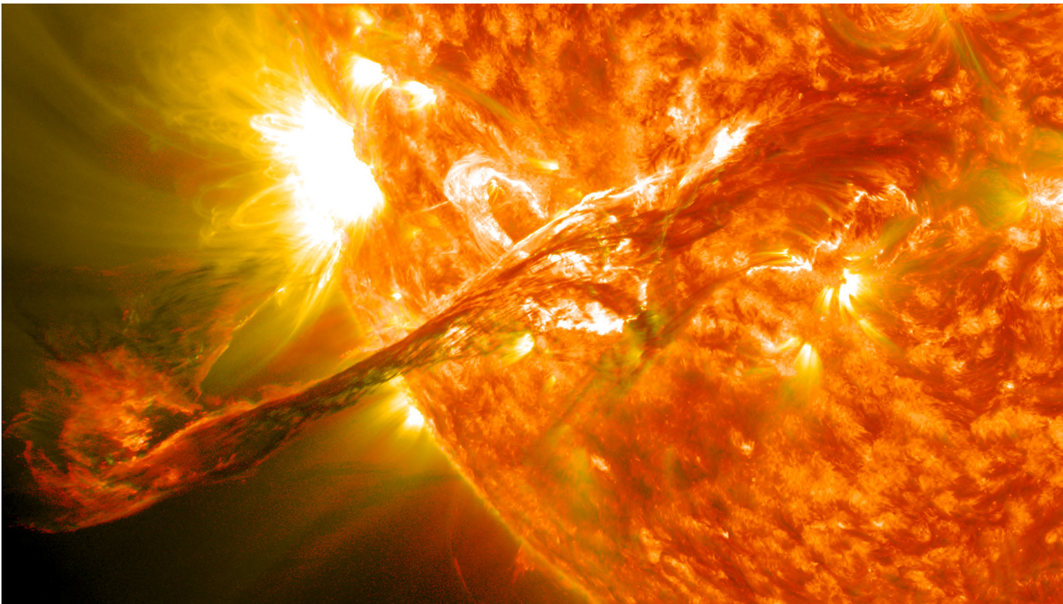
Source: NOAA (2015).

Changes in the solar wind density (e.g., solar flares), the solar wind velocity (e.g., coronal mass ejection's), and the orientation of the embedded solar magnetic field can cause significant perturbations in the geomagnetic field. The coronal mass ejection's and solar flares cause disturbances of the solar wind, and it is the interaction between theses disturbances and the Earth's magnetosphere that causes perturbations called magnetic storms and substorms (BOUDENOT, 2007).

4.2.2 Solar Flares

The solar activity is cyclical, having around 11 years, being on average seven years of high activity and four years of low activity (ASSIS, 2009). When in high solar activity, the surface of the Sun is violently disturbed, causing explosions of particles and radiation. These explosions, known as Solar Flares, emit heavy ions (tens of MeV to hundreds of GeV) in addition to alpha particles and electrons. Figure 4.4 contains a representation of a Solar Flare on the surface of the Sun.

Figure 4.4: Solar Flare.



Source: NASA (2012).

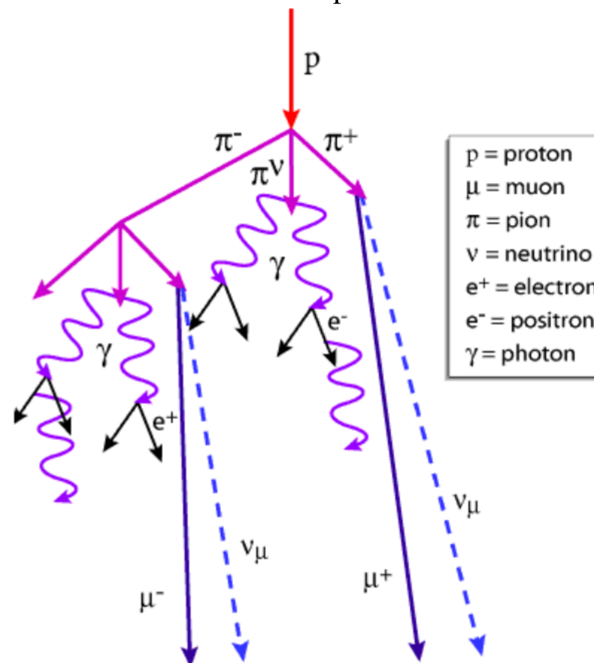
4.3 Cosmic Rays

Galactic cosmic rays consist of high energy particles with a very diverse energy spectrum. The origin of this radiation has not been truly identified; it is known that the most energetic ions come from outside the Milky Way Galaxy and the rest from within it. It is believed that they are produced and accelerated by solar flares, supernovae and galactic nucleus explosions (ZIEGLER, 1996). Cosmic rays correlate with solar activity because, in periods of low activity, the cosmic ray flow that reaches the Earth is greater when in high solar activity (MCDONALD, 1998).

By traveling in space at high velocities and with an enormous amount of energy, when entering the terrestrial atmosphere, the cosmic rays collide with the atoms present

in the atmosphere, provoking cascade nuclear reactions of particles towards the Earth's surface, as shown in Figure 4.5. Cosmic rays of galactic origin are considered primary particles. The secondary particles, coming from the cascade effect, are formed by protons, neutrons, pions and muons (BALEN, 2010). However, from the total particles generated in this cascade effect, only 5% of protons and 1% of electrons and neutrons reach the surface of the Earth at ground level. This is due to attenuation processes and the short life span of these particles (SIMIONOVSKI, 2012). Although the neutron has no electric charge, it has a higher charge generation property compared to the proton and the electron. The neutron does not directly ionize the silicon but interacts with it, causing a nuclear reaction that releases alpha, beta, and proton particles.

Figure 4.5: Nuclear cascade reactions of particles towards the Earth's surface.



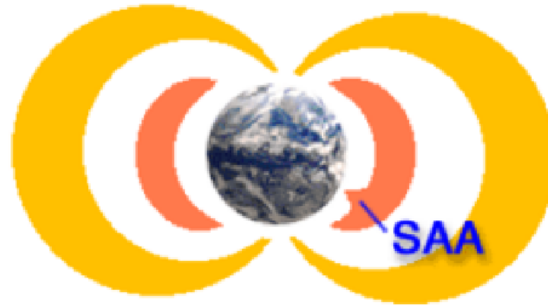
Source: Mészáros, Razzaque and Wang (2015).

4.4 South Atlantic Anomaly (SAA)

After presenting the main components related to the origin of the radiation effects, it is important to highlight an anomaly present in a specific region of the Earth. The slope of the Earth's axis of rotation relative to the axis of the magnetic field influences the distribution of the flux of particles present in the inner Van Allen belt, creating a kind of depression region (BALASUBRAMANIAN, 2008), shown in Figure 4.6. In this region, the radiation trapped by the Earth's magnetic field in the belts reaches lower

altitudes, including penetrating the atmospheric layers. It produces undesirable effects in the electronic equipment of spacecraft and satellites, which fly over southern Brazil and the Atlantic Ocean (BALEN, 2010). This region is known as the South Atlantic Anomaly (SAA).

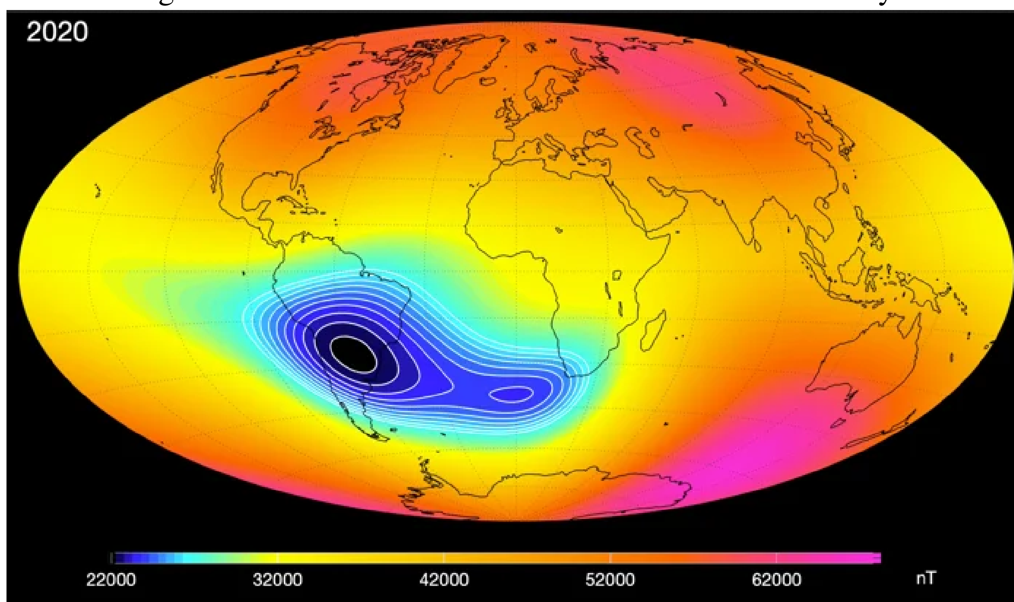
Figure 4.6: Deformation in the inner Van Allen belt of the Earth due to SAA.



Source: Aguiar (2015).

Figure 4.7 shows new satellite data from the European Space Agency (ESA), revealing that the SAA continues to evolve, with the most recent observations showing we could soon be dealing with more than one of these strange phenomena. ESA says that in the last two centuries, Earth's magnetic field has lost about 9 percent of its strength on average. The minimum field strength in the SAA dropped from approximately 24.000 nT to 22.000 nT over the past 50 years. New readings provided by the ESA's Swarm satellites show that within the past five years, the second center of minimum intensity has begun to open up within the anomaly beside Africa.

Figure 4.7: Current scenario of the South Atlantic Anomaly.



Source: ESA (2020).

4.5 Characterization of the radiation effects on electronic devices

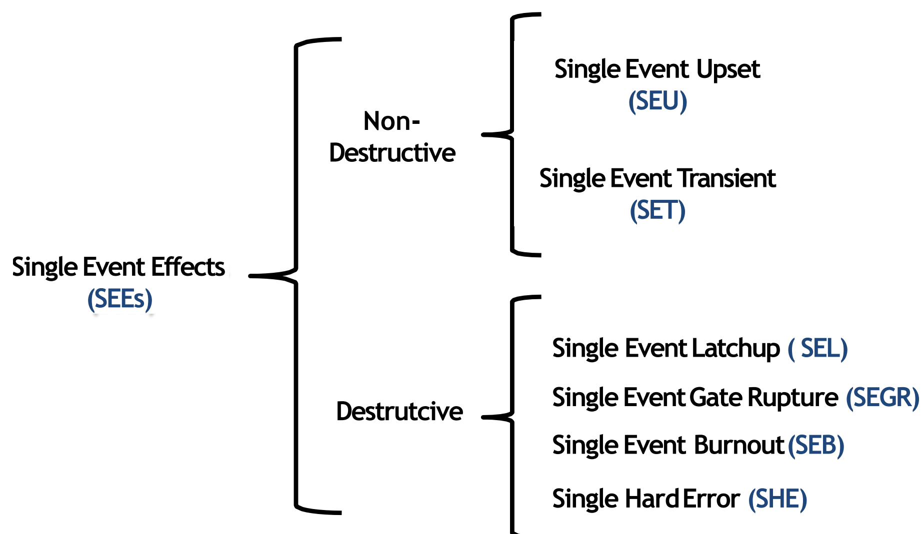
The effects of radiation affecting the operation of electronic circuits can be classified into three broad groups:

1. **Total Ionizing Dose (TID):** cumulative effects that occur due to the exposure of integrated circuits to radiation over time. They are produced after an ionizing particle reaches the surface of a device and are not undone over time, i.e., long-term effects in which its intensity depends on the intensity of the radiation and the time the circuit was exposed to this radiation (VELAZCO; FOUILLAT; REIS, 2007).
2. **Displacement Damage (DD):** causes physical damage to the crystalline structure of the material (silicon in the case of the semiconductors of interest in this work) caused by non-ionizing energy loss (NIEL) of the incident particles on the material, degrading the material and their properties.
3. **Single Event Effects (SEEs):** are effects that occur due to the bombardment of energized particles (electrons, protons, alpha particles and heavy ions) that reach the silicon, ionizing it densely and releasing energy that can damage the circuits permanently or induce transient behavior, affecting the proper functioning of the device. SEEs can be classified as destructive and non-destructive (DODD et al., 2004; CUMMINGS, 2010; AZAMBUJA; KASTENSMIDT; BECKER, 2014):
   (a) **Destructive:** are effects that permanently damage the circuit. The four main effects are: **Single Event Latchup (SEL)** occurs when the incidence of the particle causes an abnormal increase in the operation current and may cause permanent damage to the device; the **Single Event Gate Rupture (SEGR)**, which the gate oxide is damaged forming a conductive path; **Single Event Burnout (SEB)** when the particle reaches the source region of the transistor creating a current between the source and the drain. This current can generate a destructive fault in the device, the device literally burnout; and **Single Hard Error (SHE)**, the deposition of large loads of energy can damage the ability of transistors to transition state. In Sexton (2003) destructive SEE mechanisms are reviewed and discussed.
   (b) **Non-destructive:** are also commonly known as **Soft Errors**. They can also be classified into two types depending on the nature of the element reached: **Single Event Upset (SEU)** when the element hit is a sequential element, for

example, a flip-flop, modifying the state of a stored bit (bit flip); and **Single Event Transient (SET)** If the particle reaches a combinational element, for example, a multiplexer, a transient pulse is generated that may or may not be captured by a memory element.

Figure 4.8 presents the classification of the major SEEs in the literature. The focus of this work are the SET effects that occur in combinational circuits. The next section presents more details of SEEs, highlighting the SET.

Figure 4.8: Classification of major Single Event Effects.

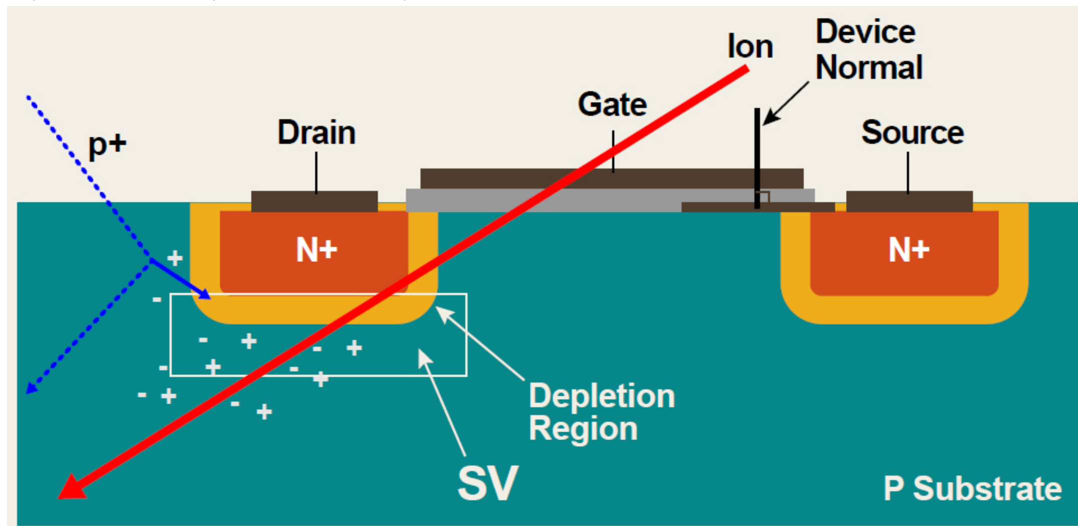


Source: Adapted from Siegle et al. (2015).

4.6 Single Event Effects (SEE)

The Single Event Effects occur due to the interaction of large ionizing particles (protons, neutrons, alpha particles and heavy ions) that pass through insulation, semiconductor layers, or even all MOS device (DODD et al., 2004). Figure 4.9 shows the SEE through the impact of an ionizing particle on the device structure. When the particle enters the silicon material, a transient path composed of ionized elements (electron-hole pairs - e^-/h) is generated. This path is arranged under a radial distribution that permeates the path of the incident particle. This transient path may have a sufficient mobile charge to drive a current pulse against the presence of the external electric field due to the polarization of the transistor.

Figure 4.9: Single Event Effects - an ionizing particle passing through a sensitive volume (SV) in an active (semiconductor) device.



Source: TNA (2018).

SEEs indicate any measurable or observable change in a state or performance of a microelectronic device, component, subsystem or system (digital or analog) as a result of the incidence of a single energetic particle. According to the intensity and the region in which this current flows, it is capable of causing faults that may be permanent in the device structure, called destructive events (hard errors), or non-destructive events (soft errors), represented by the Single Event Transient and the Single Event Upset (SEU) (MUNTEANU; AUTRAN, 2008).

The main difference between the two non-destructive events is the incidence location of the particle. If the current pulse occurs within a sequential circuit, such as latches or flip-flops, the stored original value can be inverted, producing an SEU or bit-flip (BRAMNIK; SHERBAN; SEIFERT, 2013). Similarly, the SET also generates a pulse, but its origin is by the impact of particles within a combinational circuit. If the pulse generated in a combinational circuit propagates to a sequential circuit, a SET can become a SEU.

The SEUs, unlike the SETs, have a non-transient character. They are associated with the bit inversion of memory elements. SEU may have an indefinite duration or be corrected after one or more clock cycles. As this work focuses on the SET analysis, this effect will be described in detail. However, a brief description of the destructive events will be presented first.

4.6.1 Destructive Events

Unlike the SETs, destructive events permanently damage the device. As mentioned earlier, these effects are not part of this work scope, but they will be briefly described. The destructive events are classified into several different types, such as: Single Event Latch-up (SEL), Single Hard Error (SHE), Single Event Burnout (SEB), and Single Event Gate Rupture (SEGR). The last two effects will be better described below:

(a) Single Event Burnout: occurs when the passage of a high energy ion through the device causes the generation of a dense plasma of e^{-}/h h pairs which, under the influence of polarization of the drain terminal, produces a high-density current. This resulting current, if it is not quickly drained, can generate a destructive fault on the device, causing its "burnout" (SEXTON, 2003).

(b) Single Event Gate Rupture: due to the reduction of transistors dimensions in recent technologies, the thickness of the gate oxide has also been significantly reduced. This reduction increases the electric field of the oxide since this is inversely proportional to the thickness of the dielectric. Thus, perturbations in the electric field that permeates the oxide can cause that it exceeds its dielectric rigidity, causing its rupture.

4.6.2 Single Event Transient

The SET is a transient that can propagate as a voltage or current pulse and occurs when the particle strikes at sensitive nodes of combinational elements of a circuit (SIMIONOVSKI, 2012; BAZE; BUCHNER, 1997; SAVAGE et al., 2001). To quantify the SET effects, characteristics such as amplitude, shape and current pulse duration are important quantities (BALEN, 2010).

To the extent that the SET propagates along the signal path, the pulse may have its width reduced or even increased (FERLET-CAVROIS et al., 2007) (WIRTH; KASTENSMIDT; RIBEIRO, 2008). This is due to the different propagation delays of the rising and falling of the gates that make up the circuit (parameters that depend on the load to which each gate is subjected and the sizing and technological parameters of the transistors). The pulse caused by the SET can still be attenuated in its amplitude, along the combinational circuit, reaching a memory element with a small amplitude. In this case, the pulse will

not be captured by the register, causing the electric masking. As already mentioned at the beginning of this work, another type of masking is the logical masking, characterized by the fact that it prevents a SET from propagating itself to a memory element, because it occurs or propagates itself through non-sensitized paths of combinational logic (ENTRENA et al., 2009).

The pulse propagated after the occurrence of a SET, even when not masked by the mechanisms described herein, may still undergo masking by a latching window. In this case, even by temporarily reversing the logic level at the input of a register, the pulse occurs outside the signal capture time interval. The greater the SET pulse width, the less likely it is that temporal masking occurs because the probability of the pulse being captured increases (BALEN, 2010).

The amplitude and duration of a SET depend on factors such as fabrication technology, circuit geometry, the bias voltage of the affected node, node load impedance, location of the transistor reached by the particle, in addition to factors related to the SEE itself, as the type and energy of the incident particle (BALEN, 2010).

4.6.3 Physical Mechanisms of Deposition and Charge Collection

Soft errors occur when energetic particles interact with silicon colliding with a sensitive area of the circuit and depositing an additional charge on the transistor's P-N junction region. There are basically two mechanisms of charge deposition attributed to the interaction of radiation with the silicon of a chip (DODD; MASSENGILL, 2003):

1. **Direct Ionization**: when a charged particle travels through a semiconductor material, it loses energy along its path, transferring it to the device and creating a path formed by electron-hole pairs. This resulting ionizing track, when collected by the electric field of the device, generates a transient current/voltage. Direct ionization is considered as a primary mechanism of charge deposition caused by the incidence of alpha particles or heavy ions. Lighter particles such as protons do not produce enough direct ionization charge to generate an observable transient pulse.
2. **Indirect Ionization**: it is a secondary mechanism of charge deposition, where due to nuclear reactions in the semiconductor material, light particles such as protons and neutrons can release energy in the silicon through secondary particles product of the nuclear reaction. That is, once a nuclear reaction has occurred, the charge

deposition can occur by particles product of this reaction.

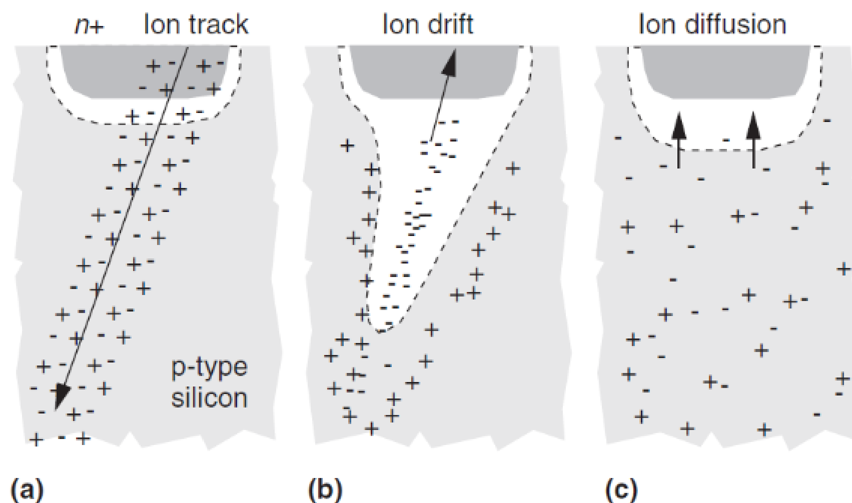
The energy deposited by a particle due to its ionization in silicon is an important metric in the study of radiation effects in nanotechnologies because it is directly related to the magnitude of the generated transient pulse. Linear Energy Transfer (LET) (shown in Equation 4.1) is the amount of energy that a particle releases per unit of compliance of the path traveled by it.

$$LET = \frac{\partial E}{\partial x} \tag{4.1}$$

The LET is dependent on the mass and energy of the particle and the ionized material, so particles with higher mass and energy ionized in denser materials have higher LETs (BAUMANN, 2005b). LET_{th} is the minimum LET to cause an effect in the circuit (FERLET-CAVROIS; MASSENGILL; GOUKER, 2013). This an important metric to evaluate the impact of radiation effects on the circuits, and it is used in two experiments of this work.

After the ionization of the particle in the silicon, i.e., after deposition of an additional charge on the affected device, the process of charge collection proceeds through two main mechanisms: Drift and Diffusion. Figure 4.10a shows the resulting ionization path crossing the depletion region formed at the p-n junctions. At the moment that this path crosses, or approaches, the depletion region, the additional carriers deposited by the ion are rapidly collected by the high-intensity electric field in this region (MUNTEANU; AUTRAN, 2008). This charge collection process is called Drift, and it is represented in

Figure 4.10: Charge Collection Mechanisms due to an Ion strike in a P-N junction.

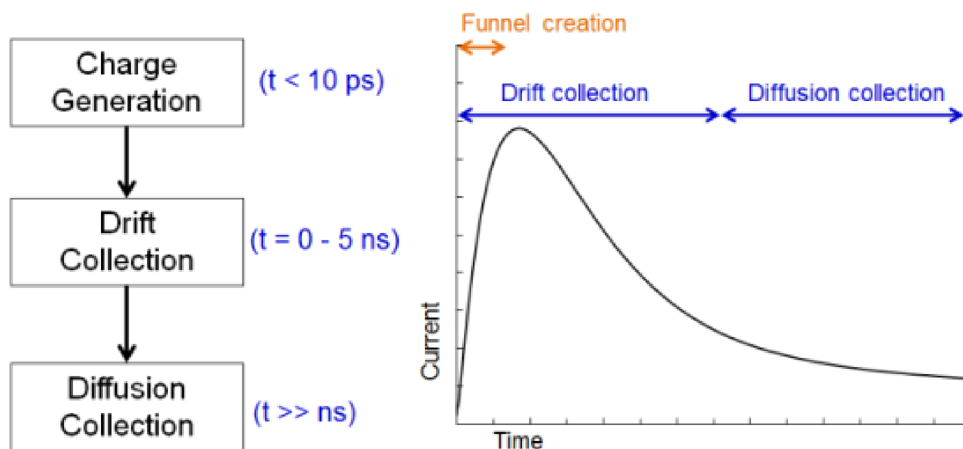


Source: Baumann (2005b).

Figure 4.10b. The passage of the particle through the depletion region is responsible for its temporary (in a matter of picoseconds) deformation. The deformation has the format of a funnel, and for this purpose, it is known as the Funneling Effect. This effect leads to an increase in the charge collection efficiency due to the rise of the depletion region area (BAUMANN, 2005a). Finally, the Diffusion process is responsible for collecting all the remaining carriers that were generated besides the depletion layer (Figure 4.10c).

The typical waveform of the resulting current from the charge collection induced by the incidence of a particle can be seen in Figure 4.11. The Drift and Funneling are very rapid processes, almost instantaneous due to the deformation of the electric field of the junction and the consequent increase in charge collection efficiency. Therefore, these processes are responsible for controlling the rapid rise of the transient current pulse, as seen in Figure 4.11. In the Diffusion process, a longer time is needed to collect the charge, causing the transient current pulse has a slow fall time.

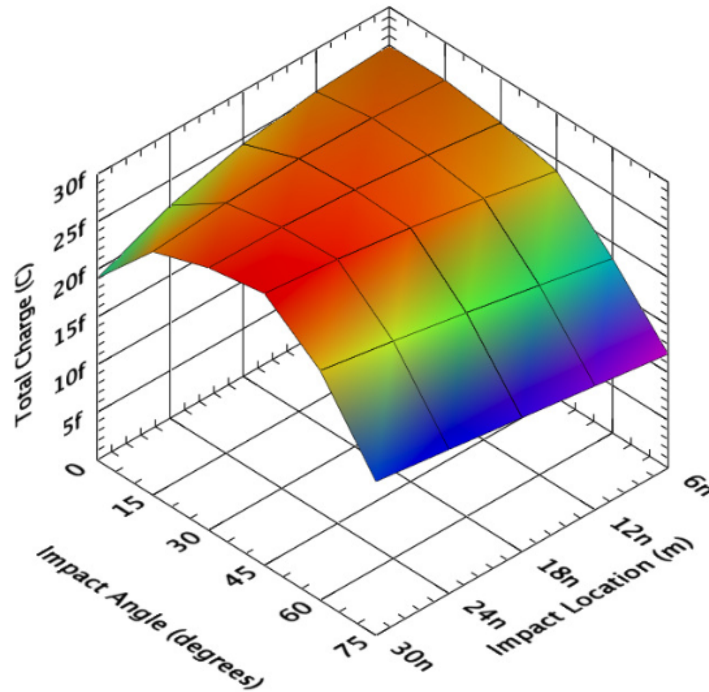
Figure 4.11: Transient Current Waveform induced by a radiation strike.



Source: Cummings (2010).

The collected charge is also dependent on the impact angle of the particle on the device and the channel distance. The work of Bartra (2016) analyzes particle impacts on the elevated source and drain terminals considering three devices with six different impact angles (0°, 15°, 30°, 45°, 60°, and 75°) in five different locations from the silicon nitride separator for each angle (6nm, 12nm, 18nm, 24nm, and 30nm). Figure 4.12 presents the collected charge results considering the heavy-ion impact of 100Mev.cm^2/mg on a 32nm Bulk CMOS transistor. The collected charge tendency, in these conditions, is to decrease when the impact is close to the nitride separator, and the impact angle is increased (BARTRA; VLADIMIRESCU; REIS, 2016).

Figure 4.12: Results of the collected charge from the heavy-ion impact at the drain terminal on the 32nm Bulk CMOS device.



Source: Bartra (2016).

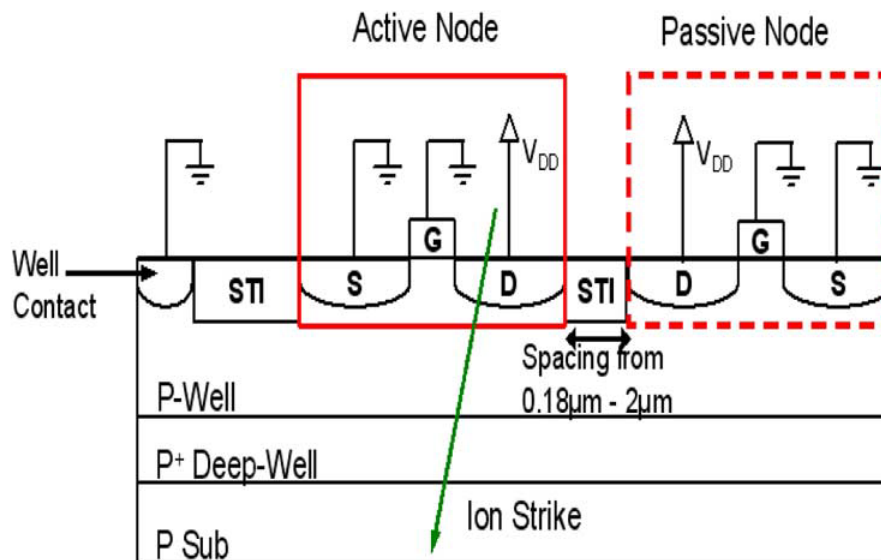
The transient pulse is generated by the interaction of energetic particles near a sensitive region of a transistor when the collected charge (Q_{coll}) exceeds the critical charge (Q_{crit}). However, in sub-22nm technological nodes, other phenomena must also be considered in the characterization of the transient pulse. The influence of the charge-sharing mechanism does not seem to have diminished for FinFET technology. TCAD results show the extent of electrical perturbations and charge-sharing, similar to what has been observed for older technologies. This effect can cause the pulse quenching in ion-induced transients, resulting in a reduced overall sensitivity of the system against SEE (BHUVA et al., 2015). These effects will be better described in the next section.

4.6.4 Emerging Effects at Advanced Technologies

The high-density integration and reduction of the nodal capacitances have enhanced the charge sharing effect at advanced technologies, increasing the susceptibility to radiation effects (OLSON et al., 2005). The charge sharing effect is characterized by the close proximity of adjacent devices, leading to the multiple node charge collection from a single ion strike. Figure 4.13 presents this effect through two adjacent NMOS devices.

As the distance between devices is reduced, an active node, i.e., the stroke node by the ion incidence and actively collecting the deposited charge, is in close proximity to an adjacent node. That way, carriers may be able to diffuse at the passive adjacent node and induce a secondary transient current pulse (AMUSAN et al., 2006).

Figure 4.13: Nodal separation setup for NMOS charge sharing.

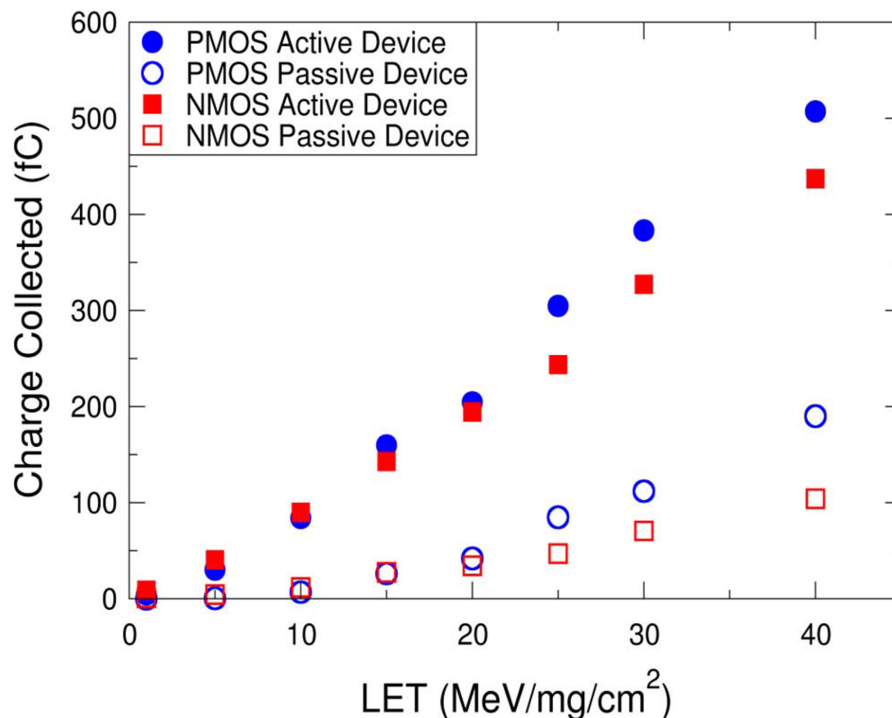


Source: Amusan et al. (2006).

The work of Amusan et al. (2006) investigates the charge collection of the PMOS and NMOS devices. The active and passive device collected charges are shown in Figure 4.14. The passive PMOS device can collect 40% of the total charge collected by the active device, while the passive NMOS collects less than 25% of the total charge. Besides the carrier diffusion process, the bipolar amplification effect is also responsible for the enhancement of charge sharing, explaining the higher collected charge for the passive PMOS device than for the passive NMOS device (AMUSAN et al., 2006; LIU et al., 2009).

The charge sharing mechanism can be considered an adverse effect due to the number of adjacent nodes affected when an ion impacts a single node. However, some researchers have noted that the charge sharing can also reduce the SET pulse width in combinational cells (AHLBIN et al., 2009; ATKINSON et al., 2011). As the signal propagation time is reduced in deeply scaled technology, the multi-collection process provided by charge sharing occurs with a similar time constant. This phenomenon can lead to shortening the SET pulse width, and it is known as the Pulse Quenching Effect (AHLBIN et al., 2009; AHLBIN et al., 2010).

Figure 4.14: Charge collection with distance of $0.18\mu m$ between adjacent devices.

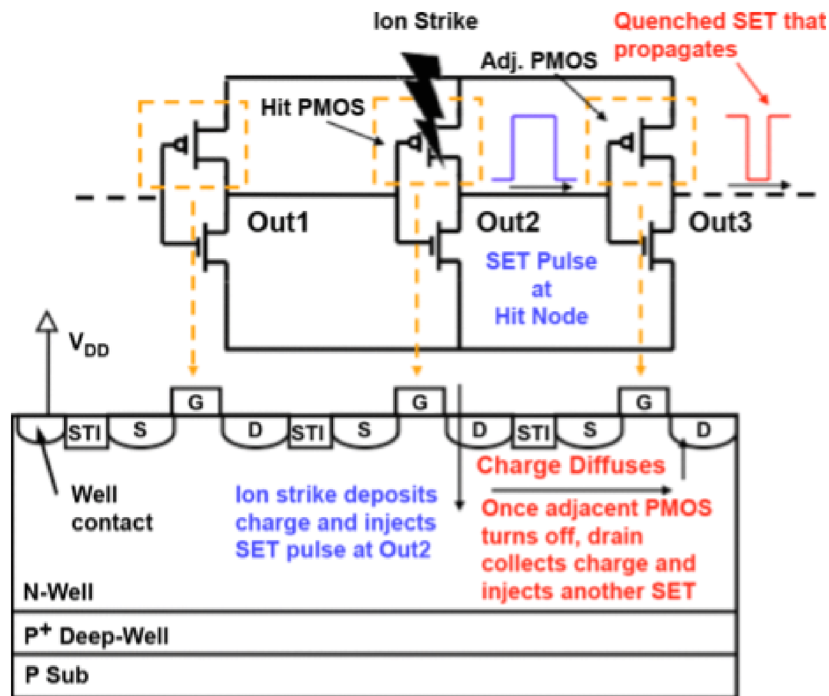


Source: Amusan et al. (2006).

Figure 4.15 shows the schematic of a three-stage inverter chain and its respective PMOS transistors in a cross-section perspective. Considering that the input signal of the first inverter is at the low level, it will lead to the PMOS device of the second inverter to turn OFF while the first and third PMOS devices are ON. If an ion strikes the sensitive off-state PMOS transistor of the second inverter, as in Figure 4.15, the resulting SET pulse at OUT2 will propagate to the next inverter, turning the adjacent PMOS device OFF. Thus, the third PMOS device will be susceptible to the charge collection by diffusion of the carriers from the charge sharing mechanism. This effect occurs due to the delayed charge collection at the stroke device and the propagation of the generated SET to the adjacent device. This process allows the third PMOS to collect the carriers from charge sharing effect and inducing a transient pulse to revert the output of the chain, as also shown in Figure 4.15.

As this work studies the effects of transient faults on FinFET devices, it is important to highlight the differences in the SET impact on this technology. The disruptive nature of the FinFET structure introduces questions in terms of understanding, predicting and mitigating SEEs in circuits. The 3D structure of FinFET devices is favorable to reduce the soft error vulnerability according to several works available in the literature (EL-MAMOUNI et al., 2011; SEIFERT et al., 2012; LEE et al., 2015; NSENGIYUMVA et al.,

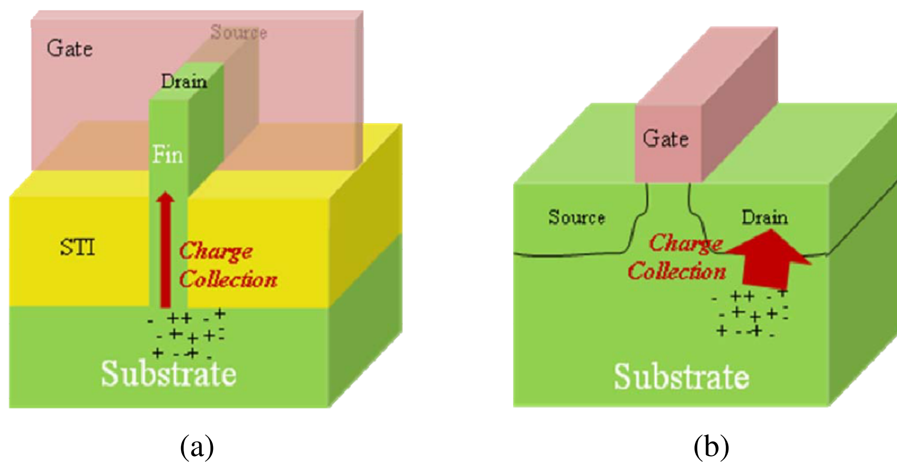
Figure 4.15: SET Pulse Quenching Effect in a inverter chain.



Source: Ahlbin et al. (2009).

2016). This reduction of the soft error vulnerability happens because the sensitive areas of FinFETs are little exposed to the charge collection region, as shown in Figure 4.16.

Figure 4.16: Comparison between 3D structures of (a) FinFET and (b) Planar Transistor.



Source: Lee et al. (2015).

The charge collection processes and the resulting sensitive area for individual transistors are essential for SEE modeling and predictive analysis for circuits. FinFET technologies collect significantly less charge than conventional planar technologies. The work of Fang and Oates (2011) indicates that charge collection for semiconductor regions in FinFET technologies is approximately reduced by 70% compared to planar technologies.

Although FinFET technology is more robust to soft errors than planar technologies, there are still many concerns that justify the study of this device. The process variability, one of the main challenges in sub-22nm technologies, can modify the LET$_{th}$ to induce a soft error. Ultra-Low-Power (ULP) circuits are increasingly being used, and low voltages increase the probability of SE occurrence. Also, with the demand for devices increasingly faster, the operation frequency increases, also increasing the possibility of a memory element capturing a SE. From a design standpoint, the accurate estimation of SEE susceptibility is crucial to ensure reliable circuits.

5 RELATED WORK

This work discusses two significant reliability challenges on the design of integrated circuits: the process variability and the radiation effects, focusing on transient faults. As mentioned earlier, few papers in the literature deal with these two effects together; however, several papers treat them separately. This chapter highlights the researches closer to the scope of this work and the state-of-the-art focusing on FinFET devices.

The work of **Nassif (2008)** and the work of **Orshansky, Nassif and Boning (2008)** serve as the theoretical basis for this work about the concepts presented on the process variability effects. In both works, the sources and characterization of the variability in the manufacturing process of integrated circuits are reviewed. Nassif (2008) uses CMOS technology with SOI substrate in three technological nodes (90nm, 65nm and 45nm) and compares three different circuits (SRAM, Inverter and Latch) regarding the variability impact on their performance. The conclusion is that the process variability impact increases as the technology shrinks and changes its character from parametric faults to catastrophic faults. The work of Orshansky, Nassif and Boning (2008) addresses in more detail all the sources, characteristics, analysis and design techniques to deal with the variability effects. The primary objective of this book is not to present simulation and tests with different technologies and circuits. The central premise is that variability must be rigorously described as random or systematic before meaningful steps can be taken to mitigate its impact on design procedures.

Still on the process variability effects, one can highlight the work of **Silva, Reis and Ribas (2009)**. This work analyzes the impact of the threshold voltage variation on the behavior of CMOS logic gates using different transistor arrangements and the relative position of the switching transistor about the power and output terminals. The significant contribution of this study to the current work is that transistor arrangements that use basic gates present a reduction in the propagation times deviation. Also, the work evaluates AOI type gates and transistor arrangements that use NAND2 gates.

The work of **Meinhardt, Zimpeck and Reis (2014)** compares the impact of process variability on I_{on} and I_{off} currents using FinFET technology in a set of technological nodes ranging from 20nm to 7nm. The prominence is in the evaluation of the Metal Gate Granularity (MGG) impact on the work-function (WF) of the gate. The results demonstrate the importance of not only evaluating variations in V_{th} but also in other parameters.

The significant influence of WFF in the threshold voltage and the I_{on} and I_{off} currents is also presented.

Zimpeck et al. (2018) evaluates a set of complex cells with different transistor arrangements, based on the transistor reordering technique, under nominal conditions and considering the gate variability at the layout level. The objective is to verify what topology is more appropriate to increase the robustness to process variability effects. The first conclusions are about the importance of investigating the effects caused by the process variability on FinFET technologies, as the electrical characteristics of circuits suffer significant changes. Results show that it is difficult to highlight a transistor arrangement as the best option, regardless of the logic function. In general, the best choice is to use the network that the series transistor is as far as possible to the output node. However, a trade-off needs to be done due to performance and power consumption penalties.

In addition to the variability impact on the circuits, many papers analyze the radiation effects. The works of **Naseer et al. (2007)** and **Keane et al. (2007)** facilitate the characterization of radioactive events through critical charge modeling. Both works present the double exponential model. This model has been widely used in the literature to find the critical charge and also simulate the SET pulse introduced by ions in combinational logic. Naseer et al. (2007) evaluates the soft error rate (SER) on SRAM cells through 3D TCAD simulations in 90nm technology. In Keane et al. (2007), a new model, to measure the critical charge, is compared to the ideal model that uses the double exponential. The most important of these two works is the presentation of the most used model in the literature to characterize the SETs (double exponential).

Although the focus of **Balen (2010)** is the programmable analog devices, its theoretical basis presents several of the concepts used in this work. The radiation effects on electronic circuits are described since their origin, clearly detailing the SEEs. The work still presents a section dedicated to radiation protection techniques for electronic circuits, also describing each of the techniques at their different levels.

The paper of **Artola, Hubert and Alioto (2014)** has some characteristics in common with this work. The work presents a comparative soft error evaluation of logic gates in bulk FinFET technology using various technological nodes. SETs induced by radiations are modeled with the MUSCA SEP3 tool, which explicitly accounts for the layout and the electrical properties of transistors. Good agreement between the calculated transient current and TCAD mixed-mode simulations is demonstrated. Besides the utilization of Bulk FinFET technology and the SET response analysis, the work of Artola, Hubert

and Alioto (2014) is also performed at the layout level and uses the LET as metric (similar to this work). However, the main objective of Artola, Hubert and Alioto (2014) is allowing for estimating the SER of logic gates for ground applications, as well as for understanding the impact of voltage and drive strength through analysis of the sensitivity to soft errors.

Zimpeck et al. (2019) evaluates circuit-level techniques to mitigate soft errors in FinFET logic gates. Besides the use of the transistor reordering technique, also explored in this dissertation, other techniques, such as the decoupling cells and the sleep transistors, are evaluated. All the techniques tend to decrease the sensibility to soft errors. For instance, decoupling cells increase the total capacitance in the output node of a certain logic gate, decreasing the critical charge required to produce a SET pulse. However, except for transistor reordering, these techniques present some penalties, mainly related to the circuit area. So, it is important to know the design objectives to choose the best option.

Tables 5.1, 5.2 and 5.3 present comparisons between the analysis carried out in the recently presented works and this dissertation. The works of **Orshansky, Nassif and Boning (2008)** and **Balen (2010)** were not included in the comparison, as they serve as a theoretical basis for this dissertation, in addition to not presenting experiments compatible with this work.

Half of the related works carry out their experiments in planar CMOS technology, and the other half use FinFET devices, such as this dissertation. Most works evaluate only one type of circuit; this dissertation evaluates in addition to a set of logical functions, different versions of C17 benchmark and majority voters.

Table 5.1: Comparison between related works and this dissertation: Technology and Circuits.

Related Works	Technology	Circuits
NASSIF (2008)	(45nm - 90nm) SOI CMOS	SRAM, Inverter and Latch
SILVA ET AL. (2009)	45nm Bulk CMOS	Logic Gates
MEINHARDT ET AL. (2014)	(7nm - 20nm) Bulk FinFET	Transistor-Level
ZIMPECK ET AL. (2018)	7nm Bulk FinFET	Logic Gates
NASEER ET AL. (2007)	90nm Bulk CMOS	SRAM cells
KEANE ET AL. (2007)	65nm Bulk CMOS	Flip-Flop and SRAM
ARTOLA ET AL. (2014)	(32nm - 65nm) Bulk FinFET	Logic Gates
ZIMPECK ET AL. (2019)	7nm Bulk FinFET	Logic Gates
THIS THESIS	7nm Bulk FinFET	Logic Gates C17 benchmark Majority Voter circuits

Source: From the author.

Unlike related works, this dissertation evaluated two reliability challenges: SET and process variability. Besides, the relationship between these challenges is assessed through the SET response under process variability analysis. The objectives and techniques considered by the works are varied. In this dissertation, it is evaluated three different techniques to deal with reliability challenges.

Table 5.2: Comparison between related works and this dissertation: Reliability challenges evaluated.

Related Works	Reliability Challenges Evaluated
NASSIF (2008)	Variability in key parameters
SILVA ET AL. (2009)	Variability through threshold voltage variation
MEINHARDT ET AL. (2014)	Process Variability through different metrics
ZIMPECK ET AL. (2018)	Process Variability through the WFF of the metal gate
NASEER ET AL. (2007)	SEU through the Qcrit, SER and LET
KEANE ET AL. (2007)	SEU through the Qcrit and SER
ARTOLA ET AL. (2014)	SET through the SER
ZIMPECK ET AL. (2019)	SET through SER and LET
THIS THESIS	Process Variability through the WFF of the metal gate SET through the LET_{th} and SET pulse width SET under process variability

Source: From the author.

Table 5.3: Comparison between related works and this dissertation: Objectives/Techniques to deal with reliability challenges.

Related Works	Objectives/Techniques to Deal With Reliability Challenges
NASSIF (2008)	Variability impact on different technologic nodes
SILVA ET AL. (2009)	Transistor Arrangement/Transistor Reordering
MEINHARDT ET AL. (2014)	Impact of the evaluated metrics on Ion and Ioff currents
ZIMPECK ET AL. (2018)	Transistor Reordering
NASEER ET AL. (2007)	Different current models to compute Qcrit
KEANE ET AL. (2007)	Switched capacitor circuit for measure the Qcrit of storage cells
ARTOLA ET AL. (2014)	Variations in the supply voltage and the cell drive strength
ZIMPECK ET AL. (2019)	Decoupling Cells, Sleep Transistors and Transistor Reordering
THIS THESIS	Different transistor arrangements Transistor Reordering Transistor Sizing

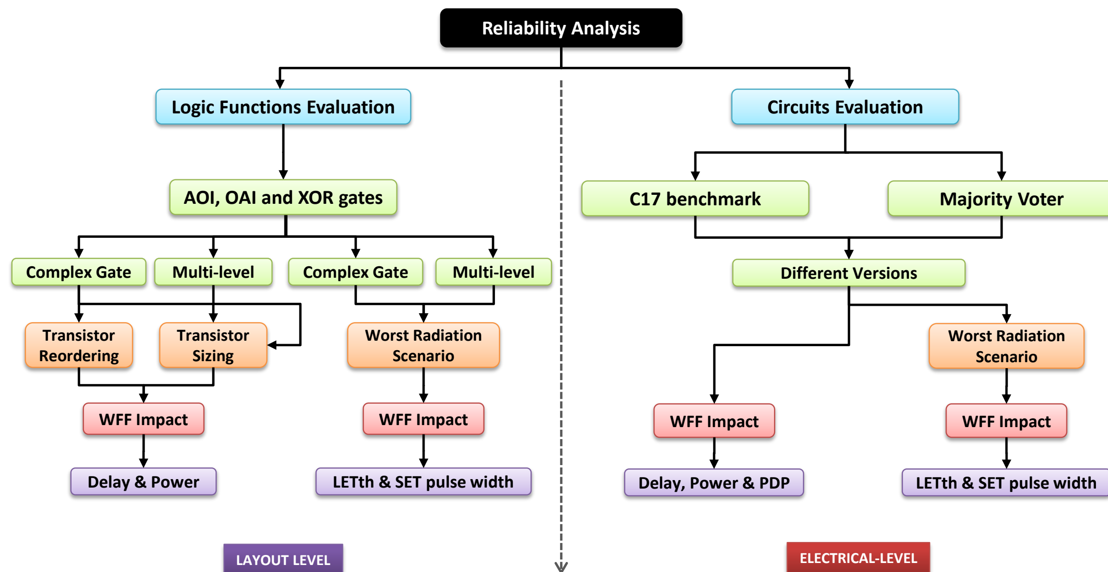
Source: From the author.

6 METHODOLOGY

This work explores different transistor arrangements for a set of logic functions and larger circuits to evaluate the SET and process variability effects. Different versions of the C17 benchmark and majority voter circuit were evaluated as a case study. The main goal is to verify how much gate mapping, through circuit-level techniques, influences the robustness to process variability and SET. The methodology adopted in all the experiments is organized to facilitate the reader's understanding of the results that will be presented in Chapter 7.

Firstly, a general methodology is presented in Sections 6.1 and 6.2, showing the differences between the two types of analysis used in this work: considering only the process variability effects and considering the process variability impact on the SET response. Figure 6.1 shows a schematic that summarizes the adopted organization. Sections 6.3 and 6.4 (in blue in the schema) present the specific methodology of the two types of applications evaluated in the work: 1) set of logic functions; and 2) C17 and majority voter circuits. Also, each type of application is performed at different abstraction levels (layout level and electrical-level).

Figure 6.1: Methodology flow for all experiments.



Source: From the author.

6.1 Process Variability Analysis

The process variability analysis can be divided into two stages: nominal behavior and process variability impact. In addition to comparing the results obtained in each stage, a general comparison of the results is also performed. The objective is to verify how much gate mapping influences the evaluated aspects of delay, power, Power-Delay Product (PDP) and mainly, the robustness to process variability. The experiments that evaluate only the process variability impact, not considering the radiation effects, follow these characteristics, and are presented in Subsections:

6.3.1 Evaluation of Transistor Reordering and Sizing

6.4.1 Process Variability impact on different transistor arrangements of C17 circuit

6.1.1 Nominal Behavior

The circuits are evaluated at nominal conditions, i.e., process variability is not considered. Nominal values are used as a form of reference values to evaluate the process variability effects. The objective is to analyze the typical characteristics of each different transistor arrangement used to implement the circuits. Propagation times, total power consumption and PDP of the different versions of the analyzed circuits are compared considering the worst-case and regardless of the output of the circuit for the C17 circuits.

6.1.2 Process Variability Impact

The analysis considering the process variability effects is performed keeping the same configurations of the previous step, however, considering the process variability impact through the WFF. Metal gate devices suffer from the WFF caused by the misalignment of metal grains in the gate. This fluctuation exhibits a multi-nominal distribution, which can be approximated by a Gaussian distribution if the number of grains on the surface of the metal gate is high enough (>10), which corresponds to the FinFET ASAP7 model characteristics. The WFF due to process variation is explored through the statistical Monte Carlo simulation process, considering a Gaussian distribution with a 3-sigma deviation of 5% the WFF, that characterizes an average and real impact of the variability effects on the devices (MEINHARDT; ZIMPECK; REIS, 2014). Two thousand simula-

tions were run for each circuit (ALIOTO; CONSOLI; PALUMBO, 2015). No correlation between different types of transistors was assumed, which means that PFET and NFET devices may come up with different variations in its parameters. Timing, total power consumption and PDP were taken for each delay arc and each Monte Carlo simulation, always aiming the worst-case. For all cases were computed mean (μ), standard deviation (σ) and normalized standard deviation (σ/μ) values. The σ/μ is used to define how much a circuit is sensitive to process variability. The lower are the values of this ratio, the more robust to variability are the circuits.

6.2 The Single Event Transient Response

The SET response analysis can be divided into three stages: worst radiation sensitive case, SET response at the ideal fabrication process and SET response under process variability. It is essential to highlight that this type of experiment also evaluates the process variability impact on the SET. That is, both reliability concerns are evaluated together. The experiments that follow these characteristics are presented in Subsections:

6.3.2 SET under WFF on FinFET Multi-level Design

6.4.2 WFF impact on the SET response of FinFET-based Majority Voters

The SET fault injection is modeled as the Messenger's equation shown in Equation 6.1 (MESSENGER, 1982) modified in the work of Srinivasan, Murley and Tang (1994), where Q_{coll} is the collected charge, τ_α ($1.64 \times 10^{-10}s$) is the collect charge timing constant, τ_β ($5 \times 10^{-11}s$) is the timing constant to establish the ion track and L ($21nm$) is the charge collection depth. The entire collected charged by the circuit is considered for analysis. The values used in this work are the typical values used for simulations and experiments in silicon presented in (CARRENO; CHOI; IYER, 1990), but modified to better characterize recent technologies, such as FinFET. This effect is reproduced on the SPICE simulation as a current source, simulating the SET effects on the transistors.

$$I(t) = \frac{Q_{coll}}{\tau_\alpha - \tau_\beta}(e^{-\frac{t}{\tau_\alpha}} - e^{-\frac{t}{\tau_\beta}}) \qquad (6.1)$$

$$Q_{coll} = 10.8 \times L \times LET$$

6.2.1 Worst Radiation Sensitive Case

The first step in the radiation sensitivity evaluation was to identify the most sensitive node and input vector at each circuit. The characteristics of this step were previously presented in (AGUIAR et al., 2017a) for majority voters evaluation. Two inverters were used for each input of the circuit and a single inverter for the output to emulate the worst fan-out scenario, i.e., lowest fan-out (FO1).

A fault injection campaign for a particle with LET estimated to 58 Mev.cm^2/mg was performed at each node of the circuits, as shown in Figure 6.5 and Figure 6.9, considering all possible input vectors. The definition of 58 Mev.cm^2/mg as the LET value used for the fault injection campaign was performed considering a higher LET that still characterizes a simulation at the atmospheric level (LET $\approx$ 60 Mev.cm^2/mg) (JAVANAINEN, 2012). Considering the amplitude and the width of the SET pulses that propagate to the circuit output allows determining which node and input vector are the most sensitive (FERLET-CAVROIS; MASSENGILL; GOUKER, 2013) and characterize the worst radiation sensitive case. After the worst radiation sensitive case was obtained, each circuit was fault injected considering this sensitive scenario, i.e., the most critical node, the sensitive input vector and the waveform of the pulse (strikes at P-type devices or N-type devices).

6.2.2 SET response at the ideal fabrication process

This step evaluates the circuit under radiation effects, but the effects of process variability are not considered. The LET$_{th}$ and the SET pulse width are used to characterize the SET response. Before starting the fault injection in the circuit, it is important to know the worst-case delay of each circuit, which will be used to determine the LET$_{th}$. Thus, the worst-case delay of each circuit was obtained.

In this work, it is considered the SET effects, more specifically, when a transient pulse propagates to the inverter chain output. The SET pulse may even be characterized at other points in the circuit, but the objective is to check whether this pulse is propagated to the circuit's output. To calculate the LET$_{th}$, two characteristics of the SET pulse were considered: amplitude and width. A fault in the circuit is considered when the SET pulse propagates to the circuit output with an amplitude that exceeds half of the nominal supply voltage ($V_{DD}/2$) and its width is greater than the circuit worst-case delay. These values are used as a form of reference values to evaluate the process variability effects.

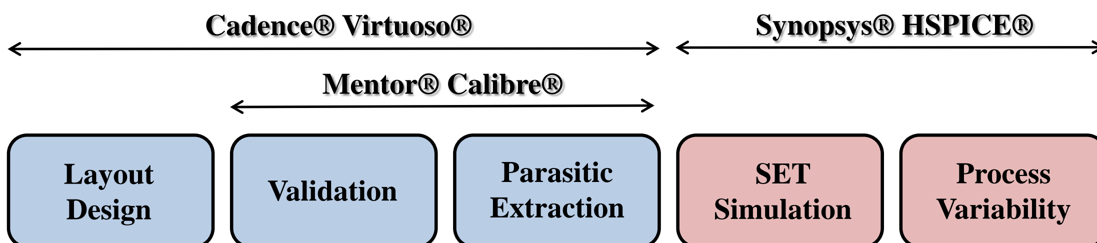
6.2.3 SET response under process variability

The analysis considering the process variability effects is performed keeping the same configurations of the previous step, but now considering the process variability impact through the WFF. The other aspects of the process variability analysis follows the same specifications presented in Subsection 6.1.2, differing only in relation to the evaluated parameters. Timing, SET pulse amplitude and width measurements were taken for each Monte Carlo simulation. The mean of these values is considered to calculate a new LET$_{th}$, i.e., a LET$_{th}$ that considers the process variability impact. Also, the standard deviation of the mean values is obtained and robustness analysis is performed using the normalized standard deviation of the SET pulse width.

6.3 Logic Functions Evaluation

The specific methodology used in each experiment that evaluates logic functions will be presented in the Subsections 6.3.1 and 6.3.2. Both experiments are carried out at the layout level. For each layout, the parasitic capacities are extracted, and a new netlist is generated. The delays of the internal connections are considered in these experiments. The design flow carried out at layout level experiments can be seen in Figure 6.2.

Figure 6.2: Design flow for layout level analysis.



Source: From the author.

All layouts were designed using the 7nm FinFET ASAP7 Process Design Kit (PDK), developed by Arizona State University in partnership with ARM (CLARK et al., 2016). Among the different models and corners available on this PDK, this work considers the regular threshold voltage (RVT) transistor model at a typical (TT) corner. Table 6.1 summarizes the key device parameters of 7nm FinFET ASAP technology. The nominal supply voltage is 0.7V, at a typical temperature of 25°C.

Table 6.1: Key parameters of 7nm FinFET ASAP technology.

Parameters		7nm
Supply Voltage		0.7V
Gate Length (L_G)		21nm
Fin Width (W_{FIN})		6.5nm
Fin Height (H_{FIN})		32nm
Oxide thickness (Tox)		2.1nm
Channel Doping		$1{\times}10^{22}m^{-3}$
Source/Drain Doping		$2{\times}10^{26}m^{-3}$
Work Function	**NFET**	4.3720eV
	PFET	4.8108eV

Source: Clark et al. (2016).

The layout of all logic cells adopts three fins as transistor sizing as recommended in the PDK to allow the internal routing of the cells (CLARK et al., 2016). The cell height is set to 7.5 tracks of metal 2 (M2) that correspond to 0.27μm for all evaluated cells. The PDK assumes EUV lithography for the key layers, a decision based on these presents near cost-effectiveness and resulting in more straightforward layout rules. Non-EUV layers assume appropriate multiple patterning schemes, i.e., self-aligned quadruple patterning (SAQP), self-aligned double patterning (SADP), or litho-etch litho-etch (LELE), based on 193nm optical immersion lithography (CLARK et al., 2016). The design rules, actual dimensions and underlying assumptions for some major layers are shown in Table 6.2.

Table 6.2: Key layer lithography assumptions, widths and pitches.

Layer	Lithography	Width/drawn (nm)	Pitch (nm)
Fin	SAQP	6.5/7	27
Active (horizontal)	EUV	54/16	108
Gate	SADP	21/20	54
SDT/LISD	EUV	25/24	54[b]
LIG	EUV	16/16	54
VIA0–VIA3	EUV	18/18	25[a]
M1–M3	EUV	18/18	36
M4 and M5	SADP	24/24	48
VIA4 and VIA5	LELE	24/24	34[a]

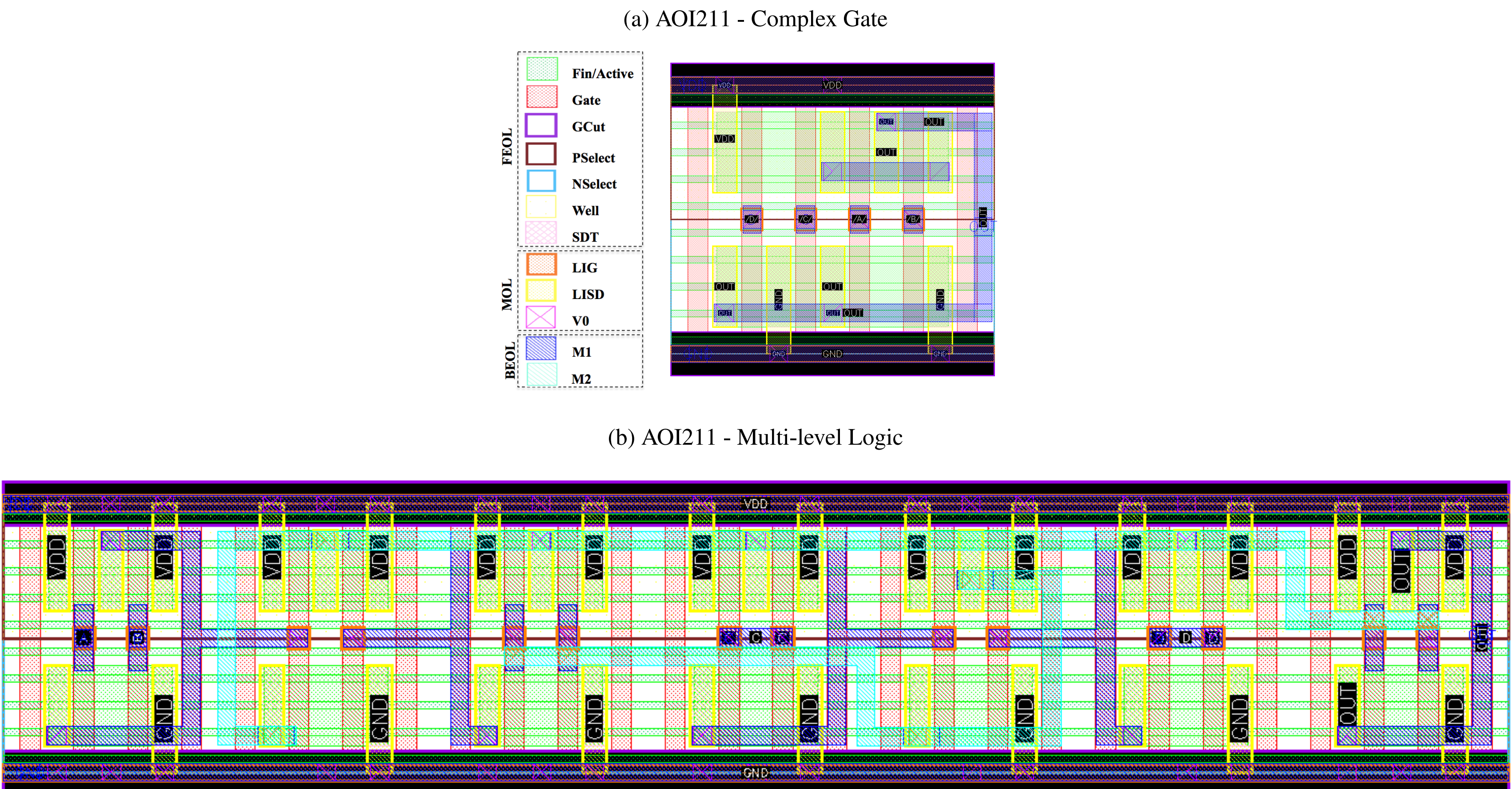
[a] Corner to corner spacing as drawn.
[b] Horizontal only.

Source: Adapted from Clark et al. (2016).

The specific design rule derivation is explained for key layers at the front end of line (FEOL), middle of line (MOL) and back end of line (BEOL) of the predictive process modeled. As an example, the layout of an AOI211 gate is presented in Figure 6.3a and Figure 6.3b in complex and multi-level logic topologies, respectively.

Figure 6.3: AOI211 layout in the two topologies: (a) complex gate and (b) multi-level of NAND2.

(a) AOI211 - Complex Gate



(b) AOI211 - Multi-level Logic

Source: From the author.

All layouts were validated by Design Rule Check (DRC) and Layout Versus Schematic (LVS) steps. The extracted netlist with parasite capacitances is obtained and it was used for the radiation sensitivity evaluation. From the extracted netlist, SPICE simulations were performed. The input switching frequency is set at 500MHz and inverters are connected to the input sources introducing realistic delays to the cells.

6.3.1 Evaluation of Transistor Reordering and Sizing

This study aims to provide bases for a better understanding of the results obtained in the following analyzes by justifying some characteristics used in all experiments. The focus is on the relation between the complex gate and the multi-level logic topologies. Two experiments are presented: transistor reordering and transistor sizing. This characterization is important because it makes the results more accurate and fair. The transistor reordering alternatives are explored on a reduced set of cells implemented only in the complex gate topology. That is, the topology that it is possible to reorder the devices' position about the output node. This experiment helps to define the suitable transistor arrangement for the complex gates functions evaluated in the next analyzes.

The relation between the process variability and the number of fins of a transistor is also evaluated. The evaluation of the process variability impact on individual transistors shows to be unrelated to the number of fins. However, the process variability effects should affect the general behavior of a circuit considering devices together on an arrangement. For the sake of compactness, the second experiment of this study shows the impact of designs with 2-4 fins in three logic cells: AOI22, OAI22 and XOR.

The influence of the transistor arrangement on complex gates layouts is considered before the logic gates design to allow the best case evaluation when compared with the multi-level gates versions. Also, the number of fins to be adopted in the design should affect the final observations. As the conditions of the experimental evaluation must be defined beforehand, the next subsections present the ideas behind the design choices of the next experiments. This experiment considers only the process variability effects and follows the methodology presented in Subsection 6.1.

6.3.1.1 Transistor Reordering

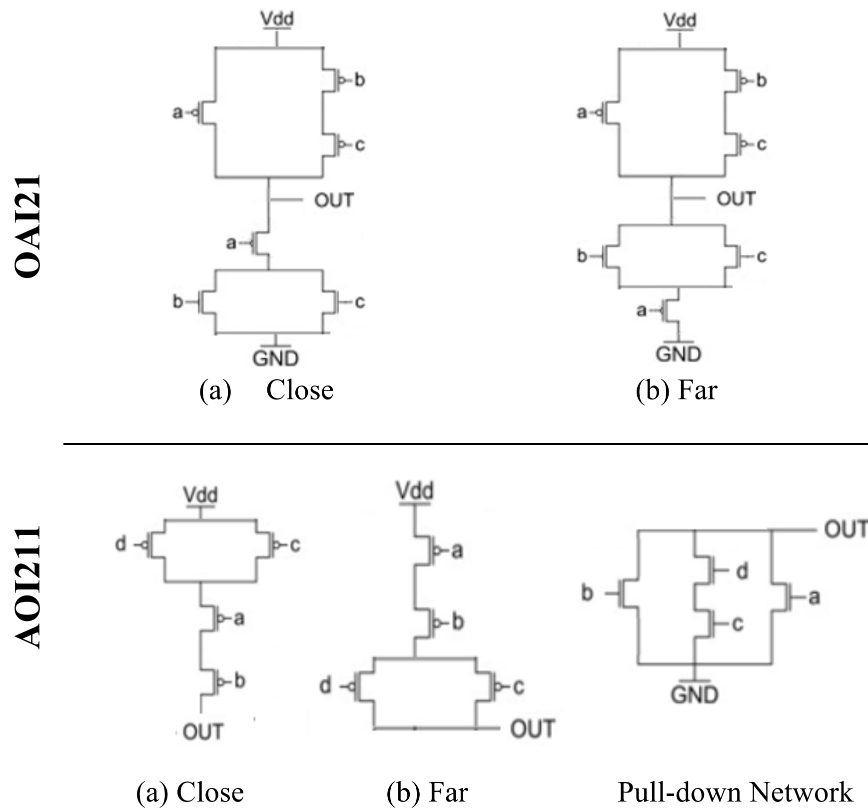
In this study, two different topologies are compared: complex and multi-level logic with basic gates. In order to obtain more precise results and to analyze in-depth the characteristics of each logic gate, the analysis of the different possible arrangements within the complex gate topology was carried out considering the nominal behavior and the real behavior with the process variability. Four logic functions, which it is possible to modify the transistor arrangement of the complex gate topology, were evaluated: AOI21, OAI21, AOI211 and OAI211.

The main idea is to modify the position of a serial transistor present in a pull-up or pull-down network of the gate. The transistor can be connected close or far related to the cell output terminal. As a general rule, AOI gates have the alternative transistor arrangements explored in the pull-up network. On the other hand, the OAI gates explored different pull-down network options. The complementary networks do not need to be rearranged because the transistors are associated in parallel. Figure 6.4 presents two examples of different transistor arrangements. For the OAI21 gate, in the pull-down network, the serial transistor with the signal *a* on the input can be connected close or far in relation to the cell output terminal. For the AOI211 gate it is the same logic, but considering the signals *a* and *b*.

6.3.1.2 Transistor Sizing

According to the 7nm FinFET PDK developer, with a 27 nm fin pitch, a high-density layout design is achieved with three fins for each PFET and NFET devices (CLARK et al., 2016; CHAVA et al., 2015). As a silicon-based channel and strain engineering are assumed for this PDK. The obtained NFET/PFET drive ratio is approximately 10:9 (CLARK et al., 2016). In this way, the cells are designed with symmetric sizing of NFET and PFET transistors. However, in order to investigate the exact number of fins (*nfin*) in parallel most appropriate for the analyzes performed in this work, a comparison was made between three different *nfin*, starting from the recommended design: 2 fins, 3 fins and 4 fins.

Figure 6.4: Example of close and far transistor arrangements: OAI21 and AOI211 gates.



(a) Close (b) Far Pull-down Network

Source: From the author.

6.3.2 SET under WFF on FinFET Multi-level Design

This experiment explores different transistor arrangements for a set of four logic functions (OAI21, OAI22, AOI211 and XOR), at the layout level, to evaluate the SET response under the process variability. Two different topologies of transistor arrangement are investigated: 1) complex gate: optimized functions designed as a complex logic gate CMOS topology; and 2) the multi-level of NAND2 gates: the functions are converted using De Morgan's theorem into the only NAND2 transistor arrangements. Previous experiments also considered topologies using only NOR2 and a mix of NAND2-NOR2-INV. However, the only NAND2 topology proved to be better, and it was chosen for this study (BRENDLER et al., 2018). Table 6.3 and Table 6.4 present the logic functions and the equations for the complex gate version and the converted multi-level composed by the NAND2 version, respectively. Although they represent the same functions, the versions are intrinsically different, which is interesting, since the comparison of similar versions does not present many advantages about the variability (ZIMPECK et al., 2018).

Table 6.3: Logic functions in the complex gate topology.

Logic Function	Complex Gate
OAI21	Y = (A+B . C)’
OAI22	Y = (A+B . C+D)’
AOI21	Y = (A.B + C + D)’
XOR	Y = A.B’ + A’.B

Source: From the author.

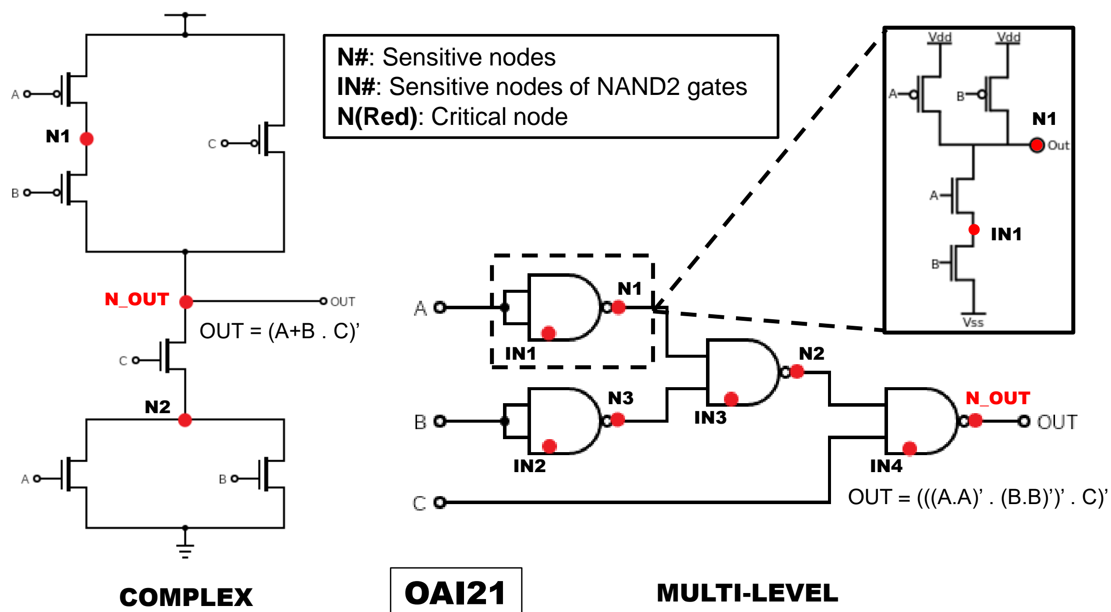
Table 6.4: Logic functions in the multi-level logic topology.

Logic Function	Multi-level version with NAND2 gates
OAI21	Y = (((A.A)’ . (B.B)’)’ . C)’
OAI22	Y = (((A.A)’ . (B.B)’)’ . ((C.C)’ . (D.D)’)’)’
AOI211	Y = (X . X)’ | X = (((A.B)’.(((C.C)’.(D.D)’)’.((C.C)’.(D.D)’)’)’
XOR	Y = ((A . (B.B)’)’ . ((A.A)’ . B)’)’

Source: From the author.

Figure 6.5 presents the schematics of the OAI21 gate in its two versions highlighting all the sensitive nodes that were considered in the worst radiation sensitive case evaluation, which will be described in section 7.1.2. This experiment considers SET and process variability effects together and follows the methodology presented in Subsection 6.2.

Figure 6.5: OAI21 schematic in complex and multi-level transistor arrangements.



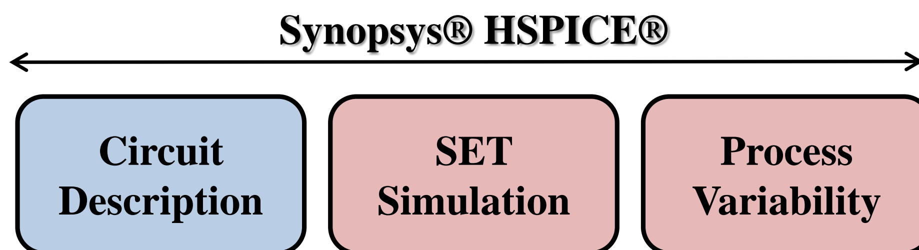
Source: From the author.

6.4 Circuits Evaluation

Regarding the circuits evaluation, two experiments are also performed. The specific methodology of each experiment will be presented in the Subsections 6.4.1 and 6.4.2. Different from the logic functions evaluation, these experiments are carried out at the electric level. Electrical simulations were performed using Synopsys HSPICE® also at the 7nm FinFET ASAP technology. The same PDK configurations of layout level experiments are used. The main difference is the design of the evaluated circuits. At the electric level, the circuits are described directly in Synopsys HSPICE®. This means that some characteristics present in the circuit design are not considered, as the delays of the internal connections. The choice for the analyzes of the circuits at the electrical level is justified by the size of the evaluated circuits and consequently, the complexity of the layouts. Still, it is known that the results obtained at the layout and electrical level present very close results, not interfering in the analyzes.

The transistor sizing also considers all transistors with three fins for all circuits. The nominal supply voltage of the model adopted is 0.7V, at a typical temperature of 25°C. The input switching frequency is set at 500MHz and inverters are connected to the input sources introducing realistic delays to the circuits. All circuits drive a Fanout 4 output capacitance. The design flow carried out in electrical-level experiments can be seen in Figure 6.6.

Figure 6.6: Design flow for electrical-level analysis.



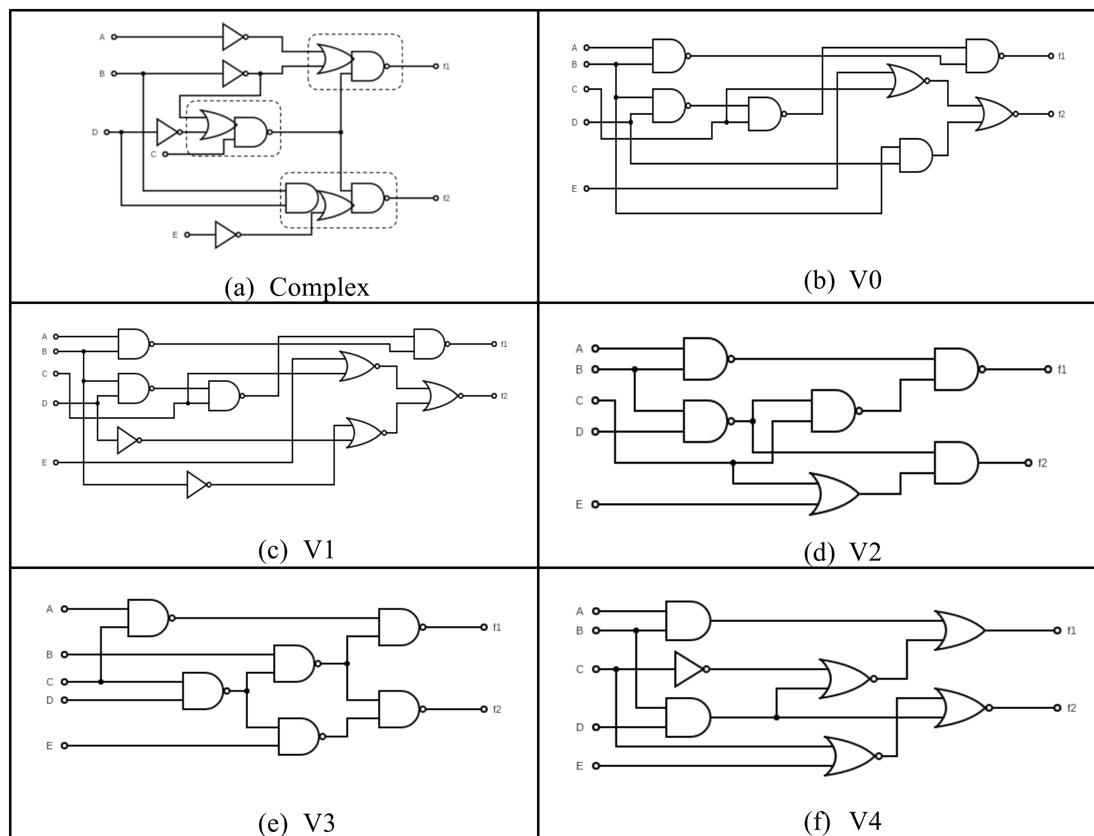
Source: From the author.

6.4.1 Process Variability impact on different transistor arrangements of C17 circuit

This experiment evaluates the impact of process variability on different versions of the C17 circuit, a benchmark that was first presented in ISCAS85 (BRGLEZ, 1985).

The circuit has five inputs and two outputs; its original version is composed of a set of two-input NAND gates. Figure 6.7 presents the six versions of the C17 circuit analyzed in this work. The original version of the C17 circuit is called V3. Five other versions of the C17 were derived from the original version. It is important to note that in addition to the different logic gates used in all versions, the complex version has a different feature. This feature is important because it allows the comparison between the use of complex and basic gates to implement a given circuit, in addition to the comparison between the different basic logic gates used in each version.

Figure 6.7: C17 circuit in (a) Complex version, and alternative versions: (b) V0, (c) V1, (d) V2, (e) V3, (f) V4.



Source: Brendler et al. (2019b).

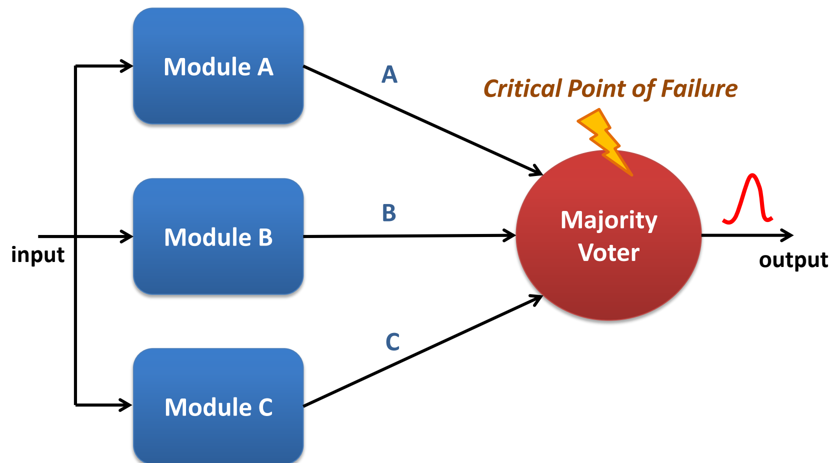
The experiment considers only the process variability effects and follows the methodology presented in Subsection 6.1. The objective is to verify how much gate mapping influences the evaluated aspects of delay, power, PDP and mainly, the robustness to process variability. Further, the number of transistors of each version of the C17 circuit is presented as an area estimate.

6.4.2 WFF impact on the SET response of FinFET-based Majority Voters

Several techniques are explored to increase the robustness of a given circuit or application. Hardware redundancy is the most adopted fault-tolerant technique. TMR technique is one of the most popular hardware redundancy techniques and it is widely explored in a variety of implementation strategies (KASTENSMIDT; CARRO; REIS, 2006; AGUIAR et al., 2017a). The concept of TMR relies on three identical circuit copies processing data and a MJV unit voting the triplicated outputs to mask single faults in one of the copies (KASTENSMIDT; CARRO; REIS, 2006). Equation 6.2 represents the logic function that translates the MJV circuit in a TMR scheme, where A, B and C constitute the signal data provided by the triplicated modules. Therefore, the voter circuit represents the critical point of failure for the TMR scheme, i.e., a soft error in the voter leads to a fault in the output (AGUIAR et al., 2017a), as it can be seen in Figure 6.8.

$$MJV_{output} = A.B + B.C + A.C \tag{6.2}$$

Figure 6.8: TMR scheme – the MJV circuit constitutes the critical point of failure.



Source: From the author.

From the Boolean function described in Equation 6.2, the majority voting function can be implemented in a plurality of circuit topologies that use different transistor arrangements. Figure 6.9 shows the seven different majority voter circuits analyzed in this work against process variability and radiation effects:

1) Classic (CLS) (CAZEAUX; ROSSI; METRA, 2004);

2) NAND-based (NAND);

3) NOR-based (NOR);

4) Kshirsagar e Patrikar (KSH) (KSHIRSAGAR; PATRIKAR, 2009);

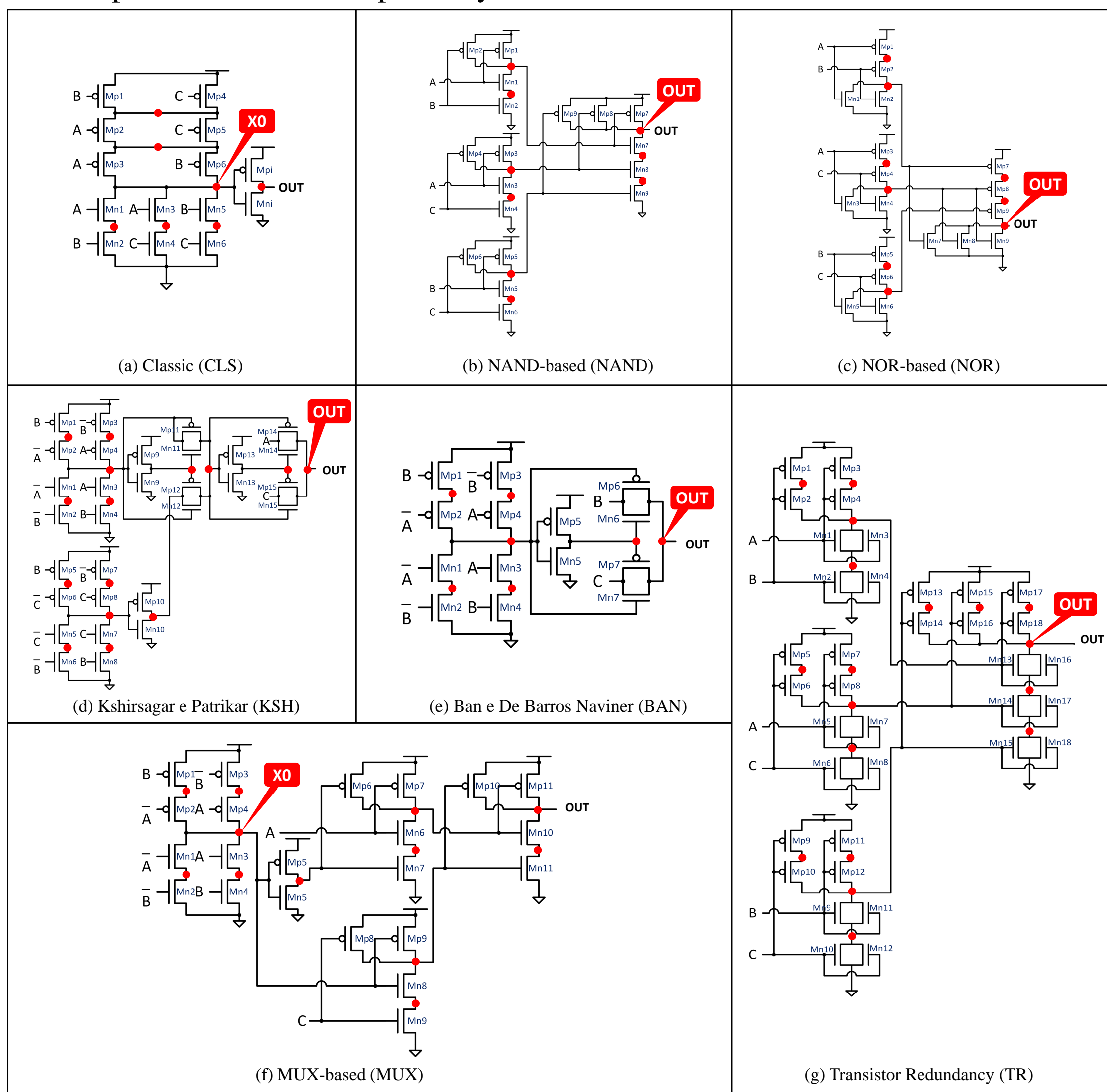
5) Ban e De Barros Naviner (BAN) (BAN; NAVINER, 2010);

6) MUX-based (MUX) (DANILOV; GORBUNOV; ANTONOV, 2014);

7) Transistor Redundancy (TR) (EL-RAZOUK; ABID, 2006).

In Figure 6.9, the sensitive nodes of each voter are highlighted with red points and the most sensitive node with red labels. For the best identification in the presentation of the results, each voter will be represented by the acronym in parentheses.

Figure 6.9: MJV versions: (a) CLS, (b) NAND, (c) NOR, (d) KSH, (e) BAN, (f) MUX and (g) TR. The sensitive nodes and the most sensitive node of each voter are highlighted with red points and labels, respectively.



(a) Classic (CLS)

(b) NAND-based (NAND)

(c) NOR-based (NOR)

(d) Kshirsagar e Patrikar (KSH)

(e) Ban e De Barros Naviner (BAN)

(f) MUX-based (MUX)

(g) Transistor Redundancy (TR)

Source: Brendler et al. (2020).

The impact of process variability through the WFF on the SET response of seven different versions of majority voter circuits is evaluated. This experiment considers SET and process variability effects together and follows the methodology presented in Subsection 6.2. A general comparison is also performed in addition to compare the results obtained in each stage. The objective is to verify how much gate mapping influences the robustness to process variability and SET, besides the WFF impact on the SET response.

7 EXPERIMENTAL RESULTS

As already detailed in the previous chapter, the results of the experiments carried out in this work will be presented in two sections. Section 7.1 presents the experiments that consider the logic functions evaluation and Section 7.2 shows the circuits-based experiments.

7.1 Logic Functions Evaluation

It is important to remember that the evaluation of logic functions is performed through two experiments. *Evaluation of Transistor Reordering and Sizing* assesses the process variability impact using the transistor reordering technique and varying the transistor sizing. *SET under WFF on FinFET Multi-level Design* demonstrates the impact of process variability on the SET effects using different logic gates in two topologies.

7.1.1 Evaluation of Transistor Reordering and Sizing

7.1.1.1 Transistor Reordering

Without considering the impact of process variability, Table 7.1 presents the worst-case delay and the total power consumption in the different arrangements used in the four logic functions in which it was possible to modify the position of the transistors. None of the arrangements (close and far) can be considered optimal since the logic functions do not present their best results for only one arrangement. Considering only the delay, the

Table 7.1: Worst-case delay and power consumption for close and far arrangements at nominal conditions.

Logic Function	**Metrics**	**Arrangement**	
		Close	**Far**
AOI21	Delay (ps)	14.98	15.29
	Power (μW)	0.142	0.150
OAI21	Delay (ps)	14.53	14.47
	Power (μW)	0.139	0.148
AOI211	Delay (ps)	24.68	24.36
	Power (μW)	0.155	0.161
OAI211	Delay (ps)	16.67	17.61
	Power (μW)	0.147	0.157

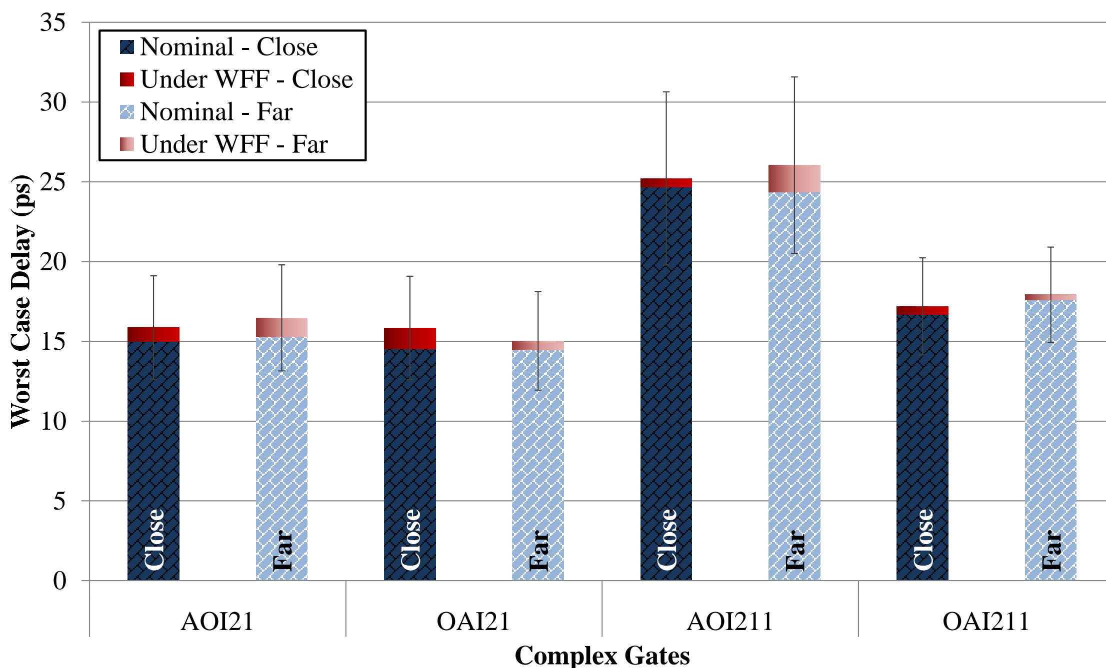
Source: Adapted from Brendler et al. (2019c).

close arrangement presents the shortest delay times for the AOI21 and OAI211, 14.98ps and 16.66ps, respectively. Already for the OAI21 and AOI211 gates, the far arrangement is the best option, with delay times equal to 14.47ps and 24.35ps, respectively. Regarding the total power consumption, the observed behavior for the delay is maintained for the AOI21 and OAI211 gates, but for the OAI21 and AOI211 gates, the close arrangement becomes the best option.

Figure 7.1 and Figure 7.2 show the difference between nominal values and the mean of the results obtained by Monte Carlo simulations considering the worst-case of the propagation delay and the power consumption, respectively. The red bars indicate the increase caused in the electrical characteristics due to process variability. The worst-case delay suffers up to 9% of deviation while the power consumption is less than 1% deviation from the nominal values.

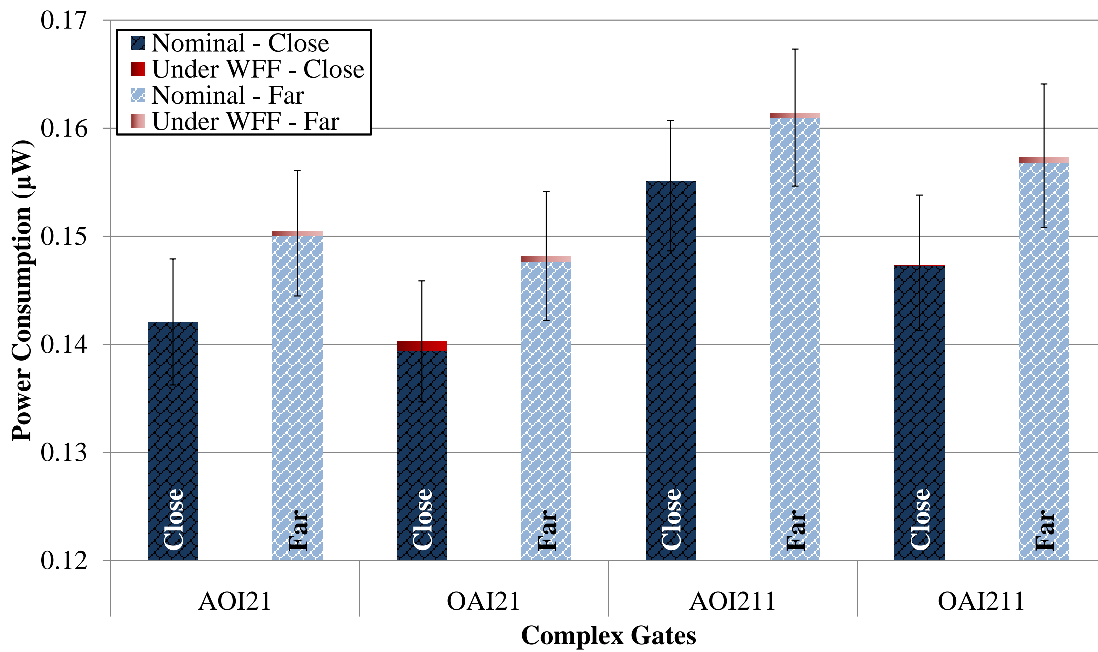
Considering the worst-case delay, it is not possible to highlight one of the transistor arrangements due to the not statistically significant difference between their values. However, regarding the total power consumption, the close arrangement is the best option. For all the evaluated functions, the close arrangement presents a power consumption, on average, 7% lower.

Figure 7.1: Difference between the worst-case delay considering nominal values and under WFF.



Source: Adapted from Brendler et al. (2019c).

Figure 7.2: Difference between power consumption considering nominal values and under WFF.

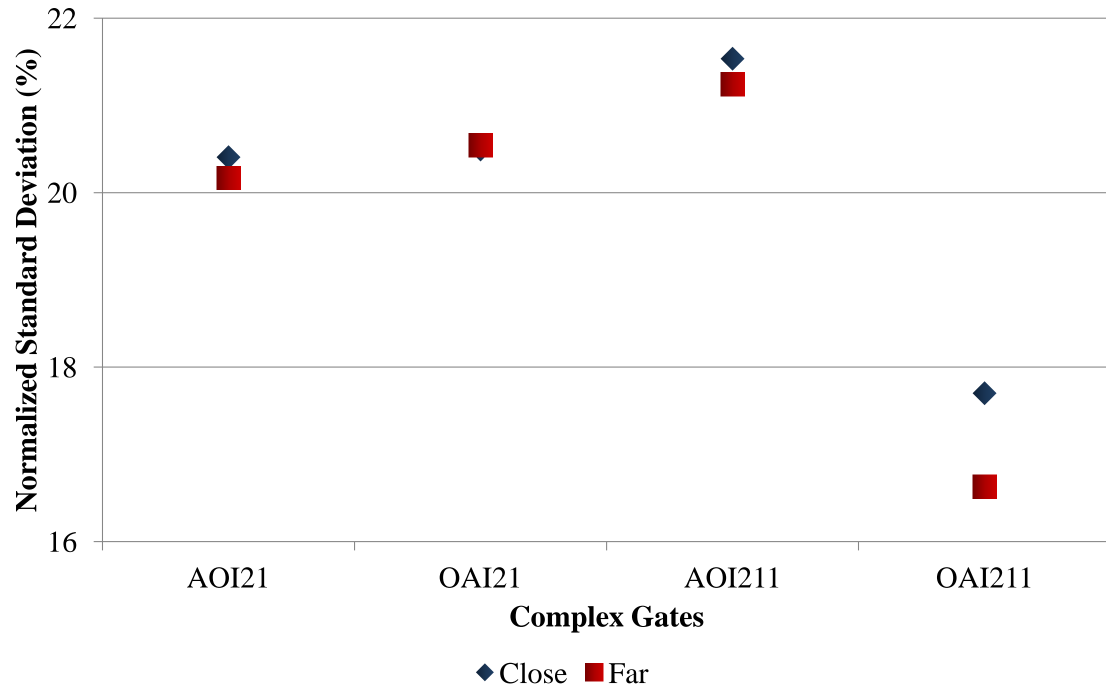


Source: Adapted from Brendler et al. (2019c).

The normalized standard deviation considering the worst-case delay and the total power consumption are shown in Figure 7.3 and Figure 7.4. The delay deviation varies around 20%, whereas considering the total power consumption, the deviation varies around 4%. It is important to note that the values between close and far arrangements, considering both the nominal behavior and the process variability are very close.

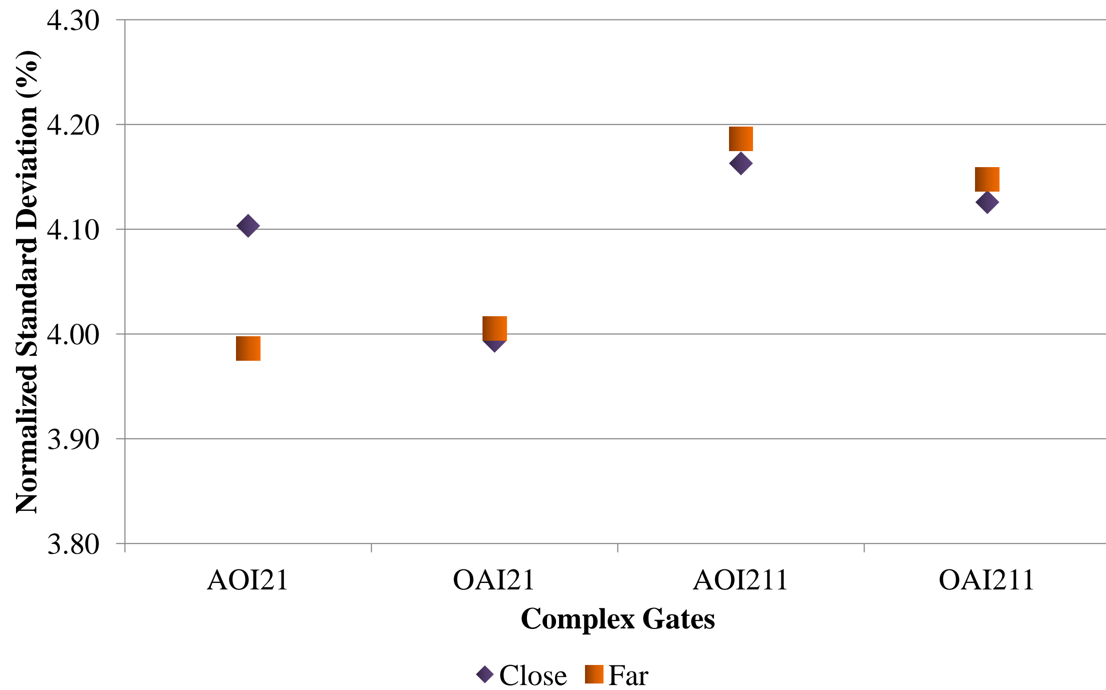
In addition to the impossibility of highlighting a particular arrangement to be used in all logic functions, another factor that minimizes the importance of choosing a specific complex gate arrangement is the proximity of the results of both the worst-case delay and the total power consumption. The delay results of close and far arrangements, not considering process variability, range from 1.5% to 5.3%. For power consumption, this variation is around 6%, in the analysis of the four logic functions. Considering the process variability, the values vary around 6% for the delay and between 3% and 6% for the power consumption. Thus, the logic functions in the complex gate topology analyzed in this work will be designed with far and close arrangements according to the best behavior.

Figure 7.3: Delay Normalized Standard Deviation considering WFF.



Source: Brendler et al. (2019c).

Figure 7.4: Total power Normalized Standard Deviation considering WFF.



Source: Brendler et al. (2019c).

7.1.1.2 Transistor Sizing

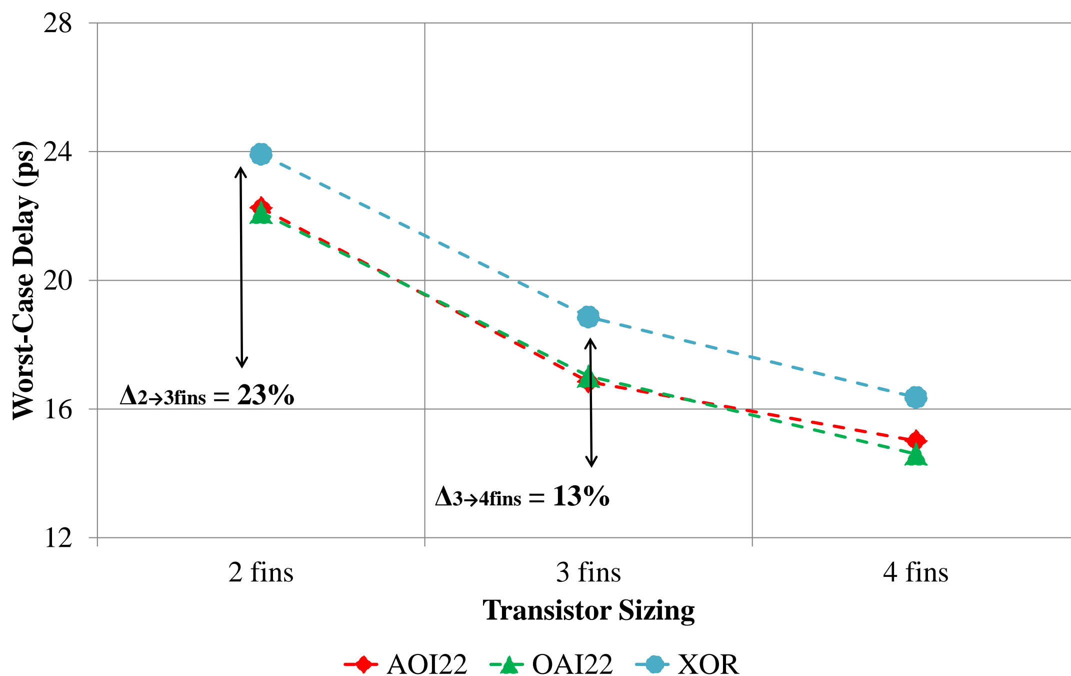
Table 7.2 presents the worst-case delay and the total power consumption, considering the nominal behavior, of the three logic functions analyzed in their different topologies considering three different numbers of fins. In this first moment, the comparison between the complex and multi-level gate topologies is not taken into account, what is important is to verify the influence of the transistor sizing in the analyzed metrics. According to the increase in the number of fins, the delay tends to decrease and the power consumption tends to increase, independently of the logic function and topology adopted. This behavior can be better observed in Figure 7.5 and Figure 7.6.

Table 7.2: Worst-case delay and total power consumption considering different transistor sizing

Logic Function	Metrics	2 fins		3 fins		4 fins	
		Complex	Multi-level	Complex	Multi-level	Complex	Multi-level
AOI22	Delay (ps)	22.25	29.39	16.85	25.66	15.01	23.82
	Power (μW)	0.143	0.236	0.156	0.285	0.169	0.328
OAI22	Delay (ps)	22.11	27.27	17.02	23.52	14.60	22.33
	Power (μW)	0.143	0.236	0.155	0.288	0.168	0.333
XOR	Delay (ps)	23.92	29.50	18.86	24.99	16.36	24.06
	Power (μW)	0.205	0.276	0.227	0.323	0.241	0.367

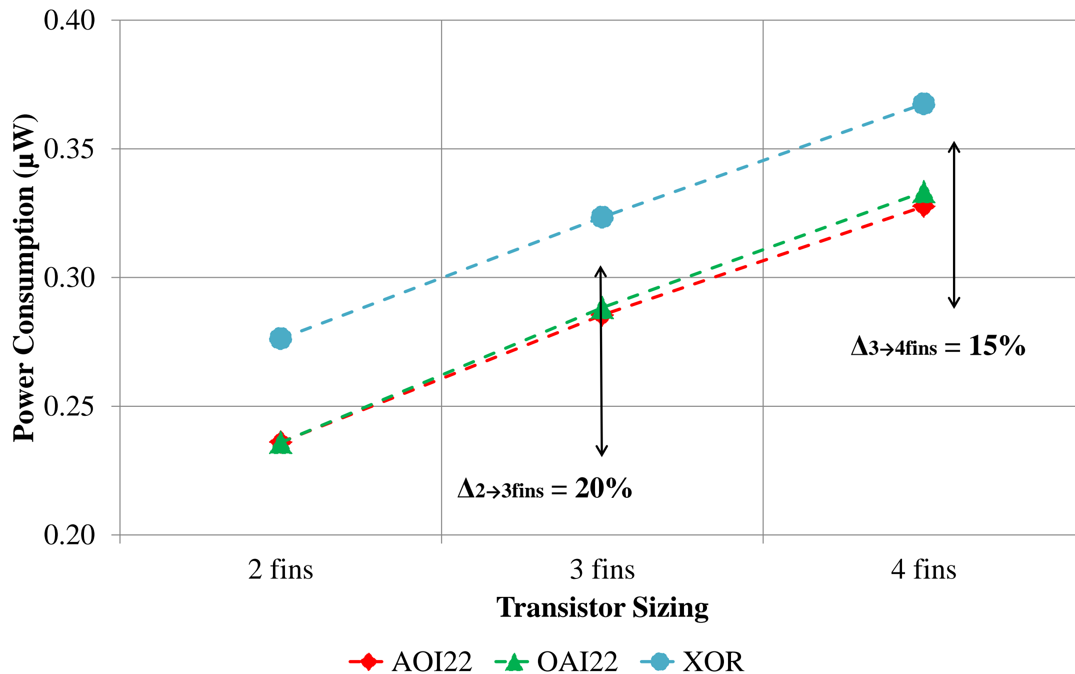
Source: Adapted from Brendler et al. (2019c).

Figure 7.5: Worst-case delay for complex gate topology considering transistor sizing.



Source: Adapted from Brendler et al. (2019c).

Figure 7.6: Total power consumption for multi-level topology considering transistor sizing.



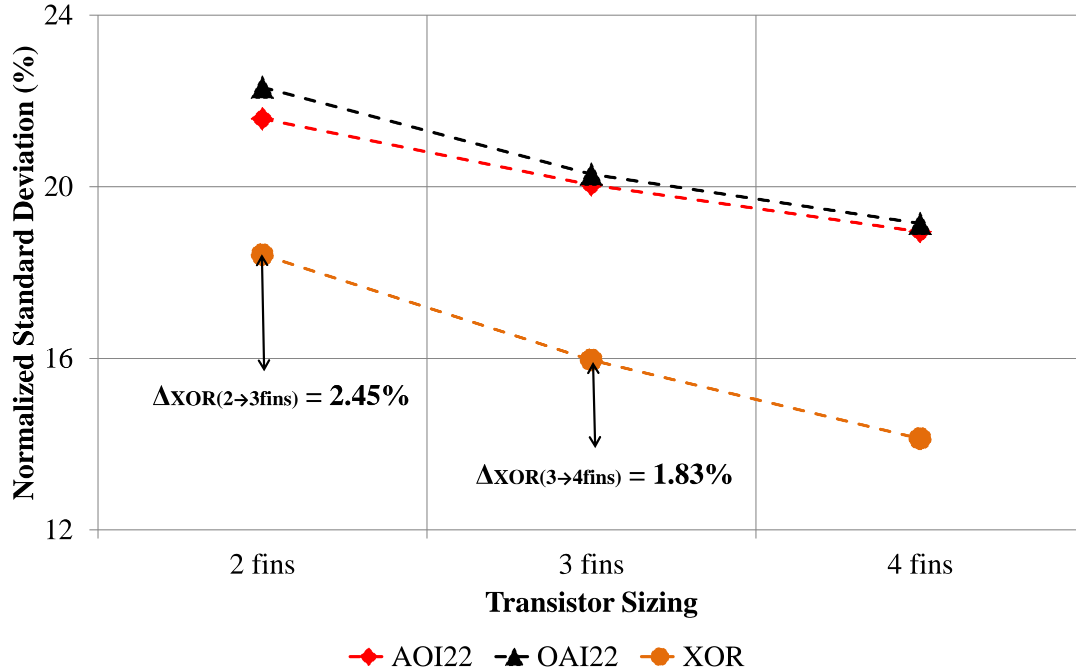
Source: Adapted from Brendler et al. (2019c).

As the complex gate and multi-level gates topology are not yet being compared, Figure 7.5 shows the delay variation according to the increase of the number of fins considering only the complex gate topology. In the graph, it is clear the impact of increasing the number of transistor fins in reducing the delay. Represented in the figure by the Δ (for 2 to 3 fins and 3 to 4 fins), the delay decreases on average by 23% comparing 2 to 3 fins design and by 13% when increasing to 4 fins. Considering the multi-level topology, these reductions are less significant: on average, 14% and 5% for the same number of fins.

Figure 7.6 shows the variation of the power consumption according to the increase in the number of fins, this time considering only the multi-level gates topology. Unlike the delay, power consumption tends to increase with the increase in the number of fins and presents a more linear behavior. In the increase of 2 to 3 fins, the power consumption increases by an average of 20%, while in the increase from 3 to 4 fins, the growth is around 15%. Considering the complex gate topology, the increases are less significant: on average, 9% and 7% for the same increase in the number of fins.

The impact of process variability is also analyzed with transistor sizing. Figure 7.7 and Figure 7.8 show the normalized standard deviation of the three logic functions analyzed using 2, 3 and 4 fins in parallel, considering the worst-case delay and the total power

Figure 7.7: Delay Normalized Standard Deviation for complex gate topology considering transistor sizing.

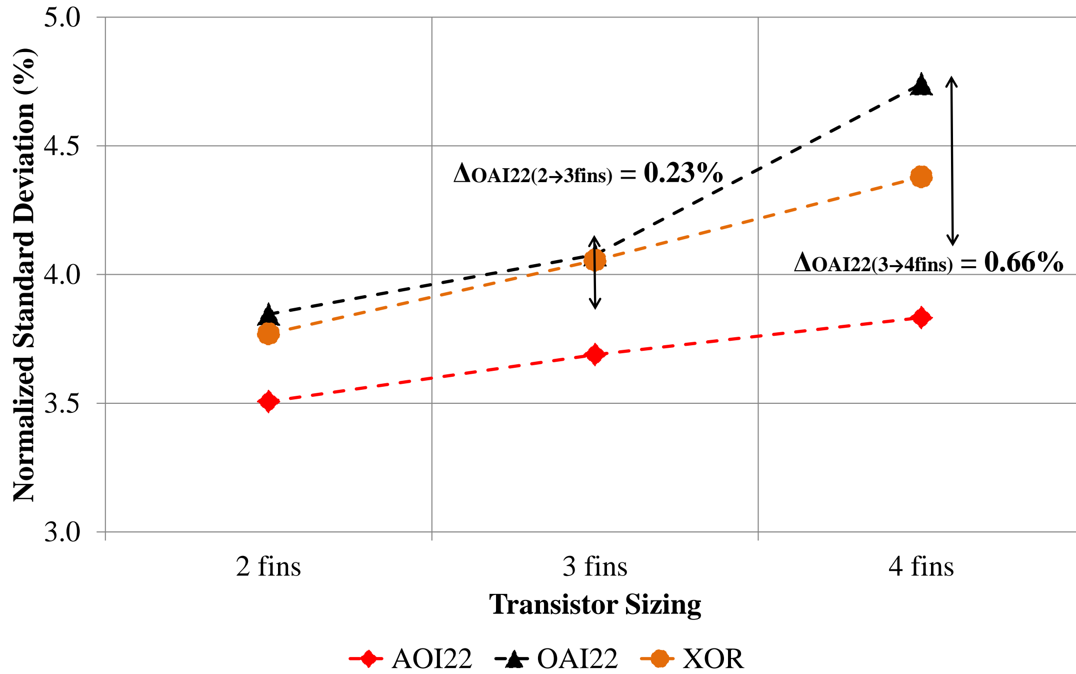


Source: Adapted from Brendler et al. (2019c).

consumption, respectively. In Figure 7.7, the logic functions were analyzed when using a complex gate topology, while in Figure 7.8 the analysis is performed with the functions implemented with a multi-level logic topology. For these analyzes, that consider the process variability impact, the Δ values refer to changes in sensitivity only for the gates with the most significant variations considering delay and power, XOR and OAI22, respectively.

The deviations of the delay times tend to decrease with the increase in the number of fins, but the deviations of the power consumption tend to increase. This behavior is the same seen in the previous analyzes, but now considering the sensitivity of the logic gates to the process variability effects in the delay and power metrics. Still, as in the analyzes under ideal conditions, the reduction of the normalized standard deviation of the delay is more significant in the transition from 2 to 3 fins (Δ_{XOR} = 2.45%) than from 3 to 4 fins (Δ_{XOR} = 1.83%). Only in power analysis, specifically for the OAI22 gate, this behavior changes. The increase in the transition from 3 to 4 fins (Δ_{OAI22} = 0.66%) is greater than the increase in the transition from 2 to 3 fins (Δ_{OAI22} = 0.23%). With the rise in the number of fins, a logic gate becomes more robust to the process variability effects considering the delay times. On the other hand, the same logic gate becomes more

Figure 7.8: Total power Normalized Standard Deviation for multi-level topology considering transistor sizing.



Source: Adapted from Brendler et al. (2019c).

sensitive to process variability, considering power consumption.

The increase in the number of fins provides advantages and disadvantages. From the obtained results, it can be realized that the reductions of delay times and deviations are more significant until *nfin*=3. After this, still obtaining better results, they are closer and closer to the previous ones, as shown by the Δ values. Taking into account the reason presented, the increase in power consumption and the area penalty according to the increase in the number of fins and the recommendation of the PDK developer, this work adopts *nfin*=3 for all the designed layouts.

7.1.2 SET under WFF on FinFET Multi-level Design

The worst radiation sensitive case was obtained before characterizing the SET response. The critical node, the most sensitive input vector and the transient pulses, which compose the worst radiation case for each logic function in both topologies, are presented in Table 7.3.

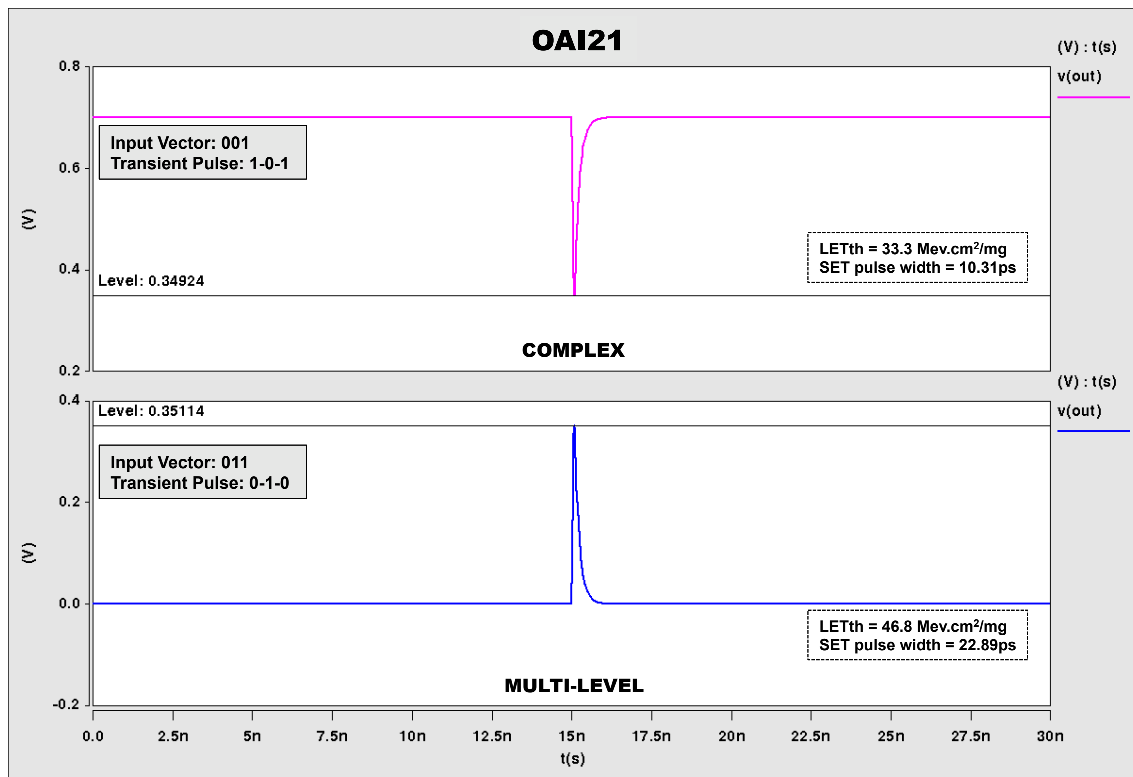
Table 7.3: Worst Radiation Sensitive Case.

Logic Function	Worst Radiation Sensitive Case	Complex Gate	Multi-level
OAI21	Critical Node	OUT	OUT
	Input Vector	001	011
	Transient Pulse	1-0-1	0-1-0
OAI22	Critical Node	OUT	OUT
	Input Vector	1001	0101
	Transient Pulse	0-1-0	0-1-0
AOI211	Critical Node	OUT	OUT
	Input Vector	0000	0101
	Transient Pulse	1-0-1	0-1-0
XOR	Critical Node	OUT	OUT
	Input Vector	11	11
	Transient Pulse	0-1-0	0-1-0

Source: Adapted from Brendler et al. (2019a).

To characterize the fault at a given node of the circuit, it is evaluated whether the SET pulse propagates to the circuit output. Thus, the probability of the critical node being the output itself is very high and this behavior is proven in the obtained results for both topologies. It can be seen that the most sensitive input vectors vary, even considering the same logic function, due to the use of a different transistor arrangement. For OAI21 and AOI211 gates, this difference between the input vectors is reflected in the format of the transient pulse (SET 101 or SET 010) that will be inserted in the node. Figure 7.9 demonstrates this behavior in more detail for the OAI21 gate, highlighting the inserted pulses considering the worst-case scenario. It is important to note that the shape of these pulses changes concerning the different input vectors of each circuit. In Figure 7.9, only the critical pulses for each topology of the OAI21 gate are presented and will be used in the next analyzes.

Figure 7.9: The difference of transient pulse format inserted in the critical node (OUT) of complex and multi-level topologies of OAI21 gate.



Source: Brendler et al. (2019a).

7.1.2.1 SET evaluation under the ideal fabrication process

The worst-case propagation delays of the four logic functions in the two topologies are shown in Table 7.4. In addition to presenting some differences between the use of complex and multi-level topologies, these propagation times are necessary to calculate the LET_{th}.

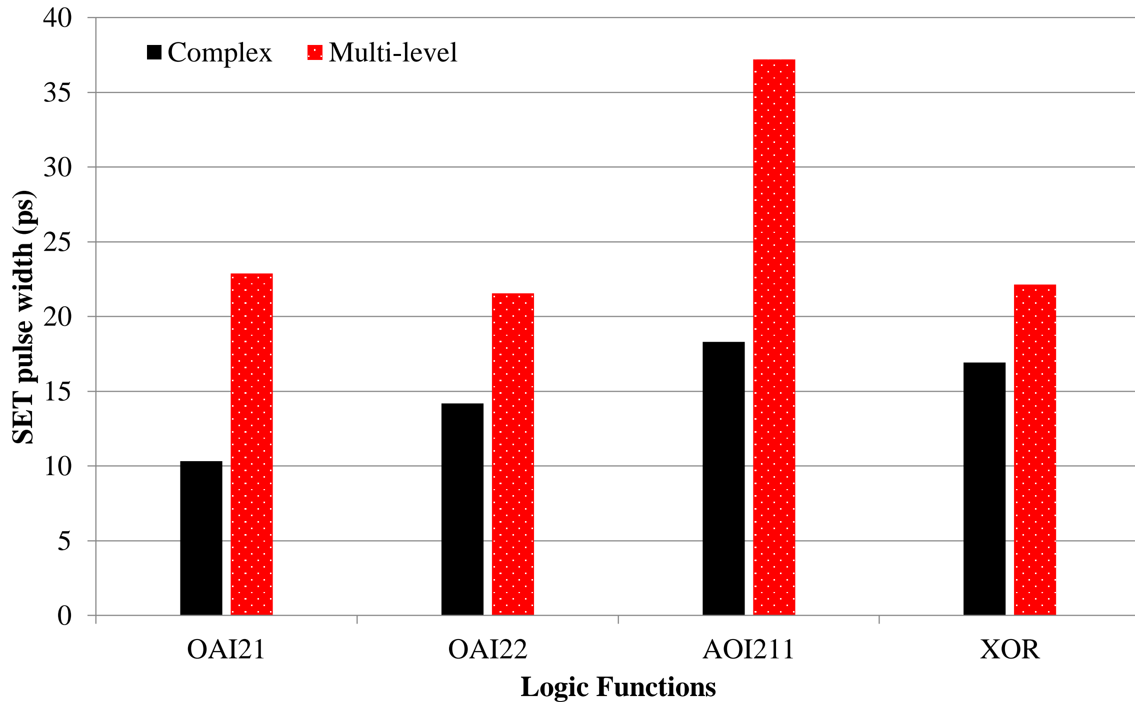
Table 7.4: Worst-case propagation delay at nominal conditions.

Logic Function	**Worst-case delay (ps)**	
	Complex Gate	Multi-level
OAI21	7.79	18.29
OAI22	9.63	18.48
AOI211	13.42	36.63
XOR	11.68	20.02

Source: Adapted from Brendler et al. (2019a).

Figure 7.10 shows the SET pulse width measured when the amplitude of this same pulse exceeds half of the nominal supply voltage in the circuit output. To calculate the LET_{th} of each logic gate, it is important to note that all values of the SET pulse width

Figure 7.10: SET pulse width at the ideal fabrication process.



Source: Brendler et al. (2019a).

shown in Figure 7.10 are greater than the worst-case delays shown in Table 7.4, characterizing the fault in the circuit output. The multi-level topology presents the SET pulse width of about 77% larger in comparison to the complex topology. This behavior does not necessarily mean a higher sensitivity of the multi-level topology to the radiation effects. The SET pulse width considering nominal conditions tends to be higher for the multi-level topology since the functions implemented in this arrangement of transistors are slower than the ones implemented in the complex topology. That is, if the SET pulse width is less than the logic gate delay, the fault would be masked.

The larger SET pulse width of the multi-level topology is not reflected in the LET_{th} calculation, as can be seen in Table 7.5. For the OAI21 and AOI211, the LET_{th} considering the multi-level topology is 40.54% and 72% higher than the LET_{th} of the complex topology, respectively. XOR gate and the OAI22 gate present a similar LET_{th}, with approximately 1% difference. The results demonstrate that multi-level topology is more robust to the radiation effects considering the ideal fabrication process since it presents higher LET_{th} values in comparison with complex topology. This behavior is related to the regularity of the layouts developed. The OAI22 and XOR gates, even in the complex topology, are already quite regular. Therefore, the use of multi-level topology for these functions has practically no impact.

Table 7.5: LET_{th} at ideal conditions.

Logic Function	LET_{th} (Mev.cm^2/mg)	
	Complex Gate	Multi-level
OAI21	33.3	46.8
OAI22	47.4	46.8
AOI211	27.5	47.3
XOR	46.8	46.9

Source: Adapted from Brendler et al. (2019a).

7.1.2.2 The SET response under WFF

As the analysis carried out considering only the radiation effects, in the process variability analysis, the worst-case propagation delay of each logic gate is also measured but considering the impact of the WFF. Table 7.6 shows the mean (μ), standard deviation (σ) and normalized standard deviation (σ/μ) of the delays for all analyzed logic gates.

Table 7.6: Worst-case propagation delay under WFF.

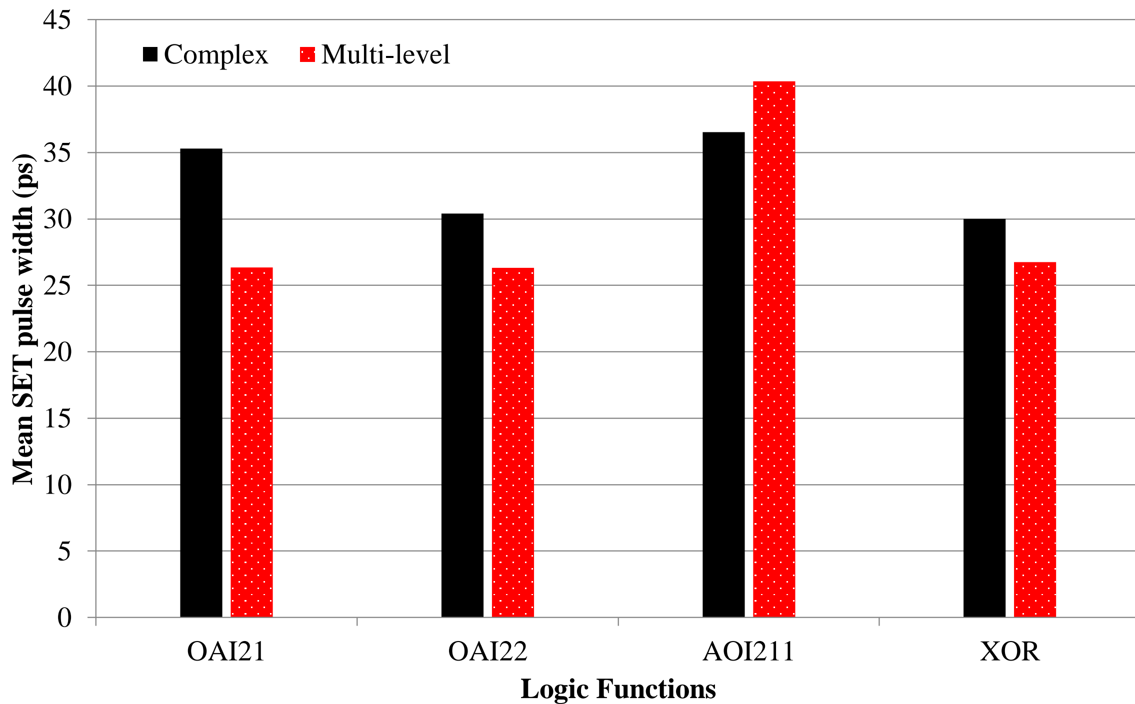
Logic Gates	Worst-case delay (ps)					
	Complex Gate			Multi-level		
	μ	σ	σ/μ (%)	μ	σ	σ/μ (%)
OAI21	8.43	2.56	30.37	19.21	4.00	20.83
OAI22	11.18	3.43	30.71	19.42	4.08	21.02
AOI211	14.71	4.64	31.56	38.52	7.62	19.78
XOR	12.49	2.84	22.73	20.95	4.39	20.98

Source: Adapted from Brendler et al. (2019a).

Figure 7.11 shows the mean of the SET pulse width for each logic function implemented in the two topologies. Unlike analysis under nominal conditions, on average, the SET pulse width for complex topology is higher, ranging from 4ps to 9ps of difference in comparison with the multi-level topology. Only for the AOI211 gate that this ratio is not established and the SET pulse width for the multi-level topology is still about 4ps higher. Considering only the SET pulse width, the complex topology is more sensitive to the effects of process variability.

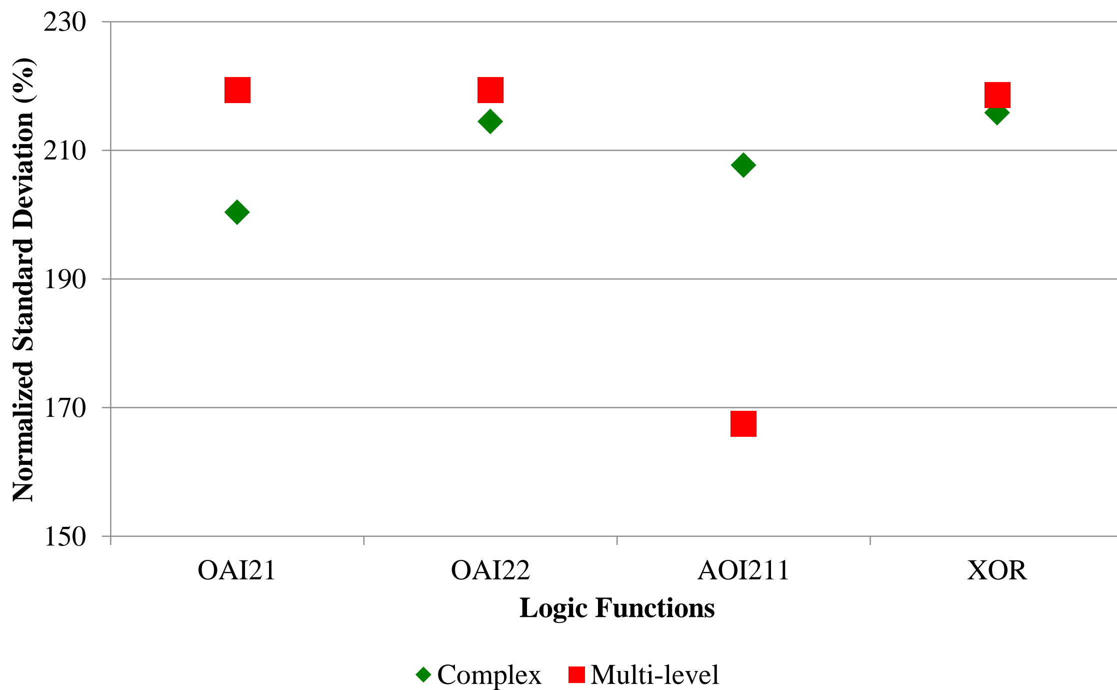
The normalized standard deviation of the SET pulse width is shown in Figure 7.12. The smaller this deviation, the more robust to the process variability effects is the topology used in each logic function. Although the complex topology presents higher mean values of the SET pulse width, these values deviate less than the values considering the multi-level topology for three of the four logic functions analyzed. This difference between the deviations is not very significant, being 2.75% for the XOR gate and approximately 19% for the OAI21 gate. As in the previous analysis, for the AOI211 gate, the behavior

Figure 7.11: Impact of WFF on SET pulse width.



Source: Brendler et al. (2019a).

Figure 7.12: Normalized standard deviation of SET pulse width.



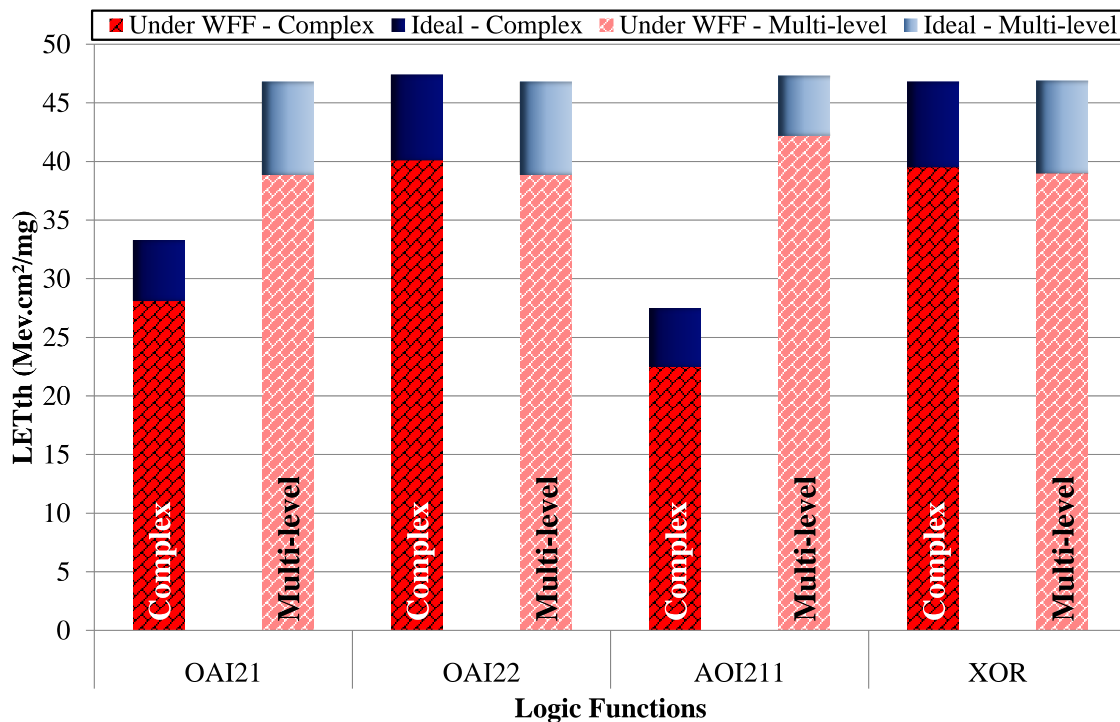
Source: Brendler et al. (2019a).

is inverse and the multi-level topology ends up having the smallest deviation. Although the complex topology suffers from increasing the SET pulse width due to the impact of the WFF, these values have a smaller deviation than the ones considering the multi-level

topology. That is, the multi-level topology has a slightly higher probability of having a SET pulse width value greater than the mean.

After obtaining the values of the SET pulse width and confirming that they are higher than the worst-case propagation delay of each logic gate, the characterization of the fault in the circuit output is complete and then a new LET_{th} can be calculated considering the impact of the WFF. Figure 7.13 shows the difference between the LET_{th} obtained considering the ideal fabrication process and the impact of the WFF for all the logic functions in the two topologies of the study. For all logic functions regardless of the adopted topology, the LET_{th} considering the impact of the WFF is smaller than the LET_{th} at nominal conditions. That is, due to WFF, a smaller amount of energy transferred by the particle is required to cause a disturbance in the circuit. All circuits become more sensitive to the radiation effects. Also, in the comparison between the different transistor arrangements used in each logic gate, the multi-level topology presents the best results. For the OAI21 and AOI211 gates, the LET_{th} considering the impact of the WFF is significantly larger in comparison with the complex topology, being 38.4% and 88% respectively. For the OAI22 and XOR gates, the LET_{th} is smaller in the same comparison. However, signalizing a not statistically significant difference, 3.1% and 1.3%, respectively.

Figure 7.13: Difference of LET_{th} considering ideal fabrication process and WFF impact.



Source: Adapted from Brendler et al. (2019a).

7.1.2.3 Area Impact

It is important to highlight one more important metric when comparing the two topologies used in this study. Table 7.7 shows the number of transistors and the area of each logic gate in the two topologies. All gates designed with the multi-level logic arrangement show an increase in the used area. In most cases, the area using the multi-level topology is more than three times larger than the complex gate topology. The OAI22 and AOI211 gates have the largest variation; the multi-level layout is about 4.5 times larger than the traditional layout. The XOR gate has the smallest increase in the comparison between the two topologies, approximately 67%.

Table 7.7: Comparison of number of transistors and area for complex gate and multi-level logic topologies.

Logic	**# Transistors**		**Area (μm^2)**	
Function	**Complex Gate**	**Multi-level**	**Complex Gate**	**Multi-level**
OAI21	6	16	0.085	0.271
OAI22	8	28	0.102	0.475
AOI211	8	28	0.102	0.475
XOR	10	20	0.203	0.339

Source: From the author.

7.2 Circuits Evaluation

As the previous section, two experiments are also evaluated considering larger circuits. *Process Variability impact on different transistor arrangements of C17 circuit* studies the robustness of different versions of the C17 circuit to process variability. *WFF impact on the SET response of FinFET-based Majority Voters* assesses the process variability effects along with soft errors on different majority voters.

7.2.1 Process Variability impact on different transistor arrangements of C17 circuit

Table 7.8 shows the total number of devices, the worst-case delay times, the total power consumption and PDP in all versions of the C17 circuit, considering the nominal behavior. Considering only the delay, multi-level versions V0-V4 show advantages when compared with the complex version. The complex version has the greatest delay being, on average, 70% greater than basic gates versions. V0 and V1 versions have the shortest delay between all analyzed circuits, 20.19ps and 20.54ps, respectively. Observing the schematic shown in Figure 6.7, it is concluded that this difference between the V0 and V1 versions is due to the optimization carried out from the V1 version to obtain the V0 version, in which the two inverters followed by the NOR logic gate are replaced by only one AND gate.

Table 7.8: Number of devices, worst-case delay, power consumption and PDP at nominal conditions.

C17	Metrics			
Version	**# Dev.**	**Delay (ps)**	**Power (μW)**	**PDP (aJ)**
Complex	28	31.58	0.319	10.07
V0	30	20.19	0.316	6.38
V1	32	20.54	0.327	6.72
V2	28	21.35	0.345	7.37
V3	24	25.30	0.320	8.10
V4	32	26.60	0.370	9.84

Source: Adapted from Brendler et al. (2019b).

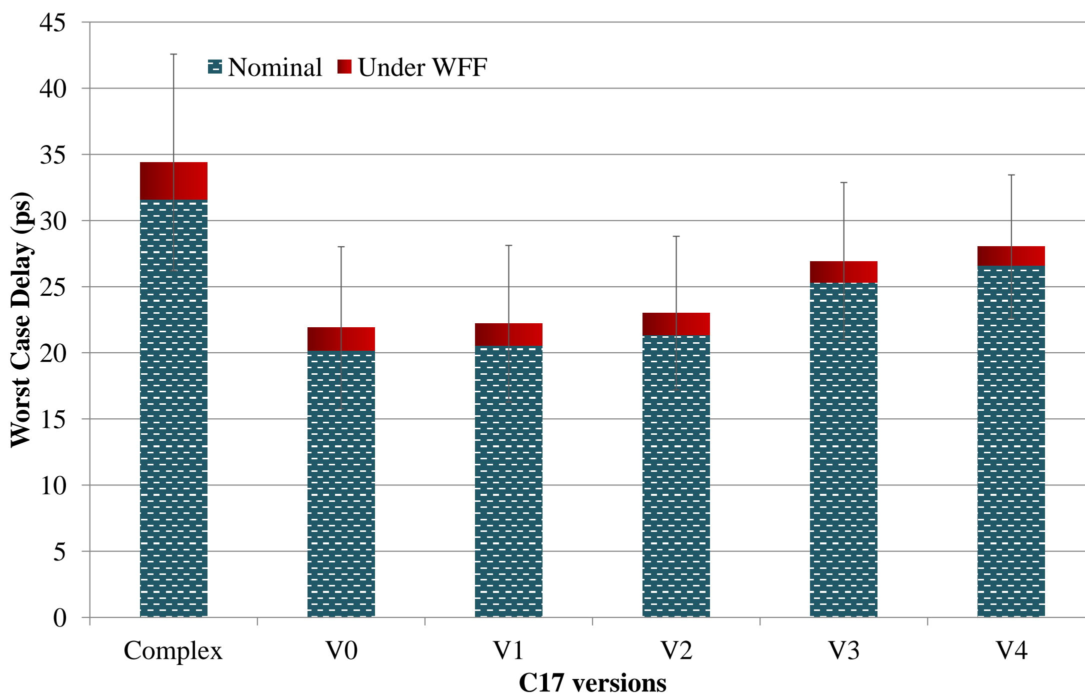
However, the difference between the power consumption of each version is lower, reaching a maximum of 15%. The best result is presented by the V0 version, with a total power consumption of 0.316μW. The V4 version is the one with the highest power consumption, 0.370μW, and the complex version has the second-lowest power consumption among the six circuits analyzed. As it is known, the number of transistors in each circuit

has total influence on the power consumed by it, observing the results obtained, it can be seen that this relation exists, but it is not predominant. Once the V0 version presented the best results for the delay and power analyzes, this behavior also reflects on the PDP. The maximum PDP difference between V0 and the other versions is around 27%.

7.2.1.1 Process Variability Impact

Figure 7.14 and Figure 7.15 show the difference between nominal values and the mean of the results obtained by Monte Carlo simulations considering the worst-case delay and the power consumption, respectively. The red bars indicate the increase caused in the electrical characteristics due to process variability.

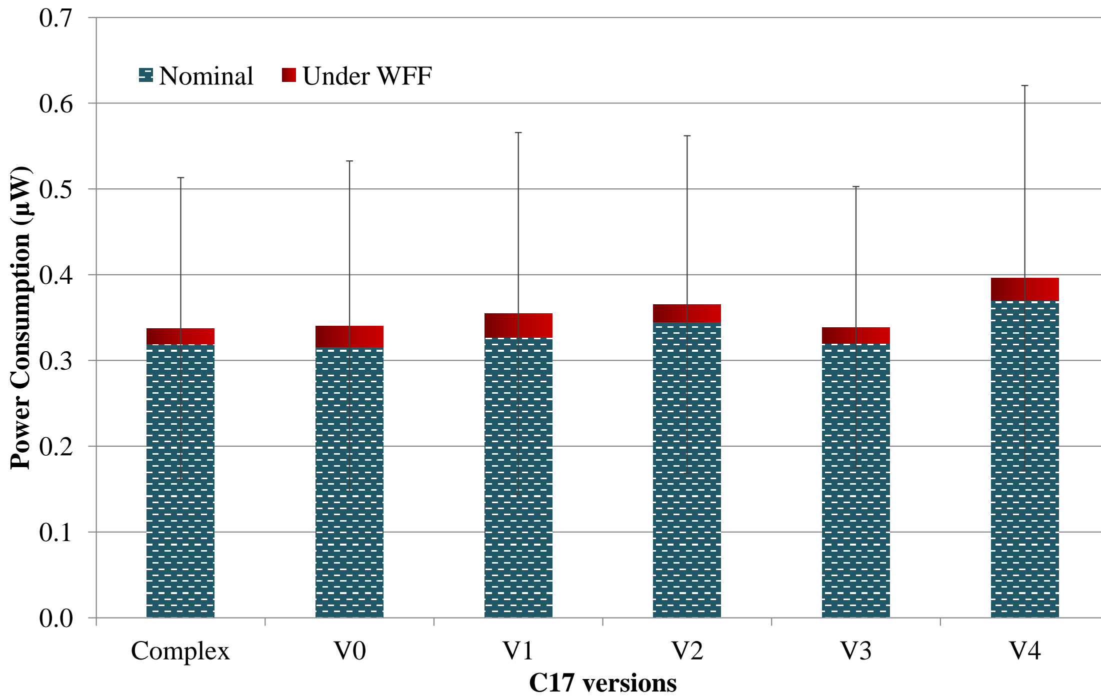
Figure 7.14: Difference between the worst-case delay considering nominal values and under WFF.



Source: Brendler et al. (2019b).

The worst-case delay suffers around 5-8% deviation from the nominal values, with the complex version being the most affected, with a deviation of 8.18%. The V0 version, which presents the best results considering the nominal behavior, is the second most impacted by the process variability with a deviation of 7.8%. In this analysis, the V4 version presents the smallest deviation among all analyzed circuits, 5.1%. Regarding the power consumption, the deviations also vary around 5-8% but are different in the analysis of each circuit. The complex version, which presented the greatest deviation of the delay, has the smallest deviation considering power consumption, 5.37%. The largest deviation

Figure 7.15: Difference between power consumption considering nominal values and under WFF.



Source: Brendler et al. (2019b).

from the nominal values is 7.92% of the V1 version.

Table 7.9 presents the exact mean values (μ) of the delay and power considering the WFF mentioned above as well as a summary of PDP results. Also, the standard deviation (σ), the normalized standard deviation (σ/μ) and the comparison of all versions with basic gates about the complex version (Δ) are presented. This Δ represents the percentage of increase or decrease of the normalized standard deviation of the basic gates versions relative to the complex version (Reference). The positive values represent the increase of this deviation, that is, the advantage of using the complex version, and consequently, the negative values represent the advantage of using the basic gates versions.

Before comparing basic and complex versions, it is important to note the general behavior of all C17 circuit versions. Figure 7.16 shows the normalized standard deviation of the delay times, the total power consumption and the PDP of all analyzed circuits. The greater is the deviation; the greater is the sensitivity to the process variability effects. The V3 and V4 versions, which did not show good results in the nominal behavior analysis, were the ones with the lowest PDP (54.1%) and delay (19.3%) deviations, respectively.

V0 and V1 versions are highly impacted by process variability. The V0 version has a deviation of approximately 28% of the delay and the V1 version has a deviation of 59.49% of the power consumed. Both are the biggest deviations in the comparison

Table 7.9: Mean, standard deviation, normalized standard deviation and delta of worst-case delay, power consumption and PDP.

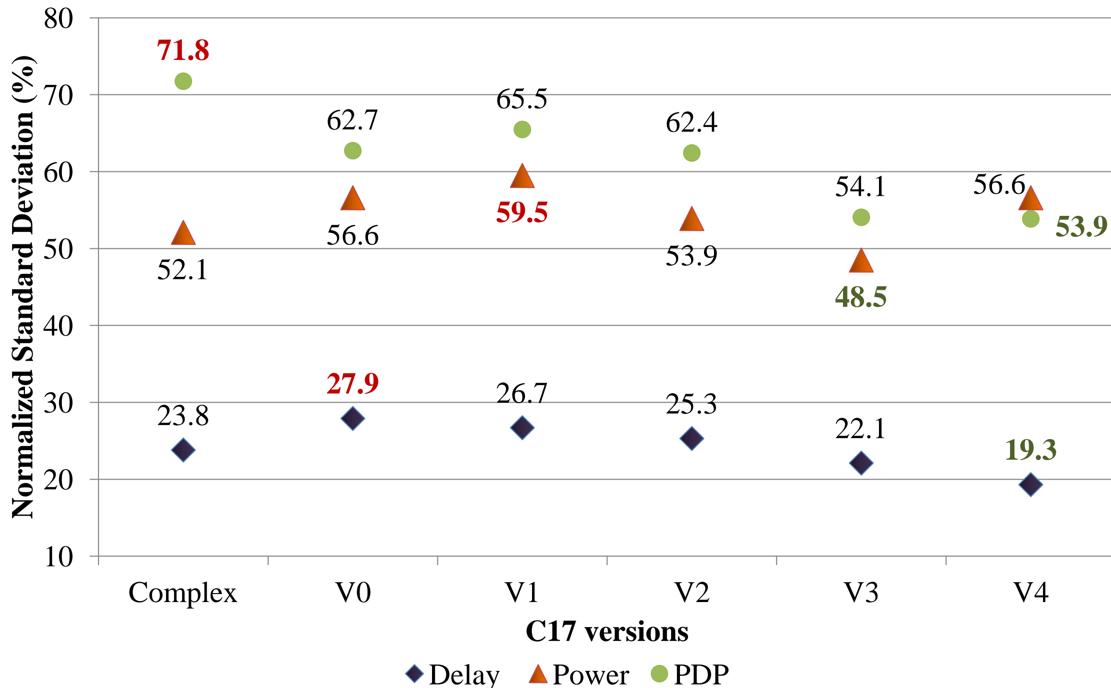
Metrics		Complex	V0	V1	V2	V3	V4
Delay	μ (ps)	34.39	21.90	22.20	23.00	26.92	28.03
	σ (ps)	8.19	6.12	5.92	5.81	5.95	5.42
	σ/μ (%)	23.80	27.95	26.67	25.26	22.10	19.34
	Δ (%)	Reference	**17.42**	**12.04**	**6.14**	**-7.15**	**-18.76**
Power	μ (μW)	0.337	0.340	0.355	0.365	0.339	0.396
	σ (μW)	0.176	0.193	0.211	0.197	0.164	0.224
	σ/μ (%)	52.16	56.60	59.49	53.87	48.47	56.59
	Δ (%)	Reference	**8.51**	**14.05**	**3.28**	**-7.08**	**8.49**
PDP	μ (aJ)	11.21	8.19	8.53	8.65	9.20	11.33
	σ (aJ)	8.05	5.14	5.58	5.40	4.97	6.10
	σ/μ (%)	71.75	62.72	65.48	62.42	54.06	53.86
	Δ (%)	Reference	-12.59	-8.74	-13.00	-24.66	-24.93

Source: Adapted from Brendler et al. (2019b).

between all the circuits. This behavior can also be seen in the PDP, where the V0 and V1 versions presented the greater values of process variability sensitivity among the multi-level versions explored.

The complex version has good behavior about process variability, it does not have the smallest deviations, but in comparison with the other five versions, it is a very interesting option. However, when the PDP is observed, the complex version is the least robust

Figure 7.16: Normalized Standard Deviation of Delay, Power and PDP considering WFF.



Source: Brendler et al. (2019b).

to process variability. To better observe this behavior, it was used the Δ previously mentioned in Table 7.9. Regarding the delay, the complex version has the deviation from the nominal values, smaller than the first three basic gates versions, second only to the V3 and V4 versions. When considering power consumption, only the V3 version has a smaller deviation than the complex version. That is, among ten comparisons (highlighted in bold in the table) performed between the deviations of each version of the C17 circuit regarding power and delay, the complex version has an advantage in seven of them. Regarding the PDP, the adoption of the complex version can be around 24% less advantageous if compared with V3 and V4 versions.

7.2.2 WFF impact on the SET response of FinFET-based Majority Voters

The worst radiation sensitive case is the first step before the SET response characterization. The critical node, the most sensitive input vector and the transient pulse format, which compose the worst-case scenario for each MJV circuit, are presented in Table 7.10.

Table 7.10: MJVs Worst Radiation Sensitive Case.

Worst-case Scenario	CLS	NAND	NOR	KSH	BAN	MUX	TR
Critical Node	X0	OUT	OUT	OUT	OUT	X0	OUT
Input Vector	100	000	111	011	101	011	011
Transient Pulse	1-0-1	0-1-0	1-0-1	1-0-1	1-0-1	1-0-1	1-0-1

Source: Adapted from Brendler et al. (2020).

To characterize the fault at a given node of the circuit, it is evaluated whether the SET pulse propagates to the circuit output. Thus, the probability of the critical node being the output itself is very high and this behavior is confirmed in the obtained results. Only for CLS and MUX voters, the critical node is another internal node (X0). Still, this node is the output before the last inverter in the CLS voter and the output of the MUX, responsible for selecting the output signal in the MUX voter. Due to the use of different transistor arrangements, the most sensitive input vectors vary for each voter. However, this variation does not occur about the shape of the transient pulse. For six of the seven analyzed voters, the most sensitive transient pulse is the SET 101.

7.2.2.1 SET response at the ideal fabrication process

Table 7.11 shows the total number of transistors and the worst-case propagation delay of all MJV circuits evaluated, considering the ideal fabrication process. In addition to presenting some differences in performance and area between the different MJV versions, the propagation times are necessary to obtain the LET_{th} values.

Table 7.11: Number of transistors and Worst-case delay under Ideal Fabrication Process.

MJV	**Metrics**	
Circuits	**#Transistors**	**Worst-case delay (ps)**
CLS	14	22.25
NAND	18	19.35
NOR	18	25.27
KSH	30	32.80
BAN	14	23.03
MUX	22	28.39
TR	36	28.90

Source: Adapted from Brendler et al. (2020).

The number of transistors used by each MJV version allows estimating the area used by each design. It is important to note that the transistor count does not consider the inverter transistors of the complemented inputs of KSH, BAN, and MUX voters. CLS, BAN, NAND and NOR voters, which have 14 to 18 transistors, have a significant advantage over TR and KSH voters, with 36 and 30 devices, respectively. The delays vary by up to 69.5% when comparing all versions. The NAND voter has the shortest delay (19.35 ps), while the KSH voter is the slowest version with 32.8 ps of delay.

The LET_{th} and the SET pulse width are presented in Table 7.12. The SET pulse width is measured when the amplitude of this pulse exceeds half of the nominal supply voltage in the circuit output. To characterize the fault and calculate the LET_{th} of each voter, it is important to note that all SET pulse width values are greater than the worst-case delay values shown in Table 7.11. The SET pulse width values follow much the same behavior as the delay values. The KSH voter has the greatest SET pulse width (34.46 ps) and the BAN voter has the shortest (25.72 ps). However, the difference between these values for all the MJVs is smaller, reaching a maximum of 34%. The SET pulse width considering the ideal fabrication process tends to be higher for slower voters.

LET_{th} values may seem high considering MJV circuits. However, similar work highlights the robustness of the 7nm FinFET technology, considering other logic functions (ZIMPECK et al., 2019; BRENDLER et al., 2019a) and also MJVs (AGUIAR et al., 2017b). For instance, NAND and NOR voters have no-fault event (at nominal supply

Table 7.12: LET_{th} and SET pulse width under ideal fabrication process.

MJV Circuits	LET_{th} (Mev.cm^2/mg)	SET pulse width (ps)
CLS	28.7	25.77
NAND	35.5	28.52
NOR	24.1	28.08
KSH	36.7	34.46
BAN	36.4	25.72
MUX	34.5	32.20
TR	35.5	34.26

Source: Adapted from Brendler et al. (2020).

voltage) considering a LET value of 15 Mev.cm^2/mg (AGUIAR et al., 2017b).

Also, in Table 7.12, it is possible to conclude that at least considering the ideal fabrication, the SET pulse width values are unrelated to the LET_{th} values. The KSH and BAN are the most robust voters to radiation effects since they have the highest LET_{th} values of all MJV versions. The NOR voter has the lowest LET_{th} value of all voters and it is the most sensitive voter to the radiation effects. This behavior is related to the use of Pass Transistor Logic (PTL) near the output of the circuits. While KSH and BAN voters use the PTL in the last stage before the output of the circuit, the NOR voter, in addition to not using PTL, has a NOR3 gate in the previous step before the output. That is, the NOR voter has three PFET transistors in series directly connected to the power supply, increasing the impact of the current source inserted in this node.

7.2.2.2 SET response under WFF

In the analysis considering the process variability, the worst-case propagation delay of each MJV circuit is also measured, but now considering the WFF impact. Table 7.13 shows the mean (μ), standard deviation (σ) and normalized standard deviation (σ/μ) of the delays for all analyzed voters.

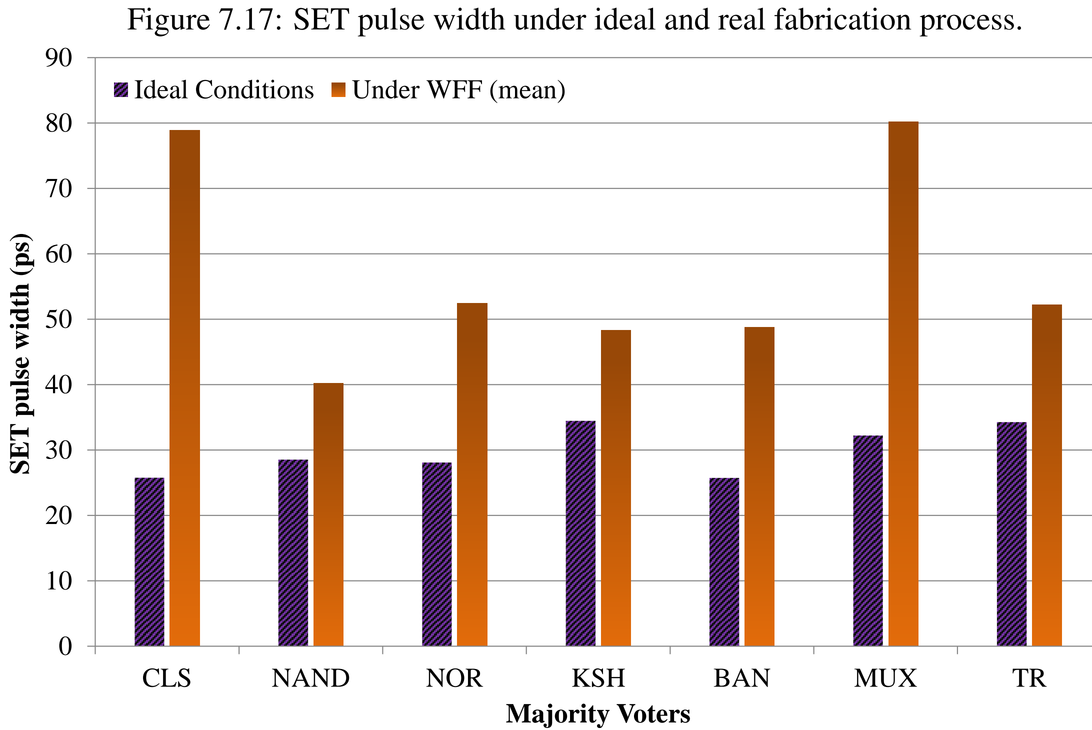
Table 7.13: Worst-case propagation delay under WFF.

MJV	Worst-case delay (ps)		
Circuits	μ	σ	σ/μ (%)
CLS	23.26	4.21	18.09
NAND	21.25	4.88	22.95
NOR	28.40	8.78	30.90
KSH	34.68	6.54	18.85
BAN	24.28	4.86	20.02
MUX	30.89	5.65	18.28
TR	31.61	7.93	25.10

Source: Adapted from Brendler et al. (2020).

Figure 7.17 shows the SET pulse width values under the ideal fabrication process and the WFF impact on these values. For all MJV circuits, the SET pulse width under WFF is larger than considering ideal conditions. CLS and MUX voters are the most impacted, the values considering the WFF are 2.1 and 1.5 times higher than the values under ideal conditions, respectively. The KSH voter is the least impacted with about 14ps of difference between the values.

Figure 7.17: SET pulse width under ideal and real fabrication process.



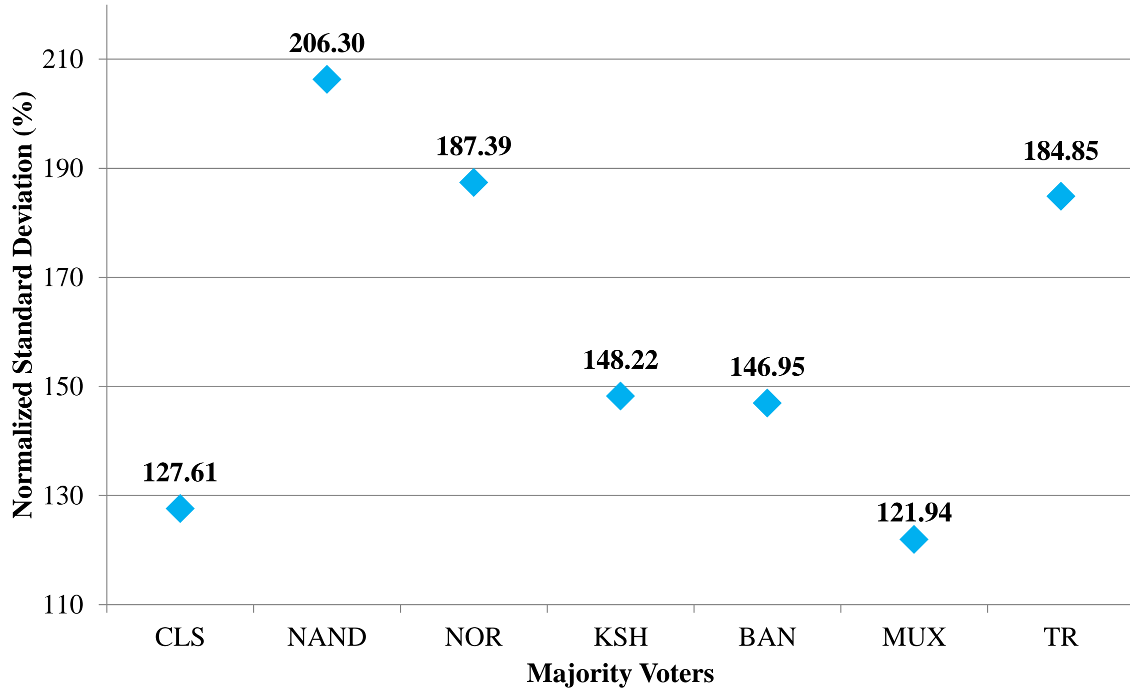
Source: Brendler et al. (2020).

The normalized standard deviation of the SET pulse width is shown in Figure 7.18. The smaller this deviation is, the more robust to the variability effects is the MJV. The average deviation of the different evaluated voters is 160.47%. The NAND voter is the most sensitive to the process variability effects, while the MUX voter is the most robust with an 84.4% smaller deviation value. This behavior is the opposite of what was seen when we analyzed the mean values of the SET pulse width. In the current analysis, the deviations are normalized by the mean, i.e., a smaller value of the SET pulse width means for the 2000 Monte Carlo simulations performed, tends to a more significant deviation. Still, this analysis allows observing the quantity and how much the values deviate from the mean values presented in the previous analysis. This behavior is reflected in the probability that the WFF will more or less impact a voter.

After obtaining the SET pulse width mean values and confirming that they are higher than the mean worst-case delay of each voter, the fault characterization in the

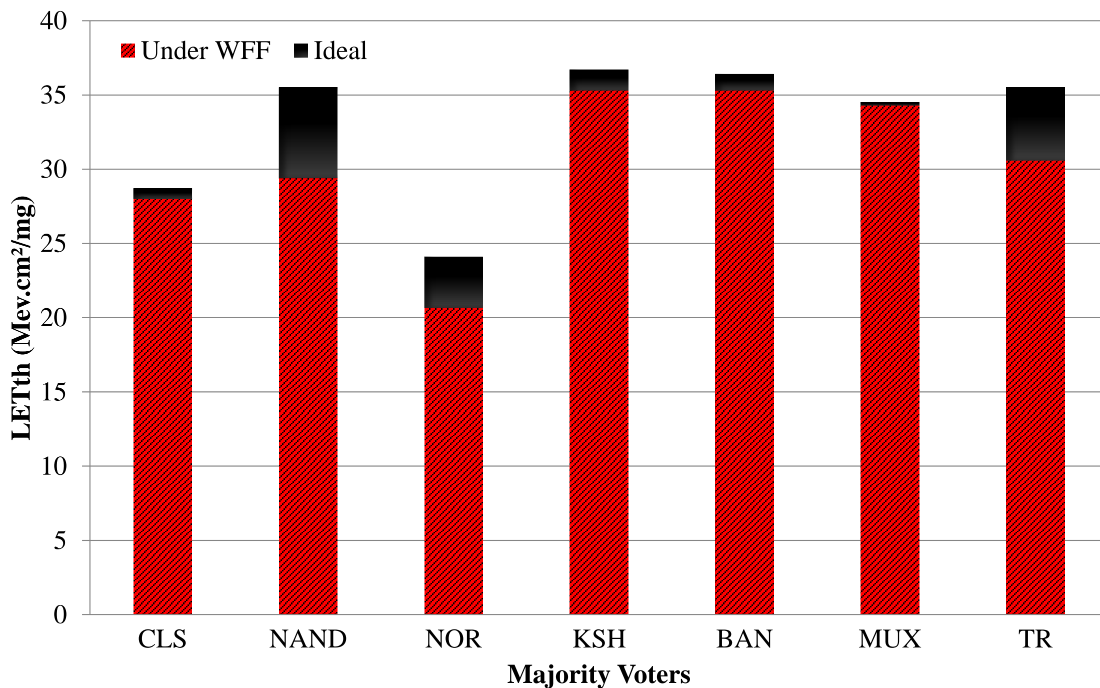
circuit output is complete. Then a new LET_{th} can be calculated considering the WFF impact. Figure 7.19 shows the difference between the LET_{th} obtained, considering the ideal fabrication process and the impact of the WFF for the evaluated MJV circuits. For

Figure 7.18: Normalized standard deviation of SET pulse width.



Source: Brendler et al. (2020).

Figure 7.19: LET_{th} considering ideal fabrication process and WFF impact.



Source: Brendler et al. (2020).

all MJV versions, the LET$_{th}$ considering the WFF impact is smaller than the LET$_{th}$ at ideal conditions. That is, due to WFF, a smaller amount of energy transferred by the particle is required to cause a disturbance in the circuit. All evaluated circuits become more sensitive to the radiation effects. Three of the seven analyzed voters showed high sensitivity to the process variability effects. The NAND voter is the most impacted, with a new LET$_{th}$ 17.2% lower than the ideal LET$_{th}$. Besides presenting one of the greatest LET$_{th}$ of all versions, the MUX voter is also the least impacted by the WFF. The new LET$_{th}$ of the MUX voter is less than 1% lower than the ideal LET$_{th}$. That is, the voter is little impacted by the process variability effects considering this metric.

8 CONCLUSIONS

The technology scaling has provided significant improvement in terms of performance and power consumption of electronic devices. However, some challenges directly related to the reliability of designs are also introduced. The variability arising from the manufacturing process of transistors and the SET from the space radiation are essential concerns in the design of integrated circuits. This work evaluated the robustness of different circuits in FinFET technology, considering the process variability and the radiation effects. Three different applications were evaluated: logic functions, different implementations of C17 benchmark, and different majority voters versions. The process variability was evaluated trough the WFF of the metal gate, and the radiation effects were evaluated through the SET response, considering the process variability effects. All the experiments were carried out using 7nm FinFET ASAP7 PDK.

Regarding the process variability impact on the logic gates, the analysis show the small influence of a serial transistor position on the complex gate topology robustness. That is, it cannot be determined if the transistor close or far to the output node will be more robust to process variability effects, as this behavior is directly related to the logic function in question. Also, the choice of using three fins as transistor sizing is justified by presenting an average behavior, considering a design that aims both performance and low-power consumption. Many works use *nfin*=1 aiming at a low-power and reduced area design. However, in addition to the performance penalties, the difficulty of routing larger circuits due to the reduced active area is also not considered. Thus, this work aims to offer a new perspective about the FinFET transistors sizing.

From the process variability impact on the C17 different versions, it is possible to identify the best candidate gate mapping version depending on the optimization metric of a specific design. In the normalized standard deviation analysis, which evaluates how much the mean values of the 2000 Monte Carlo simulations vary, one can obtain the circuit robustness to the process variability effects. Versions V3 and V4 present the smallest deviations considering power and delay, respectively. For a design that requires a balance between delay and power consumption (PDP), besides being robust to the variability effects, the best options are V3 and V4 versions (letters (e) and (f) in Figure 6.7, respectively). They have considerably lower deviations for both analyzed metrics.

It was shown how much a different transistor arrangement would influence the impact of process variability. The normalized standard deviation values, comparing the

C17 circuit different versions, vary by up to 30% the robustness to delay, around 18% the robustness to power consumption and 25% the PDP deviation. That is to say: according to their design needs, the choice of a particular transistor arrangement that implements the same logic function is of the utmost importance.

The WFF impact on the SET response was evaluated in this work, considering different circuits. A set of logic functions, implemented in two different transistor topologies, and seven different voters were compared using the 7nm FinFET technology. Regarding the ideal fabrication process, the multi-level logic topology (considering the logic functions) and the KSH voter present the largest SET pulse widths. However, they also show the highest LET_{th} values. That is, at least considering the ideal fabrication, the SET pulse width has no direct relation to the LET_{th} value. If the design objective is a more robust circuit to radiation effects, regardless of performance, power and area penalties, the multi-level logic topology is the best option to implement logic functions and the KSH voter for the majority voter circuits. Also, the use of PTL, mainly near the output of the circuits, it is an excellent alternative to deal with the SET.

Considering the process variability impact on the SET response, it is first noticed the increase in the SET pulse width for all circuits. That is, the circuits become more sensitive to the radiation effects. The complex gate topology presents a large variation of the SET pulse width values, exceeding the multi-level topology values. Even with this variation, the LET_{th} of the multi-level topology remains larger for two of the four logic functions and practically the same for the other two. This behavior confirms the conclusion of the previous analysis, in which the SET pulse width does not have a direct relation with the LET_{th} value and the multi-level logic topology (to implement logic functions) is the best option to deal with the SET effects. Also, the mean values of the SET pulse width are unrelated to each voter's sensitivity to the process variability effects, as evidenced by the normalized standard deviation. In this analysis, the MUX voter presents the best results, being the least impacted by the process variability and presenting one of the largest LET_{th} together with the KSH and BAN voters.

Although the multi-level logic topology is more robust to the reliability effects evaluated in this work, it is also important to highlight the complex gate topology advantages. The logic functions designed in the complex gate topology provide a lower delay, lower total power consumption and smaller used area. Even being more impacted by the reliability challenges, the complex gate topology can continue providing a lower delay and power consumption, depending on the difference in the topologies' metrics values at

ideal conditions.

The LET_{th} values of each circuit can also be related to the environment where they will operate. On average, the LET_{th} values of this study, considering ideal conditions, are around 42 Mev.cm^2/mg and 30 Mev.cm^2/mg for the evaluated logic functions and voters, respectively. Considering the WFF impact the values are around 36 Mev.cm^2/mg and 24 Mev.cm^2/mg. Even considering the WFF impact, these circuits are robust to the radiation effects at the ground level (LET $\leq$ 10 Mev.cm^2/mg). That is, they can be used in several applications that require a high level of fault tolerance, such as vehicles, servers and airplanes. However, these circuits are still susceptible to faults at the atmospheric level. The robustness of these circuits must be considered for applications operating in an atmospheric environment, such as low-Earth orbit satellites.

The main conclusion of the radiation experiments is about the WFF impact on the LET_{th}. For all circuits (logic functions and MJVs), regardless of the topology used, the LET_{th} value is lower, i.e., the circuits become more sensitive to the radiation effects considering the process variability impact. This conclusion is of utmost importance because it indicates that to determine the LET_{th} of a circuit, one must also consider other reliability factors such as process variability.

The analyzes of circuits with different sizes and complexities in the experiments proposed in this dissertation provides a validation of the results obtained. Both in the analyzes that considers only the process variability impact and in the analyzes of the WFF impact in the SET response, the circuits of greater complexity (C17 and MJV circuits) follow the same behavior presented by the logic functions. This behavior proves that the results obtained for each experiment can be extended for the reliability analyzes in several circuits with different sizes and complexities, according to the designer's needs.

8.1 Future Works

For the future of this work, I intend to continue evaluating the circuit reliability but focusing on the radiation effects. Several options for continuing work can be developed separately or in parallel:

- Explore the impact of other radiation effects on integrated circuits. Still considering the SEE, I also intend to evaluate the SEU effects on traditional circuits as: Flip-Flops and SRAMs. However, it would also be interesting to evaluate other types of

radiation, such as TID or DD.

- Extend the analyzes of C17 circuits also to consider the effects of radiation. As already done in the current work, using the majority voters, the main objective is to evaluate the SET response in bigger circuits and with more than one output.
- Evaluate more circuit-level techniques to try to mitigate the effects of radiation and process variability, such as decoupling cells and sleep transistors. An alternative that is already being studied is the use of decoupling cells in the most sensitive nodes of C17 circuits.
- Assess the impact of radiation effects using a specific tool. Some institutes, mainly outside the country, use their tools to characterize the radiation effects assessing SET and SEU. For this purpose, the 3D radial distribution of generated cartoons and the charge collection process are calculated based on BEOL and FEOL, obtained directly from layout design files in Graphic Data System (GDS) format.
- Reproduction of this study in other technologies and technological nodes. It would be interesting to evaluate the FD-SOI technology compared to FinFET technology.

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ANNEX A — LIST OF PUBLICATIONS

ARTICLES IN SCIENTIFIC JOURNALS:

1. **BRENDLER, LEONARDO H.**; ZIMPECK, ALEXANDRA L.; MEINHARDT, CRISTINA; REIS, RICARDO. Multi-Level Design Influences on Robustness Evaluation of 7nm FinFET Technology. IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS I: REGULAR PAPERS, v. 67, n. 2, p. 553-564, 2020. doi: 10.1109/TCSI.2019.2927374.
2. **BRENDLER, LEONARDO H.**; ZIMPECK, ALEXANDRA L.; MEINHARDT, CRISTINA; REIS, RICARDO. Gate mapping impact on variability robustness in FinFET technology. MICROELECTRONICS RELIABILITY, v. 100, p. 113448, 2019. doi: 10.1016/j.microrel.2019.113448.

BOOK CHAPTERS:

1. **BRENDLER, LEONARDO. H.**; ZIMPECK, ALEXANDRA L.; MEINHARDT, CRISTINA; REIS, RICARDO. Process Variability Impact on the SET Response of FinFET Multi-level Design. In: Metzler C., Gaillardon PE., De Micheli G., Silva-Cardenas C., Reis R. (eds) VLSI-SoC: New Technology Enabler. VLSI-SoC 2019. IFIP Advances in Information and Communication Technology, vol 586. Springer, Cham. 2020. doi: 10.1007/978-3-030-53273-4_5

COMPLETE WORKS PUBLISHED IN PROCEEDINGS OF CONFERENCES:

1. **BRENDLER, LEONARDO. H.**; ZIMPECK, ALEXANDRA L.; MEINHARDT, CRISTINA; REIS, RICARDO. Work-Function Fluctuation Impact on the SET Response of FinFET-based Majority Voters. In: 2020 IEEE 21st Latin-American Test Symposium (LATS), 2020. doi: 10.1109/LATS49555.2020.9093679.
2. **BRENDLER, LEONARDO. H.**; ZIMPECK, ALEXANDRA L.; MEINHARDT, CRISTINA; REIS, RICARDO. Evaluation of SET under Process Variability on FinFET Multi-level Design. In: 2019 IFIP/IEEE International Conference on Very Large Scale Integration (VLSI-SoC), 2019, p. 179. doi: 10.1109/VLSI-SoC.2019.8920336.

Summary published in proceedings of conferences:

1. **BRENDLER, LEONARDO. H.**; ZIMPECK, ALEXANDRA L.; MEINHARDT, CRISTINA; REIS, RICARDO. Circuit-Level Techniques to Mitigate Process Variability and SET on FinFET Technology. In: 2020 IEEE 21st Latin-American Test Symposium (LATS) - Master Thesis Contest, 2020.

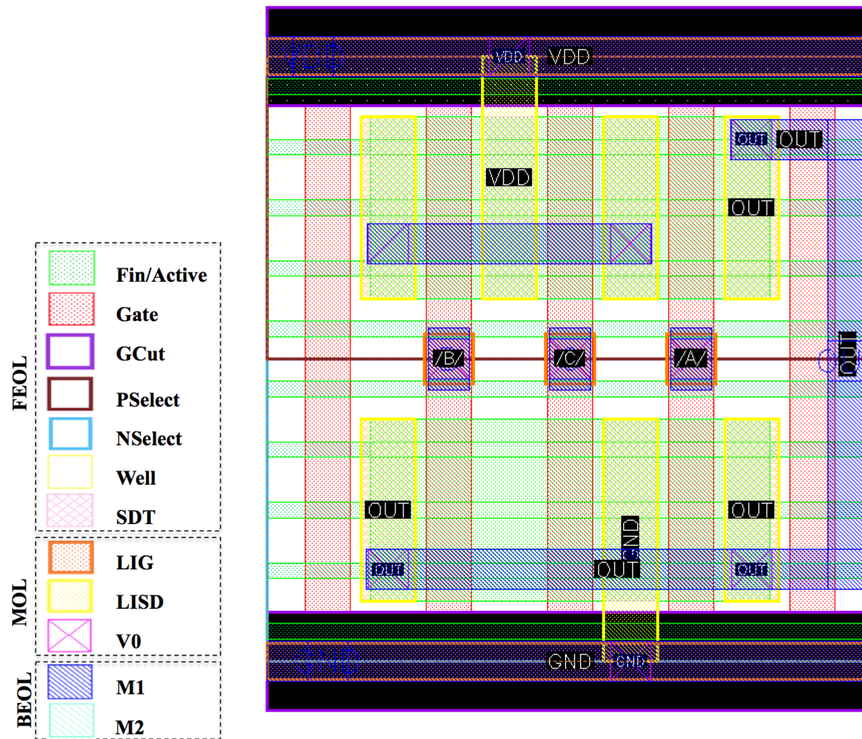
2. REIS, RICARDO; MEINHARDT, CRISTINA; ZIMPECK, ALEXANDRA L.; **BRENDLER, LEONARDO. H.**; MORAES, LEONARDO. Circuit Level Design Methods to Mitigate Soft Errors. In: 2020 IEEE 21st Latin-American Test Symposium (LATS) - Invited Tutorial, 2020. doi: 10.1109/LATS49555.2020.9093683.

3. **BRENDLER, LEONARDO H.** ; ZIMPECK, ALEXANDRA L. ; MEINHARDT, CRISTINA ; REIS, RICARDO. Impact of Process Variability and Single Event Transient on FinFET Technology. In: 2019 IFIP/IEEE 27th International Conference on Very Large Scale Integration (VLSI-SoC), 2019. p. 249. doi: 10.1109/VLSI-SoC.2019.8920355.

ANNEX B — LAYOUTS DEVELOPED

Figure B.1: AOI21 layout in the two topologies: (a) complex gate and (b) multi-level of NAND2.

(a) AOI21 - Complex Gate



(b) AOI21 - Multi-level Logic

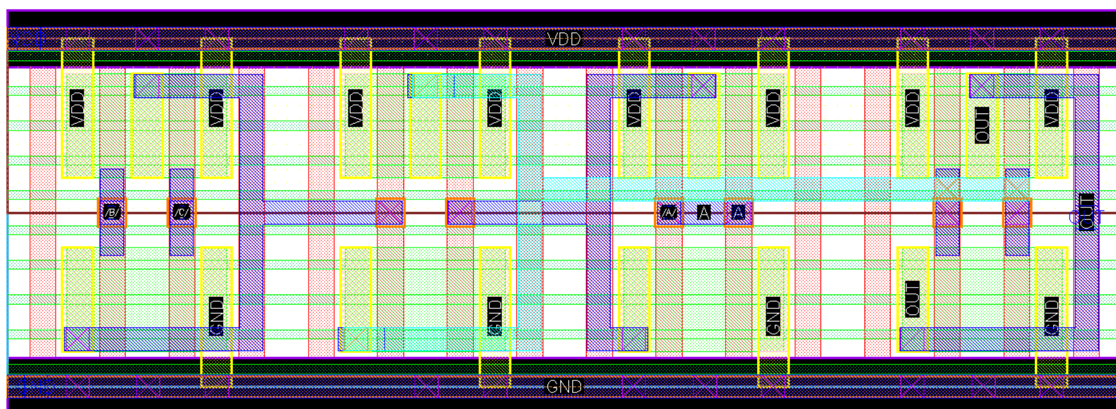
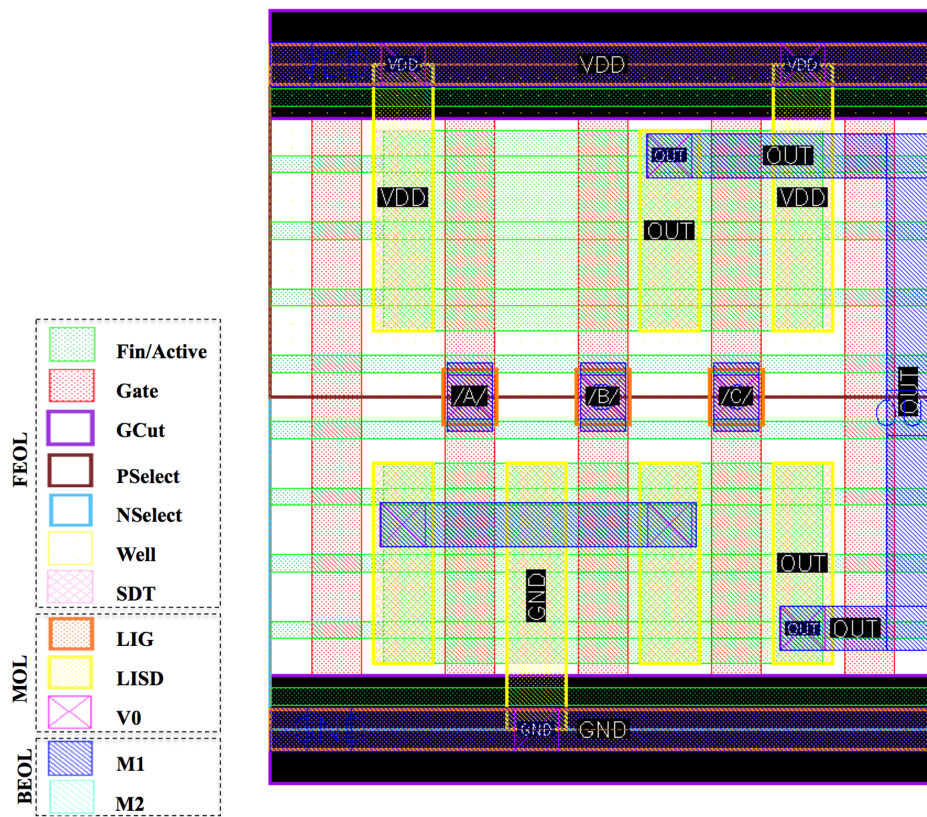


Figure B.2: OAI21 layout in the two topologies: (a) complex gate and (b) multi-level of NAND2.

(a) OAI21 - Complex Gate



(b) OAI21 - Multi-level Logic

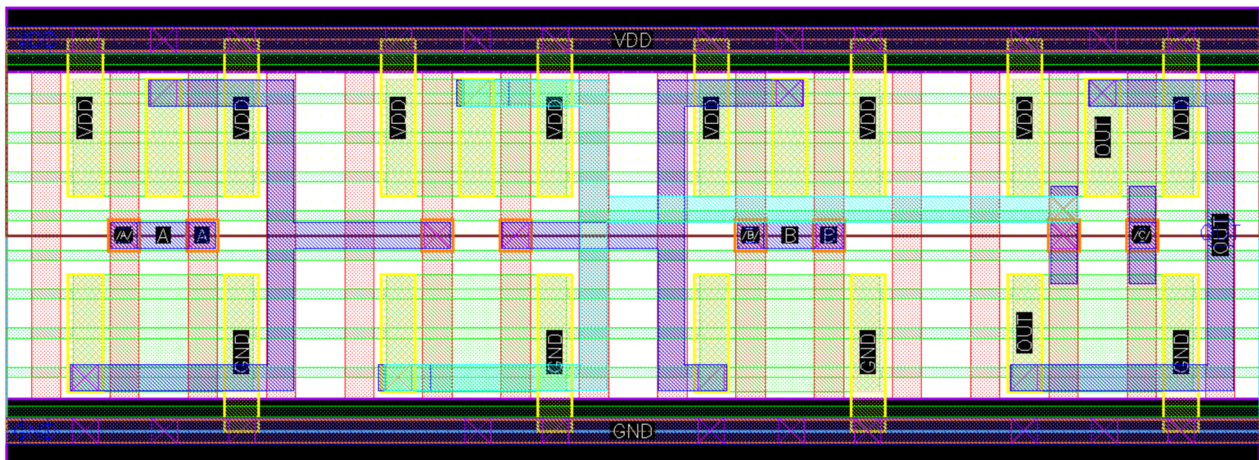
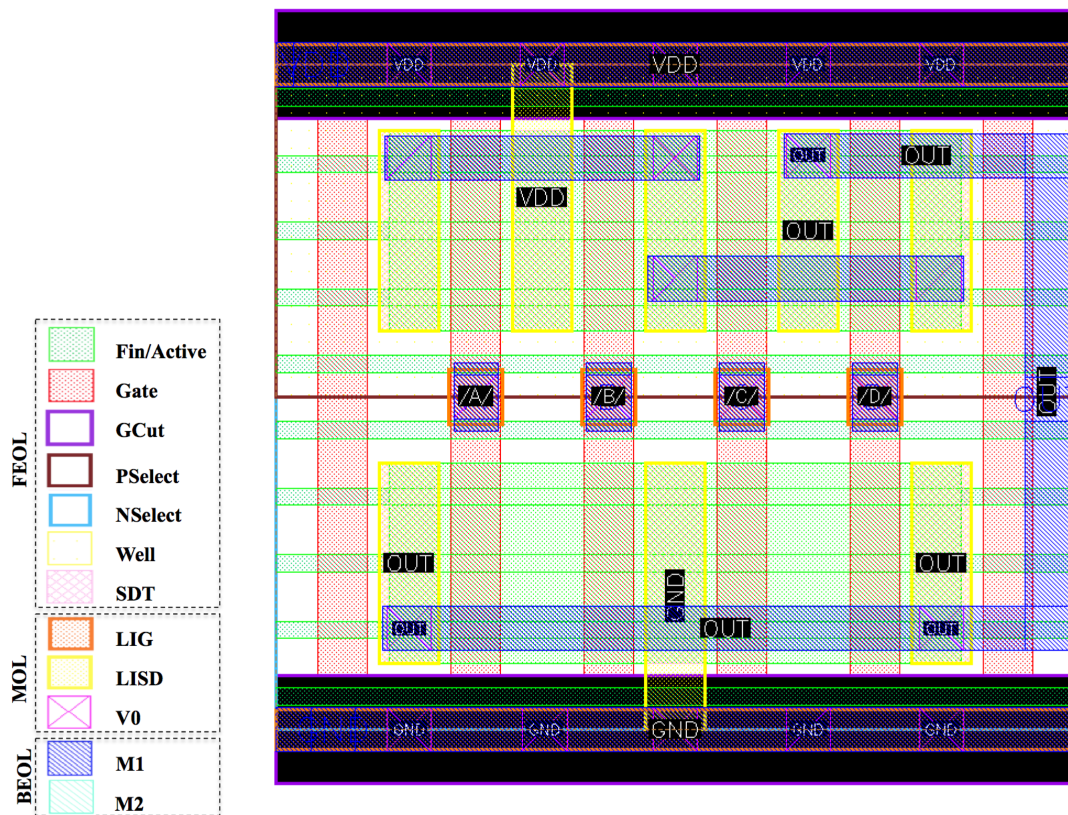


Figure B.3: AOI22 layout in the two topologies: (a) complex gate and (b) multi-level of NAND2.

(a) AOI22 - Complex Gate



(b) AOI22 - Multi-level Logic

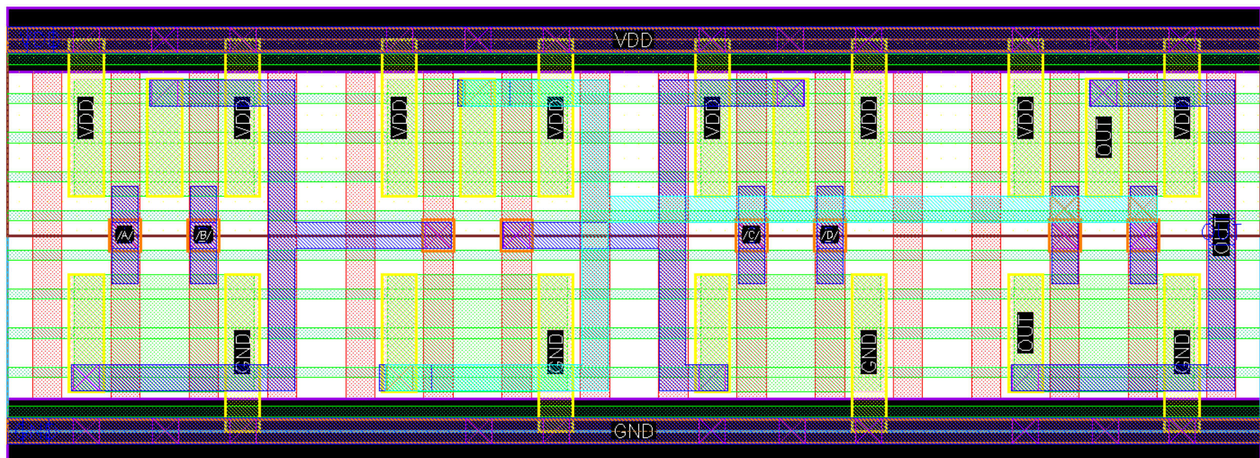
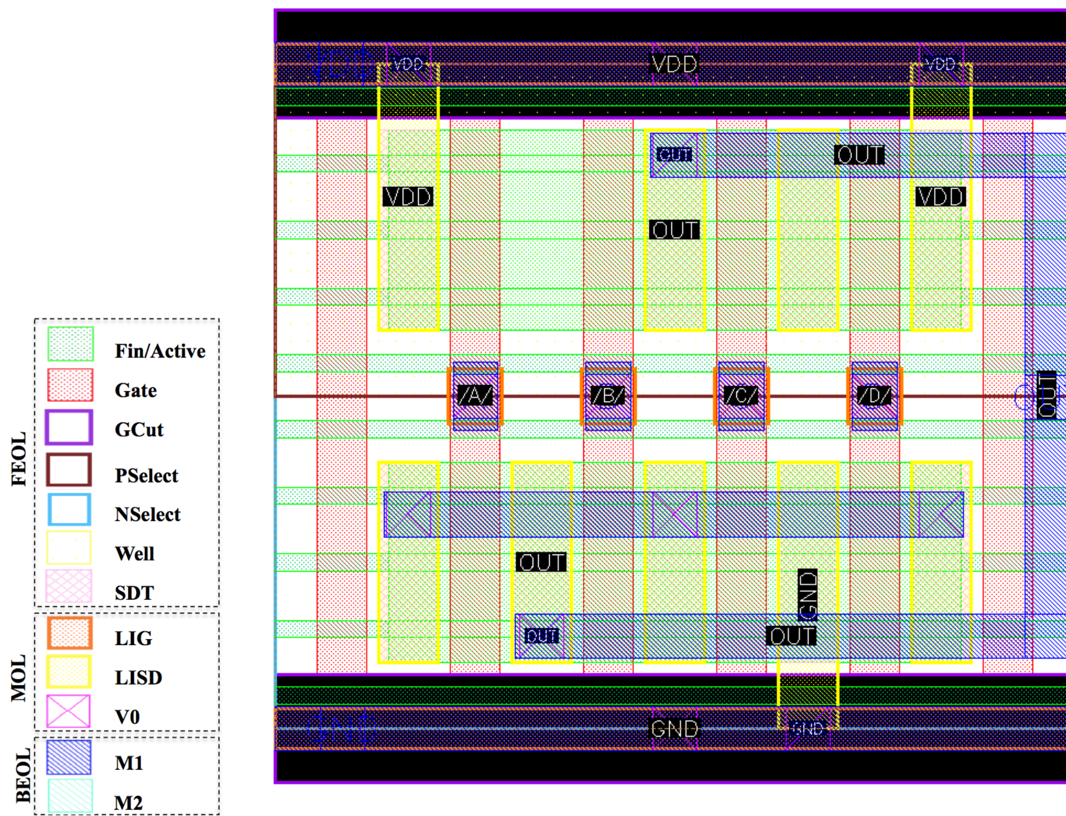


Figure B.4: OAI22 layout in the two topologies: (a) complex gate and (b) multi-level of NAND2.

(a) OAI22 - Complex Gate



(b) OAI22 - Multi-level Logic

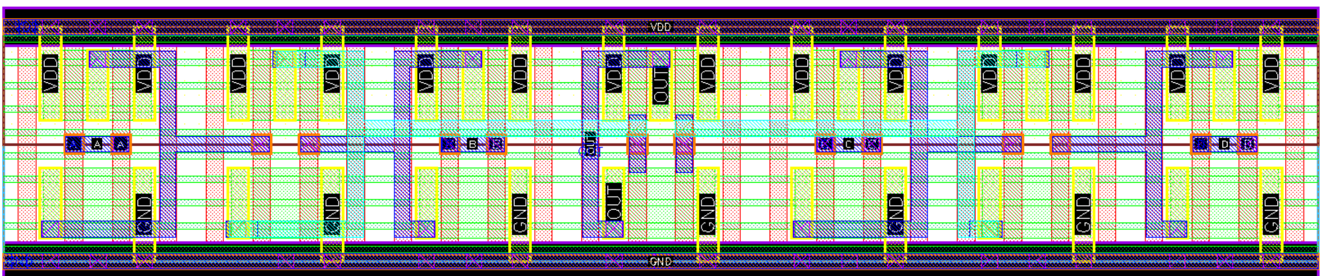
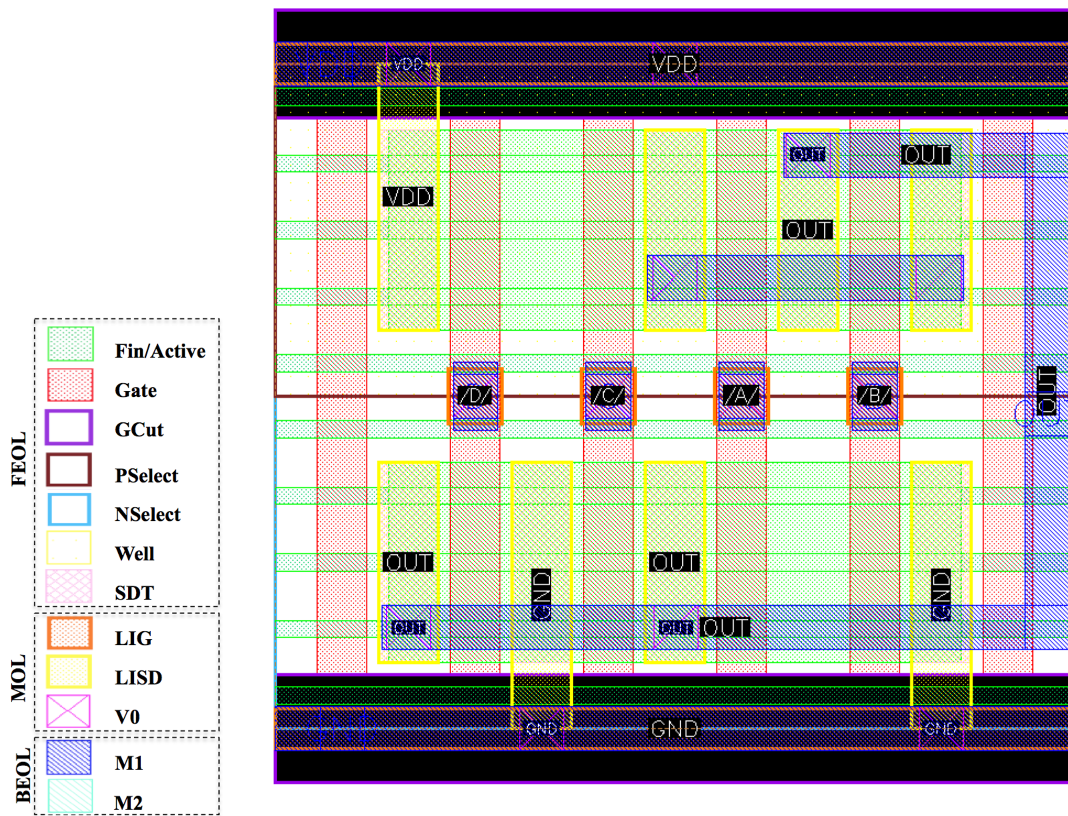


Figure B.5: AOI211 layout in the two topologies: (a) complex gate and (b) multi-level of NAND2.

(a) AOI211 - Complex Gate



(b) AOI211 - Multi-level Logic

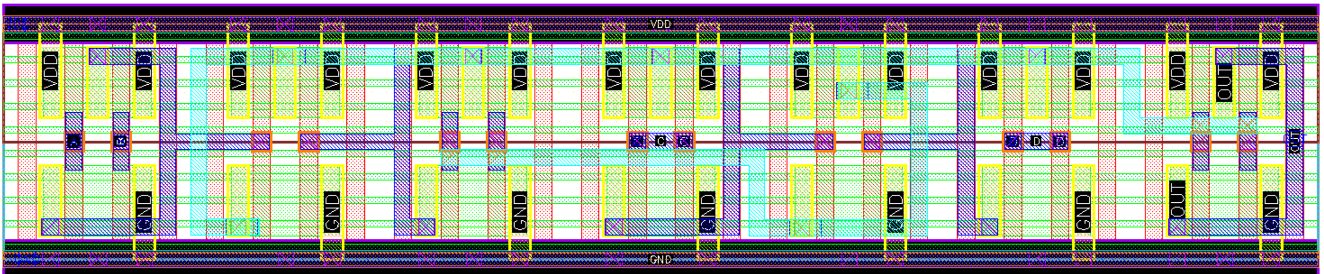
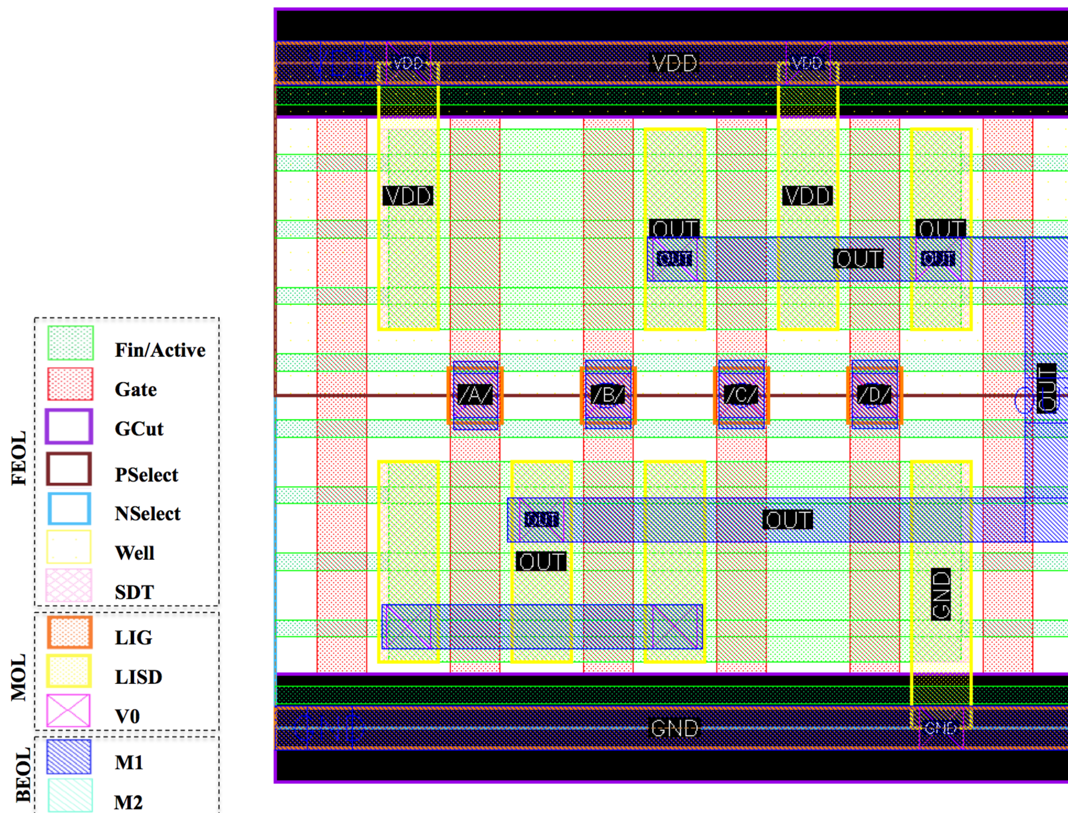


Figure B.6: OAI211 layout in the two topologies: (a) complex gate and (b) multi-level of NAND2.

(a) OAI211 - Complex Gate



(b) OAI211 - Multi-level Logic

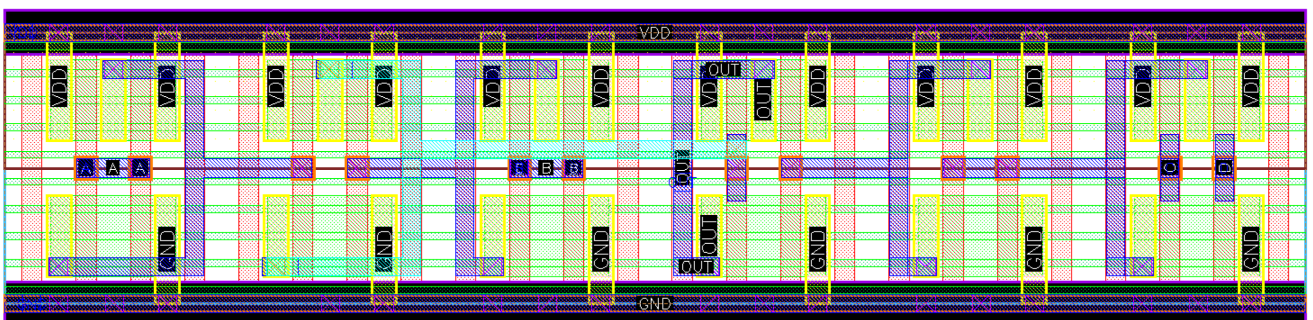
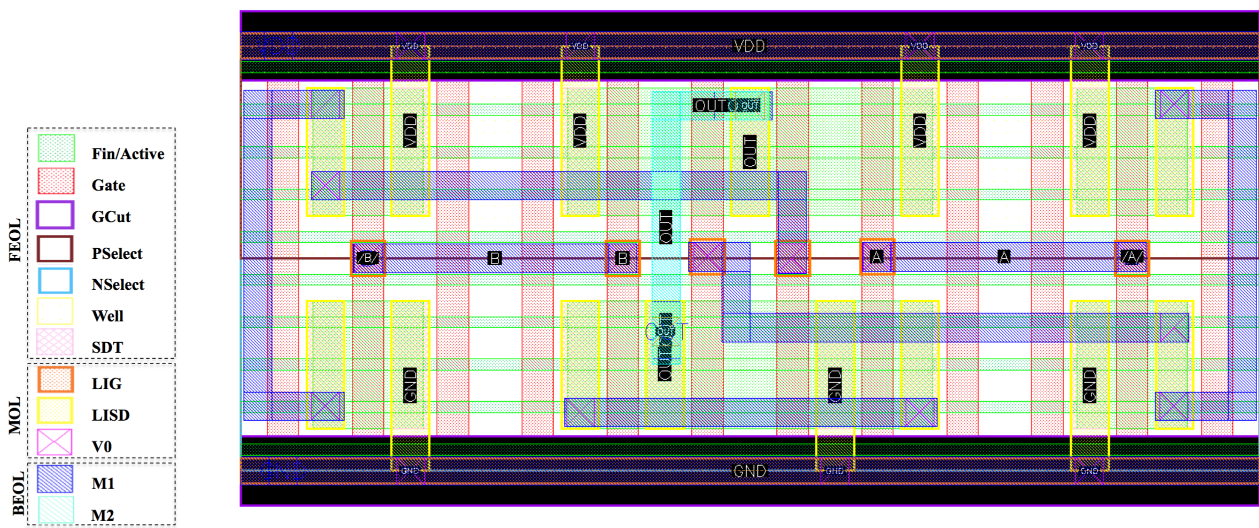
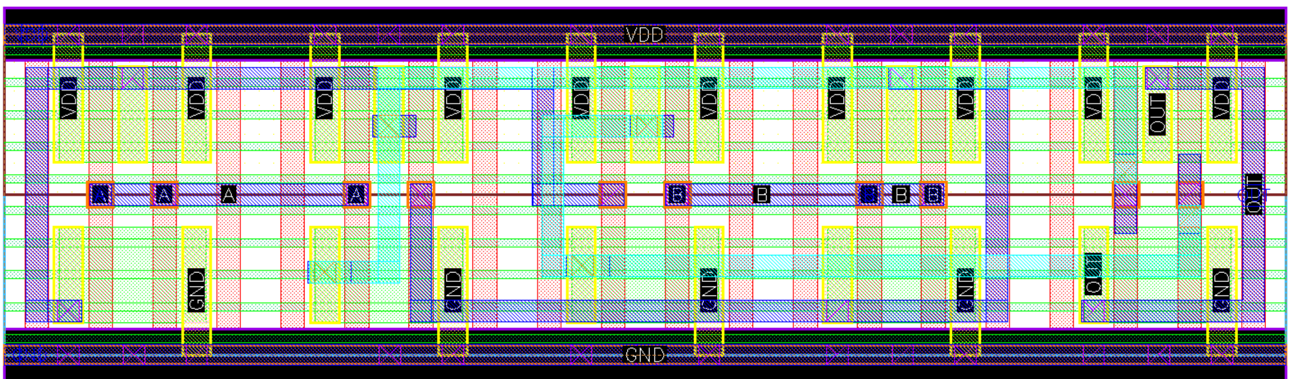


Figure B.7: XOR layout in the two topologies: (a) complex gate and (b) multi-level of NAND2.

(a) XOR - Complex Gate



(b) XOR - Multi-level Logic



ANNEX C — CIRCUITS DESCRIPTION

C.1 C17 benchmark

Listing C.1: Subcircuits of logic gates used in C17 Versions: V0-V4.

```
.include "./models/hspice/7nm_TT.pm"

.option post = 2
.param supply = 0.7

.subckt INV in out vdd gnd
MN0 out in gnd in nmos_rvt nfin=3
MP0 vdd in out in pmos_rvt nfin=3
.ends

.subckt NAND2 a b out vdd gnd
MN1 x1 b gnd b nmos_rvt nfin=3
MN2 out a x1 a nmos_rvt nfin=3
MP1 vdd a out a pmos_rvt nfin=3
MP2 vdd b out b pmos_rvt nfin=3
.ends

.subckt NOR2 a b out vdd gnd
MN6 out a gnd a nmos_rvt nfin=3
MN7 out b gnd b nmos_rvt nfin=3
MP6 vdd a x1 a pmos_rvt nfin=3
MP7 x1 b out b pmos_rvt nfin=3
.ends

.subckt AND2 a b out vdd gnd
MN3 x1 b gnd b nmos_rvt nfin=3
MN4 x2 a x1 a nmos_rvt nfin=3
MN5 out x2 gnd x2 nmos_rvt nfin=3
MP3 vdd a x2 a pmos_rvt nfin=3
MP4 vdd b x2 b pmos_rvt nfin=3
MP5 vdd x2 out x2 pmos_rvt nfin=3
.ends

.subckt OR2 a b out vdd gnd
MN3 x1 a gnd a nmos_rvt nfin=3
```

```
MN4 x1 b gnd b nmos_rvt nfin=3
MN5 out x1 gnd x1 nmos_rvt nfin=3
MP3 vdd a x2 a pmos_rvt nfin=3
MP4 x2 b x1 b pmos_rvt nfin=3
MP5 vdd x1 out x1 pmos_rvt nfin=3
.ends

.end
```

Listing C.2: C17 - Complex Version

```
.include "./models/hspice/7nm_TT.pm"

.option post = 2
.param supply = 0.7

Vvdd vdd gnd supply
Vgnd gnd gnd 0

MN1 x1 na gnd na nmos_rvt nfin=3
MN2 x1 nb gnd nb nmos_rvt nfin=3
MN3 out1 x2 x1 x2 nmos_rvt nfin=3
MN4 x3 nd gnd nd nmos_rvt nfin=3
MN5 x3 nb gnd nb nmos_rvt nfin=3
MN6 x2 c x3 c nmos_rvt nfin=3
MN7 x4 ne gnd ne nmos_rvt nfin=3
MN8 x5 d gnd d nmos_rvt nfin=3
MN9 x4 b x5 b nmos_rvt nfin=3
MN10 out2 x2 x4 x2 nmos_rvt nfin=3

MP1 vdd na x8 na pmos_rvt nfin=3
MP2 x8 nb out1 nb pmos_rvt nfin=3
MP3 vdd x2 out1 x2 pmos_rvt nfin=3
MP4 vdd nb x6 nb pmos_rvt nfin=3
MP5 x6 nd x2 nd pmos_rvt nfin=3
MP6 vdd c x2 c pmos_rvt nfin=3
MP7 vdd b x7 b pmos_rvt nfin=3
MP8 vdd d x7 d pmos_rvt nfin=3
MP9 x7 ne out2 ne pmos_rvt nfin=3
MP10 vdd x2 out2 x2 pmos_rvt nfin=3

.tran 0.001n 228n
.end
```

Listing C.3: C17 - V0 Version

```
.include "./models/hspice/7nm_TT.pm"

.option post = 2
.param supply = 0.7

Vvdd vdd gnd supply
Vgnd gnd gnd 0

X11 b a outx1 vdd gnd NAND2
X12 b d outx2 vdd gnd NAND2
X13 outx2 c outx3 vdd gnd NAND2
X14 outx3 outx1 out1 vdd gnd NAND2
X17 b d outx6 vdd gnd AND2
X18 c e outx7 vdd gnd NOR2
X19 outx7 outx6 out2 vdd gnd NOR2

.tran 0.001n 228n

.end
```

Listing C.4: C17 - V1 Version

```
.include "./models/hspice/7nm_TT.pm"

.option post = 2
.param supply = 0.7

Vvdd vdd gnd supply
Vgnd gnd gnd 0

X11 b a outx1 vdd gnd NAND2
X12 b d outx2 vdd gnd NAND2
X13 outx2 c outx3 vdd gnd NAND2
X14 outx3 outx1 out1 vdd gnd NAND2
X15 d outx4 vdd gnd INV
X16 b outx5 vdd gnd INV
X17 outx5 outx4 outx6 vdd gnd NOR2
X18 c e outx7 vdd gnd NOR2
X19 outx7 outx6 out2 vdd gnd NOR2

.tran 0.001n 228n

.end
```

Listing C.5: C17 - V2 Version

```
.include "./models/hspice/7nm_TT.pm"

.option post = 2
.param supply = 0.7

Vvdd vdd gnd supply
Vgnd gnd gnd 0

X11 b a outx1 vdd gnd NAND2
X12 b d outx2 vdd gnd NAND2
X13 outx2 c outx3 vdd gnd NAND2
X14 c e outx4 vdd gnd OR2
X15 outx1 outx3 out1 vdd gnd NAND2
X16 outx4 outx2 out2 vdd gnd AND2

.tran 0.001n 228n

.end
```

Listing C.6: C17 - V3 Version

```
.include "./models/hspice/7nm_TT.pm"

.option post = 2
.param supply = 0.7

Vvdd vdd gnd supply
Vgnd gnd gnd 0

X11 a b outx1 vdd gnd NAND2
X12 b d outx2 vdd gnd NAND2
X13 c outx2 outx3 vdd gnd NAND2
X14 outx2 e outx4 vdd gnd NAND2
X15 outx1 outx3 out1 vdd gnd NAND2
X16 outx3 outx4 out2 vdd gnd NAND2

.tran 0.001n 228n

.end
```

Listing C.7: C17 - V4 Version

```
.include "./models/hspice/7nm_TT.pm"

.option post = 2
.param supply = 0.7

Vvdd vdd gnd supply
Vgnd gnd gnd 0

X11 c outx1 vdd gnd INV
X12 b d outx2 vdd gnd AND2
X13 outx2 outx1 outx3 vdd gnd NOR2
X14 b a outx4 vdd gnd AND2
X15 outx4 outx3 out1 vdd gnd OR2
X16 c e outx5 vdd gnd NOR2
X17 outx5 outx2 out2 vdd gnd NOR2

.tran 0.001n 228n

.end
```

C.2 Majority Voters

Listing C.8: MJV - CLS Version

```
.include "./models/hspice/7nm_TT.pm"

.option post = 2
.param supply = 0.7

Vvdd vdd gnd supply
Vgnd gnd gnd 0

MN1 x0 a x1 a nmos_rvt nfin=3
MN2 x1 b gnd b nmos_rvt nfin=3
MN3 x0 a x2 a nmos_rvt nfin=3
MN4 x2 c gnd c nmos_rvt nfin=3
MN5 x0 b x3 b nmos_rvt nfin=3
MN6 x3 c gnd c nmos_rvt nfin=3
MNi out x0 gnd x0 nmos_rvt nfin=3

MP1 vdd b x4 b pmos_rvt nfin=3
MP2 x4 a x5 a pmos_rvt nfin=3
MP3 x5 a x0 a pmos_rvt nfin=3
MP4 vdd c x4 c pmos_rvt nfin=3
MP5 x4 c x5 c pmos_rvt nfin=3
MP6 x5 b x0 b pmos_rvt nfin=3
MPi vdd x0 out x0 pmos_rvt nfin=3

.tran 0.001n 30n

.end
```

Listing C.9: MJV - NAND Version

```
.include "./models/hspice/7nm_TT.pm"

.option post = 2
.param supply = 0.7

Vvdd vdd gnd supply
Vgnd gnd gnd 0

MN1 x0 a x1 a nmos_rvt nfin=3
MN2 x1 b gnd b nmos_rvt nfin=3
MN3 x2 a x3 a nmos_rvt nfin=3
MN4 x3 c gnd c nmos_rvt nfin=3
MN5 x4 b x5 b nmos_rvt nfin=3
MN6 x5 c gnd c nmos_rvt nfin=3
MN7 out x0 x6 x0 nmos_rvt nfin=3
MN8 x6 x2 x7 x2 nmos_rvt nfin=3
MN9 x7 x4 gnd x4 nmos_rvt nfin=3

MP1 vdd a x0 a pmos_rvt nfin=3
MP2 vdd b x0 b pmos_rvt nfin=3
MP3 vdd a x2 a pmos_rvt nfin=3
MP4 vdd c x2 c pmos_rvt nfin=3
MP5 vdd b x4 b pmos_rvt nfin=3
MP6 vdd c x4 c pmos_rvt nfin=3
MP7 vdd x0 out x0 pmos_rvt nfin=3
MP8 vdd x2 out x2 pmos_rvt nfin=3
MP9 vdd x4 out x4 pmos_rvt nfin=3

.tran 0.001n 30n

.end
```

Listing C.10: MJV - NOR Version

```
.include "./models/hspice/7nm_TT.pm"

.option post = 2
.param supply = 0.7

Vvdd vdd gnd supply
Vgnd gnd gnd 0

MN1 x0 a gnd a nmos_rvt nfin=3
MN2 x0 b gnd b nmos_rvt nfin=3
MN3 x1 a gnd a nmos_rvt nfin=3
MN4 x1 c gnd c nmos_rvt nfin=3
MN5 x2 b gnd b nmos_rvt nfin=3
MN6 x2 c gnd c nmos_rvt nfin=3
MN7 out x0 gnd x0 nmos_rvt nfin=3
MN8 out x1 gnd x1 nmos_rvt nfin=3
MN9 out x2 gnd x2 nmos_rvt nfin=3

MP1 vdd a x3 a pmos_rvt nfin=3
MP2 x3 b x0 b pmos_rvt nfin=3
MP3 vdd a x4 a pmos_rvt nfin=3
MP4 x4 c x1 c pmos_rvt nfin=3
MP5 vdd b x5 b pmos_rvt nfin=3
MP6 x5 c x2 c pmos_rvt nfin=3
MP7 vdd x0 x6 x0 pmos_rvt nfin=3
MP8 x6 x1 x7 x1 pmos_rvt nfin=3
MP9 x7 x2 out x2 pmos_rvt nfin=3

.tran 0.001n 30n

.end
```

Listing C.11: MJV - KSH Version

```
.include "./models/hspice/7nm_TT.pm"

.option post = 2
.param supply = 0.7

Vvdd vdd gnd supply
Vgnd gnd gnd 0

Xi0 a na vdd gnd INV
Xi1 b nb vdd gnd INV
Xi2 c nc vdd gnd INV

MN1 x0 na x1 na nmos_rvt nfin=3
MN2 x1 nb gnd nb nmos_rvt nfin=3
MN3 x0 a x2 a nmos_rvt nfin=3
MN4 x2 b gnd b nmos_rvt nfin=3
MN5 x3 nc x4 nc nmos_rvt nfin=3
MN6 x4 nb gnd nb nmos_rvt nfin=3
MN7 x3 c x5 c nmos_rvt nfin=3
MN8 x5 b gnd b nmos_rvt nfin=3
MN9 x6 x0 gnd x0 nmos_rvt nfin=3
MN10 x7 x3 gnd x3 nmos_rvt nfin=3
MN11 x0 x6 x8 x6 nmos_rvt nfin=3
MN12 x7 x0 x8 x0 nmos_rvt nfin=3
MN13 x9 x8 gnd x8 nmos_rvt nfin=3
MN14 a x9 out x9 nmos_rvt nfin=3
MN15 c x8 out x8 nmos_rvt nfin=3

MP1 vdd b x10 b pmos_rvt nfin=3
MP2 x10 na x0 na pmos_rvt nfin=3
MP3 vdd nb x11 nb pmos_rvt nfin=3
MP4 x11 a x0 a pmos_rvt nfin=3
MP5 vdd b x12 b pmos_rvt nfin=3
MP6 x12 nc x3 nc pmos_rvt nfin=3
MP7 vdd nb x13 nb pmos_rvt nfin=3
MP8 x13 c x3 c pmos_rvt nfin=3
MP9 vdd x0 x6 x0 pmos_rvt nfin=3
MP10 vdd x3 x7 x3 pmos_rvt nfin=3
MP11 x0 x0 x8 x0 pmos_rvt nfin=3
MP12 x7 x6 x8 x6 pmos_rvt nfin=3
```

```
MP13 vdd x8 x9 x8 pmos_rvt nfin=3
MP14 a x8 out x8 pmos_rvt nfin=3
MP15 c x9 out x9 pmos_rvt nfin=3

.tran 0.001n 30n

.end
```

Listing C.12: MJV - BAN Version

```
.include "./models/hspice/7nm_TT.pm"

.option post = 2
.param supply = 0.7

Vvdd vdd gnd supply
Vgnd gnd gnd 0

Xi0 a na vdd gnd INV
Xi1 b nb vdd gnd INV
Xi2 c nc vdd gnd INV

MN1 x0 na x1 na nmos_rvt nfin=3
MN2 x1 nb gnd nb nmos_rvt nfin=3
MN3 x0 a x2 a nmos_rvt nfin=3
MN4 x2 b gnd b nmos_rvt nfin=3
MN5 x3 x0 gnd x0 nmos_rvt nfin=3
MN6 b x3 out x3 nmos_rvt nfin=3
MN7 c x0 out x0 nmos_rvt nfin=3

MP1 vdd b x4 b pmos_rvt nfin=3
MP2 x4 na x0 na pmos_rvt nfin=3
MP3 vdd nb x5 nb pmos_rvt nfin=3
MP4 x5 a x0 a pmos_rvt nfin=3
MP5 vdd x0 x3 x0 pmos_rvt nfin=3
MP6 b x0 out x0 pmos_rvt nfin=3
MP7 c x3 out x3 pmos_rvt nfin=3

.tran 0.001n 30n

.end
```

Listing C.13: MJV - MUX Version

```
.include "./models/hspice/7nm_TT.pm"

.option post = 2
.param supply = 0.7

Vvdd vdd gnd supply
Vgnd gnd gnd 0

X7 a na vdd gnd INV
X8 b nb vdd gnd INV
X9 c nc vdd gnd INV

MN1 x0 na x1 na nmos_rvt nfin=3
MN2 x1 nb gnd nb nmos_rvt nfin=3
MN3 x0 a x2 a nmos_rvt nfin=3
MN4 x2 b gnd b nmos_rvt nfin=3
MN5 x3 x0 gnd x0 nmos_rvt nfin=3
MN6 x4 a x5 a nmos_rvt nfin=3
MN7 x5 x3 gnd x3 nmos_rvt nfin=3
MN8 x6 x0 x7 x0 nmos_rvt nfin=3
MN9 x7 c gnd c nmos_rvt nfin=3
MN10 out x4 x8 x4 nmos_rvt nfin=3
MN11 x8 x6 gnd x6 nmos_rvt nfin=3

MP1 vdd b x9 b pmos_rvt nfin=3
MP2 x9 na x0 na pmos_rvt nfin=3
MP3 vdd nb x10 nb pmos_rvt nfin=3
MP4 x10 a x0 a pmos_rvt nfin=3
MP5 vdd x0 x3 x0 pmos_rvt nfin=3
MP6 vdd x3 x4 x3 pmos_rvt nfin=3
MP7 vdd a x4 a pmos_rvt nfin=3
MP8 vdd c x6 c pmos_rvt nfin=3
MP9 vdd x0 x6 x0 pmos_rvt nfin=3
MP10 vdd x6 out x6 pmos_rvt nfin=3
MP11 Vdd x4 out x4 pmos_rvt nfin=3

.tran 0.001n 30n

.end
```

Listing C.14: MJV - TR Version

```
.include "./models/hspice/7nm_TT.pm"

.option post = 2
.param supply = 0.7

Vvdd vdd gnd supply
Vgnd gnd gnd 0

Xi0 a na vdd gnd INV
Xi1 b nb vdd gnd INV
Xi2 c nc vdd gnd INV

MN1 x0 a x1 a nmos_rvt nfin=3
MN2 x1 b gnd b nmos_rvt nfin=3
MN3 x0 a x1 a nmos_rvt nfin=3
MN4 x1 b gnd b nmos_rvt nfin=3
MN5 x2 a x3 a nmos_rvt nfin=3
MN6 x3 c gnd c nmos_rvt nfin=3
MN7 x2 a x3 a nmos_rvt nfin=3
MN8 x3 c gnd c nmos_rvt nfin=3
MN9 x4 b x5 b nmos_rvt nfin=3
MN10 x5 c gnd c nmos_rvt nfin=3
MN11 x4 b x5 b nmos_rvt nfin=3
MN12 x5 c gnd c nmos_rvt nfin=3
MN13 out x0 x6 x0 nmos_rvt nfin=3
MN14 x6 x2 x7 x2 nmos_rvt nfin=3
MN15 x7 x4 gnd x4 nmos_rvt nfin=3
MN16 out x0 x6 x0 nmos_rvt nfin=3
MN17 x6 x2 x7 x2 nmos_rvt nfin=3
MN18 x7 x4 gnd x4 nmos_rvt nfin=3

MP1 vdd b x8 b pmos_rvt nfin=3
MP2 x8 b x0 b pmos_rvt nfin=3
MP3 vdd a x9 a pmos_rvt nfin=3
MP4 x9 a x0 a pmos_rvt nfin=3
MP5 vdd c x10 c pmos_rvt nfin=3
MP6 x10 c x2 c pmos_rvt nfin=3
MP7 vdd a x11 a pmos_rvt nfin=3
MP8 x11 a x2 a pmos_rvt nfin=3
MP9 vdd c x12 c pmos_rvt nfin=3
```

```
41 MP10 x12 c x4 c pmos_rvt nfin=3
42 MP11 vdd b x13 b pmos_rvt nfin=3
43 MP12 x13 b x4 b pmos_rvt nfin=3
44 MP13 vdd x4 x14 x4 pmos_rvt nfin=3
45 MP14 x14 x4 out x4 pmos_rvt nfin=3
46 MP15 vdd x2 x15 x2 pmos_rvt nfin=3
47 MP16 x15 x2 out x2 pmos_rvt nfin=3
48 MP17 vdd x0 x16 x0 pmos_rvt nfin=3
49 MP18 x16 x0 out x0 pmos_rvt nfin=3
50
51 .tran 0.001n 30n
52
53 .end
```