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Fabrication of Ion Sensitive Field Effect Transistors

Dissertação apresentada como requisito parcial para a obtenção do grau de Mestre em Microeletrônica

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Dedicatória

Aos meus pais, Fernando e Sueli, e a vó Dolores que me apoiaram incondicionalmente em todos os momentos. Muito obrigado.

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Fabrication of Ion Sensitive Field Effect Transistors

Resumo

Transistores de Efeito de Campo Sensíveis a Íons (ISFETs) revolucionaram a tecnologia de sensores químicos e de pH por serem pequenos e compatíveis com tecnologias de microfabricação em grande escala. Nós desenvolvemos uma metodologia para fabricar e caracterizar sensores ISFET para medida de pH no laboratório de microeletrônica da UFRGS. Sensores ISFET do tipo NMOS com camadas de silica e alumina foram fabricados com tecnologa CMOS padrão. Transistores de W=1000μm e L=10μm foram fabricados em conjunto para monitorar o processo de fabricação através de medidas de Capacitância-Tensão (C-V) e Corrente-Tensão (I-V). Os dispositivos foram colados em suportes de circuito impresso, manualmente microsoldados e encapsulados com cola epoxy. Com o dispotivo na ponta, o suporte foi conectado a um Analisador de Parâmetros de Semicondutores em conjunto com um eletrodo de referência comercial de Ag/AgCl e imersos em soluções de pH diferente para a realização de medidas de pH. A sensibilidade à variação de pH, definida como a variação na tensão de limiar devido a presença do eletrólito, para os sensores de silica foi de 30mV/pH em ácidos e 24mV/pH para bases. Sensores de alumina tiveram uma performance muito superior e exibiram sensibilidade de 32mV/pH em ácidos e 48mV/pH em bases. A tecnologia de fabricação e o conhecimento experimental desenvolvidos nesse trabalho fornecem uma fundação essencial para projetos de pesquisa locais que buscam a aplicação de sensores de estado sólido no sensoriamento de sistemas químicos ou biológicos.

Abstract

Ion Sensitive Field Effect Transistors (ISFETs) revolutionized pH and chemical sensing technology with its small size and compatibility with high integrated fabrication technologies. We developed a methodology to fabricate and characterize ISFET probes for pH measurement at UFRGS Microelectronics Laboratory. NMOS ISFETs with a sensing layer of silica or alumina were fabricated with standard CMOS technology. Transistors (W = 1000μm, L=10μm) were also fabricated to monitor the process through Capacitance-Voltage (C-V) and Current-Voltage (I-V) measurements. Devices were glued to supports made with Printed Circuit Board (PCB) methods, manually wire bonded and encapsulated with epoxy glue. These probes were immersed into different pH solutions along with a commercial Ag/AgCl reference electrode and both were connected to a Semiconductor Parameter Analyzer to perform pH measurements. The pH sensitivity, defined as the threshold voltage shift due to the presence of the electrolyte, was 30 mV/pH for acids and 24 mV/pH for bases in the case of the silica device. Alumina sensors performed much better due to its higher intrinsic buffer capacity and exhibited 32mV/pH for acids and 48mV/pH for bases. The fabrication technology and experimental expertise developed throughout this study provide an essential foundation for further local research endeavors on chemical and biological applications of solid-state ion sensors.

Contents

List of Figures

List of Tables

Chapter 1

Introduction

The amount of H^+ ions in an aqueous solution is of ubiquitous importance in chemistry. It separates bases from acids and is ,arguably, the most defining property of the biochemical behavior of a substance. $[H^+]$ values routinely extend over several orders of magnitude and are measured through their own logarithmic scale: the pH (1.1). The pH, defined by (1.1) is carefully controlled by our bodies within 0.1 accuracy on our blood and also separates a delicious orange juice from an awful one. Current technology for measuring pH is historically tied to the demanding members of the California Fruit Growers Association who in the 1930s contacted professors of the California Institute of Technology to develop what became known as the glass electrode pH meter[1]. It was widely adopted by industries and laboratories around the world, but it is not the only technology available to measure the concentration of ions in aqueous means.

$$pH = -log[H^+] \tag{1.1}$$

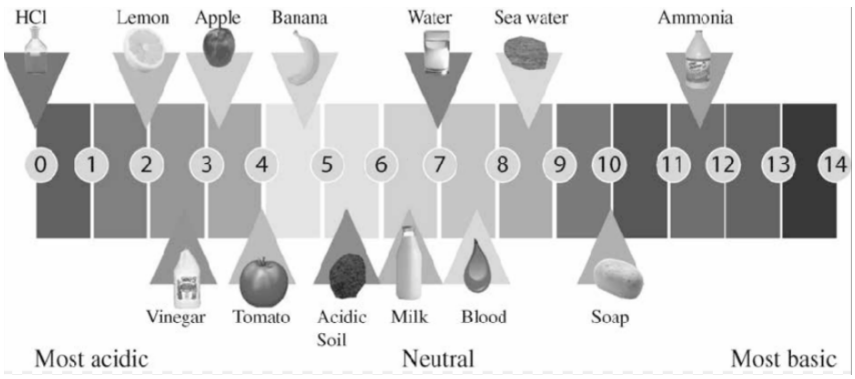


Figure 1.1: pH values for several substances.

In the 70s, the Ion Sensitive Field Effect Transistor (ISFET) was introduced by Bergveld [2] and independently by Matsuo [3] as an alternative way to measure pH in electrophysiological applications. The sensor uses a field effect transistor to measure ion activity[1] solutions such as pH. The idea is to measure changes in the transistor characteristic due to the electric field from the charged ionic compounds. To accomplish the metal gate is removed and its connection separated from the chip as a reference electrode inserted in the aqueous solution which is in contact with the exposed gate oxide (Figure 1.2).

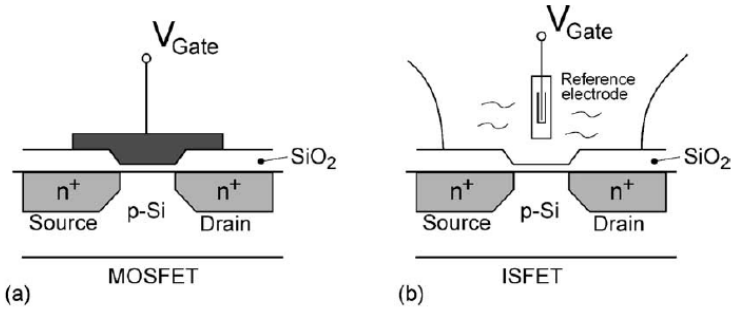


Figure 1.2: (a) The traditional MOSFET and (b) the ISFET. The metal gate is removed and the gate oxide exposed to the charges in a aqueous solution. The gate connection is tied to a reference electrode. Figure from [4].

The first application of the device took advantage of its small size and used it to probe the activity of Na^+ and H^+ ions from muscle fiber cells[5]. A micrometric transistor can make a local measurement of ion activity into an aqueous biological environment at a cellular level, something that a large glass electrode cannot. Despite its promise, electrophysiologists were not interested to use the ISFET technology at its infancy and 20 years would go by before ISFETs became routinely used for extracellular measurements [4].

Although the initial developments were made in the biomedical context, very soon the research on ISFETs went in the direction of general ion sensing. The use of different materials as a sensing layer for selectively measuring activity from specific ion species was soon shown to be possible [6] [7]. These efforts gave rise to a family of ISFET, the CHEMFETs whose membranes buffer a chosen ion species [4].

[1]Activity is discussed on chapter 3. It may be loosely defined as "effective concentration" when one takes into account the solvatation (electrical shielding) of the ion by other charged species, rendering it inactive for chemical reactions. For very dillute solutions ions are far apart, do not influence each other and the activity of an ion is maximum and equal to its molar concentration.

Different readout methods and engineering of the sensing layer were also explored to make the sensor sensitive to specific molecules or macromolecules of biomedical interest such as enzymes [8] and glucose [9] . These functionalizations of the sensor gave rise to the BIOFETs and its further subdivisions illustrated at Figure 1.3. Simply put, BIOFETs employ the transistor sensibility to charged groups selected by a biological structure attached to the gate.

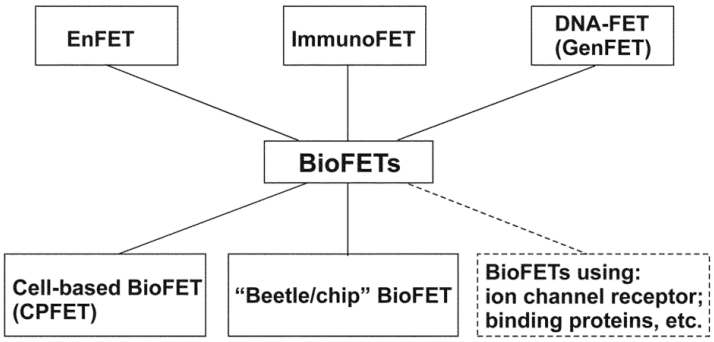


Figure 1.3: Diagram of possible BioFET classification depending on the biological recognition element used for detection [10]

ISFET ion electrodes did not hit the market until the early 1990s [4]. Proper encapsulation of the devices, long-term stability and a few incompatibilities with the standard CMOS process kept the technology away from wide commercialization for 20 years. Today, the products advertise fast response; unbreakability and possibility to probe viscous and semi-solid samples (cheese, meat); and aim markets where the vulnerability of the glass membrane electrode are issues. ISFET probes are applied to environmental monitoring, pharmaceutical needs and food pH measurements. A few companies that commercialize the products are Orion with its non-glass pHuture product line and Honeywell's Durafet (Figure 1.4). These are often accompanied by data storing and buffer recognition functions.

The potential of a CMOS-based sensor was fully realized with the introduction of ISFET arrays by the late 90s. Arrays like Figure (1.5) are ideal for DNA sequencing and played a central role in the "Human Genome Project". The technology has allowed the price of genome sequencing to drop at a higher rate than Moore's law since 2010 [11]. ISFET integration has also been used as chemical imaging devices that can spatially determine the ionic concentration of specific ions over time [12].

The following properties are what make the ISFET a valuable addition to the poten-

Figure 1.4: Honeywell Durafet pH measurement product line.

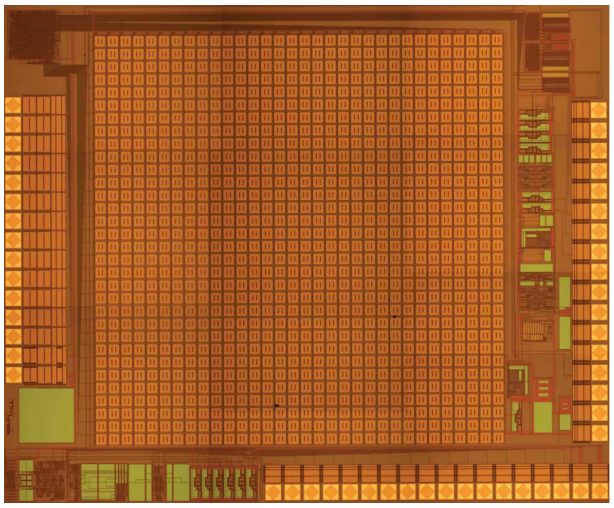


Figure 1.5: A 32x32 ISFET sensing array that can be used for chemical imaging or DNA sequencing [13]

tiometric chemical sensor family:

- Measurement of ion activity/potentials into aqueous and solid environments
- Probe ion concentration/potentials from small volumes
- High frequency of operation
- Compatibility with microelectronics processing technology allows large-scale and lab-in-a-chip applications

The latter properties were inherited from the MOSFET technology maturity and completely revolutionized chemical sensing.

It has been 40 years since Bergveld introduced the ISFET to the world and research keeps going strong. The search for new CHEMFETs and BIOFETs continues with sensors

produced with novel materials (Graphene [14], Semiconducting Nanowires [15]) along with further developments of ISFET array architectures and measuring instrumentation [16], which aim to increase the overall signal to noise ratio and produce faster and cheaper electrolyte imagers and DNA sequencers.

Chapter 2

Objectives

Develop the knowledge to design, fabricate, encapsulate and characterize ISFET sensors at UFRGS microelectronics laboratory. Design consists of choosing device‘s size and form compatible with the equipment and encapsulation technology available. Microfabrication is likely the most time consuming part of the project and will be done with a MOS recipe tuned to accommodate new materials and achieve higher resolution and sensitivity for the sensors. Encapsulation was one of the greatest barriers historically for the development of the technology and it encompasses wire bonding, probe design , device protection and isolation from the aqueous and variable pH environments where it operates. MOSFETs and ISFETs will be fabricated alongside and both will be electrically characterized. Development of an experiment to test and use ISFET sensors. By the end of this study, we hope to provide the local scientific and industrial community with a solid foundation to do further research and development with ion sensors.

Chapter 3

Fundamentals

The ISFET is a solid state device fabricated and designed with technology derived from conventional CMOS processes used in the fabrication of MOSFET transistors. It also is a chemical sensor of ionic activity in electrolytes. It is a transducer of chemical information from electrolytes into electrical parameters of solid-state devices. Therefore, electrochemistry and solid-state physics knowledge are necessary to understand the science of ISFET design and use. We begin with a rigorous definition of pH and activity followed by an introduction to potentiometric sensors in general. The main concepts from MOSFET technology and characterization are then outlined before a thorough description of the ISFET technology and its theoretical fundamentals.

3.1 pH and ionic activity

At the introductory part of this work, a simplified definition of pH was given (1.1), relating it to the logarithmic of the concentration of H^+ ions in an aqueous solution. A more rigorous definition of pH relates it to the ionic activity a_H of H^+ as in (3.1) [17]. The ionic activity of an species a_X is related to its molar concentration [X] by (3.2) [17], where γ_X is a dimensionless quantity called the ionic coefficient. The ionic coefficient is a dimensionless quantity which varies between 0 and 1[1] and takes into account the complicated interaction between neighboring ionic species inside the solution.

The activity may be thought as a measure of effectiveness with which a species influences an equilibrium in which it is a participant. For dilute solutions, the ionic species are

[1]There are special cases where it can be even greater than 1. This happens for solutions which have an extremely high concentration of ionic species.

far apart and practically do not interact and the effectiveness of an ion on the position of equilibrium becomes dependent only on its molar concentration and independent of other ions. Under these conditions, the activity coefficient becomes unity and $a_X = [X]$. As the amount of ionic species in a solution increases the neighboring ions influence each other behavior and the result is a decrease in effectiveness of the ion in influencing the chemical equilibria. Activity, therefore, becomes lower than molar concentration.

This effect that decreases the "effective concentration" is more pronounced for species that carry more electrical charge. Figure 3.1 shows the activity coefficient for species with different charges as a function of the number of ions in the solution. For neutral species, the activity coefficient is approximately 1 regardless of the concentration of ions in the solution. There are methods to model and calculate γ, but for the understanding of this study, these qualitative notions should suffice.

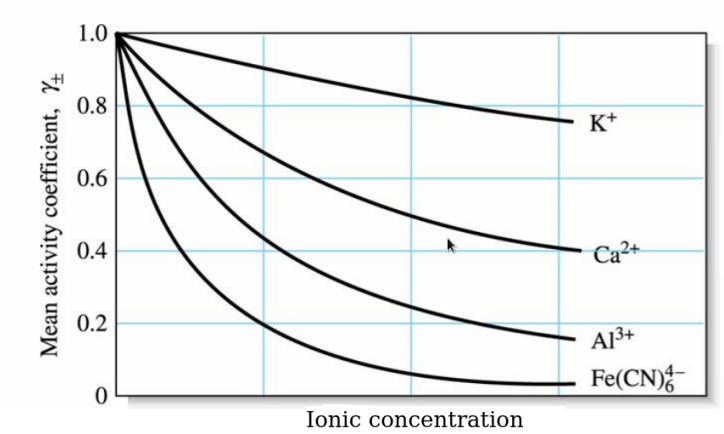


Figure 3.1: Activity coefficient dependence with the respective ion‘s charge. Figure adapted from [17].

$$pH = -\log a_H \tag{3.1}$$

$$a_X = \gamma_X [X] \tag{3.2}$$

The pH is, therefore, a dimensionless quantity that is directly related to the activity of Hydrogen, a measure of its effective concentration as a participant into equilibrium relationships. These concepts are not confined to the sole measurement of Hydrogen ions and one can talk about Calcium, Sodium or X in terms of pCa, pK or pX.

The definition of pH is intimately tied to the development of electrochemical measure-

ment methods in general. To provide some context to the discussion we should talk about the measurement of electrical potentials in solutions, potentiometry and its applications to the measurement of ionic activities.

3.2 Potentiometric Sensors

The majority of ion sensors are potentiometric. They are used on potentiometric methods which rely on the measurement of electrochemical cell potentials in absence of appreciable currents. The equipment is relatively simple and includes a reference electrode, an indicator electrode and a potential measuring device between the electrodes as illustrated in Figure 3.2 . More complex potentiometric experiments extend the setup with a number of auxiliary electrode and voltmeters.

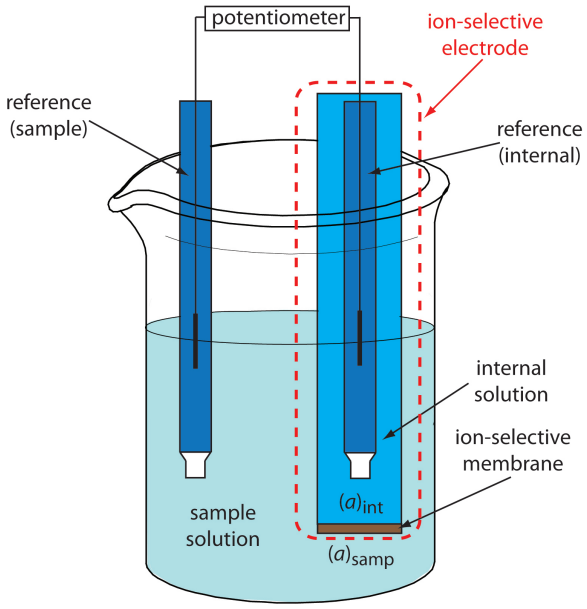


Figure 3.2: A basic electrochemical cell for potentiometric measurements. Figure from [18].

In potentiometry and electrochemistry in general, one is usually interested in the reactions and potential changes of the indicator electrode. To focus on that, the other half of the cell is called the reference electrode and is made up of phases of essentially constant composition and consequently constant voltage differences.

The electric potential can give information about several chemical parameters (activities, reaction rate, reaction constants) from an electrochemical system. In this context, potentials differences are established between solid and liquid interfaces, liquid junctions,

and between electrodes. Thermodynamics links the electrical and chemical worlds. Potential differences are related to free energy changes in the electrochemical system. For ion sensors this linkage is given by the Nernst Equation (3.3), named after the German scientist and Nobel prize winner Walther Nernst[17]:

$$E_{cell} = E^0_{cell} + \frac{RT}{nF} \ln Q \tag{3.3}$$

Where R is the gas constant (8.316 J mol^{-1} K^{-1}); T is the temperature in kelvins; F is the Faraday constant (96485.33289 C mol^{-1});n is the molar concentration; E^0_{cell} is the cell electric potential in equilibrium in and Q is the thermodynamic reaction quotient. E^0_{cell} is a constant which depends on the pair of electrodes used, it is tabulated and cited with respect to the Standard Hydrogen Electrode (SHE). Q is a dynamic version of the equilibrium constant (K), when the reaction reaches thermodynamic equilibrium $Q = K$, $E^0_{cell} = \frac{RT}{nF} \ln K$ and $E_{cell} = 0$. For a generic reaction[17]:

$$xX + bB \rightleftharpoons cC + dD$$

For the above reaction Q is given by (3.4). The activities are raised to the coefficient of the species, indicated by the lower case letters[17].

$$Q = \frac{a^x_X a^b_B}{a^c_C a^d_D} \tag{3.4}$$

Therefore, the Nernst equation gives a function between measured potential and ionic activities. Evaluating the constants and parameters at standard conditions ($T = 273K$, $n = 1M$) and changing the logarithm base from e to 10 the Nernst equation takes the form at (3.5). There is a maximum change of 59mV per logarithmic unit of Q at room temperature, that is called the Nernstian limit[17].

$$E_{cell} = E^0_{cell} + 0.059 \log Q \tag{3.5}$$

Now we can apply the Nernst equation to the pH measurement system in Figure 3.2 to relate the Hydrogen activity to the measured electrical potential of the cell. There are three points where voltage builds up in this cell. The first one is the ion selective electrode due to the different activities of H^+ ions on both sides of the glass (E_{glass}). The second source is the silver wire inside the ion selective electrode which is covered with

AgCl and immersed in the chloride solution (E_{AgCl}). The third source is the reference electrode (E_{ref}). For a well-constructed pH meter E_{ref} and E_{AgCl} are constants, therefore independent of the electrolyte. The sum of all these sources gives us the total electric potential of the system (3.6)[17].

$$E = E_{glass} + E_{AgCl} + E_{ref} \tag{3.6}$$

E_{glass} can be connected to the activities of H^+ through Nernst Equation (3.7). The first step is to apply the pH definition to the top equation and then realize that the pH_{inside} term is a constant for pH meters and can be included inside E'_0. The convenience of the pH definition for these calculations is not accidental, the modern definition was adopted due its convenience for these measurement systems[17].

$$\begin{aligned} E_{glass} &= E_0 + 0.059 \log \frac{a_{H^+_{inside}}}{a_{H^+_{outside}}} \\ E_{glass} &= E_0 + 0.059(pH_{outside} - pH_{inside}) \\ E_{glass} &= E'_0 + 0.059 pH_{outside} \end{aligned} \tag{3.7}$$

Substituting the results of (3.7) at (3.6) and sweeping all the constants under E''_0 we obtain (3.8). The Nernstian limit, in this case, translates to a maximum theoretical sensitivity of 59mV/pH at room temperature for the pH meter. This Nernstian limit is independent of the measurement system and is also valid for ISFET sensors.

$$E = E''_0 + 0.059 pH_{outside} \tag{3.8}$$

In summary, the Nernst equation tells us three very important things:

- The potential is a logarithmic function of ionic activities.
- The potential measured is a function of temperature. That is why pH meters package automatic temperature compensating systems.
- The best resolution achievable at room temperature is 59mV/pH, the Nernstian limit.

Potential measurements are always done between two points because only potential differences carry physical meaning. In conventional electrical circuits, all voltages are

cited with respect to ground, which is assumed to have a constant potential arbitrarily defined as 0V. A reliable ground must be able to sink the current from the circuit without changing its potential, therefore it must be a large conductor with negligible resistance. To talk about voltages between an electrode and an electrolyte solution, both must be connected to ground. Grounding an electrolyte with a constant potential drop, while several complex reactions between the chemical compounds and the electrodes happen, is not a trivial task. There exist several reference electrodes that serve this purpose for different electrolytes and their characteristics and consequences for ISFET technology are presented in the next section.

3.2.1 Reference Electrodes

To compare results and give meaning to the electrode potentials, a standard to which all measurements are compared is needed. The electrode potential E_{cell} from Nernst equation (3.3) is cited with respect to the standard hydrogen electrode (SHE). The electrode potentials are defined as cell potentials for a cell consisting of the electrode in question acting as the cathode and the SHE acting as the anode (positive current points out of the SHE). By convention, the SHE potential is assigned the value of 0V for all temperatures. The SHE was widely employed in early electrochemical studies but is very hard to prepare and is rarely used. It would not work as a reference electrode in many cases also because several solutions may react with it and change its potential with relation to ground. Therefore it works as a theoretical 0 to which all practical reference electrodes are cited.

A practical reference electrode is an electrode that has a stable and well-known electrode potential. Ideally, the reference electrode does not react with the electrolyte and should not change its potential regardless of the current going by it. It should present the current-potential characteristic shown in Figure 3.3. In electrochemistry, these I-V curves are usually obtained under steady-state conditions and are called polarization curves. In this terminology, a good reference electrode is nonpolarizable over the region of interest.

Summing it up, a good reference electrode has the following characteristics:

- Exhibits a potential that is constant with time.
- Exhibits little hysteresis with temperature cycling.

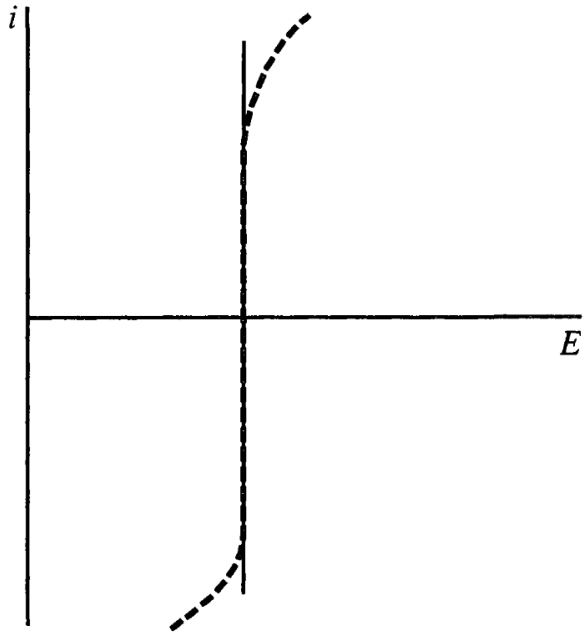


Figure 3.3: Ideal non-polarizable electrode I-V curve. Figure from [19].

- Is reversible and obeys the Nernst equation.
- Returns to its original potential if subjected to small currents.

Of specific interest for ion sensing in aqueous solutions is the Silver/Silver Chloride (Ag/AgCl) electrode. It is the most widely marketed reference electrode and consists of a silver wire coated with a layer of silver chloride. This wire is immersed in a solution of potassium chloride that is saturated with silver chloride. The electrode potential is determined by the half-reaction:

$$AgCl(s) + e^- \rightleftharpoons Ag(s) + Cl^-$$

The connection with the analyze/indicator electrode system is made through a fritted disk or a porous fiber sealed at the end of the outer tubing. This junction has a high resistance (2000 to 3000 Ω) and limits current passage. It also avoids contamination of the analyte solution with the potassium chloride because the leakage is minimal.

A Ag/AgCl electrode is usually employed as the reference electrode for ISFET measurements. The employment of this large reference electrode also leads to trouble when one wants to take advantage of the small size of a solid-state device. The construction of a reliable solid-state reference electrode (REFET) would solve this problem but the implementation of such device is a great challenge. REFETs are still under heavy development

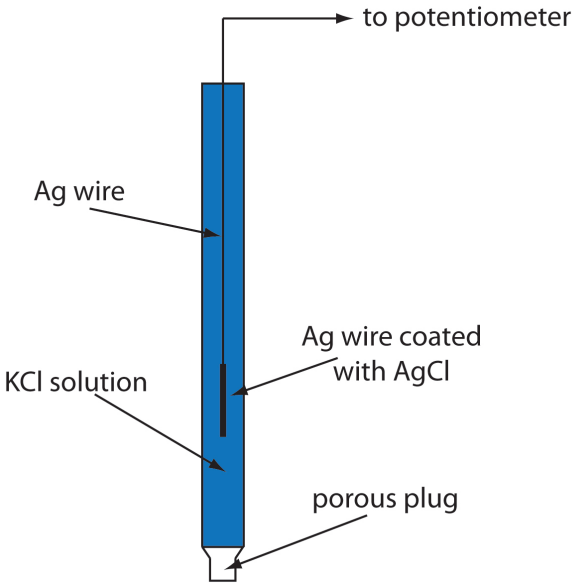


Figure 3.4: Ag/AgCl reference electrode. Figure from [18].

and research and current REFET technologies always present some kind of dependence on the solution pH which has to be artificially removed [16].

This concludes a brief introduction to the electrochemical concepts and technologies needed to understand the ISFET. There is one more topic that has to be covered before we enter into ISFET specifics, the MOSFET technology.

3.3 The MOSFET

A MOSFET is a device with 4 terminals: source, drain, gate, bulk. It is a device which allows very fine control of the current between the source an drain terminals through a region called the channel. They come in two types NMOS and PMOS transistors depending on the channel carrier type. In this study only NMOS transistors were fabricated and characterized, therefore all the fundamentals will be shown for an n-type channel transistor (NMOS).

Figure 3.5 shows the structure of an n-channel MOSFET with all its terminals indicated. Source and bulk are often shorted into what is called the body tie configuration, that is why the bulk connection is not explicitly depicted. Between the source and drain regions a conductive channel of electrons may form and allow current to flow from source to drain. Two very important structural parameters for the MOSFET are related to the channel region, its length (L) and width (W). These parameters impact the resistance of

the channel and therefore the amount of current that flows from the source to the drain terminal[20].

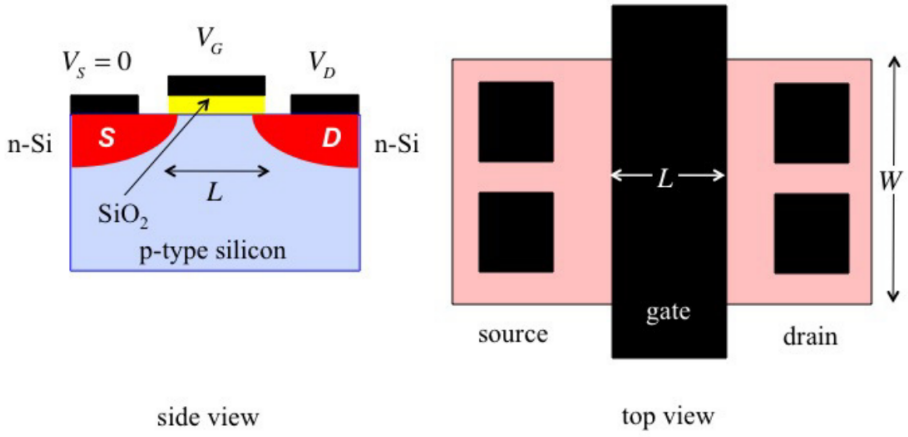


Figure 3.5: Side view (left) and top view (right) of an n-channel MOSFET. Figure from [20].

MOSFET functionality becomes clear by analyzing I-V curves of drain current (I_{DS}) versus drain voltage (V_{DS}) for constant values of gate voltage (V_{GS}) as shown in Figure 3.6. This is called the output characteristic and shows that the MOSFET operates in three regions: subthreshold, linear, and saturation. At the subthreshold region there is no channel formed and at the saturation region the channel has reached its maximum conductivity. At the linear region the MOSFET operates as a voltage controlled resistor and this is the region ISFET devices operate. The drain current at the linear region is given by equation (3.9) where V_{GS} is the gate-source voltage; V_{DS} is the drain-source voltage; μ_{eff} is the effective electron mobility in the channel; C_{ox} is the gate dielectric capacitance; W and L are respectively the width and the length of the channel and V_t is the threshold voltage[21].

$$I_{DS} = \mu_{eff} C_{ox} \frac{W}{L} [(V_{GS} - V_t)V_{DS} - \frac{1}{2}V_{DS}^2] \tag{3.9}$$

The transition between the high-resistance subthreshold region to the linear region happens when $V_{GS} > V_t$. V_t is the necessary voltage drop between the gate and the silicon channel to significantly invert the majority carrier type at the silicon surface and form a conducting channel between the source and drain connections. It is calculated with the use of equation (3.10)[21].

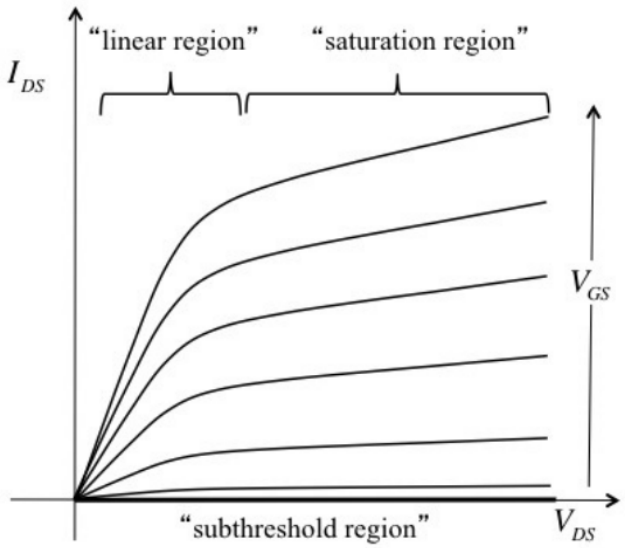


Figure 3.6: OUutput I-V characteristic curve of an n-channel MOSFET in body tie. The Vertical axis is the current that flows between the drain and source, I_{DS}.The horizontal axis represents the voltage between source and drain, V_{DS} Each curve corresponds to a different gate voltage, V_{GS}. Figure from [20].

$$V_t = \frac{\Phi_M - \Phi_{Si}}{q} - \frac{Q_{ox} + Q_{ss} + Q_B}{C_{ox}} + 2\phi_f \tag{3.10}$$

The first term at eq. (3.10) represents the workfunction difference between the metal gate (Φ_M) and silicon (Φ_{Si}), the second term contains the voltage due to the accumulated charges in the oxide (Q_{ox}), at the silicon-oxide interface (Q_{ss}) and the depletion layer in the silicon (Q_B). ϕ_f is the potential difference between the Fermi levels of doped and intrinsic silicon. The last term, $2\phi_f$, defines when strong inversion occurs on the Si/SiO_2 interface layer and depends on silicon doping level.

The definition of V_t experimentally is not as precise. It is the gate voltage at which 'significant' drain current begins to flow, and there are many ways to specify that. We extract V_t from the transfer characteristics curve: I_{DS} vs V_{GS} at constant V_{DS} (Fig. 3.7). This is performed by fitting a line to the I-V characteristic linear part. The line intercepts the V_{GS} axis approximately at the V_t value and its slope provides the transconductance parameter g_m, which is dI_{DS}/dV_{GS} for a fixed drain voltage. The choice of the fixed V_{DS} value may bias the transistor into saturation or linear region and this greatly impacts the result of the analysis. Consistency is due and all the transfer characteristics were traced

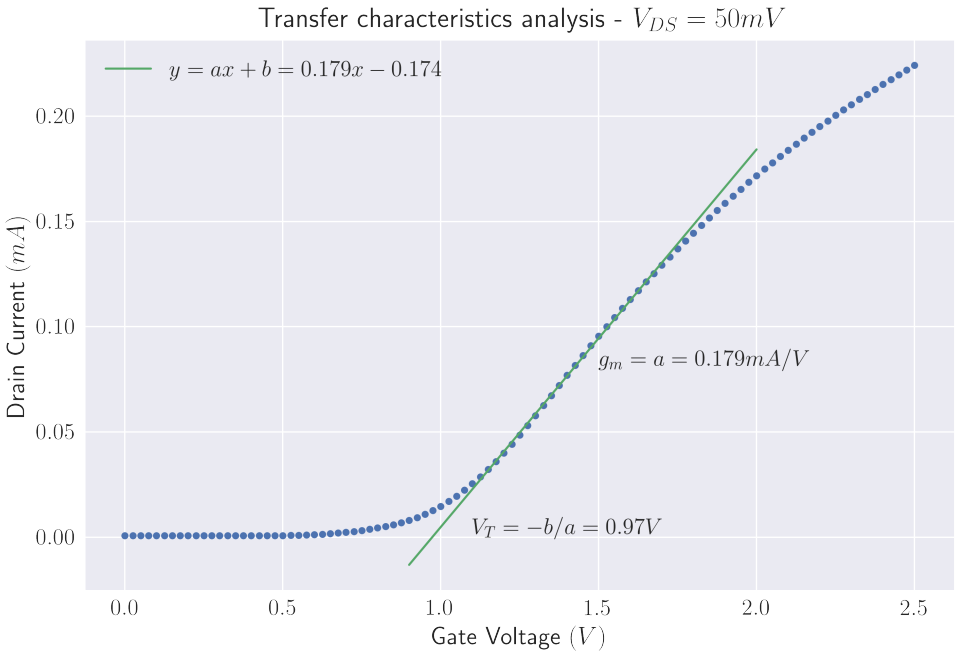


Figure 3.7: Extraction of V_t and g_m from the transfer characteristics curve. Blue dots represent data from one of our transistors. V_{DS} of 50mV places this transistor into linear operation region. All the parameter extraction was performed with the transistor in the linear region.

with the transistor operating in the linear region, with a low V_{DS} value.

Another important parameter for the understanding and characterization of the carrier transport in the MOSFET is the effective mobility (μ_{eff}) of the channel. In the bulk of semiconductors, mobility is dependent on two types of scatterings: lattice scattering and impurities scattering. In a MOSFET, the carrier motion is restricted to the very thin inversion layer between the oxide interface and the bulk. The carriers bounce between the bulk and the oxide, effectively reducing the carriers mobility. It is a difficult effect to predict theoretically and it is usually determined experimentally through equation (3.11), where g_m is extracted from the transfer characteristics and is tied to a V_{DS} value [21].

$$\mu_{eff} = \frac{g_m L}{C_{ox} V_{DS} W} \tag{3.11}$$

The only parameter from equations (3.9) and (3.11) whose experimental characterization has not been shown is C_{ox}. The measurement of C_{ox} is done through Capacitance-Voltage experiments and is explored in the next section.

3.3.1 Capacitance-Voltage Measurements

The MOS capacitor (Fig. 3.8) is a device of fundamental importance to characterize a given fabrication technology. The physics of a MOS capacitor is very rich and so is its characterization. The purpose of this section is to give a brief introduction on MOS capacitor measurement and show how we extracted information from the C-V experiments.

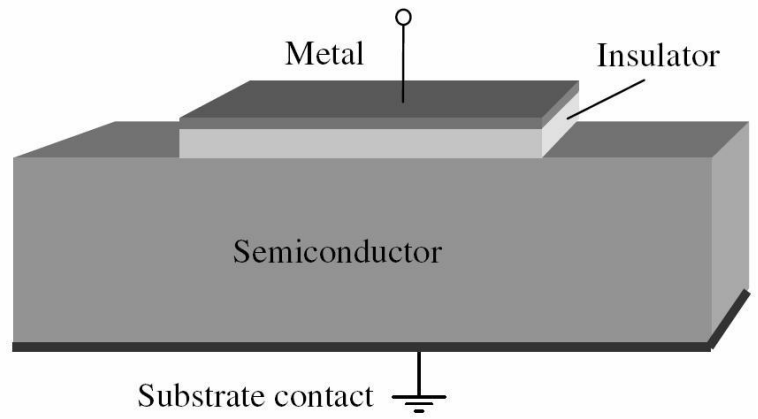


Figure 3.8: The MOS Capacitor.

The MOS structure explored in this study is formed by aluminum, an oxide (silicon dioxide and/or alumina) and P-type silicon. A generic high-frequency C-V curve for this case is illustrated in Figure 3.9. C-V measurements are done with the use of an electronic bridge. The bridge supplies a DC gate voltage (x-axis on Fig. 3.9) superimposed with an AC voltage of a few mV at a chosen frequency. The DC voltage biases the substrate into accumulation, depletion or strong inversion and the AC voltage is used to perform the capacitance measurement($dC = dQ/dV$). The AC signal frequency is considered high when it is too fast for the minority carriers generation respond to it, hundreds of kHz for p-type silicon.

The gate voltage applied is balanced by a voltage drop in the oxide and silicon surface. The total capacitance of the MOS structure is given by the series association of the oxide and silicon capacitances (3.13). The oxide capacitance is a constant which depends on the oxide thickness (t_{ox}), its dielectric constant (ε_{ox}) and the capacitor area (A) as given by (3.12). The silicon capacitance is more complex and depends on DC bias and the AC frequency. The dynamics of charge distribution on the silicon side are responsible for the accumulation, depletion and strong inversion regions in Figure 3.9.

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} A \tag{3.12}$$

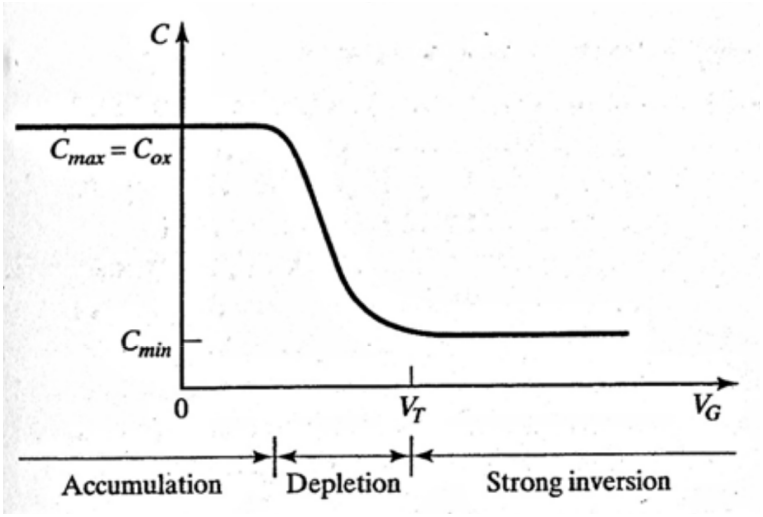


Figure 3.9: Capacitance-Voltage characteristics of an NMOS capacitor. Figure from [21].

$$\frac{1}{C} = \frac{1}{C_{ox}} + \frac{1}{C_{Si}} \tag{3.13}$$

For a negative bias applied, the silicon surface has an accumulation of holes, the majority carriers of a P substrate. The silicon capacitance is very high in this case because the holes are distributed into a very thin region close to the silicon/oxide interface and, as majority carriers, respond very quickly[2] to the AC signal. The total capacitance (3.13) reduces to C_{ox} and this is how C_{ox} is extracted[22].

As the gate voltage increases holes are driven away from the semiconductor interface and a depletion region made up of negatively charged acceptor atoms forms in the semiconductor surface. The depletion region depends only on majority carrier movement and therefore also responds to the AC signal. The width of the region increases with the square root of the surface potential, effectively decreasing the silicon capacitance. The lower silicon capacitance decreases the total capacitance (3.13) as can be seem at the depletion region in Figure 3.9.

When the gate voltage surpasses the V_t value, a thin inversion layer of minority carriers whose density depends exponentially on the surface potential forms at the surface. The exponential dependence causes this surface layer to absorb all subsequent voltage increase,

[2]The relaxation time of majority carriers is given bye the ration between the dielectric constant and the conductivity. For silicon having a resistivity of 1 ohm-cm this time is of the order of $\times 10^{-12}$ [21]

halting the depletion layer to a maximum width and minimum capacitance. For high frequencies, the very thin minority carriers layers does not respond to the AC signal and the silicon capacitance is constant and equal to the depletion layer minimum capacitance. The total capacitance stays at its minimum value at the inversion region for high AC frequencies. For low frequency measurements the thin inversion layer has a very high capacitance and the capacitance goes back to its maximum value C_{ox}.

Through the quantitative treatment of this process it is possible to extract the following key parameters listed at table 3.1.

Table 3.1: Main parameters extracted by C-V measurement

Oxide capacitance	C_{ox}	Fcm^{-2}
Flatband capacitance	C_{FB}	Fcm^{-2}
Effective charge	Q_{eff}	cm^{-2}
Threshold voltage	V_t	V

The parameter extraction begins with the determination of C_{ox} as the maximum capacitance measured at the accumulation region. The capacitor area (A) and dielectric constant are known and t_{ox} is calculated from (3.14)

$$t_{ox} = \frac{\varepsilon_0 \varepsilon_{ox} A}{C_{ox}} \tag{3.14}$$

The minimum capacitance value is then used to calculate W_{dm} through (3.15)[22].

$$W_{dm} = A\varepsilon_{Si}\left(\frac{C_{max} - C_{min}}{C_{max} C_{min}}\right) \tag{3.15}$$

The bulk carrier concentration N_A is numerically calculated through iterations of (3.16). n_i is the intrinsic carrier concentration on silicon and is typically $10^{10} cm^{-3}$. Several iterations are necessary because of the linear and logarithmic dependence on the equation[22].

$$N_A = \frac{4\varepsilon_{Si}}{qW_{dm}^2} \frac{kT}{q} \ln \frac{N_A}{n_i} \tag{3.16}$$

The next step is to calculate the flatband capacitance C_{FB} through equation (3.17)[22].

$$C_{FB} = \frac{\varepsilon_{ox}}{t_{ox} + \frac{\varepsilon_{ox}}{\varepsilon_0}\sqrt{\frac{kT\varepsilon_{Si}}{q^2 N_A}}} \tag{3.17}$$

V_{FB} is found by looking up at the C-V plot for the respective voltage value for C_{FB}. The effective charge in the oxide is then calculated by (3.18), where $\Phi_{ms} = \Phi_M - \Phi_{Si}$.

$$Q_{eff} = (\Phi_{ms} - V_{FB})\frac{\varepsilon_{ox}}{t_{ox}} \tag{3.18}$$

Finally, to calculate V_t from (3.10) we still need ϕ_f, which is given by (3.19)[22].

$$\phi_f = \frac{kT}{q} \ln \frac{N_A}{n_i} \tag{3.19}$$

The derivation of all these equations require a thorough semiconductor physics introduction as given by [23] or [21]. The equations in this particular form were taken from [22].

3.4 The ISFET

The ISFET is a very special kind of potentiometric sensor. Differently from the glass pH eletrode it relies on the field effect from transistors to detect charged species in the solution. The ISFET is a MOSFET whose gate connection is separated from the chip in the form of a reference electrode inserted in an aqueous solution which is in contact with the gate oxide (Figure 1.2).

The general equation (3.9) for the MOSFET drain current in the linear region also applies to the ISFET. With the lack of a metal gate, the equation (3.9) is adapted for the ISFET case with the inclusion of the constant potential of the reference electrode (E_{ref}) and the interfacial potential $\psi_0 - \chi^{sol}$ at the solution/oxide interface [24]. ψ_0 is the chemical parameter that changes with the solution pH and χ^{sol} is the surface dipole potential of the solvent and has a constant value. Taking these new terms into account, the Vt of the ISFET is given by (3.20) and the adapted I_{DS} current by (3.21). The resulting ISFET I-V curves are identical those from the MOSFET. The effect of pH and E_{ref} on the ISFET are similar to the effect of V_{GS} for the MOSFET[24]:

$$V_t = E_{ref} - \psi_0 + \chi^{sol} - \frac{\Phi_{Si}}{q} - \frac{Q_{ox} + Q_{ss} + Q_B}{C_{ox}} + 2\phi_f \tag{3.20}$$

$$I_{DS} = \mu C_{ox} \frac{W}{L} \{[V_{GS} - (E_{ref} - \psi_0 + \chi^{sol} - \frac{\Phi_{Si}}{q} - \frac{Q_{ox} + Q_{ss} + Q_B}{C_{ox}} + 2\phi_f)]V_{DS} - \frac{1}{2}V_{DS}^2\} \quad (3.21)$$

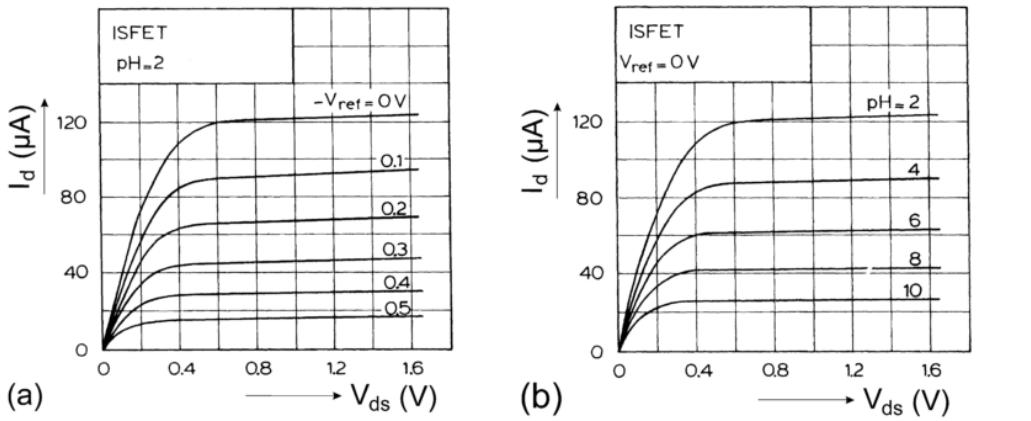


Figure 3.10: ISFET output characteristics varying (a) Reference Electrode Voltage and (b) pH. Figure from [4]

The meaning of the χ^{sol} and ψ_0 and their impact on the ISFET performance and design become clear with the description of the reactions and charge distribution at the oxide/solution interface.

3.4.1 The oxide/electrolyte interface

There are two principle kinds of processes between electrodes and electrolytes: Faradaic and non-faradaic. Faradaic processes allow redox reactions in which electrons are transfered between the electrode and the solution. These reactions follow Faraday‘s law in which the amount of chemical reaction caused by the flow of current is proportional to the amount of electricity passed. Batteries make use of faradaic mechanisms. Non-faradaic processes do not involve charge transfer and are governed by adsorption and desorption of charged species at the electrode surface. The ISFET is a non-faradaic device.

The accumulation of charge between the electrode surface and the solution during a non-faradaic interaction resembles a capacitor. Loosely speaking, one plate represents the electrode and the other the electrolyte and this structure is named the electrical double layer (Figure 3.11). There are several models to describe the electrical double layer structure and there are many models to describe the reactions between the oxide and the electrolyte. The ISFET description given in this section is from [24] and it develops a

general model that accommodates any combination of double layer and reaction models between the gate dielectric and the electrolyte.

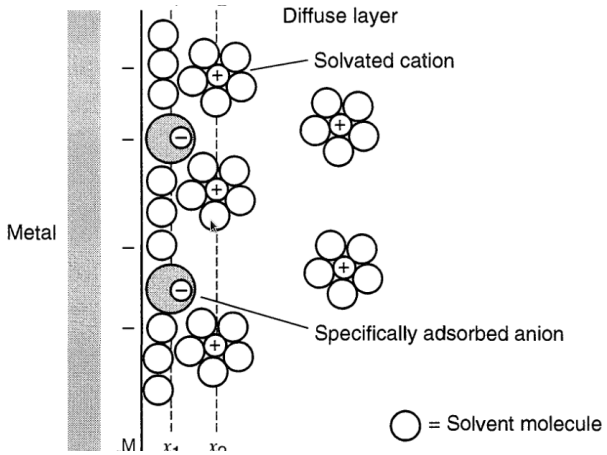


Figure 3.11: A double layer model where the anion becomes specifically adsorbed in a metal electrode. Many models exist to describe different double layer structures between different materials and electrolytes. Figure from [19].

The electrostatic potential ψ_0 introduced in (3.21) is the potential across the double layer structure as illustrated in Figure 3.12. ψ_0 builds up near the oxide surface due to charge accumulation at the oxide surface and the charge accumulates as a result of surface reaction. The model proposed introduces an intrinsic buffer capacity (β_{int}) to describe the adsorption of species at the oxide surface and a differential capacitance (C_{dif}) to describe the charge accumulation through the double layer. This potential difference between the oxide surface and the electrolyte causes a proton activity difference between the solution bulk and surface given by (3.22). Writing (3.22) in terms of pH results in (3.23). The subscripts B and S refer to the bulk and surface of the electrolyte.

$$a_{H_S^+} = a_{H_B^+} \exp \frac{-q\psi_0}{kT} \tag{3.22}$$

$$pH_S = pH_B + \frac{q\psi_0}{kT} \tag{3.23}$$

The intrinsic buffer capacity represents the ability of the surface to store charge due to a small change in the solutions' pH at the surface's vicinity and is given by (3.24) where σ_0 is the surface charge density.

$$\frac{\partial \sigma_0}{\partial pH_S} = -q\beta_{int} \tag{3.24}$$

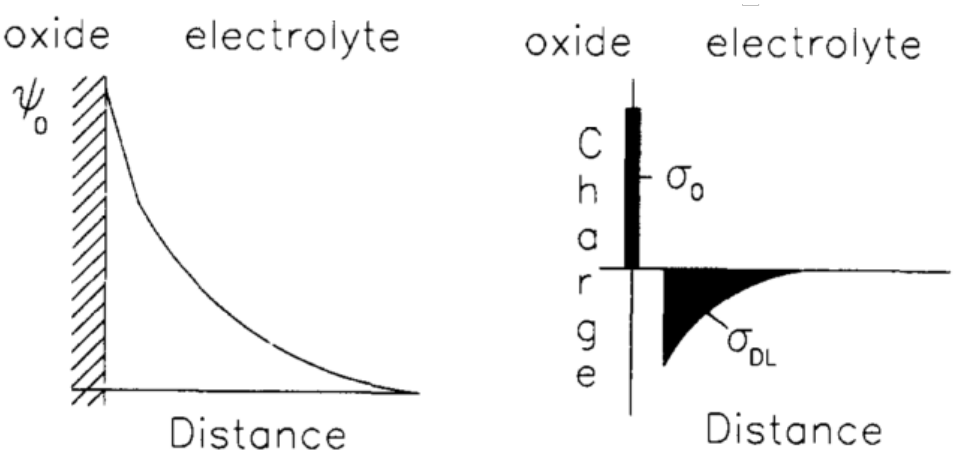


Figure 3.12: Potential ψ_0 profile on the left and charge distribution at an oxide electrolyte solution interface. Figure adapted from [24].

The differential capacitance (3.25) represents the ability of the electrolyte solution to adjust the amount of stored charge due to a small change in the electrostatic potential

$$\frac{\partial \sigma_{DL}}{\partial \psi_0} = -\frac{\sigma_0}{\partial \psi_0} = -C_{dif} \tag{3.25}$$

Combining both definitions it is possible to write the dependence of the electrostatic potential with respect to changes in the pH at the solution's surface (3.26). The goal of the following developments is to write ψ_0 in terms of pH changes in the bulk (pH_B).

$$\frac{\partial \psi_0}{\partial pH_S} = \frac{\partial \psi_0}{\partial \sigma_0}\frac{\partial \sigma_0}{\partial pH_S} = \frac{-q\beta_{int}}{C_{dif}} \tag{3.26}$$

Combining (3.26) with (3.23) the dependence with pH_B into the equation is included.

$$\frac{\partial \psi_0}{\partial (pH_B + \frac{q\psi_0}{kT})} = \frac{-q\beta_{int}}{C_{dif}} \tag{3.27}$$

Rearranging (3.27) a general expression for the sensitivity of the electrostatic potential to changes in the bulk pH is achieved (3.28).

$$\frac{\partial \psi_0}{\partial pH_B} = -2.3\frac{kT}{q}\alpha \tag{3.28}$$

Where α is given by:

$$\alpha = \frac{1}{\frac{2.3kTC_{dif}}{q^2\beta_{int}} + 1} \tag{3.29}$$

α is the sensitivity parameter and is dimensionless. The value of α varies between 0 and 1 depending on β_{int} and C_{dif} and approaches 1 for a sensitivity close to the theoretical maximum (59mV at standard conditions). For that to happen, the intrinsic buffer capacity should be much higher than the differential capacitance. This is intuitive, with higher β_{int} more charge is "buffered" into the oxide surface due to a pH change. The lower C_{dif} is the greater is the electrostatic potential response due to these "buffered" charges. The transistor is sensitive to ψ_0 and a higher change in ψ_0 due to a pH variation means a more sensitive pH sensor.

β_{int} and C_{dif} are the two key parameters on this description of the potential drop through the double layer structure and these parameters can be calculated through different models. A combination of models that gives a good agreement with experimental data is presented in the next section.

3.4.2 The intrinsic buffer capacity and the double-layer capacitance

The site-binding model introduced at [25] can be applied to describe the charging mechanism of the oxide side of the double layer and be used to predict values for β_{int} [24]. The model has the following features:

- Interactions take place at specific sites
- Interactions can be described via mass law equations
- Surface charge results from these interactions

The surface of metal-oxides contains hydroxyl groups: SiO_2, for example, contains SiOH groups. These surface molecules may donate or accept protons from the electrolyte and become either a negatively or positively charged surface site, as illustrated in Figure 3.13.

The surface reactions are, therefore

$$AOH \rightleftharpoons AO^- + H_B^+$$
$$AOH_2^+ \rightleftharpoons AOH + H_B^+$$

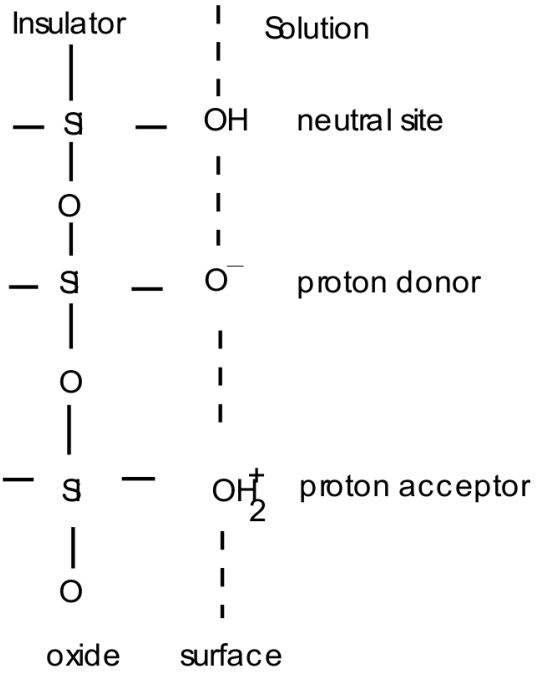


Figure 3.13: Site binding model schematics.

where A represents the metallic atom and B the bulk of the solution. The equilibrium conditions for this set of reactions are given by (3.30).

$$K_a = \frac{\nu_{AO^-} a_{H_s^+}}{\nu_{AOH}} \text{ and } K_b = \frac{\nu_{AOH} a_{H_s^+}}{\nu_{AOH_2^+}} \tag{3.30}$$

where K are the dissociation constants, ν the number of sites per unit area and $a_{H_S^+}$ is the activity of H^+ at the oxide surface. The surface charge density σ_0, introduced at (3.24), is calculated by (3.31) where N_s is the number of sites per unit area and Θ^+ and Θ^- are the fractions of N_s positively or negatively charged with AOH_2^+ AO^-, respectively. The Θ fractions can be calculated by the equilibrium reactions and substituted into (3.31) giving (3.32).

$$\sigma_0 = q(\nu_{AOH_2^+} - \nu_{AO^-}) = qN_s(\Theta^+ - \Theta^-) \tag{3.31}$$

$$\sigma_0 = qN_s \frac{a_{H_S^+}^2 - K_a K_b}{K_a K_b + K_b a_{H_S^+} + a_{H_S^+}^2} \tag{3.32}$$

Taking the partial derivative of (3.32) with respect to pH_S we arrive at the expression for the buffer capacity (3.33). All oxides whose charging mechanism are described by

association and dissociation of an amphoteric[3] group can be described by (3.33).

$$\beta_{int} = 2.3 a_{H_S^+} N_S \frac{K_b a_{H_S^+}^2 + 4 K_a K_b a_{H_S^+} + K_a K_b^2}{(K_a K_b + K_b a_{H_S^+} + a_{H_S^+}^2)^2} \tag{3.33}$$

The values of K_a, K_b and N_s are oxide dependent. The point at which the positive and negative groups are equal and the surface is electrically neutral is called the point of zero charge (pH_{pzc}) and is also an important characteristic of the oxide. Table 3.2 lists values for SiO_2 and Al_2O_3 taken from [26].

Table 3.2: Literature values for the oxide constants from (3.33)

	pK_a	pK_b	N_s	pH_{pzc}
SiO_2	6	-2	5×10^{18}	2
Al_2O_3	10	6	8×10^{18}	8

The charge on the oxide surface is balanced by the charge in the solution side of the double-layer structure. The ions in the solution are electrically attracted to the charged oxide surface but their attraction is countered by the random thermal motion which acts to equalize the concentrations in the solution.

The Gouy-Chapman-Stern theory is widely applied in colloid science to describe the charging of a double layer structure and provides a mean to calculate C_{dif}. The model breaks up the double-layer into two layers, the Stern layer and the diffuse layer. The total capacitance is given by the series association of each of the layers‘ capacitance. The Stern correction to the Gouy-Chapman removes the treatment of the ions as point charges and includes a limiting distance to which they can approach the oxide surface. The model is thoroughly described at [19] and concludes that the inverse of C_{dif} is given by (3.34), where x_2 is the distance of the Stern layer, ϕ_2 is the potential at x_2n n^0 is the concentration of each ion in the bulk, z is the charge of these ions. The first part of (3.25) is the contribution of the Stern layer and the latter the capacitance of the diffuse layer.

$$\frac{1}{C_{dif}} = \frac{x_2}{\epsilon\epsilon_0} + \frac{1}{(\frac{2\epsilon\epsilon_0 z^2 q^2 n^0}{kT})^{1/2} \cosh(\frac{zq\phi_2}{2kT})} \tag{3.34}$$

Figure 3.14 shows the predicted values of β_{int} and C_{dif} and Figure 3.15 the sensitivity parameter α for Silica and Alumina as a function of $\Delta pH = pH_B - pH_{pzc}$. These values

[3]amphoteric groups can either donate or accept protons H^+.

were calculated using a Stern capacitance of $0.2F.m^{-2}$ and the oxide constants at 3.2. By looking at 3.14 it becomes clear that Alumina has a much higher β_{int} than Silica and that both oxides perform similarly when it comes to C_{dif}. Therefore, the large difference between the sensitivity of the oxides displayed at 3.15 is due to β_{int} and Al_2O_3 has a much higher capacity of accumulating charges at its surface than SiO_2.

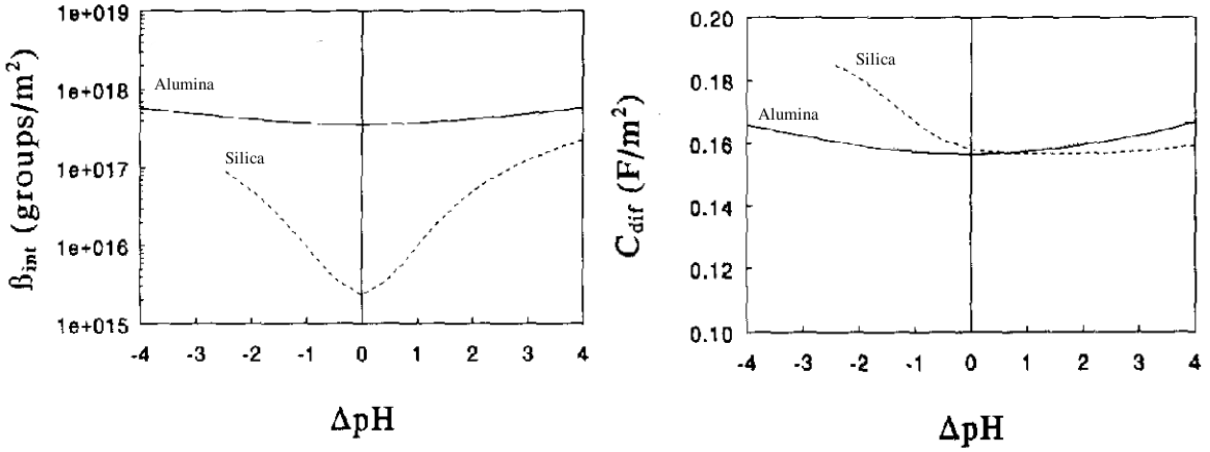


Figure 3.14: Predicted values for the intrinsic buffer capacity (left) and differential capacitance as a function of $\Delta pH = pH_B - pH_{pzc}$ for SiO_2 and Al_2O_3. Figure adapted from [27]

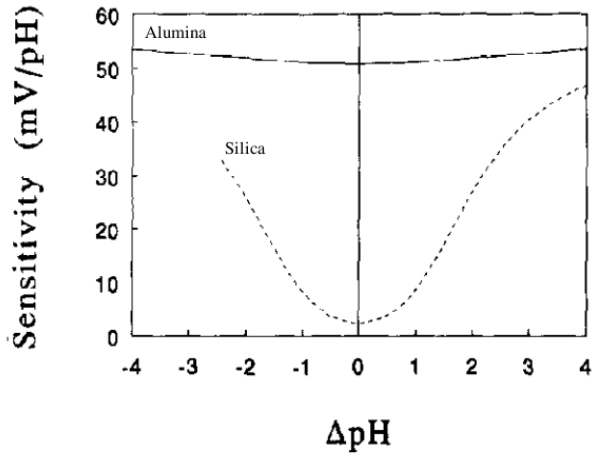


Figure 3.15: Sensitivity parameter α for SiO_2 and Al_2O_3. Figure adapted from [27]

Chapter 4

Methodology

Fabrication was performed inside the clean room facilities of UFRGS microelectronics laboratory (Fig. 4.1). The clean room had temperature, humidity and particles control. All chemical procedures used microelectronics grade chemicals and were performed inside a laminar flow fume hood.

Figure 4.1: Clean room at UFRGS microelectronics laboratory..

4.1 Mask fabrication

Masks designed with Layout Editor Software[28] served as the input to pattern the photoresist with Heidelberg μpG 101 Tabletop Micropattern Generator (Fig 4.2). The patterning was done on a stack of glass/chromium/photoresist. The drawing was made upon

the photoresist with the laser writer and the exposed chromium was removed with a Cerium etch solution.

Figure 4.2: Heidelberg μpG 101 Tabletop Micropattern Generator.

The mask production requires the tweak of several parameters within the micropattern generator. Most notably, the focus and energy of the laser that has to be adjusted for different photoresist type and thickness. For the setup employed on μpG 101 the minimum line size drawable is around 1μm. This is an important design parameter and ultimately limited the size of structures we could draw.

4.2 Cleaning

Standard RCA cleaning, piranha and some other cleaning solutions were employed during the wafer processing. It is fundamental to remove particles, organic and ionic contaminants from the wafers before high temperature processes. Deionized (D.I.) water was used throughout the cleaning and each step was followed by 5 minutes of D.I. water washing. Samples were dried with N_2 gas.

The process of RCA cleaning used was:

- RCA 1 - 4 H_2O(DI) :1 ammonium hydroxide (NH_4OH):1 hydrogen peroxide (H_2O_2), T = 80°C, 10 minutes. Organic residue and particle removal.
- RCA 2 - 4 H_2O(DI):1 hydrochloric acid (HCL):1H_2O_2, T = 80°C, 10 minutes. Metallic ions removal.

Often, a piranha solution for heavy organic removal was employed before the RCA cleaning procedure. The piranha cleaning recipe used was:

- PIRANHA - 4 sulfuric acid (H_2SO_4): 1 H_2O_2, T = 120°C, 10 minutes

Boiling acetone followed by propanol and water cleaning was employed for photoresist removal. Thrichloroetilene cleaning was used before the aluminum syntering step. Temperatures were controlled with the use of a hot plate.

4.3 Thermal oxidation and treatments

The growth of high quality SiO_2 and many thermal treatments required high temperatures at controlled atmospheres containing the desired reactants or inert gases. For these processes we used the horizontal furnace (Figure 4.3) consisting of a quartz tube fed by a constant gas laminar flow of 1L/s. The temperature was controlled through a PID system that guarantees temperatures within 1 °C of precision. High purity N_2, O_2, Argon and Forming Gas (90% N_2, 10% H_2) were employed.

Figure 4.3: Furnaces used for thermal treatments.

4.4 Photolithography

Photolithography is the micro-patterning of complex structures in photoresist which are then transfered to the chip. The recipe below was used for most photolithography steps

and requires a hot-plate, regular spinners and an exposure machine.

- Photoresist: AZ1512.
- Spin coating: 4000 RPM for 50s.
- Soft Baking: 90 100°C for 5 minutes.
- Exposure time: 50s.
- Development: 60 seconds at 5 H_2O (DI):1 AZ351.
- Wash: H_2O (DI) for 5 minutes.
- Hard Baking: 100 110°C for 5 minutes.

4.5 Ion implantation

Ion implantation is crucial to control the dopant distributions on the silicon wafer and form the source, drain, channel areas and PN junctions to isolate the devices. All the implantation steps were done at the 500 kV accelerator from UFRGS implantation laboratory (Fig. 4.4).

Figure 4.4: 500kV accelerator for ion implantation

4.6 Aluminum Physical Vapor Deposition

Aluminum was deposited with the use of a Physical Vapor Deposition (PVD) system. On our PVD setup (Fig. 4.5), high purity aluminum ores were placed on top of a tungsten

support connected to a current source. The tungsten heated by high current passage (100A) evaporates the aluminum depositing an aluminum film of a few hundred nanometers on top of the samples. The process was carried out at high vacuum ($\times 10^{-6}$torr) supplied by a mechanical and diffusion pumps.

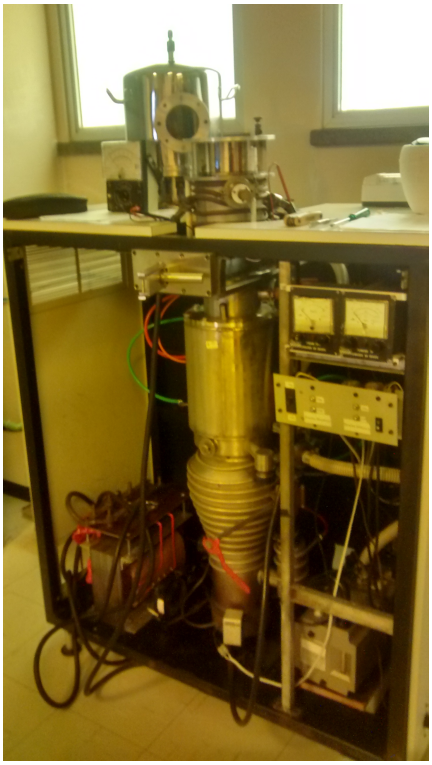


Figure 4.5: PVD system.

4.7 Atomic Layer Deposition of Alumina

Atomic Layer Deposition (ALD) was used to deposit alumina (Al_2O_3) thin films. ALD is very similar to Chemical Vapor Deposition, thin layers of the desired material are formed by a chemical reaction between the precursors gases and the wafer surface, kept at an optimal temperature. The precursors gases are supplied in cycles with just enough material to form a few atomic layers, allowing subnanometric control of film thickness. The ALD system used was a Beneq TFS 200, supplied with a 97% Trimethylaluminium ($Al_2(CH_3)_6$). The wafer was kept at 200°C and the deposition rate was of 0.122nm/cycle.

Figure 4.6: Beneq TFS 200 ALD system.

4.8 Dicing and encapsulation

Dicing was done with a wafer dicer. The individual sensors were glued to a PCB support and pads were manually wired to copper lines with very thin silver wires and silver paste. The silver wires, connection pads, copper connections and silicon side surface were manually covered with an encapsulant resin. We tried photoresist, nail polish and epoxy glue as the encapsulant material and had the best results in terms of electrical isolation and durability with the epoxy glue. The connective tip of the PCB support was left available for electrical measurements.

4.9 Ellipsometry

Ellipsometry was useful to characterize the thickness and dispersion curve of Al_2O_3 thin films. The extinction SOPRA GES-5E ellipsometer (Fig. 4.7) from the Laser and Optics laboratory at UFRGS was used. Measurements were made with an incidence angle *phi* of 75°and at the spectral interval of 350-750nm. With the use of the Winelli II software[29] the dispersion curve of the dielectric could be determined for alumina and its thickness extracted.

4.10 pH meter, reference electrode and buffer solutions

Oakton pH 510 benchtop meter[30] in Figure 4.8 was used to ascertain the pH values solutions used on the tests of the ISFET device. The reference electrode used is a single junction Ag/AgCl electrode with a temperature sensor from Oakton. The system operates at a pH range of 0 to 12 with a resolution of of 0.01 pH.

Figure 4.7: SOPRA GES-5E Ellipsometer at UFRGS Laser and Optics Laboratory.

Figure 4.8: Oakton pH 510 benchtop meter and all in one Ag/AgCl reference electrode packaged along the sensing electrode and temperature sensor.

The following buffer solutions supplied by labsynth[31] were used to calibrate and test the pH meter and the ISFET device:

- pH 4 - Potassium Biphthalate and DI water
- pH 7 - Sodium Hydroxide, Monopotassium phosphate and DI water
- pH 9 - Potassium Chloride solution 0.2M, Boric Acid solution 0.2M, Sodium Hidroxide 0.2M and DI water.

4.11 ISFET measurements

ISFET experiments were performed with the HP-4155A parameter analyzer connected to the PCB probe contacts with the sensor inserted into buffer pH solutions along with the reference electrode as illustrated at Figure 4.9. The sensor pads are connected to the source and drain pads while the reference electrode and the solution represent the gate connection. The electrode used packages a temperature sensor and a sensing electrode along with the Ag/AgCl referece electrode. Only the reference was connected to the parameter analyzer.

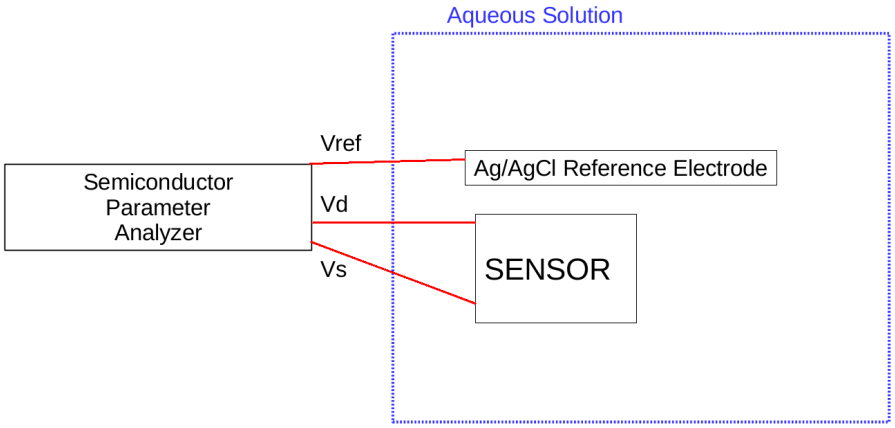


Figure 4.9: Schematic of the ISFET measurement setup. From inside an aqueous solution the reference electrode and the sensor are connected to the HP-4155A parameter analyzer

4.12 C-V and I-V Curves

Capacitance-Voltage (C-V) experiments were performed with the HP-4284 LCR meter (Figure 4.10). The measurements and parameter extraction were done with an automated system controlling the HP-4284 through the VEE Software[32] developed at [33].

Current-Voltage (I-V) Curves were made with the HP-4155A Semiconductor Parameter Analyzer (Fig. 4.11) with the sample and Source Measurement Units (SMUs) placed inside an aluminum box for electromagnetic shielding.

Figure 4.10: HP-4284 used for C-V measurements.

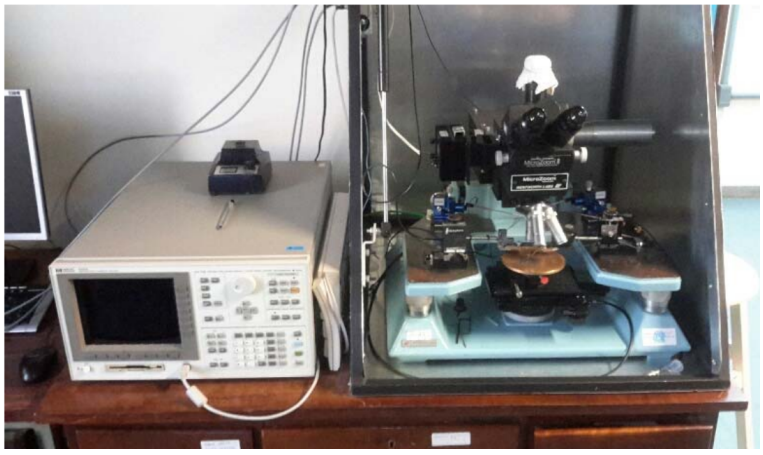


Figure 4.11: HP4155A Parameter Analyzer used for the I-V characterization. At the right the aluminum faraday cage, which provides electromagnetic shielding, encloses the microscope and the support where samples are placed.

Chapter 5

Fabrication

The recipe we applied to ISFET fabrication was adapted from a CMOS recipe previously tested in our lab [34]. Two rounds of fabrication were performed. In the first round we fabricated devices with SiO_2 (50nm) as the gate insulator. In the second round we changed the dielectric to a stack of Al_2O_3 (80nm) and SiO_2 (15nm). The process between rounds remained largely the same. Up to the gate insulator deposition both rounds are identical. This chapter is devoted to explain the details of both rounds of fabrication. The entire process was simulated in 1D with Synopsis Sentaurus CAD software[35]. The simulation was used to observe the impurities concentration profile following annealing and implantation steps at the source and drain regions. The simulation code is available at appendix A.

5.1 Silicon dioxide devices - S1 and S2

In the first fabrication round, NMOS depletion mode devices with 50nm of SiO_2 thermally grown as the ion-sensitive layer were fabricated. They were initially fabricated with a metal gate to allow electrical characterization of each device before removing the metal gate with an additional photolithography. The removal of the gate leaves the SiO_2 layer exposed and transforms the transistors into ISFETs. Two wafers went through this process and their devices are referred as S1 and S2 throughout the text. The second round of fabrication comprised of two wafers whose ion-sensitive layer is of alumina, these are referred as A1 and A2.

The fabrication process has a total of 7 lithography steps (Fig. 5.1) and we designed

the devices to have a channel dimensions W = 1000 μm and L = 10 μm. Devices were fabricated on <100> p-type silicon wafers with boron doping of 1.5×10^{14} cm^{-3} along with a monitoring capacitor of 400μm x 400μm. The process starts with the growth of a thick silicon oxide layer followed by a boron implantation out of the active areas. This ensures low field leakage currents between devices. The first lithography step protects the channel area from this implantation. The second lithography patterns the source and drain for arsenic implantation. After drive-in of arsenic dopants, the third lithography is done to expose the silicon at the channel area. Now the insulator layer, which defines the chemical sensitivity of the device is deposited or grown. We simply grew 50 nm of thermal silicon dioxide. Contact openings are then etched through the fourth lithography step, followed by aluminum deposition. Lithography number 5 forms the metal connections. After electrical characterization of the transistors, an additional lithography is done to remove the metal gate and expose the SiO_2 layer for ion sensing. The last lithography encapsulates everything except the sensing layer and metal pads with photoresist.

An overview of this first round recipe containing all the lithography, implantation and metalization steps is at Table 5.1. Figure 5.1 pictures a single device from each photolithography mask, with positive lithography in red and negative in blue. The final device is illustrated in Fig. 5.2. Each device is 4mm per 5mm and masks are 40mmx40mm with a total of 76 dies per mask.

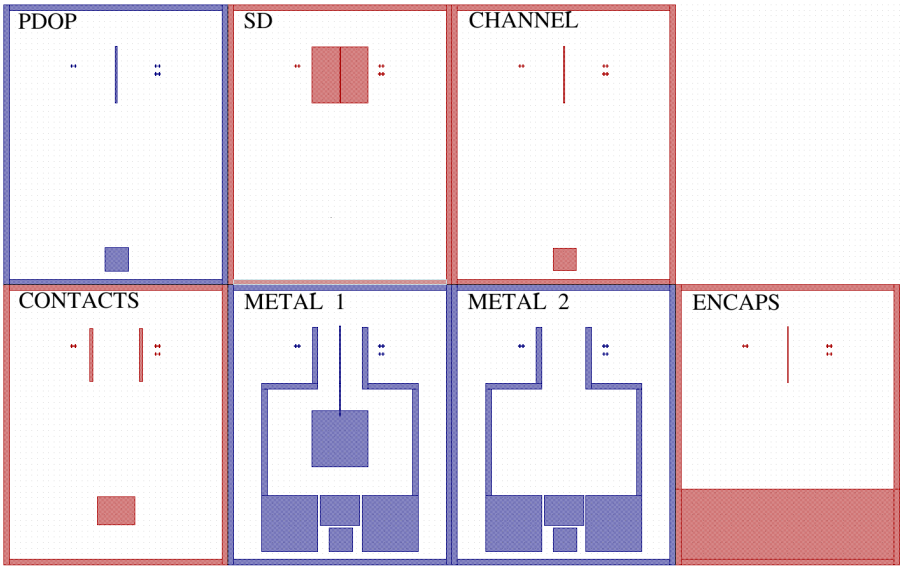


Figure 5.1: A single device from each lithography mask. Red represents positive lithography procedures and blue negative ones. The crosses present in every mask are used as alignment marks.

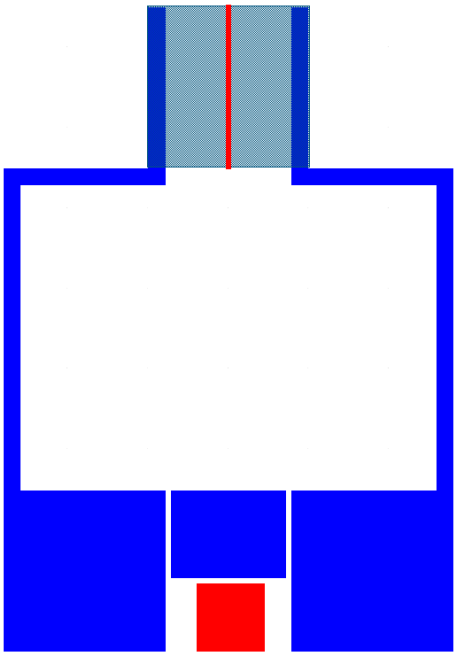


Figure 5.2: Layout of a single ISFET device. It is 4 mm wide and 5 mm tall. The red regions represent the sensing layer (W = 1000 μm, L = 10 μm) and a capacitor used for C-V process monitoring. Metal is in blue and source and drain areas are shaded. The large size of the device was chosen to allow manual encapsulation and wire bonding processes.

Table 5.1: SiO_2 devices recipe overview

Step	Process	Notes
3	Field oxide lithography	PDOP mask
4	Field oxide implantation	B^+, $4.5\times10^{13}cm^{-2}$
8	Source and drain lithography	SD mask
11	Source and drain implantation	As^+, 5×10^{15}
13	Channel lithography	CHANNEL mask
13	Ion sensitive dieletric layer formation	Thermal SiO_2, 50nm
17	Contacts lithography	CONTACTS mask
20	Metal Deposition	Aluminum, PVD
21	Metal 1 Lithography	METAL 1 mask
25	Metal Sintering	Ready for electric characterization
28	Metal 2 lithography	METAL 2 mask, no gate
29	Gate metal etching	Exposes ion sensitive layer
31	Encapsulation with photoresist lithography	ENCAPS mask

5.1.1 Recipe

1. CLEANING

   Piranha and RCA 1.

2. DRY OXIDATION: FIELD OXIDE

   Growth of 220nm of silicon dioxide through dry oxidation.

   Table 5.2: Field oxidation, T = 1150 °C.

Gas	Time (min)	Notes
O_2	100	Dry oxidation
Ar	10	Surplus oxygen removal

   This oxide plays two very important roles on the device. It isolates the neighboring devices electrically because it creates regions with very high V_t due to its high capacitance/thickness. It also prevents undesirable diffusion of boron from the silicon to the oxide because it is also implanted with boron. Boron tends to diffuse from silicon to oxide if the oxide has a low boron concentration.

3. PHOTOLITHOGRAPHY: FIELD OXIDE IMPLANTATION (PDOP)

   This photolithography protects channel area from the boron implantation.

4. BORON IMPLANTATION

   Energy 65 keV and Dose $4\times10^{13}\text{cm}^{-2}$.

   Implantation of the field oxide silicon to isolate electrically neighboring devices. Channel area is protected by photoresist in Figure 5.3.

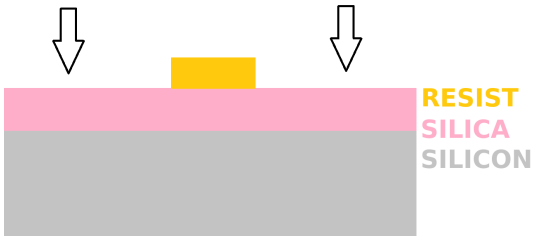


Figure 5.3: Device at the field Boron Implantation step. Channel is protected by photoresist.

5. OXIDE ETCHING

   Removal of 120nm of oxide with buffered etch at room temperature. Measured etch rate of 54nm/ minute. Approximately 105s of etching.

   The remaining 100nm are doped with Boron and serve as a diffusion barrier for boron from silicon.

6. PHOTORESIST REMOVAL AND CLEANING

   Boiling acetone, propanol, DI water wash for photoresist removal. Piranha, RCA 1 for cleaning. Details at section 4.2.

7. WET OXIDATION: OXIDE GROWTH AND BORON DRIVE-IN

   Very thick oxide growth to protect the rest of the chip from the upcoming source and drain implantation. This oxidation also accomplishes the implanted Boron drive-in.

Table 5.3: As^+ implant oxidation, T = 1000 °C.

Gas	Time (min)	Notes
Ar	10	Thermal ramp
O_2	10	Dry oxidation
H_2O	45	Wet oxidation
Ar	20	Surplus oxygen removal

Channel area thickness: S1 - 401nm, S2 - 392nm, A1 - 406nm, A2 - 401nm.

Field area thickness: S1 - 324nm, S2 - 314nm, A1 - 331nm, A2 - 324nm.

The Boron implantation procedure caused considerable damage to the silicon crystalline structure due to the high energy ion collisions. Many of the implanted atoms were also positioned at undesirable interstitial sites instead of substitutional sites right after the implantation. This high-temperature annealing step allows silicon atoms to move back into lattice sites and impurity atoms to enter substitutional sites into the lattice. Annealings with the objective of rearranging the Si structure and activating dopants are called "Drive-in". Figure 5.4 shows the simulated Boron profile at the source and drain regions right after the implantation step and following this drive-in procedure.

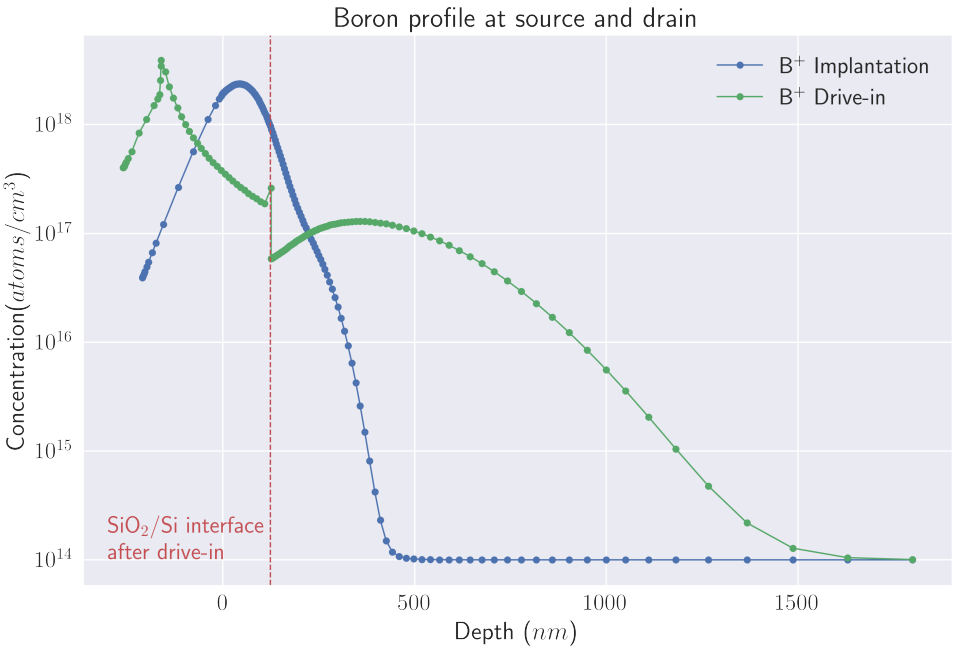


Figure 5.4: Simulated Boron profile. 0 demarks the Si interface position before any oxidation procedure.

8. PHOTOLITHOGRAPHY: SOURCE AND DRAIN (SD)

   Defines the source and drain regions, leaving them exposed for the upcoming oxide etching. This step defines W = 1000μm and L = 10μm.

9. BUFFERED OXIDE ETCH

   Buffered etching with DLV removes oxide and exposes future areas from upcoming implantation. The endpoint is visual and 7 minutes was enough to remove the 400nm thick oxide in the source and drain regions.

10. PHOTORESIST REMOVAL AND CLEANING

    Boiling acetone, propanol, DI water wash for photoresist removal. Piranha and RCA 1 cleaning. Figure 5.5 is a microscope picture of the device at this point. Source and drain areas are well defined and exposed for implantation.

11. As^+ IMPLANTATION

    Arsenic implantation at 150 keV and $5\times10^{15}\text{cm}^{-2}$.

Figure 5.5: Microscope picture of the device right before As^+ implantation. Silicon is exposed at source, drain and capacitor regions and the rest of the device is covered with a thick oxide.

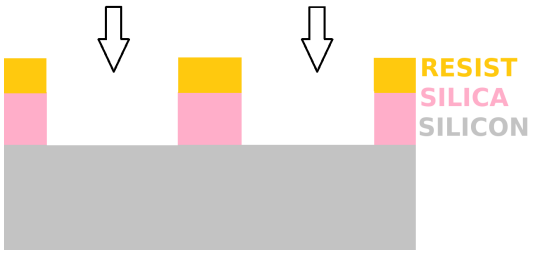


Figure 5.6: Drain and source exposed to the impinging As^+ ions.

12. As^+ DRIVE-IN

Drive-in activates As dopants, reverts the lattice damage introduced at the implantation and grows 300nm of SiO_2. Figure 5.7 shows the simulated impurities profile, expected SiO_2/Si interface and PN junction depths.

Table 5.4: As^+ Drive-in, T = 1000 °C.

Gas	Time (min)	Notes
Ar	20	Thermal ramp and deffect annealing
O_2	10	Dry oxidation
H_2O	45	Wet oxidation
Ar	20	Surplus oxygen removal

Thickness at source and drain: A1 - 383nm, S1 - 370nm, A2 - 378nm, S2 - 375nm.

Thickness at gate/capacitor: A1 - 538nm, S1 - 519nm, A2 - 538nm, S2 - 532nm.

Figure 5.7: Impurities profile after As^+ drive-in.

13. PHOTOLITHOGRAPHY: CHANNEL (CHANNEL)

    Exposes the channel area for etching and subsequent dielectric deposition. Since this is not a self-aligned process the opening is of 20μm even though L = 10μm.

14. BUFFERED OXIDE ETCH

    Buffered etch of 530nm thick SiO_2 on top of the channel area. Etch rate of 66nm/min observed on test sample, 9min and 30s of etching.

15. PHOTORESIST REMOVAL AND CLEANING

    Boiling acetone, propanol, DI water wash for photoresist removal. Piranha, RCA 1 and 2. Removal of native oxide with HF etch. It is critical to perform RCA 2 and remove native oxide here to minimize charges in the gate oxide. Details at section 4.2.

16. DRY OXIDATION: GATE OXIDE

    Growth of 50nm of SiO_2.

Table 5.5: Gate oxidation, T = 1050 °C.

Gas	Time (min)	Notes
Ar	5	Thermal ramp
O_2	60	Dry oxidation
Ar	20	Surplus oxygen removal

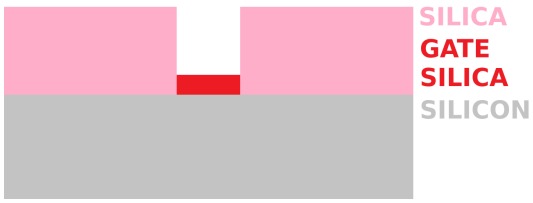


Figure 5.8: Device after gate oxidation.

Thickness at source and drain: S1 - 388nm, S2 - 381nm.

Thickness at gate/capacitor: S1 - 56nm, S2 - 55nm.

Thickness at field: S1 - 483nm, S2 - 468nm.

17. PHOTOLITHOGRAPHY: CONTACT OPENING (CON)

    Defines the contact points of the metal with the silicon source, drain, gate, bulk and capacitor regions.

18. BUFFERED OXIDE ETCH

    Buffered etch source/drain oxide (380nm) and field oxide (480nm). Etch rate of 66nm/min, 8min45s of etching performed.

    Exposes the silicon at the contact areas for upcoming metal deposition.

19. PHOTORESIST REMOVAL AND CLEANING

    Boiling acetone, propanol, DI water wash for photoresist removal. Piranha, RCA 1 for cleaning. Native oxide removed with 5% HF solution.

20. ALUMINUM DEPOSITION

    Physical vapor deposition of aluminum over the whole chip.

21. PHOTOLITHOGRAPHY: METAL 1 (MET)

    Defines connections and pad areas.

22. ALUMINUM ETCH

    Aluminum etched with H_3PO_4 at 50°C with visual end-point. DI water wash.

23. PHOTORESIST REMOVAL

    Boiling acetone, propanol, DI water wash. Piranha cannot be used anymore to clean organic residues because sulfuric acid etches aluminum.

24. CLEANING FOR SINTERING

    10 minutes in thricloroetilen followed by boiling acetone, isopropanol and DI water wash.

25. SINTERING

    20min, 450 °C at forming gas (10% H_2, 90% N_2) atmosphere.

    A Si-Al alloy forms at the contact areas to ensure ohmic contact. This is usually a very dangerous step, because at this temperature, silicon can diffuse in an inhomogeneous manner into aluminum and deep Al spikes may form and shorten the source, drain and bulk ruining the device.

    The treatment was successful and the results can be clearly visualized in Figure 5.9. Before the treatment, a large resistance due to the ill-formed contact between silicon and aluminum hinders the output curve. After the treatment an ohmic contact forms and removes the interference from the contact resistance from the output curve.

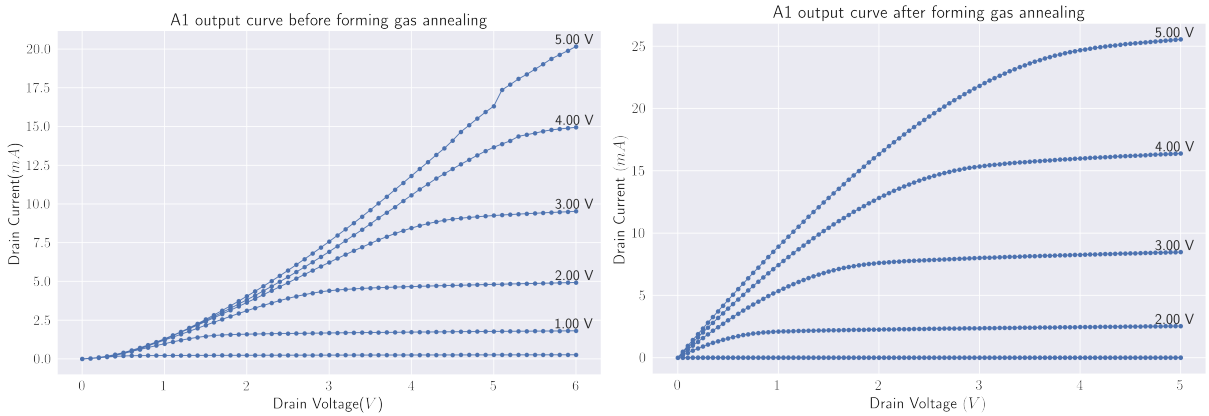


Figure 5.9: Output curve before (left) and after (right) the sintering step.

26. ELECTRICAL CHARACTERIZATION OF TRANSISTORS

For this round of fabrication electrical characterization was made into each transistor before turning then into ISFETs by removing the gate.

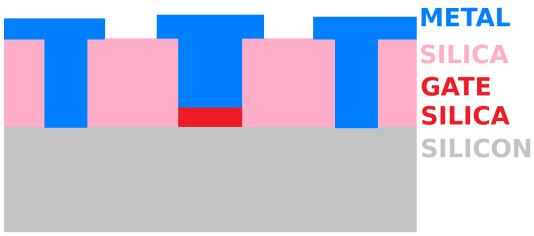


Figure 5.10: Source, drain and gate contacts ready for electrical characterization.

27. CLEANING

Boiling acetone, isopropanol, DI water wash.

28. PHOTOLITHOGRAPHY: METAL WITHOUT GATE (MET2)

This mask leaves the gate metal exposed and the rest of the aluminum covered with photoresist.

29. GATE ETCHING

Gate metal etched (Figure 5.11) with H_3PO_4 at 50°C followed by DI water wash.

Figure 5.11: Channel oxide exposed after the gate etching and the source/ drain contacts covered with photoresist.

30. PHOTORESIST REMOVAL

    Acetone, propanol, DI water wash. Again, piranha solution must be avoided due to aluminum corrosion by sulfuric acid.

31. PHOTOLITHOGRAPHY: ENCAPSULATION WITH PHOTORESIST (ENCAPS)

    This photolithography prepares the chips for the aqueous environment. Covers everything but the metal pads and the channel area with a thick and hard baked photoresist layer.

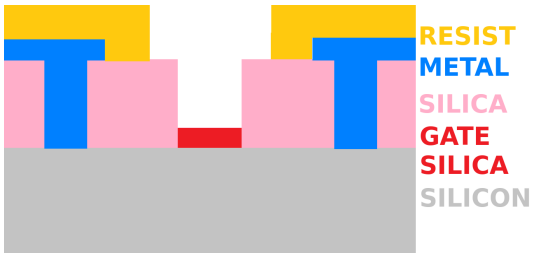


Figure 5.12: Complete SiO_2 ISFET sensor.

5.2 Alumina devices - A1 and A2

The alumina devices fabrication procedure was identical to the SiO_2 ones up to the channel oxide growth. For these devices, a passivation layer of 15nm SiO_2 was grown thermally and covered with 80 nm of ALD Al_2O_3. The thicknesses were chosen to keep the channel capacitance constant with respect to the previous round of fabrication (50nm of SiO_2). Al_2O_3 is also etched by DLV buffer solution so no changes were necessary to perform the contact etch.

In this round, a new metal mask was used (Fig. 5.13). The new mask contains 12 transistors, 60 gateless ISFET sensors with bulk and source tied and 4 ISFET sensors without the bulk/source tie. By mixing transistors and ISFET sensors we eliminated the need to perform an additional photolithography step to remove the metal gate. The trade-off to this approach is that only 12 transistors for electrical characterization are produced and the performance of each sensor cannot be compared with their individual electrical measurements. During tests of the previous round, we could not get working sensors until we manually wired the bulk and source contact. Therefore, this time the bulk and source contacts are shortened directly at the metalization step for most devices, eliminating the hassle to manually wire bond $1mm^2$ pads.

The encapsulation mask remained unchanged and the overview of this fabrication round is at table 5.6.

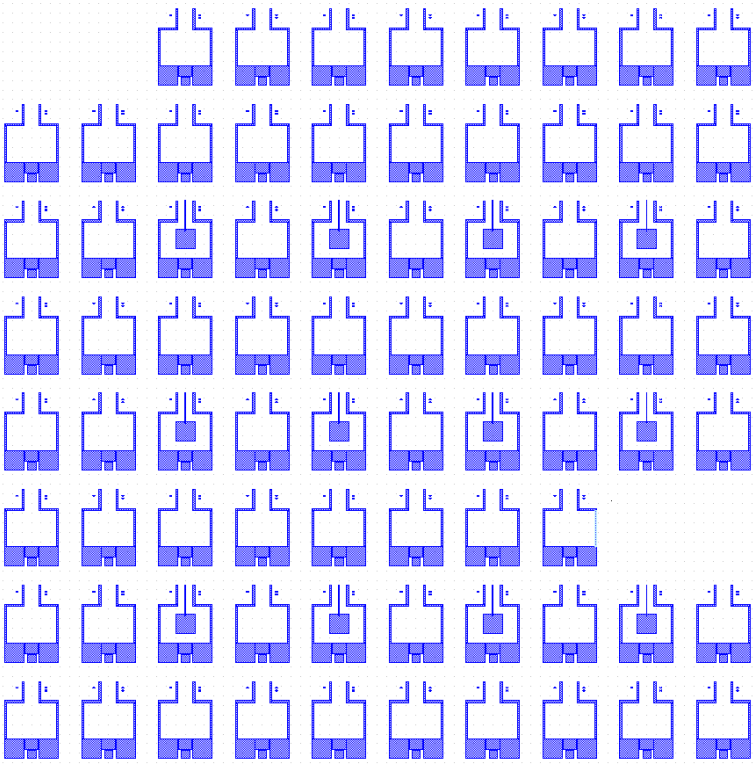


Figure 5.13: New metal mask with both transistors and gateless ISFET sensors. The sensors also had their bulk and source connections connected. This mask eliminated the METAL 2 photolithography and the need to manually wire bond bulk and source pads.

Table 5.6: Al_2O_3 devices recipe overview. Changes with respect to the previous round are in italic.

Step	Process	Notes
3	Field oxide lithography	PDOP mask
4	Field oxide implantation	B^+, $4.5\times10^{13}cm^{-2}$
8	Source and drain lithography	SD mask
11	Source and drain implantation	As^+, 5×10^{15}
13	Channel lithography	CHANNEL mask
17	*Ion sensitive dieletric layer formation*	*15nm SiO_2/80nm Al_2O_3*
18	Contacts lithography	CONTACTS mask
21	Metal Deposition	Aluminum, PVD
22	*Metal 1 Lithography*	*METAL 3 mask*
25	Metal Sintering	Ready for electric characterization
27	Encapsulation with photoresist lithography	ENCAPS mask

5.2.1 Recipe Changes

Only steps after gate oxidation are listed here. Steps 1 through 16 remain unchanged and steps referent to the metal gate removal were not required due to the new metal mask approach. Channel oxidation at step 16 was altered and followed by an ALD deposition procedure and the new mask (Fig 5.13) was introduced.

16. GATE OXIDE GROWTH

    Growth of 15nm of SiO_2.

    Table 5.7: Gate oxidation, T = 900 °C.

Gas	Time (min)	Notes
Ar	10	Thermal ramp
O_2	10	Dry oxidation
Ar	10	Surplus oxygen removal

    Monitor sample thickness: 12nm of SiO_2

17. ALD ALUMINA DEPOSITION

    Deposition of 80nm Al_2O3. Two samples besides the wafers A1 and A2 were placed in the reactor to monitor the process. One of the samples was bare silicon and the other had 12nm of SiO_2 to simulate the gate oxide.

    Alumina thickness for Si/Al_2O_3 stack: 84nm (ellipsometry).

    Alumina thickness for $Si/SiO_2/Al_2O_3$ stack: 80nm (ellipsometry).

18. PHOTOLITHOGRAPHY: CONTACT OPENING (CONTACT)

19. BUFFERED OXIDE ETCH

    Measured etch rate at DLV solution of alumina with test samples was of approximately 10nm/min. 9 minutes in the DLV solution removed the alumina and the passivation SiO_2 layer.

20. PHOTORESIST REMOVAL AND CLEANING

    Boiling acetone, propanol and DI water for photoresist removal. Piranha solution must be avoided because it etches Al_2O_3.

21. PVD ALUMINUM DEPOSITION

22. PHOTOLITHOGRAPHY: METAL LINES DEFINITION (METAL 3)

23. ALUMINUM ETCH

    This etching step is hard because the H_3PO_4 solution etches both aluminum and alumina at a temperature of 50°C. However, alumina etch rate at room temperature is very low. Therefore the etching was done in two steps. Most of the aluminum was removed at 50°C and when we visually noticed that the aluminum was coming off the gate and exposing the alumina film we lowered the temperature to room temperature. The aluminum PVD deposition is not uniform which further increases the difficulty of this etching step. The procedures were very successful for wafer A1 but A2 suffered from an overetch which completely removed the gate as seen in Figure 5.14.

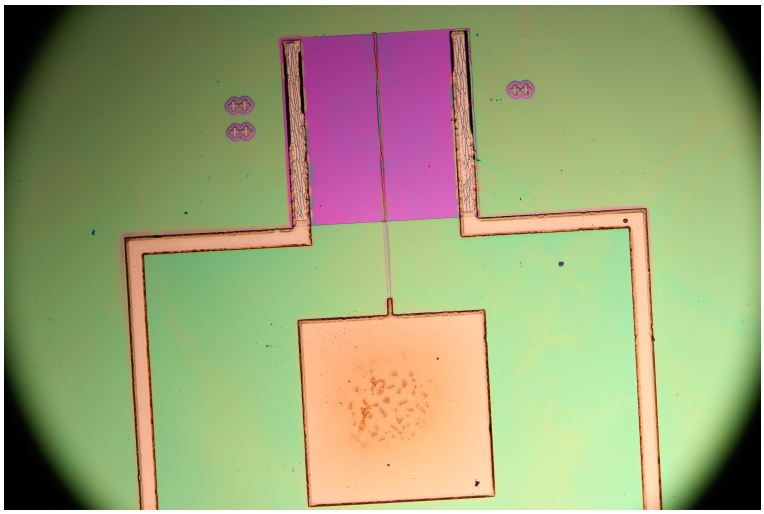


Figure 5.14: Gate was completely removed from the transistors of A2 due to overetching.

    In summary, H_3PO_4 at 50°C followed by H_3PO_4 at room temperature and DI water wash.

24. PHOTORESIST REMOVAL AND CLEANING

    Boiling acetone, propanol, DI water. Piranha solution must be avoided because it etches both aluminum and alumina.

25. CLEANING AND SINTERING

    Identical to the previous round.

26. ELECTRICAL CHARACTERIZATION OF TRANSISTORS

    Due to issues at aluminum etch steps only the 12 transistors of A1 could be characterized.

27. PHOTOLITHOGRAPHY: ENCAPSULATION WITH PHOTORESIST (ENCAPS)

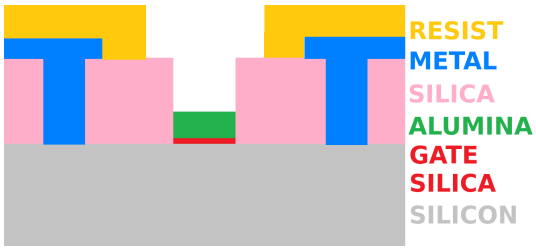


Figure 5.15: Complete Al_2O_3 ISFET sensor.

5.3 Encapsulation and wire bonding

Encapsulation is a very important issue for ISFETs. A well-performed encapsulation prevents damage caused by the aqueous environment and the passage of leakage current through the solution during measurement.

Encapsulation starts with the last photolithography step, which covers everything but the sensing layer in the channel area and the contact pads with photoresist. The wafer is then diced into individual sensors and the sensors glued with double-sided tape to a 5cm PCB probe. Pads are manually wired to copper lines of the PCB probe with very thin silver wires and silver paste. After a thermal treatment to solidify the silver paste (20 mins in the hotplate at 120 °C) the resultant contact resistance (Figure 5.18) is satisfactory. Silicon side surface and copper connections are manually covered with an encapsulant to protect them from the aqueous solutions and prevent current leakage. We tried 3 different resins as encapsulants, AZ1512 photoresist, nail polish and epoxy glue. Photoresist did not show a good isolation and durability, nail polish worked for a while but eventually showed isolation problems. Epoxy glue was the most durable and resistant of all three. Regular copper wires are welded to the tip of the PCB and the probe is ready for measurements. Figure 5.16 shows a probe without encapsulation and a probe encapsulated with blue nail polish.

S1 and S2 devices were fabricated with the METAL 1 mask, which does not connects bulk and source pads. For these devices, bulk/source tie was performed during the wire

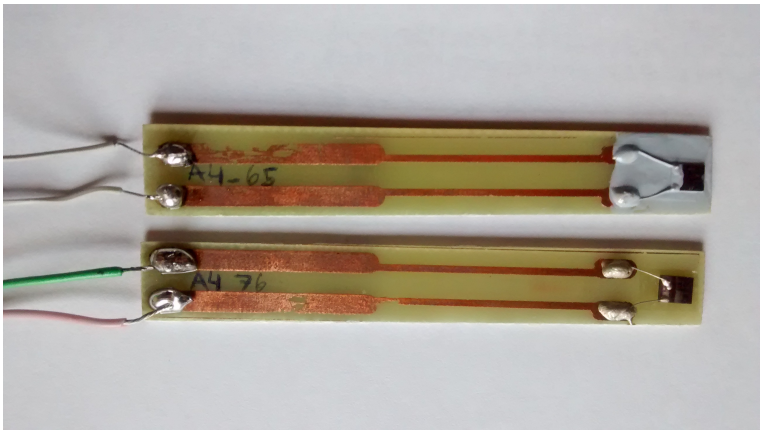


Figure 5.16: Finalized probes after wire-bonding and nail polish encapsulation on top.

bonding. Manually wire bonding 1mm^2 was time consuming and removed from the process with the introduction of the METAL 3 mask. Figure 5.17 shows the bulk and source pads connected by the silver paste coverage.

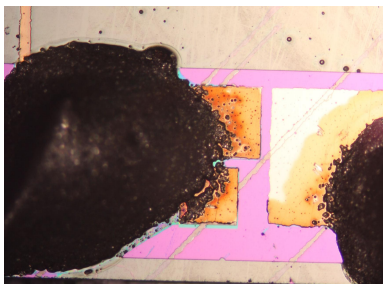


Figure 5.17: Picture of the bulk and source pads connection with the silver paste coverage.

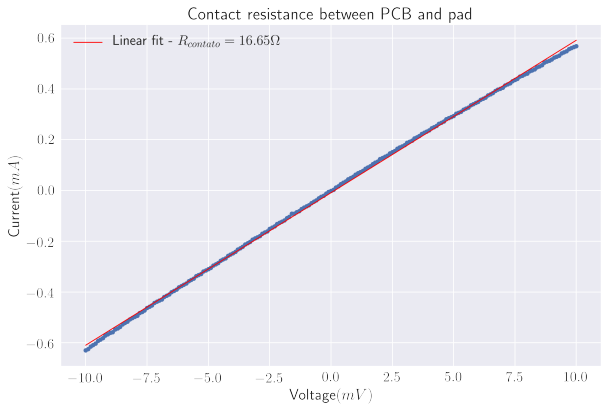


Figure 5.18: Contact resistance of the wire bonding procedure.

Chapter 6

Electrical Characterization

Three different devices were measured to characterize the MOS process: Bulk/Drain PN junction, monitor capacitor and the complete NMOS transistor. The main goal of the PN junction analysis is to quantify the transistor leakage current. The capacitance measurements provide quite a bit of information including the threshold voltage, oxide capacitance and effective oxide charge. Transistor characteristic curves are a direct quantification of the threshold voltage and on-current values. These measurements are of fundamental importance to characterize the overall fabrication process and provide a valuable approximation to the electrical response and operating range of ISFET sensors built from these transistors.

6.1 Capacitors

The parameter extraction described at Section 3.3.1 was performed for the 4 wafers (S1, S2, A1, A2). Measurements were done at HP-4284 at a frequency of 100kHz and all curves are plotted in Figure 6.1. Tables 6.1 and 6.2 summarize the parameter extraction results. A total of 10 capacitors from S1, A1 and A2, and of 8 capacitors from S2 were measured.

Table 6.1: Mean and standard deviation for the SiO_2 capacitors.

	S1	S2
V_t (V)	-0.5 (12.7%)	-0.47 (13.8%)
t_{ox} (nm)	64.6 (1.3%)	62.7(2.0%)
C_{ox} $(nFcm^{-2})$	53.4 (1.3%)	55.1 (2.0%)
Q_{eff} (cm^{-2})	1.53×10^{11} (12.7%)	1.46×10^{11}(16%)
N_A (cm^{-2})	5.1×10^{14} (13.5%)	4.24×10^{14} (17.4%)

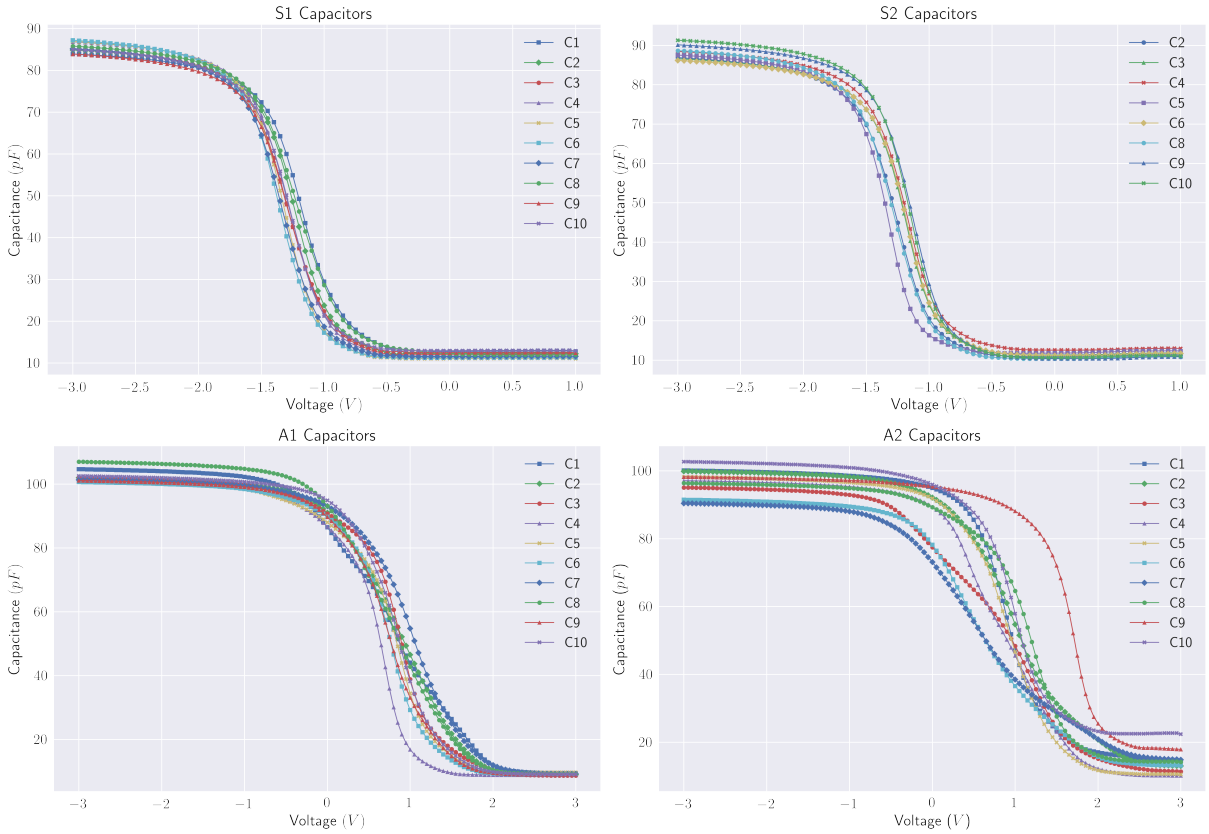


Figure 6.1: Silica (top) and Alumina C-V measurements.

Table 6.2: Mean and standard deviation for the Al_2O_3 capacitors.

	A1	A2
V_t (V)	1.61 (8.6%)	1.8 (17.1%)
$t_{ox,eff}$ (nm)	54.0 (1.9%)	57.1 (4.0%)
C_{ox} $(nFcm^{-2})$	63.9 (2.0%)	60.6 (3.9%)
Q_{eff} (cm^{-2})	-7.05×10^{11} (8.7%)	-6.8×10^{11} (17.5%)
N_A (cm^{-2})	2.45×10^{14} (7.6%)	8.65×10^{14} (7.5%)

The measured oxide capacitance for the silica devices agrees fairly well with the $61.25nF/cm^{-2}$ calculated using the oxide thickness of $55nm$ measured right after the thermal oxidation with the nanospec equipment. The silica devices show a negative V_t as designed for depletion mode devices but a very high standard deviation of 12.7% (S1) and 13.8% (S2) is observed. The root of this variability is the low and variable substrate carrier concentration. There are two ways to mitigate this issue: increase the substrate carrier concentration through a Boron implantation and/or introduce a threshold adjustment implantation step. Increasing the substrate carrier concentration lowers the channel effective mobility but, as will be seen in6.3, μ_{eff} is exceptionally high for these devices

and would still lie within reasonable values with an increased doping.

We designed the capacitors of A1 and A2 with $80nm$ $Al_2O_3/15nm$ SiO_2 because we wanted them to have a capacitance equivalent to the $60nm$ of pure SiO_2 from S1 and S2. Considering that we had no previous experience with the alumina dielectric, the resulting C_{ox} around $60nFcm^{-2}$ is reasonably close to the values around $50nFcm^{-2}$ from the pure silica capacitors. With the designed capacitance, we expected the alumina devices to have a similar V_t and to be of depletion mode. Unfortunately, we did not took into account the negative charges that come with Al_2O_3. These negative charges caused the V_t to shift all the way up to 1.6 V (A1) and 1.8 V (A2). The V_t variability of A1 (8%) and A2 (17%) are caused not only by the substrate carrier concentration issue, but also by a higher density of interfacial traps at the SiO_2/Al_2O_3 interface. These traps increase V_t even further, and cause the various curve shapes at the depletion region that are particularly evident for the A2 plots in Figure 6.1. The presence of interfacial traps is much more pronounced on A2 and that is why it has the highest standard deviation values among all wafers.

Hysteresis capacitance curves (Figure 6.2) were performed to check for mobile charges within the dielectric layers and none of the wafers showed a observable amount of mobile charges.

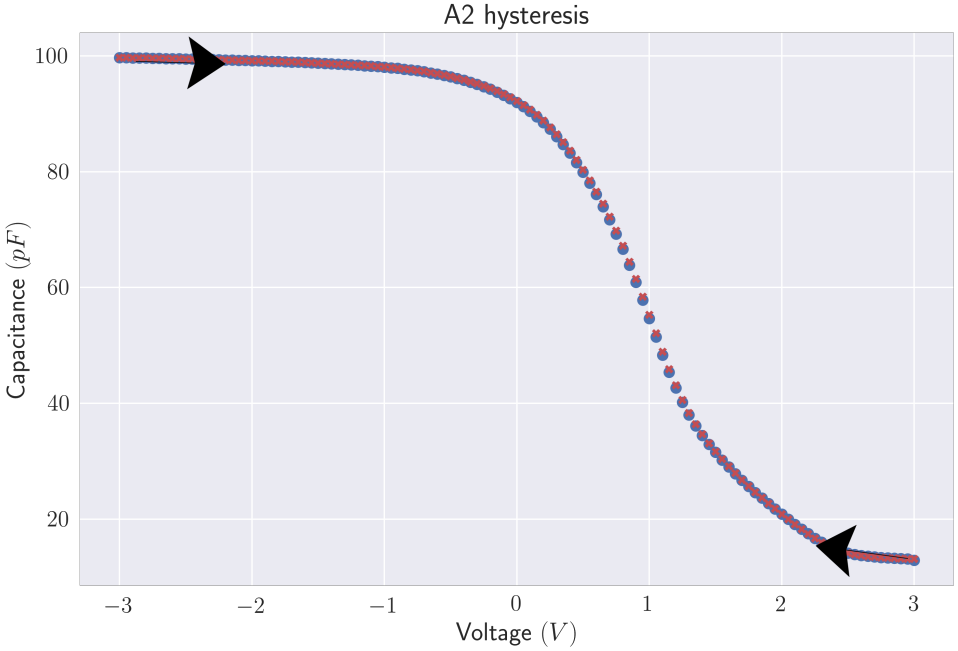


Figure 6.2: Hysteresis curve for the A2 wafer. Capacitance hysteresis was not observed due to the lack of mobile charges in the oxide.

6.2 Transistors

Transfer and output curve measurements were done on the NMOS transistors using the HP4155A Semiconductor Parameter Analyzer. V_t, g_m and μ_{eff} were extracted from the transfer curves as described in Figure 3.7 and the output curves served to check the current levels and operating range of the devices. An output and transfer curves from S1 and A1 are plotted in Figure 6.3. The parameters were extracted from a sample of 10 transistors from S1 and S2 and 7 transistors from A1. The results are summarized in Table 6.3 along with the oxide capacitance and effective charge from the C-V analysis. Five out of twelve transistors on A1 had a short circuit due to unremoved aluminum and it was not possible to make this analysis on A2 because the transistor gate was completely removed due to an overetch during the aluminum removal (Figure 5.14).

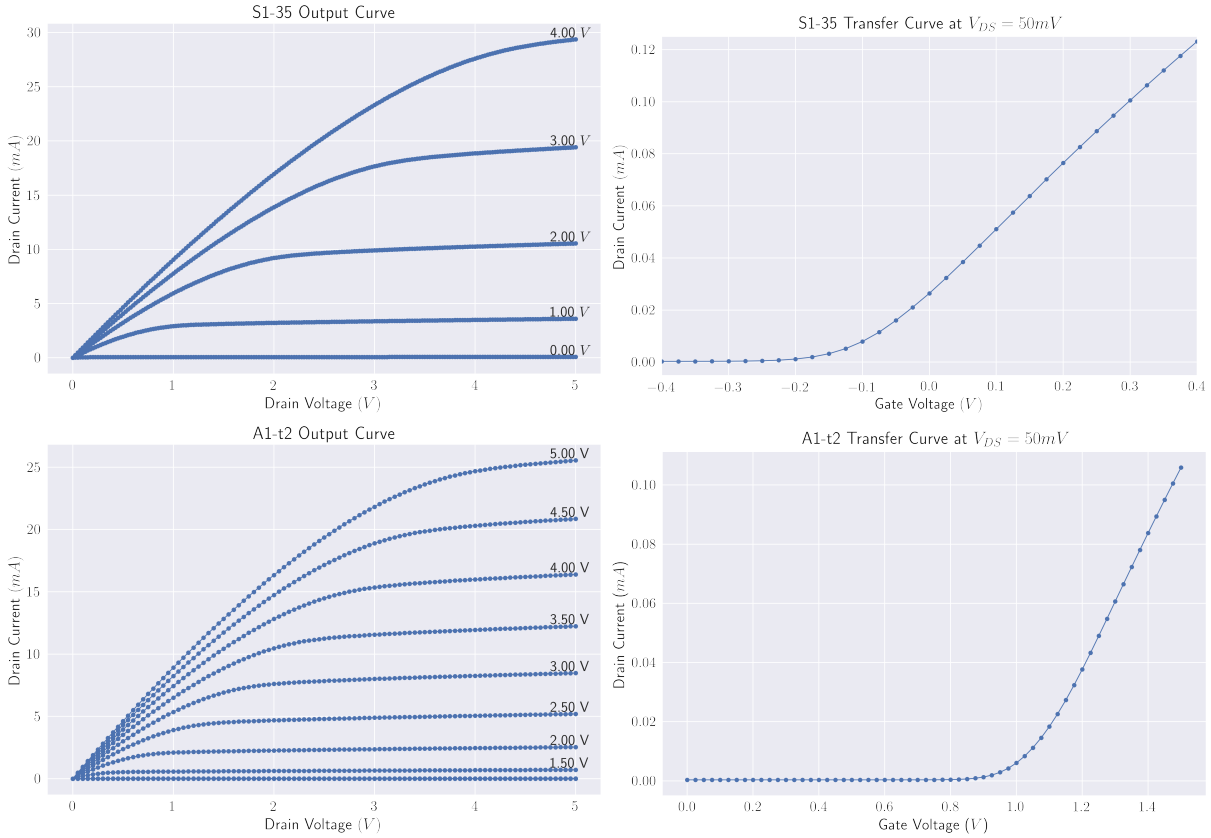


Figure 6.3: Output and transfer characteristics of a single transistor from S1 and A1.

The high current at the order of tens of mA observed at the saturation region of the output curves was a consequence of the large size of these transistors. Their size was chosen to facilitate the manual encapsulation procedure but it is also handy to work with devices that work at a current range that is easily detectable. The extracted effective

Table 6.3: Extracted parameters for S1, S2 and A1.

	S1	S2	A1
V_t (V)	-0.20 (27%)	-0.17 (34%)	1.10 (8.6%)
g_m (mS)	0.26 (14.3%)	0.25 (8.7%)	0.26 (25.6%)
μ_{eff} $(cm^2/V.s)$	1000 (14.3%)	970 (8.7%)	831 (25.6%)
C_{ox} $(nFcm^{-2})$	53.4 (1.3%)	55.1 (2.0%)	63.9 (2.0%)
Q_{eff} (cm^{-2})	1.53×10^{11} (12.7%)	1.46×10^{11}(16%)	-7.05×10^{11} (8.7%)

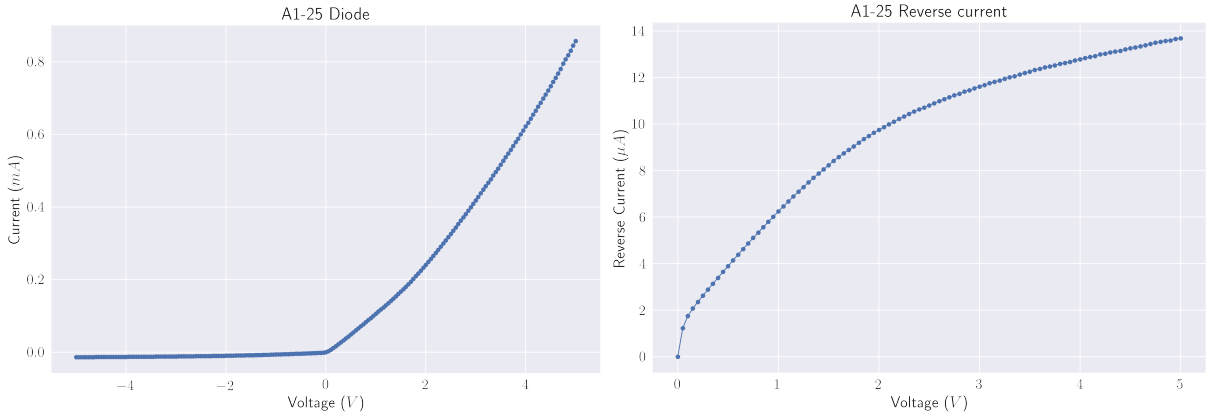
mobility is around 1000 $cm^2/V.s$ for S1 and S2 and of 831 $cm^2/V.s$ for A1. These very high mobilities are due to the exceptionally low (N_a $10^{14}cm^{-3}$) substrate doping. Usually CMOS processes employ wafers with N_a of a few orders of magnitude higher. The original recipe adapted to our process was taken from [34] and the effective mobility they found was 40% lower for N_a $10^{16}cm^{-3}$.

Unfortunately, the very high standard deviation of V_t is the price we pay for such a low and variable substrate doping. The variability for V_t was even higher than the one observed from the capacitance analysis. Nevertheless, the devices from S1 and S2 are of depletion mode and from A1 are of enhancement mode.

6.3 PN junction

In an NMOS transistor the P doped bulk and the N^+ doped drain form a PN junction that is polarized reversely whenever positive voltage is applied at the drain with respect to the bulk. Since the bulk is tied to the source, the diode is reversely polarized at all the working regions. The diode reverse current must be much smaller than the current flowing through the channel otherwise it represents an alternate low resistance path between drain and source and interferes with the transistor functionality. Therefore, the analysis of this current is essential to ensure the transistors work properly.

Figure 6.4 shows the full diode curve and the reverse current plot for a device from the A1 wafer where the reverse current reaches tens of μA for 5 volts applied. The drain to source current at 6.3 is of tens of mA and this thousandfold gap between the currents asserts that the PN junction leakage current does not interferes with our device. The reverse current at -5V was measured for 22 diodes from A1 and a mean of $93\mu A$ and a standard deviation of 83% was observed. We attribute the large variance to the difficulty of doing a defect free process at a very large drain/source area. We did not observe



(a) Complete diode curve

(b) Reverse current plot

Figure 6.4: Diode current analysis on a device from the A1 wafer.

interference with the transistor functionality even for hundreds of μA of reverse current.

Chapter 7

Sensor Characterization

In this chapter, the ISFET experiment results are presented for the silica and alumina sensors. The ISFETs and the Ag/AgCl reference electrode were inserted into a buffer solution and connected to the HP4155A semiconductor parameter analyzer (Figure 7.1). The sensor comprises of the gateless transistor glued and wired to the PCB support. The reference electrode in these experiments plays the role of the gate on the standard electrical characterization measurements. The sensors and the reference electrode were placed in a standard "claw" support that allows immersing them in the solution becker and holding them in place while connected to the parameter analyzer. This setup is optimal for prototyping as the HP4155A controlled by the LabVIEW software[36] is able to apply and record voltages and currents of all terminals simultaneously, essential for troubleshooting.

A wide range of variations of the experiment can be done with this setup. Output curves and transfer curve were collected in different pH solutions. The goal of these measurements was to characterize the influence of the solution pH on the ISFET electrical parameters and to find an optimal operating range for the sensors.

7.1 ISFET measurements

When the ISFET is inserted in an aqueous solution charges accumulate at the exposed channel insulator surface, the ions in the electrolyte respond to the accumulated charge and an electrical double layer resembling a capacitor is formed. A voltage ψ_0 builds up across the double layer and it causes a shift on V_t given by (3.20). This V_t shift is shown

Figure 7.1: ISFET experiment picture. With the use of a "claw" support the sensor and the reference electrode are placed into the aqueous solution and connected to the semiconductor parameter analyzer.

in Figure 7.2 for one of our silica sensors. For the silica sensors, a V_t shift of +0.5V was observed due to this effect. In the figure, two curves are shown: the blue curve represents the silica ISFET measured inside a pH=7 buffer solution and the green curve is the transfer curve from the silica device shown in Figure 6.3 from the previous chapter. Performing the parameter extraction for this transfer curve a V_t of 0.399 V, g_m of 0.326 mS and a μ_{eff} of 988 $cm^2/V.s$ are found. Comparing these values to the ones at 6.3 we can see that the only one that is drastically different and outside the process variation is the threshold voltage, which indicates that the transistor is basically unchanged except for the threshold voltage shift.

A similar behavior is observed for the alumina sensors at Figure 7.3. The alumina sensor has a V_t of 1.8 V inside the pH=7 buffer, a shift of 0.8V compared to the correspondent MOSFET. The shift is higher for alumina sensors due to the higher number of sites available for ions in the alumina surface, 8×10^{18}, when compared to silica‘s 5×10^{18} as noted in Table 3.2. The higher number of sites is one of the reasons that the intrinsic buffer capacity of alumina is higher and this becomes evident when the V_t shift of the sensors are compared.

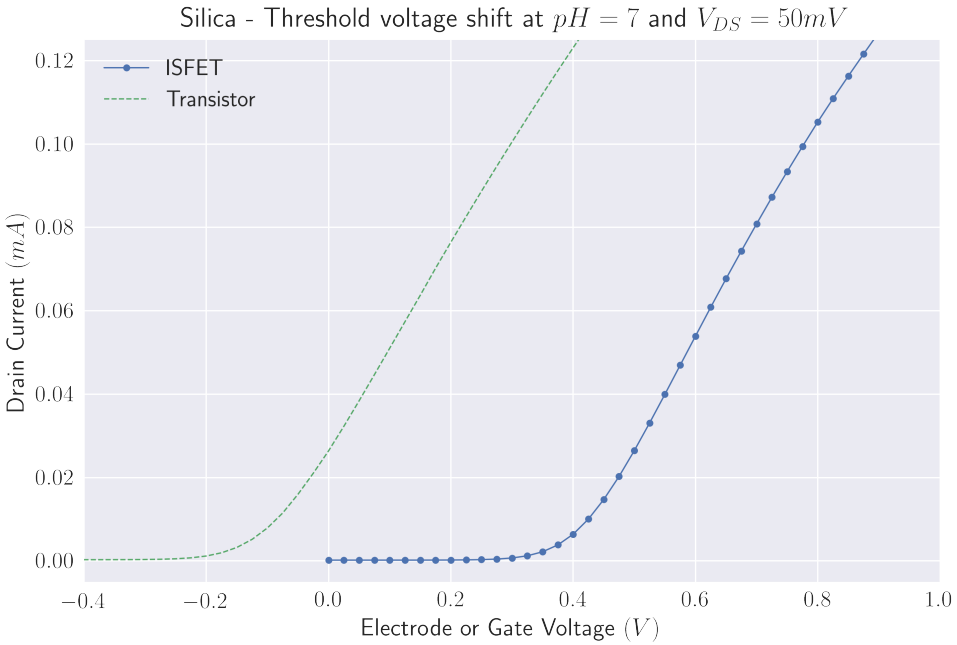


Figure 7.2: ISFET transfer curve measured within the pH=7 buffer in blue and a transfer curve from a transistor in green. A V_T shift of +0.5V is caused by the H^+ charges from the aqueous solution.

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This V_t shift is what makes the ISFET sensor pH dependent. The change of the electrical double layer potential with the bulk pH (pH_B) shifts V_t to higher values in more basic solutions and to lower values in more acid solutions. Qualitatively, it can be said that a more acid solution has a surplus of positive ions whose electric field attracts negative charges at the channel region, which facilitates the inversion condition and lowers the V_t. Quantitatively, the buffering of ions at the oxide surface is modeled by the Intrinsic Buffer Capacity (β_{int}) and the capacitive action of the double layer by the Differential Capacitance (C_{dif}) as explained in section 3.4.1. The change of ψ_0 with pH_B can be calculated through these two parameters with (3.28), and is what influences pH sensitivity.

We observed this shift experimentally by repeating the transfer analysis with the sensors inserted in pH buffer of 6.5, 7 or 7.5 at room temperature. Figure 7.4 shows the results for silica and Figure 7.5 the same measurement for the alumina sensor. The transfer curve analysis was repeated for each curve and results are summarized in Table 7.1.

Analysing the results at Table 7.1 for the silica devices the pH sensitivity is of 30mV/pH for acid solutions and 24 mV/pH for basic solutions. The Alumina sensors fared better and presented a sensitivity of 32mV/ph for acids and 48mV/pH for basic solutions. Figure

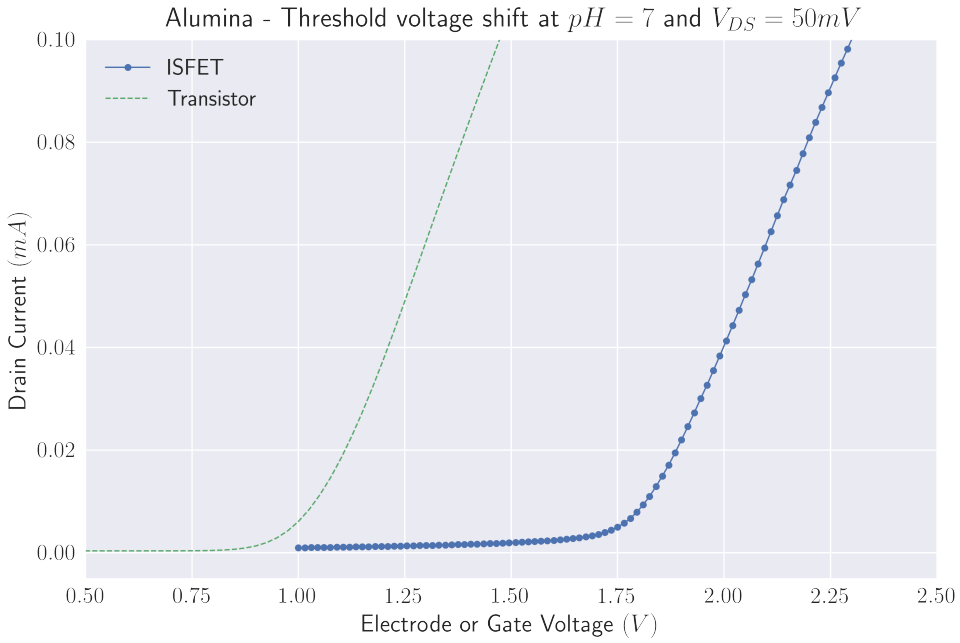

Figure 7.3: V_T shift due to electrolyte presence for alumina sensors

Table 7.1: Transfer analysis result from all curves plotted in Figures 7.4 and 7.5

	Silica			Alumina		
Solution pH	6.5	7.0	7.5	6.5	7.0	7.5
V_t (mV)	392	407	419	1778	1794	1818
g_m (mS)	0.266	0.267	0.270	0,197	0.198	0.201
μ_{eff} $(cm^2/V.s)$	964	969	978	716	718	730

3.14 shows that both oxides have a similar C_{dif} but alumina has a much higher β_{int} and that explains the superior performance of the Al_2O_3 sensors.

The results for the SiO_2 sensors are overall in very good agreement with literature and so is the Al_2O_3 sensitivity for basic solutions [6]. The results for Alumina in acidic solutions are unexpected though. Looking at figure 3.15 and literature results, it was expected a constant sensitivity. The reasons for this discrepancy is unknown but is probably related to the buffer solutions used throughout the experiment. The solution of pH 6.5 is a result of titration of NaOH into the pH=4 buffer solution of Bipthalate Potassium, while the pH 7 and pH 7.5 solutions are both from the same buffer solution of Sodium Hydroxide and Monopotassium phosphate. Further investigation is required to pinpoint specific chemical reactions that are hindering the performance of the Alumina sensor in this acidic buffer solution.

The output curves at Figure 7.6 from these ISFET sensors show the sub-threshold,

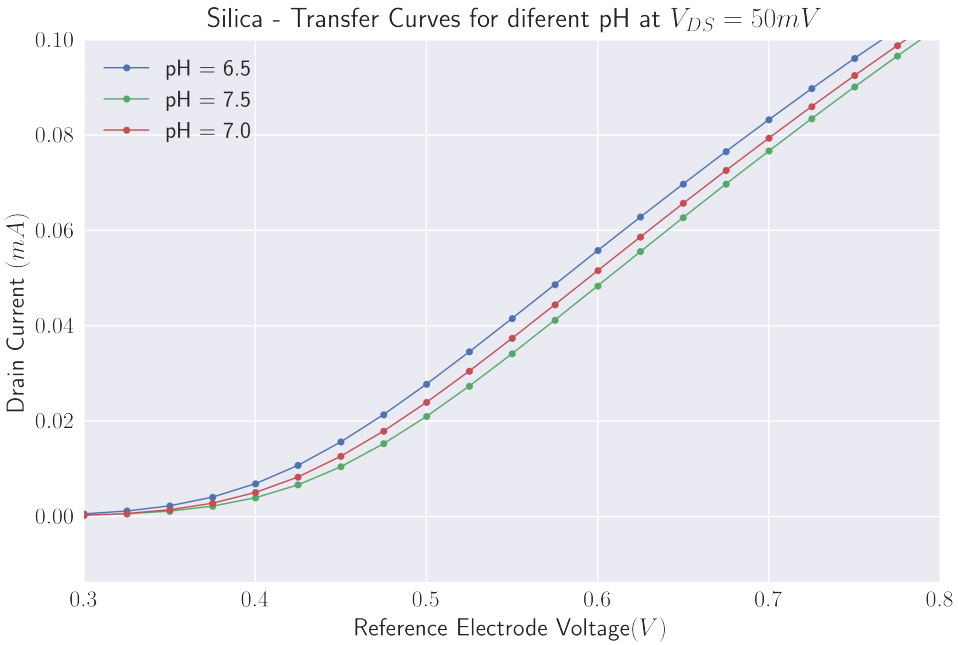

Figure 7.4: Transfer curves at different pHs for the S2-D2 silica ISFET. It was observed a V_t shift of 30mV/pH for the acid solution and of 24 mV/pH for the basic solution.

linear, and saturation regions very clearly. The interesting part is that either the reference electrode voltage or the pH of the solution can play the role of the metal gate voltage and modulate current levels. For NMOS sensors, a higher electrode voltage at the same solution increases the number of carriers in the conductive channel. If the reference electrode is kept constant and the pH of the solution changed, the V_t shift observed on the transfer curves can increase (lower pH) or decrease (higher pH) the current levels going through the channel.

The performance of the silica sensor was observed for one hour with measurements of output and transfer curves made every fifteen minutes in Figure 7.7. The goal of this experiment was to test the operational stability and look for a possible drift at the V_t shift. The transfer characteristic analysis was repeated for each curve and the results are summarized in Table 7.2. Some variation is seen in the output, curves but the transfer analysis shows steady results with respect to time. The experiment was not done for longer times to preserve the sensor.

Sensor durability is still an issue that has to be solved. Even with the epoxy glue encapsulation most sensors failed after a few minutes of use. A more robust encapsulation technology would have to be developed, with the use of molds or one of the different construction schemes as seen on [37]. Most of the methods seen on literature use equip-

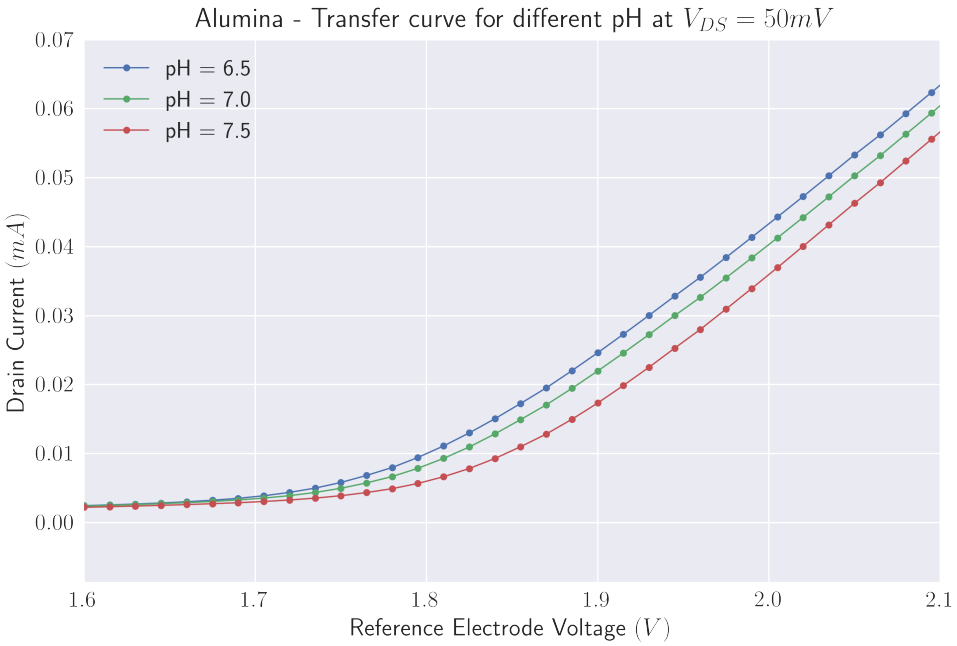

Figure 7.5: Transfer curves for the A1-57 alumina sensor. A shift of 32 mV/pH for the acid solution and of 48 mV/pH for basic solutions was observed.

ments and techniques not available in our lab. The development of these techniques and application of them into this ISFET technology could be a part of a future endeavor.

Table 7.2: Transfer characteristic parameters extracted over time for the silica sensor inside a pH=7 buffer solution

	0min	15min	30min	45min	60min
V_t (mV)	399	393	394	395	395
g_m (mS)	0.326	0.326	0.322	0.324	0.323
μ_{eff} $(cm^2/V.s)$	989	988	975	982	980

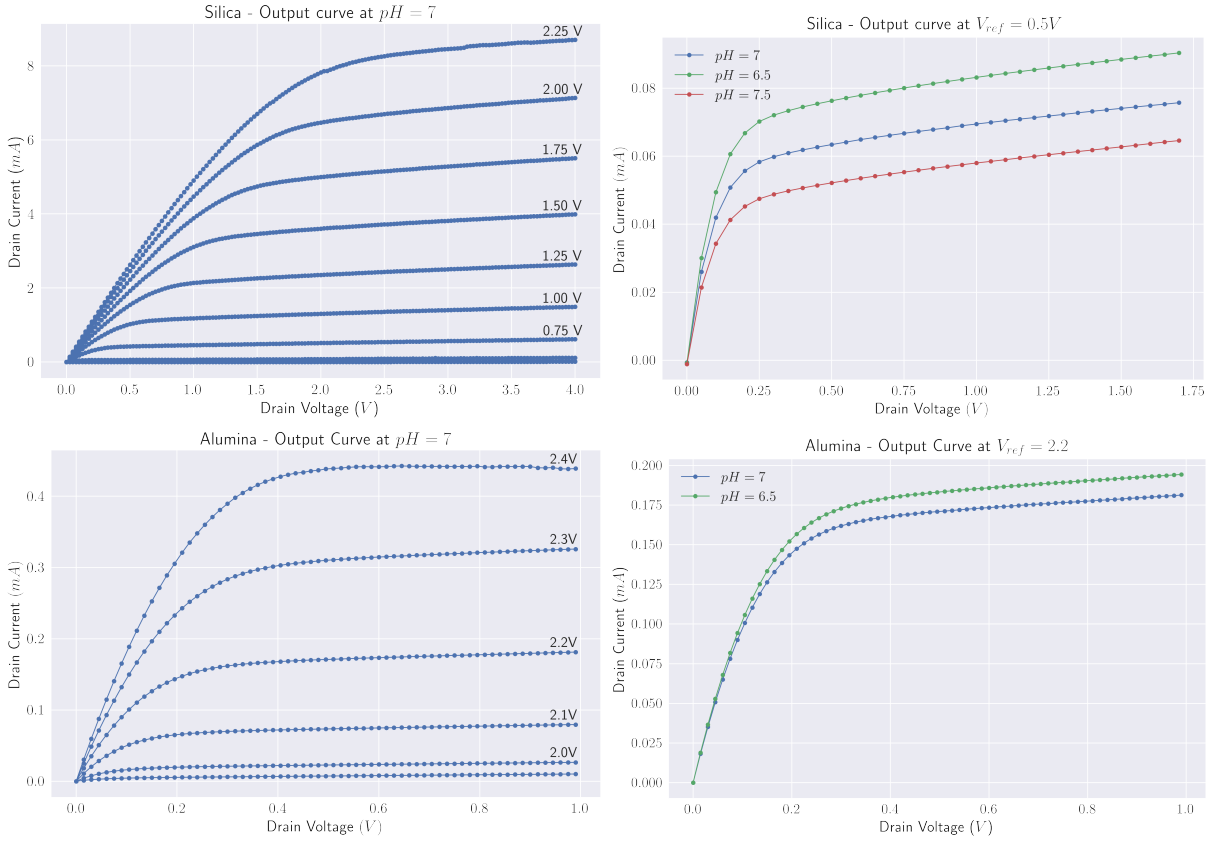

Figure 7.6: Output characteristics for the silica sensors at the top and for alumina sensors at the bottom. In the plots to the left the current is modulated by the reference electrode voltage and to the right by the pH of the solution.

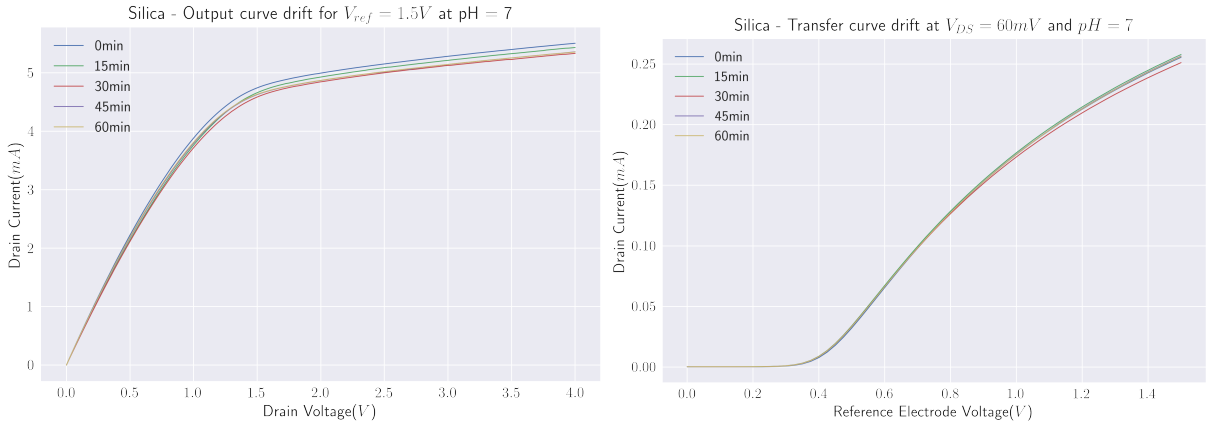

Figure 7.7: Output and transfer characteristics for the silica sensor over the interval of one hour. Each curve is taken at an identical bias and setup but at different times.

Chapter 8

Conclusion

We developed a methodology to fabricate, encapsulate and characterize properly working ISFET probes at UFRGS microelectronics laboratory. The fabrication process was entirely done with in-house CMOS compatible technology from UFRGS clean-room. The process had a total of 6 lithography steps. Large NMOS transistors (W=1000μm, L=10μm)were designed to allow manual encapsulation. Sensors with thermal silica and ALD deposited alumina as the sensing layer were fabricated and the material variety required adaptations to the recipe technology. The process was fully characterized and monitored through capacitance and I-V measurements. Silica devices presented a negative V_t but alumina devices had a positive V_t due to negative charges in the oxide. Sensors were wire-bonded to a PCB probe and encapsulation with photoresist, nail-polish and epoxy glue were done, with the latter showing the best results.

The ISFET experiment setup was done with the use of a Semiconductor Parameter Analyzer connected to a commercial Ag/AgCl reference electrode and the ISFET source and drain. The ISFET probes and the reference electrode were immersed into different pH solutions yielding a pH sensitivity for silica of 30mV/pH for acid solutions and 24 mV/pH for basic solutions. The alumina sensors presented a sensitivity of 32mV/ph for acids and 48mV/pH for basic solutions. The results were coherent with theoretical models and the literature results, with the exception of the low sensitivity of the alumina sensor in acidic environment.

The encapsulation process still has to be refined to fabricate sensors with a longer lifetime but we came a long way from the original prototypes which could barely endure one measurement. This leaves room for improvement and research perspective. This is

a rich line of research and with the fabrication and experimental foundation developed in this study it can be extended to sensors with exotic materials sensitive to different chemical or biological species.

Appendix A

Process simulation code

1D Simulation for Synopsys Sentaurus Proccess at the Source and Drain regions of the recipe described at chapter 5.

```
#####Arquivo de simulação 1D das regiões de dreno e fonte do processo ISFET 1D#####

#####MESHING#####

line x location= 0.0      spacing= 1<nm>  tag=SiTop
line x location= 250<nm>  spacing=5.0<nm>
line x location= 1<um>  spacing=50.0<nm>
line x location= 2.0<um>  spacing= 0.2<um>
line x location= 4.0<um>  spacing= 0.4<um>
line x location=10.0<um>  spacing= 2.0<um>  tag=SiBottom

#####INIT#####

region Silicon xlo=SiTop xhi=SiBottom

init concentration=1e+14<cm-3> field=Boron

#####OXIDE GROWTH#####

deposit Oxide type=isotropic thickness=210.0<nm>
```

```
#####LITOGRAFIA PARA ENRIQUECIMENTO DAS ÁREAS PASSIVAS - MÁSCARA PDOP#####

#####IMPLANT (SD ONLY)#####

implant Boron energy=65<keV> dose=4e13<cm-2>

#####Dummy Oxidation for Boron Profile data#####
diffuse temperature=450<C> time=0.0002<s>

SetPlxList { BTotal }
WritePlx SD_B_ImpB.plx

#####ETCH OXIDE#####
etch oxide thickness=110<nm> type=isotropic

#####ANNEALING/OXIDE GROWTH#####

##For inert anneal
#diffuse temperature=1000<C> time=85<min>
#strip Oxide

##Remesh

pdbSet Grid sMesh 0
mgoals min.normal.size=1<nm> max.lateral.size=0.2<um> normal.growth.ratio=1.2

diffuse temperature=1000<C> time=10<min>
diffuse temperature=1000<C> time=10<min> O2
diffuse temperature=1000<C> time=45<min> H2O
diffuse temperature=1000<C> time=20<min>
```

```
select z=1
layers

SetPlxList { BTotal }
WritePlx SD_B_DriveInB.plx

##SAVE Struct
struct tdr=SD_1D_DriveInB;

#####LITOGRAFIA FONTE E DRENO - MÁSCARA SD#####

#####STRIP OXIDE (SD ONLY)#####
#strips oxide at source and drain regions.
strip oxide

#####IMPLANT As (SD ONLY)#####

implant Arsenic energy=150<keV> dose=5e15<cm-2>

SetPlxList { BTotal }
WritePlx SD_B_ImpAs.plx

SetPlxList { Arsenic_Implant }
WritePlx SD_As_ImpAs.plx

#####"DRIVE IN" As#####

#remesh

pdbSet Grid sMesh 0
mgoals min.normal.size=1<nm> max.lateral.size=0.2<um> normal.growth.ratio=1.2
```

```
diffuse temperature=1000<C> time=10<min>
diffuse temperature=1000<C> time=10<min> O2
diffuse temperature=1000<C> time=45<min> H2O
diffuse temperature=1000<C> time=20<min>

SetPlxList { AsTotal }
WritePlx SD_As_DriveInAs.plx

SetPlxList { BTotal }
WritePlx SD_B_DriveInAs.plx

##SAVE Struct
struct tdr=SD_1D_DriveInAs;

#####Gate Oxidation#####

diffuse temperature=1000<C> time=10<min>
diffuse temperature=1000<C> time=60<min> O2
diffuse temperature=1000<C> time=20<min>

select z=1
layers

SetPlxList { AsTotal }
WritePlx SD_As_Gate.plx

SetPlxList { BTotal }
WritePlx SD_B_Gate.plx

#####Contact annealing#####

diffuse temperature=450<C> time=30<min>
```

```
select z=1
layers

SetPlxList { AsTotal }
WritePlx SD_As_Final.plx

SetPlxList { BTotal }
WritePlx SD_B_Final.plx
```

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