UNIVERSIDADE FEDERAL DO RIO GRANDE DO SUL
ESCOLA DE ENGENHARIA
ENGENHARIA DE MATERIAIS

ENG02298 TRABALHO DE DIPLOMAÇÃO

ANALYSIS OF THE ETCH-BACK OF THE FRONT EMITTER CAUSED BY THE REAR-ETCH PROCESS ON CZOCHRALSKI MONOCRYSTYLLINE P-TYPE SILICON AND DEVELOPMENT OF A GETTER PROCESS

Análise do *etch-back* do emissor frontal causado pelo processo de *rear-etch* em silício monocristalino tipo-p e desenvolvimento de um processo de *getter*

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July 2017

Resumo expandido

(Extended Abstract in Portuguese)

Introdução

A qualidade das lâminas de silicio monocristalino utilizadas na fabricação de células fotovoltaicas é significantemente limitada pela presença de impurezas e a medida que a industria demanda materiais de melhor qualidade porém mais baratos, novas técnicas de processamento devem ser implementadas como maneira de remover impurezas.

Objetivos

Durante a difusão do emissor de fósforo de uma fase gasosa no substrato do tipo-p o emissor é geralmente formado em toda a superfície da lâmina (incluindo as duas faces e as bordas). Quando os contatos são definidos, o emissor frontal e o traseiro podem ser isolados (isolamento de bordas), ou o emissor traseiro pode ser removido (ou ainda evitado). Remover ou evitar o emissor traseiro traz os mesmos (ou até mesmo melhores) benefícios do que o isolamento de bordas, logo esses processos podem ser usados também para isolamento de bodas. Várias técnicas de isolamento de bordas estão disponíveis para uso industrial, incluindo corte mecânico, corte a laser (que resultam na produção de resíduo que não pode ser reciclado e redução da área ativa das células em até 6%) e plasma etching, que apesar do bom rendimento necessita de manuseio cuidadoso e produz resíduos gasosos que necessitam ser reciclados antes de serem

descartados na atmosfera.

A Universidade de Kontanz junto com a empresta RENA desenvolveu um ataque em banho químico automatizado e em linha que remove o emissor traseiro. No processo, lâminas são transportadas através de uma solução ácida de maneira que somente a parte traseira da lâmina entra em contato com o banho químico. Células solares com contatos metálicos impressos (Screen-printed solar cells) requerem uma alta concentração de dopantes na superfície para limitar a resistência de contato, resultando em uma perda de corrente devido a resposta fraca a comprimentos de onda curtos. As células solares com emissor seletivo dopadas a laser (Laser-doped selective emitter, LDSE) superam esse problema pois possibilitam o uso de um emissor levemente dopado. Uma rota para a obtenção de um emissor levemente dopado é através da difusão de um emissor pesado (com alta concentração de dopantes ativos na superfície) seguida de um *etch-back* do emissor (que consiste em remover certa quantidade da superfície do emissor). Essa técnica para a formação de um emissor levemente dopado é particularmente interessante pois provem o beneficio extra da elevada captura de impurezas devido a difusão de grandes quantidades de fósforo. Apesar do processo de *rear-etch* ser realizado abaixo da temperatura ambiente para evitar a emissão de vapores ácidos, esses vapores podem ser emitidos. Este trabalho analisa a possibilidade de usar o processo de *rear-etch* para realizar não só suas funções primarias (isolamento de bordas e remoção do emissor traseiro) como também um *etch-back* do emissor frontal para obtenção de um emissor leve. Além disso, foram testados dois novos processos de difusão desenvolvidos a partir da adição de uma etapa de drive-in sem oxigênio aos processos de difusão padrões (do tipo Screen-print e Getter) utilizados no Sirf Industrial Research Facility (SIRF) e também a eficiência em capturar ferro dos processos.

Metodologia

Foram utilizadas amostras psudo-quadradas de silício monocristalino Czochralski tipo-P de 156 mm x 156 mm e com uma resistência de 1.6 $\Omega.cm$. As amostras foram texturizadas com

ataque ácido para formar piramides invertidas aleatórias e então submetidas a limpeza pelo método RCA antes de serem divididas em quatro grupos receberem diferentes processos de difusão.

Após a difusão, a camada de PSG formada foi removida em uma solução de 2.5% de ácido fluorídrico e as amostras foram separadas em um grupo de controle (que não foi submetido ao processo de *rear-etch*) e três grupos onde as amostras foram submetidas ao processo de *rear-etch* 1, 2 e 3 vezes. Finalmente, uma camada de 75 nm de espessura de nitreto de silício (SiNx) foi depositada nos dois lados das amostras por deposição química em fase vapor melhorada por plasma. As propriedades do emissor formado pelos diferentes processos de difusão foi caracterizada através da resistência de folha da camada dopada com fósforo, da medida da profundidade da junção p-n e do perfil de dopantes ativos na amostra (através da técnica de Electrochemical Capacitance Voltage). Medidas do tempo de vida dos portadores de carga minoritários das amostras foram realizadas antes e depois do processo de queima a fim de determinar a quantidade de ferro intersticial presente nas amostras (através do método desenvolvido por Zoth e Bergholz). Medidas de reflectância foram realizadas juntamente com imagens de fotoluminescência e medidas da resistência de folha em 49 pontos distribuídos pela superfície de cada lâmina a fim de determinar os efeitos do *etch-back* causado pelos gases originados no banho químico no emissor frontal.

Resultados e discussão

Efetividade em capturar ferro dos processos de difusão Screen-print e Getter padrões

Amostras de controle que não passaram por nenhum processo de difusão apresentaram ferro intersticial em concentrações da ordem de 10^{11} cm^{-3}. A presença de ferro intersticial não foi detectada nas amostras que passaram pelo processo de difusão do tipo Getter padrão, mesmo depois do processo de queima que poderia ter dissolvido precipitados de ferro presentes no interior das lâminas. As amostras que foram submetidas ao processo de difusão do tipo

Screen-print padrão apresentaram baixa concentração de Fe_i^+ antes da queima . Porém após serem submetidas ao processo de queima-rápida a 855 °C as mesmas apresentaram concentrações de ferro intersticial entre 10^{10} e 10^{11} cm^{-3}.

Difusões do tipo heavy-getter melhoradas

A adição de uma etapa de drive-in sem oxigênio após a pré-deposição de fósforo nos processos Screen-print e Getter padrões resultou em uma captura efetiva de ferro em ambos os processos. Foi observado também um aumento na uniformidade da concentração de dopantes ativos ao longo da superfície das amostras, que pode ser explicada pelo aumento do tempo que os átomos de fósforo tiveram para difundir na matriz de silício a elevadas temperaturas. O processo do tipo Screen-print modificado apresentou uma junção p-n mais profunda e uma maior concentração superficial de dopantes ativos. A junção mais profunda possui benefícios em relação ao processo de metalização, porém a maior concentração superficial de dopantes ativos aumenta os níveis de recombinação. Logo, o uso desse processo de difusão juntamente com um processo de *etch-back* homogêneo pode resultar em um emissor leve adequado para aplicações em células do tipo LDSE. Através de simulações realizadas no software EDNA 2 foi estimado que 100 nm devem ser removidos do emissor para que seja atingida a resistência de folha alvo de 100-120 Ω/sq para um emissor leve. O processo do tipo Getter modificado por outro lado não apresentou mudanças significativas no perfil de dopantes ativos após a adição da etapa de drive-in sem oxigênio. As medidas de ECV foram repetidas em outras amostras que passaram pelo mesmo processamento e os resultados foram os mesmos. Futuras análises incluindo a repetição do processo de difusão devem ser conduzidas a fim de entender o motivo pelo qual a profundidade da junção não aumentou e se o resultado não foi influenciado por erros no processo de difusão.

Efeito do etch-back no emissor frontral causado pelo processo de rear-etch

Apesar do processo de *rear-etch* ter realizado um *etch-back* no emissor frontal, o mesmo não atingiu a resistência de folha alvo em nenhum dos quatro processos de difusão utilizadas, e o *etch-back* realizado não foi uniforme. A uniformidade do processo foi determinada através da variação da concentração de dopantes ativos ao longo da superfície das amostras. O efeito do *etch-back* do emissor frontal na texturização das lâminas foi analisado através de medidas de reflectância após cada aplicação do processo de *rear-etch* e antes da camada anti-reflexiva de SiNx ser aplicada. Era esperado que a reflectância aumenta-se com o aumento do número de aplicações do processo de *rear-etch*, devido aos danos causados a superfície texturizada. Porém, ao observar o ponto mais baixo da curva de reflexão por comprimento de onda para o grupo de amostras que passou pelo processo de difusão do tipo Screen-print padrão pode-se notar que amostras que passaram pelo processo 1 e 2 vezes apresentam a mesma curva. Ao analisar as amostras que passaram pelo processo de difusão do tipo Getter padrão percebe-se que o menor ponto da curva diminui com o aumento do numero de vezes que o processo de *rear-etch* foi aplicado, enquanto para as amostras submetidas ao processo de difusão do tipo SP modificado apresentam um comportamento oposto. Logo, os resultados de reflexão obtidos suportam a ideia de que o *etch-back* do emissor frontal causado pelos gases liberados pelo banho químico no processo de *rear-etch* não é uniforme e não é indicado para a função proposta.

Conclusão

Os efeitos do processo de *rear-etch* no emissor frontal foram analisados e demonstram que apesar do processo ser realizado a temperatura ambiente, os gases originados pelo banho ácido resultam em um *etch-back* do emissor frontal, porém o ataque a superfície não é homogêneo e não é suficiente para remover a quantidade necessária da camada com altamente dopada.

A efetividade das receites de difusão de fósforo padrões utilizadas no SIRF na captura de fósforo foram testadas juntamente com dois processos modificados (onde houve a adição de uma etapa de drive-in em ambiente livre de oxigênio) e verificou-se que todos os processos com exceção do processo do tipo Screen-print padrão são eficientes na captura de ferro. O processo do tipo Screen-print modificado apresentou um aumento na profundidade do emissor formado e uma maior concentração de dopantes ativos na superfície e simulações realizadas no software EDNA 2 indicam que o emissor desejado pode ser obtido utilizando-se o processo seguido da remoção homogênea de 100 nm do emissor frontal.

Abstract

A lightly doped emitter can be manufactured through the formation of a heavy emitter diffusion followed by an homogeneous etch-back of the emitter. This route to form a light emitter is particularly interesting because it provides the extra benefit of phosphorus diffusion gettering (PDG) of metallic impurities, like iron. The possibility of using the rear-etch process to also perform an etch-back of the heavy diffused front emitter while removing the back emitter is analyzed in the present work, together with an analysis of the gettering efficiency of four different phosphorus emitter diffusion recipes. 156 mm x 156 mm pseudo-square Czochralski p-type silicon wafers with a bulk resistivity of 1.6 Ω.cm were used. The samples were textured by alkaline etching, RCA cleaned and then split in four groups and each group had the phosphorus emitter diffused through a different recipe. The standard Getter and Screen-print recipes used in the Solar Industrial Research Facility were used, together with two modified version of the recipes where an additional drive-in step without oxygen was added after the deposition step. After the emitter diffusions, the PSG layer formed was removed in a 2.5 % hydrofluoric acid solution and a few samples from each group were submitted to the rear-etch process 1, 2 and 3 times and then a 75 nm thick silicon nitride (SiNx) coating was deposited by plasma-enhanced chemical vapor deposition on both sides of all the wafers. The wafers were characterized in order to verify the their interstitial iron concentration before and after the fast-firing process and the effect of the rear-etch process in the front side emitter. Interstitial iron was only observed in the samples with a Screen-print diffusion. The extra oxygen-free drive-in added to the standard Screen-printing recipe resulted in a deeper junction and a higher surface concentration of active dopants, while the addition of the same drive-in step to the standard Getter diffusion didn't cause a significant impact on the formed junction. It was estimated through the EDNA 2 software that a 100 ηm etch-back of the emitter would

be necessary to reduce its sheet resistance from 24.7 to the target sheet resistance of 100 Ω/sq. Even though the rear-etch process did performed an etch-back of the front emitter it was not homogeneous, and not strong enough the reach the target sheet resistance even when the process was applied three times in a row, suggesting that the etch-back process is not suitable for the proposed application of etching back a heavily doped front emitter without adding an extra step to the manufacturing process.

Contents

Acknowledgements

So many things and people came to my mind when I was writing this section, making it the the most difficult section to write. First things first I would like to thank my parents José Carlos and Kátia for all the opportunities and support they gave to me since I was born. The present work and the completion of my Engineering degree is their merit, I just did the 'easy' part. Then, I would like to thank my friend Michael Budzon for the friendship and great support from him and his parents Mariola and Bronislav during my time in Australia, if it wasn't for you mate I wouldn't have got to Australia in the first place. My English vocabulary is still a bit limited, so it's quite difficult to express my feelings for Brett, Moonyong and Daniel. You guys gave me an opportunity that completely changed my life, in several aspects, for good. And the most important, you believed in me and gave me unconditional support in and outside the labs, even when I was breaking important samples or my nose. I will never forget the good times in Tyree building, and I will always be grateful for everything that I've learned with you guys. Moon, you were there when I needed the most and taught me to give value to the things that are actually valuable in our lives, and always pushed me to do my best. You are a inspiration for me mate, kimchi for you. Daniel, you were the greater teacher that I had during my entire degree (and you are not even an actual teacher yet). You were patient and happy to teach me anything I was interested in learning. I wish I could pay you back in choc-chip ganache muffins but not even all the muffins in the planet would make it even. Also, if it wasn't for you and your support (including exclusive LaTeX lessons) during the manufacturing of this thesis, it wouldn't exist. Thank you mate, for all the knowledge that you shared with me and for the great friend you are.. kimchi for you too. Brett, sometimes I still don't believe how great you were with me. You accepted to supervise me, and even with all the important things that you had to do around the globe (or

downstairs at the cafe) you were always happy to sit and listen to my confusing questions and give me the answers that I was looking for. You showed me that I can do something that not only makes me happy but also contributes to the future of our planet. I'm way too proud to say that I worked as your assistant, and I'll always be truly grateful for the lifetime (my lifetime, not the minority carrier one..) opportunity that you gave to me. Professor Arno, thank you for accepting to be one of my supervisors even from distance and for everything you taught me in the labs back in 2015 (when I was being introduced to solar). I would like to express my gratitude for Malcolm Abbott too, who was also part of my journey at SPREE and not only was co-supervising me but also served as inspiration of the kind of professional that I want to be. I couldn't finish this section without mentioning all the SIRF team, Ly Mai, Duc Huy Dao, Nino Borojevic, Fred Qi, Angus Keenan, Kyung Kim, who always assisted me with wafer processing and are incredible people who always made me feel at home when I was at SIRF. Also, I couldn't forget about the amazing people that I've met at SPREE and filled my days there with joy: Hongzao Li, Fung Tsun Hang, Bram Hoex (who let me attend his lectures and got me even more interested and motivated to study photovoltaics), Altaf Syed, Carlos Vargas, Jack Colwell and Alison Wenham (who assisted me with ECV measurements), Nitin Nampalli, Shaoyang Liu, Robert Largent, Wing Ki Kylie Chan, Khoo Kean Thong, Chloe Kim, Ned Western. You all made part of my journey at UNSW and made it special. Luiz and Wendy, you guys are awesome and I was very lucky to have you guys always there with me to share the good and the bad moments. Finally, I would like to say thank you to my brother Mateus (you are the best bro) and my homies who even from the other side of the globe supported me unconditionally.

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Chapter 1

Introduction

1.1 Motivation

In order to reduce the use of fossil fuels [1] to generate useful energy, the cost of energy generated through renewable sources needs to be reduced. The performance of solar cells has been increasing in the past decade and the cost of photovoltaics manufacturing has been decreasing as a result of increased material quality and fabrication methods. A way of reducing the price of energy generated through a photovoltaic device is to reduce the cost associate with materials. Thus, the use of lower quality (cheaper) substrates together with processing techniques that enhance their performance can result in cheaper energy. The quality of monocrystalline silicon wafers is significantly limited by the presence of impurities, and as the industry demands higher quality cheaper materials, newer processing techniques need to be implemented as a way to remove impurities[2].

1.2 Thesis objectives

During the phosphorus emitter diffusion from a gas phase on the p-type substrate the emitter is usually formed on the entire surface of the wafer (both sides and edges). When re-defining

the rear p-contacts, the front and rear side emitters can be isolated (edge isolation) or the residue emitter on the rear side can be either avoided or removed. To avoid or to remove the rear side emitter will give the same or even better results then the edge isolation process, so it can be used for edge isolation as well. Various edge isolation techniques are available for industrial production of screen printed solar cells [3], including mechanical and laser cutting. Mechanical edge isolation leads to a reduction in active cell area by 3 to 6% [4] for standard 125 x 125 mm^2 cells and produces waste silicon which can not be recycled. Apart from mechanical cutting, the plasma etching technique is one of the most used for edge isolation. Although it has a high throughput (the cost per wafer is quite low since several wafers are processed at the same time), however careful handling of the wafers is necessary and the waste gases produced by plasma etching are toxic and need to be filtered before disposal into the atmosphere. Konstanz University together with Rena developed an automated inline wet etching system which removes the rear side emitter [4]. In the process, wafers are transported through an acidic solution in a way that only the rear side of the wafers comes in contact with the etching bath and since the wafers don't need to be stacked the handling becomes a lot easier and the risk of damaging wafers is lower when compared to the other methods. The chemical bath is kept below room temperature to ensure almost no acidic vapors emission during the process, which could etch the front side emitter as well.

Traditional screen-printed solar cells require a high surface doping concentration to limit contact resistance [5] which results in a poor response to short wavelengths of light [6]. The Laser-doped selective emitter solar cell (LDSE) is a technology that overcomes the poor short-wavelength absorption by allowing the use of lightly doped emitter [7]. A way of achieving a lightly doped emitter is through the use a heavy emitter diffusion followed by an etch-back of the emitter. This route to form a light emitter is particularly interesting because it provides the extra benefit of phosphorous diffusion gettering (PDG) of metallic impurities like iron[8], which is detrimental to device performance.

Even though the rear-etch process used for edge isolation and rear emitter removal is conducted below room temperature to avoid the emission of acidic vapors, those vapors may still be emitted. This work studies the possibility of using the rear-etch process to perform not

only it's primary functions (edge isolation and rear emitter removal) but also as a gas-phase etch-back of the heavy diffused emitter on the front surface in the same process. Also, the efficiency of the two standard phosphorous diffusion gettering recipes used in the Solar Industrial Research Facility (SIRF) in gettering iron contaminants was analyzed, as well as the efficiency of two modified versions of the recipes where a oxygen-free drive-in step was added after the pre-deposition step.

1.3 Thesis outline

The present work consists in 6 chapters. In Chapter 1, the motivation behind this research, objectives and the outline is presented.

Chapter 2 contain the literature review; a overview of the impact of impurities in the silicon device, the effect and kinetics of iron in silicon, different cell technologies and emitter diffusion methods.

In chapter 3 the experimental method used to manufacture the samples used in this thesis is described, as well as the different emitter diffusion recipes, rear-etch process. The characterization methods and tools used throughout this work are briefly described.

The results obtained in the experiment are presented in Chapter 4. The effectiveness of the standard phosphorus diffusion recipes used in the Solar Industrial Research Facility is discussed. An evaluation of the improved heavy getter diffusion recipes that were tested are also presented and the effect of the rear-etch process in the etch-back of the front emitter is also analyzed.

Final conclusions were drawn In Chapter 5 based on the results presented in this work, and in Chapter 6 further experimental observations were outlined.

Chapter 2

Literature Review

2.1 Czochralski Monocrystalline Silicon

Monocrystalline silicon wafers represented around 35 percent of the total world market share in 2016 and will attain a share of 60 percent in 2027 [9] (Figure 2.1), mainly due to the tremendous progress in stabilizing p-type mono. In the manufacturing process, a seed silicon crystal is placed in a quartz crucible containing silicon just above its melting point. The seed is then pulled upwards with careful control of the temperature and rate of pull while rotating the ingot in order to produce large ingots of a round shaped single crystal material. Dopant atoms like phosphorus or boron can be added to the molten silicon to dope the material, resulting in n-type or p-type silicon. The use of quartz crucibles results in the contamination of the silicon ingot by different impurities like oxygen, which creates complexes with boron doping atoms that degrades the carrier lifetime [10]. Also, the melt crucible usually introduces iron in the silicon ingot.

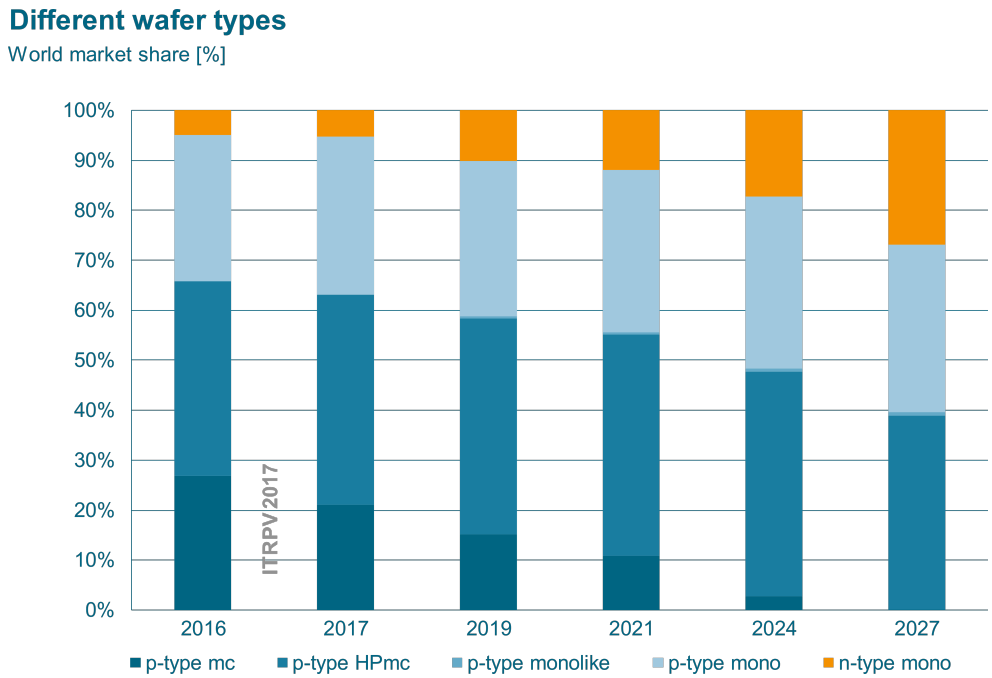

Figure 2.1: World market shares for different wafer types. Extracted from the International Technology Roadmap for Photovoltaics (ITRPV) , Eight Edition, 2017.

2.2 Impurities in Silicon Wafers

Impurities in silicon wafers are expected to influence the properties of solar cells in different ways [11]. For example, the growth of silicon crystals can be perturbed resulting in structural defects, and the bulk properties of the silicon wafer may be altered by electrically active impurity centers which reduce the minority-carrier diffusion length by increased recombination. Also, the presence of impurities may induce series or shunt resistance effects, precipitation and other junction defects mechanisms [12]. The impurities can be introduced in the wafer during different steps of the manufacturing process. In the manufacturing process of Czochralski monocrystalline silicon wafers a seed crystal is pulled out of molten silicon in a quartz crucible at temperatures above 1400 °C and impurities can thermally diffuse from the crucible into the silicon during crystal solidification [13].

2.2.1 Recombination

Any electron in the conduction band is in a meta-stable condition and will at some point stabilize to an empty valance band state, in a lower energy position. When this happens a hole is also effectively removed and this process is called recombination. Thus, both the electron and hole can participate in the conduction and are called carriers. The recombination mechanisms explain the forms os electron relaxation from the conduction band to the valance band. There are basically three recombination mechanisms that can occur in the bulk of a single-crystal semiconductor and together they can express the material's bulk minority carrier lifetime, according to the following equation:

$$\frac{1}{\tau_{bulk}} = \frac{1}{\tau_{rad}} + \frac{1}{\tau_{SRH}} + \frac{1}{\tau_{Auger}} \tag{2.1}$$

The three different recombination mechanisms that can occur in the bulk are briefly explained below:

Radiative recombination

An electron from the conduction band is directly combined with a valence's band hole releasing an photon, which has an energy similar to the band gap.

Auger recombination

When an electron and a hole recombine the emitted energy can be given to another electron in the conducted band, which is pushed high into the conduction band. This electron gradually releases it's energy thermally and goes back to the conduction band edge.

Shockley-Read-Hall recombination

Shockley-Read-Hall (SRH) [14] recombination occurs through defects and it is not present in pure perfect materials. It involves two steps. First, when a carrier (electron or hole) is relaxing from the conduction band it may become trapped in a energy state in the forbidden gap, which is introduced through defects in the crystal. Then, if another carrier with opposite

charge (electron or hole) moves up to the same energy state before the first carrier being re-emitted to the conduction band, they recombine.

Apart from the bulk of the material recombination also occurs in the surface of the solar cells. The defects at the surface are caused by the interruption of the crystal lattice's periodicity, which causes dangling bonds at the surface of the semiconductor. The high recombination rate in the surface depletes the region of minority carriers and a region of low carrier concentration results in a flow of carriers from the surroundings (higher concentration regions) to this region. Thus, the surface recombination rate is limited by the rate that minority carriers move towards the surface, and it's specified by a parameter called "surface recombination velocity". It's expressed in centimeters per second and for most semiconductors is on the order of 10^7cm/s. Reduction in surface recombination can be achieved by growing a layer on top of the semiconductor which ties up some of the dangling bonds.

2.2.1.1 Carriers

The intrinsic carrier concentration (n_i) is the number of electrons in the conduction band or the number of holes in the valance band of a material that has not had impurities added to it in order to change the carrier concentrations. It depends on the band gap of the material as well as the temperature. Doping is a technique used to change the number of holes and electrons in semiconductors and thus to increase the conductivity. The electrons/holes balance of a silicon crystal lattice can be shifted through doping with other atoms. N-type semiconductors are produced using atoms with one more valance electron than silicon (which is free to participate in the conduction, increasing the number of electrons). On the other hand, P-type semiconductors are produced using atoms with one less valence electron than silicon, which increases the concentration of holes in the material. In doped materials there's always more of one type of carrier than the other. The more abundant charge carriers are called majority carriers while the less abundant are called minority carriers and their product is a constant.

The total number of carriers in the conduction and valence band with no externally applied bias are called the equilibrium electron and hole carrier concentrations, respectively. The equilibrium carrier concentration of majority carriers is equal to the intrinsic carrier concentration plus the number of carriers added by the doping process. Usually the dopants concentration is several orders of magnitudes greater than the intrinsic carrier concentration so the majority carrier concentration is approximately equal to the doping.

The constant relation between majority and minority carriers at equilibrium can be expressed bt the Law of Mass Action:

$$n_0 \times p_0 = n_i^2 \tag{2.2}$$

Thus, the majority and minority carrier concentrations can be expressed as:

in n-type silicon:

$$n_0 = N_d \tag{2.3}$$

$$p_0 = \frac{n_i^2}{N_d} \tag{2.4}$$

and in p-type silicon:

$$p_0 = N_a \tag{2.5}$$

$$n_0 = \frac{n_i^2}{N_A} \tag{2.6}$$

Where:

- n_0 and p_0 are the electron and hole equilibrium carrier concentrations

- n_i is the temperature-dependent intrinsic carrier concentration
- N_D is the concentation of donor atoms
- N_A is the concentration of acceptor atoms

2.2.1.2 Lifetime

Even though lifetime is usually described by a single value parameter, it is a complex concept that changes according the doping level, injection of carries, illumination level and material quality. The term lifetime usually refers to the recombination lifetime of excess minority carriers, which is the average time that a carrier can spend in an excited state after electron-hole generation before it recombines.

As explained in the previous section, there are various recombination mechanisms even in a uniformly doped semiconductor. Radiative, Auger and Shockley-Read-Hall recombination of the carriers can be observed in the bulk of the material, and together they express the lifetime in the material bulk. The surface on the other hand complicates the measurement of the bulk lifetime due to it's important role in recombination. The recombination in the surface is described by a surface lifetime which depends on the surface recombination velocities (s1 and s2), the cell width and the minority carrier diffusivity. The combination of bulk and surface recombinations results in the effective lifetime of carriers (τ_{eff}) of a given sample.

$$\frac{1}{\tau_{\text{eff}}} = \frac{1}{\tau_{\text{bulk}}} + \frac{1}{\tau_{\text{surf}}} \tag{2.7}$$

The effective lifetime of carries of the samples used in this work were measured (in order to estimate the concentration of interstitial iron in the samples) through Quasi-Steady-State Lifetime measurements [20]. The QSSPC measurements rely on the number of carriers present in the semiconductor when it is exposed to a steady light, assuming that the intensity of the flash changes slowly enough to ensure that the carrier populations are always in steady state.

2.3 Iron in Silicon Wafers

2.3.1 Kinetics, detection and characterization of iron

Iron is one of the main metallic impurities in silicon devices. Due to it's considerable high solubility and fast diffusion at elevated temperatures iron is easily introduced into silicon during heat treatments [15]. In monocrystalline Czochralski silicon wafers iron is usually introduced by the melt of the crucible in the ingot growth process and the sawing process. In crystalline silicon wafers, iron contamination results in the creation of recombination centers which reduce the minority carrier diffusion length and thus the solar cell efficiency [16]. Iron diffuses interstitially in silicon [17] [18] and it is mobile even at room temperature. In p-type silicon interstitial iron can exist in different forms, but it's usually found in it's positively charged state, in which it forms pairs with negatively charged defects like shallow acceptors. At room temperature and together with negatively charged substitutional Boron iron tends to form FeB pairs. The equilibrium of the point-defect reaction between Fe_i^+ and B_s^- depends on the temperature and the boron concentration. At room temperature and boron concentration greater the $10^{14}\ cm^{-3}$ all the iron is bounded with substitutional boron in equilibrium [19]. The dissociation of the FeB pairs into positively charged interstitial iron and negatively charged substitutional boron occurs when energy is supplied through illumination, minority-carrier injection or thermal processing [21] and the relaxation of dissociated interstitial iron back into an FeB pair has been observed when kept in the dark for less the 12 hours even at room temperature [22].

Quasi Steady State Photoconductance (QSSPC) measurements can be used to estimate the interstitial iron concentration due to its influence on minority carrier lifetime. In its interstitial form, iron is an effective center for Shockley-Read-Hall recombination, increasing the minority carrier lifetime in high injection levels [23]. When comparing the minority carrier lifetime vs. excess carrier concentration curves before and after iron dissociation from FeB pairs to Fe_i a cross-over point near an excess carrier concentration of $1.2 \pm 0.6 \times 10^{14}\ cm^{-3}$ [21] characteristic

from iron can be observed.

Based on the fact that interstitial iron undergoes a reversible pairing reaction with substitutional boron and that the minority carrier lifetime is modified by this reaction Zoth and Bergholz developed a method to quantify the iron concentrations. A simplified approach of the method can be made through QSSPC, where the low-injection carrier lifetimes (τ_{FeB} and τ_{Fe_i}) are measured at the same injection level and through the Equation 2.8 the interstitial iron concentration can be estimated. C is an injection level and dopant concentration dependent proportionality coefficient [19], and the lifetime measurements are taken at an injection level of 9.1 x 10^{14} cm^{-3} [24].

$$[\mathrm{Fe}_i] = A \times \left(\frac{1}{L^2_{Fe_i}} - \frac{1}{L^2_{FeB}} \right) = C \times \left(\frac{1}{\tau_{Fe_i}} - \frac{1}{\tau_{\mathrm{FeB}}} \right) \tag{2.8}$$

Precipitated iron (which can be present in the iron silicide form $\beta - \mathrm{FeSi_2}$) on the other hand cannot be detected through lifetime techniques and can be released during thermal processes like firing. Therefore, the iron detection and characterization is realized after the SiN deposition (before firing) and after firing as well in order to determine the amount of interstitial iron present in the finished device.

2.4 Screen-printed and Laser Doped Selective Emitter solar cells

Screen-printed solar cells were first developed by Spectrolab in the late 1970s [25]. In screen-printed solar cells both front and rear metal contacts are formed by printing metal pastes on the surface of the silicon wafer according to a pattern formed in a screen, followed by an appropriate firing step in order to form: the rear Back Surface Field (BSF) as well as an ohmic contact between the front silver paste and the front surface emitter. The contact resistance between the metal contacts and silicon is high, and it depends of the firing conditions

and surface doping [25]. The surface doping concentrations have to be high to limit contact resistance and the junction needs to be deep enough to avoid the penetration of the metal contact through the p-n junction during the subsequent firing [5]. Heavily-doped emitters have a poor response to short wavelength light and thus have lower efficiencies. The laser-doped selective emitter (LDSE) solar cell structure allows the use of lightly doped emitters to avoid the loss of current due to a poor short wavelength response of standard screen-printed solar cells, resulting in higher voltages on finished devices [7]. The selective emitter structure also permits a good passivation of the front surface, a low contact resistance and also reduces the front surface recombination losses [26].

2.5 Emitter Diffusion

In order to obtain current from a solar cell, the electrical charged carriers generated by the absorption of photons in the silicon by the silicon must be separated. The separation can be done through the formation of a p-n junction in the silicon wafer, so the electrons can be collected in the n-type region while the holes are collected in the p-type region of the device due to the electric field formed at the junction. Since most of the crystalline silicon solar cells are manufactured using p-type silicon wafers, a n-type layer must be formed in order to create the p-n junction. The process of creating a n-type surface layer can be performed in diferent ways. Usually the n-type layer is formed throught the solid state diffusion of phosphorus at high temperatures, creating a layer where the concentration of the n-type diffused phosphorus dopant atoms is a lot greater than the p-type boron dopant atoms (usually 10^{19} to 10^{21} n-type dopant concentration versus 10^{15} to 10^{16} p-type dopant concentration). The process is conduced at high temperatures (usually between 800 °C and 900 °C) in order to ensure that enough phosphorus atoms penetrate into the bulk of the silicon wafer. There are a few different ways of performing the diffusion process. The two most common processes are the tube furnace process and the inline furnace process. Both of they rely on forming a phosphosilicate glass (PSG) layer which provides the phosphorus that at high temperatures is diffused into the bulk of the silicon wafer. In the first method, phosphoryl chloride ($POCl_3$) is

injected into the furnace tube as a vapour which at high temperature reacts forming the PSG layer. On the other hand, in the inline furnace process the silicon wafers are usually coated with phosphoric acid (H_3PO_4) and then conveyed through the different heating zones of the inline furnace where the PSG layer is formed. The n-type surface layer formed through the diffusion process is known as emitter. Due to the evolution of solar cell technology frequent revaluation of the process is necessary, specially to form high-performance emitters.

2.5.1 Conventional Phosphorous Diffusion Gettering

$POCl_3$ diffusion is a well-established and reliable high-throughput process to form p-n junctions on p-type silicon wafers [27]. Phosphorous diffusion using $POCl_3$ as a precursor in a tube furnace results in cells with a better performance when compared to the belt diffusion due to a more uniform active dopants concentration over the silicon surface and a getter effect of metallic impurities [28]. During the process, O_2 reacts with $POCl_3$ and forms P_2O_5 on the surface of the silicon at the same time that the surface is oxidized by the oxygen, resulting in the formation of a complex of silicon oxide and P_2O_5 (known as phosphor-silicate glass or PSG) over the silicon surface. The PSG layer provides elemental phosphorus for the diffusion by reacting with silicon. N_2 is also used in the process as a carrier gas.

$$4\,POCl_3(g) + 3\,O_2(g) \longrightarrow 2\,P_2O_5(l) + 6\,Cl_2(g)$$

$$2\,P_2O_5(l) + 5\,Si\,(s) \longrightarrow 5\,SiO_2(s) + 4\,P\,(s)$$

Chapter 3

Experimental procedure

3.1 Lifetime structure fabrication

The samples used in this work consisted in 156 mm x 156 mm pseudo-square Czochralski p-type silicon wafers with a bulk resistivity of 1.6 Ω.cm. They were textured by alkaline etching in order to create upright random pyramids, and then were submitted to RCA cleaning before being divided in four different groups to be submitted to different diffusion processes. After the diffusion was performed, the PSG layer formed was removed in a 2.5 % hydrofluoric acid solution and a 75 nm thick silicon nitride (SiNx) coating was deposited by plasma-enhanced chemical vapor deposition on both sides of the wafers. These samples containing symmetrical n^+pn^+ structure are referred as lifetime samples, because they permit us to extract sample minority carrier lifetimes as well as iron concentrations through quasi steady state photo-conductance measurements. An schematic diagram of a lifetime structure is shown in Figure ??.

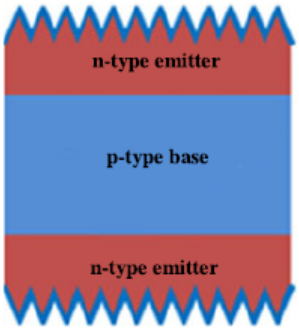

Figure 3.1: Schematic diagram of a symmetrical lifetime structure (not to scale). Extracted from Li et al [27].

3.2 Phosphorus Diffusion

POCL3 diffusion is a well-established and reliable high-throughput process to form p-n junctions on p-type silicon wafers [27]. Different diffusion recipes are used for different cell technologies in order to obtain the desired emitter properties. In this work, two primary different recipes were studied: the standard SIRF Screen-Print diffusion, the standard SIRF Getter Diffusion. Modifications of these base recipes were tested for their gettering performance. All the processes were performed in a Tempress Diffusion Furnace.

3.2.1 Screen-print Diffusion

Screen-printed solar cells usually use an homogeneous diffusion to form the emitter. The standard Screen-printed Diffusion recipe is used to form an emitter with a high surface doping concentration. At the first stage of the Standard screen-print diffusion, the PSG layer was deposited for 28 minutes at 782 °C. Then, the temperature was ramped to 892 °C for the subsequent drive-in step, with a ramp rate of 10 °C/min. The drive-in step lasted 30 minutes and the temperature was then reduced to 770 °C before unloading. The gas rates used during the whole process are show in the Table 3.1.

It is known that the O_2 concentration during the drive-in step strongly impacts the emitter and cell performance. Increasing O_2 concentration during the drive-in step produces shallower junctions and lower surface doping concentrations [27], so in order to investigate the formation of a deeper junction and a higher surface phosphorus concentration an oxygen-free drive-in step was performed in another set of samples.

The deposition and cool down steps parameters were the same, although the ramp up and drive-in steps were different. The ramp up had the same gas flow in both recipes, but the ratio between O_2 and N_2 was different. The standard Screen-print had 2 slm of N_2 and 5 slm of O_2, while the modified recipe had 7 slm of N_2 only. The drive-in step had 2.5 slm of N_2 in both recipes, while the standard recipe had also 5 slm of O_2 and the modified recipe didn't have any oxygen flow.

3.2.2 Getter Diffusion

The standard getter diffusion was developed to perform a more effective getter of impurities then the standard screen-print process is able to. The PSG deposition process was conducted at 851 °C for 45 minutes followed by a cooling step of 10 °C/min before unloading at 750 °C.

A modified version of the standard getter recipe was also developed and applied to a forth set of samples. The modified version had the addition of a oxygen-free drive-in step as well. The ramp up and drive-in steps had the same parameters as the ones used on the modified screen-print diffusion, except for the drive-in temperature which was 862 °C.

Table 3.1: Diffusion recipe gas flow configurations and parameters during various steps for (a) gettering recipe (b) screen-print emitter recipe.

Gas flows in standard liters per minute (slm)		**(a) Getter**		**(b) Screen-print**	
		Standard	**Modified**	**Standard**	**Modified**
$POCl_3$ Deposition	N_2	6.5	7.5	7.5	7.5
	N_2-POCl_3	0.6	0.6	0.6	0.6
	Total	7.1	8.1	8.1	8.1
Ramp up	N_2	-	7	2	7
	O_2	-	0	5	0
	Total	-	7	7	7
Drive-in	N_2	-	2.5	2.5	2.5
	N_2-POCl_3	-	0	0	0
	O_2	-	0	5	0
	Total	-	2.5	7.5	2.5
Cool	N_2	7.5	8.2	8.2	8.2
	O_2	0	0	0.1	0
	N_2-POCl_3	0	0	0	0
	Total	7.5	8.2	8.3	8.2

3.3 Rear-etch process

In the rear-etch process, the wafers were transported with an array of rollers through an etching solution containing hydroflouric acic (HF), nitric acid (HNO_3) and acetic acid (CH_3COOH). The chemical bath was filled up to a certain level to permit that only the rear side of the wafers was contacting the etching solution. The process parameters and listed below:

Bath temperature: 25 °C

Transport velocity: 1.3 m/min

Bath concentration: HNO_3 (70%), HF(49%) and CH_3COOH (glacial) at a volume ratio of 6.1 : 1 : 0.64.

In order to analyze how the rear-etch process etches back the front emitter, different wafers from each diffusion group were submitted to rear-etch process 1, 2 and 3 times.

3.4 Firing

The last step when manufacturing screen-printed silicon solar cells is the metallization firing in a belt furnace in order to form not only the rear aluminium electrode and back surface field (BSF) but also to enable the front-side silver past to etch the SiNx layer to form an ohmic contact to the n-type emitter. Firing is the last thermal process in the manufacturing of SP solar cells and during the process the cells experience a peak temperature in the range of 700 - 900 °C for approximately 2 to 3 seconds. The peak temperature depends of the emitter and silicon nitride antireflection coating properties as well as the type of paste used. In the present work only lifetime samples were prepared, not cells, but all the samples were fired in order to evaluate the possible release of iron from precipitates into its interstitial form after the thermal process.

The samples were fired in a belt furnace at a set peak temperature of 830 °C and a belt-speed of 4.5 m/s. After the process, the samples were left in the dark at room temperature for at least three hours in order to dissociate all the FeB pairs into interstitial iron and substitutional boron and then the concentration of interstitial iron was determined once again trough the QSSPC technique.

3.5 Characterization

The properties of the emitter formed with the diffusion process can be characterized through the measurement of the depth of the p-n junction, the sheet resistance of the phosphorus doped layer and also the phosphorus dopant profile in the silicon wafer.

3.5.1 Quasi Steady State Photo-conductance

The minority carrier lifetime of the samples was measured in different steps of the experimental procedure with a Sinton WCT-120 QSSPC bridge in order to determine the bulk and effective lifetime which enabled the extraction of interstitial iron concentrations. The Sinton bridge sensor region has a radius of 15 mm and 9 measurements were performed equally spaced across the wafer in order to evaluate the homogeneity of the processes that the samples were submitted as well as the distribution of iron across the wafers. Measurements were taken at both low injection levels with a peak illumination of 12 suns and high injection levels with peak illumination of 60 suns in order to enable the extraction of iron at the injection level of $\Delta n = 9.1 \times 10^{14}\ cm^{-3}$ (to stay away from the cross over point) and the extraction of J_{0E} at the injection level of $\Delta n = 1 \times 10^{16}\ cm^{-3}$, to minimize possible influences of SRH recombination.

3.5.2 Photoluminescence Imaging

The photoluminescence (PL) imaging [29] produces a spatially resolved visual representation of the wafer's performance. In this work, PL imaging was used to identify the presence of damaged areas after the rear-etch process. All the PL images were taken by a BTImaging LIS-R1 tool and PLPro software was used to correct photon smearing through the use of a point spread function [30]. An example of a PL image is shown in Figure ??.

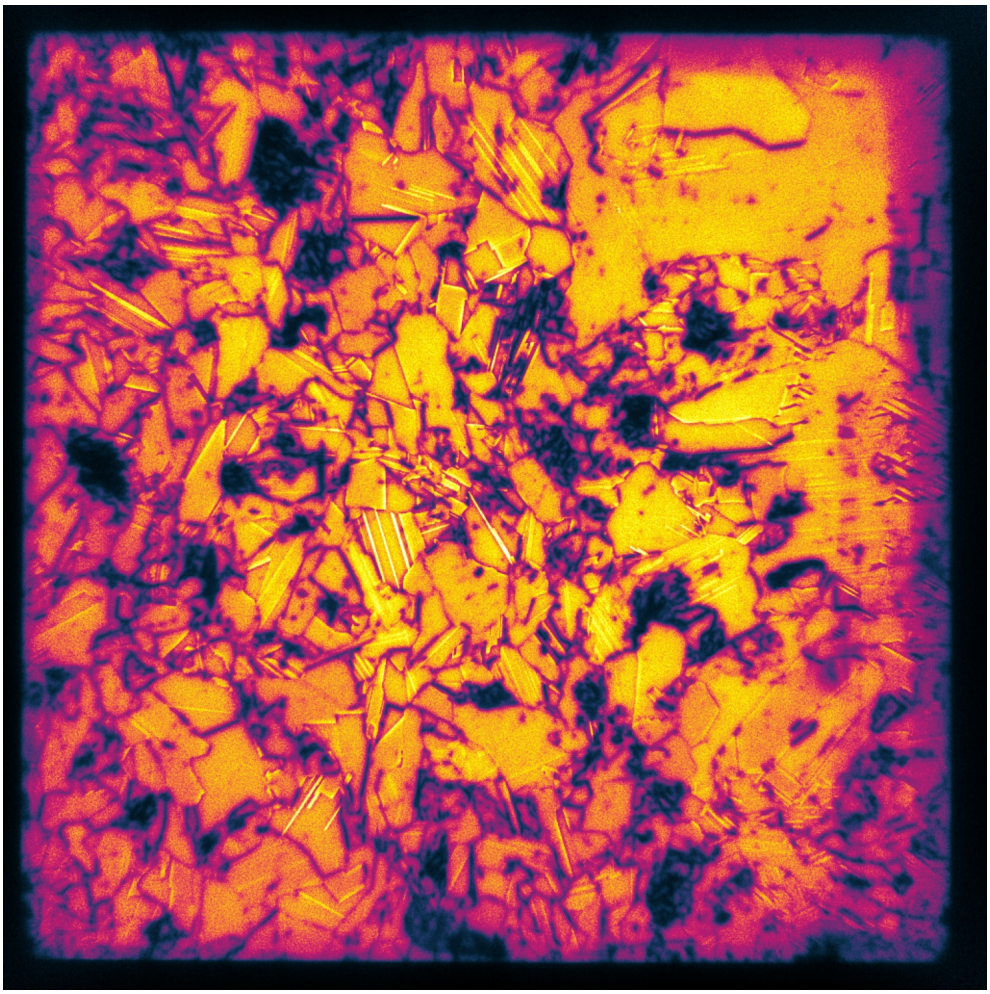

Figure 3.2: Example of a photoluminescence image taken of a multicrystalline silicon wafer prior to fast-firing. Darker regions show areas of locally higher relative non-radiative recombination whilst brighter regions show areas of greater radiative recombination.

3.5.3 Optical Reflection

Reflectance measurements were used to evaluate the effect of the etch back process on the texturing of the wafers. The measurements were taken with a Perkin Elmer Lambda 1050 UV/VIS/NIR spectrometer from 300 nm up to 1100 nm. This spectral range was chosen in order to cover the interval (350 to 1050 nm) where essentially every photon entering the solar cell is absorbed and creates an electron-hole pair. [31]

3.5.4 Sheet Resistance

In order to characterize the emitter phosphorus concentration, sheet resistance measurements were performed after the diffusion process as well as after the subsequent rear etch steps. The measurements were made using a Sherescan 2.0 tool in 49 equidistant points across the wafer's surface in order to analyze the uniformity of the diffusions.

3.5.5 Electrochemical Capacitance-Voltage

Electrochemical Capacitance Voltage (ECV) measurements were performed to obtain the doping profile into the wafer and the depth of the p-n junction. A CVP21 wafer profiler tool was used. Samples were prepared using a short hydrofluoric acid dip prior to characterisation. The samples spot size for the ECV measurement has an approximate diameter of 5 mm.

Chapter 4

Results and Discussion

4.1 Effectiveness of Standard Screen-Print and Getter diffusions in gettering iron

As explained in the previous chapters, interstitial iron is one of the main metallic impurities in silicon photovoltaic devices and contamination by iron can reduce the efficiency of solar cells. The effectiveness of the standard Getter and SP diffusion recipes in gettering iron was determined by the means of QSSPC measurements. Control samples without any PDG process had their interstitial iron concentrations determined (Figure 4.1) in order to quantify how much iron was contained in the samples before the gettering processes.

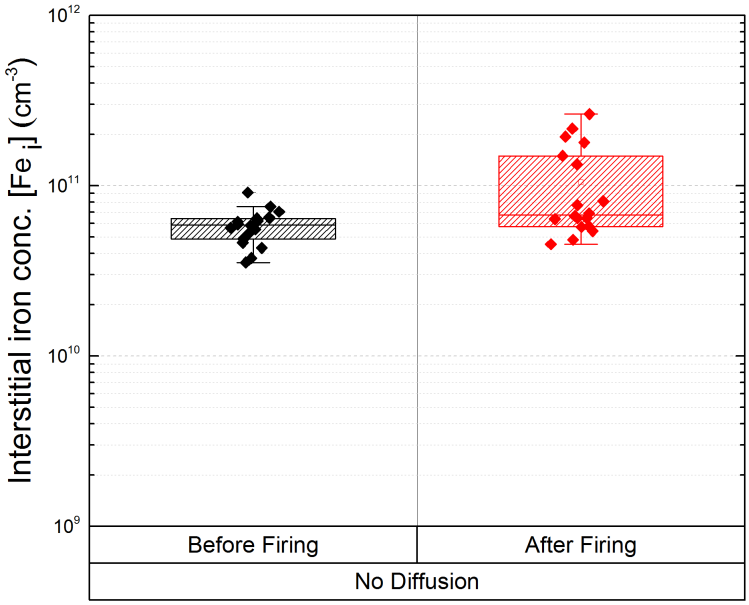

Figure 4.1: Interstitial Iron concentration on ungettered Czochralski grown monocrystalline silicon wafers before (black) and after (red) fast-firing processes.

The measurements performed in 9 points evenly distributed across the wafers surfaces did not show any increase in the effective lifetime of the samples that had the standard getter diffusion after a 10 seconds light soak at approximately 1 sun and room temperature, showing that there if there was any iron contaminating the samples it was present in concentrations below the detection limits (10^9 cm^{-3}). The presence of interstitial iron was not observed even after the firing process that could have dissolved iron precipitates in the bulk of the wafer.

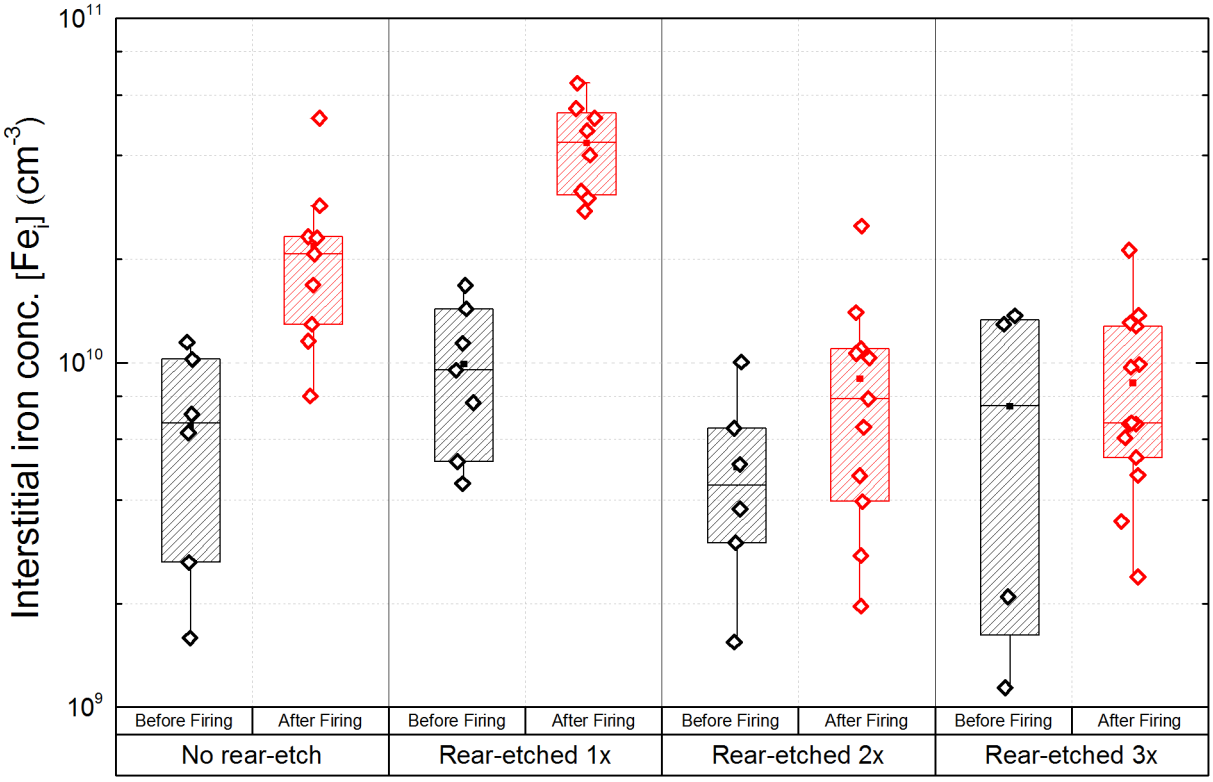

Figure 4.2: Interstitial Iron concentration on Czochralski grown monocrystalline silicon wafers with Screen-print emitter diffusion before and after multiple rear-etch steps.

Before firing, the samples that had the standard screen-print diffusion showed lower interstitial iron concentration when compared to the non-diffused samples. However, after the thermal process iron concentrations between 10^{10} and 10^{11} were observed, due to the dissolution of iron precipitates during the high temperature step. The minority carrier lifetime versus minority carrier density curves before and after suppling energy through illumination of a sample that had the standard screen-print diffusion and then fired are show in Figures 4.3 and 4.4. The cross-over point close to the injection level of 10^{14} is observed after firing, providing further evidence that interstitial iron was released into the bulk of the wafer during the thermal process.

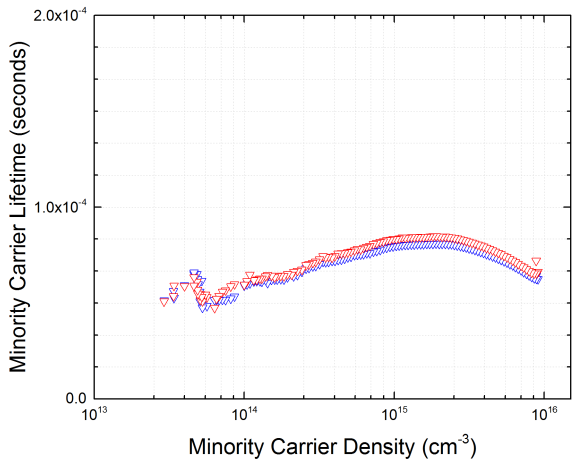

Figure 4.3: Minority Carrier Lifetime versus Minority Carrier Density curve of a unfired Czochralski grown monocrystalline silicon wafer that had the standard SP emitter diffusion, before (blue) and after (red) a 10 seconds light soak in 1 sun and 25 °C. Measured by QSSPC.

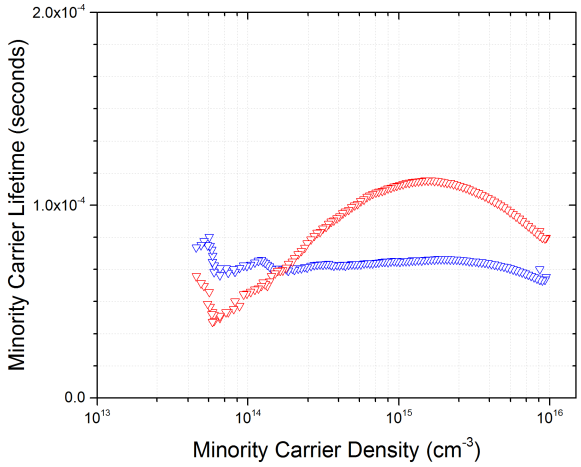

Figure 4.4: Minority Carrier Lifetime versus Minority Carrier Density curve of a Czochralski grown monocrystalline silicon wafer that had the standard SP emitter diffusion and was fired, before (blue) and after (red) a 10 seconds light soak in 1 sun and 25 °C. Measured by QSSPC.

In both cases the emitter was not removed after the phosphorus diffusion, which would have externally gettered all the iron accumulated in the phosphorus rich layer by physically removing it. Since the gettering process involves three steps [32] where the first one is to release the metallic impurities from their precipitated form, the second is the diffusion of them to the gettering region and the last one is the capture of the defects in the gettering

sites, a possible explanation for the fact that only the standard screen-print recipe released interstitial iron after the firing step is that during the diffusion process iron was able to diffuse more effectively to the gettering layer due to the higher temperature used in the recipe (which increases it's diffusivity) and also due to the longer duration of the process (60% longer). Furthermore, the greater gettering efficiency can be related to the third step of the gettering mechanism, where the emitter (which has a higher concentration of phosphorus when compared to the standard screen-print emitter) worked as an more effective external gettering layer, where the excess phosphorus on the surface can trap the metallic impurities from the bulk silicon and immobilizes them near the top emitter surface [28] [33]. This hypothesis is supported by the fact that iron silicates are dissolved at 760 °C, so the first step of the gettering process should not be the step which is limiting the efficiency of gettering, because all the precipitated iron should have been dissolved during the emitter diffusion process.

4.2 Improved heavy getter diffusions

The addition of the oxygen-free ramp-up and drive-in steps to the standard diffusion recipes resulted in a effective gettering of iron in both of them. An increase in the uniformity of the active dopants concentration across the wafer's surface was also observed in the modified recipes. The uniformity was determined dividing the average sheet resistance of each wafer by its standard deviation and the results are shown in Table 4.1. The increase in uniformity can be explained by the longer time that phosphorus atoms had to diffuse into the silicon matrix at a higher temperature.

Table 4.1: Average Sheet Resistance on the wafer's front surface after emitter diffusion for the four different Phosphorus Diffusion Gettering recipes used in this work.

Recipe	**Average SR** (Ω/sq)	**Standard deviation** (Ω/sq)	**SD / Average SR** (%)
Getter	42.8	0.8	1.86
Modified Getter	35.4	0.4	1.12
SP	57.9	4.1	7.08
Modified SP	24.7	0.5	2.02

For the screen-print recipe, the absence of oxygen during the ramp-up and drive-in steps resulted in a deeper junction and a higher surface concentration of active dopants. The ECV measurements are shown in Figure 4.5.

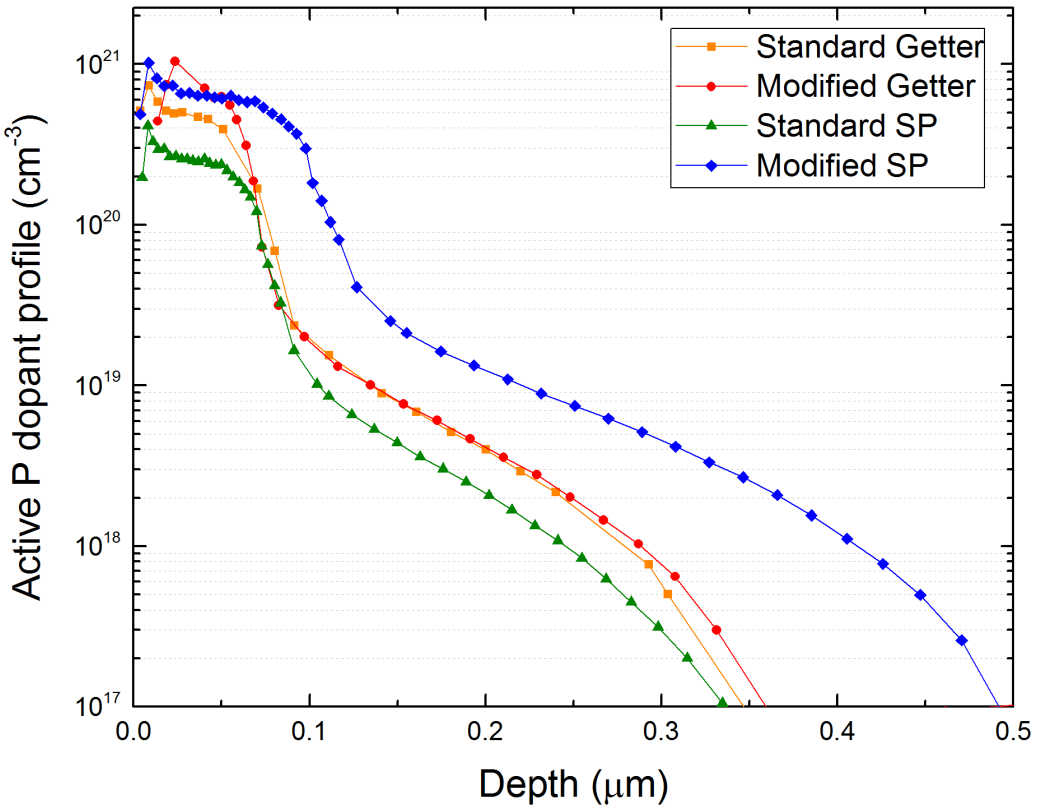

Figure 4.5: Electrochemical capacitance voltage measurements for the active phosphorus dopant profile after application of various diffusion processes.

The sheet resistance decreased from to 57.9 to 24.7 Ω/sq without the presence of oxygen during drive-in, due to the increase of the active dopants concentration as we can see in the increase of the area under the doping profile curve. The deeper junction as benefits regarding the metalization process, as it reduces the possibility of shunt formation [34], but the greater surface dopant concentration increases the recombination level. The electrical recombination properties were analyzed through QSSPC measurements on fired (SiNx) passivated lifetime structures. The average J_{0E} increased from 69.72 to 228.95 fA/cm^2 without oxygen during the drive-in step. This increase could be attributed to the increase in Auger recombination

due to the increase of active dopants and the increase in emitter SRH recombination due to increase of inactive dopants [35]. This is undesirable for solar cells.

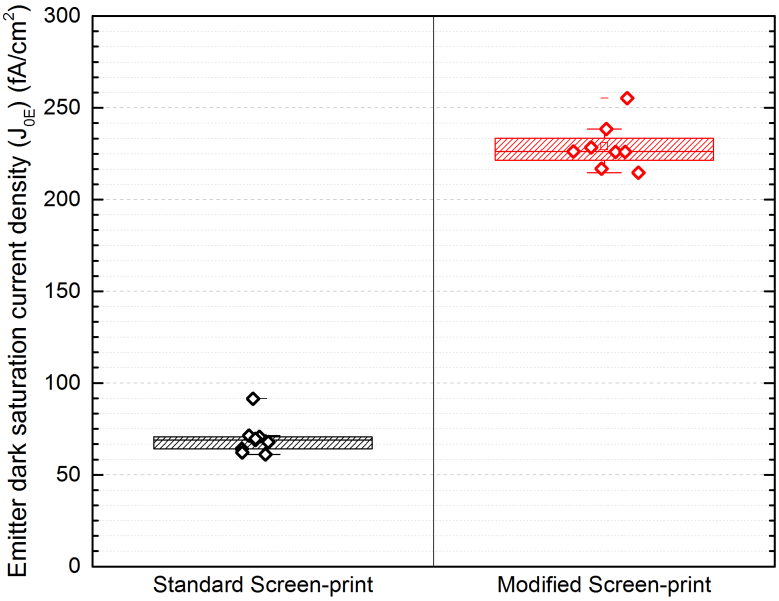

Figure 4.6: Emitter dark saturation current density of wafers that had the standard SP emitter diffusion (left) and modified SP emitter diffusion (right).

Therefore, the use of this phosphorus gettering diffusion recipe together with a more efficient emitter etch-back process could result in a decent lightly doped emitter for LDSE applications with the benefit of iron gettering. Simulations performed on the EDNA 2 software were used to estimate how much of the emitter would need to be etched back in order to achieve the target sheet resistance of 100 - 120 Ω/sq for a lightly doped emitter [36] and what would be the doping profile, emitter dark saturation current density (J_{0E}) for that scenario. It was estimated by the software that by removing 100 nm of the front emitter its sheet resistance in equilibrium would be 118 Ω/sq with a J_{0E} of 17.9 fA/cm^2. The simulated active phosphorous dopant profile after the proposed etch-back is shown below:

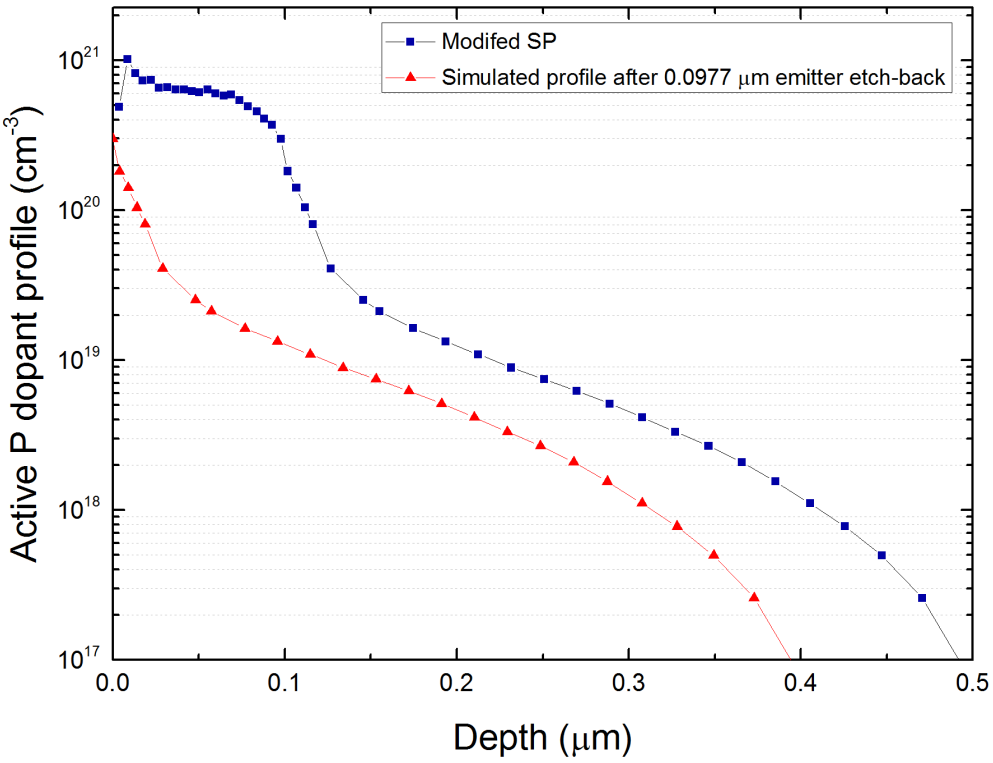

Figure 4.7: Electrochemical capacitance voltage measurements for the active phosphorus dopant profile after application of the modified SP diffusion process and the simulated doping profile after a 0.0977 micrometers emitter etch-back.

The getter recipe's doping profile on the other hand was not significantly affected by the addition of a drive-in step before cool-down. The depth of the junction was essentially the same, and just when zooming into the fist 10 nm micrometers an increase in the active dopants concentration can be seen. Therefore, a minor decrease in sheet resistance was observed (from 42.8 to 35.4 Ω/sq). It was expected that the addition of a drive-in step would drive in the emitter deeper in the wafer. The ECV measurement was repeated in other samples with the same processing conditions and the same result was obtained. Further analyzes should be carried out to investigate the reason why the depth of the emitter did not increased with the drive-in step and the diffusion process should be repeated to check if the it was not caused by an error in the process.

4.3 Effect of the etch-back on the front emitter caused by the rear-etch process

Even though the rear-etch process did performed an etch-back of the front emitter as we can see in the sheet-resistance results in table 4.2, it did not reached the target sheet-resistance of a lightly doped emitter of 100 - 120 Ω/sq [36] in any of the four different diffusion recipes. Also, the process etched the front surface of the wafers non-uniformly. The uniformity of the etching process was determined through the variation of the active dopants concentration uniformity on the front surface of the wafer, by dividing the average sheet-resistance of each sample by its standard deviation. The level of non-uniformity increased with the number of etches.

Table 4.2: Average Sheet Resistance on the wafer's front surface after application of four different diffusion processes with and without rear-etch steps.

	Average SR (ohm/sq)	**Standard deviation (ohm/sq)**	**SD / Average SR (%)**
Getter			
No rear-etch	42.8	0.8	1.86
1× *rear-etch*	49.7	1.2	2.41
2× *rear-etch*	60.8	5.8	9.53
Modified Getter			
No rear-etch	35.4	0.4	1.12
1× *rear-etch*	40.5	1.6	3.95
2× *rear-etch*	48.7	3.8	7.80
SP			
No rear-etch	57.9	4.1	7.08
1× *rear-etch*	73.9	4.3	5.81
2× *rear-etch*	84.8	6.1	7.19
Modified SP			
No rear-etch	24.7	0.5	2.02
1× *rear-etch*	27.5	0.7	2.54
2× *rear-etch*	31.7	1.9	5.99

The effect of the emitter etch-back on the texturing of the wafers was analyzed through reflectance measurements after the rear-etch steps, before the SiNx anti-reflection coating was applied. It was expected that the reflection would increase with more etching steps added to

the process, since the textured surface would be damage in the process. But when observing the lowest point of the optical reflection versus wavelength curve of the Standard Getter group of samples we can see that the sample that was rear-etched two times has lower reflection that the non-etched sample, while the one etched three times has higher reflection at that point. Also, when looking the Standard Screen-Print group we can see that the samples etched once and twice have the exact same curve. The lowest point of the reflection curve for the Modified Getter group of samples decreased with every etching step, while for the Modified Screen-print group it increased with one and two etches but showed a lower reflection when submitted to the rear-etch process three times. The optical reflection results support the idea that the etch-back of the front emitter caused by the gases from the rear-etch bath is not uniform and not reliable for the proposed function.

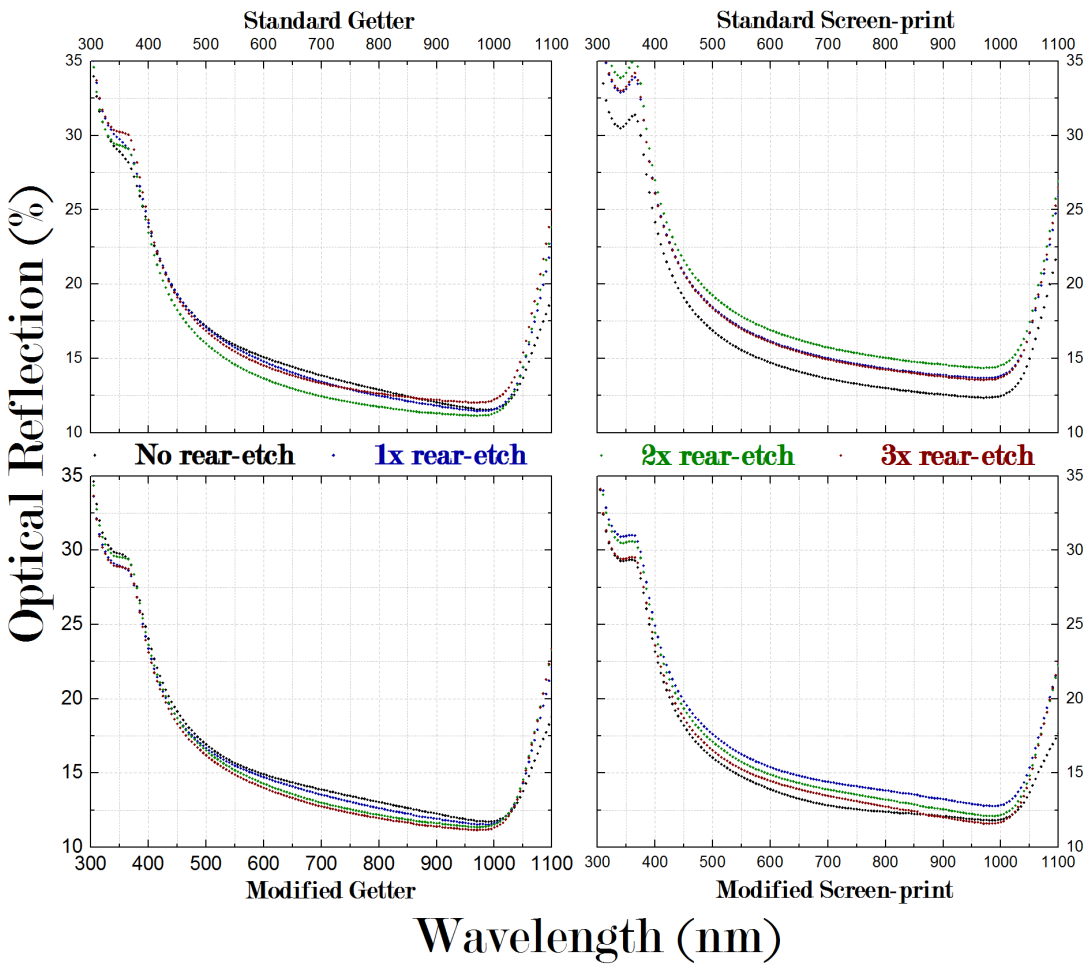

Figure 4.8: Optical reflection on the wafer's front surface after application of different diffusion processes with and without rear-etch steps.

The effective carrier lifetimes of the samples before and after the rear-etch process are displayed in figures 4.12, 4.9, 4.10 and 4.11 below. It is understood that solar cells require the entire wafer as the active region and any damage or extrinsic gettering methods left on the wafer may reduce the finished device performance [37]. An increase in the variance of the effective minority carrier lifetimes between different spots in the same wafer are observed after every etch step. The same behavior was observed in all the different groups, with the effective minority carrier lifetime varying from approximately 145 to 220 μs in the same wafer after it had the standard screen-printing diffusion and was fired, while the J_{0E} varied from approximately 74 to 56 fA/cm^2 suggesting that the change in effect lifetime is due to a defect

in the bulk of the wafer. This was confirmed by the difference in bulk lifetimes measured to be 354 μs and 685 μs respectively for the two locations.

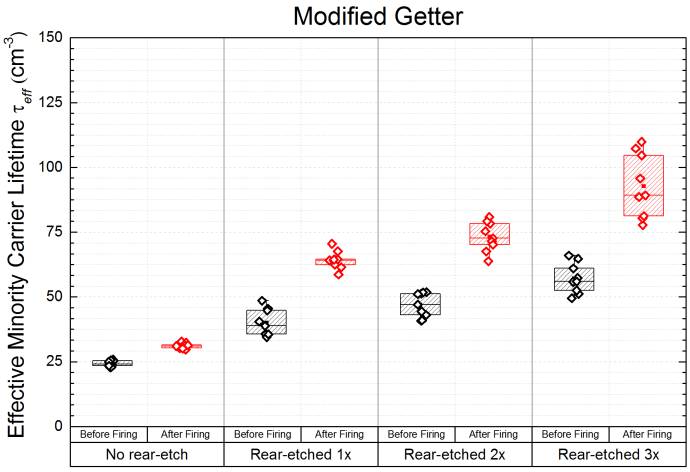

Figure 4.9: Effective Minority Carrier Lifetimes extracted at the injection level of $\Delta n = 9.1 \times 10^{14}\ cm^{-3}$ from Czochralski grown monocrystalline silicon wafers after the application of the modified getter diffusion and multiple rear-etch steps.

It is also understood that Auger recombination occurs commonly in highly doped materials [38], so the removal of the phosphorus rich layer with the rear-etch steps could be reducing the Auger recombination and thus increasing the effective lifetime. The fact that some regions of the wafer had a greater increase in lifetime than others could be attributed to a non-homogeneous etch-back of the front emitter caused by the solution's gases or due to damage left on the wafer the rear-etch steps.

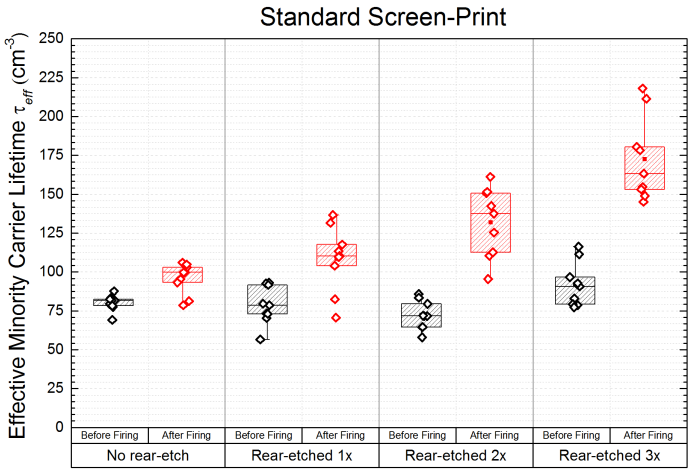

Figure 4.10: Effective Minority Carrier Lifetimes extracted at the injection level of $\Delta n = 9.1 \times 10^{14}\ cm^{-3}$ from Czochralski grown monocrystalline silicon wafers after the application of the standard SP diffusion and multiple rear-etch steps.

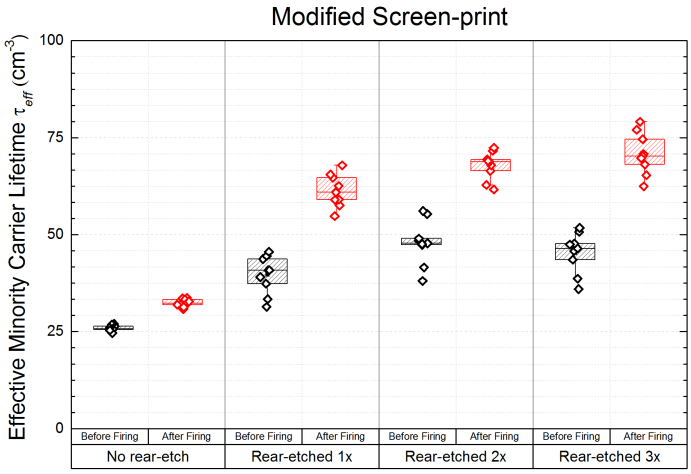

Figure 4.11: Effective Minority Carrier Lifetimes extracted at the injection level of $\Delta n = 9.1 \times 10^{14}\ cm^{-3}$ from Czochralski grown monocrystalline silicon wafers after the application of the modified SP diffusion and multiple rear-etch steps.

Finally, photoluminescence images showed that after the rear-etch processes the wafers had darker spots spread on their surfaces, which increased in size and number with subsequent rear-etches. These spots are frequently observed on the wafer's surface when the rear-etch bath is contaminated with impurities released by wafers that were previously processed in the same tool. Three other observations can be made from these photoluminescence images:

minor damage marks are present, saw damage lines (which can be masked by the diffusion) on the rear-etched wafers and also brighter regions on the wafers surfaces after the rear-etch steps that support the idea that some regions had a greater emitter etch-back caused by the chemical bath gases than others. At this stage, it is unclear on the actual impurity involved and the depth of the contamination in the wafer. This may require defect etching to determine the location of the defects.

The photoluminescence images presented below are from the wafers that had the Standard Getter diffusion and were rear-etched 1, 2 and 3 times as well as a control sample that was not rear-etched, but the same behavior was observed in all groups of samples. Increasing the number of etches increased the PL response of the solar cells, meaning that the recombination within the device was reduced.

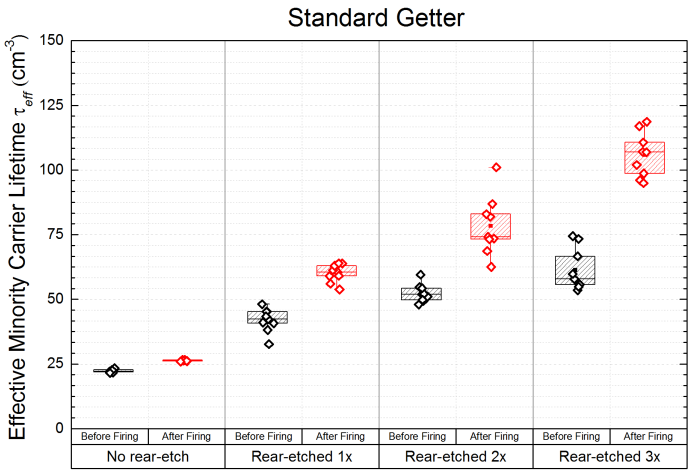

Figure 4.12: Effective Minority Carrier Lifetimes extracted at the injection level of $\Delta n = 9.1 \times 10^{14}\ cm^{-3}$ from Czochralski grown monocrystalline silicon wafers after the application of the standard getter diffusion and multiple rear-etch steps.

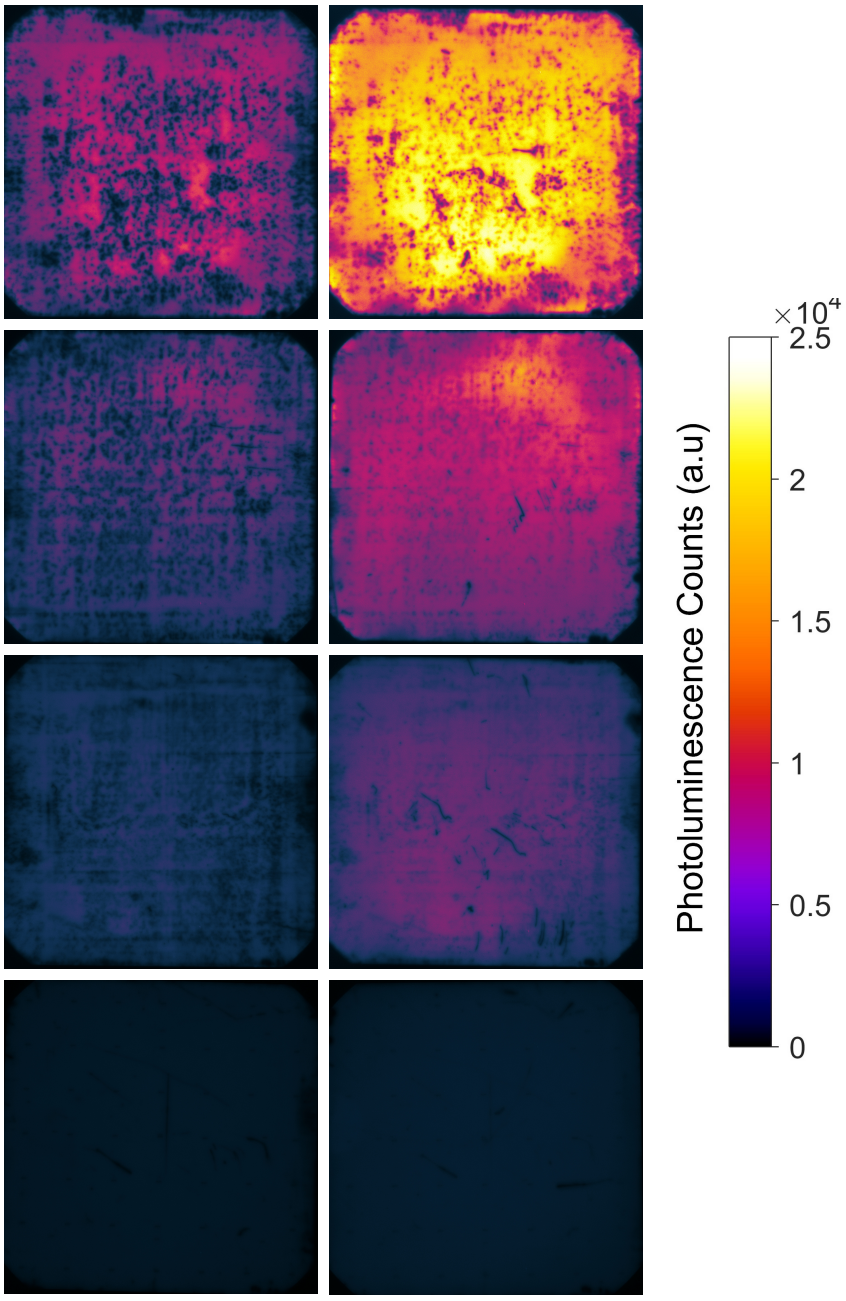

Figure 4.13: Photoluminescence Imaging showing wafers processed with the standard getter diffusion recipe before firing (left) and after firing (right). From bottom to top: no rear-etch process, rear-etched once, rear-etched twice and rear-etched 3 times.

Chapter 5

Conclusion

The work presented here mainly investigates the possibility of using the rear-etch process to perform not only it's primary function of removing the rear emitter and isolating the edges but also to perform an etch back of the front emitter. The effect of the rear-etch process in the front emitter are analyzed and demonstrate that:

- Although the process is performed below room temperature, the gases originated by the acidic etching bath do etch-back the front emitter.
- Even though the etch-back occurs, it is not homogeneous and it is not enough to etch-back the desired amount of the front emitter, even when it is performed three times in a row. Furthermore, the rear-etch process is designed to remove 2 μm of the back of the wafer so wafers that were submitted to the process three times had approximately 6 um of their back removed without achieving the desired sheet resistance on the front.
- The etch-back effect of the rear-etch bath should be taken in account when utilizing the process since it does happen and the emitter sheet resistance does change after the process.

The effectiveness of the standard PDG recipes used at the Solar Industrial Research Facility in gettering iron was also evaluated, and modified recipes with and additional oxygen-free drive-in step were tested and it was concluded that:

- The Standard Getter recipe is effective in gettering iron while the Standard SP recipe had iron released after firing. Both modified recipes did not show interstitial iron being released after firing as well.

- The Modified Screen-Print recipe had its doping profile altered by the absence of oxygen during the drive-in step. The emitter depth and the active dopant concentration near the surface increased and simulations performed in EDNA 2 showed that the desired emitter properties can be possibly achieved by performing an homogeneous etch-back of 0.0977 μm of the front emitter. The etch-back process suggested by Basu et al. [8] using a sodium hypochlorite solution at 80 °C could be tested to perform this process.

- The Modified Getter diffusion needs further analysis to understand the effects of the drive-in step on its doping profile. The diffusion process should be repeated to check if the results were due to an procedure error.

Chapter 6

Suggestions for future works

- A defect etch could be performed to try to determine how far from the wafer's surface the defected region is located.
- Other etching agents should be tested in order to perfom and homogeneous etch back of the emitter obtained through the modification of the standard Screen-Print emitter diffusion recipe.
- The rear-etch bath parameters influence on the etch-back of the front emitter should be investigated in order to reduce the reaction of the gases originated from the bath with the silicon on the front of the wafer.
- The contamination mechanism of the rear-etch bath by contaminated samples could be investigated to avoid or reduce it's occurrence.

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