Low Latency Izhikevich's Simple Neuron Model on FPGA

Vitor Bandeira, Advisors: Guilherme Bontorin e Ricardo Reis

Abstract

The Izhikevich Simple Model (ISM) for neural activity presents a good compromise between waveform quality and computational cost. FPGAs (Field-Programmable Gate Array) are powerful, flexible, and inexpensive digital hardware that can implement such a model. We present an implementation on FPGA of the ISM whose latency is up to 56 times smaller than the ones in the literature.

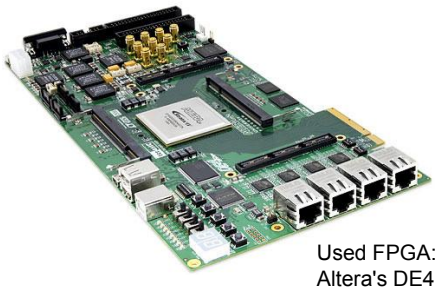
Modified Equations of ISM [1,2,3]

$$h\frac{dv}{dt} = \frac{1}{32}v^2 + 4v + 109.375 - u^* + I^*$$

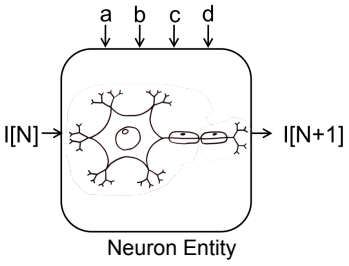
$$h\frac{du}{dt} = a^*(b^*v - u^*)$$

$$v \geq 30mV \implies \begin{cases} v \leftarrow c \\ u^* \leftarrow u^* + d \end{cases}$$

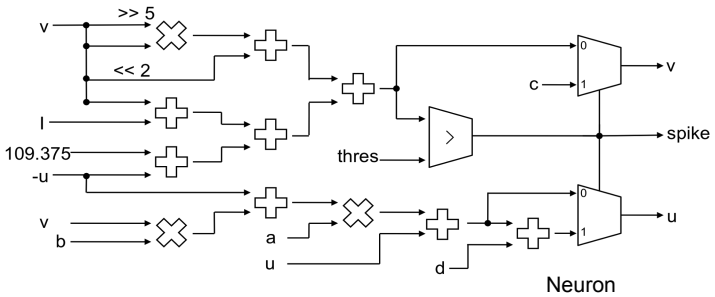
Implemented Neuron



Used FPGA: Altera's DE4

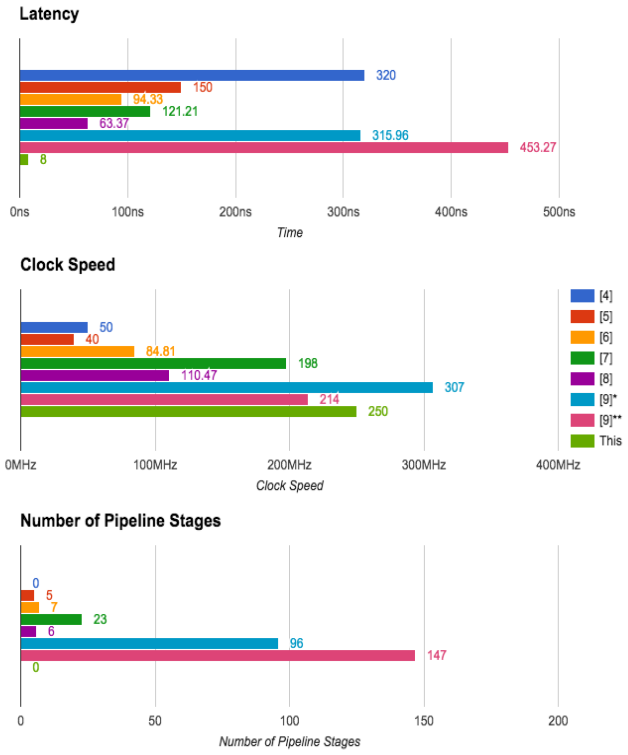


Neuron Entity



Neuron Schematics

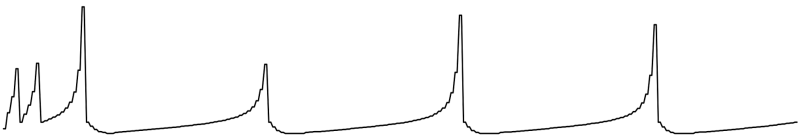
Comparison with the Literature



✔ Good waveform
✔ Up to 56x lower latency
✔ High clock speed

⊖ No pipeline
✘ No logic reuse

Results



This data was obtained from the FPGA running our implementation through the SignalTap II tool in Quartus II® Software.

Conclusions

Our implementation is best suited for hybrid networks systems and presents a fair performance for artificial-only networks. The low latency of the circuit will allow us to reuse the same neuron multiple times.

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Universidade Federal do Rio Grande do Sul
Instituto de Informática
Av. Bento Gonçalves, 9500 - Campus do Vale. Bloco IV
CP 15064, 91501-970- Porto Alegre-Brazil
Contact: {vvbandeira,reis}@inf.ufrgs.br