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Electromigration Aware Cell Design

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“The love you take is the love you make.”
The Beatles (Lennon-McCartney)

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CONTENTS

LIST OF ABBREVIATIONS AND ACRONYMS

AC	Alternating Current
ASIC	Application Specific Integrated Circuit
AOI	Complex logic gate composed by the AND, OR and inverter gates
CAD	Computer-Aided Design
CMOS	Complementary Metal-Oxide Semiconductor
DC	Direct Current
FF	Flip-Flop
GDS	Graphic Data System
GND	Ground - Negative supply voltage
HDL	Hardware Description Language
IC	Integrated Circuit
INV	inverter gate
J	Current Density
LEF	Library Exchange Format
MTTF	Mean time to failure
NAND	Logic gate that represents the boolean function (A . B)
NDR	Non-Default Routing Rules
NLDM	Non-Linear Delay Models
NMOS	N-type metal-oxide-semiconductor
NOR	Logic gate that represents the boolean function (A + B)
RMS	Root Mean Square
RTL	Register Transfer Level
SDC	Synopsys Design Constraints
SPICE	Simulation Program with Integrated Circuit Emphasis
TTF	Time to Failure
UFRGS	Universidade Federal do Rio Grande do Sul
VDD	Positive supply voltage

LIST OF SYMBOLS

A	Ampere
a	Atto
F	Farad
f	Femto
μ	Micro
m	Mili
n	Nano
Ω	Ohms
p	Pico

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ABSTRACT

Electromigration (EM) in on-chip metal interconnects is a critical reliability failure mechanism in nanometer-scale technologies. Usually works in the literature that address EM are concerned with power network EM and cell to cell interconnection EM. This work deals with another aspect of the EM problem, the cell-internal EM. This work specifically addresses the problem of electromigration on signal interconnects and on Vdd and Vss rails within a standard cell. Where there are few studies in the literature addressing this problem. To our best knowledge we just found two works in the literature that talk about the EM within a cell. (DOMAE; UEDA, 2001) found void formed due to electromigration in the interconnection portion in a CMOS inverter and then proposes some ideas to reduce the current through the wire segments where the voids were formed. The second work, (JAIN; JAIN, 2012), just cites that the standard-cell-internal-EM should be checked and the safe frequency of the cells at different operating points must be modeled. No previous work analyzed and/or modeled the EM effects on the signals inside the cells. In this way, our work is the first one to use the pin placement to reduce the EM effects inside of the cells. In this work, cell-internal EM is modeled incorporating Joule heating effects and current divergence and is used to analyze the lifetime of large benchmark circuits. An efficient graph-based algorithm is developed to speed up the characterization of cell-internal EM. This algorithm estimates the currents when the pin position is moved avoiding a new characterization for each pin position, producing an average error of just 0.53% compared to SPICE simulation. A method for optimizing the output, Vdd and Vss pin placement of the cells and consequently to optimize the circuit lifetime using minor layout modifications is proposed. To optimize the TTF of the circuits just the LEF file is changed avoiding the critical pin positions, the cell layout is not changed. The circuit lifetime could be improved up to 62.50% at the same area, delay, and power because changing the pin positions affects very marginally the routing. This lifetime improvement is achieved just avoiding the critical output pin positions of the cells, 78.54% avoiding the critical Vdd pin positions, 89.89% avoiding the critical Vss pin positions and up to 80.95% (from 1 year to 5.25 years) when output, Vdd, and Vss pin positions are all optimized simultaneously. We also show the largest and smallest lifetimes over all pin candidates for a set of cells, where the lifetime of a cell can be improved up to 76$\times$ by the output pin placement. Moreover, some examples are presented to explain why some cells have a larger TTF improvement when the output pin position is changed. Cell layout optimization changes are suggested to improve the lifetime of the cells that have a very small TTF improvement by pin placement. At circuit level, we present an analysis of the EM effects on different metal layers and different wire lengths for signal wires (nets) that connect cells.

Keywords: Electromigration, Circuit Lifetime, Cell-level, AC EM, Physical Design, Microelectronics.

Projeto de Células Considerando a Eletromigração

RESUMO

A Eletromigração (EM) nas interconexões de metal em um chip é um mecanismo crítico de falhas de confiabilidade em tecnologias de escala nanométrica. Os trabalhos na literatura que abordam os efeitos da EM geralmente estão preocupados com estes efeitos nas redes de distribuição de potência e nas interconexões entre as células. Este trabalho aborda o problema da EM em outro aspecto, no interior das células, e aborda especificamente o problema da eletromigração em interconexões de saída, Vdd e Vss dentro de uma célula padrão onde há poucos estudos na literatura que endereçam esse problema. Até onde sabe-se, há apenas dois trabalhos na literatura que falam sobre a EM no interior das células. (DOMAE; UEDA, 2001) encontrou buracos formados pela EM nas interconexões de um inversor CMOS e então propôs algumas ideias para reduzir a corrente nos segmentos de fio onde formaram-se buracos. O outro trabalho, (JAIN; JAIN, 2012), apenas cita que a EM no interior das células padrão deve ser verificada e a frequência segura das células em diferentes pontos de operação deve ser modelada. Nenhum trabalho da literatura analisou e/ou modelou os efeitos da EM nos sinais dentro das células. Desta forma, este é o primeiro trabalho a usar o posicionamento dos pinos para reduzir os efeitos da EM dentro das células. Nós modelamos a eletromigração no interior das células incorporando os efeitos de *Joule heating* e a divergência da corrente e este modelo é usado para analisar o tempo de vida de grandes circuitos integrados. Um algoritmo eficiente baseado em grafos é desenvolvido para acelerar a caracterização da EM no interior das células através do cálculos dos valores de corrente média e RMS. Os valores de corrente computados por esse algoritmo produzem um erro médio de 0.53% quando comparado com os valores dados por simulações SPICE. Um método para otimizar a posição dos pinos de saída, Vdd e Vss das células e consequentemente otimizar o tempo de vida do circuito usando pequenas modificações no leiaute é proposto. Para otimizar o TTF dos circuitos somente o arquivo LEF é alterado para evitar as posições de pino críticas, o leiaute da célula não é alterado. O tempo de vida do circuito pode ser melhorado em até 62.50% apenas evitando as posições de pino críticas da saída da célula, 78.54% e 89.89% evitando as posições críticas do pino de Vdd e Vss, respectivamente Quando as posições dos pinos de saída, Vdd e Vss são otimizadas juntas, o tempo de vida dos circuitos pode ser melhorado em até 80.95%. Além disso, nós também mostramos o maior e o menor tempo de vida sobre todos as posições candidatas de pinos para um conjunto de células, onde pode ser visto que o tempo de vida de uma célula pode ser melhorado em até 76$\times$ pelo posicionamento do pino de saída. Além disso, alguns exemplos são apresentados para explicar porque algumas células possuem uma melhora maior no TTF quando a posição do pino de saída é alterada. Mudanças para otimizar o leiaute das células são sugeridas para melhorar o tempo de vida das células que possuem uma melhora muito pequena no TTF através do posicionamento dos pinos. A nível de circuito, uma análise dos efeitos da EM é apresentada para as diferentes camadas de metal e para diferentes comprimentos de fios para os sinais (nets) que conectam as células.

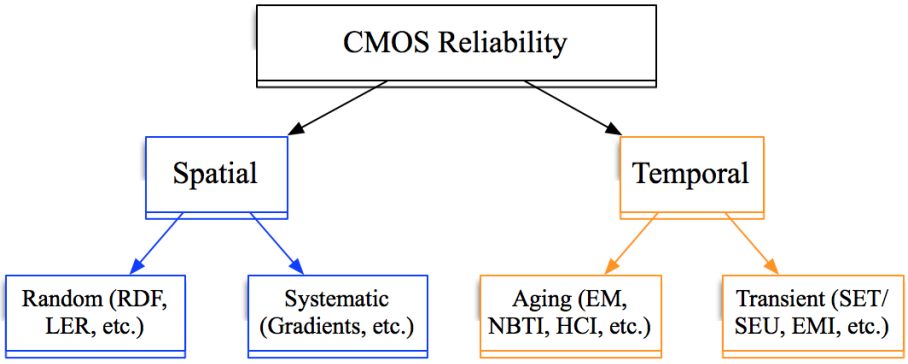
Palavras-chave: Eletromigração, Tempo de vida do circuito, TTF, Nível de célula, AC EM, Microeletrônica.

1 INTRODUCTION

Reliability is a key issue in integrated circuits (IC) designs because users expect failure-free operation throughout the product's lifetime (REIS; CAO; WIRTH, 2015), (LI; MAREK-SADOWSKA; NASSIF, 2015), (KLUDT et al., 2014). However, failure rates will likely grow as transistors and wires shrink and the supply voltage scales slowly, leading to higher current densities and temperatures. As a result, transistor and wire degrade faster shortenning the product's lifetime (ABELLA et al., 2008) (PATEL, 2014).

Nanometer CMOS reliability issues can be categorized into spatial and temporal effects as Figure 1.1 illustrates. Spatial effects are immediately visible right after production and are fixed in time and can be random (e.g. random dopant fluctuations (RDF), line edge roughness (LER), etc) or systematic (e.g. gradient effects, etc.). Temporal effects, on the other hand, are time-varying and change depending on operating conditions such as the operating voltage, temperature, switching activity, presence and activity of neighboring circuits. Temporal effects can be aging effects (e.g. electromigration (EM), hot carrier injection (HCI), negative bias temperature instability (NBTI), etc.) (SENGUPTA; SAPATNEKAR, 2014) and transient effects (e.g. single event transients (SETs), single event upsets (SEUs), electromagnetic interference (EMI), etc.) (MARICAU; GIELEN, 2013). In this work, we investigate the electromigration effects which are one of the most important aging effects on ICs, specially in nanometer technologies.

Figure 1.1: A CMOS circuit can fail from spatial or temporal unreliability effects.



Source: (MARICAU; GIELEN, 2013), (WIRTH; SILVA, 2010).

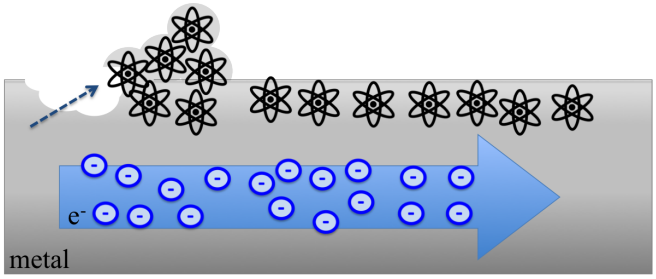
Electromigration (EM) is one of the critical reliability concerns, (WU et al., 2012) causing shorts and opens in metal interconnects, leading to interconnection failures and decreasing the mean time to failure (MTTF) of the chip. Particularly for copper metallization at 45nm and below, EM affects global and local interconnects and is a major source of wire and via failure (SRINIVASAN et al., 2004) in a chip, limiting the performance scaling (GEDEN, 2011), (XIE; NARAYANAN; XIE, 2012), (KAHNG; NATH; ROSING, 2013), (VAIDYANATHAN et al., 2014). The gap between what circuit design needs and what technology allows is rapidly widening for maximum allowed current density in interconnects. This is the so-called EM crisis (LI et al., 2014). In this way, the concern of EM reliability has attracted more attention from circuit and chip designers, integrators

and reliability engineers (LI et al., 2014). Thereby, it challenges the state-of-the-art in design, physics, process and CAD processes(PARK; JAIN; KRISHNAN, 2010).

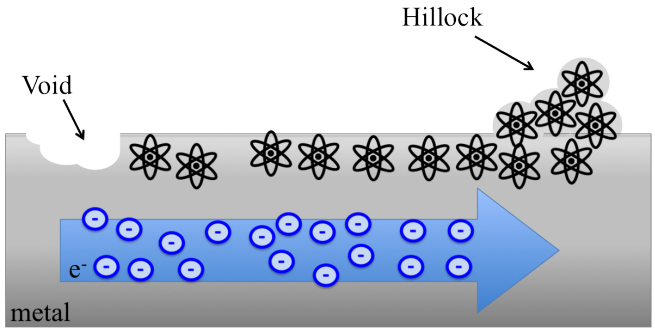
1.1 Electromigration (EM)

Electromigration is an increasing concern in on-chip wires and vias in future technologies (LIENIG, 2013). EM failures may result when a current flows through an on-chip wire over a long period of time and the current density is high enough to cause a physical migration of atoms in the wire (SAPATNEKAR, 2013) (RANGARAJAN; DENG, 2013). High temperatures and higher current densities (which increase the dragging force) increase metal atoms likelihood to move (ABELLA et al., 2008). Thus, the drift of metal atoms along with the electron flow causes a metal depletion upstream, creating voids, and a deposition of metal downstream, creating hillocks, along the current flow direction as Figure 1.2 shows.

Figure 1.2: (a) The drift of metal atoms along with the flow of electrons (b) causing voids and hillocks.



(a)

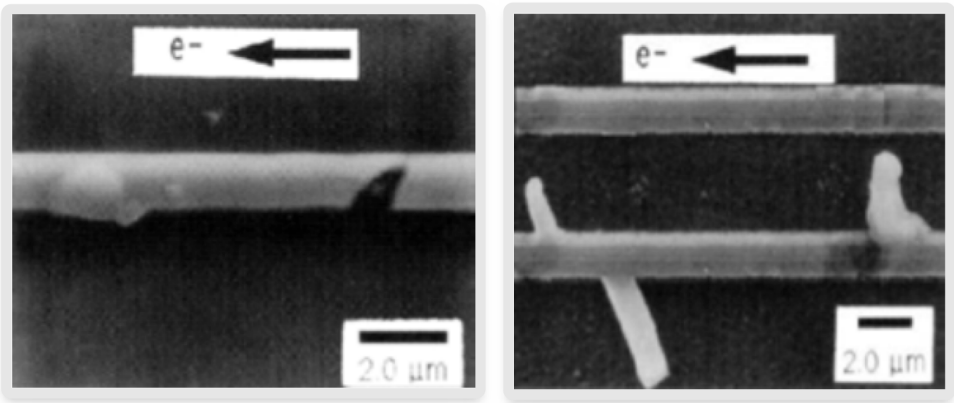


(b)

Source: (GEDEN, 2011).

The upstream thinning increases the wire resistance and ultimately results in open-circuit failures as the first example in Figure 1.3 presents. While the downstream deposition may cause short-circuit failure to the nearby metal as second example in Figure 1.3. Consequently, EM effect slows down the circuit through time, and in the worst case can lead to the eventual loss of one or more connections and an intermittent failure of the entire circuit (XIE; NARAYANAN; XIE, 2012).

Figure 1.3: Void (open circuit) and hillock (short circuit).



Source: (GEDEN, 2011).

1.2 Electromigration in Future Technologies (LIENIG, 2013)

With the technology miniaturization, line widths will continue to decrease over time, as well the wire cross-sectional areas. Table 1.1 (LIENIG, 2013) shows that the cross-sectional area shrinks from about 1,000nm^2 in 2014 to less than 500nm^2 in 2018 (LIENIG, 2013). The currents are also reduced due to lower supply voltages and shrinking gate capacitances.

Table 1.1: Predicted technology parameters based on the ITRS, 2011 edition (ITRS, 2011); maximum currents and current densities for copper at 105^0C.

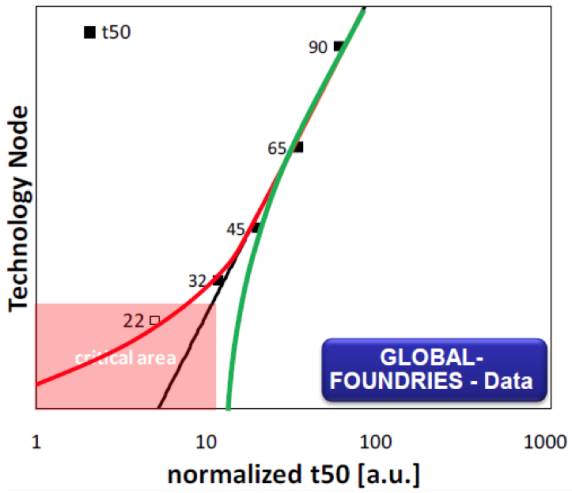
Year	**2014**	**2016**	**2018**	**2020**	**2022**	**2024**	**2026**
Gate length (nm)	18.41	15.34	12.78	10.65	8.88	7.40	6.16
On-chip local clock frequency (GHz)	4.211	4.555	4.927	5.329	5.764	6.234	6.743
DC equivalent maximum current (μA)*	18.14	12.96	10.33	7.36	5.53	4.45	3.52
Metal 1 properties							
Width - half-pitch (nm)	23.84	18.92	15.02	11.92	9.46	7.51	5.96
Apect ratio	1.9	2.0	2.0	2.0	2.1	2.1	2.2
Layer thickness (nm)*	45.49	37.84	30.03	23.84	19.87	15.77	13.11
Cross-sectional area nm^2*	1,079.7	716.0	451.0	284.1	187.9	118.4	78.13
DC equivalent current densities (MA/cm^2)							
Maximum tolerable current density (w/o EM degradation)**	4.8	3.0	1.8	1.1	0.7	0.4	0.3
Maximum current density (solutions unknown)**	25.4	15.4	9.3	5.6	3.4	2.1	1.2
Required current density for driving four inverter gates	1.68	1.81	2.29	2.59	2.94	3.76	4.50

* Calculated values, based on given width W, aspect ratio A/R, and current density J in (ITRS, 2011), calculated as follows: layer thickness $T = A/R \cdot W$, cross-sectional area $A = W \cdot T$ and current $I = J \cdot A$.
** Approximated values from the ITRS figure INTC9 (ITRS, 2011).
All remaining values are from the ITRS 2011 edition (ITRS, 2011).

Source: (LIENIG, 2013).

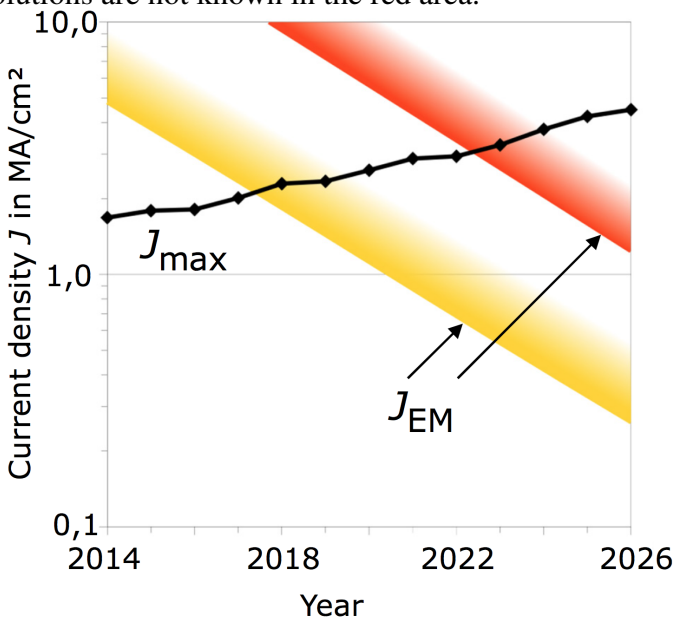
However, the decrease in cross-sectional areas increases the current densities J (as Figure 1.5 shows) and consequently decreases the lifetime by half each new generation, as presented in Figure 1.4, where a critical area to EM is visible below about 28nm. The green line in Figure 1.4 shows the EM enhancement urgently needed.

Figure 1.4: Evolution of lifetime versus technology node. Black line shows the effect of reduced critical void volume: Green line shows the EM enhancement urgently needed.



Source: (ITRS, 2011) (*Courtesis of A. Aubel/ Globalfoundries*).

Figure 1.5: Expected development of current densities (J_{max}) needed for driving four inverter gates, according to ITRS 2011 (see also Table 1.1). EM degradation needs to be considered when crossing the yellow barrier of current densities (J_{EM}). As of now, manufacturable solutions are not known in the red area.



Source: (LIENIG, 2013).

According to the Figure 1.5 based on the Interconnect Chapter of the 2011 International Technology Roadmap for Semiconductors (ITRS) (ITRS, 2011), the maximum current density limits (from EM reliability considerations) become the barrier to further frequency scaling from 2018 onwards. Moreover, the ITRS indicates that all minimum-sized interconnects will be EM-affected by 2018, potentially limiting any further down-scaling of wire sizes (Figure 1.5, yellow barrier) (LIENIG, 2013). As the total length of interconnect per IC will continue to increase, reliability requirements per length unit of the wires need to increase in order to maintain overall IC reliability. The ITRS thus states

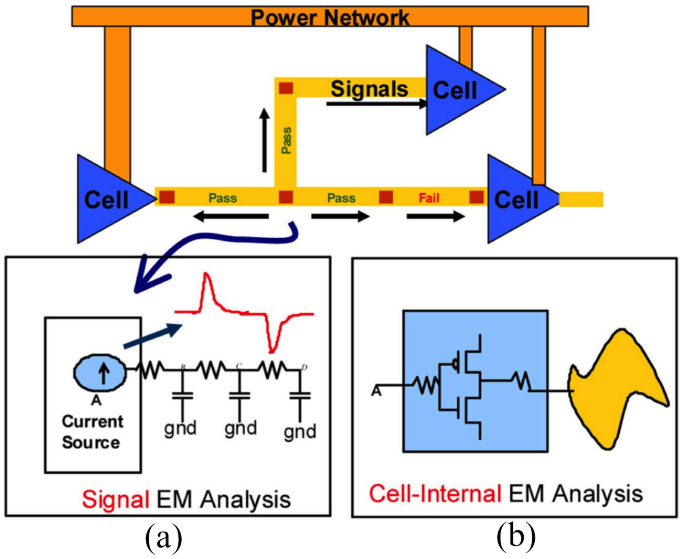
that no known solutions are available for the EM-related reliability requirements that we will face approximately in 2023 (Figure 1.5, red barrier) (LIENIG, 2013). This shows the great importance of the research seeking for solutions that mitigate the EM effects mainly on the latest technologies.

Design tools can significantly improve the EM robustness of the generated layout by utilizing EM-optimized layout configurations as constraints during synthesis steps, such as routing. It is believed that this inclusion of EM-specific requirements in the physical design can provide relief from severe reliability constraints in future technologies (LIENIG, 2013).

1.3 Motivation and Contributions

Traditionally, EM has been a significant concern in global power delivery networks (XIE; NARAYANAN; XIE, 2012), where the direction of current flow is generally unidirectional, resulting in a steady migration pattern over time (SAPATNEKAR, 2013). Recently, two new issues have emerged, as Figure 1.6 shows.

Figure 1.6: Problem space: (a) current source modeling for signal-EM analysis and (b) load abstraction for cell-internal EM analysis.



Source: (JAIN; JAIN, 2012).

First, EM analysis can no longer be restricted just to global wires. Traditional EM analysis has focused on higher metal layers, but with shrinking wire dimensions and increasing currents, the current densities in lower metal layers are also now in the range where EM effects are manifested. EM effects are visible at current densities of about 1MA/cm^2, and such current densities are seen in the internal metal wires of standard cells, resulting in cell-internal signal EM (JAIN; JAIN, 2012). These high current densities arise because local interconnect wires within standard cells typically use low wire widths to ensure compact cell layouts. In short metal wires, such effects were traditionally thought to be offset by Blech length considerations (BLECH, 1976), but for reasons discussed on Section 3.3.3, such effects do not help protect intra-cell wires in designs at deeply scaled technology nodes. Second, EM has become increasingly important in signal wires, where the direction of current flow is bidirectional. This is due to increased

current densities, whose impact on EM is amplified by Joule heating effects (LEE, 2012a), (AGARWAL et al., 2014), since EM depends exponentially on temperature. Therefore, the current that flows through these wires to charge/discharge the output load can be large enough to create significant EM effects over the lifetime of the chip.

For signal nets with bidirectional current flow, the time-average of the current waveform is often close to zero. However, even in cases where the current in both directions is identical, it is observed that EM effects are manifested, as presented in Section 3.1.

Intra-cell power networks are also associated with EM concerns. In going down to deeply scaled technology nodes, the current through the power rails of the cells has remained roughly constant while the cross-sectional area of power rails has decreased, causing the current density in power rails to increase (WANG; TAM; CHEN, 2014). Moreover, the power rails are generally subjected to a unidirectional current flow, referred as DC electromigration, which acts more aggressively in causing electromigration (PELLOIE, 2013).

In the cell library used in this work, we can see high current densities on the Vdd and Vss power rails as well as on signal wires, reducing the lifetime of the cells. For example, we compute signal wires in an INV_X4 (inverter with size 4, where the transistors are 4 times larger than the minimum transistor size) cell to have an effective average current density of 1.8 MA/cm^2 at 2GHz, while power wires have an effective current density of 2.15 MA/cm^2 in a 22nm technology. This switching rate is very realistic, and can be seen in, for example, clock buffers in almost any modern design, as well as in cells that switch at 25% probability in a 4GHz design.

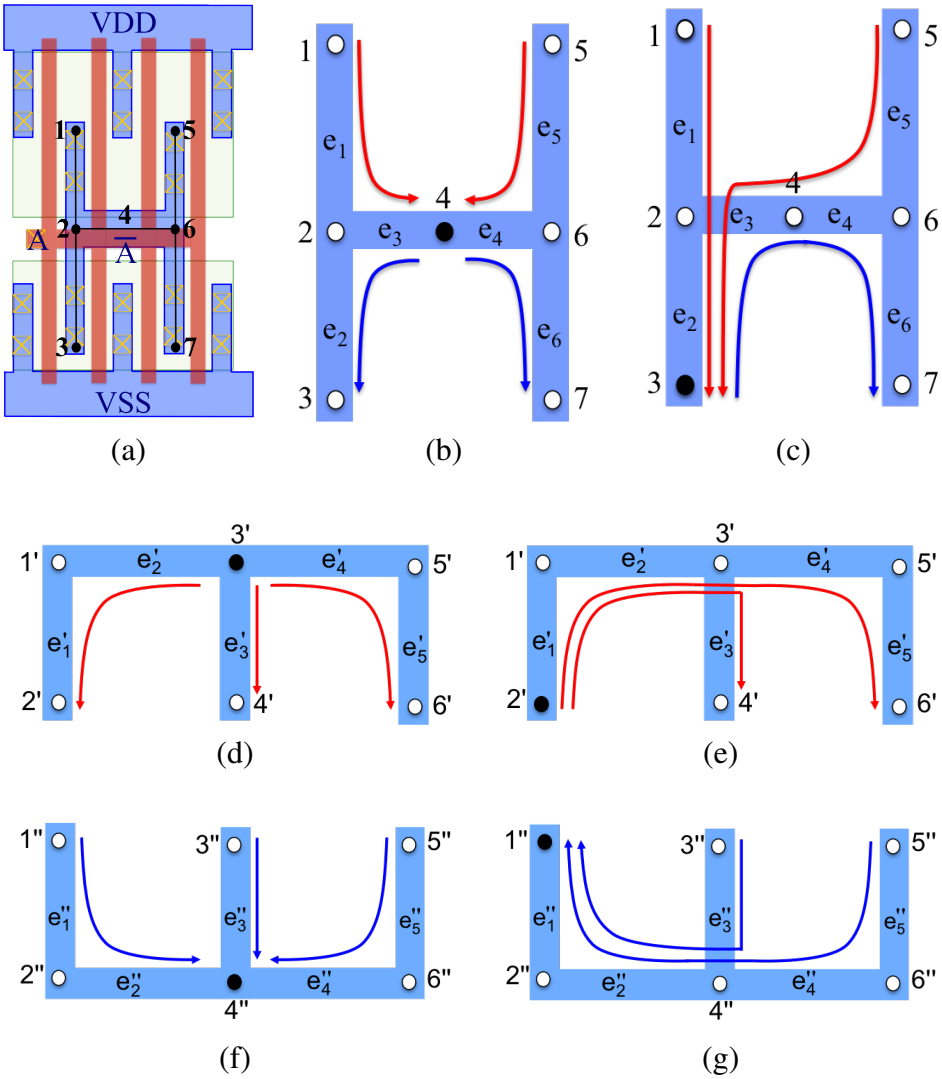
While the cell-internal signal EM problem has been described in industry publications such as (JAIN; JAIN, 2012), its efficient analysis is an open problem. In this work, we study the problem of systematically analyzing cell-internal signal EM due to both AC EM on signal wires and DC EM on the Vdd and Vss rails of the cells. We devise a solution that facilitates the analysis and optimization of cell-internal signal EM for a standard cell library based design. We first develop an approach to efficiently characterize cell-internal EM over all output, Vdd, and Vss pin locations within a cell, incorporating Joule heating effects into our analysis. We then formulate the pin optimization problem that chooses cell output pins during place-and-route so as to maximize the design lifetime.

To motivate the problem, we use the example of the INV_X4 (inverter with size 4) cell, whose layout is shown in Fig. 1.7(a), from the 45nm NANGATE Open cell library (NANGATE, 2011). The input signal A is connected to the polysilicon structure. The layout uses four parallel transistors for the pull-up (poly over p-diffusion in the upper half of the figure) and four for the pull-down (poly over n-diffusion in the lower half of the figure), and the output signal can be tapped along the H-shaped metal net in the center of the cell. The positions where the output pin can be placed are numbered 1 through 7, and the edges of the structure are labeled e_1 through e_6, as shown in the figure. Since the four PMOS transistors are all identical, by symmetry, the currents injected at nodes 1 and 5 are equal; similarly, the NMOS-injected currents at nodes 3 and 7 are equal.

Considering the cell-internal signal EM. When the output pin is at node 4, the charge/discharge current is as shown in Fig. 1.7(b). The distribution is similar when the pin is at node 2 or 6 (because of the asymmetry in the parasitics at these two nodes is very small), except that the current direction in e_3 and e_4, respectively, is in opposite direction (reversed). Moving the pin changes the current distribution in e_1–e_6. The currents and the TTF is calculated for each edge, i.e., each wire segment is analysed separately. If the pin is at node 3 (Fig. 1.7(c)), since the rise and fall discharge currents have similar values, the

charging current in edge e_2 is about $2\times$ larger than the earlier case, while the discharging current is about the same (with opposite direction). As quantified in Chapter 3, the larger peak current leads to a stronger net electron wind that causes EM, resulting in a larger *effective average current*, and therefore, a lower lifetime. In fact, based on exact parasitic extraction of the layout, fed to SPICE (thus including short-circuit and leakage currents), the average effective EM current through e_2 is $2.43\times$ for 22nm technology larger than when the pin is at node 4. Accounting for Joule heating, this results in a $2.79\times$ lifetime reduction. For the Vdd and Vss pins, a similar effect occurs when the pin position is changed.

Figure 1.7: (a) The layout and output pin position options for INV_X4. Charge/discharge currents when the output pin is at (b) node 4 and (c) node 3. The red [blue] lines represent rise [fall] currents. (d) The Vdd pin position options for INV_X4 and the currents when the Vdd pin is at node $3'$ and (e) node $2'$. (f) The Vss pin position options for INV_X4 and the currents when the Vss pin is at node $4''$ and (g) node $1''$.



Source: (POSSER et al., 2015 - under review).

Next, we consider EM on the supply wires. Fig. 1.7(d) and (e) represent the Vdd rail, where the Vdd pin can be placed on the nodes numbered $1'$ through $6'$. Fig. 1.7(d) shows

how the charge current is flowing through the edges when the Vdd pin is placed at node $3'$. We can see that the current flows are symmetric for this pin position. Since the edge e'_3 supplies two transistors, as shown in Fig. 1.7(a), the current flowing through e'_3 is larger than the current flowing through the other edges, which each supply just one transistor. Thus, the edge e'_3 is the critical edge when the Vdd pin is placed at node $3'$. Fig. 1.7(e) shows the current flowing through the edges when the Vdd pin is placed at node $2'$. In this case, the current flowing through edge e'_1 supplies three of the four transistors, is $3\times$ larger than the current flowing through this same edge when the pin is at node $3'$. Thus, this is the critical edge for this pin position, reducing the lifetime of the cell by $2\times$ compared with the lifetime when the pin is placed at node $3'$.

Similarly, the Vss rail of the INV_X4 cell is represented in Figs. 1.7(f) and (g). The Vss pin can be placed on the numbered nodes $1''$ through $6''$, and the currents being discharged through the edges by the Vss pin placed at node $4''$ are shown in Fig. 1.7(f). Using a similar argument as for the Vdd case, moving the pin from node $4''$ in Fig. 1.7(f) to pin $1''$ in Fig. 1.7(g) changes the critical edge from e''_3 to e''_1, and the lifetime again degrades by about $2\times$.

So, the contributions of this work can be summarized as follows:

1. A study of the problem of analyzing the EM effects inside standard cells
   - for signal wires, output wire, where the current that flows through the local interconnect wires to charge/discharge the output load can be large enough to create significant EM effects over the lifetime of the chip, and;
   - for the supply wires, Vdd and Vss, where their lifetime is dependent on the pin position.
2. The EM modeling incorporating Joule heating effects and the current divergence to estimate the lifetime of the signal and supply wires (Chapter 3).
3. An approach to efficiently characterize cell-internal EM over all output, Vdd and Vss pin locations within a cell using a reference pin position. Wherein a graph-based algorithm is used to compute the currents through each edge when the pin position is moved from the reference case to another location. (Chapter 4).
4. The pin placement optimization problem formulation (Chapter 5)
   - whereby place-and-route chooses cell signal output pins in such a way that the lifetime of the overall design is maximized;
   - for the supply pins, Vdd and Vss, where the pins are placed with the objective to optimize the circuit lifetime.

   The pin positions to be avoided by the router will depend on the logic of the gate and on the wire shape. The pin positions that produce a high current density in one or more wire segments will be avoided. The critical pin positions are avoided just changing the LEF (Library Exchange Format) file of the cells, the cell layouts are not changed. In this way, just the routing step of the design flow changes to consider the TTF-optimized LEF file.
5. Cell layout optimization changes are suggested to improve the cell robustness from the EM perspective. These robust cells can replace the critical cells affected by

EM in the circuits, if the circuit should have a larger TTF than the TTF achieved just by the pin position optimization. For this, the current flows and the EM effects behavior for different pin positions and different logic gate are presented (Chapter 6).

6. At circuit level, we present an analysis of the EM effects on different metal layers and different wire lengths for signal wires (nets) that connect cells. The delay behavior and how the average current reduces through the wire are also reported in this analysis (Chapter 7).

Part of this work was developed while the author was on an internship at University of Minnesota working with Prof. Sachin S. Sapatnekar and his research group.

1.4 Thesis Organization

The rest of this work is organized as follows. A review of existent works that address the EM problem is presented in Chapter 2. Some concepts of the digital circuit physical design flow and the steps where techniques to mitigate the EM effects could be applied are presented in Section 2.1. Chapter 3 describes how the cell-internal EM is modeled in our work incorporating Joule heating effects and the current divergence. The current calculation approach for our cell-internal EM analysis flow is presented in Chapter 4, where the algebras to calculate the average and RMS currents for different pin positions are described. Our graph-based algorithm that computes the current through each edge when the pin is moved is also presented in this Chapter. Next, a method for optimizing the circuit lifetime using incremental layout modifications is proposed. The circuit lifetime can be increased by placing the output, Vdd, and Vss pins appropriately, avoiding the critical pin positions that reduce the lifetime of the cells by EM. The implementation flow is then discussed in Chapter 5. The experimental results of our approach are shown in Chapter 6. We are presenting an EM analysis at circuit level for the nets that connect the cells. The tests are considering different metal layers and different wire lengths for the nets (Chapter 7) At last, conclusions, future works and the publications are presented on Chapter 8.

2 STATE OF THE ART

EM is a well-known problem and many methods have been proposed to model and to mitigate the EM effects in different design stages, as Section 2.1 presents, for different types of interconnections as presented in Section 2.2.

2.1 Mitigating the EM effects in Different IC Design Flow Stages

There are two main methodologies used in IC design to develop application specific integrated circuits (ASICs): the full-custom and the standard cells (WESTE; HARRIS, 2005) (RABAEY; CHANDRAKASAN; NIKOLIC, 2002).

In a full-custom methodology, each individual transistor and interconnections in the circuit are designed in a customized way. Every design stage is carefully done to obtain the best possible circuit option in terms of area, speed and power consumption. Transistors are deliberately laid out in chips most compactly, spending months by many designers and engineers (CHEN, 1999), increasing significantly the final design cost. The full-custom methodology is generally used to construct the standard-cell library and in analog designs.

Traditional standard-cell based synthesis flow have been used in the industry and academia for a very long time. The cells are taken from a pre-designed and pre-characterized cell library, generally, designed-by-hand. Standard-cell based synthesis flows are known to be very reliable and predictable.

The standard-cell based synthesis flow generally follows the methodology presented in Figure 2.1 and can be divided into two main stages: logic synthesis and physical synthesis. The logic synthesis receives as input a circuit description (in VHDL, Verilog), the design constraints and the cell library file (.lib, .db) and generates a structural description composed by logic gates and registers. This step explores the selection of logic gates from a cell library to represent the best result considering the design constraints. The physical synthesis generates the circuit layout from the structural description provided by the logic synthesis following these steps (KAHNG, 2011):

- floorplanning: usually is the first step of the physical synthesis. It is responsible to define the position of the high level blocks in the total circuit area. The I/O pads position and power supply network are also defined in this step;

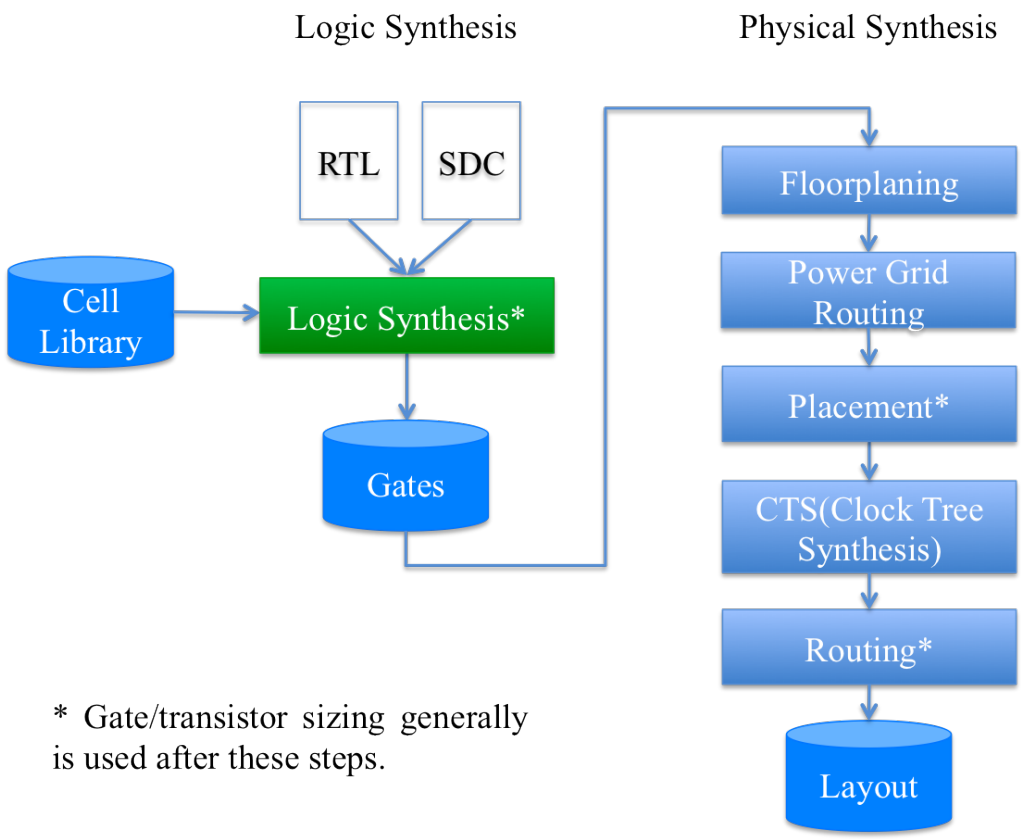
- power grid routing: determines not only the layout of the power-ground distribution network, but also the placement of supply I/O pads or bumps (KAHNG, 2011);

- placement: is responsible to place the cells (gates) that compose the circuit in the circuit area aiming to reduce the wire length;

- CTS - Clock Tree Synthesis: performs the clock tree routing in syncronous circuits to distribute the clock signal throughout the circuit;

- signal routing: performs the signal routing among the cells respecting the connections description from the circuit netlist;

Figure 2.1: Standard-cell based synthesis flow.



Source: (RABAEY; CHANDRAKASAN; NIKOLIC, 2002; WESTE; HARRIS, 2005).

- gate/transistor sizing: is used throughout the design flow to correct timing errors and to optimize the design. It is commonly used after logic synthesis, placement, routing (LEE, 2012b). The gate/transistor sizing has as objective to determine the best size for each logic gate (transistor) of the circuit considering the current that must be supplied to charge the attached load (POSSER et al., 2012) (REIMANN et al., 2013) (FLACH et al., 2013) (FLACH et al., 2014) (POSSER et al., 2014).

After the routing, the layout of the circuit is complete. However, the characteristics of the circuit have to be verified to know if the circuit will operate as required. For this, verifications are used to check if the circuit meets the specifications generated early. If the product requirements are not met, a rework is required (BUTZEN, 2012) (KAHNG, 2011).

EM-aware optimization is an important part of high reliability circuit design (XIE; NARAYANAN; XIE, 2012), where technology nodes smaller than 65 nm require power-integrity (e.g., IR drop-aware timing, electromigration reliability) analysis flows (KAHNG, 2011). Thus, we have to include some steps in the IC design flow to consider and reduce the EM problem in the circuits. In this work, the circuit lifetime is improved under cell-internal EM in the routing step of the standard-cell based synthesis flow. Chapter 5 shows in details the implementation flow used in this work. Previous works in the literature have applied techniques through the IC design flow to mitigate the EM.

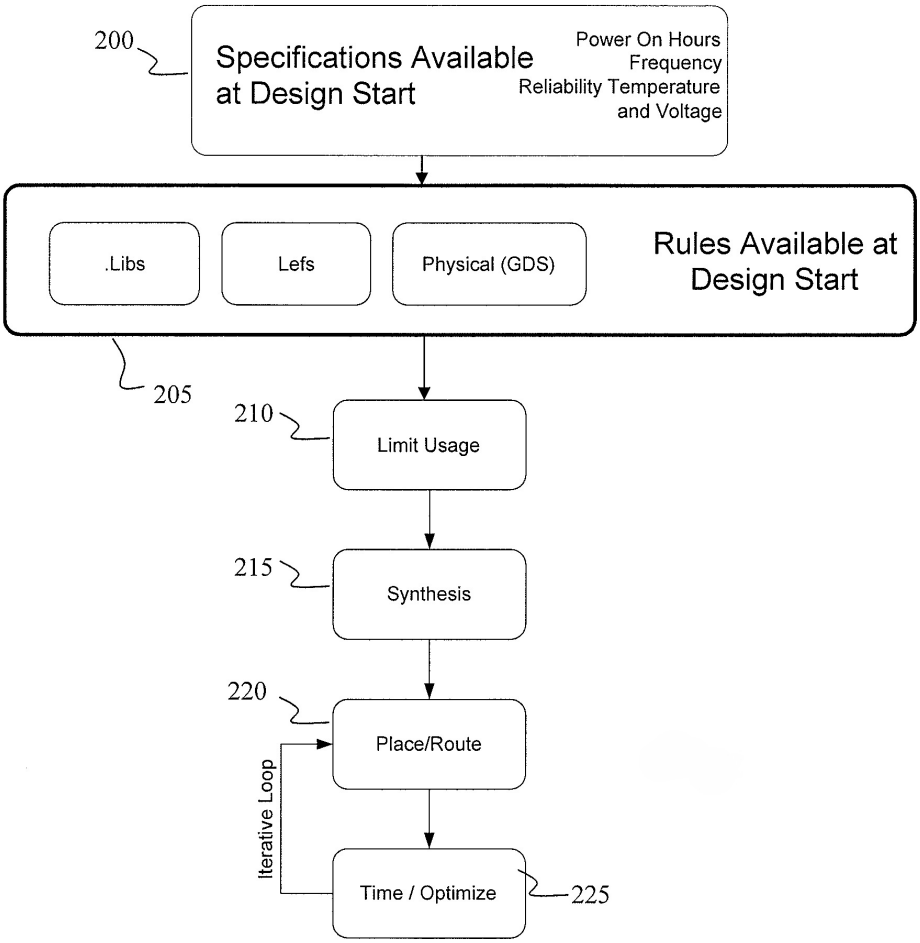
(BALHISER et al., 2005) presents a method and system for enabling efficient identification of nets that are at risk of failure due to the effects of electromigration permitting targeted assessment and redesign of the identified nets before the final steps of the design.

An early-stage calculation to determine the worst-case bounds on interconnect segment currents under the effect of EM is presented in (JERKE; LIENIG, 2010). This early-stage calculation enables nets to be separated into critical and non-critical sets. Only the set of critical nets, which is typically considerably smaller, requires subsequent special consideration during physical design and layout verification due to current density design limits. The algorithms used are fast enough to run on every net and can be used to the pre-layout identification of nets that are potentially troublesome and may need sizing.

Sections below present the most relevant EM related works in details with their techniques in different steps of the design flow aiming to produce EM-aware designs.

2.1.1 Method of managing electro migration in logic designs and design structure thereof (BARWIN; BICKFORD, 2013)

Figure 2.2: Flow diagram implementing processes proposed.



Source: (BARWIN; BICKFORD, 2013).

Considering the standard-cell based synthesis flow (RABAEY; CHANDRAKASAN; NIKOLIC, 2002) (WESTE; HARRIS, 2005) for integrated circuits design, (BARWIN; BICKFORD, 2013) presents an invention that provides a method to avoid potential EM violations during an early design step, before the logic synthesis. Available circuit information is used to modify maximum capacitance or maximum output slew rate that each individual cell is allowed to drive, it is possible to design a circuit early in the design

cycle to avoid EM violations. And, by knowing EM violations prior to arriving at the layout of the circuit design, a considerable time and expense during later design stages can be saved, e.g., simulation and testing, by not having to redesign the circuit. On the other hand, this methodology can super estimate the EM violations making the circuit works below its maximum performance. Or, if the EM violations are super estimated, an additional step to evaluate the EM effects on the final circuit layout have to be included.

The proposed flow is presented in Figure 2.2, where the design specifications and rules are set at blocks 200 and 205. At block 210 is the contribution of the work, the program control will limit usage, e.g., limit the output capacitance that the cell can drive to avoid EM violations, by calculating the maximum output slew or output capacitance on each output pin using the available specifications and rules. At block 215, the logic synthesis is performed using the constraints from block 210. At block 220, the place and route steps are executed. At block 225, the program control will time and optimize the circuit. Blocks 220 and 225 will undergo an iterative loop until the design meets its specifications.

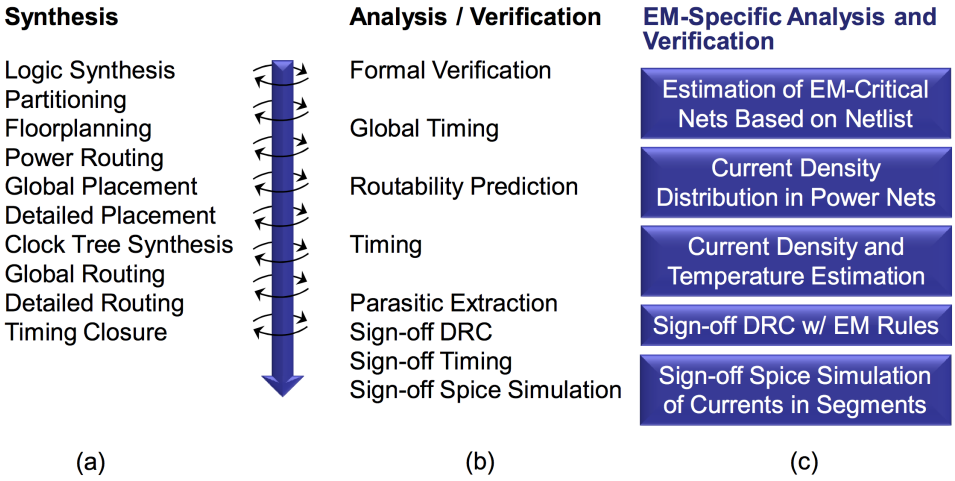
2.1.2 Electromigration and its impact on physical design in future technologies (LIENIG, 2013)

The EM problem during layout synthesis is addressed in (LIENIG, 2013), focusing on basic design issues that affect electromigration during interconnect physical design. The aim is to increase current density limits in the interconnect by utilizing electromigration-inhibiting measures, such as short-length and reservoir effects (Section 2.2.4). Exploitation of these effects at the layout stage provides partial relief of EM concerns in today's design flows. Design tools can significantly improve the EM robustness of the generated layout by utilizing EM-optimized layout configurations as constraints during synthesis steps, such as routing. It is believed that the inclusion of EM-specific requirements in the physical design can provide relief from severe reliability constraints in future technologies.

(LIENIG, 2013) presents flow options to analyze the impact of electromigration on circuit reliability as Figure 2.3(c) shows. These options are used in different synthesis steps of the digital design flow (Figure 2.1 and Figure 2.3(a)). The verification steps presented in Figure 2.3(b) ensure that the circuit acquires the required electrical characteristics and functions, and meets the reliability and manufacturability criteria. (LIENIG, 2013) cities different ways to do an EM analysis, but specific techniques are not presented to mitigate the EM effects. Moreover, the cell-internal EM is not referred.

The flow options to analyze the impact of the EM have only been partly supported to date by layout tools. However, "Sign-off DRC w/ EM-rules" and "Sign-off Spice Simulation" with subsequent current density verification are now standard functions in state-of-the-art digital layout tools. For example, the Synopsys IC Compiler has a signal electromigration analysis and repair improving the design reliability (SYNOPSYS, 2014a) and Cadence Encounter (SUMMERS, 2013) in the running power and rail analysis take into account the electromigration (EM) model file where the various metal width and via sizes are considered. These functions are also available as stand-alone verification tools (for example, Apache Totem MMX, Mentor Calibre PERC, Tanner HiPerVerify).

Figure 2.3: Synthesis-analysis loops in the design flow for digital circuits. The critical steps - physical synthesis (a) and analysis (b) - are shown, supplemented by options to address current density and other electromigration issues (c).



Source: (LIENIG, 2013).

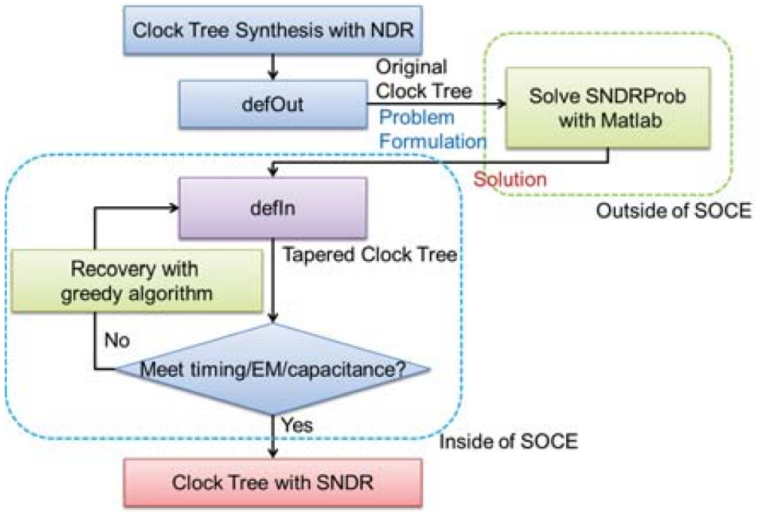
2.1.3 Smart Non-default Routing for Clock Power Reduction (KAHNG; KANG; LEE, 2013)

(KAHNG; KANG; LEE, 2013) studies the EM problem in clock networks. For new technologies the Non-Default Routing rules (NDRs) are integrated to clock network synthesis methodologies. NDRs apply wider wire widths and spacing to address electromigration constraints, and to reduce parasitic and delay variations. (KAHNG; KANG; LEE, 2013) propose a "smart" NDRs (SNDR) to substitute narrower-width NDRs for selected clock segments while maintaining all skew, slew, insertion delay and EM reliability criteria. A wire sizing problem is formulated of choosing per-segment NDRs to minimize the capacitance of the clock tree subject to electrical and reliability constraints, and a solution to this problem for each subnet is given. Then, the SNDR approach is extended to the entire clock tree by propagating skew constraints from downstream to upstream subnets. Also, a methodology to apply SNDRs without disruption of standard clock network synthesis flows is used.

The flow that implements SNDRs proposed in (KAHNG; KANG; LEE, 2013) uses a commercial place-and-route tool and is presented in Figure 2.4. Clock tree synthesis with a given fixed NDR is performed for an input design. After routing, the locations of buffers and flip-flops are extracted, which are the sources and sinks of clock nets, along with all clock wire segments, from the routed DEF (LEF DEF GUIDE, 2009) of the implemented design. From this information, the optimization instances are constructed with appropriate timing (delay, skew, slew) and EM constraints. Solving each optimization instance to obtain wire sizing solutions for every edge of each given subnet. Then the original DEF file with the obtained wire sizing solutions for each subnet is updated. The modified DEF is read back into the P&R tool, and RC values are recalculated. With the updated RC values, electrical/timing or EM reliability violations are check; if there are any violations caused by an SNDR on a wire segment, that segment is reverted to its original NDR.

SNDR methodology was executed with a 32/28nm library (SYNOPSYS, 2014b) and open-source benchmark netlists. SNDR presented power and capacitance reduction versus the fixed-NDR (4W5S) methodology used in a commercial tool.

Figure 2.4: Overall implementation flow.

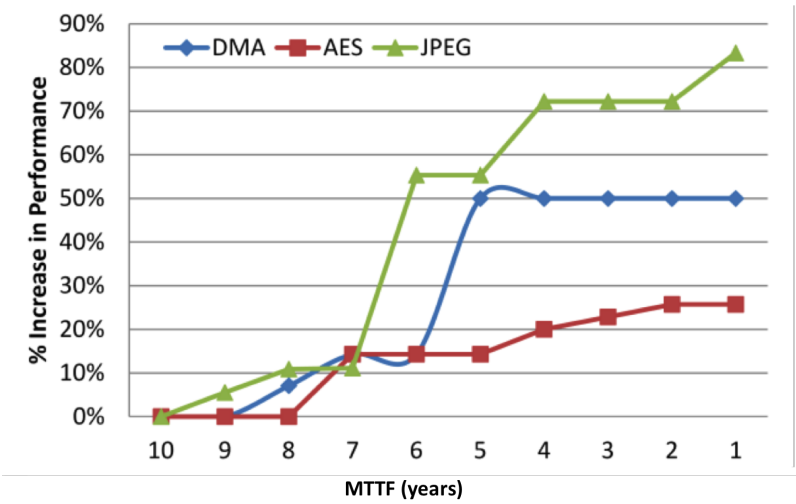


Source: (KAHNG; KANG; LEE, 2013).

2.1.4 On potential design impacts of electromigration awareness (KAHNG; NATH; ROSING, 2013)

(KAHNG; NATH; ROSING, 2013) present two studies: EM lifetime versus performance with fixed resource budget, and EM lifetime versus resource with fixed performance. AES, DMA and JPEG designs are used as example for TSMC 45GS and 65GPLUS technology libraries. (KAHNG; NATH; ROSING, 2013) show that the performance scaling achieved by reducing the EM lifetime requirement depends on the EM slack in the circuit, which in turn depends on factors such as timing constraints, length of critical paths and the mix of cell sizes. Depending on these factors, the performance gain can range from 10% to 80% when the lifetime requirement is reduced from 10 years to one year, as Figure 2.5 shows.

Figure 2.5: Percentage increase in F_{max} at 45nm due to reduced MTTF requirement.

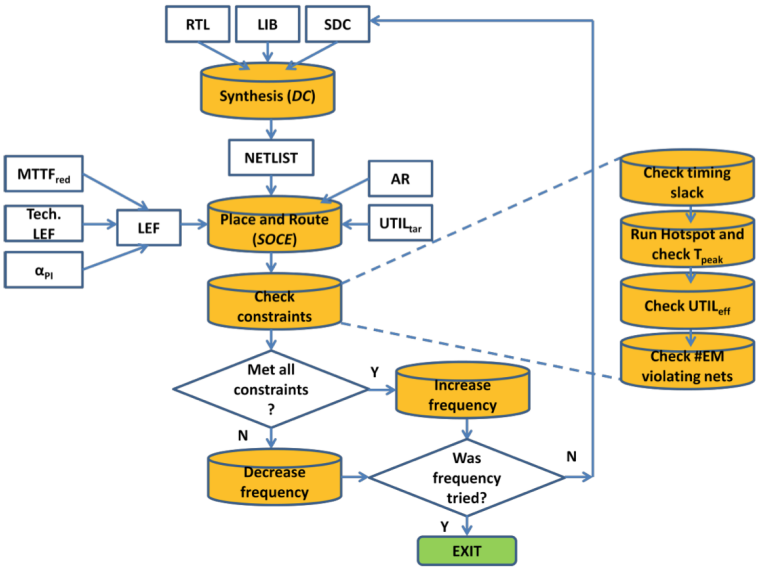


Source: (KAHNG; NATH; ROSING, 2013).

Figure 2.6 shows the flow presented in (KAHNG; NATH; ROSING, 2013) to find the highest possible maximum frequency of a design for a given reduced MTTF require-

ment. Synopsys DesignCompiler (SYNOPSYS, 2013a) and Cadence SOC Encounter (CADENCE, 2013) flows are used to synthesize the circuits and the thermal analysis is done using Hotspot. The flow used follows the same main steps presented in Figure 2.1. The steps changed to consider the EM are described in details below.

Figure 2.6: Automated flow to determine F_{max}.



Source: (KAHNG; NATH; ROSING, 2013).

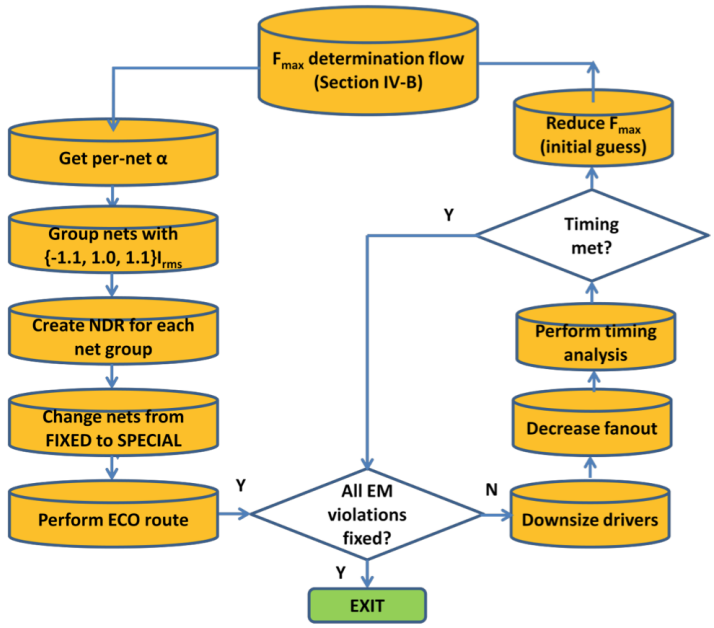
- Characterize current density limits in each metal layer in the technology LEFs based on upper bound on the peak temperature of the design (T_{UB}), switching activity, and reduced MTTF requirements (MTTF$_{red}$) using Black's Equation described in Chapter 3 (Equation 3.1).
- Place and route the post-synthesis netlist using the newly characterized technology LEF from the previous step.
- Perform post-route extraction, timing and signal integrity (SI) analysis. Fix EM violations using P&R tool commands.
- Calculate peak temperature of the design (T_{peak}) from chip and core areas, ambient temperature (T_{amb}), and power using Hotspot (SKADRON et al., 2003) calibrated to a 45nm Qualcomm SoC package.
- Check that all constraints are met.
- If all constraints are met, then increase frequency (decrease clock period in SDC) using binary search. If any constraint is violated, decrease frequency (increase clock period) using binary search.
- If the next frequency has already given a valid solution, then exit, else repeat the flow using a frequency obtained from the previous step.

(KAHNG; NATH; ROSING, 2013) also study how conventional EM fixes using per net Non-Default Rule (NDR) routing, downsizing of drivers, and fanout reduction affect

performance at reduced lifetime requirements. This study indicates, e.g., that NDR routing can increase performance by up to 5% but at the cost of 2% increase in area at a reduced 7-year lifetime requirement.

Figure 2.7 shows the flow to create NDRs per net; the following steps describe implementation in Cadence SOC Encounter (CADENCE, 2013).

Figure 2.7: Per-net NDRs flow to fix EM I_{rms} violations.



Source: (KAHNG; NATH; ROSING, 2013).

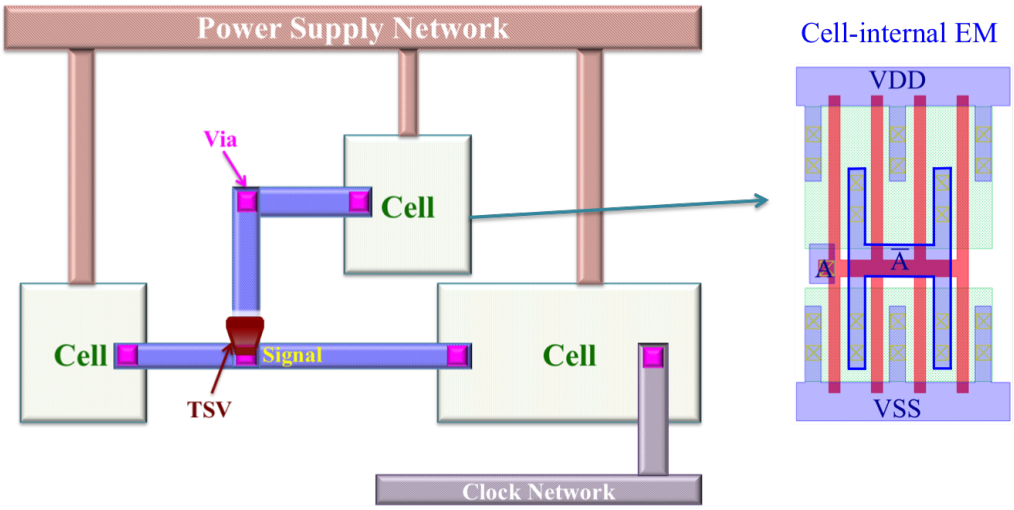
- Group EM critical nets by I_{rms} (which is a function of the switching activity on the net) and create NDRs for wire-width and spacing depending on the extent of I_{rms}.
- Find the extent of current density violations vis-a-vis LEF in each metal layer. Apply NDRs to grouped nets. If any of these nets are "FIXED" (such as clock nets), then convert them to SPECIAL nets for re-routing.
- Select all violating nets for Engineering Change Order (ECO) routing. Perform ECO routing of these nets. Then, verify AC limit violations after re-route. If there are AC limit violations, decrease fanout of these nets and perform ECO routing.
- If violations remain after the second ECO route, swap large drivers with smaller drivers and redo timing analysis. If no timing violations, then accept this new frequency and exit, else reduce frequency and run the flow presented in Figure 2.6. If frequency $\leq F_{max}$ obtained from the flow in Figure 2.6, then exit.

2.2 Mitigating the EM Effects in Different Types of Interconnections

Electromigration (EM) is an aging effect taking place in interconnect wires, contacts and vias in an integrated circuit (TU, 2003). Most works in the literature are considering the different net classes to mitigate the EM effects: TSVs (present in 3D circuits), power supply network, clock network and vias, as Figure 2.8 presents, but few works told about the EM in the signal interconnects within a standard cell (*internal-cell EM*) that is the

focus of this work. The EM effects for the different net classes and the two works that cite something about the cell-internal EM are related in the next subsections.

Figure 2.8: Different types of interconnections within the circuit where EM occurs.



Source: from author (2015).

2.2.1 TSVs

In the last years several strategies were proposed to mitigate the EM impact on through-silicon-via (TSVs). An electromigration (EM) reliability study for TSV-based 3D ICs and 3D power delivery networks (PDNs) is presented in (ZHAO et al., 2013). A transient power integrity analysis flow for lifetime prediction is developed, which integrates the EM modeling approach.

(PAK; LIM; PAN, 2013) model the EM on TSVs and local vias used together for vertical power delivery. (CHENG et al., 2013) propose a framework at architecture level to alleviate EM effects of defective TSVs. At first, the relationship between various TSV defects and EM induced TSV mean time to failure (MTTF) degradation is analyzed. Then, a framework to protect defective TSVs and improve EM MTTF by balancing their current flow directions is proposed.

2.2.2 Power Delivery Network

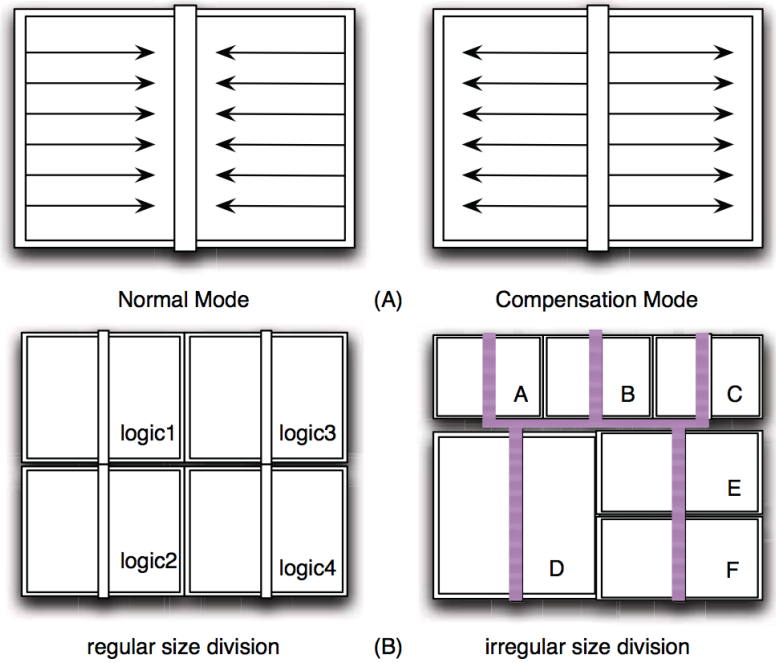
Due to shrinking wire widths and increasing current densities, there is little or no margin left between the predicted EM stress and that allowed by the EM design rules in the power delivery networks (PDNs) (FAWAZ; CHATTERJEE; NAJM, 2013). Most works in the literature are concerned with the EM effects in the power delivery network.

(ABELLA et al., 2008) presented refueling that is a microarchitectural technique to make up for EM in power/ground grids using the self-healing effect that can undo EM. This effect occurs when current flows in both directions of a wire. The parts of the wire that are prone to form voids when current flows in one direction are prone to form hillocks when it flows in the opposite direction. Thus, if the same amount of current flows in each direction, EM self-heals. It consists of injecting current whenever the amount of current in one direction is higher than the amount in the opposite direction.

Other solution based on the electromigration AC healing effect is presented in (XIE; NARAYANAN; XIE, 2012) to extend the lifetime of power supply networks. An algo-

rithm for the EM-aware design that can be integrated into the standard-cell place and route flow is also presented. The topology of power networks to produce balanced bidirectional current on power rails is changed, as Figure 2.9 shows, with compensation strip insertion. There are two operation modes: the normal mode and the compensation mode. The current flow directions on power rails are shown in Figure 2.9A. Both modes are driven by the same set of PADs to prevent PAD number increase. In the normal mode, power is supplied to the block from the Power/Ground (P/G) ring. The transistors connecting PADs and the compensation strip are off, thus the strip is in high-impedance state. In the compensation mode, the PAD supplies the compensation strip, and the P/G ring is in high-impedance state. If a block is too big to meet the IR drop requirement, it can be divided into regular or irregular sub-blocks with their compensation strips connected together as illustrated in Figure 2.9B. The sub-blocks switch into the normal or the compensation mode simultaneously.

Figure 2.9: (A) A vertical Power/Ground (P/G) strip (compensation strip) is added in the middle of the layout with two working modes (normal mode: power is supplied to the block from the P/G ring with the compensation strip in high-impedance state; compensation mode: the PAD supplies the compensation strip, with the regular P/G ring in high-impedance state); (B) chip layout divided into regular or irregular sizes with power grid.



Source: (XIE; NARAYANAN; XIE, 2012).

(MISHRA; SAPATNEKAR, 2013) overcomes the limitations and drawbacks that the classical circuit-level EM models have: first, they do not accurately capture the physics of degradation in copper dual-damascene (CuDD) metallization, and second, they fail to model the inherent resilience in a circuit that keeps it functioning even after a wire fails. For a single wire, this probabilistic analysis encapsulates known realities about CuDD wires, e.g., that some regions of these wires are more susceptible to EM than others, and that void formation/growth show statistical behavior. So, (MISHRA; SAPATNEKAR, 2013) applies these ideas to the analysis of on-chip power grids and demonstrate the inherent robustness of these grids that maintains supply integrity under some EM failures.

A mesh model to estimate the MTTF and reliability of power grid under the influence of EM, taking into account the redundancies due to it's mesh structure is proposed in (CHATTERJEE; FAWAZ; NAJM, 2013). To implement the mesh model, a framework to estimate the change in statistics of an interconnect as its effective-EM current varies was developed. Moreover, a fast and exact approach to update the voltage drops is presented. The proposed mesh model accounts for the redundancies in the grid based, that gives a longer lifetime than a series system, and thus obtains a more realistic estimate of grid's lifetime and reliability.

Another EM checking approach that reduces the pessimism in EM prediction for power/ground grids is presented in (FAWAZ; CHATTERJEE; NAJM, 2013). A framework for EM checking is proposed, allowing users to specify conditions-of-use type constraints that help capture realistic chip workload and which includes the use of a novel mesh model for EM prediction in the grid, instead of the traditional series model employed for EM reliability estimation. To compare the two models, the series system TTF was computed at the optimal points obtained, and the mesh model TTF was 2-3X larger than that of the series system.

2.2.3 Clock Network

At advanced process nodes, non-default routing rules (NDRs) are integral to clock network synthesis methodologies. One of the reasons for this is that the signal electromigration (EM) limits are violated by minimum-width wires when large buffers (e.g., 32X) are used to drive large fanouts (e.g., anywhere from 16 to 40 loads for each clock buffer instance in a typical buffered clock tree solution). To satisfy EM limits, wider wiring must be used (KAHNG; KANG; LEE, 2013). In this way, NDRs apply wider wire widths and spacing to address electromigration constraints, and to reduce parasitic and delay variations. However, wider wires result in larger driven capacitance and dynamic power. A practical methodology to apply "smart" NDR in standard clock tree synthesis flows is formulated in (KAHNG; KANG; LEE, 2013) to minimize wire capacitance under skew, slew, delay and EM constraints. The problem is solved for each subnet of a given clock tree and the potential for capacitance and power reduction is quantified. More details of this work are presented in Section 2.1.3.

An early work that also is concerned with EM in clock networks is presented in (PULLELA; MENEZES; PILLAGE, 1995), where an EM constraint is considered in their low-power clock tree design methodology. They optimize a clock tree with buffer insertion by decreasing wire width while satisfying bounds on process variation-dependent skew and current densities that affect directly the EM.

2.2.4 Vias

Particular attention needs to be paid to vias and contact holes, because generally the ampacity [1] of a (tungsten) via is less than that of a metal wire of the same width. Moreover, migration velocities in the via material, the diffusion barrier and the metal wire differ. Hence, vias are one of the prime points of void nucleation and thus EM failure (LIENIG, 2013).

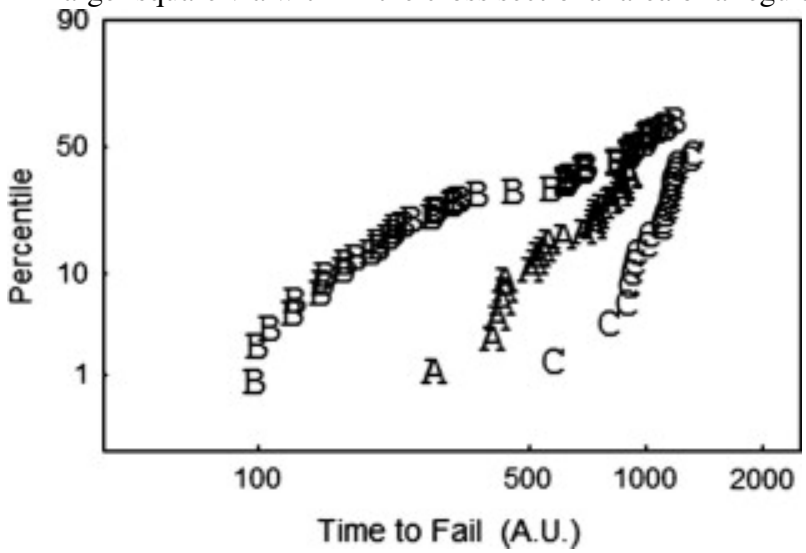
The situation can be improved when redundant vias are used (LI et al., 2005), (LIENIG, 2006). The via array geometry is crucial: multiple vias need to be arranged so that

[1] Ampacity is the maximum amount of electrical current a conductor or device can carry before sustaining immediate or progressive deterioration.

the resulting current flow and thus EM degradation is distributed as evenly as possible throughout the parallel vias (LIENIG, 2006). However, for the advanced technologies, the minimum required via to via spacing does not always scale with the via size and line width and the metal lines may not be wide enough to accommodate multiple vias along the line width.

One of the solutions for this problem is to offer multiple via size options in addition to the regular square via, like large square via and rectangular bar via (LI et al., 2014) as shown in Figure 2.10. While the large and bar via options are very helpful and efficient for circuit designs with better reliability and scaling, they also bring in challenges and complexities to the manufacturing process control. Instead of optimizing the integration process window to single size via, a balance for all via sizes is needed.

Figure 2.10: EM performance variation with different via sizes. A - 2 regular square vias along line width; B - 1 rectangular bar via with 2x the cross sectional area of a regular square via; C - 1 larger square via with 4x the cross sectional area of a regular square via.



Source: (LI et al., 2014).

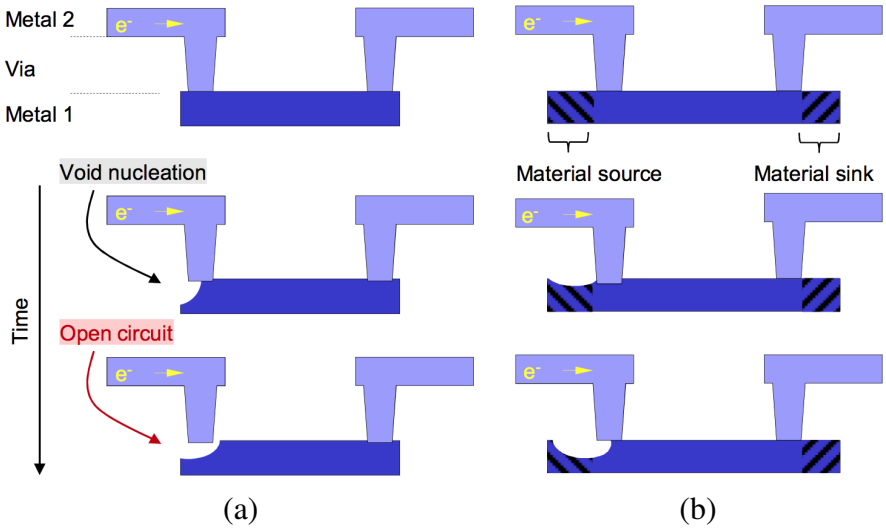
Other solution to improve the lifetime of vias is presented in (Nguyen et al., 2002) where the "reservoir effect" is used to improve the lifetime of multiple-level interconnects. Figure 2.11 shows how reservoir effect can be used considering the direction of current flow. Reservoirs can act as sources that have to be drained before voids generated by electromigration become critical to the circuit. This does not actually decrease the effects of electromigration itself, but prolongs the time to failure due to void growth (LIENIG, 2013).

The reservoir effect is also leveraged by using multiple vias, as we presented before from (LI et al., 2005), (LIENIG, 2006) works, since via arrays have a larger reservoir area than a single via. Experimental results in (Nguyen et al., 2002) indicate that the prolonged lifetime achieved is more a result of the increased reservoir area than of current sharing between vias.

The generation of voids in the vicinity of vias is strongly influenced by the geometry of the via configuration. Depending on whether a specific wire segment is connected from above or below, the configuration is called via-above or via-below, respectively (CHOI et al., 2004), (THOMPSON, 2008). Figure 2.12 shows that even a low-volume void causes a failure if placed directly underneath the via, whereas a void in a via-below configuration

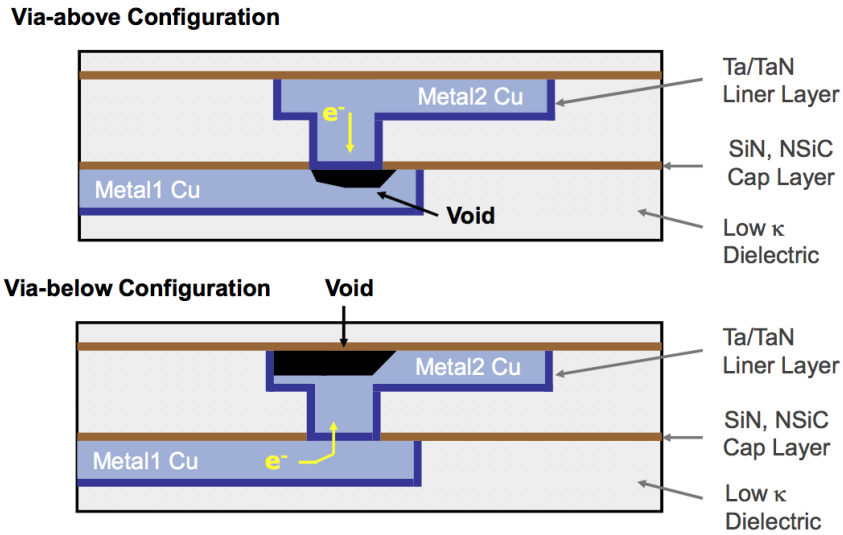
has to grow larger before the interconnect is destroyed (LIENIG, 2013).

Figure 2.11: The reservoir effect in (b) extends the lifetime of the via configuration compared to a regular via without layer overlaps (a).



Source: (LIENIG, 2013).

Figure 2.12: Via-above and via-below configurations with their different damage locations partly due to the interface/surface diffusion prevalent in copper wires.



Source: (LIENIG, 2013).

(PARK; JAIN; KRISHNAN, 2010) presents an EM check method named Via Node Vector that addresses the EM interactions and checks the EM reliability at the lead connection sites (called via node). Moreover, three new factors are introduced: length (FL), width (FW), and interaction (FB). It is a model that considers the divergence of the current flowing in the interconnects taking into account the vias.

2.2.5 Cell-internal EM

To consider the EM inside of the cells is different than to consider in other interconnections because the current flowing through the wire segments depends on the logic of the gates. To the best of our knowledge, in the literature there are just two works talking about the EM in the signal wires within the cells, (JAIN; JAIN, 2012) and (DOMAE; UEDA, 2001). (JAIN; JAIN, 2012) just cites that it is important to consider the EM effects inside of the cells, but it is not presented a solution for that. (DOMAE; UEDA, 2001) saw the EM effects in the wires inside of the cells when an inverter was fabricated and tested, and the suggested some layout changes to reduce the EM effects. These works are detailed as follow.

2.2.5.1 Accurate Current Estimation for Interconnect Reliability Analysis (JAIN; JAIN, 2012)

The section "standard-cell EM analysis and modeling" in (JAIN; JAIN, 2012) cites that robust design of standard cells itself is at the crux of an SoC's design integrity. So, the standard cells need to be reliably operating at the guaranteed conditions. During the process of library design, utmost care needs to be taken to set the correct EM targets for different cells. These targets could be in terms of the maximum operating load, frequency, voltage, input-output slew, temperature, and lifetimes.

To enable performing the standard-cell internal EM checks at chip level a method of modeling the safe frequency of the cell at different operating points is used. This information can be used to identify EM-critical cell instances and take corresponding design fixes. Good timing constraints, like a maximum frequency, are very effective in limiting the EM-critical cells, which are usually instances operating at high loads, frequencies or bad slews (typically less than few hundreds).

(JAIN; JAIN, 2012) cites that the available models to estimate RMS and AVG current are not accurate to predict the EM safety of standard cells and suggest to use SPICE simulation. As SPICE simulation is very accurate, and, can also be runtime efficient if the initial filtering of non-EM-critical cells is done properly, through library characterized data.

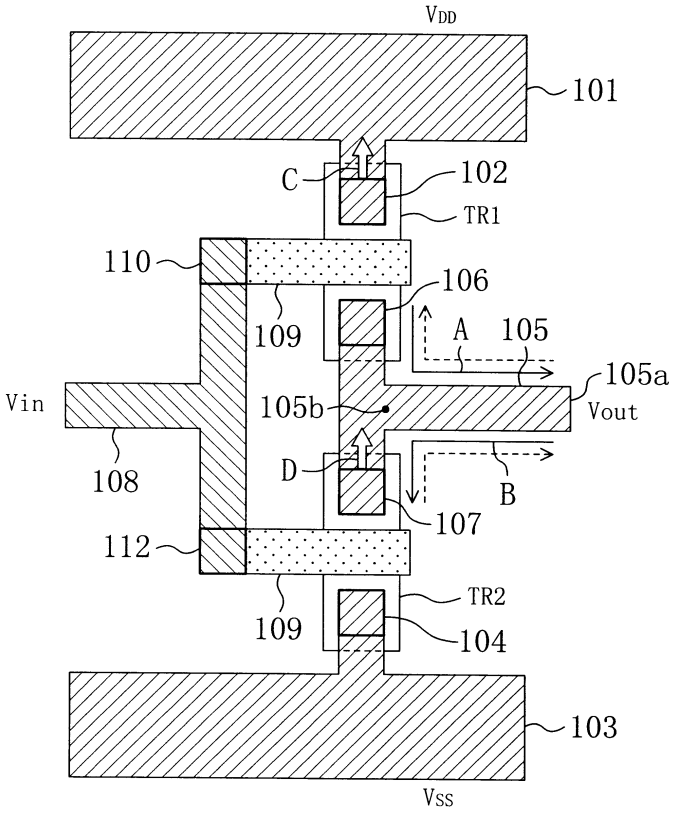
2.2.5.2 CMOS inverter and standard cell the same (DOMAE; UEDA, 2001)

(DOMAE; UEDA, 2001) presents a patent that tested the reliability of a CMOS inverter with the structure shown in Figure 2.13. As a result, an interconnection failure was spotted in the interconnection portion of the CMOS inverter. It was also found this interconnection failure in the CMOS inverter on the last stage in a standard cell composed of a plurality of CMOS inverters. The void was formed in an interconnection region near a contact connected to the source or drain of the p- and n-channel MOS transistors $TR1$ and $TR2$ as shown in Figure 2.13. Specifically, large voids were formed in the power line 101 near the first contact 102 connected to the source of the p-channel MOS transistor $TR1$ and in the output signal line 105 near the fourth contact 109 connected to the drain of the n-channel MOS transistor $TR2$.

In Figure 2.13 the broken line arrow indicates the electrons flow direction and the line arrow indicates the current direction, i.e., electron flow and current are in the opposite direction. The current flows bidirectionally between a branch point $105b$ and the output terminal $105a$ in the output signal line 105, but only unidirectionally between the third contact 106 and the branch point $105b$ and between the fourth contact 107 and the branch

point $105b$. Accordingly, electromigration might possibly happen in these regions of the output signal line 105, even though these regions are short.

Figure 2.13: A plan view of a CMOS inverter layout.



Source: (DOMAE; UEDA, 2001).

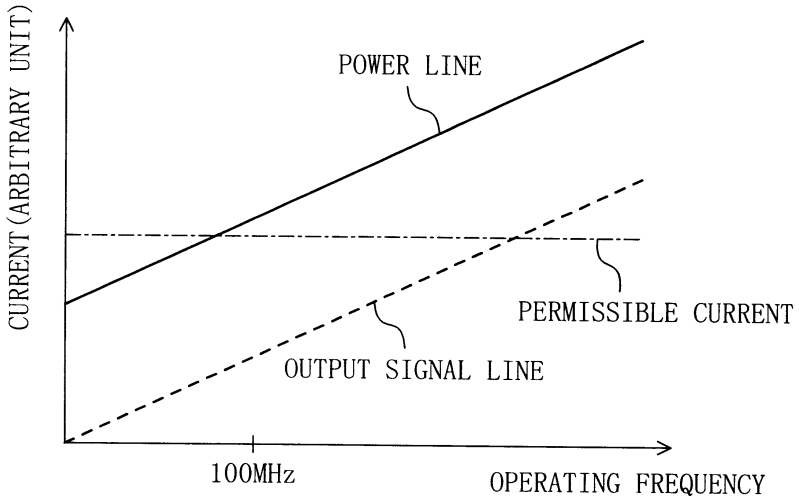
In addition, in the downsized interconnection structure for a CMOS inverter, the line width of an interconnect is substantially equal to the width of a contact as shown in Figure 2.13, contacts 102 and 104. Comparing to the conventional interconnection structure where the contacts have a metal enclosure, a void is less likely to expand in a portion of a metal interconnect, from which electrons flow out through the end of a contact. This is because while the metal atoms are moving in response to the momentum of electrons, the vacancies left by the metal atoms are filled in with those supplied from the regions of the metal interconnect surrounding the contact. In contrast, in the interconnection structure shown in Figure 2.13, a void is more likely to expand in that portion of the metal interconnect. This is because while the metal atoms are moving in response to the momentum of the electrons, no metal atoms are supplied from those regions of the metal interconnect surrounding the contact.

Figure 2.14 shows the amount of current flowing through the power line and output signal line increases proportionally to the operating frequency. However, since the operating frequency is very likely to go on rising, the amount of current flowing through an output signal line will exceed the permissible current. Thus, looking this Figure from 2001, it was expected that electromigration on an output signal line would be a serious problem in the near future. And this is what our work is presenting.

A solution to improve the reliability in the output wire and other one for the power and ground lines are presented in this invention. To reduce the electromigration effect in the output wire for the inverter in Figure 2.13, the second output signal line 105 is

connected to the contact 107, close to the drain of the NMOS transistor. So, a current flowing through the output terminal of the inverter into the second output signal line, is directly supplied to the contact (107). Thus, electrons and metal atoms, which exist in a portion of the first output signal line near the contact, do not move toward the first output signal line (line from 107 to 106 contact), then electromigration does not happen in that portion of the first output signal line near the contact 107. For the power and ground lines, electromigration happens in a portion of the power (101) and ground (103) lines near the contacts 102 and 104, Figure 2.13. In such a case, by increasing the line width of that portion of the power/ground line near the contact, it is possible to prevent a void from being formed.

Figure 2.14: The relationships between the operating frequency of a CMOS inverter and the amount of current flowing through a power line and between the operating frequency and the amount of current flowing through an output signal line.



Source: (DOMAE; UEDA, 2001).

2.3 Summary of Related Works

The main works that have contributed for our work and their characteristics are presented in Table 2.1

Table 2.1: Main related works and their main contributions.

Work	Focus	Contributions
(BALHISER et al., 2005)	nets in a digital IC design	• identify nets that are at risk of failure due to EM effects • allow targeted assessment and redesign of the identified nets
(JERKE; LIENIG, 2010)	nets in a digital IC design	• separated the nets into critical and non-critical sets by nn early-stage calculation • critical nets require special consideration during physical design and layout verification due to current density design limits
(ABELLA et al., 2008)	bidirectional wires and power/ground grids	• reduce the EM effects by driving similar amounts of current in both directions to produce a recovery
(XIE; NARAYANAN; XIE, 2012)	power/ground grids	• design methodology for self-healing EM
(MISHRA; SAPATNEKAR, 2013)	power grids	• a probabilistic analysis that encapsulates known realities about CuDD wires
(CHATTERJEE; FAWAZ; NAJM, 2013)	Mesh Power Grids	• a model to determine the failure of the grid • take into account the redundancies due its mesh structure.
(FAWAZ; CHATTERJEE; NAJM, 2013)	Power/ground Grids	• EM checking approach that reduces the pessimism in EM prediction • allow the users to specify conditions-of-use type constraints
(KAHNG; KANG; LEE, 2013)	clock network	• apply "smart" non-default routing rules (NDRs) in standard clock tree synthesis flows to minimize wire capacitance under skew, slew, delay and EM constraints
(LI et al., 2014)	vias	• use multiple via size options in addition to the regular square via, like large square via and rectangular bar via
(Nguyen et al., 2002)	vias	• the "reservoir effect" is used to improve the lifetime of multiple-level interconnects.
(PARK; JAIN; KRISHNAN, 2010)	Interconnects considering the via node	• present an EM check method that addresses the EM interactions and checks the EM reliability at the lead connection sites
(JAIN; JAIN, 2012)	standard-cell	cite that it is important to model • the average and RMS currents used for electromigration (EM) reliability analysis • the safe frequency of the cell at different operating points to be used during the library design
(DOMAE; UEDA, 2001)	output and VDD/GND wire of a CMOS inverter	Reduce the EM effects by • moving the output terminal position • increasing the line width that enclosures the contact connected to the VDD and GND wire

Source: from author (2015).

2.4 Conclusions

In the era of striking for full circuit design automation, it is important to incorporate EM aware circuit design strategies in the design, checking and verification tools. It is imperative for the electronic design automation (EDA) tools to be able to recognize and identify those circuits with critical EM implementations. In reality, this task is so com-

plicated; none of the existing EDA tools can perform and optimize EM analysis on the whole circuit, considering all the cell layouts and connections. To take more advantage of different layouts with different EM benefits, it often needs human intervention to avoid having too aggressive designs or keeping too much EM margins by the EDA tools (LI et al., 2014).

Current density verification and thus the detection of electromigration issues are already an integral part of the sign-off verification of circuit layouts. Current density violations detected during sign-off are corrected by layout modifications - by the widening of wires, for example (LIENIG, 2013).

Although there were many works aiming at mitigating the EM effects. The traditional EM analysis has focused on higher metal layers and in these types of interconnections: power supply network (Section 2.2.2), clock network (Section 2.2.3) and vias (Section 2.2.4). Thus, with the wire shrinking and increasing currents, the current densities in lower metal layers are also now in the range where EM effects are visible. So, the current flowing through the local interconnect wires within standard cells can be large enough to create significant EM effects over the lifetime of the chip. While the cell-internal signal EM problem is described in a patent (DOMAE; UEDA, 2001) and industry publications (JAIN; JAIN, 2012) as Section 2.2.5 presents, its efficient analysis is an open problem.

This work analyzes and gives a solution to improve the lifetime of the standard-cells considering the cell-internal signal EM problem.

3 MODELING CELL-INTERNAL EM

3.1 Modeling Time-to-Failure Under EM

For EM lifetime estimation, we use the well-known Black's equation (BLACK, 1969) developed by the physicist J. R. Black at the end of the 1960s:

$$TTF = A\ J^{-n} \exp\left(\frac{Q}{k_B T_m}\right) \tag{3.1}$$

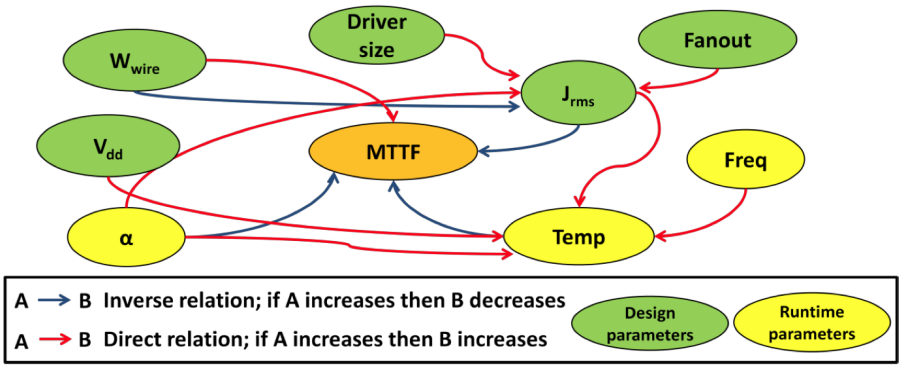
where TTF is the time-to-failure (lifetime), A is an empirical constant that depends on the material properties of the interconnect, J is the current density, the exponent n is typically between 1 and 2, Q is the activation energy, k_B is Boltzmann's constant and T_m is the metal temperature. Black's equation shows that current density J and the temperature T are deciding factors in the physical design process that affect electromigration. Current density is giving by

$$J = \frac{I_{avg}}{T_w W}, \tag{3.2}$$

where W and T_w are the wire width and thickness and I_{avg} is the average current.

As 2011 ITRS presents (ITRS, 2011), the lifetime of an interconnect is the time to reach the minimum void size which is able to electrically open the interconnect. As (KAHNG; NATH; ROSING, 2013) presents, EM lifetime is affected by design parameters such as wire width, fanout, driver size, and operating voltage - since all of these affect current density. Switching activity (α), frequency and temperature are the runtime parameters that affect EM. Figure 3.1 (KAHNG; NATH; ROSING, 2013) shows the relation to EM MTTF of these factors, with positive [negative] correlations to MTTF shown as red [blue] directed edges. For example, to meet EM MTTF margin at a given wire width upper bound we can reduce J_{rms}, and driver size, producing a slower circuit. To meet EM MTTF margin at a given performance requirement, we can increase the wire width (W_{wire}) that increases the capacitance and dynamic power.

Figure 3.1: Design and runtime factors affecting EM MTTF.



Source: (KAHNG; NATH; ROSING, 2013).

For wires with unidirectional current flow (e.g., many power grid wires), EM causes a steady unidirectional migration of metal items, and I_{avg} is simply the time average of the

current. In contrast, currents in signal wires may flow in both directions as they charge and discharge the output load.

For signal nets with bidirectional current flow, the time-average of the current waveform is often close to zero. However, even in cases where the current in both directions is identical, it is observed that EM effects are manifested. In this effect, often referred to as *AC EM*, the motion of atoms under one direction of current flow is partially, but not fully, negated by the "sweep-back" recovery effect that moves atoms in the opposite direction when the current is reversed. This partial recovery is captured by an *effective average current*, I_{avg} (LEE, 2012a; JAIN; JAIN, 2012) (also called Average Current Recovery (ACR) model (TING et al., 1993)):

$$I_{avg} = I^{+}_{avg} - \mathcal{R} \cdot I^{-}_{avg}, \tag{3.3}$$

where $\mathcal{R}$ represents the *recovery factor* that captures sweep-back. Here, I^{+}_{avg}, is the largest of the average currents (forward-direction) and I^{-}_{avg} is the smallest current (reverse-direction). For signal wires in a cell, the rise and fall cycle currents are not always in opposing directions. We consider two cases:

Case I: When the rise and fall currents, I^{r}_{avg} and I^{f}_{avg}, are in opposite directions, as in edge e_3 in Fig. 1.7(c), Eq. (3.3) yields:

$$I_{avg} = \frac{\max\left(\left|I^{r}_{avg}\right|, \left|I^{f}_{avg}\right|\right) - \mathcal{R} \cdot \min\left(\left|I^{r}_{avg}\right|, \left|I^{f}_{avg}\right|\right)}{2} \tag{3.4}$$

where the factor of 2 arises because half the transitions correspond to an output rise and half to an output fall.

In (TING et al., 1993), the Average Current Recovery (ACR) model heuristically accounts for the degree of damage recovery during opposite-polarity pulses through a single recovery parameter. The coefficient $\mathcal{R}$ accounts for the degree of damage recovery and may vary from zero to one. At $\mathcal{R}$ = 0, any annealing or damage recovery due to opposite polarity pulses is ignored, and the effective current density is due solely to the positive pulse contribution. At $\mathcal{R}$ = 1, perfect annealing occurs during negative pulses.

Case II: When the rise and fall currents are in the same direction (e.g., in edge e_1 in Fig. 1.7(c), where the charging rise current and the short-circuit current (not shown) during the fall transition both flow downwards), then

$$I_{avg} = \frac{\left|I^{r}_{avg}\right| + \left|I^{f}_{avg}\right|}{2} \tag{3.5}$$

In this work, we use a recovery factor $\mathcal{R}$ of 0.7, consistent with industry practice and published data (LEE, 2012a). We use $A = 1.47 \times 10^{7}$As/m^2 in SI units, which corresponds to an allowable current density of 10^{10} A/m^2 over a lifetime of 10 years at 378K, with an activation energy, $Q = 0.85$eV (HU et al., 2007).

3.2 Joule Heating

The flow of current in an interconnect results in an increase in temperature within the wire due to a phenomenon known as Joule heating that accelerates temperature-dependent electromigration (JONGGOOK; TYREE; CROWELL, 1999). From Eq. (3.1), a temperature rise hastens the EM-induced TTF. The temperature T_m in a wire is given by:

$$T_m = T_{ref} + \Delta T_{Joule} \tag{3.6}$$

where T_{ref} is the reference chip temperature for EM analysis and ΔT_{Joule} is the temperature rise due to Joule heating. In the steady-state, the wire temperature rises by (BANERJEE; MEHROTRA, 2001):

$$\Delta T_{Joule} = I_{rms}^2 R R_\theta \tag{3.7}$$

We can observe that the wire temperature has an inherent squared dependency on the root mean square RMS wire current, I_{rms}, of the signal wire. Here, R is the wire resistance, and R_θ is the thermal impedance of the wire to the substrate, giving by:

$$R_\theta = \frac{t_{ins}}{K_{ins} L W_{eff}}, \tag{3.8}$$

where t_{ins} is the dielectric thickness, K_{ins} is the thermal conductivity normal to the plane of the dielectric, L is the wire length, and W_{eff} is given by:

$$W_{eff} = W + 0.88 t_{ins}, \tag{3.9}$$

for a wire width W. We obtain R by parasitic extraction using a commercial tool and use $t_{ins} = 120$nm (FREEPDK45, 2011) and $K_{ins} = 0.07$W/m.K (BANERJEE; MEHROTRA, 2001).

3.2.1 Local hot spots from Joule Heating (LI et al., 2014)

(LI et al., 2014) presents the importance of the Joule heating in the interactions among the neighboring metal lines. The Joule heating can rise the temperature in the local hot spots. Local hot spots can have significant impact on the number of critical EM elements.

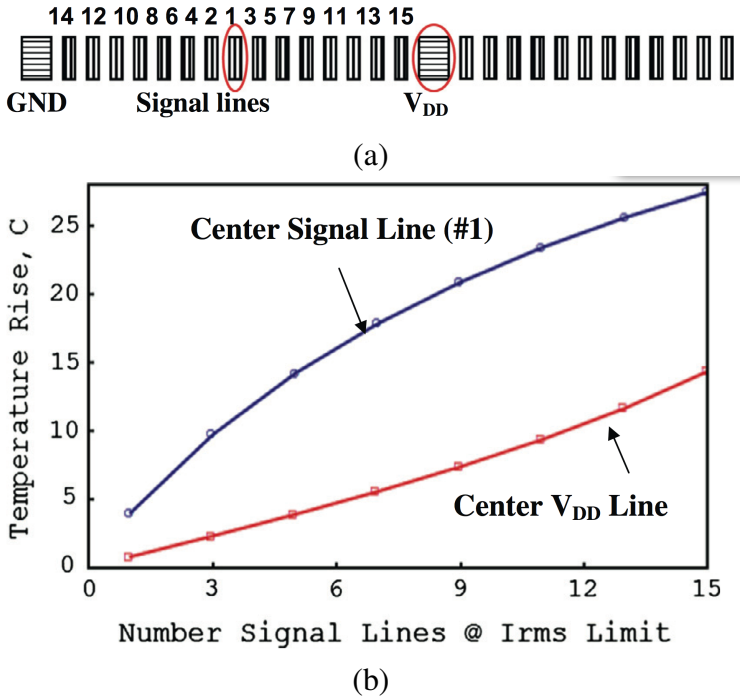
One example of the neighboring metal line interactions is presented in (LI et al., 2014) and it is illustrated in Figure 3.2. Figure 3.2(a) shows a hypothetical layout block with signal lines only carrying AC current and power lines carrying DC current. Figure 3.2(b) illustrates the Joule heating effect on the center signal line (line #1) with different number of signal lines carrying AC currents to its I_{rms} limit, which is defined to cause a 5°C temperature rise if the line is isolated. When all the signal lines carrying currents to their I_{rms} limits, the temperature rise from Joule heating (itself and its neighbors) of the central signal line can be greater than 25°C, way above that if it is isolated.

(LI et al., 2014) show that the similarly effect occurs with the interaction of the signal lines with the central VDD line, causing significant temperature rise in the VDD line as well. Though the current passing through the VDD line itself causes minimal joule heating, the neighboring signal lines acting together can heat the VDD line to higher than 10°C, which could shorten its EM lifetime by almost 50%. This 10°C Joule heating on the center VDD line will increase its equivalent critical EM count from 1 (assuming it was designed to its J_{max} limit at the nominal use temperature) to 180,000. Evaluating the I_{avg} and I_{rms} interactions and local temperature from joule heating (i.e. identifying hot spots) is an important part of the chip level EM budgeting. This is especially true for the local areas tightly packed with actively switching signal and power lines (LI et al., 2014) .

3.3 Current Divergence

In this work we are also considering the current divergence effect to calculate the effective average current through the edges of the signal wires. Current divergence addresses the EM interactions considering the vias and checks the EM reliability at the lead

Figure 3.2: An example of local Joule heating interactions caused metal line temperature rise. The numbers used in the x-axis in (b) start from the closest neighbors of the subject line (#1 signal line or the center (circled) VDD line.



Source: (LI et al., 2014).

connection sites taking into account the lead EM interaction. The current divergence was presented in (PARK; JAIN; KRISHNAN, 2010) and it is detailed below.

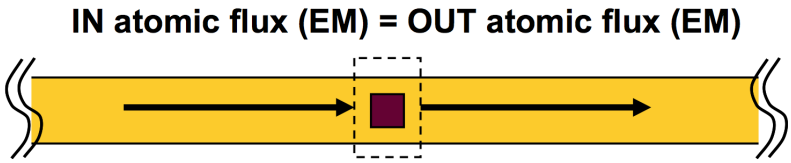
3.3.1 New electromigration validation: Via Node Vector Method (PARK; JAIN; KRISHNAN, 2010)

An EM check method named Via Node Vector is proposed in (PARK; JAIN; KRISHNAN, 2010). This method addresses the EM interactions and checks the EM reliability at the lead connection sites (called via node), different than the conventional EM check that ignores the lead EM interaction and only checks the local current densities. It converts the electrical current density of each lead into an effective current density for the EM interaction consideration.

Electromigration (EM) is atomic flux driven by electrical current and its divergence at a site leads to interconnect failure, either in form of increasing lead resistance or shorting out the circuits. The EM divergence is a net atomic flux at a site between IN and OUT electromigrated atoms. Even if the amount of atomic flux is very large along an interconnect, there can be no atomic flux divergence (EM damage) if the atomic flux is uniform along the interconnect, as Figure 3.3 (PARK; JAIN; KRISHNAN, 2010) shows.

The local current density is related to the amount of the atomic flux but does not correctly represent the divergence of the atomic flux. So, (PARK; JAIN; KRISHNAN, 2010) suggest that the best practice to check EM reliability is to limit the atomic flux divergence at a “via node” where the flux meets, such as vias, contacts, lead merge, or division points as the atomic flux is completely blocked and cannot migrate to the upper or lower layer.

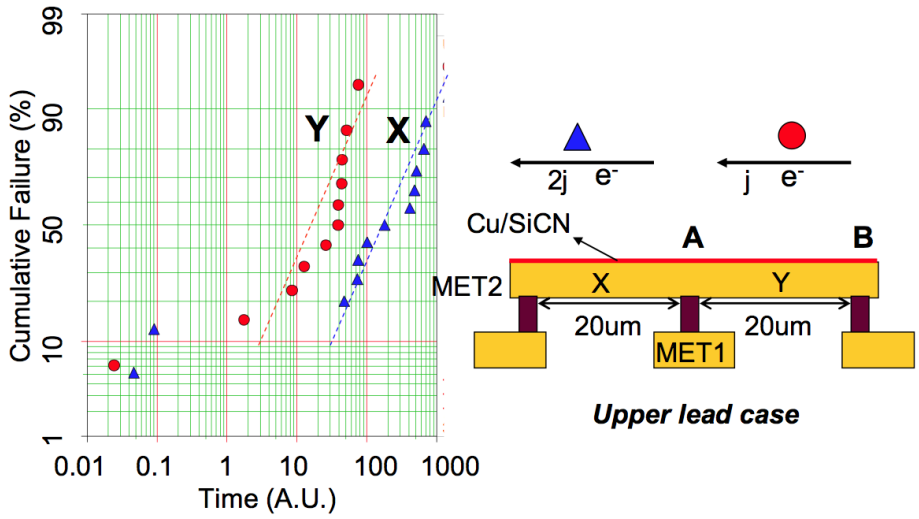
Figure 3.3: As the 'IN' and 'OUT' atomic flux are the same, the atomic flux divergence along the interconnect is zero, resulting in no EM damage.



Source: (PARK; JAIN; KRISHNAN, 2010).

A good example to explain the divergence problem giving by (PARK; JAIN; KRISHNAN, 2010) is presented in Figure 3.4, where it shows the EM lifetimes of two connected leads, X and Y. The anode end of lead Y is connected to the cathode end of lead X which is stressed at $2j$, while lead Y is at j, where j is the current density. The width and length of the two leads are the same, thus $2\times$ more current flows through X than Y. The conventional method expects faster failure for lead X with $2j$, but experiments show that lead Y (with only j) fails $10\times$ earlier. The conventional check assumes the two leads are isolated in terms of EM reliability, but they are physically connected and their atomic flux indeed interacts. Thus, the actual divergence at the via node A and via node B is not purely determined by the local current density of the each lead X and Y, respectively. Lead X has a current flow of $2j$ but is supplied a current of j from lead Y. So, the electrical divergence at via node A is just j. Lead Y has a current flow of j, but the current keeps flowing into X with a larger amount of $2j$. The atomic flux from lead Y is not accumulated at via node A, but will be transferred into lead X at a faster rate due to the higher current density of $2j$. It will eventually increase the atom depletion rate from via node B and make the EM lifetime of lead Y short. A conservative electrical way to consider this effect is to add the two current densities, which makes the current divergence $3j$ from via node B, meaning that the EM lifetime of lead Y is similar to that of an isolated single lead having $3j$ current density. Thus lead Y fails much earlier than lead X. (The $3\times$ larger current density now makes $10\times$ shorter lifetime.)

Figure 3.4: Lead Y flows at half the current density of lead X, but fails faster than lead X; contrary to the conventional EM expectation. The new via node vector method explains it well with the divergence effect.



Source: (PARK; JAIN; KRISHNAN, 2010).

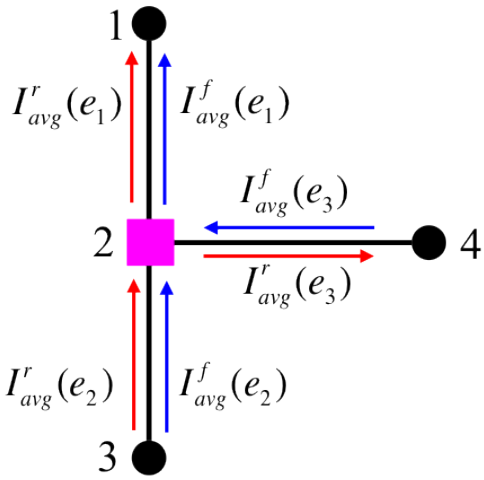
The conventional EM check ignores the lead EM interaction in circuits and only checks the local current densities. The method presented in (PARK; JAIN; KRISHNAN, 2010) addresses the EM interactions and checks the EM reliability at the lead connection sites (called via node). It converts the electrical current density of each lead into an effective current density for the EM interactions by applying three different non-electrical impacts on the atomic flux of a connected lead - length, width and interaction - to electrical current density.

In this proposed work, the width is considered when we address the current density by $(I_{avg}/(WT_w)$, where I_{avg} is the average current, W is the width of the wire (interconnection) and T_w is the thickness of the wire. The length is influenced by the "back-stress" [1] occurs in Al interconnects due to its protective oxide (TU, 2011), as in Cu interconnections the back-stress force is not significant enough, we are not considering the length. And the interaction factor doesn't matter for our case. The way we are addressing the current divergence is better explained below.

3.3.2 Applying Current Divergence in the Proposed EM model

A via in a copper interconnect allows the flow of electrical current but acts as a barrier for the migration of metal atoms under EM. Thus, the average current used for EM computation depends on the magnitude and direction of currents in neighboring wires where the metal migration flux is blocked by a via, as Section 3.3.1 presented. The computation of the average EM current can be performed according to the flux-divergence criterion presented in (PARK; JAIN; KRISHNAN, 2010) (Section 3.3.1), which says that the average EM current for a wire is the sum of the current through the wire and the divergence at the via. *This new average current replaces all average currents in Section 3.1.*

Figure 3.5: Current divergence for a multifanout tree.



Source: (POSSER et al., 2014).

Example: Consider the example of Fig. 3.5 showing the left half of the H-shaped INV_X4 (we can use any other logic gate) output wire presented in Fig. 1.7. Note that all metal wires within the H-shaped structure are routed on the same metal layer as in the Nangate 45nm library (NANGATE, 2011), regardless of direction. Here, the output pin is placed

[1] The back stress effect is proportional to JL of a lead where J is the current density and L is a lead length. The lead will have a long EM lifetime when JL is reduced (CHENG et al., 2008).

at node 2 and consequently a via is placed over this node. The arrows in Fig. 3.5 indicate the direction of electron flow of the current in this wire during the rise and fall transitions. Poly-metal contacts (nodes 1, 3) are also blocking boundaries for metal atoms, and flux divergence must be used for wires at these nodes. Since voids in Cu interconnects are formed near the vias, we consider the two vias at either end of each edge. If an edge has multiple vias (e.g., e_1 has vias at nodes 1 and 2), the EM average current considering the divergence current, ($I_{avg,d}$), uses the largest divergence.

For edge e_1, node 1 does not see a void: the electron flow in this edge, during both the rise and fall transitions, is in the direction of node 1, and EM voids are only caused by electron flow away from the via. However, for the via at node 2, there is an effective outflow and the EM average current for edge e_1 with respect to via 2, $I_{avg,d}(e_1)$, is computed using Eq. (3.5) as the rise and fall electron flows are in the same direction:

$$I_{avg,d}(e_1) = \frac{\left|I^r_{avg,d}(e_1)\right| + \left|I^f_{avg,d}(e_1)\right|}{2}$$

where

$$\begin{aligned} I^r_{avg,d}(e_1) &= I^r_{avg}(e_1) - I^r_{avg}(e_2) + I^r_{avg}(e_3) \\ I^f_{avg,d}(e_1) &= I^f_{avg}(e_1) - I^f_{avg}(e_2) - I^f_{avg}(e_3) \end{aligned}$$

The expression for $I^r_{avg,d}$ above has contributions from:

- Current in e_1, drawing metal flux away from the via, and adds to void formation.
- Current in e_2, which inserts flux into the via: although this current flows to the output load through the via at node 2, due to the blocking boundary at the via, the metal flux does not pass through, but instead, accumulates atoms, thus negating void formation.
- Current in e_3, which draws flux away from node 2.

The expression for $I^f_{avg,d}$ is similarly derived.

For edge e_3, we see Case II of Section 3.1 because the rise and fall electron flows are in the opposite direction. From Eq. (3.4),

$$I_{avg,d}(e_3) = \frac{\left|(I^r_{avg,d}(e_3)\right| - \mathcal{R} \cdot \left|I^f_{avg,d}(e_3)\right|}{2}$$

where

$$\begin{aligned} I^r_{avg,d}(e_3) &= I^r_{avg}(e_3) - I^r_{avg}(e_2) + I^r_{avg}(e_1) \\ I^f_{avg,d}(e_3) &= I^f_{avg}(e_3) + I^f_{avg}(e_2) - I^f_{avg}(e_1) \end{aligned}$$

The algorithm 3.1 presents the current divergence calculation, where all vias (vias and contacts) v are visited. For each via v, the neighbor edges e are stored in $nbr_edges(v)$. For each edge e in $nbr_edges(v)$, the $I^r_{avg,d}$ and $I^f_{avg,d}$ are calculated as Example presented. The $I_{avg,d}$ of the edge is calculated using the Eq. (3.4) when the rise and fall electron flows are in the opposite direction and the Eq. (3.5) when the electron flows are in the same direction. Finally, the $I_{avg,d}$ value of the edge considering that via is stored. After all vias and all edges be visited, each edge e is visited again. The $I_{avg,d}$ for each edge e will be the largest divergence among all vias.

Algorithm 3.1 Current Divergence Calculator

```
    V = List of all Vias
    nbr_edges(v) = List of neighboring edges in V
 1: for each v in V do
 2:     Get neighbors of v store it in nbr_edges(v)
 3:     for each edge e in nbr_edges(v) do
 4:         Calculate I^r_avg,d, I^f_avg,d using (PARK; JAIN; KRISHNAN, 2010)
 5:         Calculate I_avg,d using Eq. (3.4) or Eq. (3.5)
 6:         Store this value as I_avg,d(e, v)
 7:     end for
 8: end for
 9: for each edge e do
10:     I_avg,d = max_{i∈V}(I_avg,d(e, i))
11: end for
```

3.3.3 The Impact of Blech Length on Cell-Internal Interconnects

As pointed out by Blech (BLECH, 1976), the migration of metal atoms results in a concentration gradient and a back stress that opposes the electron wind force that causes electromigration. This is typically translated into a criterion whereby the product of the current density and wire length must exceed a critical value; if it does not, the wire is deemed immortal.

Although intracell wires are short, the Blech criterion cannot be applied directly to signal interconnects in standard cells, as indicated in (JAIN; JAIN, 2012; LEE, 2012a). This may also be explained by observing that the bidirectional nature of AC EM does not allow a substantial buildup in the concentration gradient, and therefore the back-stress that opposes the electron wind is limited. For Vdd and Vss wires, although the wires shown in an individual cell may be short, they are typically concatenated along an entire row of standard cells, implying that the actual length of the wire is much larger than the short segment seen in the layout schematic of a single cell, to the point where the length of the wire does not make it immortal under the Blech criterion.

3.4 Conclusions

In this section we presented how we are modeling the cell-internal EM. To calculate the lifetime we are using the Black's equation (Eq. 3.1), where the current density J is calculated using the AVG current (I_{avg}). When the rise and fall currents are in opposite directions, I_{avg} is calculated as in Eq. 3.4, using the recovery factor. When the currents are in the same direction, I_{avg} is calculated using Eq. 3.5.

The Joule heating effects are incorporated in the lifetime calculation using Eq. 3.7. Moreover, the current divergence is also considered in our work on the computation of the average EM current and consequently computing the lifetime, as Section 3.3 presented.

4 CURRENT CALCULATION

This chapter presents how the average and RMS current values are calculated to model the EM effects in this work.

For a standard cell with m output pin positions, characterization for delay and power can be performed at any one of the pin positions. Since the cell-internal wire parasitics in a standard cell are negligible and are dominated by transistor parasitics, this characterized value is accurate at all other pin locations and practically does not affect the cell timing. This is also true for the transients on the Vdd and Vss pin networks, which are essentially independent of the pin positions.

The evaluation of EM TTF requires a characterization of (a) the average and RMS currents through a Vdd/Vss line and (b) the average currents, I^r_{avg} and I^f_{avg} and the RMS current I_{rms}. All of these parameters are dependent on the pin position, as demonstrated in Fig. 1.7, and an obvious approach would be to enumerate the characterization over all possible combinations. For a library with N_{lib} cells, each with an average of m output pin positions, d Vdd pin positions and s Vss pin positions, this implies $m \times d \times s$ characterizations. However, given that EM evaluations in Vdd, Vss, and signal nets are independent, this can be brought down to $m + d + s$ characterizations. With this reduction, the CPU time required for standard cell characterization is given by:

$$T_{char} = (m + d + s) \cdot N_{corners} \cdot N_{lib} \cdot T^{avg}_{char,cell} \tag{4.1}$$

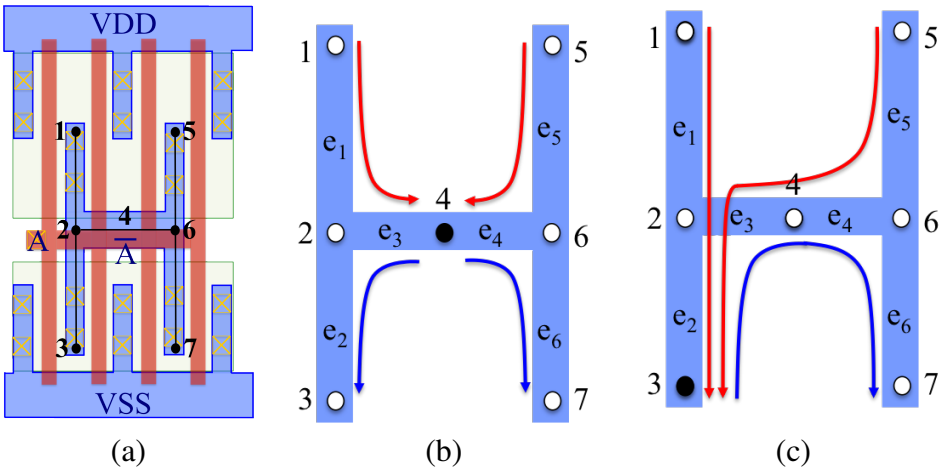
where $N_{corners}$ represents the number of corners at which the cell is characterized, and $T^{avg}_{char,cell}$ is the average characterization time (typically SPICE simulations for the output rising/falling cases) for each cell. A typical library may have $N_{lib} = 200$ cells. In our experiments, the average characterization time to build the 7×7 .lib table for a cell in the 45nm NANGATE library is found to be $T^{avg}_{char,cell} = 17.5$s. For the NANGATE library, the average number of pin positions $m = 12$, $d = 10$, $s = 10$, and the number of corners, $N_{corners} = 15$. This yields $T_{char} = 19$ days to characterize the library, which is $(m+d+s)$ times (=32× for this example) the cost of characterizing each cell at one pin position for output, Vdd and Vss pins. At more advanced process nodes, the number of corners goes up significantly, and therefore T_{char} can be much higher if the corners characterization are not parallelized.

In this work, we show that a simpler approach is possible, speeding up the characterization time by a factor of almost $(m + d + s)$, 32 for our example above. This implies that the above 19-day characterization can be conducted more practically, in about half a day. Our procedure extracts the average and RMS current information from the same simulations used for delay and power characterization, at a *reference pin position*, and then uses inexpensive graph traversals to evaluate EM for other pin positions. In other words, the additional overhead over conventional cell characterization is negligible.

To illustrate the EM characterization procedure for the output signal wire, consider INV_X4 in Figure 4.1 with the output pin at node 4. We will temporarily ignore short-circuit and leakage currents to simplify the example. Here, all PMOS [NMOS] devices are identical and inject equal charge/discharge currents. Figure 4.2 presents an example using the average current values for the rise transition from a SPICE simulation. Figure

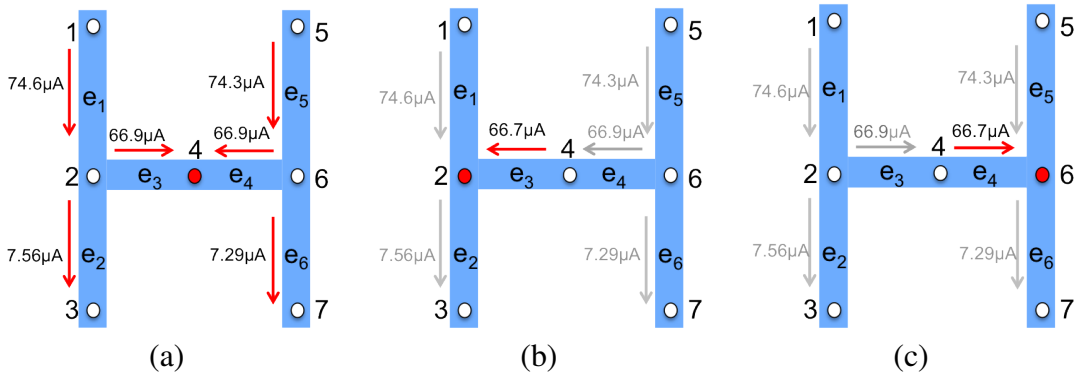
4.2(a) presents the values when the output pin is at node 4 (reference pin position). When the pin is moved to node 2 [node 6], the distribution of currents in the branches remains similar, except edge e_3 [e_4], which now carries an almost equal current in the opposite direction. Figure 4.2(b) shows the average current values when the output pin is moved to node 2, where just the current through the edge e_3 changes, the values and arrows in grey show the unchanged values and current directions when the pin is moved. The same happens when the pin is at node 6, as Figure 4.2(c) shows. Therefore, the Joule heating and EM lifetime for each edge are unchanged, and only the current divergence calculations change because the current direction changed.

Figure 4.1: (a) The layout and output pin position options for INV_X4. Charge/discharge currents when the output pin is at (b) node 4 and (c) node 3. The red [blue] lines represent rise [fall] currents.



Source: (POSSER et al., 2014), (POSSER et al., 2015 - under review).

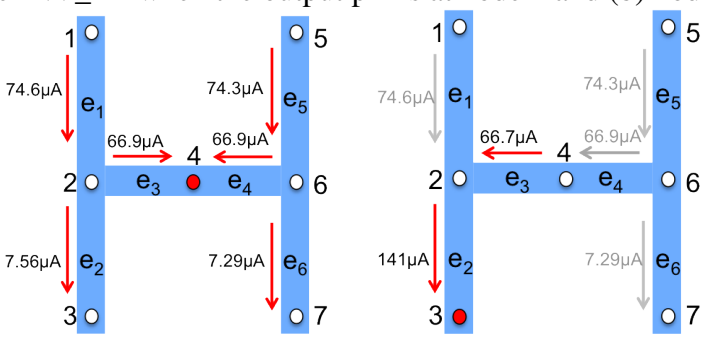
Figure 4.2: (a) AVG current values in Ampere (A) for the rise transition from SPICE simulation for the INV_X4 when the output pin is at node 4, (b) node 2 and (c) node 6.



Source: from author (2015).

When the pin is moved from node 4 to node 3, the PMOS current injected at node 5 is redirected to also flow through e_2 and e_3. The only changed current magnitudes correspond to segments e_2 and e_3; those for the other wire segments remain almost the same since intracell wire parasitics are small, as Figure 4.3 shows.

Figure 4.3: (a) AVG current values in Ampere (A) for the rise transition from SPICE simulation for the INV_X4 when the output pin is at node 4 and (b) node 3.



(a) (b)

Source: from author (2015).

Both cases above show incremental changes in current flow patterns when the pin is moved. Similar observations may be made when the Vdd and Vss pins are moved: in each case, the difference from moving a pin arises because of a redirection of a set of currents. These facts indicate that it may be possible to reduce the characterization effort by performing a single SPICE simulation for one pin position, called the *reference case*, and inferring the current densities for every other pin position from this data by determining the current redirection. We develop a graph-based method for determining this redirection, and an algebra for computing I_{avg} and I_{rms} for each pin position based on the values from the reference case.

The reference case is characterized for a fixed reference frequency, f_{ref}, chosen to be 1GHz in our experiments. If a given design operates at a frequency f and an activity factor α, as long as the circuit operates correctly at that frequency (i.e., all transitions can be completed), it is easy to infer the average and RMS currents in each branch. The average and RMS currents are multiplicatively scaled by factors of $\alpha f/f_{ref}$ and $\sqrt{\alpha f/f_{ref}}$, respectively.

4.1 Current Flows Using Graph Traversals

We present a graph-based algorithm that computes the currents through each edge when the pin position is moved from the reference case to another location. Our algorithm captures the effect of charge/discharge currents, short-circuit currents, and leakage currents (neglected in the example above), and its pseudocode is shown in Algorithm 4.1. For the output net (but not for Vdd/Vss nets), the short-circuit and leakage currents are unaffected by the pin location, and for all nets, Figures 4.1, 4.2 and 4.3 show that the flow of the charge/discharge currents is affected by the output pin position. Coupling capacitance currents are the same for almost all nets since moving the pin does not significantly change the transient waveforms in these nets. Appendix B explain why the coupling capacitances currents are also considered.

Our algorithm uses graph traversals to trace the change in the current path when the pin position is moved from the reference pin position, *ref*, to any candidate pin position on the output net, as enumerated in a candidate set C. Lines 1–6 perform a SPICE simulation at reference pin location *ref* to compute each average and triangle representations for edge currents during rise and fall on the output net, and over the cycle for the Vdd and Vss components. The charge/discharge, short-circuit/leakage and coupling capacitance

currents for each edge are determined from the simulation.

Algorithm 4.1 Efficient cell EM current characterization.

Input: Undirected graph $G(V, E)$ with separate connected components for the cell output, Vdd, and Vss nets; Reference pins *ref* for output, Vdd, and Vss for each connected component $\in V$; Set of candidate pin positions $C \subseteq V$ for output, Vdd, and Vss components.

Output: I_{avg} for all Vdd and Vss edges, $I^{+}_{avg}(e)$, $I^{-}_{avg}(e)$ for all output edges, $I_{rms}(e)$ $\forall\, e \in E\, \forall$ pin positions in C.

1: SPICE-simulate the cell with the output, Vdd, and Vss at *ref*, find triangle representations, average of edge currents during rise, fall.
2: **for each** connected components $\in$ Vdd, Vss, output **do**
3: **for each** current injection point j **do**
4: $P_j^{\{r/f\}}$ = {charge/discharge} path from j to *ref*.
5: Find charge/discharge, short-circuit/leakage, and coupling capacitance currents injected at j.
6: **end for**
7: **for each** pin position $i \in C$ **do**
8: Compute unique path P_i from *ref* to pin position i. The direction of P_i is from *ref* to i for output and Vss, and from i to *ref* for Vdd.
9: **for each** current injection point j **do**
10: New {charge,discharge} path from j to i, $P_j'^{\{r/f\}}$ = algebraic sum of paths P_i and $P_j^{\{r/f\}}$.
11: Update the current for each edge in P'_j, For the output net, update only the {charge,discharge} current, keeping short-circuit/leakage, and coupling capacitance currents unchanged; for Vdd/Vss nets, update all currents, except coupling capacitance currents which are unchanged.
12: **end for**
13: Compute $I_{avg}(e)$ for Vdd/Vss or $\{I^{+}_{avg}(e),\ I^{-}_{avg}(e)\}$ for output, as well as $I_{rms}(e)\ \forall\, e \in E$ for pin position i.
14: **end for**
15: **end for**
16: **return**

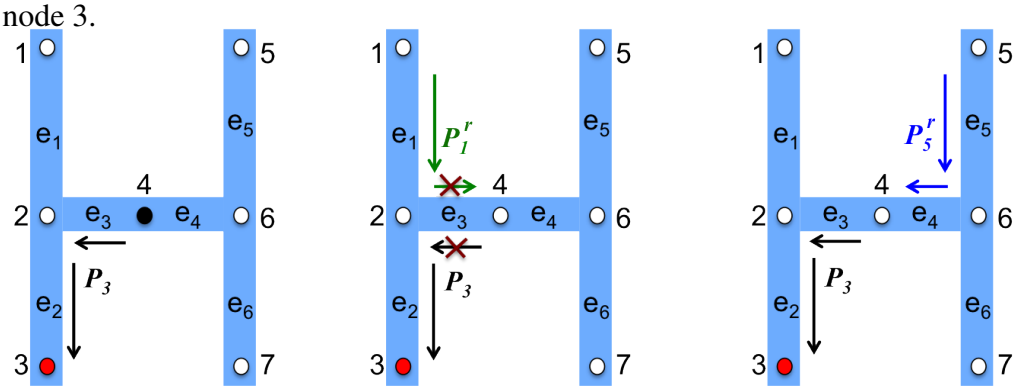
The output metallization has several points that are connected to the NMOS and PMOS transistors: we refer to these as *current injection points*. For example, in Fig. 1.7(b), the NMOS and PMOS current injection points are at nodes {1,5} and {3, 7}, respectively. Next, in the **for** loop that commences at line 7, we determine the current contribution for each candidate pin position in C. The graph-based approach determines the unique path P_i from the reference pin position *ref* to pin candidate i (line 8). Note that the Vss pin draws current out from the cell while the Vdd pin injects current, and therefore the direction of the path P_i is reversed for the two cases. For the output pin, we use the same direction as the Vss pin, but the precise direction does not matter due to the max/min operators used in Eq. (3.4).

For each current injection point, the charge/discharge path for pin candidate i (lines 9–12) is the algebraic sum of P_i and the charge/discharge path P_j for the reference pin position. The currents are updated in line 13.

Example (output pin): The key idea is illustrated in Fig. 4.4 for the rise transition when

the pin is moved from reference node 4 to node 3: the unique path P_3 between these nodes is shown at left. The two figures on the right show the algebraic addition of path P_3 with paths P_1^r and P_5^r, respectively, corresponding to the two rise current injection points. After cancellations, the resulting path successfully shows the new path for charging currents: $\{e_1, e_2\}$ for the PMOS current from node 1, and $\{e_5, e_4, e_3, e_2\}$ for the PMOS current from node 5. The charge/discharge currents are updated in lines 9–11, while the short-circuit and leakage contributions are the same as the reference case.

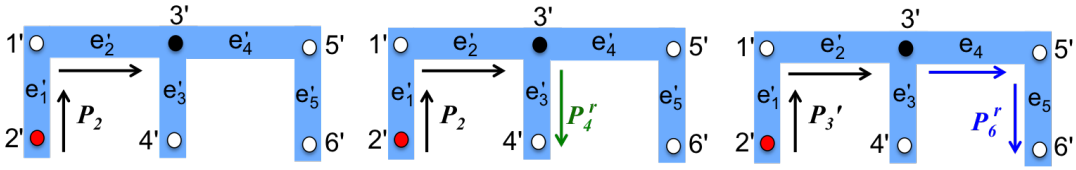
Figure 4.4: Recomputation of the rise currents when the pin is moved from reference node 4 to node 3.



Source: (POSSER et al., 2014), (POSSER et al., 2015 - under review).

Example (Vdd pin): Fig. 4.5 shows an example of how our graph-based algorithm is applied for the Vdd pin. The example considers the case when the pin is moved from reference node $3'$ to node $2'$: the unique path P_2 between these nodes is shown at left. Note that according to line 6, the direction of this path is the opposite of that used for the output and Vss components. The algebraic addition of path P_2 with paths P_4^r and P_6^r is shown on the two figures on the right, respectively, corresponding to the two rise current charging points. The resulting paths for charging currents are: $\{e'_3, e'_2, e'_1\}$ for the PMOS current from node $4'$, and $\{e'_5, e'_4, e'_2, e'_1\}$ for the PMOS current from node $6'$.

Figure 4.5: Our graph based algorithm applied to the Vdd pin when the pin is moved from node $3'$ to node $2'$.



Source: (POSSER et al., 2015 - under review).

4.2 Algebra for Average/RMS Current Updates

The current waveforms in the wire segments, for the rise and fall transitions, are used to calculate the RMS and effective average current through the wire: the former is used to measure self-heating, and the latter is used in the EM TTF formula. We now develop an algebra for efficient RMS and effective average current updates for various pin positions, given information for the reference case.

4.2.1 Algebra for Computing Average Current

For edge e, I_{avg} during a rise or fall half-cycle is given by:

$$I_{avg}(\mathrm{e}) = \frac{1}{T/2}\int_0^{T/2} I(\mathrm{e})(t)dt = \frac{1}{T/2}\sum_{i\in S}\int_0^{T/2} I(p_i(e))(t)dt \tag{4.2}$$

where the summation is over the set S of all current insertion points whose currents contribute to the current in edge e.

When the pin is moved, the set S is modified, and some entries are added and removed to the set. For example, in Figure 1.7, when the pin is moved from node 4 to node 3, the current in edge e_2 has new contributions from current insertion points 5 (rise) and 7 (fall) and a removal of the contribution from point 3; the current in e_3 must subtract the contribution of current insertion point 1 (rise) and 3 (fall), and add contributions from insertion points 5 (rise) and 6 (fall). To perform these operations, we can simply add or subtract the average currents associated with the corresponding current insertion point. For a current $I(p_i)$ from a pin insertion point p_i that is added or subtracted, we can write

$$\begin{aligned}(I(\mathrm{e}) \pm I(p_i))_{avg} &= \frac{1}{T/2}\int_0^{T/2}(I(\mathrm{e})(t) \pm I(p_i))dt \\ &= I_{avg}(\mathrm{e}) \pm I_{avg}(p_i)\end{aligned}$$

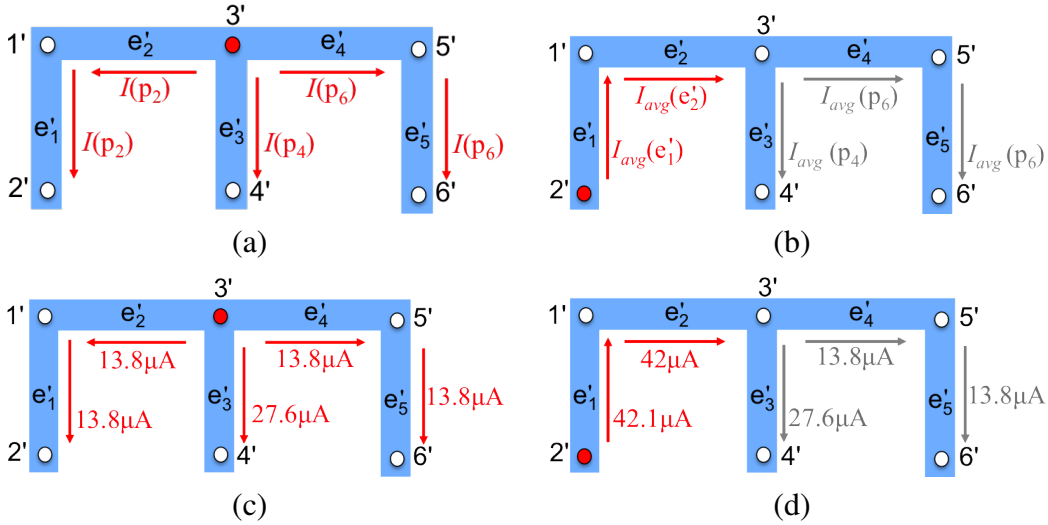
Therefore, I_{avg} updates for a new pin position simply involve add/subtract operations on average reference case currents.

Example: For the Vdd net example shown in Figure 4.5, we illustrate how the average current values are updated. Figure 4.6(a) and (b) show the formal representation of how the currents change when the pin is moved from node $3'$ to node $2'$, while Figure 4.6(c) and (d) show the SPICE simulation results when the pin is at node $3'$ and at node $2'$, respectively. Figure 4.6(a) shows the rise currents $I_{avg}(p_i)$ charging the pin insertion points p_i when the Vdd pin is placed at node $3'$. In this example, for the INV_X4, there are three insertion points, $2'$, $4'$ and $6'$. When the pin is moved from node $3'$ to node $2'$, the currents through the edges e'_3, e'_4 and e'_5 remain the same and are shown in a grey color in Fig. 4.6(b) and (d). The currents that must be updated are those through the edges e'_1 and e'_2, $I_{avg}(\mathrm{e}'_1)$ and $I_{avg}(\mathrm{e}'_2)$, respectively. Calculating by our algebra and using the notation and values in Figure 4.6, $I_{avg}(\mathrm{e}'_1)$ and $I_{avg}(\mathrm{e}'_2)$ are each given by:

$$I_{avg}(e'_1) = I_{avg}(e'_2) = I_{avg}(\mathrm{p}_4) + I_{avg}(\mathrm{p}_6) = 27.6\mu A + 13.8\mu A = 41.4\mu A$$

Comparing the calculated by our algebra with the value from SPICE simulation for the new pin position, this value is seen to be very close to the actual value of 42μA.

Figure 4.6: The Vdd pin position options for INV_X4 and the current values when the Vdd pin is at (a) and (c) node 3′ and (b) and (d) node 2′.



Source: (POSSER et al., 2015 - under review).

Example for the output pin: Using the AVG current values (in Ampere) in Figure 4.3, when the pin is moved from node 4 to node 3, the current in edge e_2 has the contribution from the current insertion point 1 (74.6μA) and a new contribution from current insertion point 5 (74.3μA) and a removal of the contribution from insertion point 3 (7.56μA). Then, the current through e_2 when the pin is at node 3 is giving by 74.6μA + 74.3μA - 7.56μA = 141μA, as Figure 4.3(b) shows. The current in e_3 must subtract the contribution of current insertion point 1 (74.6μA), and add contributions from insertion point 5 (74.3μA), so the current through e_3 is giving by 66.9μA - 74.6μA + 74.3μA = 66.6μA, practically the same as computed by SPICE simulation (as shown in Figure 4.3(b)) that was 66.7μA.

4.2.2 Algebra for Computing the RMS Current

The waveform for the current drawn by each device may be approximated by a triangle with height I_a, and with a nonzero current for a period of T' seconds, where $T' < T$, the clock period (this current model is widely used). It is well-known (NASTASE, 2013) that the RMS value of such a waveform is

$$I_{rms,\Delta} = I_a \sqrt{\frac{T'}{3T}} \tag{4.3}$$

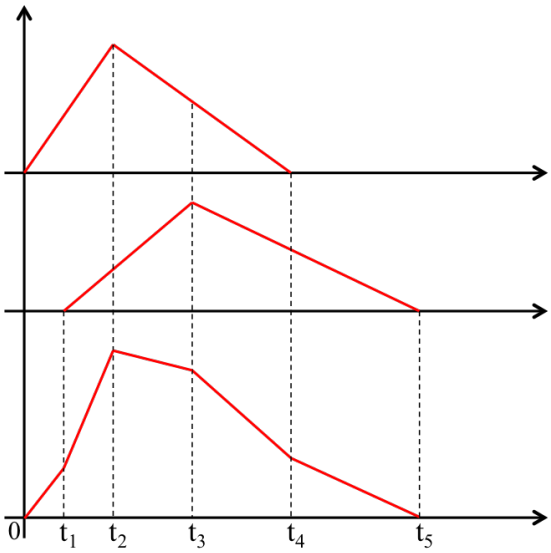
Due to the tree structure of the output wire, the current in each edge is a sum or difference of a set of such triangular signals, and this set can be determined based on a tree traversal. The sum (or difference) of a set of triangular waveforms, potentially each with different heights, start times, and end times, can be represented as a piecewise linear waveform, and thus each edge current has this form. To find the RMS value of such a piecewise linear waveform, we can decompose it into a set of nonintersecting (except at the edges) triangles and trapezoids, as shown in Figure 4.7.

The RMS for this waveform can be shown to be:

$$I^2_{rms} = \sum_{\text{all triangles } i} I^2_{rms,\Delta_i} + \sum_{\text{all trapezoids } i} I^2_{rms,trap_i} \tag{4.4}$$

To use the above equation, we use Equation (4.3) for the RMS of a triangular waveform, and the following formula for the RMS of a trapezoid bounded by the time axis,

Figure 4.7: The sum of the two upper triangular waveforms can be represented as a set of piecewise triangular or trapezoidal segments (below).



Source: (POSSER et al., 2014), (POSSER et al., 2015 - under review).

with value I_b at time b and I_c at time c, where $c > b$:

$$I_{rms,trap} = \sqrt{\frac{(I_b^2 + I_b I_c + I_c^2)\,(c-b)}{3T}} \tag{4.5}$$

For INV_X4, since the transistors of each type are all identical and are driven by the same input signal, each PMOS [NMOS] device injects an identical charging [discharging] current waveform; however in general, the currents may be different. Since the intracell resistive parasitics of the output metallization are small, some combination of these nearly unchanged currents is summed up along each edge during each half-cycle. The set of triangular PMOS waveforms that contribute to the current in each edge in Fig. 4.1 is simply the set of PMOS devices i whose charge or discharge path (Algorithm 4.1) traverses edge i. When the output is moved from node 4 to node 3, the current through an edge loses some set membership and gains others. The updated set of triangles add up, in general, to a waveform with triangles and trapezoids, whose RMS value is given by Equation (4.4). For the Vdd and Vss rails, the currents are updated in the same way. Vdd rail injects current to charge the PMOS devices and the Vss rail discharge the current from the NMOS transistors.

The RMS current value for the entire clock period considering the rise and fall transitions is calculated as:

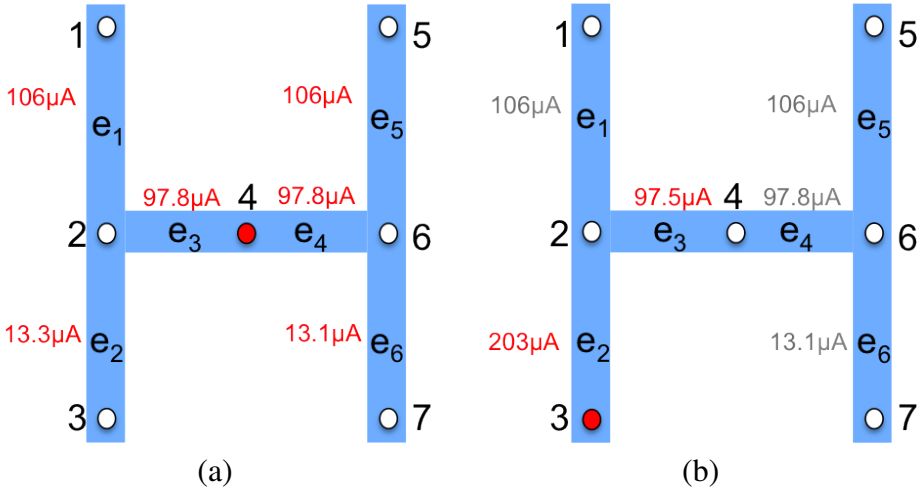
$$I_{rms} = \sqrt{\frac{(I_{rms}^f)^2 + (I_{rms}^r)^2}{2}} \tag{4.6}$$

where I_{rms}^f is the RMS current during the fall period, i.e., during half period and I_{rms}^r is the RMS current during the rise period, i.e., during the other half period.

4.2.2.1 Example

Figure 4.8 shows the RMS current values in Ampere (A) for the rise transition from SPICE simulation for the INV_X4 when the output pin is at node 4 (Figure 4.8(a)) and when the pin is moved to node 3 (Figure 4.8(b)).

Figure 4.8: (a) RMS current values in Ampere for the rise transition from SPICE simulation for the INV_X4 when the output pin is at node 4 and (b) node 3.



Source: from author (2015).

To calculate the RMS current, we will consider the same idea used to calculate the average current, considering the Algorithm 4.1 where a pin position is used as reference case to calculate the current for the other pin positions. In this way, the RMS current in edge e_2 has the contribution from the current insertion point 1 and a new contribution from current insertion point 5 (point 1 and point 5 have the same current value) and a removal of the contribution from insertion point 3. So, the current through e_2 when the pin is at node 3 is given by $Wave_{point1} + Wave_{point5} - Wave_{point3}$, i.e., the addition of the waveforms of the insertion point 1 and 5 ($Wave_{point1} + Wave_{point5}$) and the subtraction of the waveform of the insertion point 3 ($Wave_{point3}$).

Figure 4.9 presents the current waveforms from a SPICE simulation for the rise transition of the insertion point 1 (top wave), that is equal to the waveform of the insertion point 5, and insertion point 3 (middle wave) for the reference case of the pin position (pin at node 4). When the pin is moved to node 3, the resulting wave for the current through e_2 is the bottom wave in the Figure 4.9.

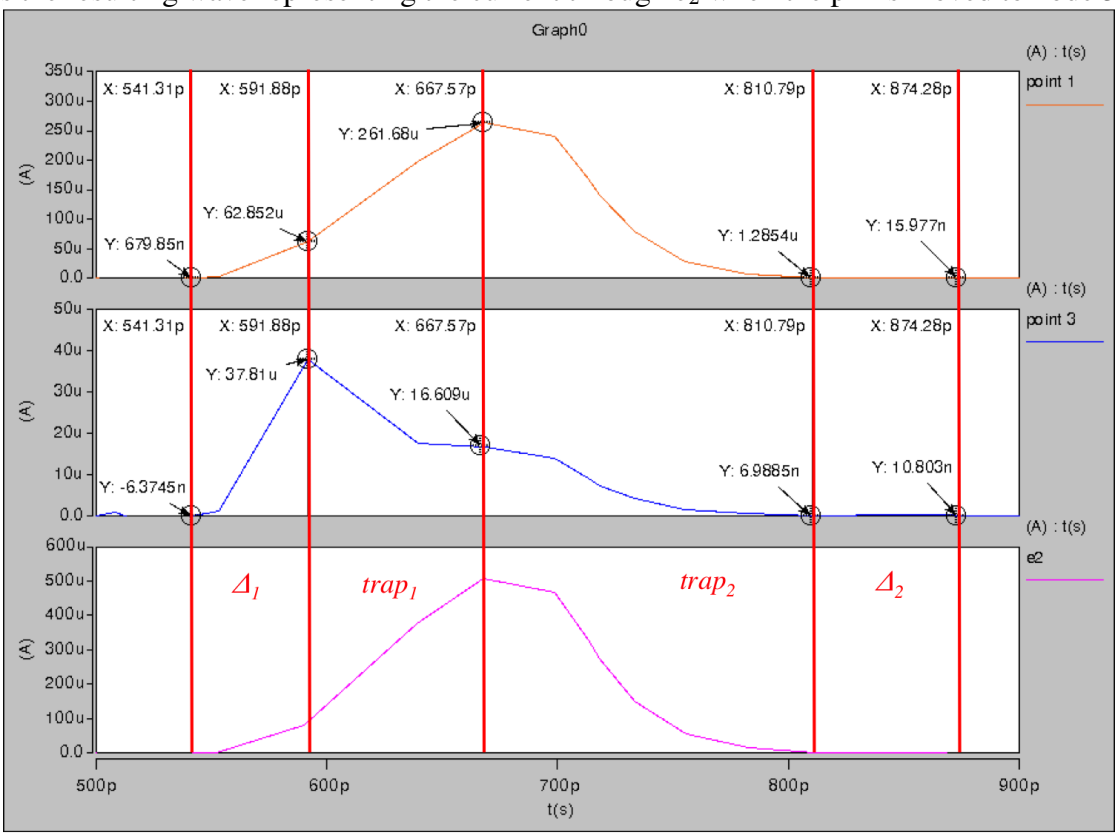
To compute the RMS current through e_2, we start computing the I_{rms} for each triangle and trapezoid of the waves, using the equations 4.3 and 4.5. The I_{rms} through the edge e_2 considering the waves in Figure 4.9 will be given by:

$$I_{rms_{e2}}^{rise\ 2} = I_{rms,\Delta_1}^2 + I_{rms,trap_1}^2 + I_{rms,trap_2}^2 + I_{rms,\Delta_2}^2$$

where

$$\begin{aligned}
I_{rms,\Delta_1}^2 &= I_{rms,\Delta_{1_{point1}}} + I_{rms,\Delta_{1_{point5}}} - I_{rms,\Delta_{1_{point3}}} \\
I_{rms,trap_1}^2 &= I_{rms,trap_{1_{point1}}} + I_{rms,trap_{1_{point5}}} - I_{rms,trap_{1_{point3}}} \\
I_{rms,trap_2}^2 &= I_{rms,trap_{2_{point1}}} + I_{rms,trap_{2_{point5}}} - I_{rms,\Delta_{2_{point3}}} \\
I_{rms,\Delta_2}^2 &= I_{rms,\Delta_{2_{point1}}} + I_{rms,\Delta_{2_{point5}}}
\end{aligned}$$

Figure 4.9: Current waveforms from a SPICE simulation for the rise transition of the insertion point 1 (that is equal of the wave for the insertion point 5) and insertion point 3 considering that the pin position is at the reference case (pin at node 4). The bottom wave is the resulting wave representing the current through e_2 when the pin is moved to node 3.



Source: (SYNOPSYS, 2013b) adapted by author (2015).

Using the values shown in Figure 4.9 of the waves for point 1 and point 3, the I_{rms} for each triangle and trapezoid is calculated. As the simulation was executed at 1GHz, the period is 1ns and the half period for the rise transition is 0.5ns, so T is 0.5ns. As the current of the injection point 5 is equal to point 1, the values are the same and, so, the values for point 1 are multiplied by 2. The units are not in the equations, where the current values are represented in μA and the time values are in ns.

$$
\begin{aligned}
I^2_{rms,\Delta_1} &= \left(62.852\sqrt{\frac{0.051}{1.5}}\right) * 2 - \left(37.81\sqrt{\frac{0.051}{1.5}}\right) \\
I^2_{rms,trap_1} &= \left(\sqrt{\frac{(62.852^2 + 62.852 * 261.68 + 261.68^2)(0.076)}{1.5}}\right) * 2 \\
&- \left(\sqrt{\frac{(37.81^2 + 37.81 * 16.609 + 16.609^2)(0.076)}{1.5}}\right) \\
I^2_{rms,trap_2} &= \left(\sqrt{\frac{(261.68^2 + 261.68 * 1.285 + 1.285^2)(0.143)}{1.5}}\right) * 2 - \left(16.609\sqrt{\frac{0.143}{1.5}}\right) \\
I^2_{rms,\Delta_2} &= \left(1.285\sqrt{\frac{0.063}{1.5}}\right) * 2
\end{aligned}
$$

resulting in

$$
\begin{aligned}
I^2_{rms,\Delta_1} &= (11.59 * 2) - (6.97) = 16.21 \\
I^2_{rms,trap_1} &= (67.10 * 2) - (10.87) = 123.33 \\
I^2_{rms,trap_2} &= (81.00 * 2) - (5.13) = 156.87 \\
I^2_{rms,\Delta_2} &= (0.26 * 2) = 0.52
\end{aligned}
$$

So, the final result will be:

$$
\begin{aligned}
{I^{rise}_{rms_{e2}}}^2 &= (16.21^2) + (123.33^2) + (156.87^2) + (0.52^2) \\
I^{rise}_{rms_{e2}} &= \sqrt{262.76 + 15210.29 + 24608.2 + 0.27} \\
I^{rise}_{rms_{e2}} &= 200.20\mu A
\end{aligned}
$$

The $I^{rise}_{rms_{e2}}$ result given by our formulation, 2e-4A, is very close to the result given by SPICE simulation, 2.03e-4A, shown in Figure 4.8. So, we can see that the formulation works as expected.

The current in e_3 must subtract the contribution of current insertion point 1 and add contributions from insertion point 5, so the current through e_3 is given by $Wave_{e_3} - Wave_{point1} + Wave_{point5}$, as the current values for the $Wave_{point1}$ and $Wave_{point5}$ are the same, the RMS current value through e_3 does not change when the pin position is changed from node 4 to node 3. In Figure 4.8 the values are a little bit different, 9.78e-5A and 9.75e-5, but they are very close, keeping the accuracy of our results.

4.3 Results

Table 4.1 shows the results of our characterization approach for the set of cells of the NANGATE cell library used in this work based on a single SPICE simulation, followed by graph traversals and the current update algebra. These results were calculated for the output pin positions. One reference case is chosen for each cell and the number of output candidate pin positions varies from 6 to 25, with an average of about 12 pin candidates per cell. The number of pin candidates is the number of simulations saved using our graph-based algorithm. The number of Vdd candidate pin positions varies from 4 to 26 and for Vss varies from 5 to 26, with an average of about 10 pin candidates per cell, as Tables 6.3 and 6.4 show. For this library, the number of SPICE simulations is therefore reduced by about 32× (12+10+10), significant and worthwhile savings even for an one-time library characterization task. The Table 4.1 shows the edge within each cell that shows the largest error for the effective average current: in each case, this error is seen to be small, 0.53% on average, while the computational savings for characterization are large. The largest error is 1.23% and the smallest error is 0.08%.

Table 4.1: Comparison with SPICE for I_{avg} calculated using our algorithm. For each cell, the value corresponds to the edge current with the largest error.

Cell	**# Candidates**	**SPICE**	**Ours**	**Error (%)**
NAND2_X2	8	4.72e-5	4.70e-5	0.32%
NAND2_X4	10	4.27e-5	4.31e-5	0.99%
NOR2_X2	6	2.74e-5	2.76e-5	0.72%
NOR2_X4	8	2.22e-5	2.23e-5	0.28%
AOI21_X2	8	3.81e-5	3.81e-5	0.09%
AOI21_X4	11	3.00e-5	2.96e-5	1.23%
INV_X4	7	9.84e-5	9.88e-5	0.46%
INV_X8	13	1.02e-4	1.02e-4	0.64%
INV_X16	25	1.29e-4	1.28e-4	0.63%
BUF_X4	7	9.79e-5	9.85e-5	0.57%
BUF_X8	13	1.12e-4	1.11e-4	0.36%
BUF_X16	25	1.24e-4	1.25e-4	0.08%
AVG	11.8	-	-	**0.53%**

Source: (POSSER et al., 2014).

5 EXPERIMENTAL SETUP

We now present the experimental setup used in this work for analyzing and improving circuit lifetime under cell-internal EM. Since we do not have yet access to a library at a recent technology node, where EM effects are more significant (JAIN; JAIN, 2012), our evaluation is based on scaling layouts from the NANGATE 45nm cell library down to 22nm. While this may not strictly obey all design rules at a 22nm node, the transistor and wire sizes are comparable to 22nm libraries, and so are the currents. The layout parasitic extraction was done using the 45nm FreePDK (FREEPDK45, 2011) models and the Calibre xRC (MENTOR, 2013) tool.

Initially the cells are characterized for the average and RMS currents in each cell under a reference pin position. The cells are characterized considering $f_{ref} = 1$GHz and for 7 different values each for the input slew and output load. As higher is the frequency larger will be the EM effects. The characterization thus generates a 7×7 look-up table with the RMS and average current values for the slew and load values, and these values are determined based on SPICE characterization of the scaled 22nm library based on publicly available 22nm SPICE ASU PTM models for the High Performance applications (PTM HP) (ZHAO; CAO, 2007).

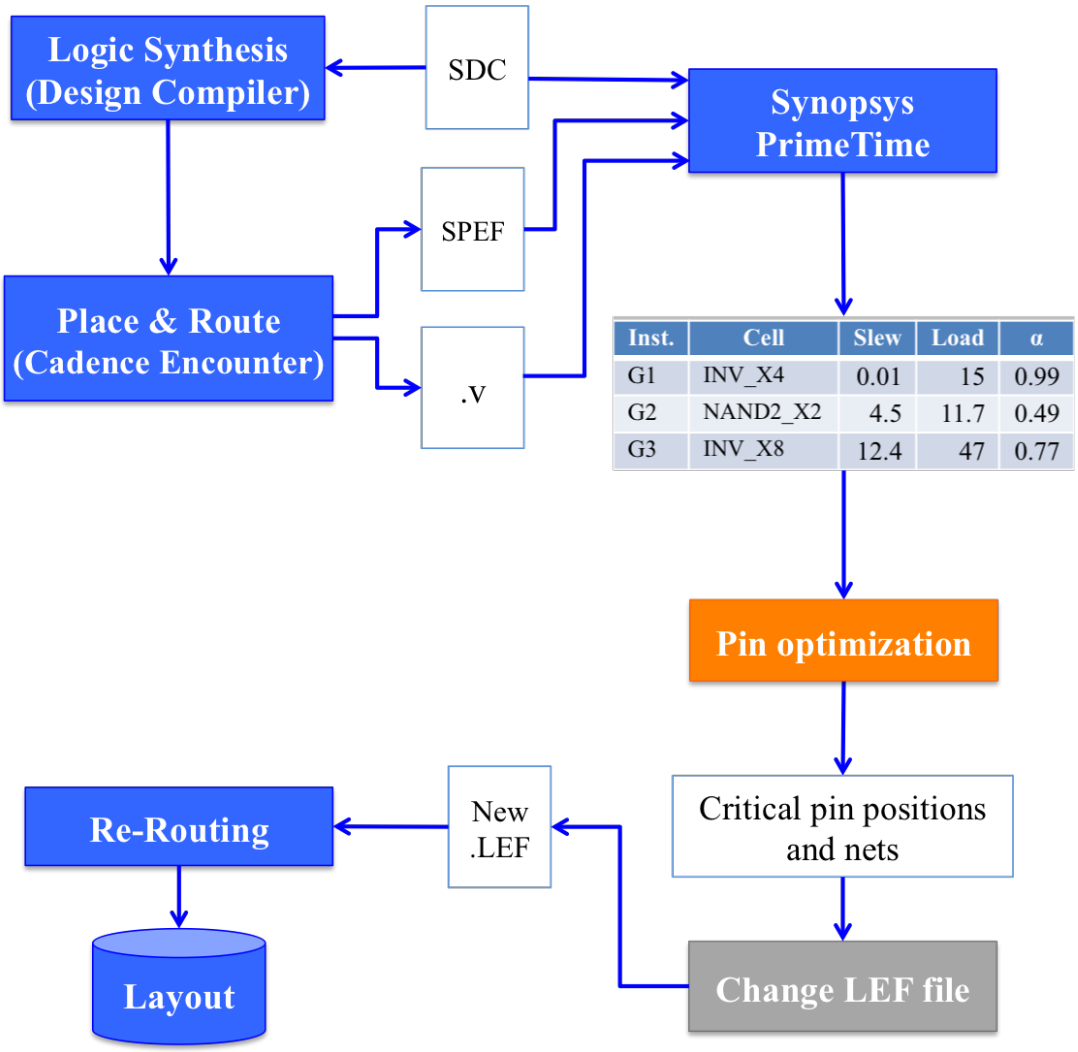
Hereafter, the analysis follows the flow presented in Figure 5.1. First, we synthesize ITC'99 and ISCAS'89 benchmarks using Design Compiler (SYNOPSYS, 2013a) with delay specs set to the best achievable frequency. The cells from the NANGATE library (NANGATE, 2011) used in this work are: NAND2_X2, NAND2_X4, NOR2_X2, NOR2_X4, AOI21_X2, AOI21_X4, INV_X4, INV_X8, INV_X16, BUF_X4, BUF_X8, BUF_X16, DFF_X2, DFFR_X2 and DFFS_X2. We focus on EM in the combinational cells.

Each circuit is placed and routed using Cadence Encounter (CADENCE, 2013). After the routing, the SPEF file with the extracted wire RCs and the Verilog netlist are saved. The timing, power, area and wirelength are reported. Synopys PrimeTime reads the SPEF, Verilog, and SDC files and reports the input slew, output load, and switching probability (α) for each instance of the circuit. The PrimeTime timing report provides the slew, load, and switching probability for all cell instances. These informations are used as input in our method to optimize the TTF (lifetime) of the circuits by the output pin position optimization, where its flow is shown in Figure 5.2.

To optimize the pin position considering all instances in the circuit, for each instance, based on the reported slew and load, we calculate I_{avg} and I_{rms} for each internal wire segment of the output pin (e.g., edges from e_1 to e_6 in Figure 4.1), interpolating from a 7×7 look-up table characterized for the reference pin position, and infer currents for each candidate position using the approach of this work presented in Chapter 4. The TTF is found using Eq. (3.1) at 378K, a typical EM specification. To calculate the TTF, beyond the I_{avg} and I_{rms} values, the wire information (width, length and resistance) are also important and are provided considering the dimensions of the cell layout and the parasitic extraction. The TTF for each wire segment (edge) is calculated considering these information.

The **worst TTF** of the circuit is given by the instance in the circuit that has the smallest

Figure 5.1: The implementation flow used in this work considering the standard-cell based synthesis flow.



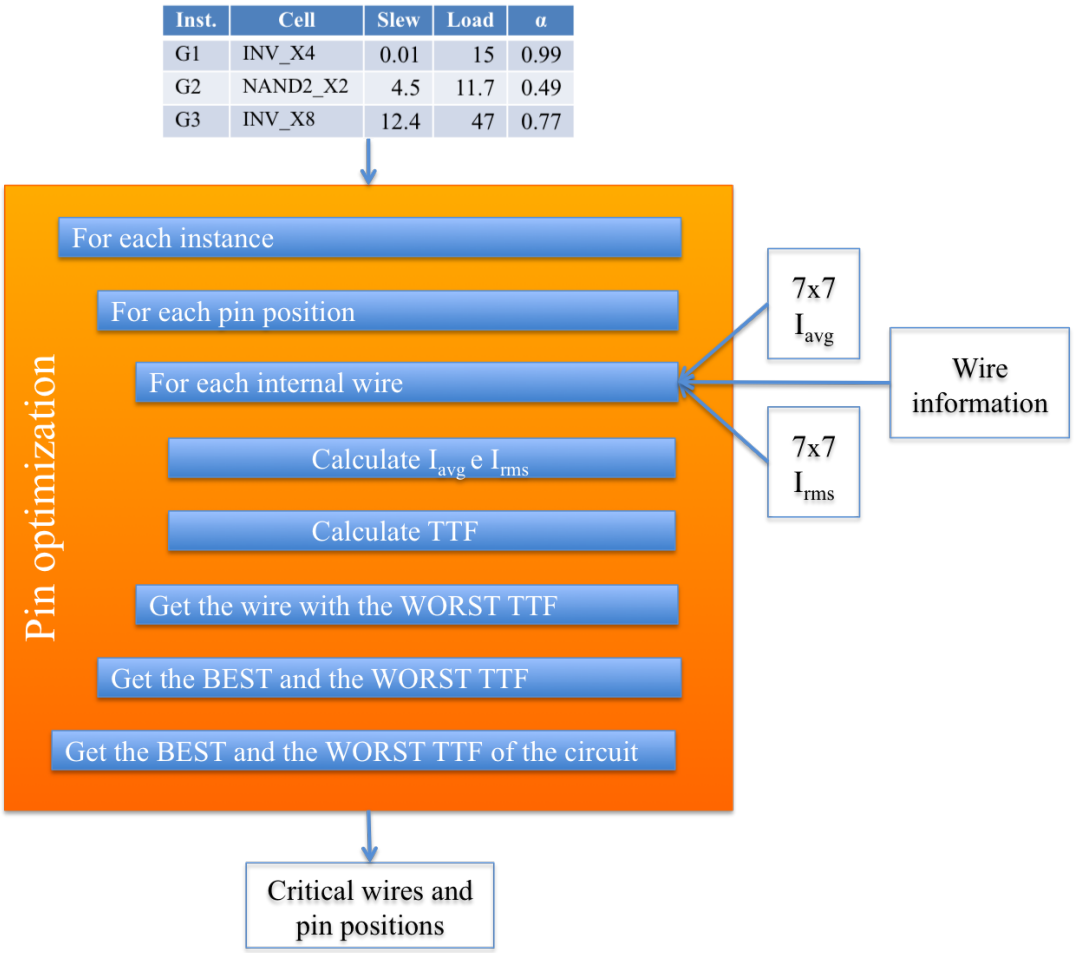
Source: (POSSER et al., 2015 - under review).

TTF. For this, for each instance is calculated the best and the worst TTF, i.e., the best and the worst pin position. The worst TTF for each pin position is the internal wire with the smallest TTF. Considering that the failure of a single wire caused by EM can result in the failure of the entire circuit (LIENIG, 2013). To compute the best TTF that the circuit can achieve under output pin selection, for each cell we determine the output pin position with the best TTF. The smallest best TTF over the entire circuit is the "weakest link" using the best possible pin positions, and is reported as the **best TTF** of the circuit.

Next, we turn to the problem of optimization, and the objective of our method is to optimize the lifetime of the circuit. We choose the lifetime specification to the best TTF in the circuit. We report the critical pin positions (pin candidates for which the lifetime is smaller than the best TTF) for each cell instance in the circuit, and invalidate these pins. We also enforce a design requirement that limits the maximum allowable Joule heating in a wire. A typical Joule heating specification is a 5°C temperature rise. We invalidate pin candidates in a cell that violate these requirements, Joule heating and lifetime. In this way we are trying to increase the number of pin positions for the router, helping to improve the routability, differently if we just selecting the **best TTF**. Our pin optimization tool also

can report the TTF for each pin position of each instance in the circuit. This information can be used with other tools to optimize the EM TTF of the circuits.

Figure 5.2: The pin optimization flow used in this work to optimize the lifetime of the circuit avoiding the critical pin positions.



Source: (POSSER et al., 2015 - under review).

For the output pin position optimization, we provide the above information to the router, describing pin positions to be avoided. We implement this by changing the pin information in the Library Exchange Format (LEF) file to outlaw the critical pin positions as we build a new TTF-optimized layout, as the last steps in Figure 5.1 presents. The layout of the cells are not changed, just the LEF file for each cell is changed. For the Nangate library used in this work, there is one version of the LEF file for each cell. The circuit is re-routed considering this new LEF file. Then, the timing, power, area and wirelength are reported to compare if the circuits have a significant change in the results with the pin optimization.

For the Vdd and Vss pins, the LEF file was not changed to avoid the critical pin positions and the circuit was not re-synthesized considering the restricted Vdd and Vss pin positions, because the impact on the global power grid is negligible due to these minor changes. Therefore, it is enough for our analysis to just perform local analyses.

6 RESULTS

Tables 6.1, 6.3 and 6.4 present the results of our lifetime evaluation scheme for the set of library cells considering the output, Vdd, and Vss pin placement, respectively, at 2GHz. The best and worst TTF values correspond to the largest and smallest lifetimes over all pin candidates. The TTF is calculated for two different switching activities (α) of 50% and 100% of the clock frequency: although few cells in a layout switch frequently, it is likely one of these cells that could be an EM bottleneck. The 100% switching case is a clear upper bound on the lifetime of the cell: typical cells, even worst-case cells, switch at a significantly lower rate, except on always-on networks such as core elements of the clock network. The tables show that the pin position is important: choosing a good pin position could better balance current flow and improve EM lifetime. It can be noted that the worst TTFs for the X16 cells are extremely small: this is due to the large number of pin choices for such cells, and due to the effects of large currents associated with specific pin positions, as well as divergence effects.

Table 6.1: TTF in years for each cell in the library for the output pin positions.

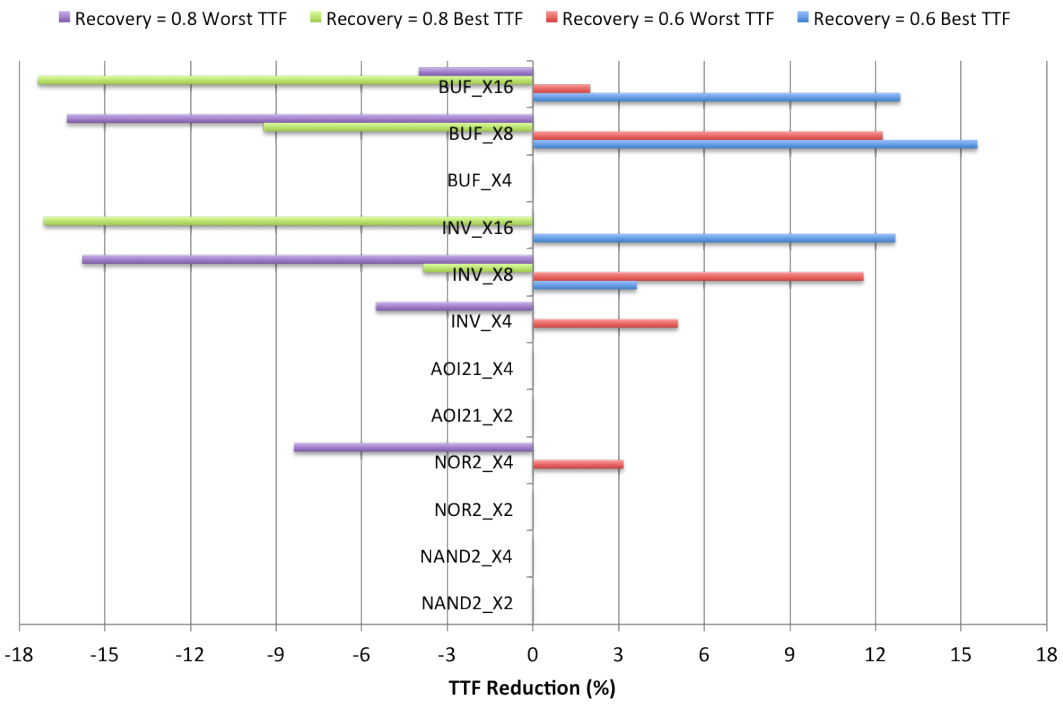
Cell	**Recovery = 0.7**				**Recovery = 0.6**		**Recovery = 0.8**	
	50% (α)		**100% (α)**		**100% (α)**		**100% (α)**	
	Best TTF	**Worst TTF**	**Best TTF**	**Worst TTF**	**Best TTF**	**Worst TTF**	**Best TTF**	**Worst TTF**
NAND2_X2	22.03	21.85	10.95	10.85	10.95	10.85	10.95	10.85
NAND2_X4	27.65	20.37	8.75	8.08	8.75	8.08	8.75	8.08
NOR2_X2	24.33	24.30	12.11	12.07	12.11	12.07	12.11	12.07
NOR2_X4	29.61	25.71	14.74	10.75	14.74	**10.41**	14.74	**11.65**
AOI21_X2	28.32	28.30	14.12	14.11	14.12	14.11	14.12	14.11
AOI21_X4	13.13	13.10	6.47	6.43	6.47	6.43	6.47	6.43
INV_X4	23.23	9.90	11.49	4.73	11.49	**4.49**	11.49	**4.99**
INV_X8	33.80	16.92	9.09	1.90	**8.76**	**1.68**	**9.44**	**2.20**
INV_X16	30.80	2.42	15.53	0.20	**13.56**	**0.19**	**18.19**	**0.20**
BUF_X4	25.85	12.93	12.64	6.35	12.64	6.35	12.64	6.35
BUF_X8	40.93	13.55	10.92	1.96	**9.22**	**1.72**	**11.95**	**2.28**
BUF_X16	35.91	3.17	17.65	0.50	**15.38**	**0.49**	**20.71**	**0.52**

Source: (POSSER et al., 2014).

Table 6.1 also shows the TTF results for a 100% (α) considering a recovery factor of 0.6 and 0.8. *All the other results presented in this work are calculated for a 0.7 recovery factor*, as already cited. The recovery factor is used when the current flows are in opposite directions, as Eq. 3.4 shows. The TTF values in bold are those ones that change when the recovery factor changes, i.e., the currents flowing through the critical edges are in the same direction and the average current is calculated as Eq. 3.5. Changing the recovery factor, from 0.7 to 0.6 or 0.8 the TTF changes from 2% to 17.34%. The difference is because as larger is the current to be recovered larger is the difference from the previous recovery to the new recovery value. Figure 6.1 presents how much (in %) the TTF reduces

when the recovery factor is changed to from 0.7 to 0.6 and how much the TTF increases (negative % values) for a recovery factor of 0.8.

Figure 6.1: TTF reduction when the recovery factor is changed from 0.7 to 0.6 and 0.8 for a switching activity of 100% considering the values presented in Table 6.1. Negative values implies in a TTF increase.



Source: from author (2015).

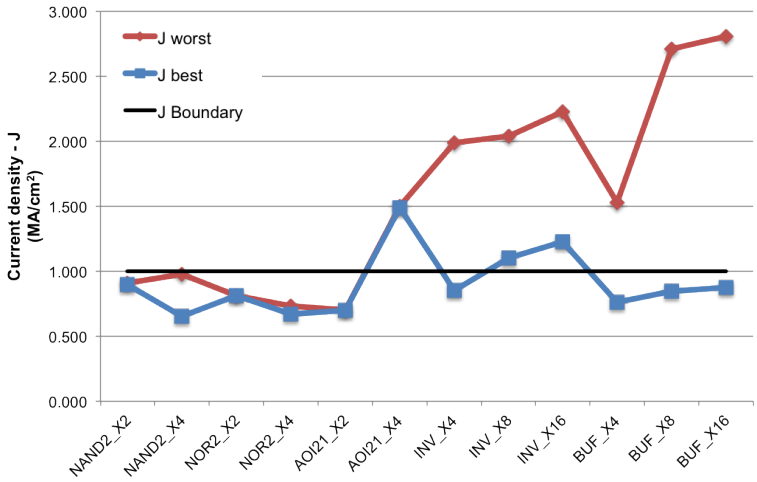
Table 6.2 shows the current density (J) values for the worst and best TTF presented in Table 6.1 for a 100% switching activity and a 0.7 recovery factor for each cell. Area (in μm^2) and the number of PMOS and NMOS transistors are also presented, where for the BUF cells the values between brackets are the number of transistors suppling the output. Figure 6.2 shows the current density (J) values presented in Table 6.2, where 1MA/cm^2 is considered the J boundary, because the EM effects are visible from this current density (ITRS, 2011). Remembering that the EM effects are not just influenced by J, they are also influenced by Joule heating that is depended on the RMS current. The J values higher than 1MA/cm^2 are for the INV, BUF and AOI21_X4 cells. For the cells with 2 inputs, J is smaller than the boundary limit and the TTF is not so critical, it is higher or close to 10 years. Just for the NAND2_X4 the worst TTF is 8.08 years.

Table 6.2: Current density (J) values for the worst and best TTF, area and number of PMOS and NMOS transistors of each cell.

Cell	**J for worst TTF (MA/cm^2)**	**J for best TTF (MA/cm^2)**	**Area (μm^2)**	**# PMOS transistors**	**# NMOS transistors**
NAND2_X2	0.907	0.898	0.318	4	4
NAND2_X4	0.976	0.652	0.572	8	8
NOR2_X2	0.814	0.814	0.318	4	4
NOR2_X4	0.735	0.671	0.572	8	8
AOI21_X2	0.702	0.701	0.445	6	6
AOI21_X4	1.500	1.490	0.826	12	12
INV_X4	1.990	0.853	0.318	4	4
INV_X8	2.040	1.100	0.572	8	8
INV_X16	2.230	1.230	1.080	16	16
BUF_X4	1.530	0.764	0.445	6 (4)	6 (4)
BUF_X8	2.710	0.846	0.826	12 (8)	12 (8)
BUF_X16	2.810	0.878	1.589	24 (16)	24 (16)

Source: from author (2015).

Figure 6.2: Current density (J) values for the worst and best TTF.



Source: from author (2015).

Placing the Vdd and Vss pins on the best position could improve the INV_X16 lifetime in about 31× and 69×, switching 100% of the time, as Tables 6.3 and 6.4 show, respectively. These low lifetimes correspond to very high switching rates: in other words, some pin positions would be impermissible on clock buffers, but may be permissible on nets with low switching activity. For the cell AOI21_X2 the TTF almost doesn't change when the Vdd pin position changes. However, changing the Vss pin position the lifetime can be improved on about 2×. The pin placement has a larger lifetime improvement for the Vss pin than for the Vdd pin. This is because for some cells (AOI21_X2, for example) the geometry of the Vdd and Vss wires are different, producing different pin position options and consequently different current distribution. While this result may include possible inaccuracies from our direct geometric scaling of the publicly-available 45nm cell layouts to 22nm, the impact of pin positions is real and can be extreme for large cells.

To counter this effect, a cell layout may use wider wires to control current densities, or more practically, outlaw a set of critical positions. For example, for each of the X16 cells, pin positions that see more balanced currents provide high lifetimes (as shown by the best TTF for these cells). More details about the INV_X16 cell are presented in Section 6.1.4.

Table 6.3: TTF in years for each cell in the library for different Vdd pin positions.

Cell	**# Candidates**	**50% switching**		**100% switching**	
		Best TTF	**Worst TTF**	**Best TTF**	**Worst TTF**
NAND2_X2	6	24.84	22.28	12.38	11.10
NAND2_X4	10	23.66	11.36	11.80	5.57
NOR2_X2	5	51.10	24.13	25.48	12.02
NOR2_X4	6	24.84	12.14	12.39	5.93
AOI21_X2	4	28.34	28.23	14.11	14.05
AOI21_X4	5	26.45	13.40	13.16	6.61
INV_X4	6	18.75	9.03	9.32	4.41
INV_X8	10	18.43	4.31	9.16	1.57
INV_X16	18	15.69	1.42	7.64	0.25
BUF_X4	8	22.45	7.35	11.12	3.52
BUF_X8	14	21.40	3.24	10.37	1.24
BUF_X16	26	11.03	1.24	5.31	0.25
AVG	**9.83**	-	-	-	-

Source: (POSSER et al., 2015 - under review).

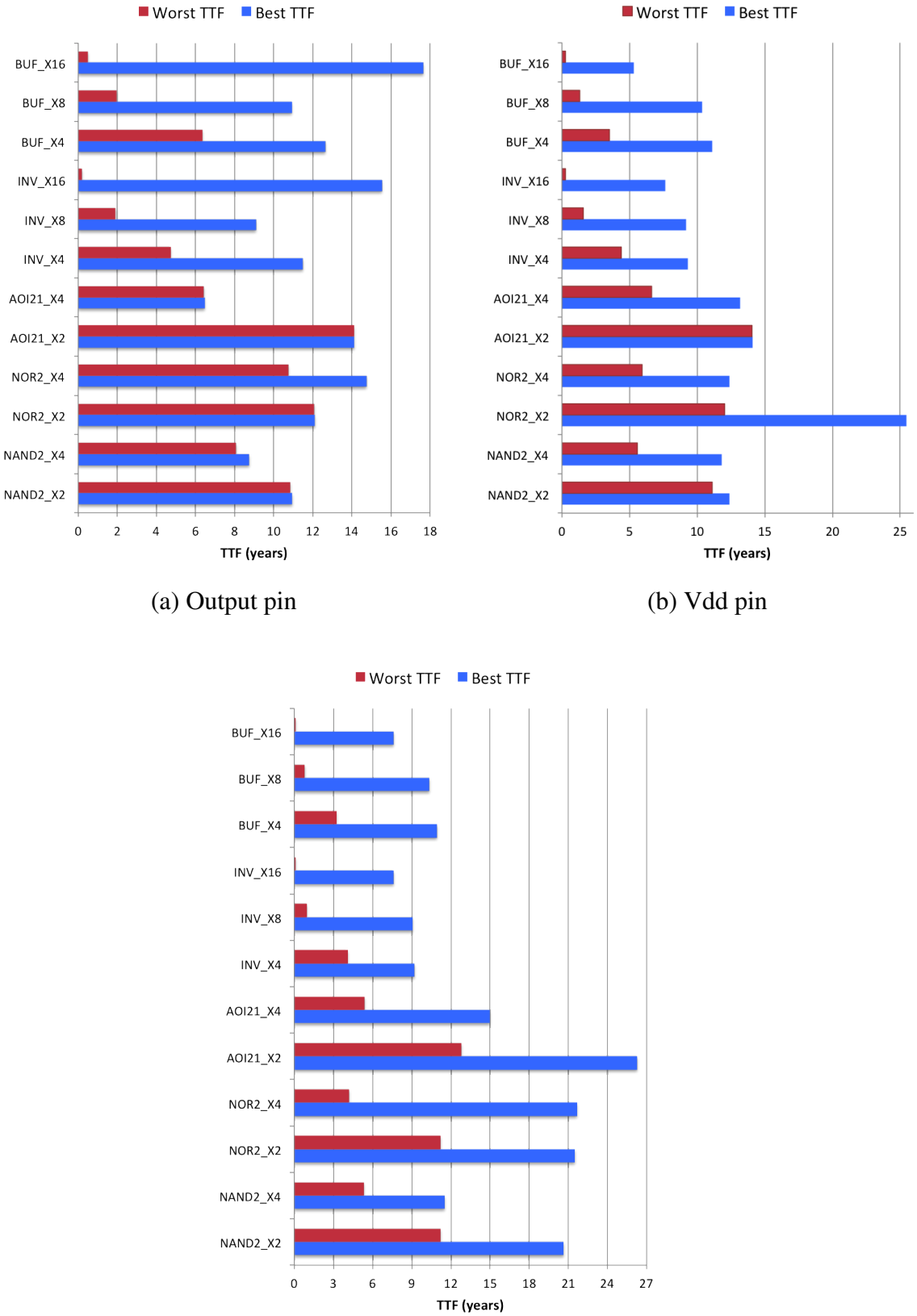
Table 6.4: TTF in years for each cell in the library for different Vss pin positions.

Cell	**# Candidates**	**50% switching**		**100% switching**	
		Best TTF	**Worst TTF**	**Best TTF**	**Worst TTF**
NAND2_X2	5	41.38	22.57	20.63	11.20
NAND2_X4	5	23.22	10.99	11.52	5.33
NOR2_X2	6	43.05	22.57	21.49	11.20
NOR2_X4	10	43.39	10.81	21.65	4.20
AOI21_X2	6	52.59	25.74	26.26	12.80
AOI21_X4	10	30.56	12.39	14.98	5.39
INV_X4	6	18.67	8.68	9.21	4.10
INV_X8	10	18.35	3.32	9.06	0.95
INV_X16	18	15.68	0.92	7.61	0.11
BUF_X4	8	22.28	7.04	10.93	3.23
BUF_X8	14	21.42	2.77	10.35	0.81
BUF_X16	26	15.68	0.92	7.61	0.11
AVG	**10.33**	-	-	-	-

Source: (POSSER et al., 2015 - under review).

Figure 6.3 shows a chart representation for the TTF in years for each cell considering the different (a) output, (b) Vdd and (c) Vss pin positions at 100% switching activity. The values are the same presented in Tables 6.1, 6.3 and 6.4.

Figure 6.3: TTF for each cell for different (a) output, (b) Vdd and (c) Vss pin positions for a 100% switching activity presented in Tables 6.1, 6.3 and 6.4.



(a) Output pin

(b) Vdd pin

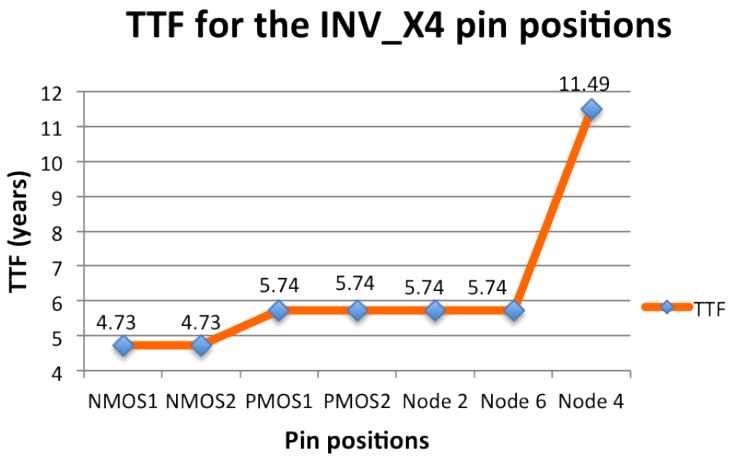
(c) Vss pin

Source: from author (2015).

The maximum load capacitance is different for each cell. The cells with a larger size can load a larger capacitance without increasing the delay. Considering the load capacitance used in the Nangate cell library, as we are scaling to a lower technology node (22nm), the max capacitance should usually reduce. This is because the sizes of the loads go down, so the gate capacitance goes down, and also the length of each wire also goes down (distance from driver to load, or to first buffer for a buffered interconnect). So this should be factored into the output load values. Then, we found for each cell the maximum output load that the cell can load without violate the condition $((delay + transition\_time/2) > target\_period)$ and the VDD signal is able to reach the VDD voltage (0.88V for 22nm).

Figure 6.4 shows the TTF in years for the different pin position options for an INV_X4 (Figure 1.7), considering a switching activity of 100% at 2GHz. It is possible to see a lifetime difference between the pin positions. When the pin is at node 4, the TTF is 2× larger than when the pin is at PMOS or at node 2 or node 6 and 2.78× larger than when the pin is at NMOS. For this cell, the best TTF, i.e., the TTF achievable changing the pin position is 7.38 years and the worst TTF is 2.65 years at 2GHz.

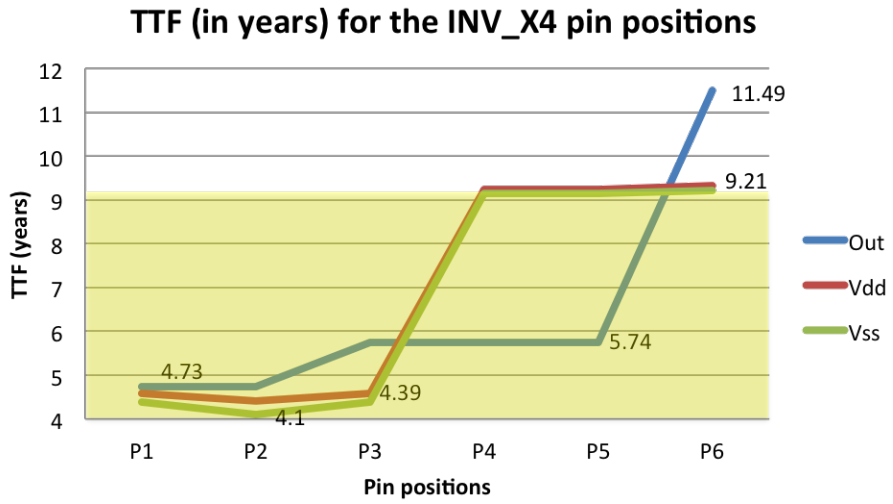
Figure 6.4: TTF in years for various pin positions in INV_X4, considering a switching activity of 100% and a frequency of 2GHz.



Source: (POSSER et al., 2014).

Figure 6.5 shows the TTF in years for the different output, Vdd, and Vss pin position options for an INV_X4, considering a switching activity of 100% at 2GHz. The values for the output pin are the same shown in Figure 6.4. The different pin positions are named from P1 to P6, where the TTF changes for each different pin position. Relating to Figure 1.7, P1 is when the output pin is at node 3, Vdd is at node 2 and Vss is at node 1. P2 is when the output pin is at node 7, Vdd is at node 4 and Vss is at node 3. These are the critical pin positions for this cell, where they have the smallest TTF. Avoiding the critical pin positions, the largest TTF that the INV_X4 can achieve is 9.21 years, that is limited by the Vss pin. So, to achieve the maximum TTF, all pin positions with a TTF smaller than 9.21 years are avoided, as the colorful area in the chart shows. The TTF for the INV_X4 can be improved in 2.25× avoiding the critical output, Vdd, and Vss pin positions. For this cell, the best TTF given by the output pin is 11.49 years and this value cannot be achieved because it is limited by the best TTF of the Vss pin, that is 9.21 years. Moreover, the worst TTF of this cell is 4.1 years and it is also given by the Vss pin.

Figure 6.5: TTF for some INV_X4 output, Vdd and Vss pin positions at 100% switching.



Source: (POSSER et al., 2015 - under review).

Table 6.5 presents the results for a set of ITC'99 and ISCAS'89 benchmarks circuits mapped to our set of characterized cells and placed-and-routed. For each benchmark the number of combinational cells, the clock period, total power consumption (leakage and switching power), area of core and total wirelength (WL) are presented, as reported by Encounter.

Table 6.5: Timing, power, area and wirelength reports from the Encounter tool after place and route the set of benchmark circuits.

Circuit	**# of comb. cells**	**Period** (ns)	**Power** (mW)	**Area of core** (μm^2)	**Total wire length** (μm)
b05	859	0.544	0.551	504	2682.50
b07	461	0.306	0.352	317	1426.87
b11	821	0.384	0.460	471	2439.83
b12	1217	0.282	0.810	824	4236.15
b13	340	0.208	0.467	272	1272.99
s5378	1219	0.299	0.679	890	6418.27
s9234	1044	0.373	0.584	849	4873.30
s13207	1401	0.720	1.063	1733	7146.48
s38417	10068	0.493	8.836	7959	46419.93

Source: (POSSER et al., 2014), (POSSER et al., 2015 - under review).

The best and worst TTF values are computed as described in Chapter 5 and are presented in Table 6.6. These results correspond to a post place-and-route layout with no EM awareness, and the gap between the best and worst TTF values indicates how much the lifetime can be improved. The worst TTF is considering that the router chooses the worst pin position, where the TTF of the cell will be the smallest value. The best TTF is achieved when the critical pin positions are avoided. The number of critical nets corresponds to the nets that violate the Joule heating constraint (5K), and the number of critical cells corresponds to the cells that have pin positions that corresponds to lifetimes

below the best TTF. Interestingly, these numbers are both small, implying that large improvements to the lifetime can be obtained through a few small changes to the layout. Note that the best TTF values are in the range required for many modern applications (e.g., mobile devices) with short TTF specs of $3-4$ years. Generally the intended TTF for many electronic interconnects in integrated circuits is approximately 10 years (ITRS, 2011; LIENIG, 2013).

Table 6.6: Cell-internal EM analysis for a set of benchmark circuits computing the best and worst TTF values as described in Chapter 5 for the output pin position.

Circuit	**Worst TTF (years)**	**Best TTF (years)**	**TTF Improv.**	**# of critical nets**	**# of critical instances**	$\frac{critical\_instances}{total\_instances}$
b05	4.07	6.53	37.59%	-	4	0.47%
b07	3.81	5.25	27.43%	-	3	0.65%
b11	2.75	5.82	52.80%	1	5	0.61%
b12	3.13	3.14	0.15%	3	1	0.08%
b13	3.89	6.05	35.70%	1	7	2.06%
s5378	2.74	3.59	23.67%	2	1	0.08%
s9234	2.73	3.48	21.39%	-	1	0.10%
s13207	4.94	13.18	62.50%	-	7	0.50%
s38417	3.43	5.77	40.51%	2	6	0.06%

Source: (POSSER et al., 2014), (POSSER et al., 2015 - under review).

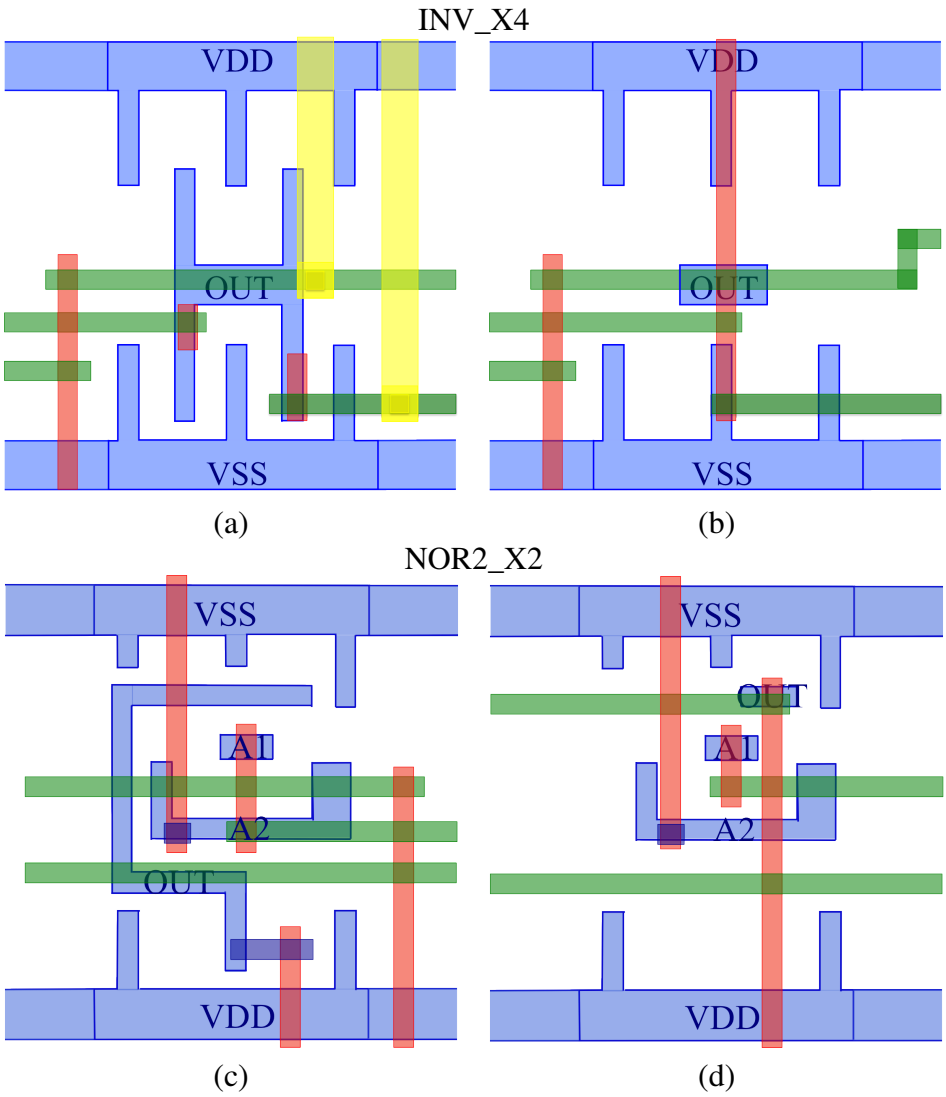
Table 6.6 shows that the lifetime of a circuit can be improved by up to 62.50% by altering the pin position of a few cells. The benchmark where the TTF improvement is small is b12: the critical cell for this circuit is a NOR2_X2 where the worst TTF is 3.13 and the best TTF is 3.14, i.e., changing the pin position the TTF does not change the lifetime significantly. The largest TTF improvement is for s13207, where the critical cell is an INV_X4 where the worst TTF for this instance in the circuit , given by the worst pin position, is 4.94 years and the best TTF is 13.18 years.

We now redo the routing step to guarantee that the best TTF in Table 6.6 can be met by outlawing all pin positions whose TTF is worse than the best TTF in Table 6.6, or that result in a cell-internal Joule heating violation. Since the best TTF was computed by choosing the best pin position for each cell, and then finding the weakest link by determining the shortest TTF among these cells, a few cells may be forced to use a single pin, but most cells will have the choice of a number of pin positions, and the circuit lifetime will be significantly enhanced. (Note that by the definition of best TTF, each cell is guaranteed to have at least one allowable pin).

After these new constraints are imposed on the pin positions, the router makes incremental changes to some interconnect routes. Figure 6.6 shows how the router changed the interconnections around an instance of the INV_X4 and NOR2_X2, respectively, when the critical pin positions are avoided. Figure 6.6(a) shows the connections to INV_X4 considering the original LEF file, where the H-shape is the output of the cell and the output pin can be placed anywhere in this H-shape. The same happens for the NOR2_X2 cell in Figure 6.6(c), where the output is the largest metal 1 wire (blue) and it is connected to ZN. While, Figures 6.6(b) and (d) show the connections when the critical pin positions are avoided and the output pin can be placed just in the center of the INV_X4 (blue connection in the center) and for the NOR2_X2 is the most superior on right metal

1. Thereby, the routes are changed to consider the constrained cell.

Figure 6.6: Routing through an INV_X4 (a) and (b) and a NOR2_X2 cells considering (a) and (c) the original LEF file and (b) and (d) avoiding the critical pin positions.



Source: from author (2015).

Table 6.7 shows the results after physical synthesis considering the best pin positions, i.e., for each cell, we disallow EM-unsafe pin positions. Thus, we see that the circuit lifetime is improved up to 62.50% while keeping the delay, area and power of the circuit unchanged, and with marginal changes ($\leq 0.15\%$) to the total wirelength (in fact, for one circuit, b12, the wirelength and the clock period are even slightly improved). As there are only a few instances with critical pin positions and critical wire segments, the TTF can be increased without major changes in the circuit. A set of tests increasing the number of instances that are changed to avoid the EM-unsafe pin positions is presented in Appendix A.

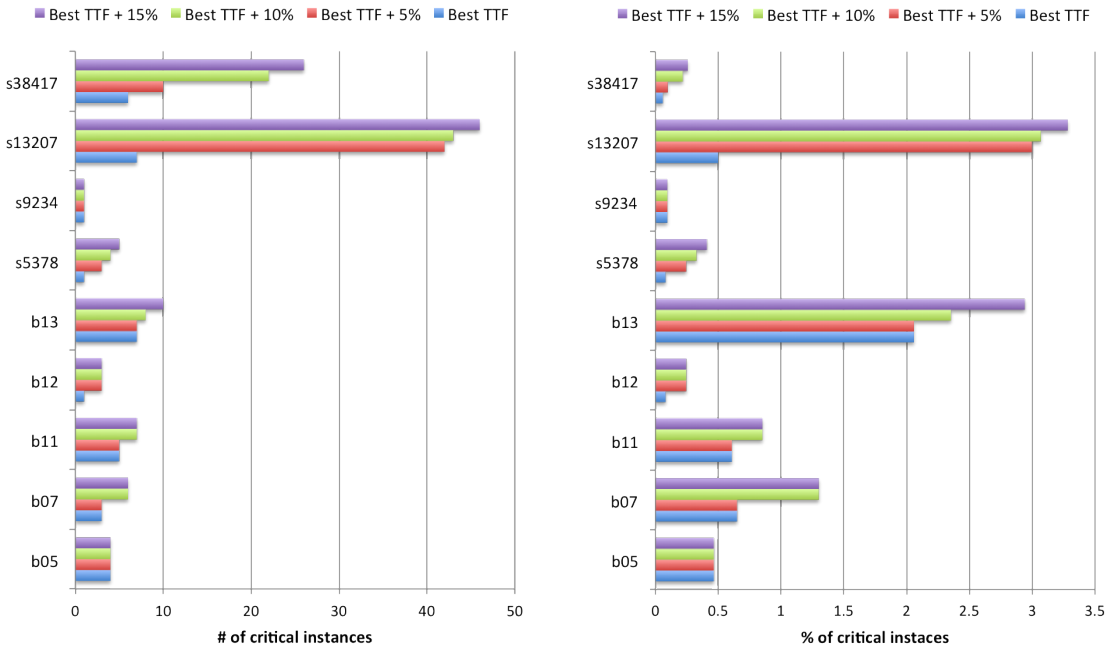
Table 6.7: Performance impact of EM-aware physical synthesis using pin optimization. The reports are from the Encounter tool after the circuit be replaced considering the optimized pin positions.

Circuit	Period (ns)	Δ Period (%)	Power (mW)	Area (μm^2)	WL (μm)	Δ WL (%)
b05	0.544	-	0.551	504	2682.6	0.00
b07	0.306	-	0.353	317	1428.5	0.12
b11	0.384	-	0.460	471	2443.5	0.15
b12	0.280	-0.89	0.808	824	4112.8	-2.91
b13	0.208	-	0.467	272	1273.5	0.04
s5378	0.299	-	0.679	890	6422.2	0.06
s9234	0.373	-	0.584	849	4873.4	0.00
s13207	0.720	-	1.063	1733	7146.6	0.02
s38417	0.493	-	8.836	7959	46420.2	0.00

Source: (POSSER et al., 2014), (POSSER et al., 2015 - under review).

For these tests we are considering the best TTF that the circuit can achieve by avoiding the output critical pin positions. Considering a TTF 5%, 10% and 15% larger than the best TTF, the number of critical instances increase a little bit for most circuits. A larger increase is observed for s13207 and s38417 circuits, as Figure 6.7(a) shows. Nevertheless, the percentage of the number of critical instances compared with the total instance number is small, less than 3.3%, as Figure 6.7 (b) shows.

Figure 6.7: (a) Number (#) and (b) percentage (%) of critical instances compared with the circuit total instances increasing the best TTF by 5%, 10% and 15%.

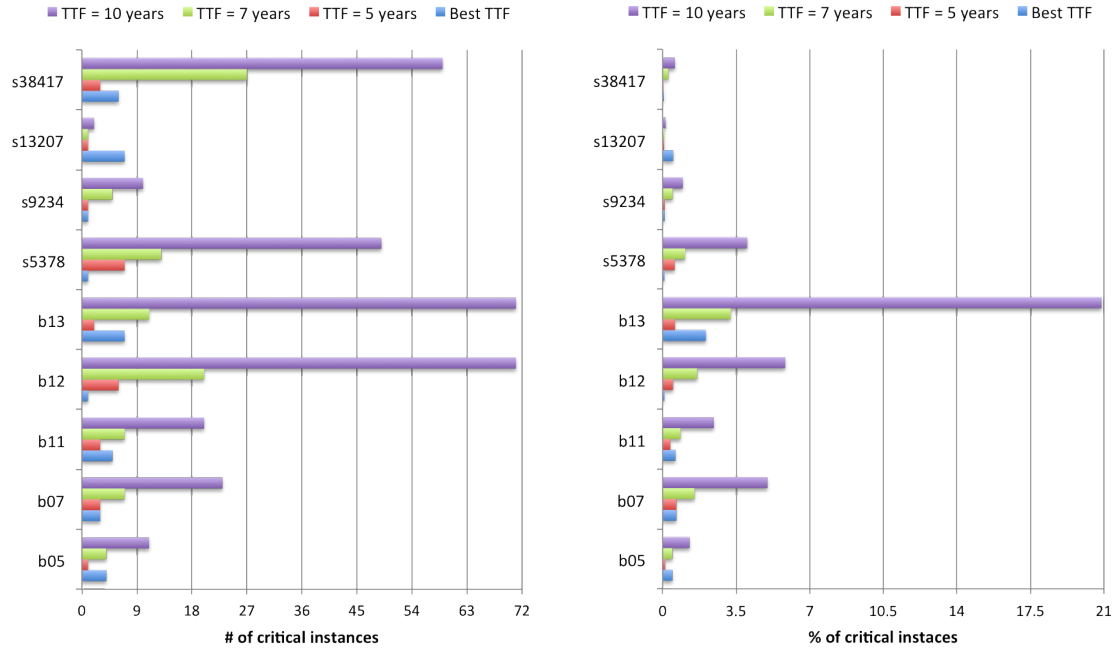


(a) (b)

Source: from author (2015).

Considering a specific TTF of 5, 7 and 10 years, Figure 6.8(a) shows the number of critical instances for each benchmark circuit. This number increases significantly for most circuits targeting 10 years as TTF. Comparing the number of critical instances with the total number of instances, more than 3.5% of the instances are critical for 4 circuits and for circuit b13, about 21% of the instances are critical to achieve a lifetime of 10 years, as Figure 6.8(b) presents. For a lifetime of 7 years, less than 3.5% of the instances are critical for all circuits tested in this work.

Figure 6.8: (a) Number (#) and (b) percentage (%) of critical instances compared with the circuit total instances for a TTF of 5, 7 and 10 years.



(a) (b)

Source: from author (2015).

Tables 6.8 and 6.9 present the lifetime optimization results considering the Vdd and Vss pin placement, respectively. The results are obtained in the same way as those considering the output pin placement and for the same benchmark circuit set. The worst and best TTF are shown for each circuit and its TTF improvement. Furthermore, the number of critical nets and critical cells that have to be avoided to achieve the best TTF are also shown. For the Vdd pin, avoiding the critical pin positions the TTF of the circuits can be improved from 38.53% to 78.54%, as Table 6.8 shows. For most circuits the number of critical cells is very small, about 10. For the circuits s13207 and s38417 the number of critical cells is 48 and 39, respectively, representing about 3.4% of the total number of cells.

The results for the Vss pin placement are shown in Table 6.9, where a higher TTF improvement is possible by choosing the best Vss pin position than choosing the best output or Vdd pin positions. The TTF can be improved from 61.01% to 89.89% avoiding the critical Vss pin positions. The number of critical nets and cells are also larger than for output and Vdd pins. The largest number is for b13 circuit, where there are 204 critical cells and this is 60% of the total number of the cells in the circuit. For the other circuits, the number of critical cells is not larger than 3.8% of the total number of cells of the

circuit.

Table 6.8: Vdd pin analysis for a set of benchmark circuits.

Circuit	Worst TTF (years)	Best TTF (years)	TTF Improv.	# of critical nets	# of critical instances	$\frac{critical\_instances}{total\_instances}$
b05	4.26	7.87	45.87%	-	7	0.81%
b07	1.15	5.36	78.54%	9	7	1.52%
b11	2.94	7.18	59.05%	-	10	1.22%
b12	2.60	4.23	38.53%	-	8	0.66%
b13	2.08	5.06	58.89%	-	9	2.65%
s5378	2.40	5.27	54.46%	-	11	0.90%
s9234	2.38	6.04	60.60%	-	7	0.67%
s13207	5.20	11.85	56.12%	-	48	3.43%
s38417	3.73	6.30	40.79%	-	39	0.39%

Source: (POSSER et al., 2015 - under review).

Table 6.9: Vss pin analysis for a set of benchmark circuits.

Circuit	Worst TTF (years)	Best TTF (years)	TTF Improv.	# of critical nets	# of critical cells	$\frac{critical\_instances}{total\_instances}$
b05	3.56	9.37	62.01%	1	14	1.63%
b07	1.00	7.77	87.13%	9	29	6.29%
b11	2.17	6.64	67.32%	15	10	1.22%
b12	1.32	7.34	82.02%	27	47	3.86%
b13	1.04	10.29	89.89%	12	204	60.00%
s5378	1.22	5.61	78.25%	15	12	0.98%
s9234	2.23	5.73	61.08%	8	8	0.77%
s13207	4.41	11.31	61.01%	2	12	0.86%
s38417	2.51	8.29	69.72%	22	68	0.68%

Source: (POSSER et al., 2015 - under review).

Tables 6.6, 6.8 and 6.9 show the TTF improvement when the output, Vdd or Vss pin positions, respectively, are optimized separately. In this way, the results when the benchmark circuits are optimized to avoid the critical pin positions simultaneously are shown in Table 6.10. The best TTF of the circuit is the smallest best TTF among the output, Vdd, and Vss pin optimization values. Consequently, the worst TTF is the smallest TTF among the worst TTF of the pin positions. The number of critical cells is reduced compared to the Vss pin optimization because the TTF limit (best TTF) is smaller, reducing the number of critical pin positions and consequently the number of cells. By optimizing the pin positions, the lifetime of the circuits could be improved up to 80.95%. That is the case of the b07 circuit, where the lifetime can be improved from 1 year to 5.25 years, avoiding the critical pin positions of just 7 cells.

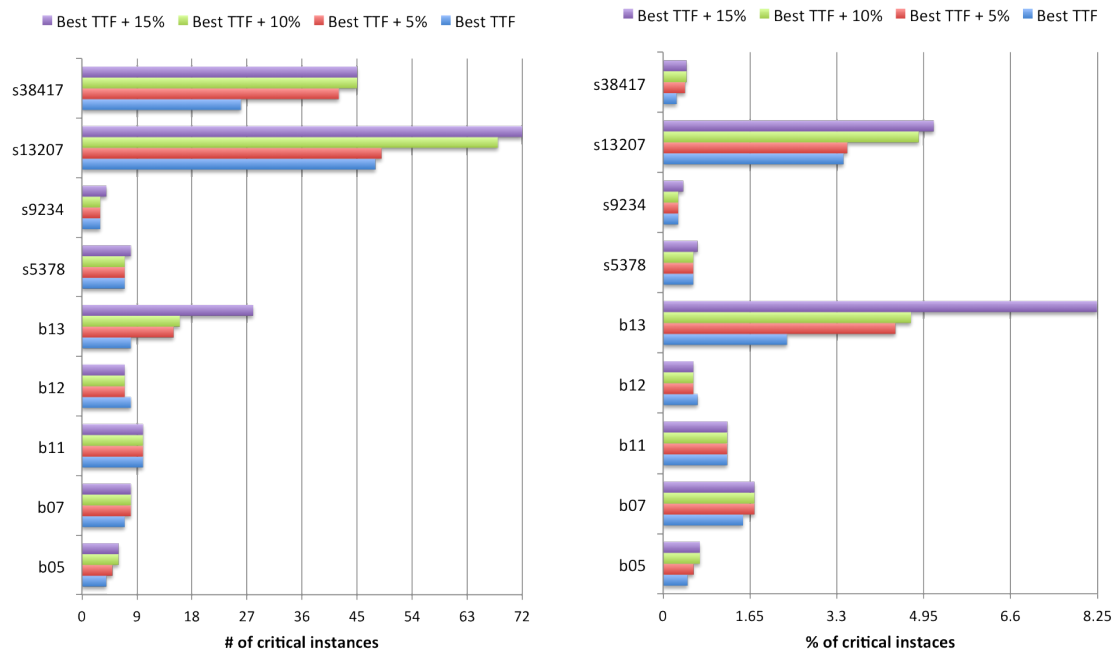
Table 6.10: TTF results optimizing the output, Vdd, and Vss pin positions for a set of benchmark circuits.

Circuit	Worst TTF (years)	Best TTF (years)	TTF Improv.	# of critical nets	# of critical cells	$\frac{critical\_instances}{total\_instances}$
b05	3.56	6.53	45.48%	1	4	0.47%
b07	1.00	5.25	80.95%	18	7	1.52%
b11	2.17	5.82	62.71%	16	10	1.22%
b12	1.32	3.14	57.96%	30	8	0.66%
b13	1.04	5.06	79.45%	13	8	2.35%
s5378	1.22	3.59	66.02%	17	7	0.57%
s9234	2.23	3.48	35.92%	8	3	0.29%
s13207	4.41	11.31	61.01%	2	48	3.43%
s38417	2.51	5.77	56.60%	24	26	0.26%

Source: (POSSER et al., 2014), (POSSER et al., 2015 - under review), (POSSER et al., 2015a).

For a TTF 5%, 10% and 15% larger than the best TTF achieved when the output, Vdd and Vss pins are optimized simultaneously, the number of critical instances increase more significantly for the s38417, s13207 and b13 circuits, as Figure 6.9(a) shows. Comparing the number of critical instances with the total instance number, just 2 circuits have more than 1.75% of critical instances, s13207 and b13. The circuit with the largest percentage of critical cells is b13, with about 8.25%, as Figure 6.9 (b) shows.

Figure 6.9: (a) Number (#) and (b) percentage (%) of critical instances compared with the circuit total instances optimizing the output, Vdd and Vss pin positions to achieve an increased best TTF by 5%, 10% and 15%.

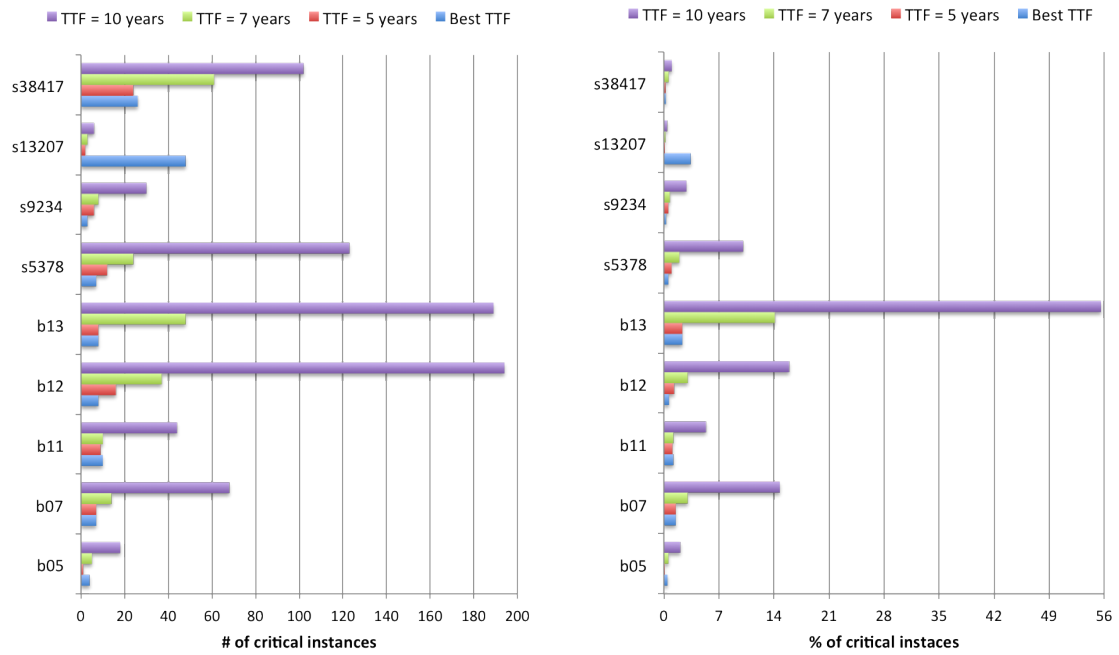


(a) (b)

Source: from author (2015).

Considering a specific TTF of 5, 7 and 10 years, Figure 6.10(a) shows the number of critical instances for each benchmark circuit. This number increases significantly for most circuits targeting a lifetime of 10 years. For a lifetime smaller than 10 years, all circuits have less than 60 critical instances. Looking the percentage of critical instances compared with the total number of instances, the circuit b13 has a considerable % of critical instances when the lifetime is larger than 7 years, achieving about 55% of the instances for a TTF of 10 years, as Figure 6.10(b) presents. For other 3 circuits, s5378, b12 and b07, more than 6% of the instances are critical for a lifetime of 10 years.

Figure 6.10: (a) Number (#) and (b) percentage (%) of critical instances compared with the circuit total instances optimizing the output, Vdd and Vss pin positions for a TTF of 5, 7 and 10 years.



(a) (b)

Source: from author (2015).

Runtime: As previously cited, the circuit analysis is executed by Encounter tool and the runtime for each benchmark is less than 40s. The critical pin positions for each circuit are reported in under 1s.

6.1 The Electromigration Effects for Different Logic Gates

Taking into account the cell-internal signal EM analysis for the output signal wire presented in this work, where the current density varies with layout geometry and is a dominant factor in determining the electromigration, this section presents:

1. an analysis of the EM effects on the cell-internal signal wires observing how the current flows through the output wire segments of different logic gates and different output wire geometry. Some examples of the cells are presented to explain why some cells have a larger TTF improvement when the output pin position is changed;

2. some suggestions to optimize the cell layouts to make the cells more robust from the EM perspective.

The idea is to use these robust cells replacing the critical cells that are affected by EM in the circuits. The objective is to increase the circuit TTF beyond the TTF achieved just by the pin position optimization. The critical cells are that ones with the highest switching activity. As shown in Table 6.6, the number of critical cells to be replaced is small, for a 10,000 gates design, is just 6. Thus, the increasing in area or the lost in performance doing the critical cells more robust to EM practically does not affect the overall results.

This study is motivated by the results presented in Table 6.1 showing that the TTF of the cells can be maximized optimizing the output pin placement. We can see that the TTF for some cells almost does not change when the pin position changes, as for the NAND2_X2, NAND2_X4, NOR2_X2, AOI21_X2 and AOI21_X4. On the other hand, the TTF for the other cells can be improved up to 76× (INV_X16) choosing the best pin position. Thus, in the next sections, we are presenting the analysis for some of those logic gates shown in Table 6.1. The simulations are based on scaling the layouts in the NANGATE 45nm cell library down to 22nm. The currents through the edges of the cell output signal wire are calculated by SPICE simulation using the publicly available 22nm PTM model (PTM HP) (ZHAO; CAO, 2007). The input slew and output load used in the simulations are tested to allow that the circuit operates correctly at 2GHz, where all transitions can be completed.

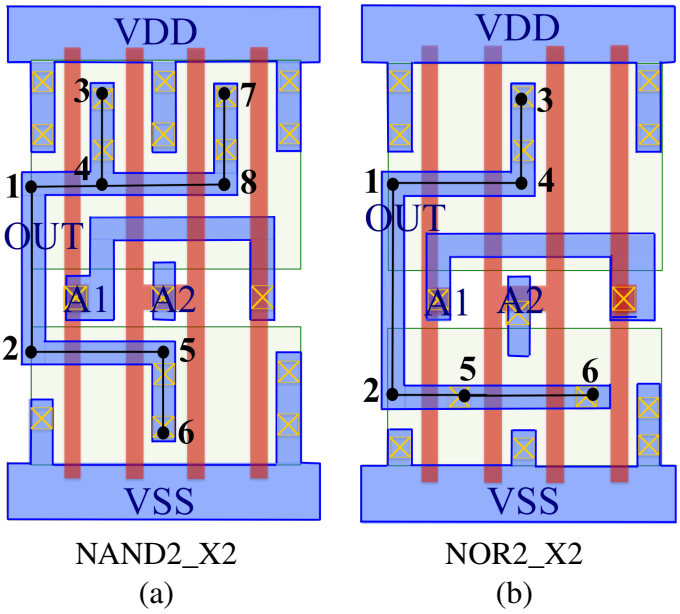
6.1.1 NAND2_X2 and NOR2_X2 gates

Figures 6.11 (a) and (b) show the layouts of the NAND2_X2 and NOR2_X2 gates. These gates have two inputs, A1 (first and fourth transistors) and A2 (second and third transistors). The output signal for the NAND2_X2 is represented by the 1-8 nodes and for the NOR2_X2 is represented by the 1-6 nodes. These two cells have a very small TTF difference among the different pin position options where the best and the worst TTF are very similar, as Table 6.1 shows.

Figure 6.12 shows the average current values through the edges e_1-e_7 of the NAND2-_X2 output signal wire considering an input slew of $78p$s and an output load of $4.5f$F. As the wire width and wire thickness is the same for all wire segments, the larger current density through the wire segments (edges) will be determined by the larger I_{avg} value among the edges.

The current injection points whose currents contribute to the current in the edges for the rise transition are the nodes 3 and 7 and for the fall transition is just the node 6. Nodes 3 and 7 inject a current of 11.1μA each one, so the maximum rise current flowing through the edges will be about the sum of these 2 currents, as Figures 6.12 (a) and (c) shows for the edge e_2 (21.4μA). For the fall transition, the node 6 injects 26.3μA. If the output pin is at node 1 (Figures 6.12 (a) and (b)), the critical edge is e_4 with an I_{avg} (Eq. 3.5) of 15.45μA from node 6. When the output pin is at node 6 (Figures 6.12 (c) and (d)), the edge e_4 is also the critical edge with an I_{avg} of 15.24μA, a little bit smaller current, where the TTF will be not so much different than the TTF when the output pin is at node 1. Placing the output pin at other nodes (2, 3, 4, 5, 7 and 8) the larger current will be very similar to the current presented when the output pin is at node 1. Thus, the best output pin position for the NAND2_X2 is at node 6, where the TTF is a little bit higher than the TTF when the output pin is at other position, as Table 6.1 also shows the small difference between the best and worst TTF for this cell.

Figure 6.11: The layout and output pin position options for a (a) NAND2_X2 and for a NOR2_X2 (b) gate.



Source: (POSSER et al., 2015).

For the NOR2_X2 cell, a similar effect happens but in a reverse way. For the NOR2_X2, there is just one node injecting the rise current (node 3 in Figure 6.11 (b)) and two nodes injecting the fall current (nodes 5 and 6 in Figure 6.11 (b)). The modifications applied for the PMOS transistors in a NAND2_X2 will be applied for the NMOS transistors in a NOR2_X2 gate.

6.1.1.1 TTF improvement by layout modifications

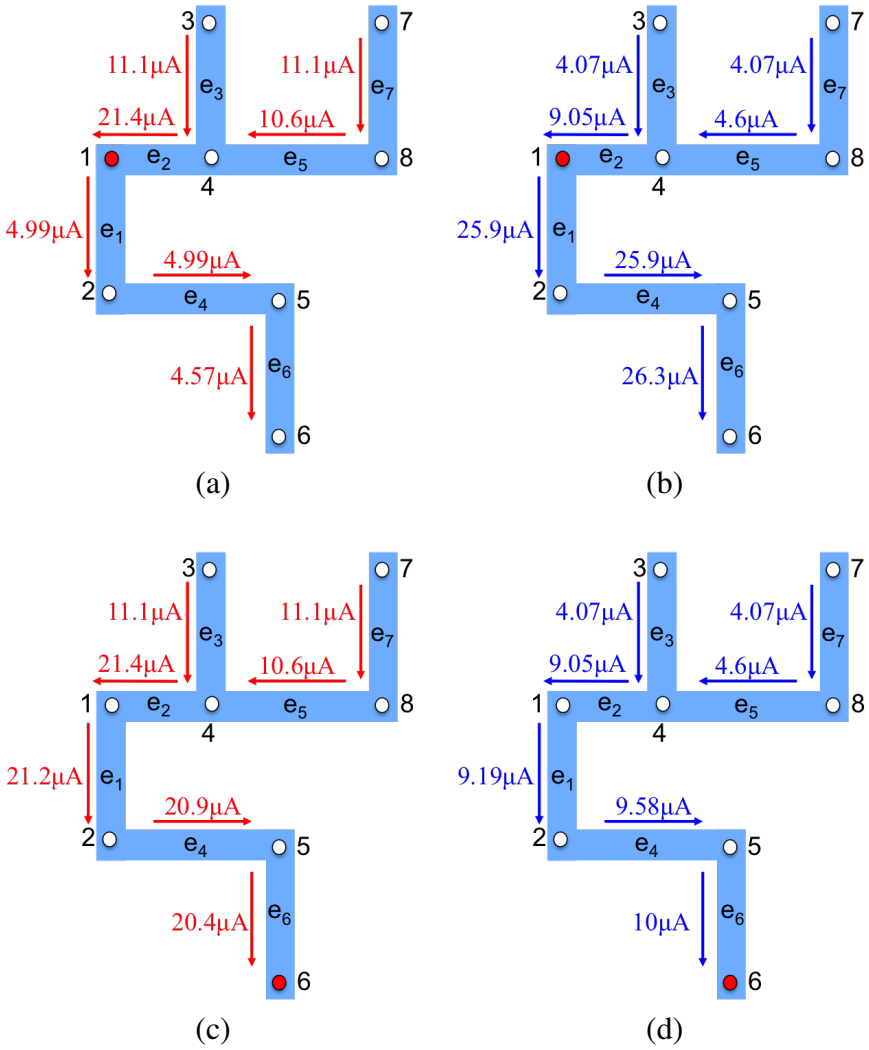
The output wire shape of the NAND2_X2 gate, as well as the NOR2_X2 gate, can be changed to improve the TTF. Figures 6.13(a), (b) and (c) present three options to improve the lifetime of the cells by changing the shape of the output wire of the NAND2_X2 gate. For the proposed solutions, the most symmetric shape for the output wire is considered. This strategy, in addition with a wider wire segment between nodes 3 and 4, can provide a more balanced current distribution through the output pin.

The first option is presenting a solution with a metal 1 finger for each PMOS transistor joining these currents at node 3. This change will avoid a large current through the edge e_2, as Figure 6.12 (a) shows, and the larger current will be between the nodes 3 and 4. Thus, the width of the edge between these nodes is increased from 34nm to 49nm. Moreover, the pin should be placed at this edge. This will provide a lifetime increase in 43%.

The second option, presented in Figure 6.13 (b) is using just metal 2 for the output wire facilitating the routing. The wire shapes in the second and third options are practically the same used in the first option, where the lifetime of the second option is improved by increasing the width of the edge between nodes 4 and 5 for the second option. and of the edges between nodes 3 and 6 for the third option. As metal 2 has a higher thickness than metal 1 and some different properties, its lifetime is larger than metal 1 (POSSER et al., 2014a).

The third option, Figure 6.13 (c), is using metal 2 for the vertical connections and

Figure 6.12: Average current values through the output wire segments of the NAND2_X2 gate when the output pin is at node 1, (a) and falling (b) and at node 6, (c) and (d). The red [blue] lines represent rise [fall] currents.



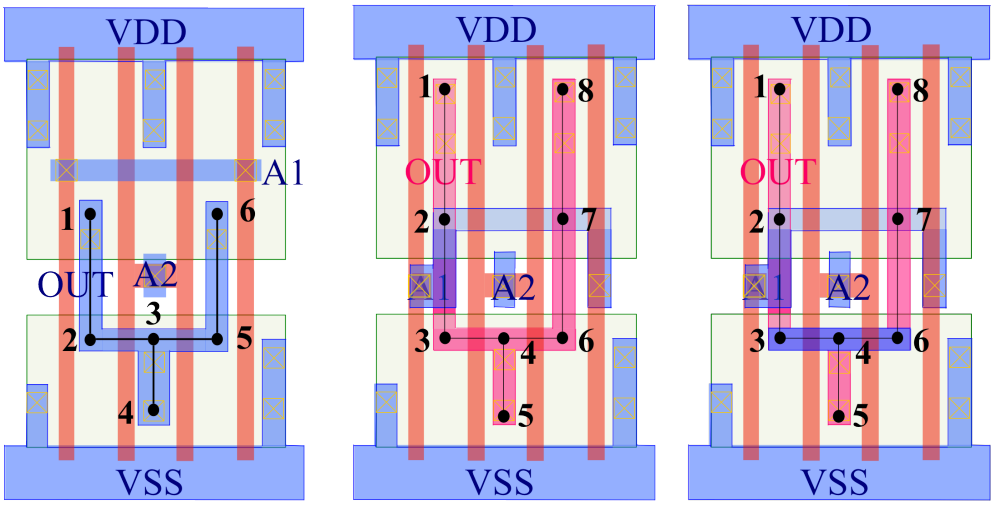
Source: (POSSER et al., 2015).

metal 1 for the horizontal connections of the output wire. The lifetime is improved by increasing the width of the edges between nodes 3 and 6. For the newest technologies, mainly below 32nm, wider metal in critical nets, and even in some cases the outputs of the cells will use metal 2 to reduce the EM effects(YERIC et al., 2013).

6.1.2 AOI21_X2

The layout of the AOI21_X2 gate (AND, OR, inverter cell) is shown in the Figure 6.14. It has three inputs, A (first and second transistors), B1 (fourth and fifth transistors) and B2 (third and sixth transistors). The output signal is represented by the 1-8 nodes in the center of the cell.

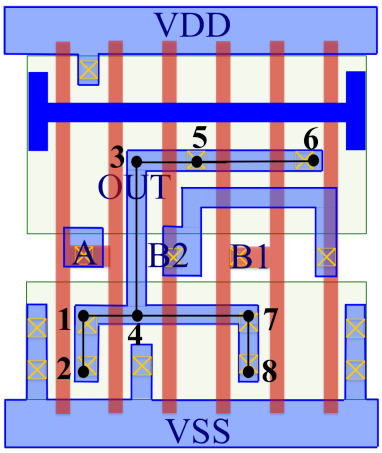
Figure 6.13: NAND2_X2 layout modification using just metal 1 (a), using just metal 2 (b) and using metal 1 and 2 (c) for the new output wire shape.



(a) (b) (c)

Source: (POSSER et al., 2015).

Figure 6.14: The layout and output pin position options for an AOI21_X2 gate.



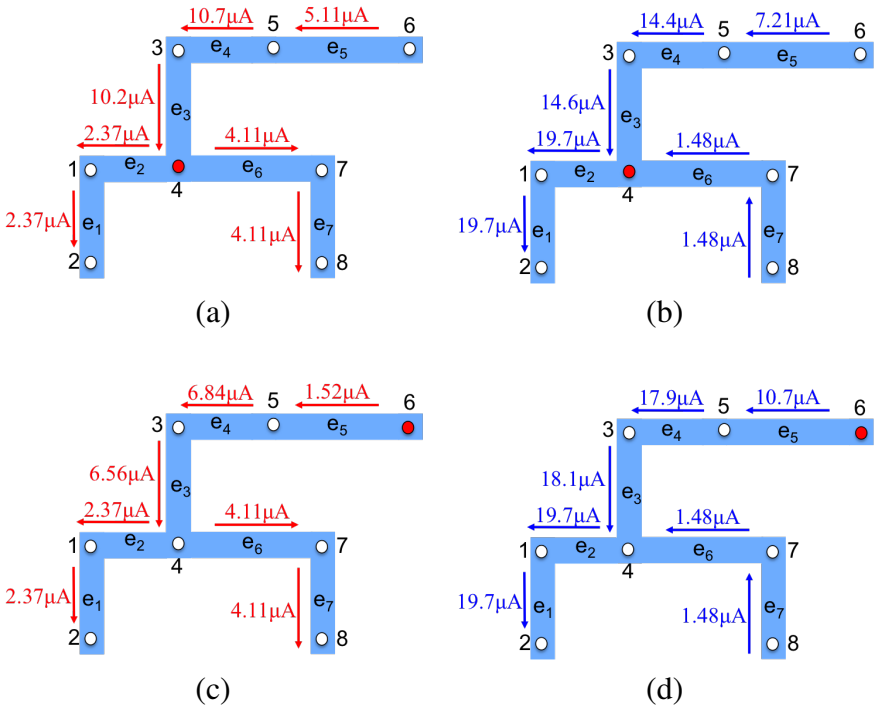
Source: (POSSER et al., 2015).

As Table 6.1 shows, AOI21_X2 gate has practically the same TTF when the output pin position changes (from 14.11 years to 14.12 years for a switching activity of 100%). To understand why this happen, Figure 6.15 is presenting the average current values through the edges e_1-e_7 of the output signal considering $78ps$ as input slew and $1fF$ as output load. The wire width is larger just for the edge e_1, for the other edges is the same width and the current density through these wire segments will be determined by the largest I_{avg}.

For the rise transition, the current injection points are the nodes 5 and 6 and for the fall transition are the nodes 2 and 8, as Figures 6.14 and 6.15 show. When the output pin is at node 4, Figure 6.15 (a) and (b), e_4 is the critical edge with an I_{avg} (Eq. 3.5) of $12.55\mu A$. When the output pin changes to node 6, Figure 6.15 (c) and (d), the rise and fall currents through e_4 change, but this edge remains the critical edge with an I_{avg} of $12.37\mu A$. This current value is a little bit smaller than the previous value, keeping the lifetime of the edge almost the same. If the output pin is placed at nodes 1, 2, 3, 7 and 8 the critical edge and the current values will be the same that when the output pin is at node 4. If the output

pin is placed at node 5, the critical edge and current value will be the same that when the output pin is at node 6.

Figure 6.15: Rise [red] and fall [blue] average current values through the output wire segments of the AOI21_X2 when the output is at node 4(a) and (b) and node 6 (c) and (d).



Source: (POSSER et al., 2015).

6.1.2.1 TTF improvement by layout modifications

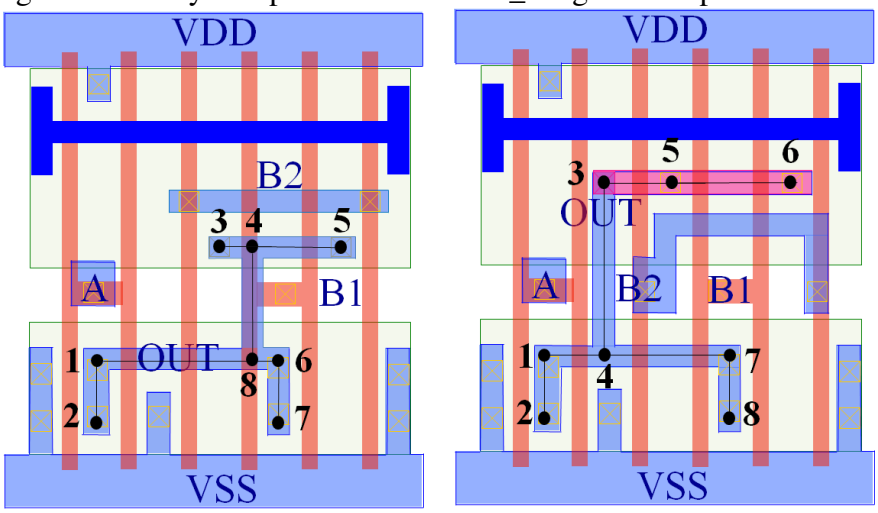
Two different layout options for the AOI21_X2 gate are presented in Figures 6.16 (a) and (b). The lifetime of the AOI21_X2 gate can be improved by changing the shape of the output wire.

In Figure 6.16 (a) the output pin shape is changed aiming a more symmetric current distribution using just metal 1 and avoiding the large current through the edge e_4 in Figure 6.15, and the output pin have to be placed at edge between nodes 4 and 8. Figure 6.16 (b) shows a layout improvement where the wire segments of the output from node 3 to node 5 and from node 5 to node 6 are using metal 2, reducing the current density because the metal 2 has a larger thickness, different proprieties and provides a possibility to use a wider wire. The output pin have to be placed at these edges in metal 2.

6.1.3 NOR2_X4

The layout of the NOR2_X4 gate is shown in the Figure 6.17. This is a NOR gate with size 4, i.e., the transistor widths are four times larger than the minimum width. This gate has two inputs, A1 (second, third, sixth and seventh transistors) and A2 (first, fourth, fifth and seventh transistors). The output signal (OUT) is represented by the 1-8 nodes in the center of the cell. As Table 6.1 shows, the TTF of the NOR2_X4 gate can be improved about 37% when the output pin position changes avoiding the critical pin positions, considering a 100% switching rate.

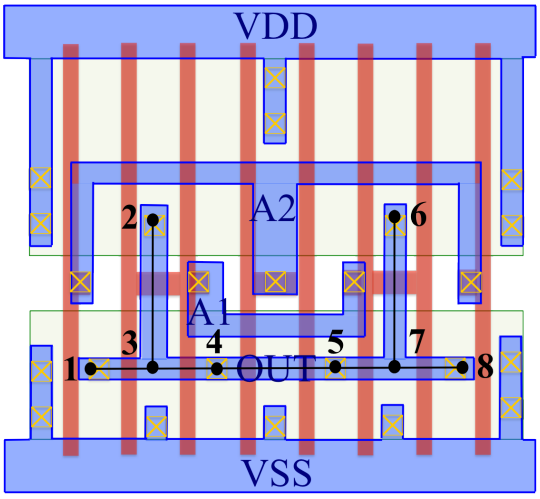
Figure 6.16: Layout options for a AOI21_X2 gate to improve the TTF.



(a) (b)

Source: (POSSER et al., 2015).

Figure 6.17: The layout and output pin position options for a NOR2_X4 gate.



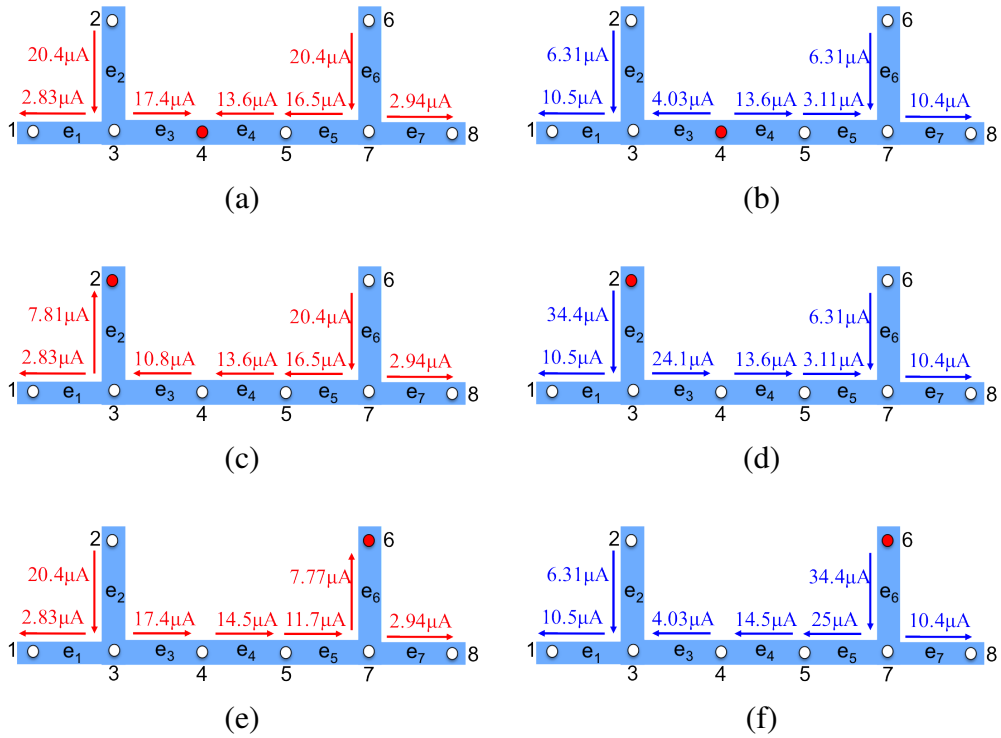
Source: (POSSER et al., 2015).

To explain how the current density and consequently the TTF of the cell changes for different pin positions, Figure 6.18 is presenting the average current values through the edges e_1-e_7 of the output signal obtained by SPICE simulation. For this simulation, we are considering $78ps$ as input slew and $8fF$ as output load. The wire thickness is the same for all wire segments, and the wire width is 20% larger just for the edge e_2, for the other edges the wire width is the same. Consequently, the current density through these wire segments will be determined by the largest I_{avg}.

For the rise transition, the current injection points are the nodes 2 and 6 and for the fall transition the current injection points are the nodes 1, 4, 5 and 8, as Figures 6.17 and 6.18 show. When the output pin is at node 4, Figure 6.18 (a) and (b), e_6 is the critical edge with an I_{avg} (Eq. 3.5) of 13.18μA. The same happens when the output pin is at nodes 1, 3, 5, 7 and 8, i.e., the critical edge is e_6. Changing the output pin to node 2 (Figure 6.18 (c) and (d)), even that e_2 is wider than the other edges, this is the critical edge with an I_{avg} (Eq. 3.4) of 14.52μA. When the output pin is changed to node 6, Figure 6.18 (e) and

(f), the critical edge will be e_6 with an I_{avg} of 14.48μA. This pin position produces the largest current through an edge, so this is the worst pin position for this cell. To find the best TTF (14.74 years, as Table 6.1 shows), the output pin can be placed at someone of these nodes 1, 3, 4, 5, 7 and 8. If the desired TTF is larger than that one achieved by the pin placement, some layout improvements can be made. One example is to increase the width of the edge e_6.

Figure 6.18: Rise [red] and fall [blue] average current values through the NOR2_X4 output wire segments when the output pin is at node 4 (a) and (b), node 2 (c) and (d) and, node 6 (e) and (f).



Source: (POSSER et al., 2015).

6.1.4 INV_X16

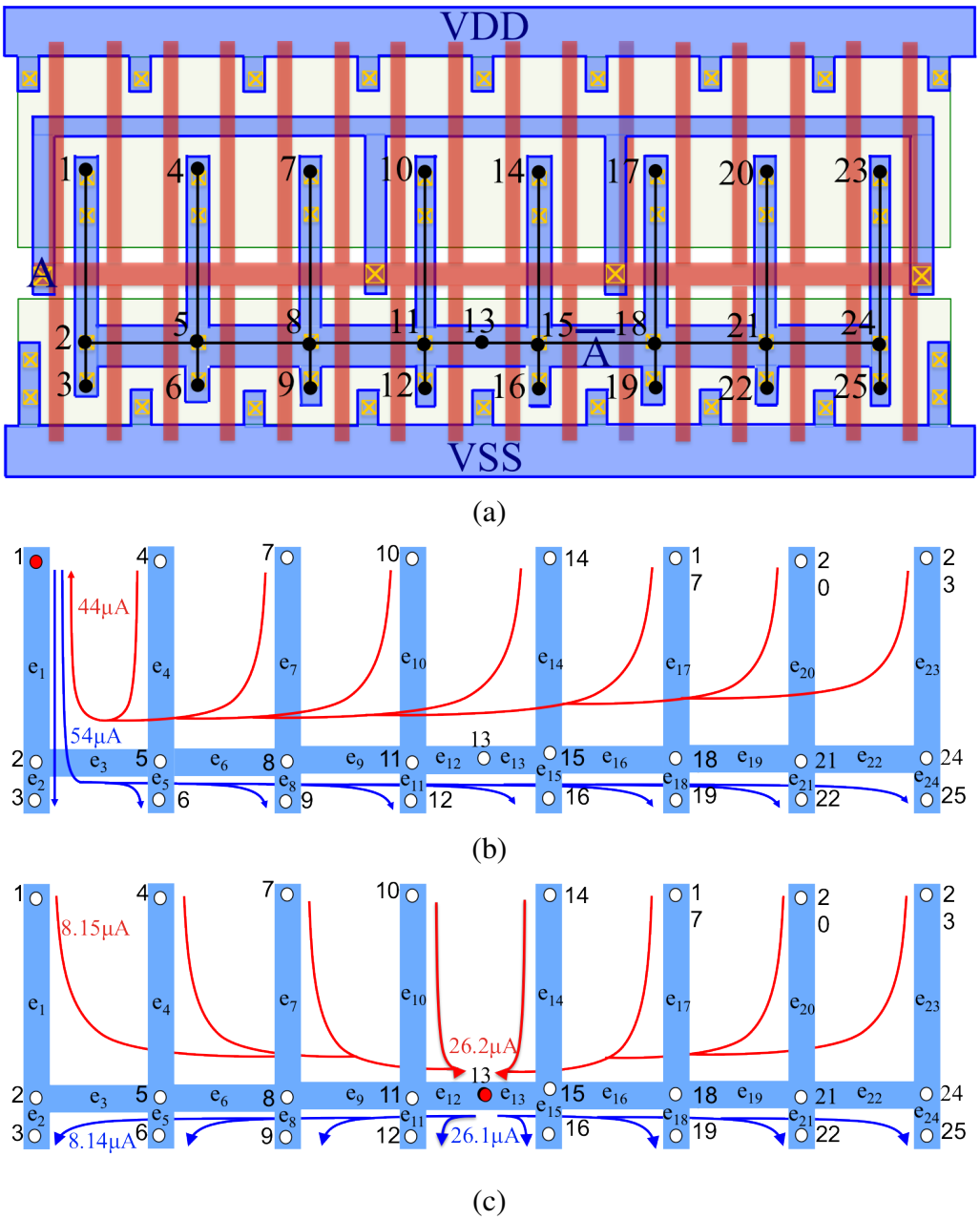
The largest TTF improvements choosing the best output pin position for the cells is for the inverter and buffer gates, where the largest improvement is for the INV_X16 cell, as Table 6.1 shows.

Figure 6.19 shows the layout of the INV_X16 (inverter with size 16). The output signal is represented by the 1-25 nodes in the center of the cell. The INV_X16 gate has 16 PMOS injection points and 16 NMOS injection points, as Figure 6.19 (a) shows. Thereby, depending where the pin is placed the current injected by all PMOS or NMOS injection points is flowing through the same edge, as the example in Figure 6.19 (b), where the pin is at node 1. In this case, there is a very large current density through edge e_1 and consequently a very low lifetime compared with other pin positions where the current given by the injection points is better distributed through the edges, that is the case in Figure 6.19 (c) where the output pin is at node 13, in the middle of the output wire. The horizontal edges (e_3, e_6, e_9, e_12, e_13, e_16, e_19 and e_22) are two times wider than the vertical edges.

The current injected at each PMOS injection point (1, 4, 7, 10, 14, 17, 20 and 23) is about 8.15μA and at each NMOS injection point (3, 6, 9, 12, 16, 19, 22 and 25) is about

the same, 8.14μA, as Figure 6.19 (c) shows. Pin at node 13 is the best pin position for the INV_X16, where the critical edges are the edges connected to the PMOS injection points (e_1, e_4, e_7, e_10, e_14, e_17, e_20 and e_23). Figure 6.19 (c) also shows that the rise current away node 13 is 26.2μA from edge e_12 and the same value from edge e_13. The fall current through these edges is about the same, but reversed. When the output pin is at node 1, the current from/to all injection points is flowing through e_1, as Figure 6.19 (b) shows, producing a large current through this edge, reducing its lifetime. This pin position produces the worst TTF for this gate, where the critical edge is e_1.

Figure 6.19: The layout of the INV_X16 (a), charge/discharge currents when the output pin is at (b) node 1 and (c) node 13. The red [blue] lines represent rise [fall] currents.



(a)

(b)

(c)

Source: (POSSER et al., 2015).

6.2 Conclusion

In this Chapter we presented the results obtained from our cell-internal EM analysis. The results present the importance of the pin placement for the output, Vdd and Vss pins. The tests executed for the bechmark circuits show that the circuit TTF can be improved up to 62.50% avoiding the critical output pin positions, 78.54% avoiding the critical Vdd pin positions and 89.89% avoiding the critical Vss pin positions.

We are also showing an analysis of the cell-internal signal EM effects for different logic gates considering just the output pin positions. Some logic gates presented a large lifetime improvement possibility changing the output pin position. This is caused by the way that the currents are flowing through the wire segments when the output pin is placed in different positions. In other hand, for some logic gates the lifetime remains practically unchanged when the output pin position changes. This is because the critical current density, that is through the critical edge, does not change when the output pin position and current flows change. Some layout improvements are suggested to increase the TTF of these cells where changing the output pin position, the TTF practically unchanged.

As a future work, we intend to construct the layouts with the modifications that improve the TTF of the gates. Moreover, the layout parasitics will be extracted and then the gates will be characterized to calculate the accurate TTF of the cells.

7 ANALYZING THE ELECTROMIGRATION EFFECTS ON DIFFERENT METAL LAYERS AND DIFFERENT WIRE LENGTHS

The analyzes, tests and results presented in the previous chapters of this work are treating the EM effects at cell level, for the wires inside of the cells. In this Chapter we are testing the EM effects at circuit level, on the nets that connect the cells (POSSER et al., 2014a). As the nets are signal wires, the direction of current flow is bidirectional and generally is referred as AC electromigration. The AC electromigration has become a serious concern and its limits become tighter with the technology scaling due to the increasing of the on-current of drivers with smaller channel lengths, the decreasing of the interconnect widths and a faster switching of the transistors increasing the operation frequency (KAHNG; NATH; ROSING, 2013). Thus, in this chapter the EM effects on these nets are analyzed for 6 different metal layers and three different wire lengths, 100μm, 200μm and 300μm in 22nm technology. The layouts are constructed considering the 45nm technology and scaled to 22nm technology.

The contributions presented in this chapter are as follows:

- To show how the EM affects different metal layers and different wire lengths.
- To analyze the delay behavior for the different metal layers and wire lengths.
- To present how the average current I_{avg} reduces through the wire.

The average and RMS currents are characterized at 2GHz as a reference frequency, f_{ref}. The simulation results presented in the Section 6 are considering an activity factor, α, of 100% at 2GHz. If the design is operating in a different frequency f and activity factor α, the average and RMS currents can be inferred, they are multiplicatively scaled by factors of $\alpha f/f_{ref}$ and $\sqrt{\alpha f/f_{ref}}$, respectively, as (POSSER et al., 2014) presents.

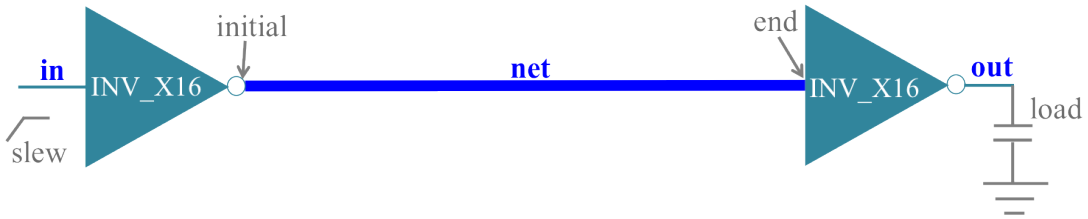
The EM lifetime estimation is computed as presented in Chapter 3, incorporating the Joule heating effects according to the Section 3.2 shows. As the Joule heating depends on the RMS current I_{rms}, wire resistance R, dielectric thickness t_{ins} and the thermal conductivity K_{ins}. We obtain I_{rms} by SPICE characterization. R is obtained by parasitic extraction using a commercial tool, t_{ins} changes for different metal layers, as Table 7.1 shows, and $K_{ins} = 0.07$W/m.K (BANERJEE; MEHROTRA, 2001).

7.1 Experimental Setup

To evaluate the EM effects in different metal layers considering different wire lengths, the block diagram presented in Figure 7.1 is the test case used to run the experiments. The block diagram is composed by two INV_X16 from the 45nm NANGATE Open cell library (NANGATE, 2011) connected by a net (wire). In the tests, we are changing the metal layer and the wire length of this net. The width of this net is the minimum value given by the technology, as Table 7.1 presents. For each metal layer and different wire length, a different layout is designed and the parasitics are extracted using a commercial

tool. The parasitic extractor divides the wire into a number of wire segments. Thus, a separate TTF is calculated for each wire segment and the worst TTF is considered. The worst TTF is the TTF of the closest segment of the first INV_X16, this is because the parasitics of each segment reduce the current flowing through the next segment.

Figure 7.1: Block diagram used to analyze the characteristics for different metal layers with different wire lengths.



Source: (POSSER et al., 2014a).

Table 7.1 presents the minimum wire width (W), the wire thickness (T_w) and the dielectric thickness t_{ins} considered in our tests based on the values from the Free PDK 45nm technology (FREEPDK45, 2011) and the scaled values to 22nm technology.

Table 7.1: Minimum wire width (W), wire thickness (T_w) and the dielectric thickness t_{ins} based on the values from 45nm technology (FREEPDK45, 2011) and the values scaled to 22nm technology.

Metal layers	**45nm technology (FREEPDK45, 2011)**			**22nm technology**		
	W **(nm)**	T_w **(nm)**	t_{ins} **(nm)**	W **(nm)**	T_w **(nm)**	t_{ins} **(nm)**
M1	70	130	120	34	64	59
M2	70	140	120	34	68	59
M3	70	140	120	34	68	59
M4	140	280	290	68	137	142
M5	140	280	290	68	137	142
M6	140	280	290	68	137	142

Source: (POSSER et al., 2014a).

The simulations are executed considering the layout constructed based on the block diagram shown in Figure 7.1. The structure of the block diagram is kept; just the wire length and the metal layer of the net are changed. The layouts are scaled from the 45nm Nangate cell library down to 22nm technology. In 45nm, the wire lengths used in the layout are 200μm, 400μm and 600μm. Scaling to 22nm technology, these wire lengths will be about 100μm, 200μm and 300μm. SPICE simulation is used to characterize the layout for I_{avg} and I_{rms} values considering 2GHz as a reference frequency, f_{ref}, and a temperature of 378K. The simulations are executed considering the scaled 22nm library based on the 22nm SPICE ASU PTM model for High Performance applications (PTM HP), and the supply voltage (VDD) used is 0.88V.

The design is characterized for 7 different values each for the input slew and output load, generating a 7×7 look-up table with the RMS and average current values. The

input slew values are applied to the in signal that is the input of the first inverter in the Figure 7.1. The output load is the capacitance connected to the out signal, i.e., to the output of the second INV_X16. The output load of the first INV_X16 is a combination of the net capacitance plus the capacitance of the second INV_X16 plus the output load connected to the second INV_X16. The maximum input slew and output load values are determined based on SPICE simulation. They are limited by the largest values that enable the out signal to reach the VDD value and to get an output transition time smaller than the maximum input slew, defined as 198.5ps. The other constraints are the minimum input slew, defined as 1.2ps and the minimum output load, equal to 0.6fF, which is an approximation of the input capacitance of the inverter with size 1 scaled from the 45nm technology to the 22nm technology. The TTF values are calculated considering just the current through the wire, the TTF of the vias is not calculated.

7.2 Simulation Results

The results presented in this section are considering the layout of the block diagram shown in Figure 7.1. Table 7.3 presents the worst TTF for a combination of allowable input slew and output load and the conditions where it occurs, i.e., the input slew and the output load of the worst TTF that are presented in Table 7.2 . Moreover, the TTF reduction is also shown for the conditions when the wire length that connects the two INV_X16 in the Figure 7.1 is increased from 100μm to 200μm and from 200μm to 300μm in 22nm technology. The input slew for the worst TTF was the same for all test cases, and it is the minimum input slew considered in our tests. This is expected because as faster is the input transition, larger is the provided current reducing the TTF. The output load presented in the table is that connected to the second INV_X16 in Figure 7.1 and its value for the worst TTF is always larger than the constraint 0.6fF.

Table 7.2: Input slew and output load for the different wirelengths of the net in the layout presented in Figure 7.1.

Metal	**Input slew** (ps)			**Output load** (fF)		
layers	**100**μm	**200**μm	**300**μm	**100**μm	**200**μm	**300**μm
M1	1.2	1.2	1.2	0.60	0.60	0.60
M2	1.2	1.2	1.2	0.60	0.60	1.20
M3	1.2	1.2	1.2	0.60	0.60	0.60
M4	1.2	1.2	1.2	2.00	0.60	0.60
M5	1.2	1.2	1.2	2.00	0.60	0.60
M6	1.2	1.2	1.2	2.00	0.60	7.50

Source: (POSSER et al., 2014a).

About the EM effects, Table 7.3 shows that as lower is the metal layer, lower is the lifetime of the wire. Considering that traditional IC implementation flows have an intended TTF of at least 10 years (KAHNG; NATH; ROSING, 2013) (LIENIG, 2013), there are some TTF values in the table smaller than 10 years. And we are considering the test cases with a TTF smaller than 10 years as critical. The wires in metal 1 are all critical, where the criticality is increased as the wire length increases. The wires in metal 2 and metal 3

have a critical TTF for a wire length of 200μm and 300μm, for a wire length of 100μm the TTF is larger than 10 years. For the metal layers 4, 5 and 6 the TTF is not critical for the wire lengths we are considering in this work, where the smallest TTF for these metal layers is 23.89 years for a wire length of 300μm. The TTF reduction when the wire length is increased from 100μm to 200μm is about 35% and from 200μm to 300μm the TTF is reduced from 3.85% to 27.61%.

Table 7.3: TTF and the TTF reduction when the wire (net) length of the layout presented in Figure 7.1 is changed from 100μm to 200μm and from 200μm to 300μm.

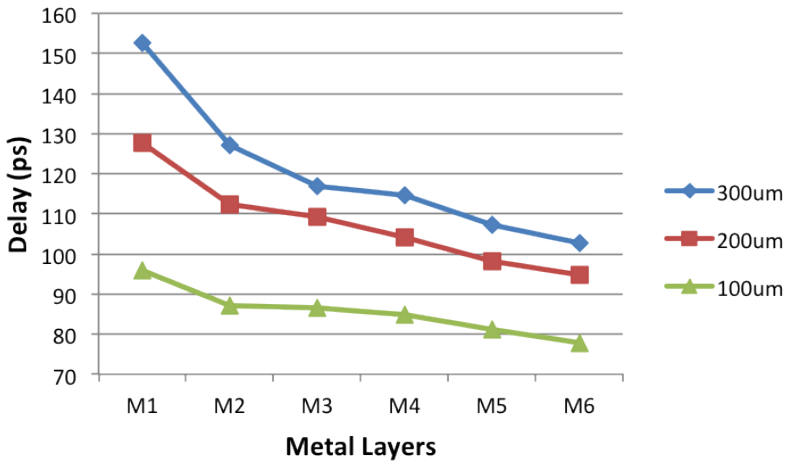
Metal layers	**TTF (years)**			**TTF reduction (%)**	
	100μm	**200μm**	**300μm**	$\frac{200\mu m}{100\mu m}$	$\frac{300\mu m}{200\mu m}$
M1	8.59	5.71	5.49	**33.53**	**3.85**
M2	11.06	6.94	5.50	**37.25**	**20.75**
M3	13.10	8.54	6.85	**34.81**	**19.79**
M4	52.52	33.00	23.89	**37.17**	**27.61**
M5	58.90	38.88	28.75	**33.99**	**26.05**
M6	63.00	42.82	31.99	**32.03**	**25.29**

Source: (POSSER et al., 2014a).

Our tests show that the TTF is smaller for lower metal layers, even when the metal layers have the same wire width, wire length and wire thickness. One reason for this is the parasitic capacitance on the wire. Looking the parasitic extraction file, as possible to see that the parasitic capacitances are larger as lower is the metal layer.

Figure 7.2 shows the delay (ps) by metal layers considering the three different wire lengths 100μm, 200μm and 300μm of the test cases presented in Tables 7.2 and 7.3. The figure shows that the delay increases as the wire length increases because the wire resistance increases. Furthermore, as higher is the metal layer, smaller is the delay because the wire width and wire thickness are higher, reducing the wire resistance.

Figure 7.2: Delay (ps) by metal layers considering the three different wire lengths in 22nm 100μm, 200μm and 300μm.



Source: (POSSER et al., 2014a).

Table 7.4 presents the maximum input slew and the maximum output transition time (tt) from 5% to 95% (95%-5%) of the output signal in ps for the different metal layers and wire lengths tested in this work. The maximum input slew we are considering, 198.5ps, is about 40% of the clock period (500ps).

All the maximum output transition time values shown in Table 7.4 are smaller than the maximum input slew. Thus, the second inverter is able to load other cells and wires since the output signal can reach the VDD value and the output transition time is respected. For metals 1, 2 and 3 and wire length of 300μm, the input slew has to be smaller than the maximum value because using larger input slew than the values presented in the table the output transition time constraint is not respected.

Table 7.4: Max input slew and max output transition time (tt) for the different metal layers and wire lengths used in this work.

Metal layers	**100μm**		**200μm**		**300μm**	
	input slew (ps)	**output tt (ps)**	**input slew (ps)**	**output tt (ps)**	**input slew (ps)**	**output tt (ps)**
M1	198.5	142.4	198.5	155.1	17.2	197.2
M2	198.5	144.0	198.5	155.6	130.0	174.0
M3	198.5	142.6	198.5	156.6	180.0	161.8
M4	198.5	142.4	198.5	162.5	198.5	171.0
M5	198.5	137.9	198.5	160.5	198.5	172.1
M6	198.5	130.6	198.5	160.3	198.5	170.0

Source: (POSSER et al., 2014a).

Table 7.5 presents the effective average current I_{avg} in μm, calculated by equation 3.3, for the tests presented in Table 7.2, i.e., for that input slew and output load. Table presents the I_{avg} value at the point where the net starts (initial), that is the point connected to the via that is connected to the output of the first INV_X16. And the average current at the point where the net ends (end), that is the point connected to the via that is connected to the input of the second INV_X16 in the Figure 7.1.

Table 7.5: The effective average current (I_{avg}) in μA at the point where the net starts (initial) and at the point where the net ends (end) for the different wire lengths.

Metal layers	**100μm**			**200μm**			**300μm**		
	Initial	**End**	**Red. ($\times$)**	**Initial**	**End**	**Red. ($\times$)**	**Initial**	**End**	**Red. ($\times$)**
M1	15.5	6.87	**2.26**	21.9	6.27	**3.49**	25.3	5.48	**4.62**
M2	14.4	6.97	**2.07**	21.0	6.71	**2.22**	25.6	6.11	**4.19**
M3	13.1	6.94	**1.89**	18.7	6.73	**2.78**	22.6	6.20	**3.65**
M4	14.5	7.03	**2.06**	21.1	6.85	**3.08**	27.4	6.63	**4.13**
M5	13.2	7.04	**1.88**	18.7	6.88	**2.72**	24.0	6.71	**3.58**
M6	12.5	7.06	**1.77**	17.4	6.89	**2.53**	22.3	6.69	**3.33**

Source: (POSSER et al., 2014a).

The average current reduces significantly along the wire, as Table 7.5 shows. For a wire with 100μm, the current reduces from 1.77 to 2.26$\times$ until reaching the via connected to the second inverter. The metal 1 has the largest current reduction. For a wire length of 200μm, the current is reduced from 2.22 to 3.49$\times$ along the wire. For a wire with 300μm, the current reduces from 3.33 to 4.62$\times$ through the wire in our test cases.

Table 7.6 shows that increasing the wire length, the I_{avg} current at the *initial* point reduces from 63.2 to 89% when the wire length is increased from 100μm to 300μm. At the end *point* of the wire, the I_{avg} current reduces from 4.7 to 20.2% when increasing the wire length from 100μm to 300μm.

Table 7.6: The I_{avg} reduction (Red.) in $\times$ and the I_{avg} reduction at the begin and end points when the wire length is increased considering the values presented in Table 7.5.

Metal layers	**Initial comparison (%)**			**End comparison (%)**		
	$\frac{200\mu m}{100\mu m}$	$\frac{300\mu m}{200\mu m}$	$\frac{300\mu m}{100\mu m}$	$\frac{200\mu m}{100\mu m}$	$\frac{300\mu m}{200\mu m}$	$\frac{300\mu m}{100\mu m}$
M1	41.3	15.5	63.2	8.7	12.6	20.2
M2	45.8	21.9	77.8	3.7	8.9	12.3
M3	42.8	20.9	72.5	3.0	7.9	10.7
M4	45.5	29.9	89.0	2.6	3.2	5.7
M5	41.7	28.3	81.8	2.3	2.5	4.7
M6	39.2	28.2	78.4	2.4	2.9	5.2

Source: (POSSER et al., 2014a).

7.3 Conclusion

This chapter has shown an analysis of the EM effects on different metal layers for different wire lengths. We can conclude that as lower is the metal layer, lower is the lifetime of the wire. Then, higher metal layers have smaller EM effects and consequently a higher lifetime for the wires. We are considering critical the nets with a TTF smaller than 10 years. The wider wires have a larger TTF because the current density through these wires is smaller, reducing the EM effects. The signal nets in metal 1 in out test cases for wire lengths of 100μm, 200μm and 300μm are critical and the lifetime is reduced as the wire length increases. The wires in metal 2 and metal 3 have a critical TTF for a wire length of 200μm and 300μm. For the metal layers 4, 5 and 6 the TTF is not critical for the wire lengths we are considering in this work. The delay in our test cases increases when the wire length increases and decreases for a higher metal layer, i.e., as lower is the metal layer higher is the delay.

As a future work, we intend to evaluate the EM effects on the vias, comparing the effects for the different metal layer vias and considering the vias connected to different wire lengths.

8 CONCLUSION AND FUTURE WORKS

We have developed an approach to touch upon the problem of cell-internal EM, addressing the problem of EM on signal interconnects and on Vdd and Vss rails within a standard cell. A new modeling approach that includes Joule heating effects and current divergence is presented. Based on the review through the literature, few works are concerned with cell-internal EM. To our knowledge, there are no other published approach addressing this problem directly. Thus, our work is the first one to optimize the pin positions of the output, Vdd and Vss wires in standard cells improving the circuit lifetime. We now summarize the main contributions of this work and the possible future works. Publications achieved by the author both within the scope of this work and in cooperation with other researchers in other themes are listed in Section 8.3.

8.1 Summary of Contributions

The main contributions of this work are summarized as follows:

- **A study of the problem of analyzing the EM effects inside standard cells for the output, Vdd and Vss wires:** we show that the current that flows through the local interconnect wires can be large enough to create significant EM effects over the lifetime of the chip.

- **Cell-internal EM modeling:** The EM was modeled incorporating Joule heating effects and the current divergence to estimate the lifetime of the signal and supply wires.

- **An approach to efficiently characterize cell-internal EM over all output, Vdd and Vss pin locations within a cell using a reference pin position:** Wherein a graph-based algorithm is used to compute the currents through each edge when the pin position is moved from the reference case to another location. This algorithm speeds up the characterization by the number of different pin positions along with the AVG and RMS currents computation, producing a small calculation error compared to SPICE simulation, just 0.53% on average.

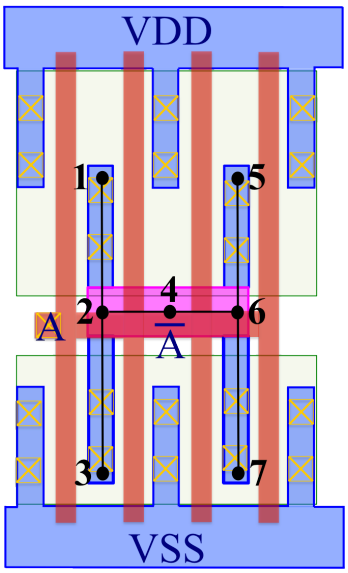
- **The pin placement optimization problem formulation for the output, Vdd and Vss pins, where the lifetime of the overall design is maximized:** The pin optimization reports the critical pin positions to be avoided to maximize the circuit lifetime. They are avoided by just changing the LEF (Library Exchange Format) file of the cells, the cell layouts are not changed. Applying this optimization, the circuit lifetime could be improved up to 62.50% for the benchmark set used in this work. This improvement was possible by just avoiding the critical output pin positions, keeping the circuit area, delay, power and wirelength. When the output, Vdd, and Vss pin positions are optimized, the lifetime of the circuits could be improved up to 80.95%.

8.2 Future Works

As we already have presented, there are few works concerned with the EM effects through the wires within a cell. We presented that the lifetime of the circuit could be improved substantially avoiding the critical pin positions of the output, Vdd and Vss wires. Thereby, we intend to continue this work where some possibilities are presented below.

1. The EM problem is intensifying with the latest technologies making it necessary to more robust designs, wider metals in critical nets and even in some cases the outputs of the cells will use metal 2 to reduce the EM effects (YERIC et al., 2013). Thus, we intend to study the EM effects considering two metal layers on the output signal of the cell, wherein the first metal is used for the vertical interconnections and metal 2 for the horizontal interconnections like the new technologies are using (BAN et al., 2014) (VAIDYANATHAN et al., 2014), as Figure 8.1. Moreover, in this case the EM effects on the vias from metal 1 to metal 2 also should be considered.

Figure 8.1: Layout of the INV_X4 where the output pin is using 2 metal layers, metal 1 for the vertical interconnections and metal 2 for the horizontal interconnections.



Source: from author (2015).

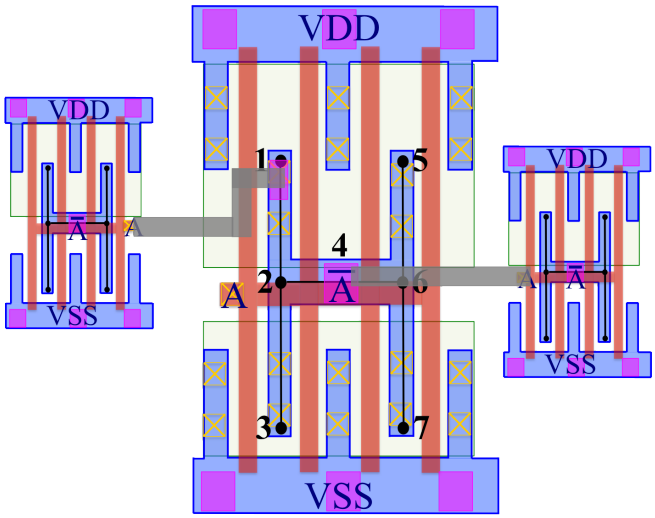
2. To synthesize the circuits avoiding the critical Vdd and Vss pin positions.

3. To consider more than 1 pin placed simultaneously on the Vdd and Vss rails. And also on the output wire for cells with a fanout larger than one, i.e., driving more than one cell as Figure 8.2 shows.

4. To estimate the temperature, used to calculate the TTF, for each cell considering a heat map from a commercial tool. The idea is to use this temperature information to analyze the final TTF, considering the global information to apply to the cells.

5. To study how the commercial tools, like Encounter (CADENCE, 2013) and Virtuoso (CADENCE, 2015) from Cadence analyze the EM and the current density through the circuit wires. The type of wires that these tools are able to analyze will also be studied and reported.

Figure 8.2: Layout of the INV_X4 with the output, Vdd e Vss pins placed. The output of the cell is connected to other two cells.



Source: from author (2015).

6. To construct the layouts with the modifications that improve the TTF of the logic gates where the lifetime remains practically unchanged when the output pin position changes or when the lifetime is below of a given specification. One layout modification is to do the critical wires wider to increase its lifetime. Moreover, the layout parasitics will be extracted and then the gates will be characterized to calculate the accurate TTF of the cells.

7. We also would like to test the EM effects considering cell layouts constructed using the 32/28nm Synopsys PDK library (SYNOPSYS, 2014b) and the FreePDK in 15nm (FREEPDK15, 2014) used to construct the NanGate FreePDK15 Open Cell Library (NANGATE, 2014). Furthermore, we intend also use libraries from foundries in recent technologies, like TSMC, Global Foundries.

8.3 Publications

The following publications were achieved by the author during the PhD course.

8.3.1 Patent

Considering that the theme of this thesis is a new method in the literature, in 2013 we started a process to achieve a patent application to U.S. Patent and Trademark Office ("USPTO"). The patent information are as follow.

POSSER, G.; MISHRA, V.; SAPATNEKAR, S. S.; JAIN, P.; REIS, R. Cell-level Signal Electromigration. 2014, Estados Unidos. Attorney Docket Number: U11.12-0229 in 30/05/2014 at United States Patent and Trademark Office.

8.3.2 Awards

The author was member of the team that won the 1st Place in the Primary Ranking of the ISPD 2013 Discrete Gate Sizing Contest organized by ACM/SIGDA and Intel researchers. As well as, this team also won the 1st Place in the Secondary Ranking and

the 2nd Place in Primary Ranking of the ISPD 2012 Discrete Gate Sizing Contest.

8.3.3 Journal

1. POSSER, G.; MISHRA, V.; JAIN, P.; REIS, R.; SAPATNEKAR, S. S. Cell-Internal Electromigration: analysis and pin placement based optimization. **IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems**, (under review), 2015.

2. FLACH, G.; REIMANN, T.; POSSER, G.; JOHANN, M.; REIS, R. Effective Method for Simultaneous Gate Sizing and Vth Assignment Using Lagrangian Relaxation. **IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems**, v.33, n.4, p.546-557, April 2014.

3. POSSER, G.; FLACH, G.; WILKE, G.; REIS, R. Gate sizing using geometric programming. **Analog Integrated Circuits and Signal Processing**, [S.l.], v.73, n.3, p.831-840, 2012.

8.3.4 International Conferences, Symposiums and Workshops

1. POSSER, G.; MISHRA, V.; JAIN, P.; REIS, R.; SAPATNEKAR, S. S. A Systematic Approach for Analyzing and Optimizing Cell-Internal Signal Electromigration. In: ICCAD'14, 2014. p.486-491.

2. POSSER, G.; MISHRA, V.; REIS, R.; SAPATNEKAR, S. S. Analyzing the Electromigration Effects on Different Metal Layers and Different Wire Lengths. In: ICECS 2014, Marseille, France. 2014, p.682-685.

3. POSSER, G.; PARIS, L. de; MISHRA, V.; JAIN, P.; REIS, R.; SAPATNEKAR, S. S. Reducing the Signal Electromigration Effects on Different Logic Gates by Cell Layout Optimization. In: VI Latin American Symposium on Circuits & Systems - LASCAS 2015, Montevideo, Uruguay, 2015.

4. POSSER, G.; MISHRA, V.; JAIN, P.; REIS, R.; SAPATNEKAR, S. S. Uma Abordagem Sistemática para Analisar e Otimizar os Efeitos da Eletromigração nos Sinais Internos das Células. In: XXI IBERCHIP, Montevideo, Uruguay, 2015.

5. POSSER, G.; BELOMO, J.; MEINHARDT, C.; REIS, R. Perfomance Improvement with Dedicated TransistorSizing for MOSFET and FinFET Devices. In: 2014 IEEE Computer Society Annual Symposium on VLSI (ISVLSI), 2014.

6. POSSER, G.; BELOMO, J.; MEINHARDT, C.; SAPATNEKAR, S. S.; REIS, R. Dimensionamento de Transistores para dispositivos MOSFETs e FinFETs. In: Iberchip, 2014, Santiago/Chile.

7. FLACH, G.; REIMANN, T.; POSSER, G.; JOHANN, M.; REIS, R. Dimensionamento de Portas e Assinalamento de Vth Simultâneos usando Relaxação Lagrangiana. In: Iberchip, 2014, Santiago/Chile.

8. FLACH, G.; REIMANN, T.; POSSER, G.; JOHANN, M.; REIS, R. Simultaneous gate sizing and Vth assignment using Lagrangian Relaxation and delay sensitivities. In: IEEE Computer Society Annual Symposium on VLSI (ISVLSI), 2013. p.84-89.

9. REIMANN, T. ; POSSER, G.; FLACH, G.; JOHANN, M.; REIS, R. Simultaneous gate sizing and Vt assignment using Fanin/Fanout ratio and Simulated Annealing. In: IEEE International Symposium on Circuits and Systems (ISCAS), 2013. p.2549-2552.

10. REIMANN, T. ; POSSER, G.; FLACH, G.; JOHANN, M.; REIS, R. Dimensionamento de Portas e Assinalamento de Vt usando Fanin/Fanout e Simulated Annealing. In: XIX Iberchip Workshop, 2013, Cusco.

11. POSSER, G.; REIS, R.; SAPATNEKAR, S. S. Transistor Sizing for MOSFET and FINFET Devices. In: VLSI-SoC 2013's Ph.D. Forum, 2013, Istanbul.

12. POSSER, G.; FLACH, G.; WILKE, G.; REIS, R. Dimensionamento de Portas Lógicas e de Transistores Minimizando Atraso e Área. In: 18th Workshop IBERCHIP, 2012, Playa Del Carmen.

13. POSSER, G.; FLACH, G.; WILKE, G.; REIS, R. Tradeoff Between Delay and Area in the Gate Sizing using Geometric Programming. In: Third IEEE Latin American Symposium on Circuits and Systems - LASCAS, 2012, Playa Del Carmen.

14. POSSER, G.; FLACH, G.; WILKE, G.; REIS, R. Transistor Sizing and Gate Sizing Using Geometric Programming Considering Delay Minimization. In: 10th IEEE International NEWCAS Conference, 2012, Montreal/Canada.

15. POSSER, G.; FLACH, G.; WILKE, G.; REIS, R. Gate Sizing using Geometric Programming. In: IEEE Latin American Symposium on Circuits and Systems - LASCAS, 2011, Bogotá.

16. POSSER, G.; ZIESEMER JR., A.; GUIMARÃES JR., D.; WILKE, G.; REIS, R. Estudo da Qualidade do Leiaute de Células Geradas Automaticamente. In: Iberchip, 2011, Bogotá.

17. POSSER, G.; FLACH, G.; WILKE, G.; REIS, R. Transistor Sizing and Gate Sizing Using Geometric Programming. In: 1st Workshop on Circuits and Systems Design - WCAS 2011, 2011, João Pessoa/PB.

18. POSSER, G.; FLACH, G.; WILKE, G.; REIS, R. Gate Sizing Using Geometric Programming Minimizing Delay and Area. In: IEEE Computer Society Annual Symposium on VLSI - ISVLSI, 2011, Chennai. p. 315-316.

8.3.5 Local Conferences, Symposiums and Workshops

1. FLACH, G.; REIMANN, T.; POSSER, G.; JOHANN, M.; REIS, R. Simultaneous Gate Sizing and Vth Assignment using Lagrangian Relaxation and Delay Sensitivities. In: 28th South Symposium on Microelectronics - SIM 2013, 2013, Porto Alegre - RS.

2. POSSER, G.; FLACH, G.; WILKE, G.; REIS, R. Transistor Sizing and Gate Sizing Using Geometric Programming Considering Delay Minimization. In: 27th South Symposium on Microelectronics - SIM 2012, 2012, Ijuí e São Miguel das Missões.

3. BELOMO, J. ; POSSER, G.; FLACH, G. ; REIS, R. An Introduction of Geometric Programming Using Gate Sizing. In: 27th South Symposium on Microelectronics - SIM 2012, 2012, Ijuí e São Miguel das Missões.

4. POSSER, G.; FLACH, G.; WILKE, G.; REIS, R. Gate Sizing Minimizing Delay and Power/Area. In: 26th South Symposium on Microelectronics - SIM, 2011, Novo Hamburgo/Gramado.

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APPENDIX A IMPACT ON PHYSICAL SYNTHESIS CONSIDERING DIFFERENT AMOUNTS OF INSTANCES WITH EM AWARENESS

As Chapter 6 presented, the TTF of the cells can be improved avoiding the critical pin positions that produces high current densities through some wire segments and consequently EM effects in these wires. For this, a pin placement problem was formulated to achieve the best TTF of a circuit placing the output, Vdd and Vss pins. The physical synthesis was executed for a set of benchmark circuits with no EM awareness and after for the "best" output pin positions (we did not execute yet the physical synthesis avoiding the critical Vdd and Vss pin positions), where the number of critical cells is small. In this way, to consider the constrained pin positions for these cells, the router makes changes to some interconnect routes. As the number of critical cells is small, the results after physical synthesis considering the best pin positions shows a TTF improvement up to 62.50% while keeping the delay, area and power of the circuit unchanged.

In this way, this appendix is presenting a set of tests to show the percentage of cell instances that can have EM-unsafe pin positions avoided with a low impact in area, delay, power and wirelength. The physical synthesis is executed for the set of benchmark circuits for these conditions:

- with no EM awareness, considering the traditional situation with all output pin positions from the original LEF file (original results).
- for the "best" output pin positions, that are the results presented in Chapter 6 (best TTF results).
- considering a TTF of 10 years, where there are a large number of critical cell instances (10 years TTF results).
- changing about 50% of the total number of instances of the circuit to avoid the EM-unsafe pin positions of these cells (50% instances changed results).
- avoiding the EM-unsafe pin positions of about 100% of the instances of the circuit (100% instances changed results).

Then, the area, delay, power and wirelength are reported for each one of these conditions to show what is the impact when the number of cells that have their output pin positions restricted increases.

Figures A.1-A.9 show the period, total power (leakage + switching power), area of core and the total wirelength variation (%) compared to the original results when the number of instances changed (%) to avoid the critical pin positions increases. The positive values shows that the characteristics are improved and the negative values shows the opposite. The four points in the charts are representing the following situations:

1. the first point are the results considering the best TTF results compared to the original results.

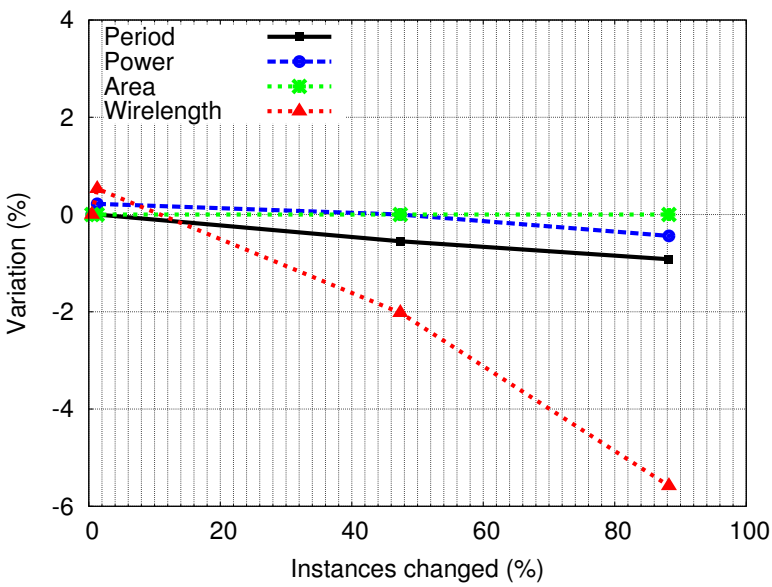
2. the second point are the results when a TTF of 10 years is considered compared to the original results.

3. the third point are the results when about 50% of the instances are changed to avoid the critical pin positions compared to the original results.

4. the fourth point are the results when about 100% of the instances are changed to avoid the critical pin positions compared to the original results.

Figure A.1 shows the variation results for the benchmark b05, where the area is kept the same of the original results. The period and power increase less than 1% and the wirelength increases about 2% when about 50% of the cells have the critical pin positions avoided and 6% when about 100% of the instances avoid the EM-unsafe pin positions.

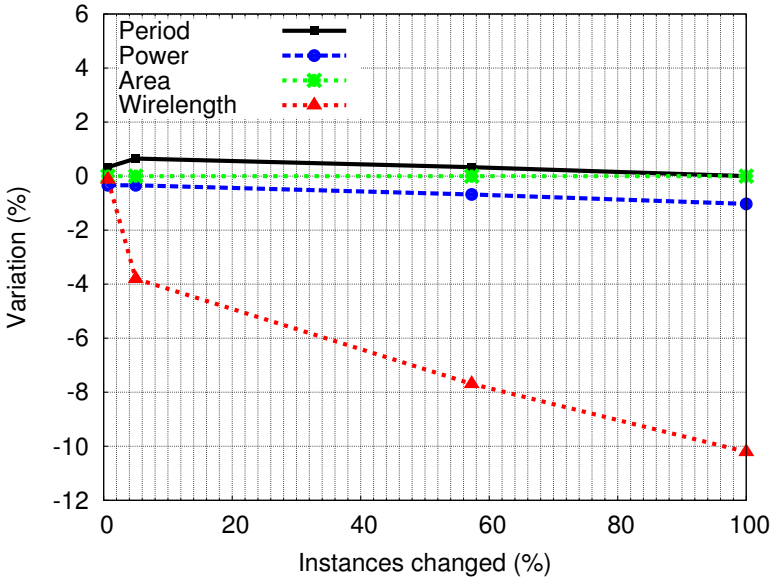
Figure A.1: Period, power, area and wirelength variation (%) when the number of instances changed (%) to avoid the critical pin positions increases for the benchmark b05.



Source: from author (2015).

The variation results for the benchmark b07 are shown in Figure A.2. Area is kept the same of the original results. The period and power change less than 1% and the wirelength increases a maximum of 10% when 100% of the instances avoid the EM-unsafe pin positions.

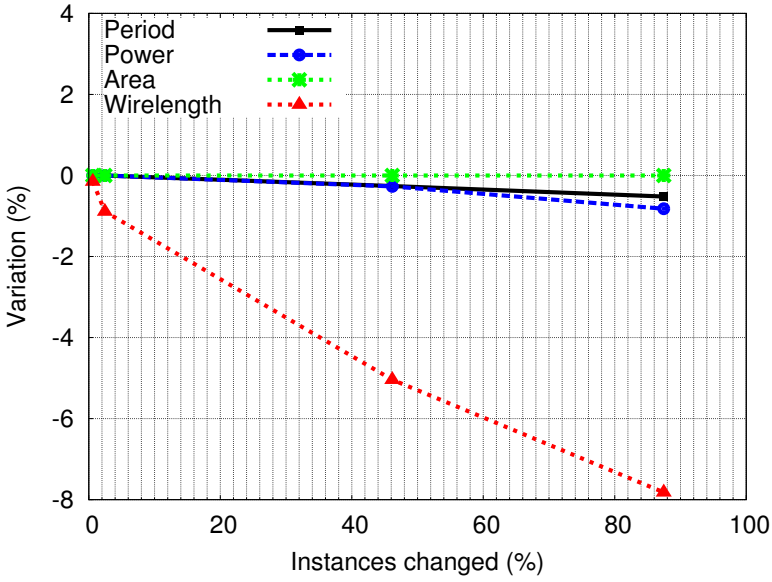
Figure A.2: Period, power, area and wirelength variation (%) when the number of instances changed (%) to avoid the critical pin positions increases for the benchmark b07.



Source: from author (2015).

The variation results for the benchmark b11 are shown in Figure A.3. Area is kept the same of the original results. The period and power reduce less than 1% and the wirelength increases about 5% when 50% of the instances are avoiding the critical pin positions. When 100% of the instances avoid the EM-unsafe pin positions, the wirelength increases about 8%.

Figure A.3: Period, power, area and wirelength variation (%) when the number of instances changed (%) to avoid the critical pin positions increases for the benchmark b11.

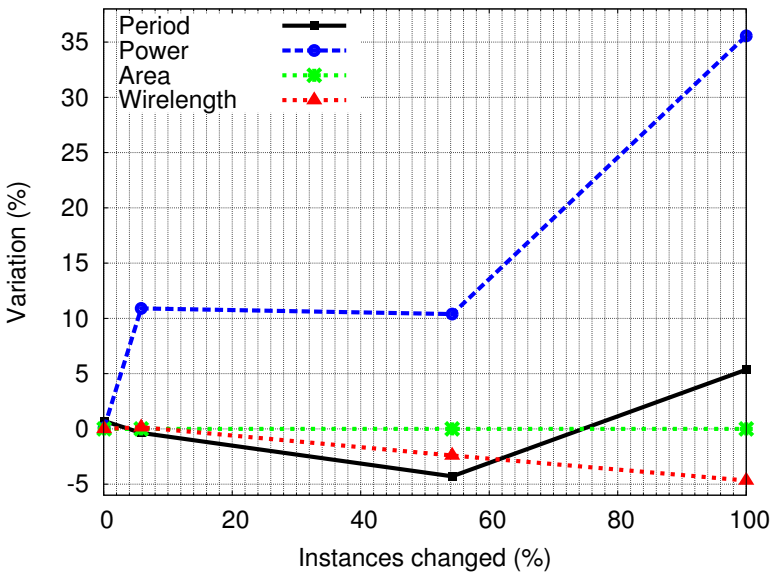


Source: from author (2015).

Figure A.4 shows the variation results for the benchmark b12. For this circuit, the area is kept the same of the original results. The other characteristics have a larger variation

than the variation in other circuits. The wire length increases up to 5% when 100% of the instances avoid the EM-unsafe pin positions. The period increases about 5% when about 50% of the instances are avoiding the critical pin positions and the period reduces more than 5% when 100% of the instances avoid the EM-unsafe pin positions. As more instances have the critical pin position avoided, more the power is reduced. The power could be reduced about 35% avoiding the critical pin positions of the all instances in this circuit. For this circuit, the routes did by the router when the pin positions are restricted for all instances in the circuit were better than the previous routing, with less pin position constraints. Doing the synthesis considering different combinations of the restricted instances, the results can change considerably for this circuit. For example, keeping the power like the power for the original synthesis and reducing the wirelength; reducing the area of core or; just keeping the characteristics close to the original synthesis. The routing is greatly affected by the output pin positions of some cells, where a more constrained routing (due the critical pins avoiding) can produces better results than an unconstrained, where all output pin positions can be used.

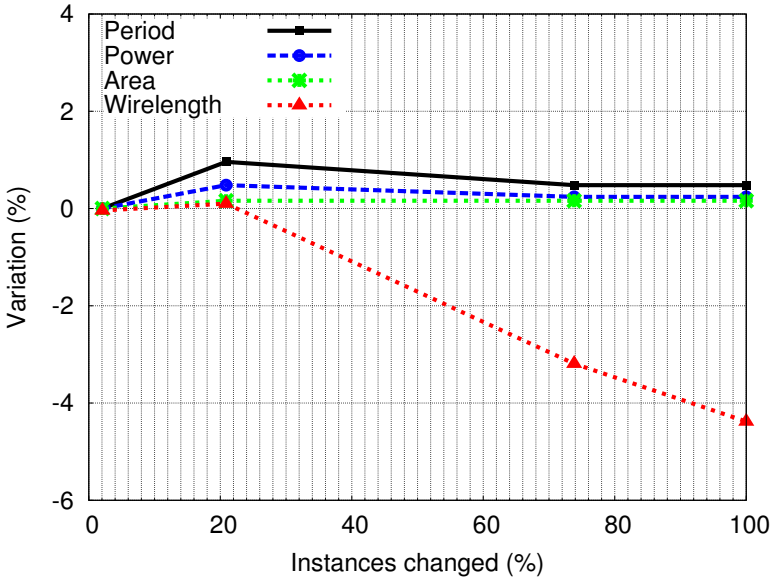
Figure A.4: Period, power, area and wirelength variation (%) when the number of instances changed (%) to avoid the critical pin positions increases for the benchmark b12.



Source: from author (2015).

The variation results for the benchmark b13 are shown in Figure A.5. Area is kept practically the same of the original results. The period and power can be reduced about up to 1%, where the higher reduction is when the critical pin positions are avoided to achieve a TTF of 10 years. The wirelength increases about 3% when 50% of the instances are avoiding the critical pin positions. When 100% of the instances avoid the EM-unsafe pin positions, the wirelength increases less than 5%.

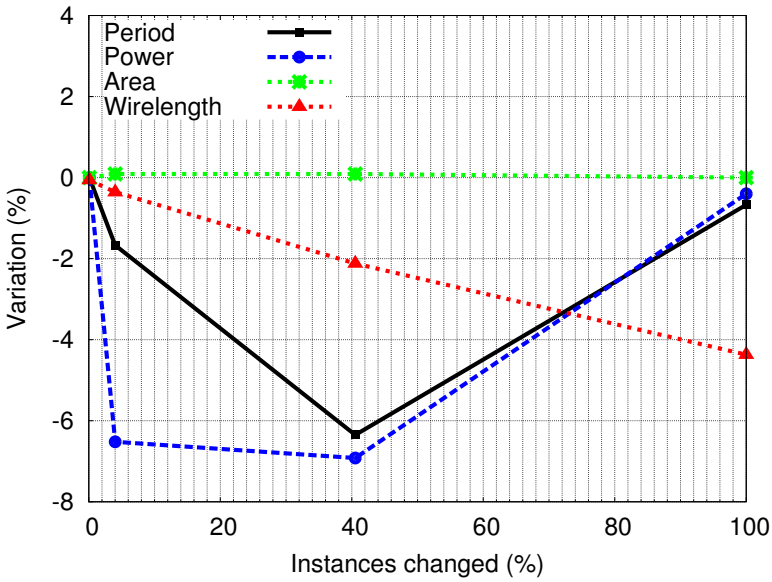
Figure A.5: Period, power, area and wirelength variation (%) when the number of instances changed (%) to avoid the critical pin positions increases for the benchmark b13.



Source: from author (2015).

Figure A.6 shows the variation results for the benchmark s5378. Area is kept the same of the original results. The worst results are presented when 50% of the instances are avoiding the critical pin positions, where the period increases more than 6%, power increases about 7% and the wirelength increases about 2%. When 100% of the instances avoid the EM-unsafe pin positions, the period and power increase less than 1%, while the wirelength increases about 4%.

Figure A.6: Period, power, area and wirelength variation (%) when the number of instances changed (%) to avoid the critical pin positions increases for the benchmark s5378.

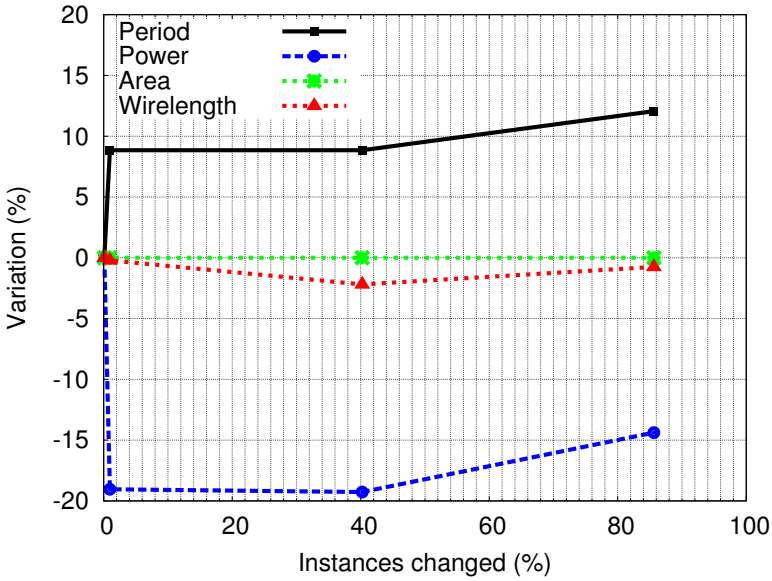


Source: from author (2015).

The variation results for the benchmark s9234 are shown in Figure A.7. Area is kept the same of the original results. The period could be reduced about 10%. Power increases

about 20% when a TTF of 10 years is considered and when about 50% of the instances are avoiding the critical pin positions. When about 100% of the instances avoid the EM-unsafe pin positions, the power increases about 15%. The wirelength increases less than 1%.

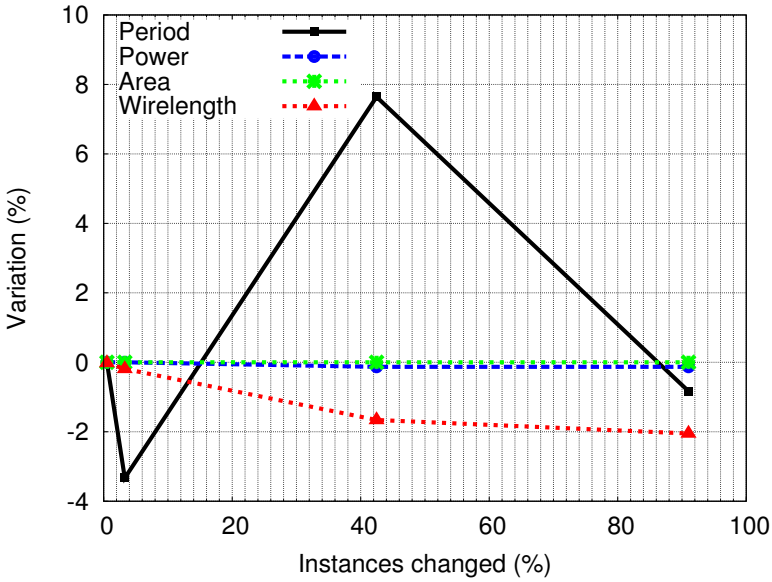
Figure A.7: Period, power, area and wirelength variation (%) when the number of instances changed (%) to avoid the critical pin positions increases for the benchmark s9234.



Source: from author (2015).

Figure A.8 shows the variation results for the benchmark s13207. Area and power are kept practically the same of the original results. The period is improved in almost 8% when 50% of the instances are avoiding the critical pin positions. For the other cases, it is slightly increased. The wirelength increases about 2% when more than 40% of the instances are changed.

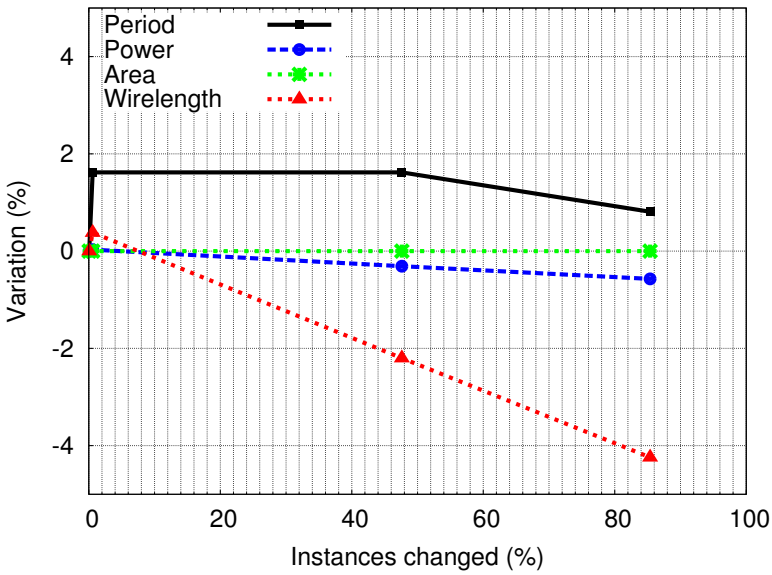
Figure A.8: Period, power, area and wirelength variation (%) when the number of instances changed (%) to avoid the critical pin positions increases for the benchmark s13207.



Source: from author (2015).

The variation results for the benchmark s38417 are shown in Figure A.9. Area is kept the same of the original results. The period could be reduced about 1.8%. Power increases less than 1%. And the wirelength increases about 2% when about 50% of the instances are avoiding the critical pin positions. When about 100% of the instances avoid the EM-unsafe pin positions, the wirelength increases about 4%.

Figure A.9: Period, power, area and wirelength variation (%) when the number of instances changed (%) to avoid the critical pin positions increases for the benchmark s38417.



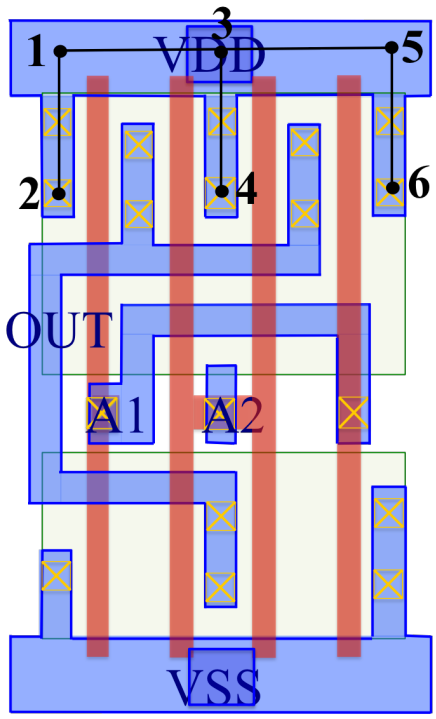
Source: from author (2015).

APPENDIX B COUPLING CAPACITANCE CURRENTS

The coupling capacitances are considered in our graph-based algorithm (Algorithm 4.1) that computes the currents through each edge when the pin position is moved from the reference case to another location. This Appendix is explaining why the coupling capacitances had to be included to compute accurately the currents using the Algorithm.

Figure B.1 shows the layout of the NAND2_X2 cell, where the Vdd and Vss pins are placed on the middle of these rails. This cell has two inputs, input A1 that are the second and third transistors and input A2, the first and fourth transistors.

Figure B.1: Layout of the NAND2_X2 cell.

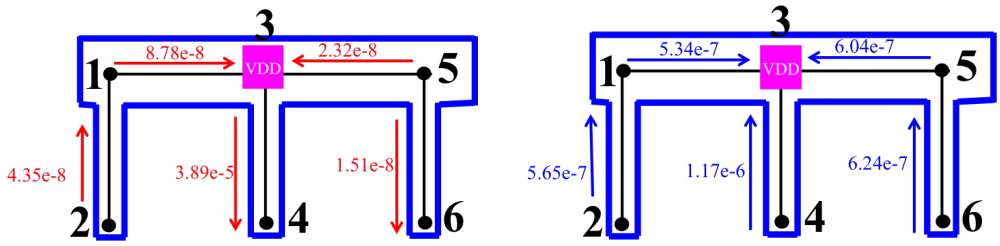


Source: from author (2015).

The average current direction and values in Ampere (A) through the wire segments of the Vdd rail, when the Vdd pin is at middle (node 3) are presented in Figure B.2. The red lines and values are the charge current values and the blue lines and values are the short circuit currents. This example is shown the critical input combination case, where more current is flowing through the edges (causing more EM), A1=0 and A2=1. In this way, the edge from node 3 to node 4 is charging the current through two transistors to the output. This is the critical wire segment when the pin is at middle (node 3).

Figure B.3 shows the average current values when the Vdd pin is placed at node 1. The arrows and values in grey represent the currents that are kept the same than when the pin is at node 3. Just the currents through the edge from node 1 to node 3 change. Based on the values from the reference pin position (node 3), the charge current through this edge is given by 3.89e-5 - 2.32e-8 = 3.888e-6 and the short circuit current is calculated by

Figure B.2: (a) Charge current (in A) and (b) short circuit current (in A) through the wire segments of the VDD rail when the Vdd pin is at middle (node 3) from SPICE simulation.

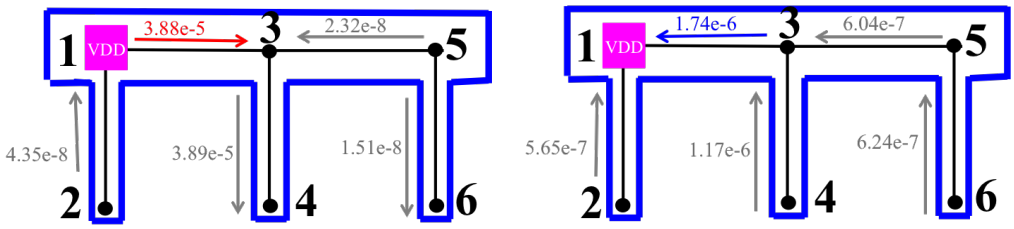


(a) (b)

Source: from author (2015).

6.04e-7 + 1.17e-6 = 1.77e-6, accordingly with the Algorithm 4.1. The calculated values are very similar of the values given by SPICE simulation. The same behavior is seen when the pin is placed at node 5.

Figure B.3: (a) Charge current (in A) and (b) short circuit current (in A) through the wire segments of the VDD rail when the Vdd pin is at left (node 1) from SPICE simulation.



(a) (b)

Source: from author (2015).

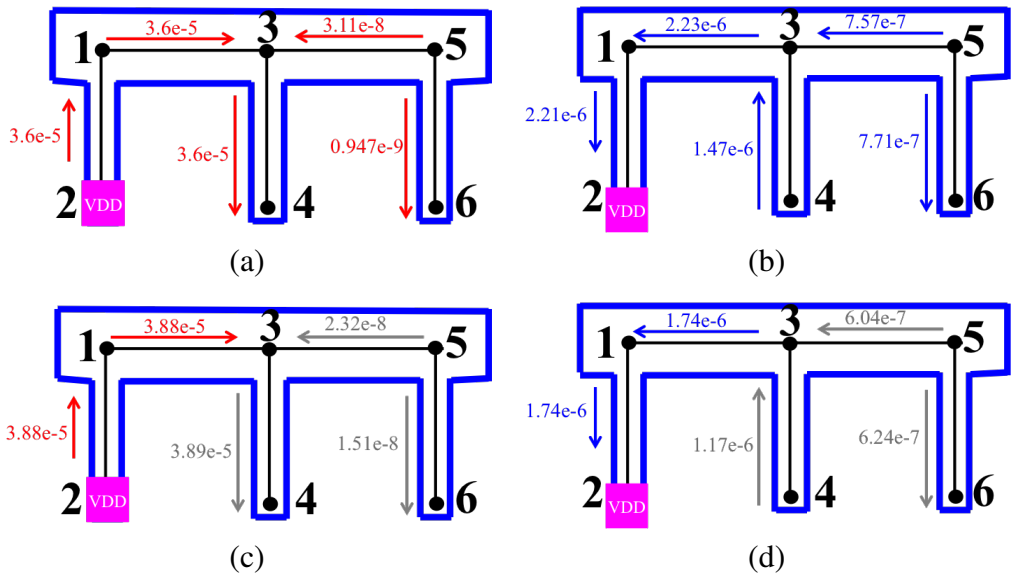
Figure B.4 shows the average current values when the Vdd pin is placed at node 2. Figures B.4(a) and (b) show the values from SPICE simulation and (c) and (d) are the currents calculated considering just the current values and directions from the reference pin position. The values from SPICE simulation are different of the values expected considering the reference pin position (node 3), represented by the arrows and values in grey, Figures B.4(c) and (d). For example, the currents through the edge from node 3 to node 4 should be 3.89e-5 and 1.17e-6 (instead of 3.6e-5 and 1.47e-6, respectively) accordingly with the values when the pin is at node 3.

For the NAND2_X2 cell, the algorithm just considering the charge and short circuit current works well when the pin is at node 1, 3 and 5, but do not work well when the pin is at the fingers, nodes 2, 4 and 6. To find why this difference in the values appears for the NAND2_X2 cell, because for other cells like INV and BUF this difference does not happen, we looked through the layout extracted parasitics and we found some coupling capacitances between the VDD and the OUT wires that are producing this difference in the results.

Considering that the coupling capacitance currents are the same for almost all nets since moving the pin does not significantly change the transient waveforms in these nets. Thus, to consider the case of the NAND2_X2 cell, the change is simple: for the reference case, the currents through the wires as well as through the coupling capacitances would be measured. In this way, the charge/discharge, short-circuit/leakage and coupling capac-

itance currents for each edge are determined from the simulation to improve the accuracy of our algorithm.

Figure B.4: (a) (c) Charge current and (b) (d) short circuit current through the wire segments of the VDD rail when the Vdd pin is at node 2. (a) and (b) values are from SPICE simulation and (c) and (d) are calculated just considering the currents and directions.



Source: from author (2015).