UNIVERSIDADE FEDERAL DO RIO GRANDE DO SUL
INSTITUTO DE INFORMÁTICA
PROGRAMA DE PÓS-GRADUAÇÃO EM MICROELETRÔNICA

MATEUS BERNARDINO MOREIRA

Low Power Digitally Controlled Oscillator for IoT Applications

Thesis presented in partial fulfillment
of the requirements for the degree of
Master of Microelectronics

Advisor: Prof. Dr. Sergio Bampi
Coadvisor: Dr. Filipe Dias Baumgratz

Porto Alegre
June 2021

CIP — CATALOGING-IN-PUBLICATION

MOREIRA, MATEUS BERNARDINO

Low Power Digitally Controlled Oscillator for IoT Applications / MATEUS BERNARDINO MOREIRA. – Porto Alegre: PGMICRO da UFRGS, 2021.

84 f.: il.

Thesis (Master) – Universidade Federal do Rio Grande do Sul. Programa de Pós-Graduação em Microeletrônica, Porto Alegre, BR–RS, 2021. Advisor: Sergio Bampi; Coadvisor: Filipe Dias Baumgratz.

1. Low-power design, low-voltage, digitally controlled oscillator (DCO),transformed-based oscillator, Unified Current-Control Model (UICM), Internet-of-Things. I. Bampi, Sergio. II. Baumgratz, Filipe Dias. III. Título.

In memory of
Adelaide Fantinel Bernardino

AGRADECIMENTOS

Primeiramente gostaria de agradecer a Deus por tudo. Por toda a provisão, por me sustentar todos os dias da minha vida e por me proporcionar a conclusão do meu mestrado.

À minha esposa, Mariane, por sempre me apoiar, me incentivar e estar sempre ao meu lado nos momentos difíceis. Seu apoio fez toda a diferença durante todas as etapas dessa conquista.

Aos meus pais, Altamir e Eronita, por todo o suporte durante esta trajetória e durante a vida. Por sempre me motivarem a seguir em frente e correr atrás dos meus objetivos. Por todo auxílio e orações sempre.

Ao meu irmão, Cristiano, minha cunhada Suéllen, por me encorajarem sempre da melhor forma e fazerem sempre parte das minhas conquistas.

Aos meu sogros Nazáre e João, bem como meus cunhados, por todas as orações, incentivos e compreensão ao longo desse percurso.

À minhas aVós Maria, Lica e Antônia, que me servem como exemplos de motivação e força, por todo apoio e orações sempre.

Ao meu orientador Professor Dr. Sergio Bampi e ao meu co-orientador Dr. Filipe Dias Baumgratz por terem me fornecido esta oportunidade, pela orientação e, conhecimentos compartilhados que me guiaram a esta conquista. Ao Professor Sandro Binsfeld da UNISINOS por todo auxílio e discussòes técnicas que me ajudaram muito durante meu mestrado.

Aos meus colegas dos Laboratórios 110, 217 e 215 da UFRGS, pela amizade, ajuda e momentos de descontração que contribuíram para essa tragetória tornando-a mais leve. Ao meus antigos colegas da extinta FLORIPA-DH, Roddy, Alberto e Juan pela amizade e conhecimentos partilhados ao longo deste caminho.

À CAPES e à FAPERGS pelo auxílio financeiro que possibilitaram a execussão do meu mestrado.

ABSTRACT

This work is focused on the design of a Low Power CMOS DCO for IEEE 802.11ah in IoT applications. The design methodology is based on the Unified current-control model (UICM), which is a physics-based model and enables an accurate all-region model of the operation of the device. Additionally, a transformer-based resonator has been used to solve the low-quality factor issue of integrated inductors. Two digitally controlled oscillators (DCO) have been implemented to show the advantages of utilizing a transformed-based resonator and the methodology based on the UICM model. These designs aim for the operation in low voltage supply (VDD) since VDD scaling is a trend in systems-on-chip (SoCs), in which the circuitry is mostly digital. Despite the degradation caused by VDD scaling, new RF and analog circuits must deliver similar performance of the older CMOS nodes. The first DCO design was a low power LC-tank DCO, implemented in 40nm bulk-CMOS. The first design presented a DCO operating at 45% of the nominal VDD without compromise the performance. By reducing the VDD below the nominal value, this DCO reduces power consumption, which is a crucial feature for IoT circuits. The main contribution of this first DCO is the reduction of VDD scaling impact on the phase-noise do the DCO. The LC-based DCO operates from 1.8 to 1.86 GHz. At the maximum frequency and 0.395 V VDD, the power consumption is a mere 380 μW with a phase-noise of -119.3 dBc/Hz at 1 MHz. The circuit occupies an area of 0.46 mm^2 in 40 nm CMOS, mostly due to the inductor. The second DCO design was a low-power transformer-based DCO design, implemented in 28nm bulk-CMOS. This second design aims for the VDD reduction to below 0.3 V. Operating in a frequency range similar to the LC-based DCO, the transformer-based DCO operated with 0.280 V VDD with a power consumption of 97 μW. Meanwhile, the phase-noise was -101.95 dBc/Hz at 1 MHz. Even in the worst-case scenario (i.e., slow-slow and 85^{o}C), this second DCO was able to operate at 0.330 V VDD, consuming 126 μW, while it keeps a similar phase-noise performance of the typical case. The core circuit occupies an area of 0.364 mm^2.

Keywords: Low-power design, low-voltage, digitally controlled oscillator (DCO),transformed-based oscillator, Unified Current-Control Model (UICM), Internet-of-Things.

RESUMO

Este trabalho objetiva o projeto de um DCO de baixa potência em CMOS para aplicações de IoT e aderentes ao padrão IEEE 802.11ah. A metodologia de projeto é baseada no modelo de controle de corrente unificado (UICM), que é um modelo com embasamento físico que permite uma operação precisa em todas as regiões de operação do dispositivo. Adicionalmente, é utilizado um ressonador baseado em transformador visando solucionar os problemas provenientes do baixo fator de qualidade de indutores integrados. Para destacar as melhorias obtidas com o projeto do ressonador baseado em transformador e com a metodologia baseada no modelo UICM, dois projetos de DCO são realizados. Esses projetos visam a operação com baixa tensão de alimentação (VDD), uma vez que o escalonamento do VDD é uma tendência em sistemas em chip (SoCs), em que o circuito é majoritariamente digital. Independente da degradação causada pelo escalonamento de VDD, circuitos analógicos e de RF atuais devem oferecer desempenho semelhante ao alcançado em tecnologias CMOS mais antigas. O primeiro projeto foi um DCO de baixa potência com tanque LC, implementado em tecnologia bulk-CMOS de 40nm. O primeiro projeto apresentou uma operação a 45% do VDD nominal sem comprometer o desempenho. Ao reduzir o VDD abaixo do valor nominal, este DCO reduz o consumo de energia, que é uma característica crucial para circuitos IoT. A principal contribuição deste DCO é a redução do impacto do escalonamento do VDD no ruído de fase. O DCO com tanque LC opera de 1,8 a 1,86 GHz. Na frequência máxima e com VDD de apenas 0,395 V, o consumo de energia é 380 μW e o ruído de fase é -119,3 dBc/Hz a 1 MHz. O circuito ocupa uma área de 0.46 mm^2 em processo CMOS de 40 nm. O segundo projeto foi um DCO de baixa potência baseado em transformador, implementado em tecnologia bulk-CMOS de 28nm. Este projeto visa a redução de VDD abaixo de 0,3 V. Operando em uma faixa de frequência semelhante ao primeiro DCO, o DCO baseado em transformador opera com VDD de 0,280 V e com consumo de potência de 97 μW. O ruído de fase foi de -101,95 dBc/Hz a 1 MHz. Mesmo no pior caso de processo, este DCO opera a um VDD de 0,330 V, consumindo 126 μW, com o ruído de fase semelhante ao caso típico. O circuito ocupa uma área de 0.364 mm^2.

Palavras-chave: Projeto de baixa potência, baixa tensão, oscilador digitalmente controlado (DCO),oscilador baseado em transformador, internet das coisas.

LIST OF ABBREVIATIONS AND ACRONYMS

IoT	Internet of Things
WiFi	Wireless Network based on IEEE 802.11 standard
BLE	Bluetooth Low Energy
NFC	Near Field Communication
RFID	Radio-Frequency Identification
LNA	Low Noise Amplifier
PLL	Phase Locked Loop
ADPLL	All Digital Phase Locked Loop
PDKs	Process Design Kits
TSMC	Taiwan Semi-Conductors
WPAN	Wireless Personal Area Network
VCO	Voltage Controlled Oscillator
DCO	Digitally Controlled Oscillator
TDC	Time to Digital Converter
DLF	Digital Loop Filter
FREF	Reference Frequency
FCLK	Output Variable Clock
DTC	Digital to time Converter
PHR_F	Fractional part of the reference Phase
PHR	Reference Phase
FCW	Frequency Command Word
CKR	Re-time Reference Rate
OTW	Oscillator Tuning Word
WI	Weak Inversion

MI	Moderate Inversion
SI	Strong Inversion
PN	Phase Noise
FOM	Figure Of Merit
PFN	Power-Frequency-Normalized
PGR	Patterned Ground Shield
DRC	Design Rule Check
UICM	Unified Current-Control Model
SNR	Signal to Noise Ratio
ACR	Adjacent Channel Rejection

LIST OF SYMBOLS

ω_0	central frequency in radians
Q_p	Primary Quality Factor
Q_s	Secondary Quality Factor
I_D	Drain Current of Transistor
I_s	Specific Current of Transistor
i_f	Inversion Level
n	Slope Factor
n_L	Inductance Ratio
V_{T0}	Equilibrium Threshold Voltage
gm_g	Gate transconductance
GM	Large Signal Transconductance
k_m	Coupling Factor
R_p	Inductor Parallel Resistance
R_s	Inductor Series Resistance
ϕ_t	Thermal Voltage
I_{tail}	Tail Transistor current
K_B	Boltzmann Constant
T	Temperature Coefficient
P_{DC}	DC Power
f_0	Central Frequency
C_{wi}	Inter-winding capacitance
C_{ox}	Oxide Capacitance
R_{si}	Substrate resistance
L_P	Primary Inductance

L_S	Secondary Inductance
V_G	Gate Voltage
V_P	Pinch-Off Voltage
I_{SH}	Sheet Normalization Current
V_{FB}	Flat Band Voltage
ϕ_F	Fermi Potential
i_{fmax}	Maximum inversion Level
V_{dsat}	Drain to Source Saturation Voltage
V_{dstail}	Drain to Source Saturation Voltage of tail transistor

LIST OF FIGURES

LIST OF TABLES

CONTENTS

1 INTRODUCTION

1.1 Motivation

The growth of devices connected to the internet with the passing of years increases the interest in the study and development of electronic devices for the IoT (*Internet of Things*). The concept of the IoT is defined by a network composed by smart devices that can exchange information with similar ones through wireless channels, without any human interaction.(SRINIVASAN; ARUMUGAM, 2016). The objects that compose the IoT network can be sensors, *Radio-Frequency Identification* (RFID) tags, actuators, mobile cell phone and others. Furthermore, there are several different protocols which connect these devices as *Wireless Network based on IEEE 802.11 Standard* (WiFi), Bluetooth, *Bluetooth Low Energy* (BLE), *Near Field Communication* (NFC), Zigbee, RFID protocols and a mobile phone network. (MASI, 2018).

The WiFi, which is defined as the IEEE 802.11 standard, was created to perform a wireless connection between computers. The WiFI was created for short range communications, which fall in a range of up to 100 meters. The Bluetooth standard was created for providing communication between devices on the range of a few meters. This standard of communication was intended to substitute the transfer cables in consumer electronics. The WiFi standard and the Bluetooth do not support a lot of devices connected at the same time in the same network with low data rates and low power consumption, as the IoT applications require(FERRO; POTORT, 2005)(PAALA et al., 2019).

The Zigbee standard is suitable for applications that require low data transmission rates, low power consumption, and a lot of devices connected to the same network. These features make this protocol suitable for IoT applications. This protocol emerged as an alternative to the WiFi and the Bluetooth standards to reduce the front-end power consumption. This standard reduces power consumption keeping, however, the same range of the WiFI(ELARABI; DEEP; RAI, 2015).

The RFID protocol uses two main devices to perform the communication: the TAG and the reader. The TAG is the device which contains the information that will be read wirelessly. The reader can also modify the information coming from the TAG. The RFID protocol permits a very low power communication due to the possibility of the implementation of passive TAGs. The limitation of this protocol is that the communication range is on average 7 meters or much less (below one meter)(SAFKHANI et al., 2012).

The NFC standard, as the name suggests, is applied in very short communications range. This standard was created by NXP together with Nokia and Sony. This standard makes possible communications by means of a device that reads from and writes information to a card. In this mode of operation the device acts as a reader. Furthermore, the most popular use of this protocol is the data transfer between two handsets by coil tapping. In addition, there is a third mode that emulates a card which will have its information read by an external reader (CHENG et al., 2009).

The most widespread standard for short-range IoT communication in low-cost consumer electronics is the BLE. It is capable of fulfilling the low power requirements of IoT(KUO et al., 2017). This standard is defined as *wireless personal area network* (WPAN) and achieves a communication range of 100 meters(BERTULETTI et al., 2016). The WiFi-HaLow standard (IEEE 802.11ah) can increase considerably the communication range, up to 1 km. The sub-GHz frequency of operation makes possible a low power consumption with a low data rate. This characteristic, added to the longer distance range, makes WiFi-HaLow a competitive solution for wireless sensor networks, IoT applications, and overall applications which demand lots of devices connected and very low power consumption in each device(ANDRADE et al., 2017).

The number of connected IoT devices is estimated to double in five years, and has reached about 24 billion connections in 2020. Although there has been a considerable growth in the number of connections over the years, the IoT applications are just beginning to scale up. (GSM Association, 2020). Furthermore, there are estimates that the market of IoT sensors will reach an mark of 27 billion US dollars by 2021(FORBES, 2020)(CHERNYSHEV et al., 2017). These data corroborates the first predictions of the increase in the number of connections by IoT devices in the next years.

To improve the efficiency of the IoT network, the design of Ultra-Low Power Transceivers becomes necessary to enhance the battery lifetime of autonomous or semi-autonomous nodes. Furthermore, when lots of devices are connected to the IoT network, the battery replacement of each one becomes highly impractical or undesired(LEE et al., 2018).

In the RF transceiver front-end, the 3 most power-hungry blocks are: the *Low Noise Amplifier* (LNA) in the receiver, oscillator in the *Phase Locked Loop* (PLL) or *All Digital Phase Locked Loop* (ADPLL), and the power amplifier in the transmitter. In particular, reducing the power consumption of the oscillator is a considerable challenge since the power level impacts directly the phase-noise performance (YU et al., 2017)(KANG;

WENG; LIU, 2009).

1.2 Goals

This Master´s thesis is focused on the Design of a Low Power DCO for the WiFi-Halow Standard (IEEE 802.11ah) which enables low power consumption and long-range transmission due to the center frequency of operation below 1 GHz (BA et al., 2018). Furthermore, these features make this standard suitable to IoT and therefore to this work (ANDRADE et al., 2017), which is focused in the low power applications. The Wi-Fi Halow standard has different frequency bands for each country: 863-868 MHz in Europe, 902–928 MHz in the USA and Brazil, and 916.5–927.5 MHz in Japan. The most common channel bandwidths adopted in 802.11.ah (Wi-Fi Halow) are 1 MHz and 2 MHz(ADAME et al., 2014).

The goal of this work is to achieve results comparable with the state of art in controlled oscillators, in terms of power consumption without compromising the phase noise performance required for the given wireless standard. The weak inversion operation of the transistors in the DCO and the transformed-based resonator are two relevant techniques to be explored in this thesis. Both approaches are not new in the literature. However, they remain excellent design options for low power oscillation design(LEE; MOHAMMADI, 2007a)(GHORBEL et al., 2018)(BABAIE; SHAHMOHAMMADI; STASZEWSKI, 2015a). In this work the operational frequency is 1.8 GHz, twice the WiFi HaLow standard. The *Process Design Kits* (PDKs) used to Design the DCOs in this Master´s thesis are the 40nm and 28nm both from *Taiwan Semiconductor Manufacturing Company* (TSMC).

1.3 M.Sc. Thesis Organization

Aiming to cover all basics related to the DCO, chapter 2 of this Master´s thesis addresses an introduction to PLLs and to frequency synthesizers. The main characteristics, the most popular topologies of cross-coupled oscillators, and an introduction to the phase-noise are also presented in this chapter. The principle of transformer loading in the context of DCO is covered in chapter 3. In chapter 4 the I-V transistor model used for analytical modelling of device operation is reviewed, as it provides basic design equa-

tions. Furthermore, the transistor threshold voltage extraction method used here is also derived in chapter 4. Aiming to arrive at the best compromise in the topology of the low power oscillator, in chapter 5 two DCO designs are developed and compared: one with only inductor-based resonator and another with transformer-based resonator. Finally in chapter 6 the conclusions and future works proposed are presented.

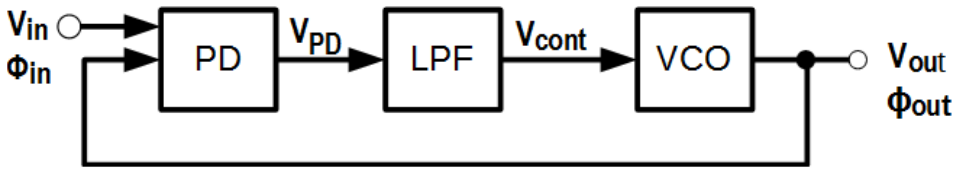
2 DIGITALLY CONTROLLED OSCILLATOR

2.1 Introduction to Low-Power Frequency Synthesizers

Frequency synthesizers are defined as circuits that generate a single or multiple frequencies from a reference one(RADER; GOLD, 1971). The most common example of synthesizer is the *phase-locked loop* (PLL). The PLL is largely used to generate a reference frequency inside the integrated transceivers. The main objective of this block is to obtain a precise reference frequency and phase to be delivered to the system, with a low phase-noise.

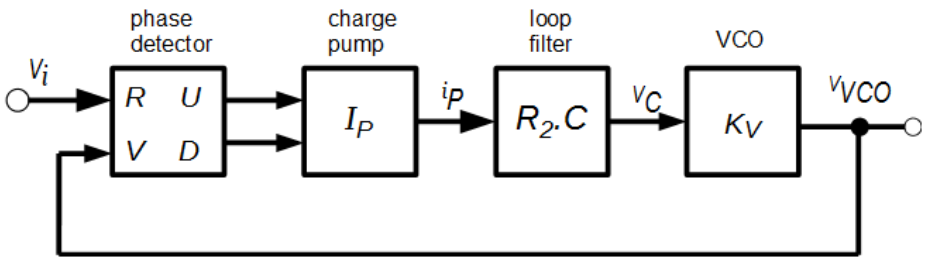
The main topology of this block (Figure 2.1) is composed by: a phase-detector, a low-pass filter, a voltage controlled oscillator and a negative feedback loop. The phase detector compares the phase of the incoming and more stable (with regards to temperature, voltage, and process variations) signal from from the reference input signal with the output frequency from VCO. The phase detector generates a DC voltage signal with high-frequency components which are filtered by the low pass filter. The resulting low frequency voltage signal (Vcont) controls the frequency of the oscillator.

Figure 2.1: PLL classical topology.



Source:Adapted from (RAZAVI, 1998)

Figure 2.2: Charge-Pump PLL.



Source:Adapted from (LU; LIU; LI, 2014)

The Charge-Pump based PLL is another basic architecture of the PLL which is described by improvement in the static phase error and the capture range of the PLL. In

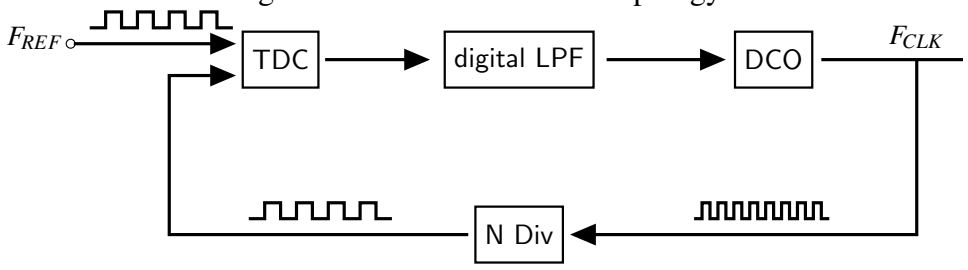
this topology, the low pass filter from the basic topology is replaced by the loop filter, and the charge pump is added after the phase detector to convert the digital signal into current. The loop filter acts as a current-to-voltage conversion to process the signal that comes from the charge-pump. Figure 2.2 shows the conceptual architecture of the Charge-Pump Based PLL(LU; LIU; LI, 2014)(RAZAVI, 1998).

2.2 All-Digital PLL (ADPLL)

The high scalability of the CMOS processes from generation to generation, which allows by the dimensional scaling the reduction of power consumption and an increase in the number of transistors on the same chip, makes the digital approach a good choice instead of analog ones for certain range of functions. The all-Digital phase-locked loop arises from this concept. Furthermore, the digital design methodology and robustness for developing this block solves some problems posed by the more traditional analog PLLs. The ADPLL consumes less area, as it does not require the large analog filters necessary in the conventional PLL. Hence, all circuit is on-chip, which differs from the analog charge-pump PLL that usually needs off-chip resistors and capacitors to implement the loop-filter, aiming to achieve low PLL bandwidth (FERREIRA et al., 2019) (JANG; JEONG; JEON, 2018).

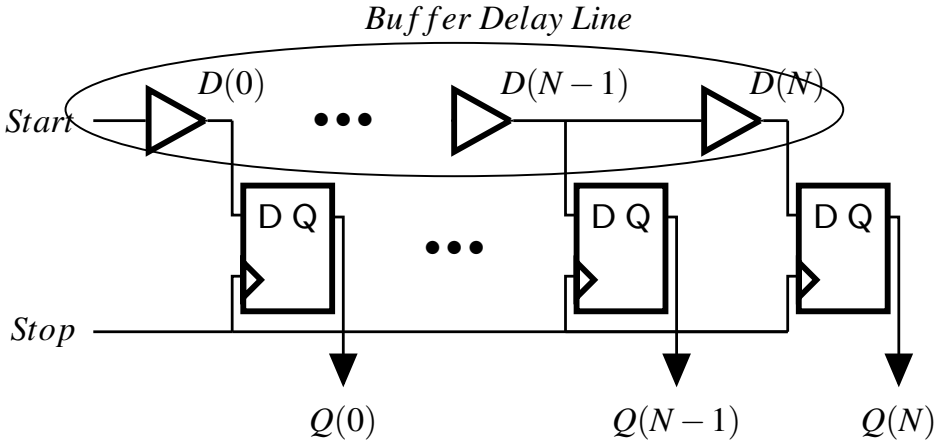
Figure 2.3 presents the most common ADPLL topology composed by: a Time-to-Digital Converter (TDC) which detects the phase error between *Output Variable Clock*(FCLK) and the Reference Frequency (FREF) clock, a Digital Loop Filter (DLF) that locks DCO in frequency and phase, and a Digitally-Controlled Oscillator (DCO) which generates the output variable frequency clock FCLK. In addition, after the oscillator, a frequency divider, which transforms the analog output of DCO into a digital one is placed. The most common DCO topology is an LC-based oscillator, since it introduces less phase-noise than other topologies like the ring oscillators.

Figure 2.3: ADPLL classical topology.



Source:Author

Figure 2.4: Flash TDC Architecture.



Source:Author

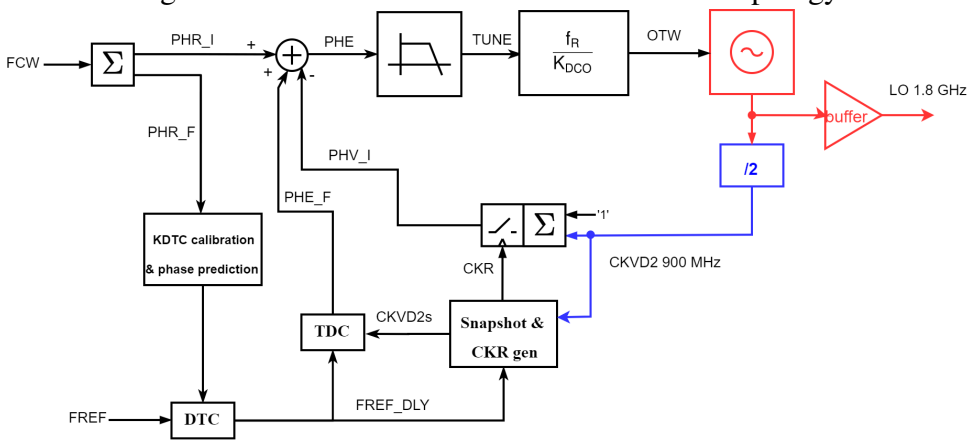
The most common architecture of the TDC is based on Delay line elements. The Flash TDC architecture is presented by Figure 2.4. The start and stop signals of flash TDC are the (FCLK) and (FREF) respectively. The variable reference clock signal coming from the oscillator is delayed in the delay chain. The stop signal controls the clock of the sampling flip-flops. The measure of a time interval is indicated by the start and stop signals. When the signal coming from the oscillator pass through the delay element, the corresponding sampling flip-flop set its output to high. Hence, when the clock signal has still not reached through the rightmost delay elements, the corresponding memory elements remain with their outputs low. The digital thermometer scale is decoded into a binary word, hence the conversion of the time-interval duration to a digital word (a TDC). The resolution period is defined as the unit delay in an element in the delay line (FERREIRA et al., 2019).

The ADPLL topology which can reduce the power consumption considerably while also decreasing the spurs levels of the ADPLL is the DTC counter-based ADPLL topology presented in the Figure 2.5. The digital to time converter (DTC) acts as a delay line, which is in charge of delay the reference clock with the information coming from the fractional part of the reference phase (PHR_F)(CHEN et al., 2015). This architecture is based on the phase prediction method described in (ZHUANG; STASZEWSKI, 2012), which is composed of an accumulator, a DTC, and a TDC. The frequency control work (FCW) is accumulated and creates the fractional and integer parts of the reference phase (PHR). In addition, it makes part of the phase-detection the snapshot, the re-time reference rate (CKR), and the variable frequency accumulator.

The frequency command word (FCW) is the rate of the output frequency coming

from the oscillator by the reference frequency FREF. In this topology, the bits requirements of TDC can be reduced due to the presence of the DTC. The DTC delays the reference signal by the control of the fractional part of the reference phase (PHR_F). Hence, the signal that comes from the DTC is almost in phase with the signal coming from the snapshot, which results in a decrease in the required bits of the TDC block. This reduction on the TDC bits saves power and also contributes to decrease the magnitude of spurs. The DTC can consume less power with the same number of bits of the TDC. The DTC dominates the spurs level in the DTC-based architecture. However, the spurs problem stemming from the DTC can be solved with the gain calibration technique.

Figure 2.5: DTC-TDC counter-based ADPLL topology.



Source: The Author

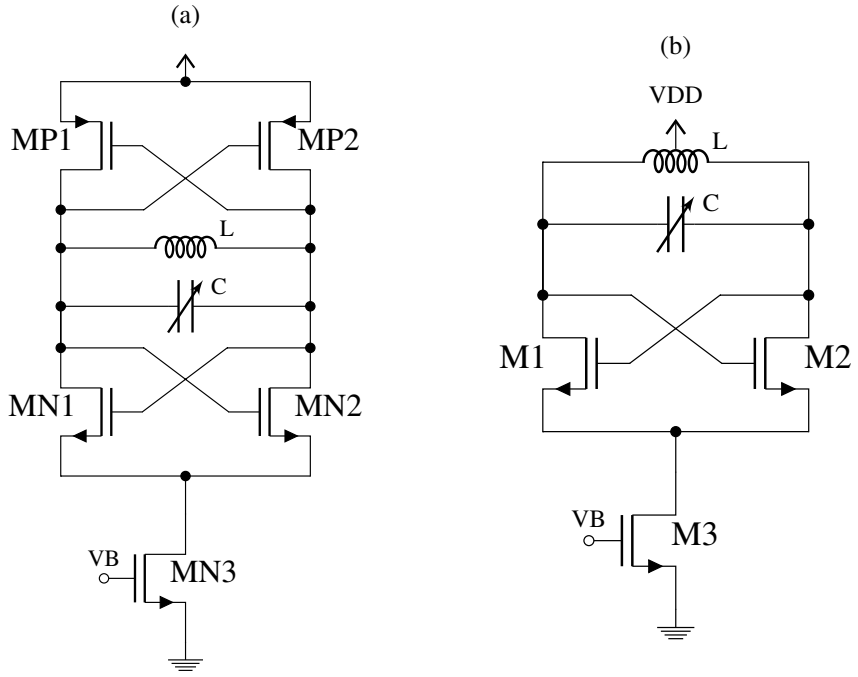
2.3 Introduction to Digitally Controlled Oscillator(DCO)

The main LC-oscillator topologies presented in the literature are shown in Figure 2.6. They are the NMOS-only topology and the complementary push-pull. On one hand, the first is more suitable for supply voltage scaling. On the other hand, the second one takes advantage of the so-called current reuse to save power. In addition, the complementary push-pull topology suffers from higher capacitance from routing due to the additional PMOS cross-couple pair. Hence, the extra transconductance source becomes a problem in a weak inversion operation. For the ultra low power operation, the NMOS-only is also more suitable due to the larger transistor sizing requirements. The tuning range from complementary push-pull also results less in this application.

The main differences between a voltage controlled oscillator and a digitally controlled one are addressed to the frequency control method. The first receives a voltage

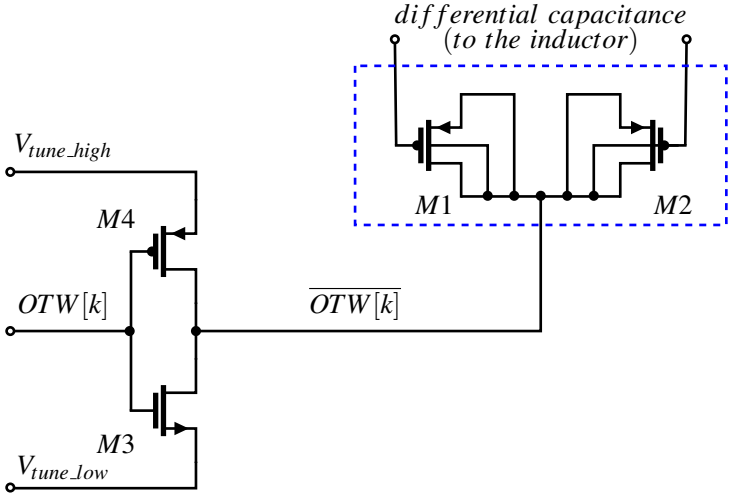
stimulus to set the oscillation frequency. The second delivers the output voltage with the frequency set by the Oscillator Tune Word (OTW) that is provided at the output of a digital filter. The Digitally-Controlled Oscillator (DCO) represents the heart of the ADPLL, which is in charge of delivering the desired variable frequency.

Figure 2.6: (a) Complementary push-pull LC oscillator. (b) NMOS-only LC oscillator.



Source:Author

Figure 2.7: Schematic of binary switchable capacitance.



Source:Adapted from (STASZEWSKI et al., 2003)

The binary switchable capacitance method to control the DCO frequency is shown on Figure 2.7. The cell comprises two PMOS transistors connected in a differential varactor configuration. Hence, the voltages $V_{tunehigh}$ and $V_{tunelow}$ set the unit cell to the high

or low-capacitance mode. The capacitor bank is formed by different number of these unit cells. Each bit of the OTW sets one of these cells to the required capacitance mode.

The quality factor of the resonator limits the maximum number of bits. The increase in the number of bits results in a decrease in the quality factor of the resonator. Furthermore, the number of bits also limits the tuning range due to the added resultant capacitance from routing. The number of bits also sets the resolution of the DCO. Therefore, there is a trade-off between the tuning range of the DCO and the maximum resolution that can be achieved. The resolution must be equal or less than the channel bandwidth to avoid locking problems into ADPLL.

The binary switchable capacitance becomes a solution to the highly non linear capacitance versus control voltage behavior of the CMOS varactors. This problem is increased in the deep-submicron CMOS process, which reduces considerably the linear range of the varactors. This results in the considerable increase in the gain of oscillator, which results in more sensitivity to noise and process variations. Figure 2.8 shows the behavior of the varactors in a conventional and in a deep-submicron CMOS process. The oscillation gain is derived from the following equation:

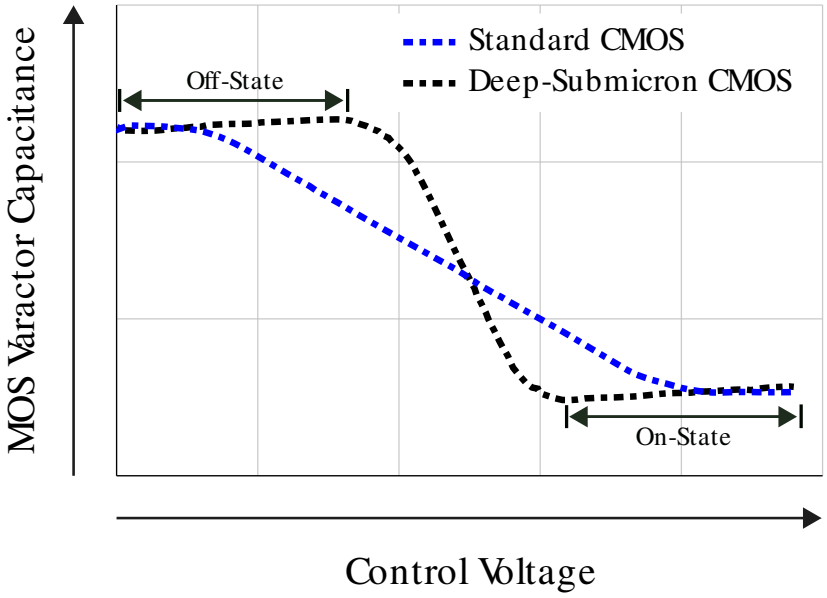
$$K_{VCO} = \Delta_f / \Delta_V \tag{2.1}$$

The binary switchable capacitance method then reduces the impact of the noise and the process variations due to the operation on the two modes only to each bit. This makes this method less prone to process variation as the circuit is not required to work in the linear region of the curve. In the linear region of the curve any threshold variation due to process will result in a considerable change in the oscillator frequency of operation (STASZEWSKI et al., 2003).

2.4 Tank Losses

The LC-Oscillators described earlier has the negative resistance as the principle of oscillation. A LC-tank, when excited by a pulse of current, starts to oscillate with a frequency of the periodic signal equal to resonance frequency of resonator. In an ideal case, which the tank do not have losses, the oscillation remains stable. However, in the real scenario, when the tank resonates, remains the resistance which represents the losses of the resonator. Hence, the signal is dissipated in the resistor and the oscillation die.

Figure 2.8: Capacitance vs Voltage Curve of MOS Varactor.

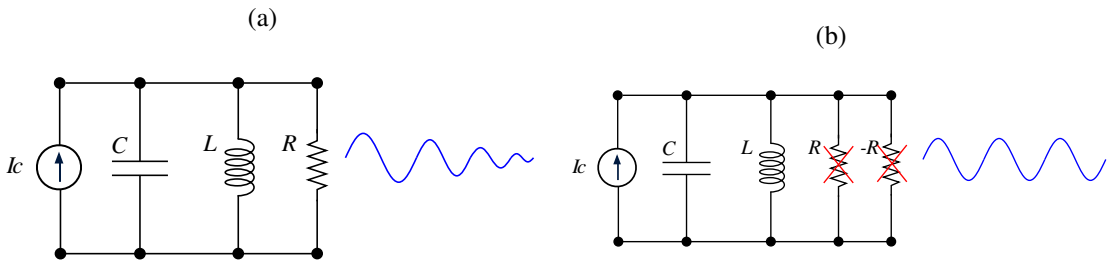


Source:Adapted from (STASZEWSKI et al., 2003)

Figure 2.9(a) represents this phenomena.

To avoid this problem and sustain the oscillation, the losses must be cancelled. The solution to this issue is to provide a negative resistance, which cancels the resultant resistance at resonance as Figure 2.9(b) shows(RAZAVI, 1998). The most common circuit configuration which provides a negative resistance is the cross-coupled pair. In the case of complementary push-pull topology, the NMOS pair provides one and the PMOS pair provide the second one. Hence, the negative resistances are added to cancel the resistance of the tank.

Figure 2.9: (a) Resonant tank circuit response to a current impulse without negative resistance. (b) Resonance tank circuit response to a current impulse with negative resistance.



Source:Adapted from (RAZAVI, 1998)

In the LC-based oscillator, the losses of the resonator are dominated by parallel

resistance of the inductor (R_p) given by:

$$R_p \approx L^2\omega_0^2/R_s \tag{2.2}$$

where R_s is the series resistance, L is the inductance and ω_0 is the DCO frequency of operation. This equation shows that by increasing the size of the inductor the parallel resistance will also increase. However, this assumption is limited by the self-resonance frequency of the inductor which limits the maximum size of the inductive element by required frequency of operation. In addition, the quality factor of the coil also decreases by the increases of the its series resistance. When the coil increases the series resistance also increases resulting in a decrease in the quality factor of the inductor. Equation 2.2 shows the impact of the quality factor represented by R_s. To solve this problem related to the size of the inductor, the most useful strategy is to improve the quality factor (Q) of the device. The power consumption of the classical LC oscillator is inversely proportional to the quality factor of the inductor. Integrated oscillators on bulk silicon CMOS processes suffer from low quality factors. The quality factor of the inductor, which represents an efficiency parameter, is derived as:

$$Q = L\omega_0/R_s \tag{2.3}$$

To maximize the quality factor of inductor we need to reduce its series resistance (R_s). In addition, increasing the operating frequency of the system also helps to improve the quality, up to a certain frequency range (RAZAVI, 1997).

2.5 Start-up and Steady-State Conditions

The oscillator starts when the transconductance (gm_g) of the transistors in the cross-coupled pair is larger than tank losses, which are represented by the parallel resistance of the inductor R_p. This condition is defined as

$$gm_g \geqslant \frac{2}{R_p}. \tag{2.4}$$

After the oscillator starts, the voltage across the tank increases and the oscillator starts to function as a large signal block. Furthermore, the cross-coupled pair works as a current source. In this regime, the small-signal transconductance of the transistor which is derived

from 2.5 is no longer useful. The transconductance from the cross-coupled pair must be replaced and represented by equation 2.6(TOUMAZOU; MOSCHYTZ; GILBERT, 2004):

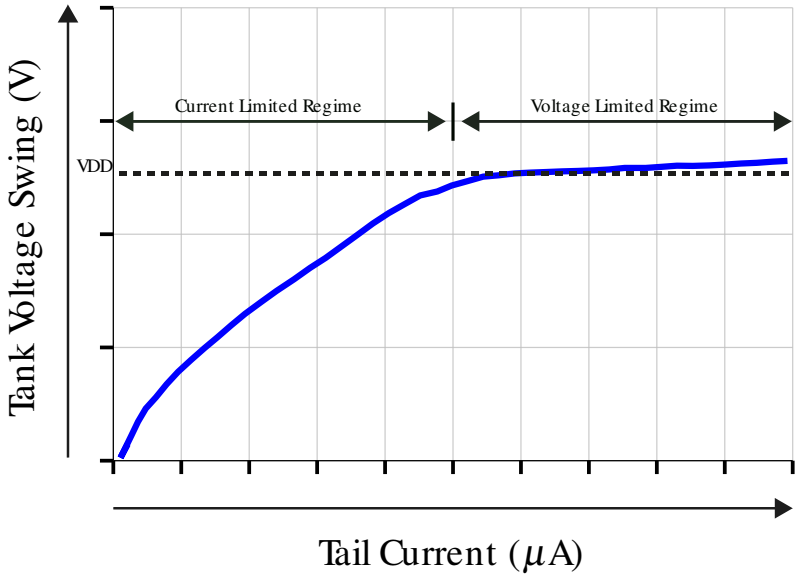
$$gm_g = \frac{2I_S}{n\phi_t}(\sqrt{1+i_f} - 1) \approx \frac{I_D}{n\phi_t} \tag{2.5}$$

$$GM = \frac{2I_D}{V_{tank}} \tag{2.6}$$

Equation 2.6 shows that the large signal transconductance decreases with an increased voltage amplitude across the tank. Therefore, the start-up condition is not capable of keeping the oscillation causing it not to be sustained. The oscillator operates either in a current-limited regime or in a voltage-limited regime. During the current-limited operation, the voltage amplitude is given by

$$V_{tank} = I_{tail}R_p \tag{2.7}$$

Figure 2.10: Tail Current versus Tank Amplitude Voltage



Source:Adapted from (TOUMAZOU; MOSCHYTZ; GILBERT, 2004; HAJIMIRI; LEE, 1999)

where I_{tail} is the tail current and R_p is the tank parallel resistance. Meanwhile, during the voltage-limited operation, the voltage amplitude across the tank is approximately equal to VDD (TOUMAZOU; MOSCHYTZ; GILBERT, 2004; HAJIMIRI; LEE, 1999). Figure 2.10 shows the behavior of the voltage amplitude across the tank in these two regimes. Assuming that the maximum voltage across the tank is VDD and its value

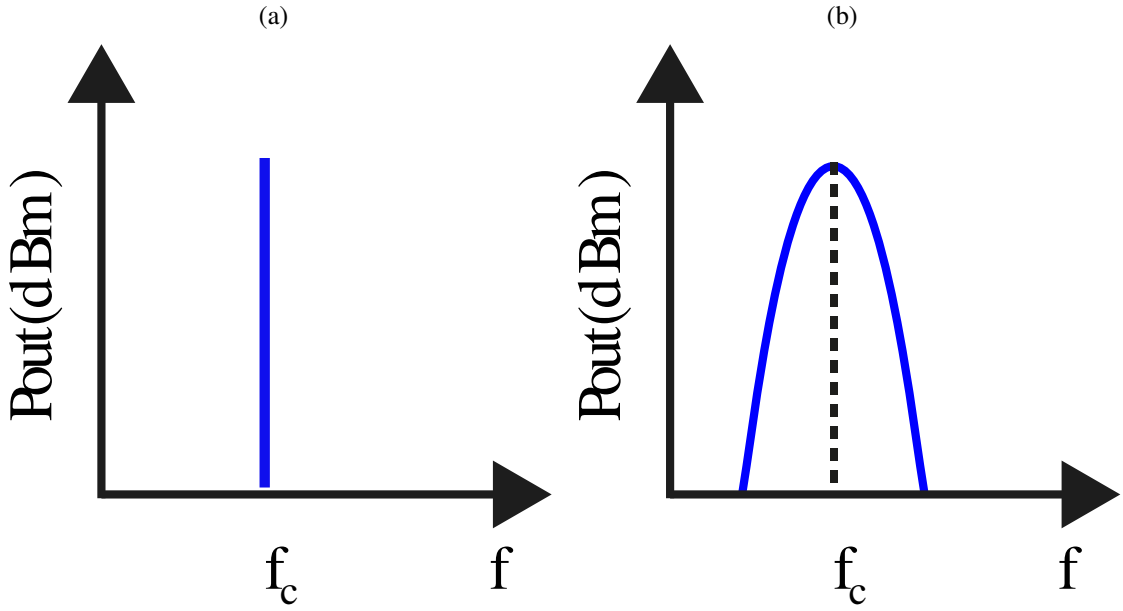
will not exceed 400mV for ultra-low voltage oscillators, which represents approximately $16\phi_t$. The new condition derived from 2.8 satisfies both the start-up and the steady-state conditions.

$$gm_g \geqslant \frac{4}{R_p}. \tag{2.8}$$

2.6 Phase Noise in Weak inversion Oscillators

An ideal LC-oscillator presents an output signal at the resonance frequency of its passive components. This results in an output signal precisely at the resonance frequency and without of any other components. The spectrum of this signal is presented on the Figure 2.11(a). However, the LC tank is not ideal and has a finite quality factor. The noise coming from trapped charges in transistors channel/oxide interfaces and from other sources can perturb the output signal resulting in noise in the oscillation phase, or phase-noise for short. The real output spectrum of an LC-oscillator can be observed in the Figure 2.11(b). It is possible to observe that the signal has a power output in other frequencies. The output power decreases when the frequency moves away from the carrier frequency. Hence, when it is plotted the phase-noise versus offset from the carrier, the shape of the curve is a descending line.

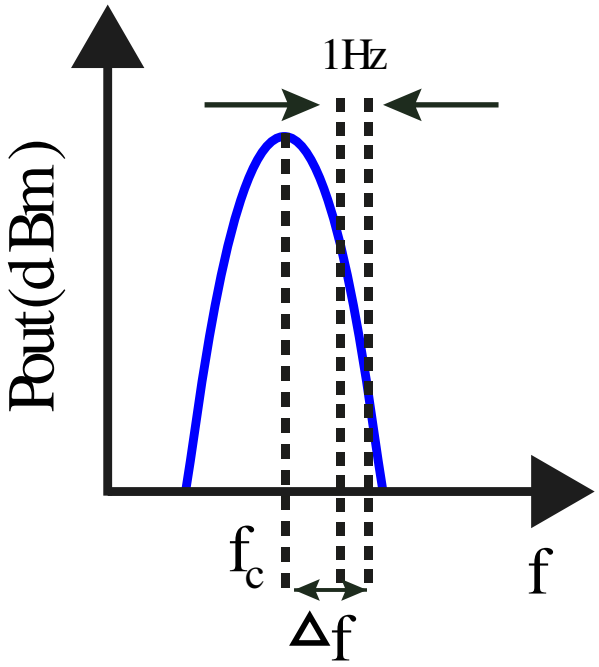
Figure 2.11: (a) Spectrum of the ideal oscillator output tone. (b) Spectrum of the output tone from oscillator with phase noise.



Source:Adapted from (RAZAVI, 1998)

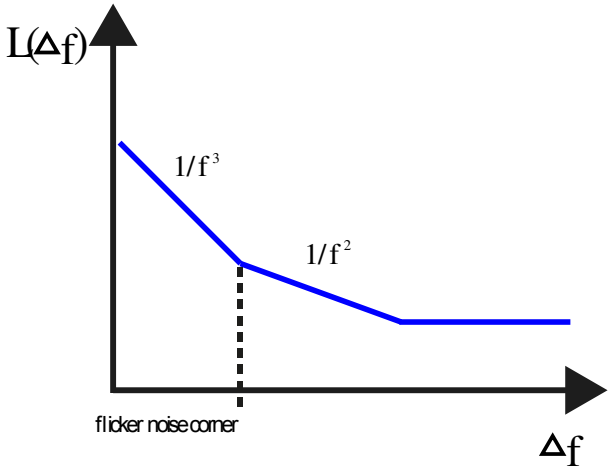
The phase-noise is computed at a frequency offset from the carrier considering a bandwidth of 1 Hz. The signal of this bandwidth is measured at an offset from the carrier and normalized to the power of the carrier. Hence, the phase-noise is measured in dBc/Hz. Figure 2.12 shows this quantification.

Figure 2.12: Phase Noise Definition.



Source: Adapted from (RAZAVI, 1998)

Figure 2.13: Phase Noise versus Offset from the Carrier.



Source:Adapted from (Hajimiri; Lee, 1998)

The phase-noise (PN) of an oscillator is a fundamental characteristic since it describes the oscillator spectrum purity around f_0(Hajimiri; Lee, 1998). At a frequency offset, Δf, from f_0, the PN spectrum exhibits three regions: $\frac{1}{f}$, $\frac{1}{f^2}$, and $\frac{1}{f^3}$. Figure 2.13 shows the illustration of these three regions. The CMOS transistor is the main noise con-

tributor in $\frac{1}{f^2}$ and $\frac{1}{f^3}$ regions. Each of those regions has a different mechanism triggering the PN. For instance, the PN is triggered by the flicker noise in the $\frac{1}{f^2}$ region and by white noise in the $\frac{1}{f^3}$ region. Due to the relation between PN and noise of the transistors, it is possible to establish a relation between PN and the forward inversion level (i_f) (Hajimiri; Lee, 1998; Fiorelli; Peralias; Silveira, 2011a; Cunha; Schneider; Galup-Montoro, 1998). PN in the regions $\frac{1}{f^2}$ and $\frac{1}{f^3}$ are respectively given by

$$\mathcal{L}_{1/f^2}(\Delta f) = 10\log\left(k_B T \frac{4\pi^2 \Gamma_{rms}^2}{g m_g n^2 \phi_T^2} \frac{\lambda}{(i_f+1)Q^2}\right) + 10\log\left(\frac{f_O^2}{\Delta f^2}\right)$$

and

$$\mathcal{L}_{1/f^3}(\Delta f) = 10\log\left(\frac{\Gamma_{av}^2 K'_{F,n}}{4WL} \frac{\pi^2}{n^2\phi_T^2} \frac{1}{(i_f+1)Q^2}\right) + 10\log\left(\frac{f_O^2}{\Delta f^3}\right),$$

where λ is the excess noise factor of the white noise, k_B is the Boltzmann constant, T is the absolute temperature, Γ_{rms} is the root mean square (rms) value of the impulse sensitivity function Γ (Hajimiri; Lee, 1998), $K'_{F,n}$ is the NMOS transistor normalized flicker noise constant, and Γ_{av} is the average value of the impulse sensitivity function as defined in (Hajimiri; Lee, 1998).

Since the transistor biased in weak-inversion (WI) has large dimensions, it has a low flicker noise. Conversely, the white noise has similar values regardless of the region of operation. The main difference is the type of noise that dominates the white noise. In WI, the white noise is mainly composed of shot noise. Meanwhile, in moderate-inversion (MI) and strong-inversion (SI), white noise is dominated by thermal noise. Since all the regions (WI, MI, and SI) have similar values for white noise, but the WI region presents a lower flicker noise than the other two regions, one can conclude that the WI region presents the lowest PN (LEE; MOHAMMADI, 2007b). Consequently, it is highly recommended to bias the transistors in WI when targeting ultra-low-power applications. Not only for power efficiency reason but for PN improvement as well.

2.7 Figures of merit for Oscillators

The Figure of merit is a standard to compare oscillators designed for different purposes with the same metric. The most popular figure of merit for oscillator is derived

from the Equation 2.9:

$$FOM = \mathcal{L}_{offset} - 20\log\left(\frac{f_0}{f_{offset}}\right) + 10\log\left(\frac{P_{DC}}{1mW}\right) \tag{2.9}$$

Where the $\mathcal{L}_{offset}$ represents the phase noise from a measured offset from carrier, f_0 is the oscillation frequency and P_{DC} denotes the power consumption of the block. The main issue of this figure of merit is that the phase noise represent the greater impact of FOM. Therefore, to express the merit of ultra-low-power designs, this figure of merit will not be useful or realistic(WANG et al., 2007).

In order to analyze the performance, the figure of merit useful in the literature is the power-frequency-normalized (PFN) and can be derived from(LEE; MOHAMMADI, 2007b):

$$PFN = 10\log\left[\left(\frac{kT}{P_{DC}}\right)\left(\frac{f_0}{f_{offset}}\right)^2\right] - \mathcal{L}_{offset} \tag{2.10}$$

Where the k is the boltzmann constant and T is the temperature. The main issue concerning this figure-of-merit (FOM) is: it only adds the impact of the temperature on the first one. Furthermore, as in the equation 2.9, the relation of the frequency from carrier to the offset frequency is squared. This results that oscillators which operate at higher frequencies achieve in general better PFN. To address this issue and to compute the impact of this work related to power consumption at the state-of-art, a new figure-of-merit is proposed in this work:

$$FOM = \mathcal{L}_{offset} - 20\log\left(\frac{f_0}{f_{offset}}\right) + 40\log\left(\frac{P_{DC}}{1mW}\right) \tag{2.11}$$

This figure of merit is a modification of equation 2.9. The impact of power consumption in the FOM is increased. This metric is chosen because this work aims to achieve ultra-low power consumption. Furthermore, the term in the equation which describes the oscillator power consumption is raised to the fourth power. Therefore, the impact of the power consumption of the oscillator will be increased.

2.8 State of Art for Low Power Oscillators

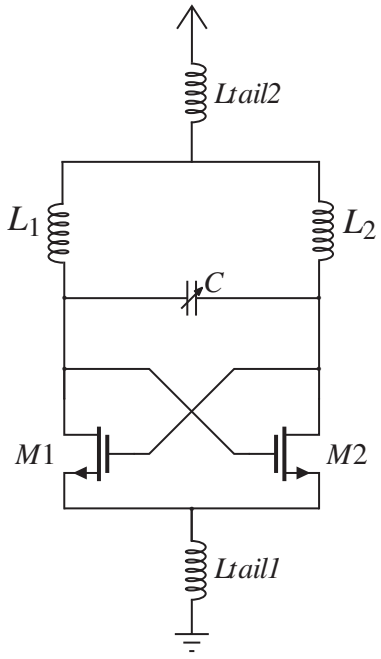
The firsts integrated transceivers date back to the 1980s and were addressed to mobile telecommunications (LEENAERTS; TANG; VAUCHER, 2003). The device tech-

nology used in those early designs are bipolar transistors which consume more power and allow for a lower integration than CMOS. Both features added to a high degree of integration between digital and analog circuits, making the CMOS process the most useful not only for integrated transceivers but also for the majority of the integrated analog circuits. In the beginning, the higher achievable operating frequency of the bipolar process in comparison to the then-available CMOS made the bipolar a better choice to design transceiver(HABEKOITE et al., 1987). Nowadays, this assumption is not true due to the scalability of CMOS process which enables high frequency of operation(KANG; NIKNEJAD, 2013)(VOLKAERTS; STEYAERT; REYNAERT, 2011)(LOO; WIN; YEO, 2018).

The main difference of performance of the transceivers over the last passing years refers to the power consumption. The power supply reduction is directly impacted by the reduction of the oxide thickness added to the decrease of the threshold voltage of transistor. It is possible to note this in the voltage controlled oscillators from (BOUZERARA; ELAROUSSI, 2005) and (YU et al., 2006). The first one is an adapted push-pull complementary topology with a LC-resonator and an inductive source degeneration technique to reduce the phase-noise. This work presents a power consumption of 2.8mW with 1.8V of supply voltage and was designed for a 350nm CMOS technology. The second design shows a big improvement in the power consumption with differential Colpitts topology designed for a 180nm CMOS technology. This VCO achieves a power consumption of $1.2m$W with a power supply of 1V. Furthermore, both oscillators operates at the same frequency of 1.8GHz.

A different approach to improve the power efficiency of a cross-coupled voltage controlled oscillator is presented in (LEE; MOHAMMADI, 2007b). The architecture used by the author is the NMOS-only structure with an LC-resonator and a two tail inductors. The figure 2.14 shows the architecture proposed by author. The tail inductors are added to reduce the phase-noise from the tail transistor and they also help to save power. However, the main design technique employed in this work is the weak inversion operation of the transistors. Furthermore, this work explores the exponential relation between current and voltage of the FET device in weak inversion operation to obtain the maximum gm to Id ratio. As a result of this design topology choice, the power consumption achieved in this work is merely 0.43mW with a very simple topology. Moreover, the resulting phase-noise is -106 dBc/Hz at a 400kHz offset from the carrier. The oscillation frequency in this example 2.63GHz.

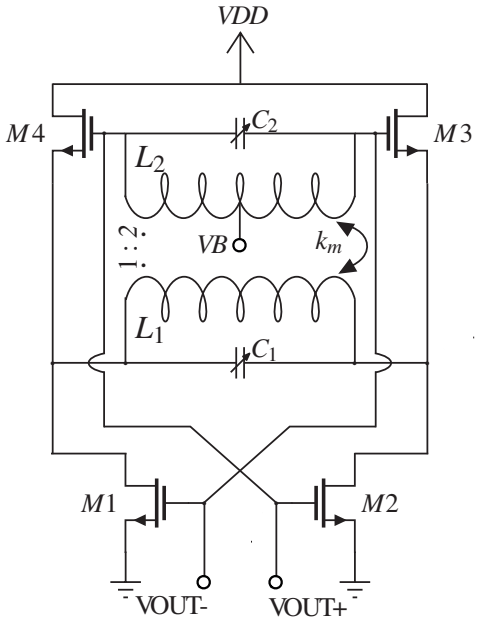
Figure 2.14: LC-VCO with tail inductors.



Source:Adapted from (LEE; MOHAMMADI, 2007b)

In (BABAIE; SHAHMOHAMMADI; STASZEWSKI, 2015b) the goal of the author is to combine the supply voltage scaling advantage from NMOS-only topology with the current efficiency characteristic of complementary push-pull to improve power consumption. Hence, a new configuration of the oscillator which transforms the fixed current source of the NMOS-only topology in a one that changes the direction during a half of oscillation period as complementary push-pull topology is proposed. The proposed architecture is presented in figure 2.15. Furthermore, with this architecture, the authors achieve operation for supply voltage below 0.5V with current efficiency. To achieve this mode of operation it was necessary to implement a transformer-based resonator which also improves the quality factor of the tank. The achieved supply voltage and power consumption were 0.5V and 0.5mW, respectively, at the 4.8GHz central frequency. The phase noise also improves with the switching current operation and thus results in -139dBc/Hz at 10MHz of offset from the carrier.

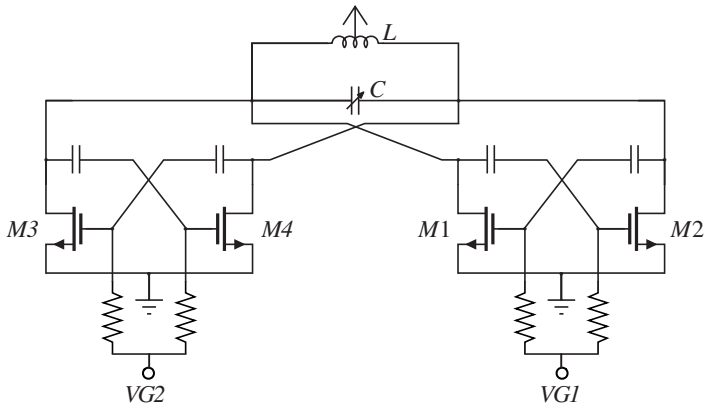
Figure 2.15: NMOS-Only with Alternating current source Oscillator.



Source:Adapted from (BABAIE; SHAHMOHAMMADI; STASZEWSKI, 2015b)

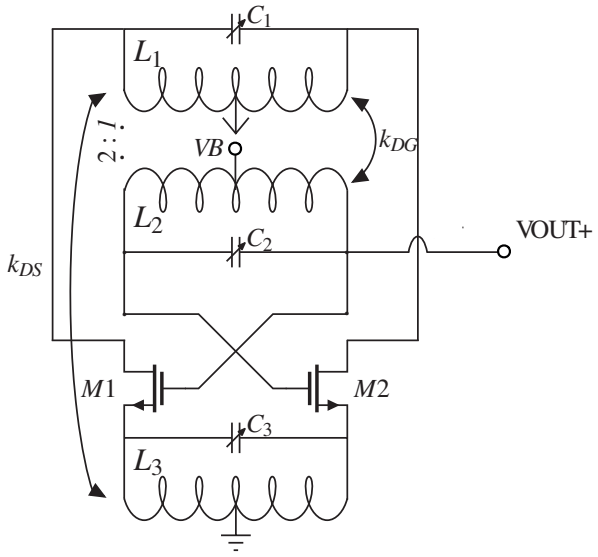
The change in the conduction angle of the oscillator is a technique to improve the phase noise. The class-C is the choice in (OKADA et al., 2009) which on one hand improves the phase noise and on the other hand cannot operate with a low supply voltage. To solve this problem the author proposed a dual conduction Class-C operation, which is presented in the figure 2.16. . Hence, the circuit is composed of two cross-coupled pair to perform a dual operation. Each one of these pairs of transistors operates with different bias sources and consequently with a distinct conduction angle. Hence, the work achieves ultra low power operation without compromising the phase-noise. The dual class-C idea operates at 4.5GHz and consumes 0.114mW with -104dBc/Hz at 1MHz.

Figure 2.16: Dual Class-C Oscillator.



Source:Adapted from (OKADA et al., 2009)

Figure 2.17: DCO with Trifilar Coil-based resonator.



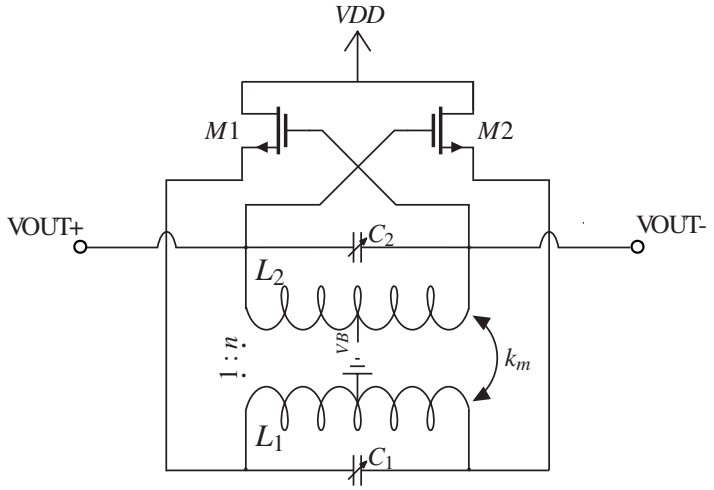
Source:Adapted from (LI et al., 2017)

The class-F operation is another possibility to design low power oscillators due to the voltage gain obtained from the transformer. However, the minimum supply voltage cannot be below the value of the threshold of the transistor. To solve this problem, in (LI et al., 2017) a new circuit is proposed, adapted from the class-F oscillator. It uses a Trifilar-Coil as the inductive element of the resonator. Consequently, the voltage gain from the transformer is improved and the minimum supply results possible below the threshold of the device. The technology used in this work is the 16nm FinFet CMOS and the design needs 0.6mW of power consumption for the oscillator. The supply voltage is reduced to 0.2V and the phase noise is -134dBc/Hz at 1MHz. The architecture of this oscillator with the trifilar-coil implementation is shown in figure 2.17.

Another design that also works with a very low supply voltage of 0.2V is presented by(YANG et al., 2019). Figure 2.18 shows the topology chosen by its authors. The extremely low voltage supply results in a power consumption of 0.67mW. The central frequency is 2.4GHz and the phase noise results in -119dBc/Hz at 1MHz offset. The proposed design is based on improving the problems addressed with the transformer feedback oscillator and with the Trifilar-Coil based on class-F operation discussed earlier. The new circuit uses a gate to source feedback instead of gate to drain feedback from class-F or source to drain from basic transform feedback topology. The transformer design also is a different one. Both coils are vertically coupled which results in a very challenging design due to the different sheet resistance from metals of each coil. The vertically coupled coils result in a lower quality factor to the secondary in comparison to the primary. The

final circuit results in just one cross-coupled pair composed of NMOS transistor, added to a transformer based resonator.

Figure 2.18: Gate-to-source transformer-feedback ULV VCO.



Source:Adapted from (YANG et al., 2019)

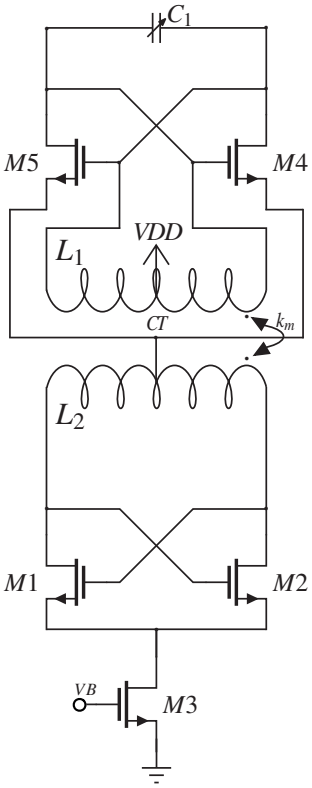
A new topology of the oscillator, which is presented in the figure 2.19, was recently added to the state of art by (LIU et al., 2019). The frequency control of this oscillator is made digitally, thus this circuit is a digitally controlled oscillator instead of a voltage controlled oscillator. The goal of this design is to add this oscillator to a low power fractinonal-N ADPLL. This design also aims reduce the power consumption below 0.5mW. The circuit is composed by two NMOS cross-coupled pairs to improve the achievable transconductance. Both cross-coupled pairs are coupled by a transformer which composed the resonator together of the capacitors bank of each side of coils. The final power consumption of this design is merely 0.107mW, the phase-noise is 107dBc/Hz at 1MHz offset from the carrier, and the oscillation frequency is 2.46GHz.

Table 2.1: State of Art
Source:Author

	I*	II*	III*	IV*	V*	VI*
Process (nm)	180	65	28	16	40	180
Phase Noise (dBc/Hz)	-104 @1MHz	-107 @1MHz	-119 @1MHz	-134 @10MHz	-139 @10MHz	-106 @400kHz
Frequency (GHz)	4.5	2.46	2.24-2.6	3.2-4.0	4.8	2.63
VDD (V)	0.2	0.45	0.2	0.2	0.5	0.45
Power (mW)	0.114***	0.107***	0.67***	0.6***	0.48***	0.43***

*Measurement Results I-(OKADA et al., 2009) IV-(LI et al., 2017)
**Simulation Results II-(LIU et al., 2019) V-(BABAIE; SHAHMOHAMMADI; STASZEWSKI, 2015b)
***Without Output Buffer III-(YANG et al., 2019) VI-(LEE; MOHAMMADI, 2007b)

Figure 2.19: Transformer-based stacked-gm DCO.



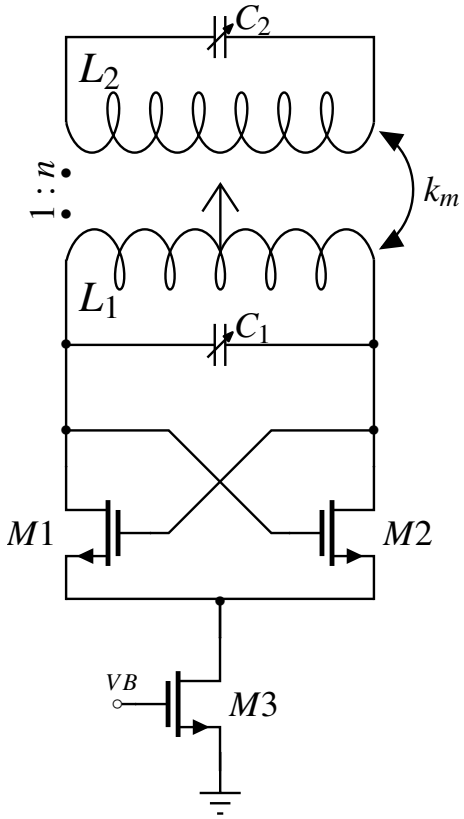
Source:Adapted from (LIU et al., 2019)

To list all the relevant features of the designs previously reviewed and to compare their most important results, Table 2.1 summarizes the main figures achieved by their authors. The table 2.1 will be used in chapter 5 as reference to compare with results achieved in the course of this Master´s thesis.

2.9 Proposed Topology

The main objective of this work is to design an ultra-low voltage digitally controlled oscillator that achieves a power consumption comparable to the state of art without compromising its phase-noise. Furthermore, the goal of this work is to achieve low power operation with a basic topology and then to prove that it is possible to design it with transistors operating only in weak inversion - a new design approach to the DCO - combined with improvements in the design of the resonator. To achieve this, the topology presented in Figure 2.20 is proposed and will be developed further in the next chapters.

Figure 2.20: Transformer-Based DCO



Source:Adapted from (EL-GOUHARY; NEIHART, 2011)

The topology is an NMOS-only presented at the beginning of this chapter. The main improvement addressed here is the transformed-based resonator, which increases the parallel resistance of the tank. With the proposed topology it is expected to show later that the current consumption can decrease due to the transformer in the resonator. Furthermore, the minimum required supply voltage for oscillation is also reduced due to its inherent single cross-coupled pair.

2.10 Conclusion

In this chapter the basics of the frequency synthesizers and PLLs were presented. Furthermore, the basic topologies of PLLs and ADPLL with the main differences and functionalities were summarized. This chapter also had the purpose of showing the main functionality of the oscillators in the PLLs and ADPLLs. In addition, the motivation behind the intensive digital approach to the Phase Locked loop is discussed. The main topologies of digitally controlled oscillators present in the literature were summarized in this chapter. The main figures of merit described in the literature were reviewed. The issues of the losses in the resonator and the conditions to sustain an oscillation were also discussed. The direct relation between the weak inversion operation and the phase noise was addressed. Finally, the proposed topology to achieve the goals of this Master´s thesis was presented.

3 TRANSFORMER BASED RESONATOR

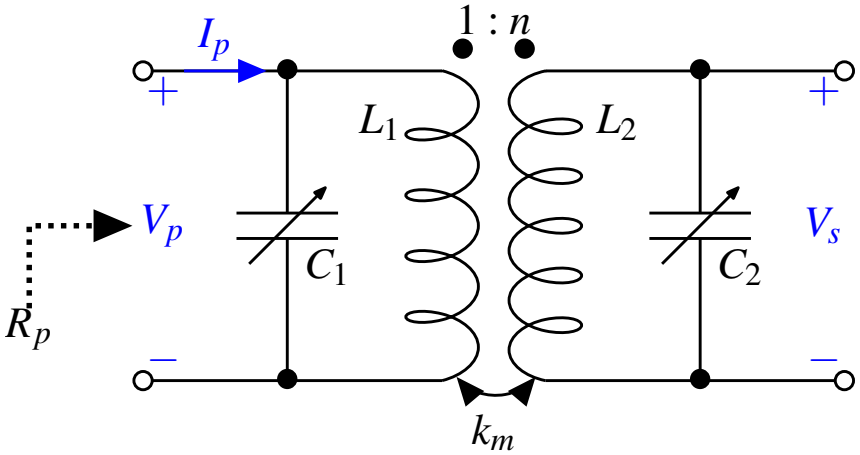
3.1 Introduction

The improvements of the inductor in the LC-based oscillator is limited by the technology. As discussed previously, the goal of this work is to obtain the maximum quality factor of the inductor, henceforth achieving the maximum parallel resistance for the resonator with a minimum required area. The expectation is that less power consumption will be required from the oscillator and the phase noise will be also improved. Ultra-low power operation demands a very high-quality factor to satisfy the power consumption and phase noise requirements. In addition, with a single inductor designed in the latest technologies (i.e. 40nm CMOS for one particular design in chapter 5) it is difficult to improve the DCO design. From this need, the transformer based resonator arises as a viable option or solution (STRAAYER; CABANILLAS; REBEIZ, 2002).

3.2 Principle of Operation

The transformer resonator is a very useful approach when the ultra-low power consumption is required. In comparison to the oscillator that uses an LC resonator, the phase noise can be improved by 6 dB just by the transformer-based resonator implementation. The phase-noise improvement results from the bandwidth reduction by the increase of the quality factor (BAEK et al., 2003). Figure 3.1 shows a transformer-based resonator implementation.

Figure 3.1: Transformer Based Resonator Parallel Resistance



Source:Adapted from (BABAIE et al., 2016)

The transformer results in only a parallel resistance when C_1 and C_2 resonate with the L_1 and L_2 respectively. The parallel resistance at the resonance is derived from the Equation 3.1(BABAIE et al., 2016).

$$R_p \approx L_1 \omega_0 Q_1 \left(1 + k_m^2 \frac{Q_2}{Q_1}\right) \tag{3.1}$$

Where Q_1 and Q_2 are respectively the quality factors of the first (primary) and second (secondary) coils, and k_m is the transformer coupling coefficient. If k_m is 1 and Q_1 and Q_2 are the same, which is an ideal situation, the R_p of the transformer-based resonator is two times larger than the R_p of the single-inductor-based. This assumption also considers that the inductance of the single-inductor and the of the primary and the secondary of the transformer is the same. Just this doubling helps to reduce the oscillator power consumption.

3.3 Transformer Layout

The shape of the transformer layout is an essential part of its design. The most common shapes are the square and the octagonal. On one hand, the shape octagonal can slightly improve the quality factors of each coil of the transformer. On the other hand, the shape square can achieve much higher inductance on each coil due to the increase in the total length of coils. This behavior is similar to a simple inductor.

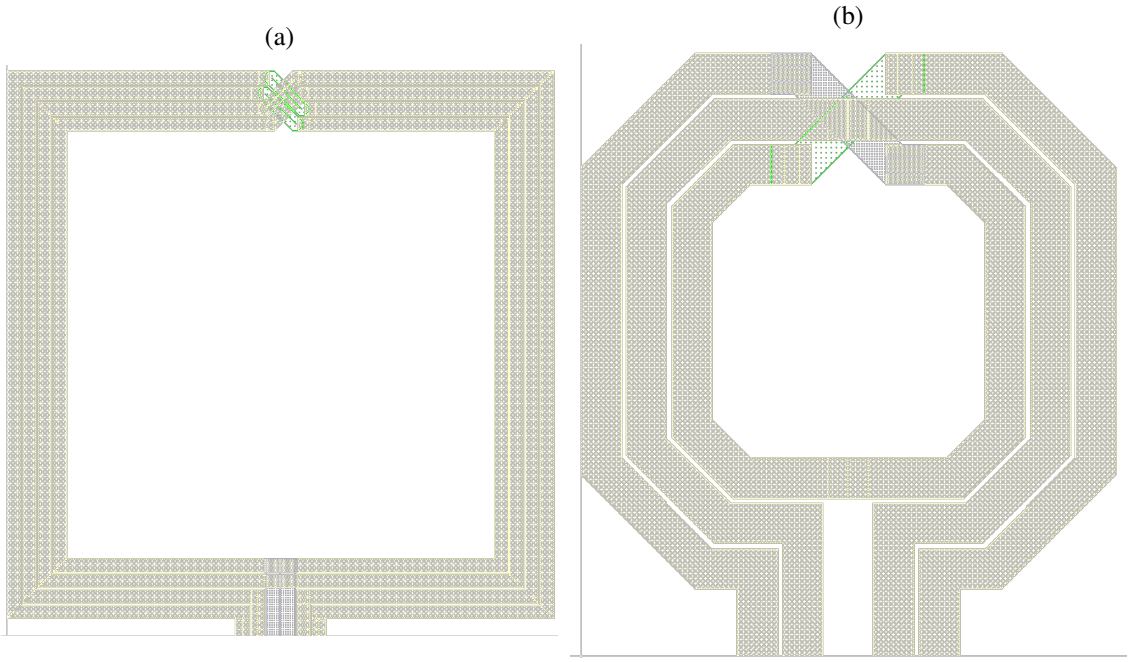
Furthermore, the coupling method also impacts the performance of the transformer. There are two most useful coupled methods on the actual CMOS technologies: the stacked and the planar approaches. The stacked method improves the coupling factor in comparison to the planar one. However, the quality factor of secondary is increased on the planar method due to the possibility of using the same top-level metal of the primary. The ultra-thick metal generally is the top-level of metal. Furthermore, in the most current technologies, there is only one ultra-thick metal. In the stacked topology, the primary and secondary must be performed in different levels of metal films, which decrease the quality factor of the secondary coil (LONG, 2000)(LEITE, 2011). Figure 3.2 shows the configurations of planar transformer while Figure 3.3 shows the stacked one.

In the 28 nm technology which is used in this work, there are only three metal layers (M8, M9, and AP) thicker than the other underlying thin metals. However, there is only one ultra-thick metal: the M9. Hence, the planar topology is a better choice in this

case. The impact on the quality factor of the secondary coil when the stacked topology is used will be much higher than the impact in the coupling factor when the planar one is used.

Another challenge in the transformer design, when it refers to CMOS processes, is that it suffers from substrate loss. The main problem here is the finite resistivity of the substrate. This conductive behavior of the substrate combined with the capacitive coupling between the conductors and substrate makes that current flows through it. Furthermore, eddy currents also flows in the substrate due to the electromagnetic induction. These losses further decrease the quality factors of the coils. To avoid this problem, the insertion of the Patterned Ground Shield (PGR) is an option and used in (EL-GHARNITI; KERHERVE; BEGUERET, 2006), while the floating shield is used in(CHEUNG; LONG, 2006). The main problem here is that, even presenting favorable results in frequencies below 10 GHz, both solutions do not present a significant impact on the quality factor at frequencies below 2 GHz, which is the case for the oscillator focused in this work.

Figure 3.2: (a) Square Planar Transformer. (b) Octagonal Planar Transformer.

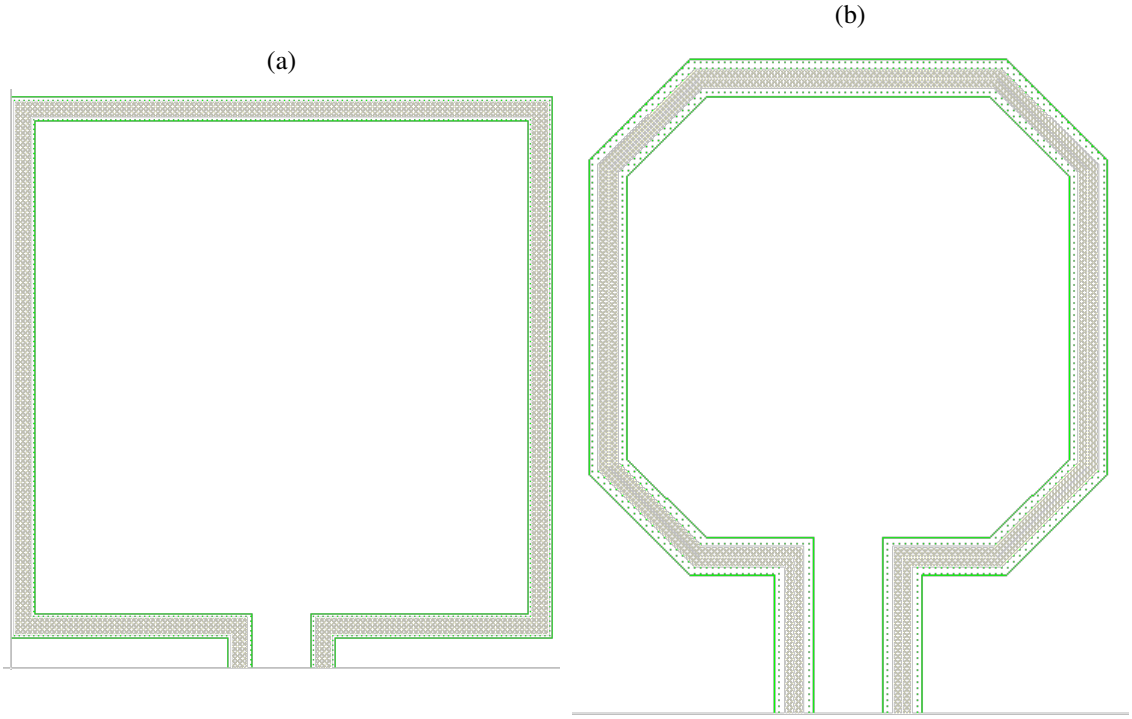


Source:Author

3.4 Transformer Simulations

To simulate the transformer together with the layout of the DCO in the Cadence ambient, it is necessary to design and simulate it in an electromagnetic simulator to com-

Figure 3.3: (a) Square Stacked Transformer. (b) Octagonal Stacked Transformer.



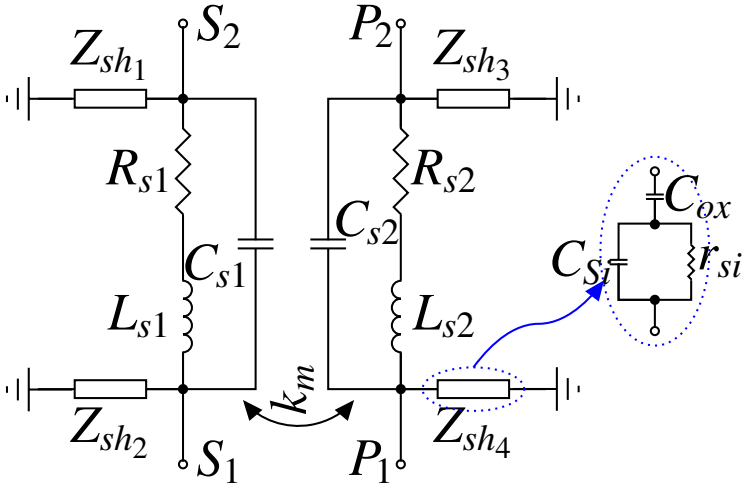
Source:Author

pute its effects and extract its time-domain model. To design and simulate the transformer, this work uses two electromagnetic simulators: the ASITIC and the Advanced Design System ADS from Keysight. The first one, to obtain the first layout which will be adjusted to satisfy DRC issues in the layout editor environment (also Cadence Virtuoso(TM) herein). Furthermore, the ASITIC also helps to get the preliminary results from the transformer simulations. The second, to finish the electromagnetic simulations using the momentum microwave results of the transformer and to extract the time domain model in order to execute the final simulations with the layout of the oscillator.

3.5 Time Domain Model

The first step to extract the time domain model of the transformer is to choose a lumped model that represents precisely the behavior of the transformer in the required frequency range. The oscillator proposed in this work operates at 1.8GHz, which corresponds to the double of the WiFi-HaLow standard central frequency in some countries. Hence, the size of the transformer decreases and, thus, the overall quality factor increases. Figure 3.4 shows the model which will be used in this work. The lumped model is composed by a two π-model of each coil coupled by a coupling factor k_m. The $R_{ss,sp}$, $C_{s,p}$,

Figure 3.4: Transformer lumped model



Source:Adapted from (KANG; GIL; SHIN, 2005)

and $L_{s,p}$ are respectively the resistances, the capacitances, and the self-inductances of the coils. Additionally, the impedances Z_{sh1-4} model the coupling to the substrate.

3.6 Conclusion

This chapter dealt with the impact of the transformer-based resonator in the power consumption of the oscillator. Furthermore, the improvements in the phase-noise of this block are also discussed. Additionally, the steps and methods for integrated transformer simulations were exposed. To conclude, the time domain model which is used for the transformer in this design was showed.

4 DESIGN METHODOLOGY

4.1 Introduction

The design of a low power LC-oscillator can be split into main steps. The first remains about the minimizing the losses of the resonator to improve both the power consumption and the phase-noise of the oscillator. The second is related to the sizing and the bias condition of the transistors which impacts on the noise contribution by the devices. The transistor must be sized to achieve the required transconductance to satisfy the start-up and steady-state conditions. Furthermore, the noise contribution of the transistor changes with the inversion level as presented earlier. In the deep-submicron process, the maximum gm/I_d achieved is lower than the obtained in old technologies. To achieve the same power consumption it is necessary to compensate the difference of the gm/I_d by the improvement of the quality factor of the resonator.

The present study proposes a new design methodology for oscillators aiming to optimize circuit performance at low power. The methodology is based on the Unified Current-Control Model (UICM) which is a physics-based model and enables an accurate all-region modeling of the operation of the device (Cunha; Schneider; Galup-Montoro, 1998), not based on an empirical model such as (Fiorelli; Peralias; Silveira, 2011b). In addition, the proposed methodology also describes the design of a transformer to maximize the R_p seen by the cross-coupled differential pair. In this design, the required ω_0 is twice the operating frequency of the WiFi HaLow standard, i.e. $2\pi \times 1.8$ GHz (in rads/sec).

The methodology is presented by the following steps: first is presented the transformer design and parameters extraction, the method to extract the parameters of the transistor is showed in section 4.3, the sizing of the transistor and the minimum V_{DD} required to sustain the oscillation are discussed in the sections 4.4 and 4.5 respectively.

4.2 Transformer Design and Parameters Extraction

The first step in the design is related to the configuration of the transformer and to extract its equivalent time-domain model. The transformer is designed to achieve the maximum R_p possible. As described by Equation 3.1, the R_p depends on both quality factors of the primary and secondary coils. The coupled factor also impacts on the max-

imum achievable parallel resistance. The best-coupled method in the technology used (TSMC 28nm) is the planar one. This is due to there is only one ultra-thick metal in this technology. When there is a high difference in the sheet resistance to the metals of the primary and secondary coils the quality of the secondary coil, which is designed on the lower metal, is severely impacted. The best configuration of the number of turns to the primary and secondary must be checked too. There is an impact on the quality factor by the number of turns of both primary and secondary coils due to the crossing of metals. To check the best configuration to the transformer considering the number of turns and width of primary and secondary and better metals to primary and secondary, ASITIC and ADS from Keysight software are used.

To extract the equivalent π-model of each coil from the S-parameter simulation. Each coil is extracted separately, first to obtain the π-model presented in Figure 4.1. Where R_s, C_{wi}, and L are respectively the parasitic resistance, the inter-winding capacitance, and the inductance of the coil. Additionally, the impedances Z_{sh1-2} model the coupling to the substrate. Furthermore, P_1 and P_2 represents the two ports in the simulation. Each coil was simulated in a two-port electromagnetic simulation and the parameters are extracted from S-parameters results. First, the inductor L is extracted at low-frequency from the following equation (SCHIMPF; BENNA; PROETEL, 2001):

$$L = \frac{im\left[\frac{1}{Y_{21}}\right]}{\omega} \tag{4.1}$$

After computing the inductance, the inter-winding capacitance C_{wi} is extracted from the resonance of $im(1/Y_{21})$ which results:

$$C_{wi} = \frac{1}{\omega^2 L} \tag{4.2}$$

The parasitic resistance (R_s) is also extracted from the low-frequency analysis of Y_{21} as follows:

$$R_s = real\left[\frac{1}{Y_{21}}\right] \tag{4.3}$$

The first step is to extract the oxide capacitance (C_{ox}) also from a low-frequency analysis. At low-frequencies, the influence from the substrate becomes negligible. The oxide capacitance from both sides of the model are extracted from the following equations

(KANG; GIL; SHIN, 2005):

$$C_{ox1} = -\frac{1}{\omega Im\left[\frac{1}{Y_{11}+Y_{12}}\right]} \tag{4.4}$$

$$C_{ox2} = -\frac{1}{\omega Im\left[\frac{1}{Y_{22}+Y_{12}}\right]} \tag{4.5}$$

To compute the influence of the substrate, the analysis must be done at high-frequencies. Therefore, the r_{si} and C_{si} from both sides of the model are extracted at high frequencies using the following equations(CHEN et al., 2008):

$$r_{si1} = \frac{1}{Real\left[Y_{11}+Y_{12}\right]} \tag{4.6}$$

$$r_{si2} = \frac{1}{Real\left[Y_{22}+Y_{12}\right]} \tag{4.7}$$

$$C_{si1} = \frac{Im\left[Y_{11}+Y_{12}\right]}{\omega} \tag{4.8}$$

$$C_{si2} = \frac{Im\left[Y_{22}+Y_{12}\right]}{\omega} \tag{4.9}$$

After computing all parameters of the π-model for each coil, a two-port electromagnetic simulation of the transformer must be performed to compute the coupling factor between two coils and then to obtain the model of Figure 3.4. The k_m is obtained from the Z-parameter simulation of the transformer, and it is given by (LEITE et al., 2009),

$$k_m = \sqrt{\frac{imag(Z_{12})\ imag(Z_{21})}{imag(Z_{11})\ imag(Z_{22})}}. \tag{4.10}$$

After computing the complete model of the transformer, a new simulation must be performed in order to execute the fine adjusts. In addition, the quality factor, which is defined by the ratio between the energy stored to the energy dissipated by Joule heating, for each coil of the transformer is computed from the 2-port electromagnetic simulation and are derived from the following equations:

$$Q_p = \frac{im(Z_{11})}{real(Z_{11})} \tag{4.11}$$

$$Q_s = \frac{im(Z_{22})}{real(Z_{22})} \tag{4.12}$$

Furthermore, the inductance of primary and secondary are extracted from the ratio of the imaginary part of the impedance to the ω corresponding the frequency of operation. From the equations below are derived the primary and secondary inductances at a two port measurement.

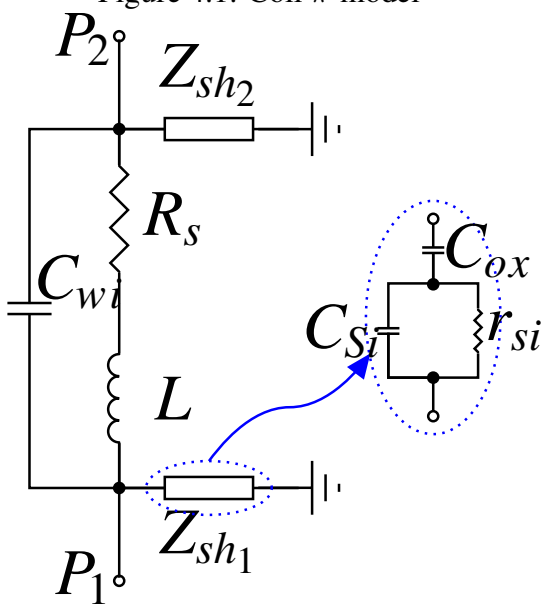
$$L_p = \frac{im(Z_{11})}{\omega_0} \tag{4.13}$$

$$L_s = \frac{im(Z_{22})}{\omega_0} \tag{4.14}$$

The inductance ratio, which impacts directly on the transformer voltage gain, is derived from the following equation:

$$n_L = L_2/L_1 \tag{4.15}$$

Figure 4.1: Coil π-model



Source:Adapted from (KANG; GIL; SHIN, 2005)

4.3 Transistor Parameters Extraction

The second step in the proposed methodology is to extract the design parameters of the Unified Charge-Control Model for MOSFETs (UICM Model), such as the equilibrium threshold voltage (V_{T0}), the sheet normalization current($I_{SH} = \mu_n C'_{ox} n \phi_t^2/2$), and the

slope factor (n) of the transistor. The I_{SH} and the V_{T0} are extracted from the curve $V_G \times gm_g/i_d$. Meanwhile, n is extracted from the $V_G \times V_P$ sweep, where V_G and V_P are respectively gate and pinch-off voltage of the transistor. The slope factor and the gm_g/id are derived from the following equations:

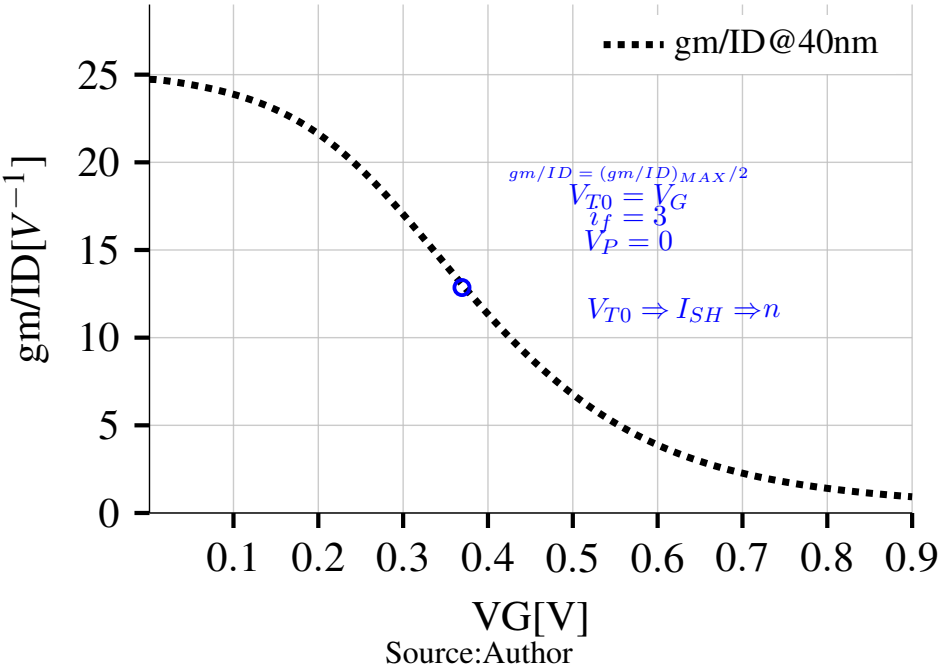
$$n = \frac{1}{(dV_P/dV_G)} \tag{4.16}$$

$$gm_g/i_d = \frac{d \ln i_d}{dV_G} \tag{4.17}$$

Figure 4.2 shows the plot of the gm_g to i_d curve for the NMOS FET with 28nm channel length, in order to extract the V_{T0}. And the plot with the results from the slope factor extraction is shown in Figure 4.3. The equilibrium threshold voltage (V_{T0}) at bulk-to-source voltage $= 0V$ is derived from the Equation 4.18.

$$V_{T0} \approx V_{FB} + 2\phi_F + \gamma\sqrt{2\phi_F} \tag{4.18}$$

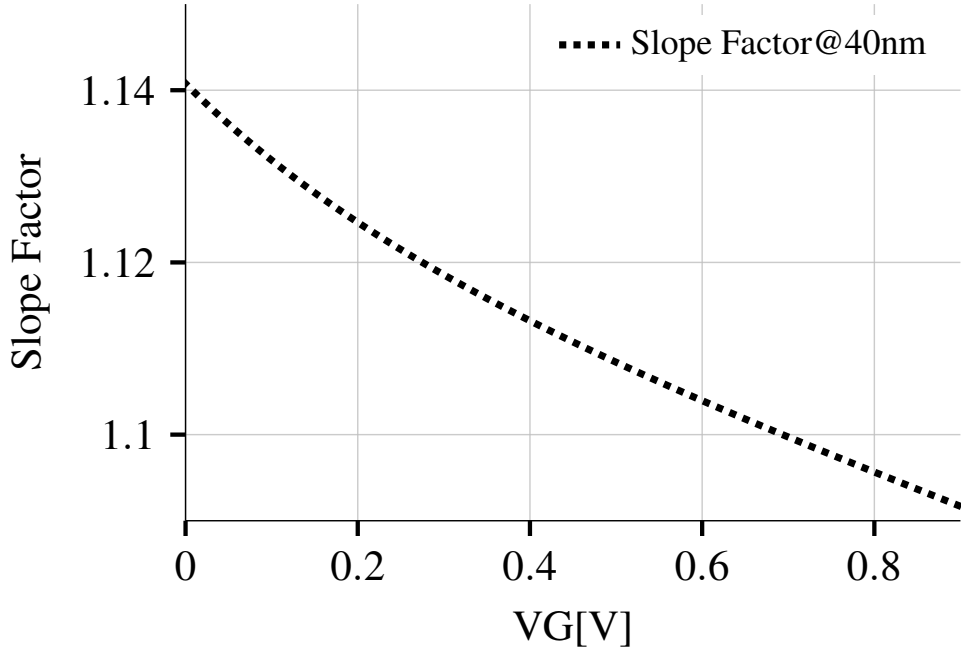
Figure 4.2: The simulated gmg/id vs. VG plot for an NMOS 40nm transistor



Source:Author

In the next steps, all transistors are assumed in saturation, which results in the absence of the reverse current component in the UICM model. Hence, the normalized reverse current i_r is also disregarded.

Figure 4.3: Slope factor curve for tsmc 40nm tecnology



Source:Author

4.4 Cross-Coupled Pair

The third step is the sizing of the cross-coupled pair using the UICM equations in such a way that both the start-up and the steady-state conditions discussed in chapter 2 are satisfied. First, one must select a gm_g to satisfy both start-up and steady-state conditions. Second, define the maximum inversion level (i_{fmax}), which is given by,

$$i_{fmax} = \left(\frac{2I_D}{n\phi_t gm_g} - 1\right)^2 - 1, \tag{4.19}$$

where I_D is the drain current and ϕ_t is the thermal voltage. Third, the saturation level (V_{dsat}) and the normalization current (I_S) are calculated using the equations 4.20 and 4.21.

$$V_{dsat} = \phi_t \left(\sqrt{1 + i_f} + 3\right) \tag{4.20}$$

$$I_S = \frac{n\phi_t gm_g}{2(\sqrt{1 + i_f} - 1)}. \tag{4.21}$$

Finally, based on the previous equations, the transistor width and length ratio

(W/L) of the cross-coupled pair is given by Equation 4.22.

$$\frac{w}{l} = \frac{I_S}{I_{SH}} \tag{4.22}$$

Since the tail transistor works with twice the current of the cross-coupled pair, it is two times larger when biased for the same inversion level i_f. However, whenever another i_f is selected for the tail transistor, I_S has to be redefined.

4.5 Minimum Supply Voltage

The fourth step is to define the minimum supply voltage required to maintain the oscillation condition. VDD scaling is chiefly limited by V_{dsat} of the tail transistor since its drain-to-source voltage (V_{ds}) is proportional to VDD. Hence, VDD_{min} is given by

$$VDD_{min} = n\phi_t \left[\sqrt{1+i_f} - 2 + ln\left(\sqrt{1+i_f} - 1\right)\right] + V_{T0} + V_{dstail},$$

where V_{dstail} is the drain-to-source voltage of the tail transistor. In this design, all the transistors have the same inversion level, which is the minimum inversion level to obtain the drain to source voltage requirements for the low voltage implementation goal.

4.6 Capacitor bank

The final step is about the frequency control. The capacitor bank must be chosen carefully. The PMOS as varactor presents higher capacitance per unit area. The PMOS also presents better noise characteristics in comparison with the NMOS transistor. Therefore to perform the capacitor banks to each side of the transformer the PMOS transistor is used as a varactor. The varactors with MOS transistor results in a better quality factor due to not required switches like in switched capacitors option.

The layout of the capacitor bank severely impacts the quality factor and on the tuning range of the oscillator. It is necessary to minimize the impact of the resistance inserted by the routing together with the reduction of the parasitic capacitance. To minimizing the parasitic resistance it is necessary to increase the width of the wires, however the capacitance increase. Therefore, there is a trade-off between the parasitics that must

be checked on the layout to achieve a better relationship between both.

The number of bits also must be checked. The number of bits also impacts on the tuning range and on the quality factor. This is due to the increase on routing by the increase in the number of bits. Therefore, the maximum number of bits that results in a satisfactory tuning range and power consumption must be chosen.

4.7 Conclusion

This chapter focused on presenting the design methodology for the DCO . The method to extract the time-domain model of the transformer was first presented. The step by step method to size the transistors in order to maximize the power improvements (reductions) was explained. In addition, the key transistor parameters extraction methods to insert the physical effects in the design equations were also presented.

5 DCO DESIGNS

5.1 DCO system requirements

To compute the DCO system requirements it is necessary take into account the ADPLL requirements. In this work, those are set in the context of the WiFi HaLow standard minimum requirements. Table 5.1 shows the specification of the WiFi HaLow ADPLL system (SOUZA et al., 2020). To cover all Wi-Fi Halow standard bands, a frequency range from 860MHz to 930MHz is necessary. This covers the WiFi HaLow operation in Europe and in countries like the United States, Japan, and Brazil.

The most power hungry block of the ADPLL is the DCO. The main target of this work is to design an oscillator with a power consumption below 500μW to achieve a result competitive with the state of art. Hence, a power consumption below 800μW for all system is a possible goal (CHILLARA et al., 2014)(LIU et al., 2019). The settling time of the ADPLL to frequency lock depends on the step in which a frequency jump happens (STASZEWSKI; BALSARA, 2006). As in (LIU et al., 2019), for example, for a small frequency jump the time to lock the frequency is 2μs. While, for a large frequency jump, the settling time increases to 50μs. The locking behavior depends on the phase detector, in this case the TDC, and the digital loop filter. Both blocks need some clock cycles to deliver the required oscillation tuning word in order to control and lock the frequency of the DCO (WU, 2014) (JIANG, 2011). Based on this, and looking for achieving the state of art, a settling time less than 50μs is chosen.

The reference noise floor coming from the buffers and measurement equipments is set to -135dBc/Hz as in (WU, 2014). To define the maximum phase noise level at which the ADPLL can operate satisfactorily, the minimum signal to noise ratio (SNR) that the receiver can allow must be computed. For (ANDRADE et al., 2017), the minimum signal to noise ratio is defined, by simulation, as 5dB. For a robust operation, a SNR of 10 dB is considered. Therefore, the minimum phase-noise for a 1 MHz of bandwidth necessary for the receiver safe operation, is computed from the following equation:

$$PN_{dBc} = -SNR_{min} - 10log10(BW) \tag{5.1}$$

The phase noise requirement of -70dBc/Hz is derived from equation 5.1, which is not a big problem for most ADPLL designs. However, the adjacent channel rejection (ACR) must be taken into account for a spot noise requirements at a larger offset from the

carrier. Then, the phase noise can be derived from:

$$PN_{dBc}@1MHz = PN_{dBc} - ACR \tag{5.2}$$

This results a phase noise of -89 dBc/Hz for a channel bandwidth of 1MHz. In (LIU et al., 2019), the phase-noise of the ADPLL just results about 2 dB above the DCO phase-noise, which is the critical one. Therefore, for a robust design, a phase-noise of -100 dBc/Hz is the goal for the DCO design under this study. Other frequency components can appear in the ADPLL spectrum. This effect is caused by the presence of spurious tones, which are measured in dBc at a specific frequency location of the spectrum. The spurs emission must be below of -30dBc for safe operation. The time error variance, namely jitter, is required to be less than 2.6 ps to be competitive with results from the literature.

Table 5.1: Specifications of WiFi HaLoW ADPLL system
Source:Author

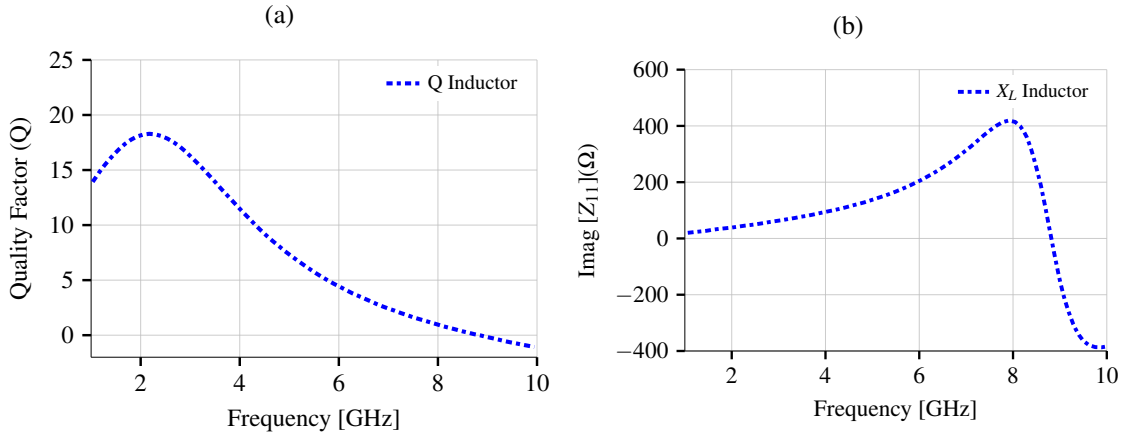
Parameter	Target
Frequency Band	860-930 MHz
Power Consumption	$< 800\,\mu$W
DCO Power Consumption	$< 500\,\mu$W
Settling Time	$50\,\mu$s
Reference noise floor	-135 dBc/Hz
Spurious @ 1 MHz offset	-30 dBc
Inband phase noise floor	-70 dBc
Phase noise @ 1 MHz offset	-89 dBc/Hz
DCO Phase noise @ 1 MHz offset	-100 dBc/Hz
Integrated RMS jitter	< 2.6 ps

5.2 Inductor-Based DCO Design in 40nm

To understand the impact of the weak inversion operation in the power consumption and in the phase-noise of the DCO, a first design with the inductor-based topology presented in the Figure 2.5b, is performed in 40nm CMOS technology using the methodology described previously. The inductor was configured to obtain the maximum parallel resistance, and save as power as possible. The inductor was designed with three turns and achieve a quality factor of 18 at 1.8 GHz, with a inductance of 3 nH. Hence, with a outer diameter of 510μm, the parallel resistance is estimated at just 610 Ω.

Figure 5.1 shows the behavior of the inductor quality factor as a function of frequency. Also, the reactance plot versus frequency is presented and shows a self resonance at 8.8 GHz. At the frequency in which the system operates, the self resonance is much more dependent on the inter-winding capacitance than the capacitance to the substrate. Hence, the inductor must be designed to obtain a self resonance frequency as far as possible from the operational frequency.

Figure 5.1: (a) Quality factor behavior. (b) Imaginary part of Inductor impedance.



Source:Author

The parameters of the NMOS transistors were extracted from Spectre(TM) electrical simulations. The gm to id curve and the slope factor were presented previously in Figures 4.2 and 4.3 respectively. The maximum gm to id ratio is approximately 25, which reflects the impact of such very short channel of this technology. The slope factor shows a slight variation with respect to the change in the gate voltage of the transistor. The extracted slope factor is approximately 1.1. From the gm to id curve an equilibrium threshold voltage of 370 mV was extracted

After extracting the process parameters of the minimum-L transistor, the design of the oscillator to compute the impact of the inversion level on the power consumption and on the phase-noise is performed. Furthermore, three designs of DCO at different inversion levels is performed at the schematic level. In each design, all transistors have the same inversion level to easy compute its impact. The capacitance used in the circuit is an ideal capacitance which results in a operational frequency of 1.8 GHz. The simulation results at different inversion levels are presented in table 5.2.

The results show the impact of inversion level in the reduction of DCO power consumption. Figure 5.3 shows that phase-noise in weak and moderate inversions are equivalent, which ratifies the previous assumptions. The design under strong inversion

regime does not apply to this technology since it would result in a VDD higher than the nominal. The increase on inversion level until the strong inversion has a much more visible impact on the VDD by the increase in the saturation voltage of the tail transistor which was described by Equation 4.20.

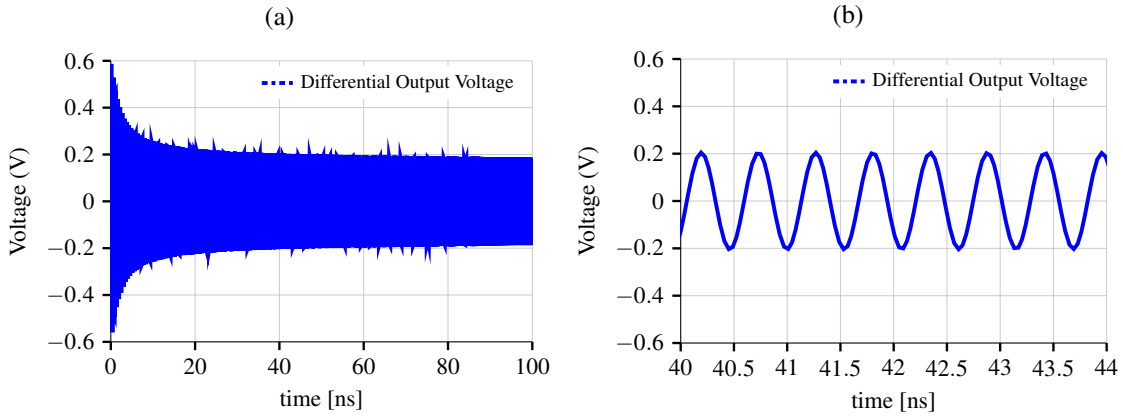
Table 5.2 shows an increase of more than thirty times in the width of the tail transistor when the inversion level varies from 25 to 0.5 (from moderate to weak inversion). In the same range, the DCO power consumption is improved (reduced, in the WI design) by a factor close to five, which is a very significant reduction. To reduce power consumption without increasing phase-noise, $i_f = 0.25$ was selected for the DCO design even with the resulting larger transistor widths. The impact of large device sizes can reduce the reachable frequency range due to the minimum possible resulting capacitance in the resonator.

The final step of the design is related to the frequency control method. The frequency band allocated to the Wifi Halow standard varies from country to country. For instance, this DCO design will cover a band from 902 to 927.5 MHz, which complies with the allocated band in US and Japan. The channel bandwidth is 1 MHz. In this design, ω_0 is 2π x 1.8 GHz, twice the operating frequency of the WiFi HaLow standard. To cover this band with such small resolution, the DCO uses a bank of capacitors implemented with binary switchable capacitances as presented earlier and depicted in Figure 2.7. The unit cell is composed by two PMOS transistors connected as varactors in a differential configuration. The PMOS transistor achieves a higher capacitance with lower size in comparison with the NMOS device. The voltages $V_{tune_{high}}$ and $V_{tune_{low}}$ are 0.9 and 0V respectively. Hence, in the design, we set the unit cell to the high or low-capacitance mode of the oscillator tuning word (OTW). The final configuration of the capacitor bank has 8 bits, which covers the entire band with the selected resolution.

Figure 5.4 shows the LC-based oscillator layout with DCO parameters presented in table 5.3. The capacitance changes from 1.32 pF to 2.06 pF to obtain a frequency range of 60 MHz. These values of capacitance do not take into account the impact of the capacitance from routing. The post-layout simulation shows a DCO power consumption of 380 μW. This result is twice the result obtained from the schematic simulation previously shown. The difference is in part from the decrease of the quality factor of the tank due to the capacitor bank routing. The simulation result of the differential output voltage is presented on figure 5.2. The phase-noise post-layout simulation results considering the corners are presented in figure 5.5. The corner case used in this analysis is only with the

NMOS and PMOS in slow condition. This is due to the slow condition requiring higher current consumption from the transistor than a fast condition to sustain a stable oscillation. The circuit would obviously benefit from a fast case condition. Hence, this corner was not simulated. The slight variation on the threshold voltage of the PMOS varactors do not affect considerably the circuit due to the large difference between the threshold voltage of the transistor and the high control voltage.

Figure 5.2: (a) Differential Output Voltage behavior. (b) Differential Output Voltage zoom view.



Source:Author

The power consumption corner analysis is presented in table 5.4. In the worst case, the DCO operates with a 405 mV VDD and a 490 µW power consumption. Even in the worst case, the DCO achieves the requirements of power consumption and the phase-noise. However, the tuning range is affected by the large transistor. The large transistor becomes necessary to achieve the required transconductance in order to satisfy both start-up and steady-state conditions without much increase in the current consumption. The problem is, even the effort on the weak inversion operation, the required transconductance to sustain an oscillation remains big. This happens due to the low parallel resistance of the inductor. The octagonal shape of the inductor also makes it difficult to achieve high inductance with a small size.

The comparison between this design and the state-of-art previously presented in table 2.1 shows a competitive VDD and power consumption, though with good phase-noise simulation results. It is important to observe that all designs in the table of state-of-art operate at higher frequencies than this work. Hence, the quality factor reachable is higher. Two designs uses an older process which, to one hand, requires higher voltages to complete the operation of system. However, to another hand, it requires less current consumption to achieves the necessary transconductance due to better gm to id characteristic.

Table 5.2: LC-Based DCO Power Reduction Analysis
Source:Author

i_f	VDD (V)	I_{M3}(mA)	Power(μW)	W_{M3}(μm)
0.25	0.355	0.500	177.5	570
5	0.530	0.852	451	48
25	0.710	1.17	831	16.8

Figure 5.3: Phase noise schematic simulation results of LC-based DCO.

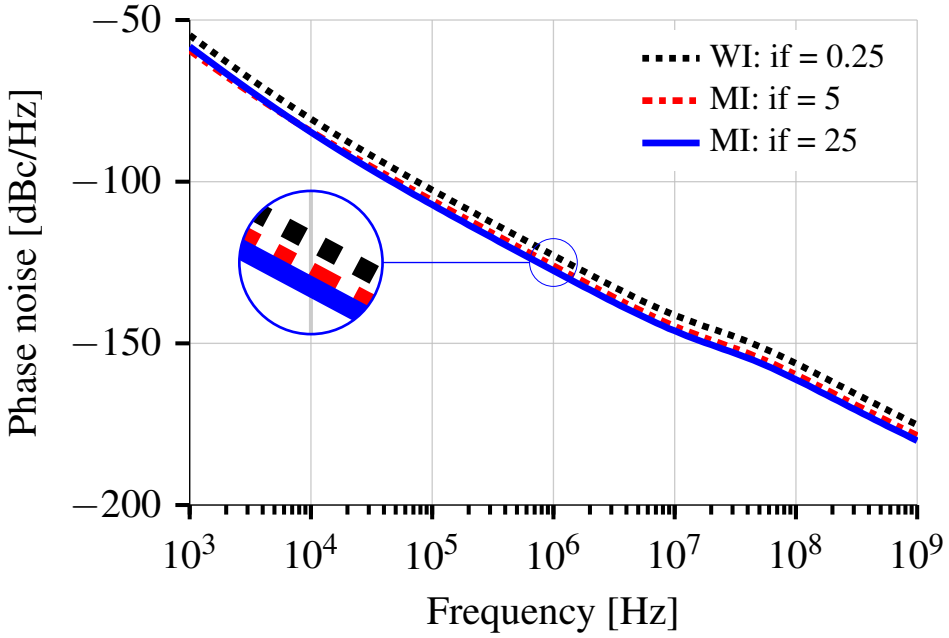


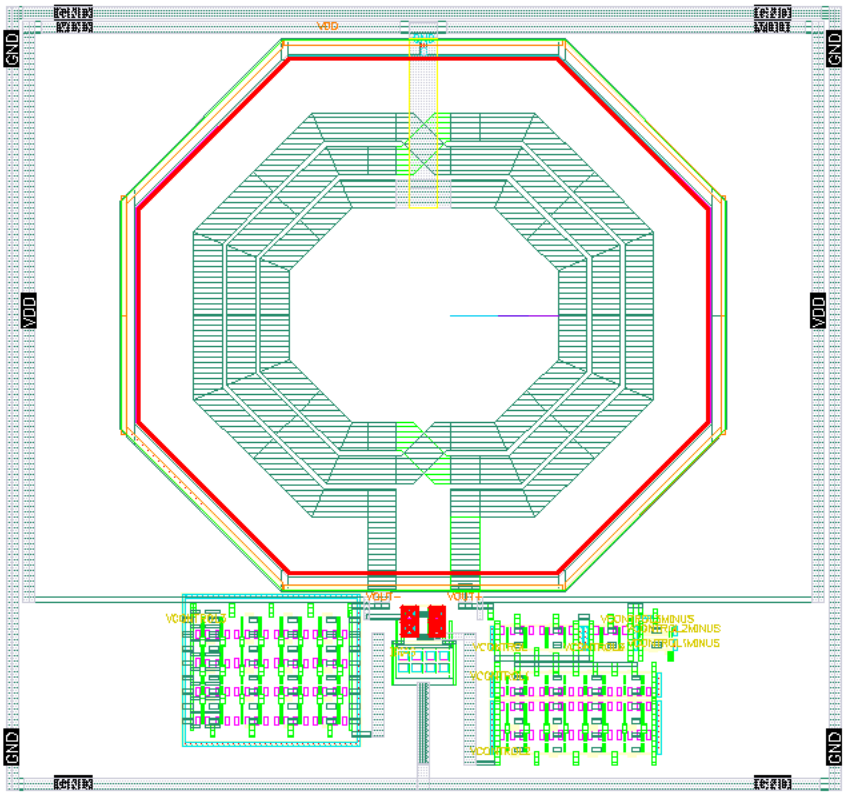
Table 5.3: LC-Based DCO Parameters
Source:Author

Parameter	Value
$(w/l)_{M1,M2}$	285 μm/40 nm
$(w/l)_{M3}$	570 μm/40 nm
L	3 nH
Cmin	1.32 pF @1.86 GHz
Cmax	2.06 pF @1.8 GHz

Table 5.4: LC-Based DCO Power Consumption Corner Analysis
Source:Author

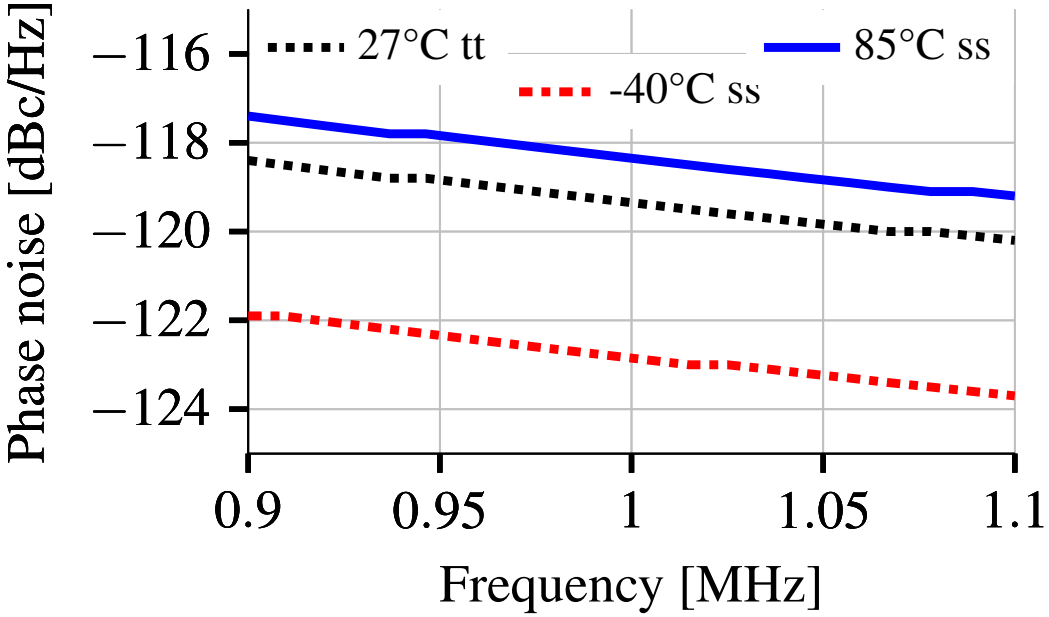
Temperature (°C)	27	-40	85
Corner	tt	ss	ss
VDD (mV)	395	405	405
Power (μW)	380	309	490
Phase Noise (dBc/Hz@1MHz)	-119.3	-122.8	-118.3

Figure 5.4: Layout of the proposed LC-based DCO



Source:Author

Figure 5.5: Phase noise post-layout simulation results of the LC-based DCO.



Source:Author

This design shows that the design methodology herein presented based on UICM model is a good alternative for low-power and low-VDD operation. The designed inductor-based DCO with phase-noise of -119.3 dBc/Hz at 1 MHz, 380 μW of power consumption

at 1.86 GHz and 0.395 V VDD, with a circuit area of 0.46 mm^2 meets the requirements of phase-noise and power consumption presented at the beginning of this chapter for the ADPLL to be designed later by other team. The DCO reaches 60 MHz of tuning range, which enables the application to the Wi-Fi HaLow standard. However, this tuning range do not cover the entire range of the specifications of Wi-Fi Halow standard. Low-power and low-VDD performance is kept even in corners operation, which makes this design also suitable for IoT applications.

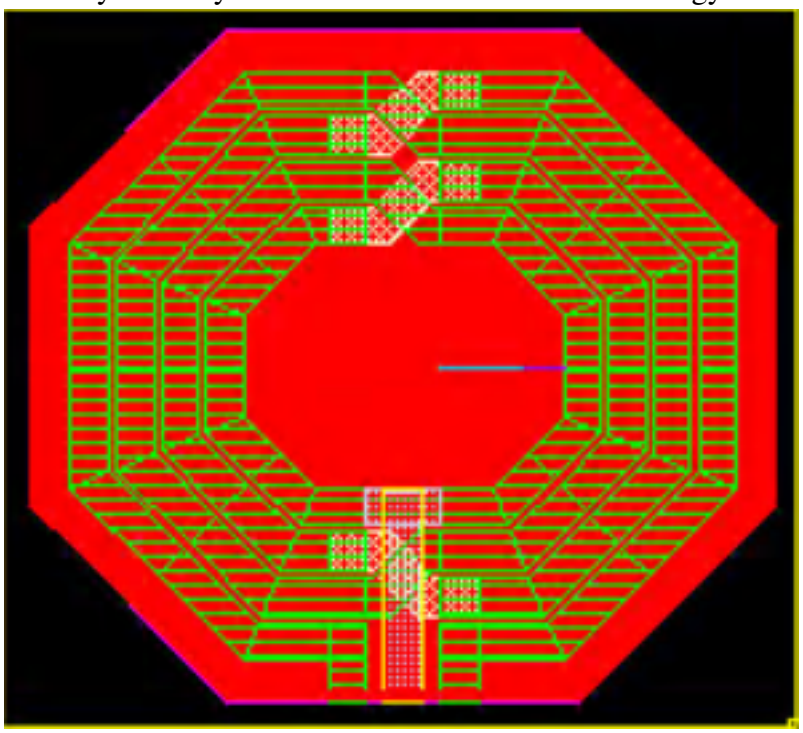
5.3 Transformer-Based DCO Design in 28nm

To improve the low power consumption of the oscillator, a second DCO design is developed herein, for the 28nm technology from TSMC. This new design uses a transformer instead of an inductor in the resonator, in order to increase the overall parallel resistance from the tank of the oscillator. However, first of all, it is necessary to compute the improvements on the design when the transformer is used instead of just the inductor. To do this, an inductor is first designed in this technology to compare the resulting losses from each one.

The inductor chosen for this analysis is the symmetric inductor available on the technology. This inductor is configured to achieve the maximum quality factor with an inductance of $4nH$ and with the minimum possible area. The inductor is configured with the maximum width to increase the quality factor. Furthermore, the device is composed of 4 turns to achieve the required inductance with a minimum area. The space between turns is the maximum possible in order to increase the self-resonance and, thus remains far from the operational frequency of the system. The layout of the inductor is presented in figure 5.6 and it size is 396.5μm.

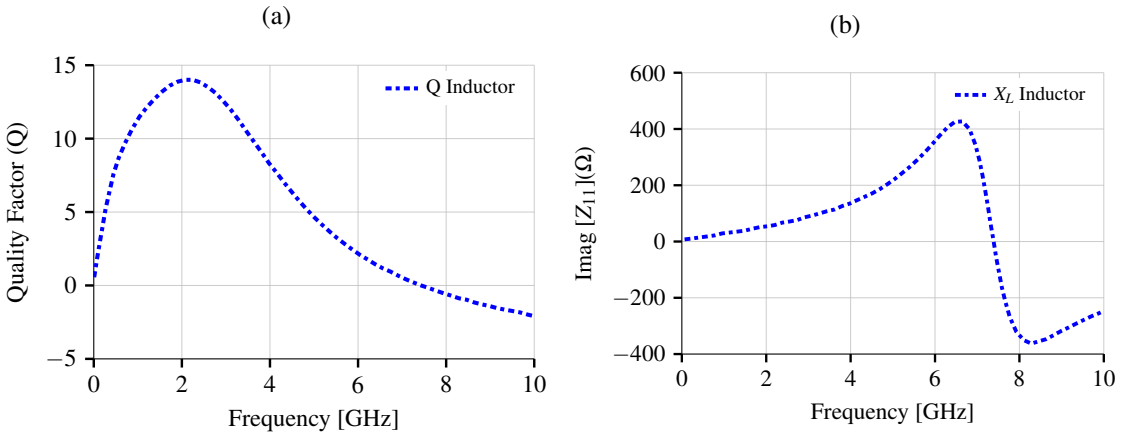
The simulation results of the inductor is presented in figure 5.7. The quality factor (Q) behavior with the frequency is observed in figure 5.7(a). The quality factor at 1.8 GHz is 13.6 which results in a parallel resistance of merely 616 Ω. The quality factor of inductor designed in 28 nm is less than the coil designed in 40 nm due to the decrease of the thickness of the top metals. The obtained self-resonance frequency is 7.4 GHz, which is far from the operational frequency as intended. The reactance of the inductive element can be observed in figure 5.7(b).

Figure 5.6: Layout of Symmetric Inductor in 28nm Technology from TSMC



Source:Author

Figure 5.7: (a) Quality factor behavior. (b) Imaginary part of Inductor impedance.

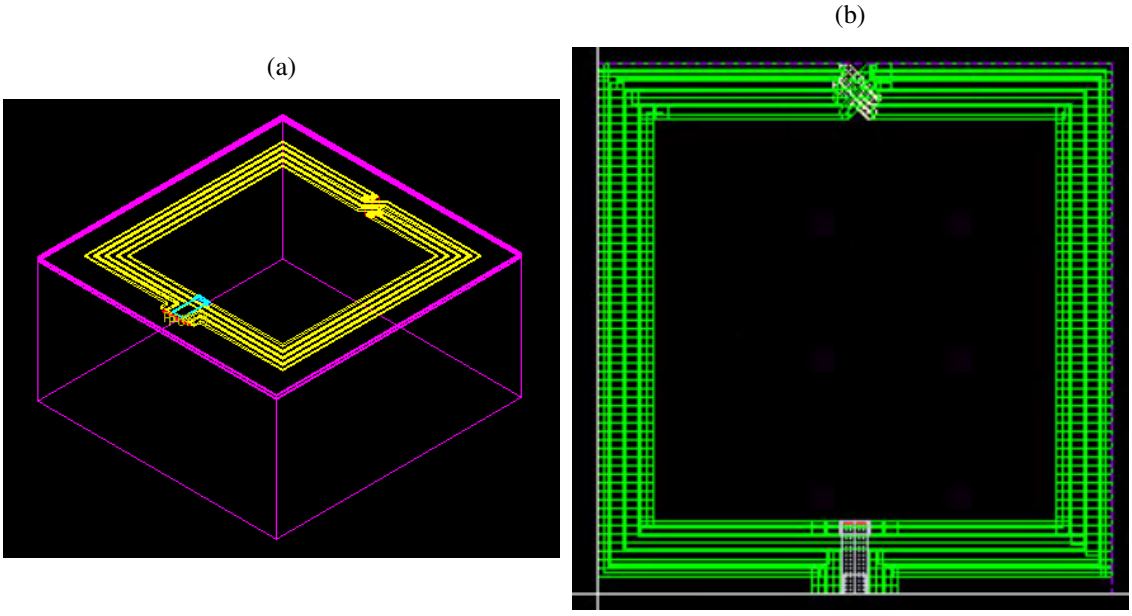


Source:Author

To increase the parallel resistance of the inductive element, a planar transformer was designed first in Cadence Tool to check the DRC rules, and after, it was simulated by electromagnetic simulation in ADS from Keysight. The transformer layout is planar, to achieve the same as possible loss condition in both coils. The width of both coils is 12 μm to achieve a good quality factor on both, without decrease considerably the coupled factor. The primary and secondary was designed with 2 turns to increase the inductance of the primary and the coupled factor between both coils.

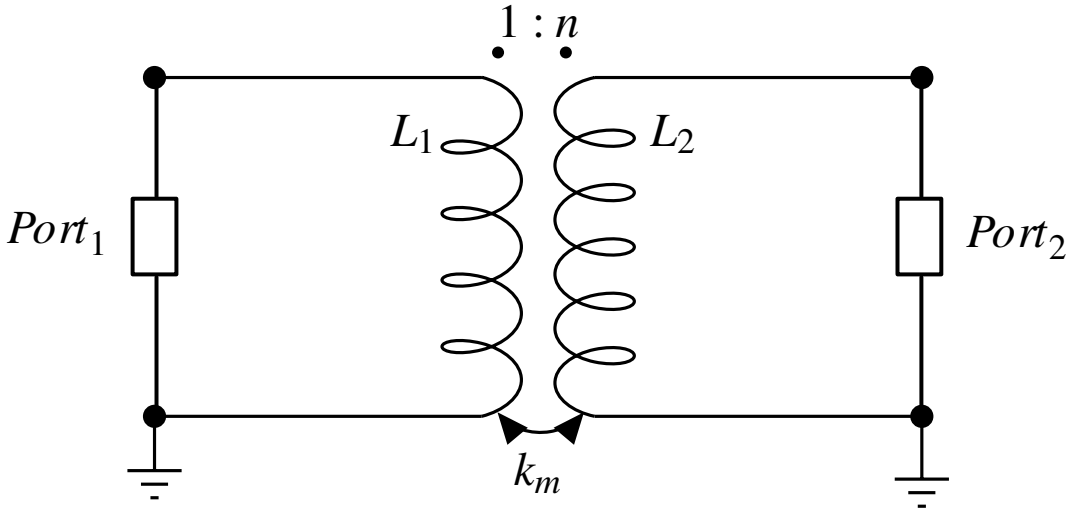
The increase of numbers of turns decrease the quality factor due to the metal crossing. The primary and secondary was designed in metal 9 with the metal 8 as the crossing metal due to the higher thickness and better sheet resistance of these metals. To performer the center-tap, the metal AP is choosed also due to its good losses characteristics. Figure 5.8 shows the layout of the transformer in Cadence and its 3D view on the EM simulation from ADS.

Figure 5.8: (a) 3D view of the transformer on EM Simulation. (b) Layout of the Transformer on Cadence.



Source: The Author

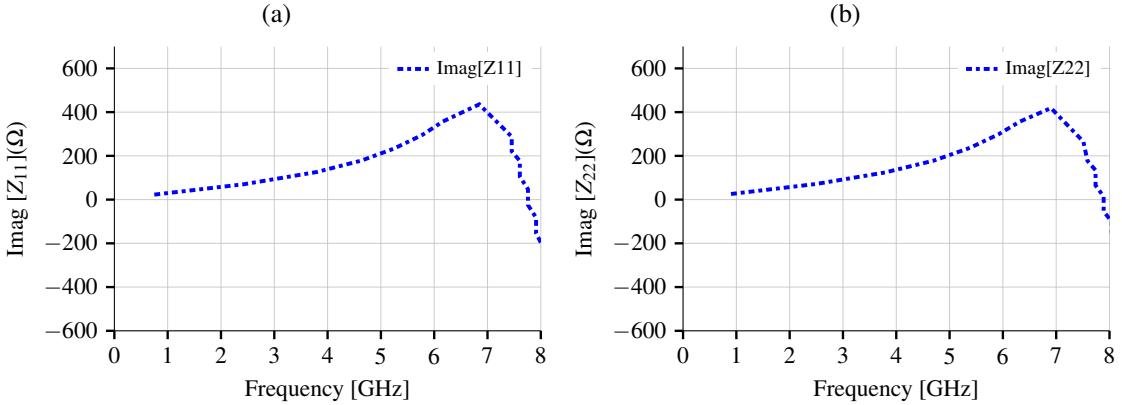
Figure 5.9: Setup for 2-port EM Simulation of the Transformer.



Source:Author

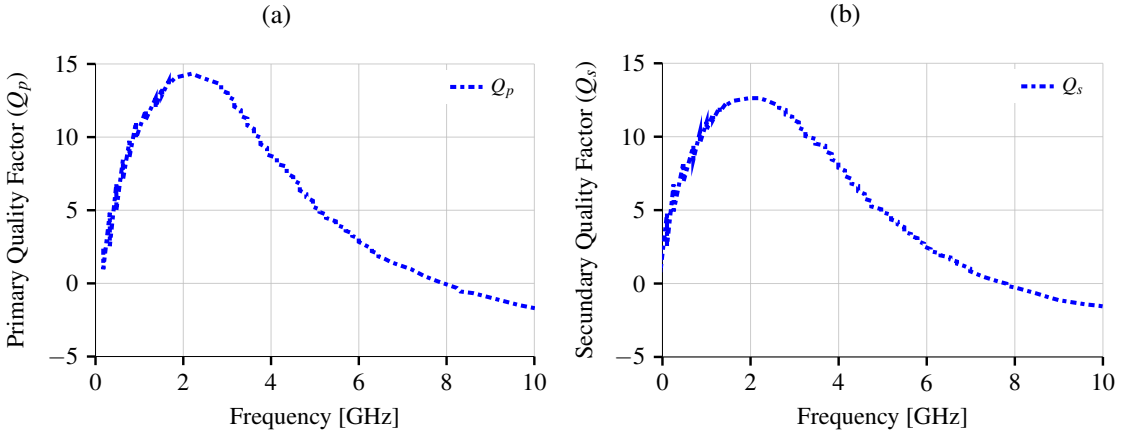
The transformer was simulated in a 2-port electromagnetic simulation in a configuration that shows Figure 5.9. Where L_1 and L_2 represents the primary and secondary coil respectively.The simulation results, which figure outs the imaginary part of impedance and the quality factors of each coil, are presented in the Figures 5.10 and 5.11 respectively.

Figure 5.10: (a)Imaginary Part of Z11 . (b) Imaginary Part of Z22



Source:Author

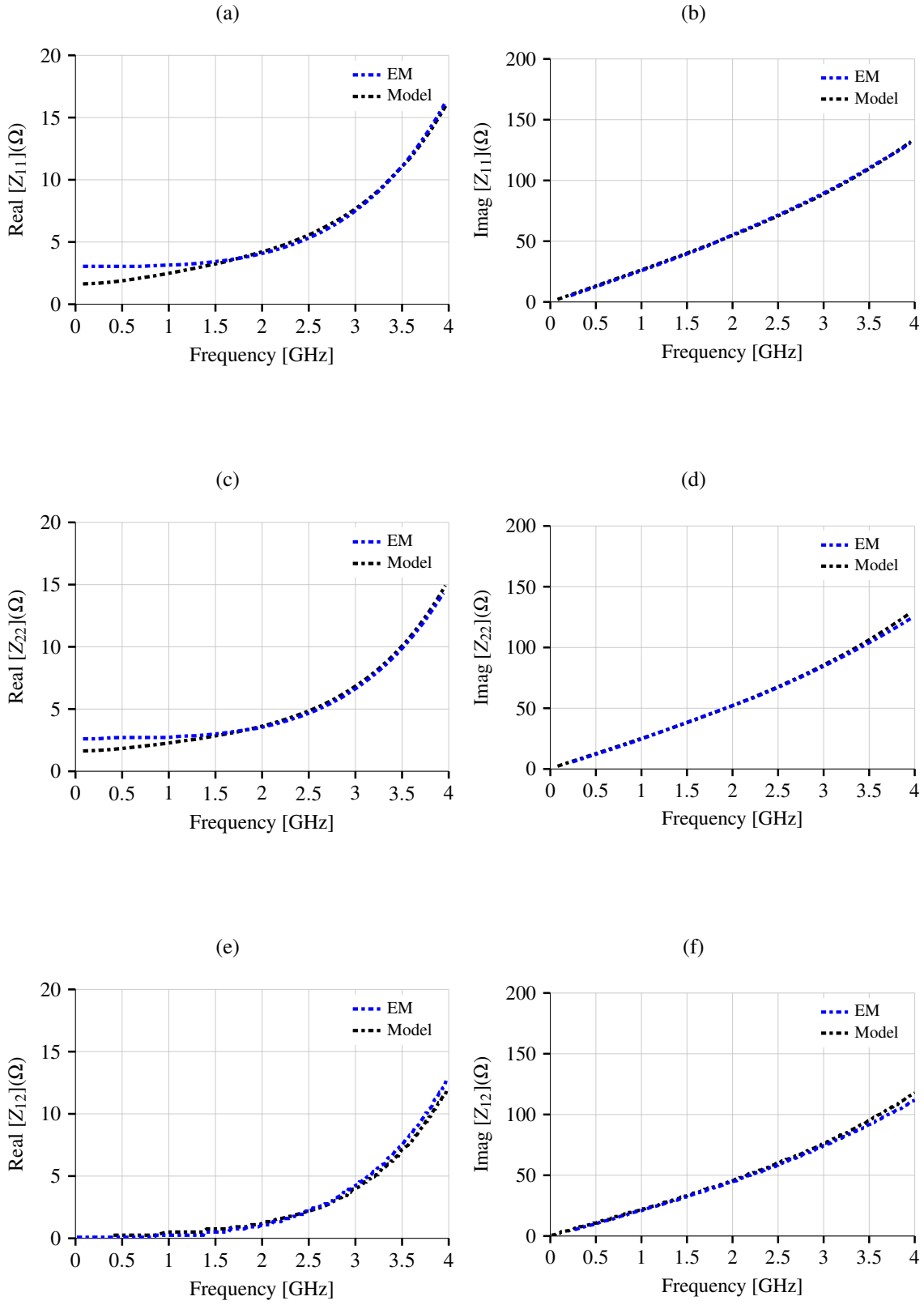
Figure 5.11: (a) Primary Quality Factor. (b) Secondary Quality Factor



Source:Author

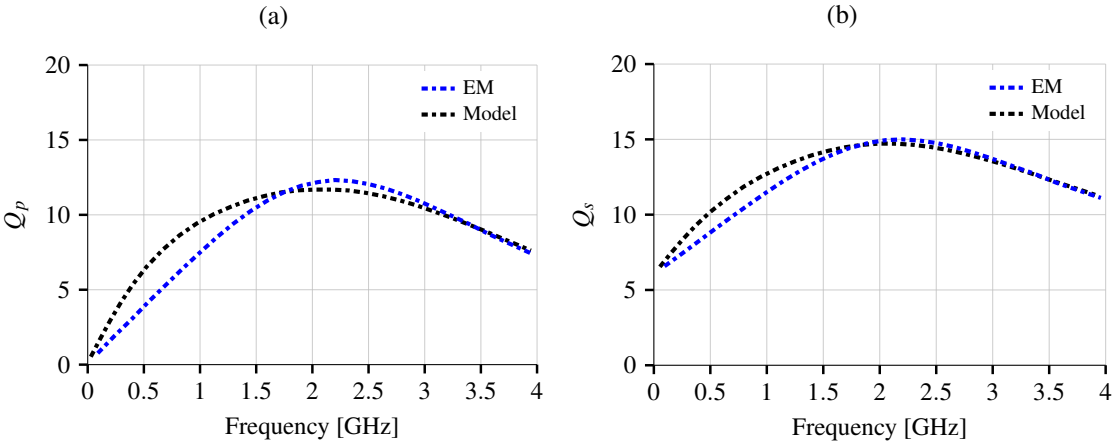
The extracted inductance of the primary and secondary are 4.15 nH and 4.37 nH, respectively. The quality factors obtained at 1.8 GHz are 14.35 for the primary coil and 12.64 for the secondary coil. Table 5.5 summarizes the final parameters of the transformer. The time domain model was extracted by using the methodology described previously. The comparison between the electromagnetic simulation and the time domain model is illustrated in the Figures 5.12 and 5.13. These results prove a good agreement between the two simulations that were performed by the author.

Figure 5.12: Comparison between EM simulations of the Transformer layout and the time domain model.



Source:Author

Figure 5.13: (a) Primary Quality Factor Plot. (b) Secondary Quality Factor Plot.



Source:Author

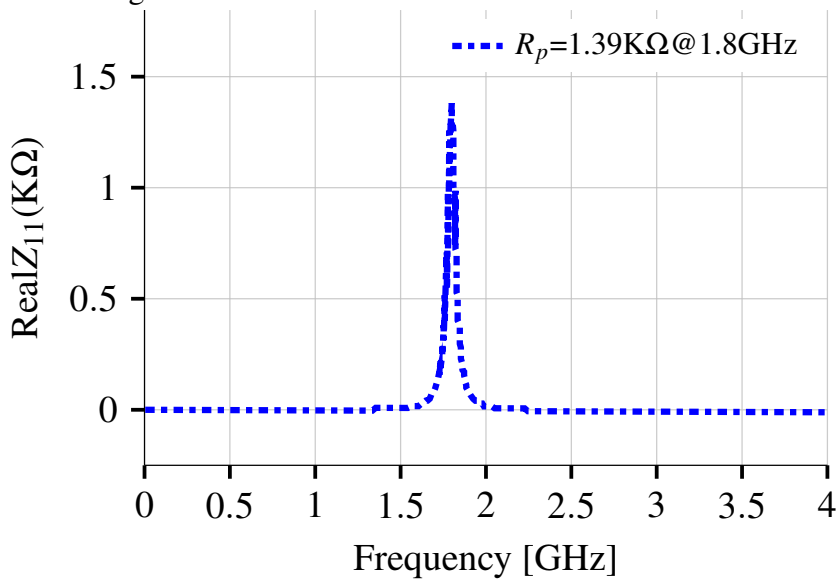
Table 5.5: Transformer Parameters

Source:Author

Parameter	Value
width of L1	12μm
width of L2	12μm
turns of L1	2
turns of L2	2
Outer Diameter	500μm
L1	4.15 nH
L2	4.37 nH
Q1	14.35
Q2	12.64
k_m	0.835
Main Metal	M9
Crossing Metal	M8
Center-tap Metal	AP

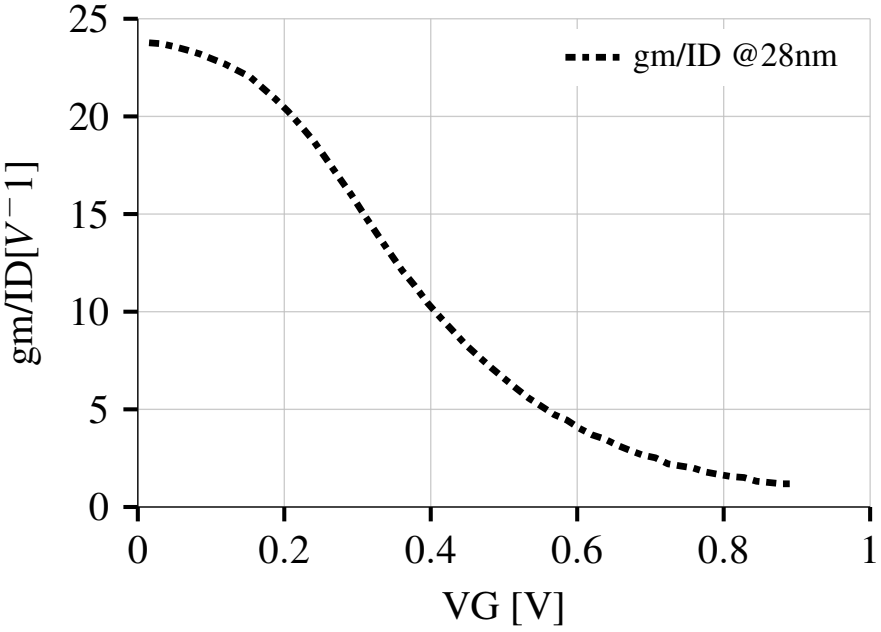
To compute the parallel resistance of the transformer, the time-domain model is simulated with Cadence with ideal capacitors on each side of the transformer in order to resonate at 1.8GHz. Figure 5.14 shows the result of this analysis. The parallel resistance achieved in this design is 1.39KΩ, which represents more than double of the equivalent resistance of the single inductors designed in both the 40 nm and 28 nm commercial CMOS technologies. These results confirm that the transformed-based oscillator is a good choice to improve the DCO power consumption.

Figure 5.14: Parallel Resistance from Transformer



Source:Author

Figure 5.15: VG to gmg/id plot in a 28nm technology

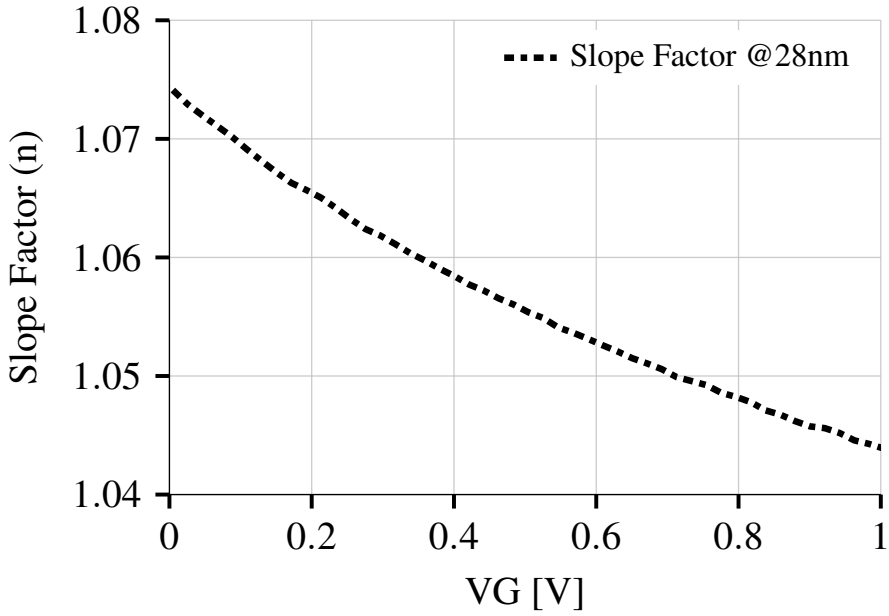


Source:Author

In the next step, the parameters of the NMOS transistor were extracted in order to start the oscillator design. Figure 5.15 shows the curve of the gm to id ratio. It is possible to observe that the maximum level of the gm to id curve is slightly below that obtained from the 40 nm technology. This is due to the shorter channel length of the transistor considered in Figuer 5.15 . The equilibrium threshold voltage extracted for this 28nm

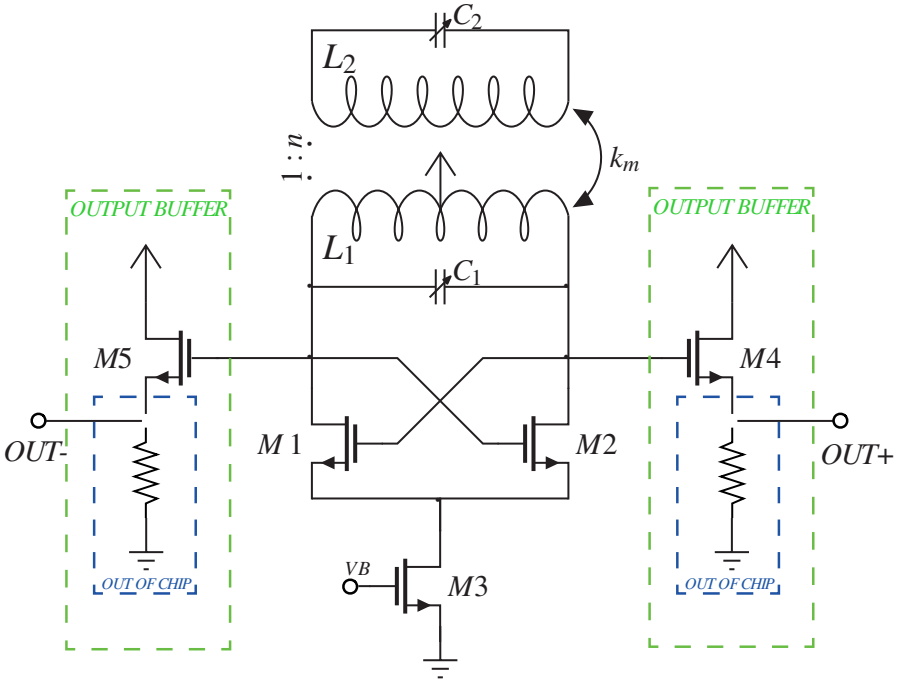
NMOS is 353.32 mV. In addition, the variation of the slope factor with the gate bias is presented in Figure 5.16.

Figure 5.16: VG to n plot in a 28nm technology



Source:Author

Figure 5.17: Schematic of Proposed Transformer Based DCO with Output Buffers.

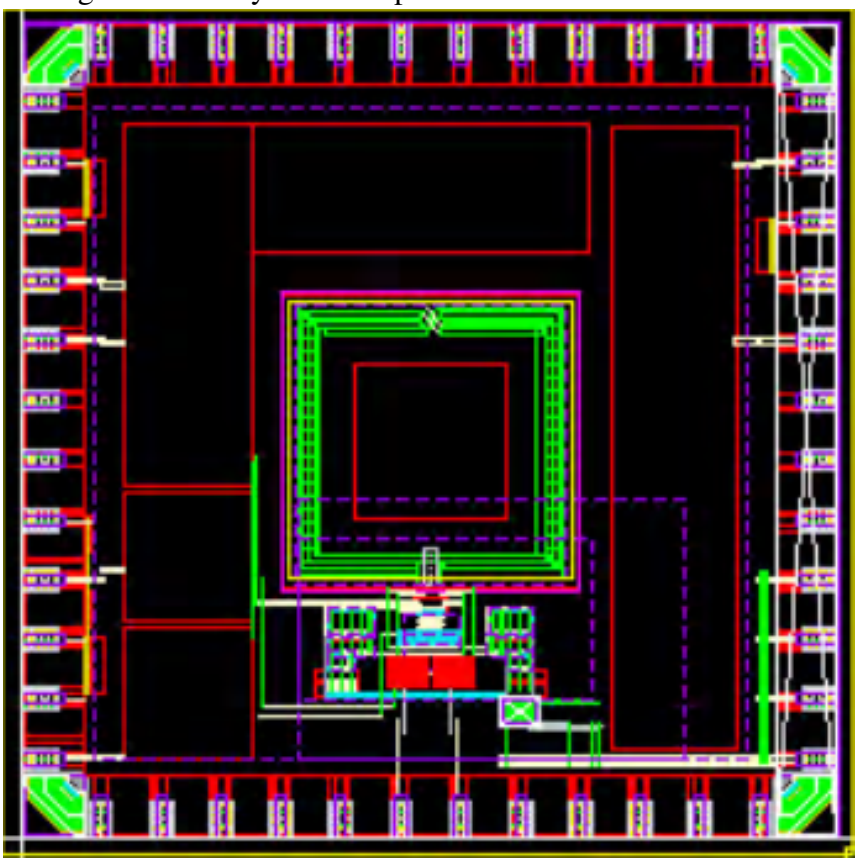


Source:Author

The DCO is designed following the methodology proposed previously. It is done after the transistor parameters are extracted and the transformer is designed, in order to

optimize the DCO for power reduction. Furthermore, the final goals of this master thesis are the design, validation, fabrication and measurements of the 28nm oscillator. For such a prototyping, an output buffer is placed on each side of the oscillator to decrease its output impedance and to deliver the maximum output voltage level to the load. To increase the output power, the buffers are biased by a 0.9 V supply voltage. The current bias of the buffers is made by an external resistor, which in the real measurements will be replaced by a variable resistor in order to have possible adjustments for the measurements after fabrication. The final schematic of the oscillator is presented in Figure 5.17. In addition, the final parameters of the DCO are shown in the Table 5.6. The final die layout, suitable for fabrication - which was not possible to finalize at the time of this writing - has 2.26mm^2 with the pads. The final layout is illustrated in Figure 5.18.

Figure 5.18: Layout of Proposed Transformer-Based DCO.



Source:Author

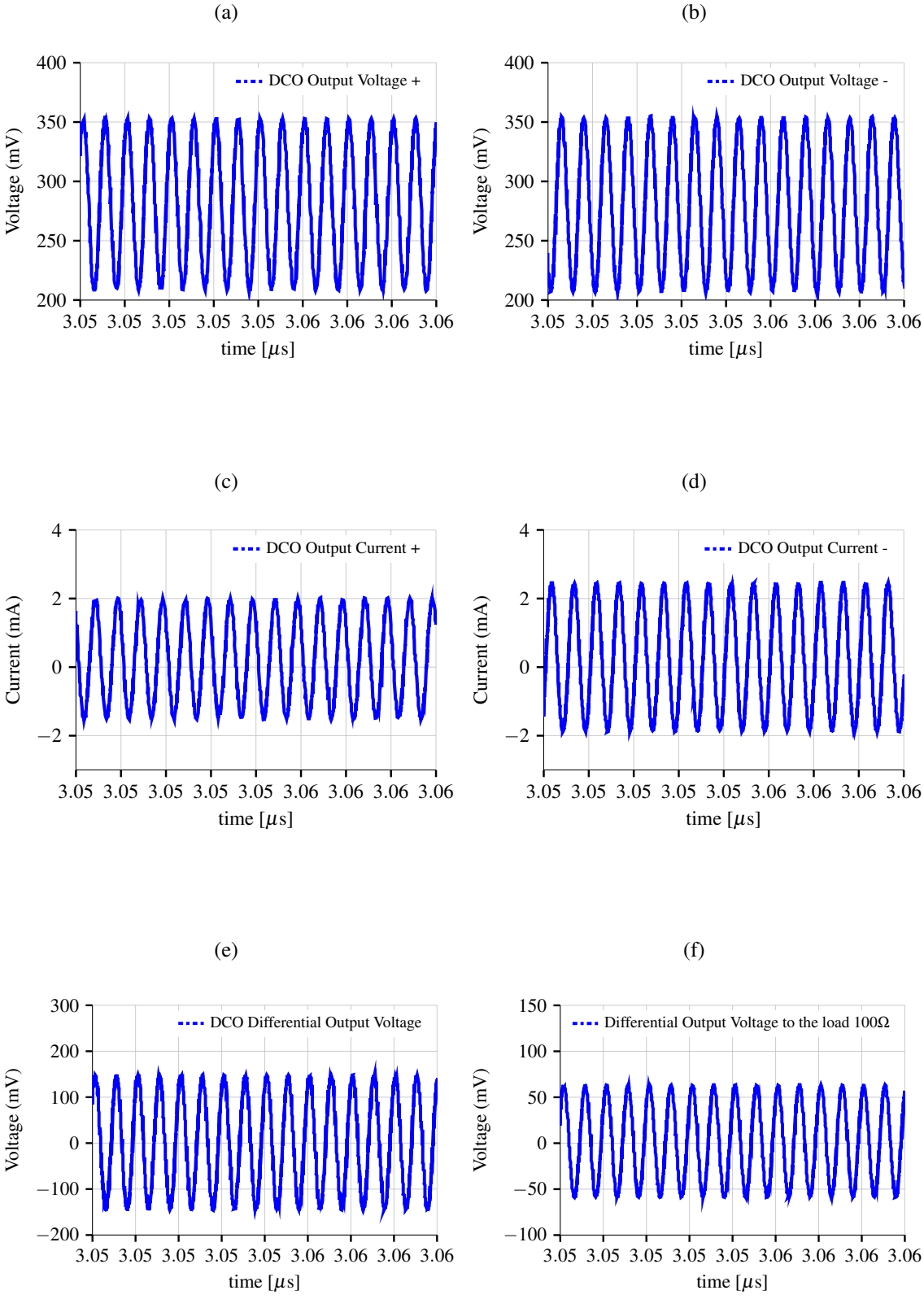
Table 5.6: The transformer-Based DCO Parameters
Source:Author

Parameter	Value
$(w/l)_{M1,M2}$	144 μm/28 nm
$(w/l)_{M3}$	288 μm/28 nm
L1	4.15 nH
L2	4.37 nH
C1min	1.25 pF @1.86 GHz
C1max	1.71 pF @1.74 GHz
C2min	1.25 pF @1.86 GHz
C2max	1.71 pF @1.74 GHz

The final implementation of the capacitor bank has 5 bits to control the capacitance on each side of the transformer, which enables the oscillator to cover the entire band of interest for 802.11ah with the selected resolution. The DCO varies the frequency from 1.74 to 1.86 GHz, which results in a 120 MHz of frequency range. The power consumption and phase-noise are computed at the 1.86 GHz frequency. At this frequency, the 28nm DCO achieves a power consumption of just 97μw under a 0.280 V of power supply. The transient response of the oscillator is presented in figure 5.19. The vout+ and vout- correspond to the positive and negative voltages across the tank. Hence, the DCO differential output voltage represents the differential portion of this voltage. The DCO output currents also refer to the current from the tank. In addition, the differential output voltage to the load correspond to the output signal from buffers to a 100 Ω load. Finally, the post-layout simulation for the DCO phase-noise results in -101.95 dBc/Hz, which satisfies the required specification for the WiFi HaLow standard operation.

The power consumption and phase-noise post-layout simulations results are presented in the Table 5.7. The achieved power consumption results show very competitive results even at the worst-case corner. At the same time, the worst-case corners analysis presents a result higher than defined by the specifications at the beginning of this chapter. However, the phase-noise specification was more demanding than the minimum acceptable, for a robust operation after fabrication. The worst case result is inside of the calculated to WiFi HaLoW standard. The shape of phase-noise at each corner is presented in Figure 5.20.

Figure 5.19: Transient Response of the Transformed-Based DCO



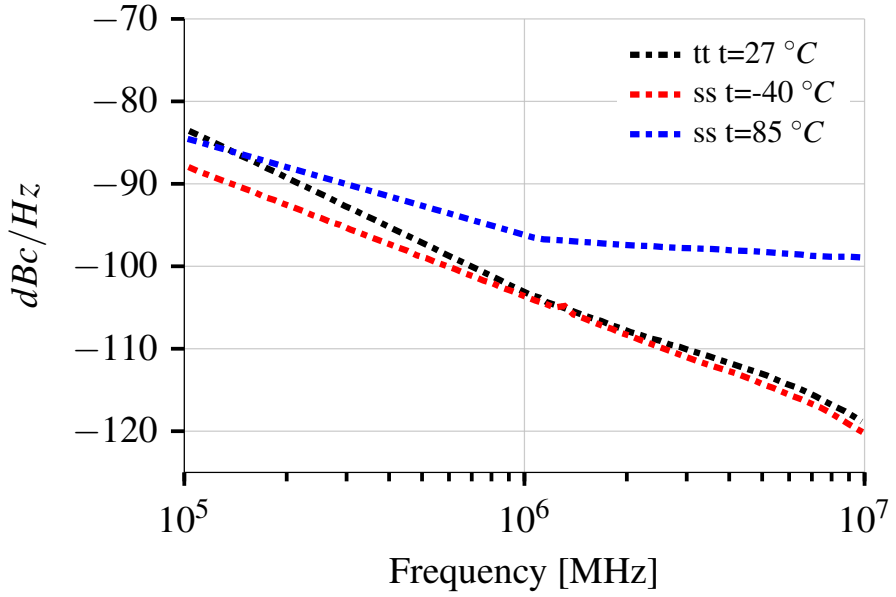
Source:Author

Table 5.7: Transformer Based DCO Power Consumption Corner Analysis

Source:Author

Temperature (°C)	27	-40	85
Corner	tt	ss	ss
VDD (mV)	280	330	330
Power (μW)	97	86	126
Phase Noise (dBc/Hz@1MHz)	-101.95	-102.92	-95.54

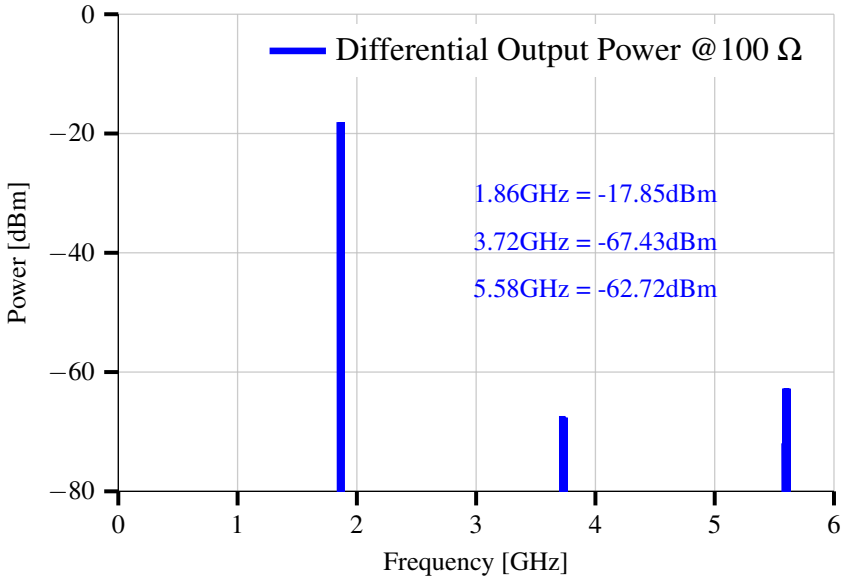
Figure 5.20: Phase Noise Corners Analysis of Transformer-Based DCO



Source:Author

The spectrum of the output power delivered to the load is presented on the figure 5.21. In the required operation frequency the differential output power is -17 dBm which is sufficient to the measurements. The second and third harmonics presents much less power, which shows a very selective behavior from the designed oscillator.

Figure 5.21: Spectrum of Output Power delivered to the Load



Source:Author

A comparison with the state-of-art is presented in Table 5.8. The power consumption of our transformed-based DCO design is very competitive. This shows that the topology proposed and designed based on the UICM transistor model for sizing is very useful to achieve very low power consumption and low $V_D D$ operation. In addition, the inductor-based resonator also presents competitive results for power consumption without compromising the phase-noise. The comparison with the state-of-art shows that the main goal of this work was achieved, namely to reach a very low power consumption with an improved basic DCO topology. All the other low power designs listed in Table 5.8 and close to the state-of-art, use new topologies which were presented in Chapter 2, in order to achieve low power figures.

When the transformed-based DCO is compared with the state-of-art by means of the main figure-of-merit (FOM), it does not present as good figures in the comparison. When the metric used is such FOM, the main impact in it is related to the phase-noise performance, while the power consumption does not impact so much this FOM. Such comparison is not very appropriate since the power consumption is the main goal of this work. The same happens when PFN is the metric used to compare the transformed-based DCO with other works, the design does not achieve also competitive results for PFN. This happens due to the squared term in the equation, which is a relation between the central frequency to the frequency offset considered. This results that the circuit designs which operate with a higher tuning range to operational frequency relation are prone to achieve

better figures, as in the first figure-of-merit.

The inductor-based DCO presents in general better results if compared by means of the main FOM metric. This occurs because the phase-noise is considerably better than most of the presented state-of-art works in Table 5.8. Furthermore, the power consumption is also increased considerably in comparison to the transformed-based design. In view of these results, the impact of the low frequency of operation is compensated.

When the new proposed figure-of-merit, presented in chapter 3, is used to compare the transformed-based DCO to state-of-art the results are very competitive. The transformed-based DCO presents better results than most of the state-of-art designs. Only two designs, which presents better phase noise with very close power consumption, shows better results. These two designs presents a higher frequency of operation, which results in a better quality factor to the resonator.

Table 5.8: Comparison with the State of Art
Source:Author

	Transformer-based	LC-based	I*	II*	III*	IV*	V*	VI*
Process (nm)	28	40	180	65	28	16	40	180
Phase Noise (dBc/Hz)	-101.95 @1MHz	-119.3 @1MHz	-104 @1MHz	-107 @1MHz	-119 @1MHz	-134 @10MHz	-139 @10MHz	-106 @400kHz
Frequency (GHz)	1.86	1.86	4.5	2.46	2.24-2.6	3.2-4.0	4.8	2.63
VDD (V)	0.28	0.395	0.2	0.45	0.2	0.2	0.5	0.45
Power (mW)	0.097***	0.380***	0.114***	0.107***	0.67***	0.6***	0.48***	0.43***
FOM	-177.47	-188.89	-186.49	-184.52	-189.04	-188.26	-194.23	-186.02
PFN(dB)	3.64	15.06	12.66	10.69	15.21	14.43	20.40	12.19
FOM_{Pdc}	-201.85	-195.48	-208.77	-207.62	-188.23	-188.89	-197.77	-191

*Measurement Results **Simulation Results ***Without Output Buffer
I-(OKADA et al., 2009)
II-(LIU et al., 2019)
III-(YANG et al., 2019)
IV-(LI et al., 2017)
V-(BABAIE; SHAHMOHAMMADI; STASZEWSKI, 2015b)
VI-(LEE; MOHAMMADI, 2007b)

6 CONCLUSION AND FUTURE WORKS

This Master´s work intended to cover the study and implementation of the low power design of digitally controlled CMOS oscillators suitable to serve in the RF front-end of WiFI HaLow compliant systems. The goal and motivation were discussed in chapter 1. In chapter 2 a brief introduction to frequency synthesizers and phase locked loops are presented. The main characteristics of the digitally controlled oscillators are also discussed. A review of the state-of-art prior works, aiming to compare with this M.Sc. thesis work, is also presented in Chapter 2. Hence, a topology to solve the power consumption issue without decreasing the oscillator phase-noise is chosen and proposed as the main design target of this work.

The transformer based resonator characteristics, which is one of the contributions of this work, are addressed in chapter 3. The principles of operation, together with the proposed time-domain model characteristics of the transformer, are also presented and discussed in this chapter.

The low power DCO design methodology based on the UICM model, which accounts for the physics characteristics of the transistor and describes all operating regions of the device, was finally presented in chapter 4. This chapter also covers the transistor and transformer extraction parameters methodology. The transistor equation and methodology for sizing were also addressed.

Finally, chapter 5 presented two DCO designs developed by the author, in two different CMOS technologies, to show the impact of the UICM model based design methodology in two cases: with an inductor-based resonator and with a transformer-based one. The inductor-based was designed in a commercial 40 nm CMOS bulk technology, while the transformer-based DCO was designed for fabrication in a 28 nm CMOS bulk technology.

The inductor-based designed DCO achieves phase-noise of -119.3 dBc/Hz at 1 MHz, 380 µW of power consumption at 1.86 GHz and 0.395 V VDD, with a circuit area of 0.46 mm2. These were obtained with post-layout and extracted electrical simulations. This DCO reaches 60 MHz of tuning range, which enables the application to the Wi-Fi HaLow Standard. Low-power and low-VDD performance is kept even in corners operation, which makes this design also suitable for IoT applications.

In the transformer-based DCO, the inductor of the classical LC topology was replaced by a transformer to improve both performance and power consumption. The de-

signed DCO achieves phase-noise of -101.95 dBc/Hz at 1 MHz offset, 97 μW of power consumption under typical PVT at 1.86 GHz and 0.280 V VDD operation, with a circuit area of 2.26 mm^2 with buffers and PADS. DCO extracted simulations show 120 MHz of tuning range. Low-power and low-VDD performance is demonstrated to hold even in operation at worst case corners, which makes this design more suitable for IoT applications than the first one. Both DCO designs developed show competitive results in phase-noise and power consumption.

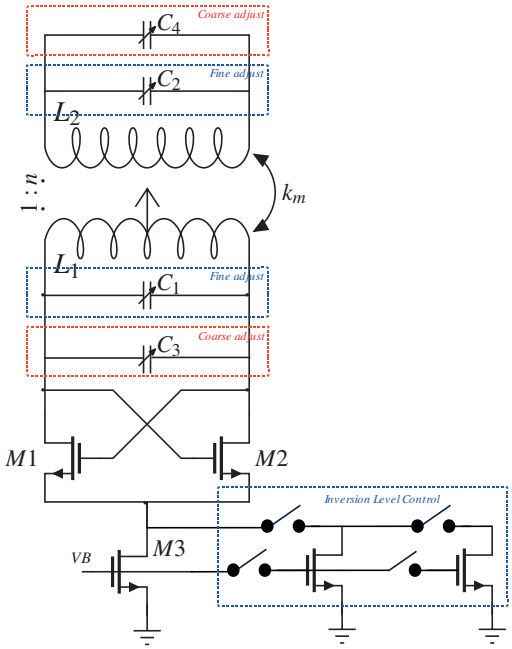
For future works, an improvement in the designed transformer-based DCO is proposed, in order to make this circuit architecture most robust to process variations. The first improvement is to increase the frequency range and frequency steps by increasing the number programming of bits. Two capacitors banks on each side of the transformer is proposed. The first one is composed by MOM capacitors to perform coarse adjusts. Then, the fine frequency adjustment is performed by the varactors as binary switchable capacitances, as presented previously in this work. The coarse adjustment is proposed to be made by MOM capacitors due to their better process variability characteristics. Furthermore, with the process variation corrections made by the MOM capacitors bank, then the fine adjustment can be made satisfactorily by the varactors.

The operation in weak inversion for the transistors in the DCO can becomes a concern for startup problems. Due to the exponential relation between current and voltage of the devices in this regime, then any slight variation in the threshold voltage of transistors incurs in a high variation of the MOSFET drain current. Hence, some circuits post-fabrication may have a startup problem, which can result in the absence of oscillation in the DCO. To solve this issue, an inversion level control added to the DCO is to be explored in proposed future works. The inversion level is controlled by the multiplicity of the tail transistor. To increase or decrease its current capability at start-up, switches are proposed to be placed in the circuit, to add or remove transistors in parallel with the tail transistor.

The phase-noise of the transformed-based DCO can also be improved to cover other applications. As discussed in this work, the phase noise is inversely proportional to the power consumption. Therefore, to improve the phase-noise the oscillator power consumption must be increased. Hence, the tail transistor current must be also increased. To perform this, the tail transistor must be increased in its width. Consequently, the inversion level control previously referred also can solve this issue. Figure 6.1 shows this new proposed topology for future work.

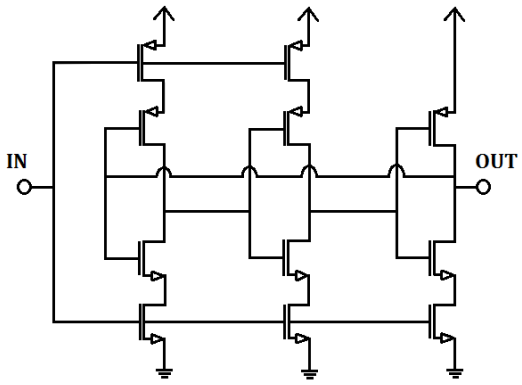
Another required future implementation and addition to the presented work is the inclusion of a divider-by-2 circuit. The divider is necessary to place the oscillator into an ADPLL, together with the time-to-digital converter and the other ADPLL blocks. A low power divider topology presented in (BA; SALIMI; MATEMAN, 2017) is chosen due to the low power goal of this work. The topology is based on a three stage ring oscillator as Figure 6.2 shows.

Figure 6.1: Future Transformer-Based DCO Topology to decrease the process variations impact



Source:Author

Figure 6.2: Low Power Divider by 2 Topology.



Source:Adapted from(BA et al., 2018)

REFERENCES

ADAME, T. et al. Ieee 802.11ah: The wifi approach for m2m communications. **IEEE Wireless Communications**, v. 21, p. 144–152, 12 2014.

ANDRADE, N. et al. Low power ieee 802.11ah receiver system-level design aiming for iot applications. In: 2017 30TH SYMPOSIUM ON INTEGRATED CIRCUITS AND SYSTEMS DESIGN (SBCCI). [S.l.]: IEEE, 2017.

BA, A.; SALIMI, K.; MATEMAN, P. A 4mw-rx 7mw-tx ieee 802.11ah fully-integrated rf transceiver. In: 2017 IEEE RADIO FREQUENCY INTEGRATED CIRCUITS SYMPOSIUM (RFIC). [S.l.]: IEEE, 2017.

BA, A. et al. A 4mw-rx 7mw-tx ieee 802.11ah fully-integrated rf transceiver. In: 2017 IEEE RADIO FREQUENCY INTEGRATED CIRCUITS SYMPOSIUM (RFIC). [S.l.]: IEEE, 2018.

BABAIE, M. et al. A Fully Integrated Bluetooth Low-Energy Transmitter in 28 nm CMOS With 36% System Efficiency at 3 dBm. **IEEE Journal of Solid-State Circuits**, v. 51, n. 7, p. 1547 – 1565, 2016. ISSN 1558-173X.

BABAIE, M.; SHAHMOHAMMADI, M.; STASZEWSKI, R. B. A 0.5 v 0.5 mw switching current source oscillator. In: 2015 IEEE RADIO FREQUENCY INTEGRATED CIRCUITS SYMPOSIUM (RFIC). [S.l.]: IEEE, 2015.

BABAIE, M.; SHAHMOHAMMADI, M.; STASZEWSKI, R. B. A 0.5V 0.5mW switching current source oscillator. In: 2015 IEEE Radio Frequency Integrated Circuits Symposium (RFIC). [S.l.]: IEEE, 2015. p. 183 – 186.

BAEK, D. et al. Analysis on Resonator Coupling and its application to CMOS Quadrature VCO at 8 GHz . In: 2003 IEEE Radio Frequency Integrated Circuits Symposium (RFIC). [S.l.]: IEEE, 2003. p. 85 – 88.

BERTULETTI, S. et al. Indoor distance estimated from bluetooth low energy signal strength: comparison of regression models. In: 2016 IEEE SENSORS APPLICATIONS SYMPOSIUM (SAS). [S.l.]: IEEE, 2016.

BOUZERARA, L.; ELAROUSSI, M. Low-voltage, low-power and highly-tunable 1.8GHz CMOS LC voltage controlled oscillator. In: **International Symposium on Signals, Circuits and Systems, 2005. ISSCS 2005**. [S.l.: s.n.], 2005.

CHEN, H.-H. et al. Accurate Systematic Model-Parameter Extraction for On-Chip Spiral Inductors. In: **IEEE TRANSACTIONS ON ELECTRON DEVICES**. [S.l.: s.n.], 2008. v. 55, n. 11, p. 3267–3273.

CHEN, P. et al. Design and built-in characterization of digital-to-time converters for ultra-low power ADPLLs. In: **European Solid-State Circuits Conference**. [S.l.]: IEEE Computer Society, 2015. v. 2015-Octob, p. 283–286. ISBN 9781467374705. ISSN 19308833.

CHENG, H.-C. et al. A Generic Model for NFC-based Mobile Commerce . In: IEEE 2009 11th International Conference on Advanced Communication Technology. [S.l.]: IEEE, 2009. p. 2009–2014.

CHERNYSHEV, M. et al. Internet of things (iot): Research, simulators, and testbeds. In: 2018 IEEE INTERNET OF THINGS JOURNAL. [S.l.]: IEEE, 2017. p. 1637 – 1647.

CHEUNG, T. S. D.; LONG, J. R. Shielded passive devices for silicon-based monolithic microwave and millimeter-wave integrated circuits. In: IEEE JOURNAL OF SOLID-STATE CIRCUITS. [S.l.]: IEEE, 2006. p. 1183–1200.

CHILLARA, V. K. et al. An 860 uW 2.1-to-2.7GHz All-Digital PLL-Based Frequency Modulator with a DTC-Assisted Snapshot TDC for WPAN (Bluetooth Smart and ZigBee) Applications. In: 2014 IEEE International Solid-state Circuits Conference (ISSCC). [S.l.]: IEEE, 2014. p. 172–174.

Cunha, A.; Schneider, M.; Galup-Montoro, C. An MOS Transistor Model for Analog Circuit Design. **IEEE Journal of Solid-State Circuits**, v. 33, n. 10, p. 1510–1519, 1998. ISSN 0018-9200.

EL-GHARNITI, O.; KERHERVE, E.; BEGUERET, J.-B. Characterization of Si-Based Monolithic Transformers with Patterned Ground Shield. In: 2006 IEEE RADIO FREQUENCY INTEGRATED CIRCUITS SYMPOSIUM (RFIC). [S.l.]: IEEE, 2006.

EL-GOUHARY, A.; NEIHART, N. M. Analysis of transformer-based resonator quality factor and bandwidth and the implications to vcos. In: 2011 IEEE INTERNATIONAL SYMPOSIUM OF CIRCUITS AND SYSTEMS (ISCAS). [S.l.]: IEEE, 2011.

ELARABI, T.; DEEP, V.; RAI, C. K. Design and Simulation of State-of-Art ZigBee Transmitter for IoT Wireless Devices. In: 2015 IEEE International Symposium on Signal Processing and Information Technology (ISSPIT). [S.l.]: IEEE, 2015. p. 297–300.

FERREIRA, L. et al. Review on the Evolution of Low-power and Highly-linear Time-to-Digital Converters - TDC. In: 2019 IEEE Latin American Symposium on Circuits and Systems (LASCAS). [S.l.]: IEEE, 2019.

FERRO, E.; POTORT, F. BLUETOOTH AND WI-FI WIRELESS PROTOCOLS: A SURVEY AND A COMPARISON. In: **IEEE Wireless Communications**. [S.l.: s.n.], 2005. v. 12, n. 1, p. 12–26.

Fiorelli, R.; Peralias, E. J.; Silveira, F. LC-VCO Design Optimization Methodology Based on the g_m/I_D Ratio for Nanometer CMOS Technologies. **IEEE Transactions on Microwave Theory and Techniques**, v. 59, n. 7, p. 1822–1831, July 2011. ISSN 0018-9480.

Fiorelli, R.; Peralias, E. J.; Silveira, F. LC-VCO Design Optimization Methodology Based on the g_m/I_D Ratio for Nanometer CMOS Technologies. **IEEE Transactions on Microwave Theory and Techniques**, v. 59, n. 7, p. 1822–1831, July 2011. ISSN 0018-9480.

FORBES. **In Theory, IoT Is The Key To A Better Tomorrow – If We Can Overcome Its Challenges**. [S.l.], 2020. Available from Internet: <https://www.forbes.com/sites/forbestechcouncil/2020/02/20/>. Accessed in: 30 jul. 2020.

GHORBEL, I. et al. A subthreshold low-power nmos lc-vco design for autonomous connected objects. In: 2018 30TH INTERNATIONAL CONFERENCE ON MICROELECTRONICS (ICM). [S.l.]: IEEE, 2018.

GSM Association. **IoT connections forecast: the impact of Covid-19**. London United Kingdom, 2020. Available from Internet: <https://data.gsmaintelligence.com/research/research/research-2020/iot-connections-forecast-the-impact-of-covid-19>. Accessed in: 30 jul. 2020.

HABEKOITE, E. et al. State of the Art in the Analog CMOS Circuit Design. In: **Proceedings of the IEEE**. [S.l.: s.n.], 1987. v. 75, n. 6, p. 816–828.

Hajimiri, A.; Lee, T. H. A general theory of phase noise in electrical oscillators. **IEEE Journal of Solid-State Circuits**, v. 33, n. 2, p. 179–194, Feb 1998. ISSN 0018-9200.

HAJIMIRI, A.; LEE, T. H. Design Issues in CMOS Differential LC Oscillators. **IEEE Journal of Solid-State Circuits**, v. 34, p. 717–724, 5 1999.

JANG, T.; JEONG, S.; JEON, D. A noise reconfigurable all-digital phase-locked loop using a switched capacitor-based frequency-locked loop and a noise detector. **IEEE Journal of Solid-State Circuits**, v. 53, p. 102–114, 1 2018.

JIANG, W. ADPLL Design for WiMAX. **Master Thesis**, 2011.

KANG, J.-J.; WENG, R.-M.; LIU, C.-Y. A low-power cmos power amplifier for ieee 802.11a applications. In: 2009 ASIA PACIFIC MICROWAVE CONFERENCE. [S.l.]: IEEE, 2009.

KANG, M.; GIL, M. J.; SHIN, H. A Simple Parameter Extraction Method of Spiral On-Chip Inductors. In: **IEEE TRANSACTIONS ON ELECTRON DEVICES**. [S.l.: s.n.], 2005. v. 52, n. 9, p. 1976–1981.

KANG, S.; NIKNEJAD, A. M. A 100ghz active-varactor vco and a bi-directionally injection-locked loop in 65nm cmos. In: 2013 IEEE RADIO FREQUENCY INTEGRATED CIRCUITS SYMPOSIUM (RFIC). [S.l.]: IEEE, 2013.

KUO, F.-W. et al. A bluetooth low-energy transceiver with 3.7-mw all-digital transmitter, 2.75-mw high-if discrete-time receiver, and tx/rx switchable on-chip matching network. **IEEE Journal of Solid-State Circuits**, v. 52, p. 1144–1162, 2 2017.

LEE, D. et al. Low power fsk transceiver using adpll with direct modulation and integrated spdt for ble application. In: 2018 23RD ASIA AND SOUTH PACIFIC DESIGN AUTOMATION CONFERENCE (ASP-DAC). [S.l.]: IEEE, 2018.

LEE, H.; MOHAMMADI, S. A Subthreshold Low Phase Noise CMOS LC VCO for Ultra Low Power Applications. **IEEE Microwave and Wireless Components Letters**, v. 17, p. 796–798, 11 2007.

LEE, H.; MOHAMMADI, S. A Subthreshold Low Phase Noise CMOS LC VCO for Ultra Low Power Applications. **IEEE Microwave and Wireless Components Letters**, v. 17, p. 796–798, 11 2007.

LEENAERTS, D.; TANG, J. van der; VAUCHER, C. S. **Circuit Design for RF Transceivers**. 1. ed. NEW YORK: Kluwer Academic, 2003. ISBN 0-7923-75551-3.

LEITE, B. Design and modeling of mm-wave integrated transformers in CMOS and BiCMOS technologies. **PhD Thesis**, 2011.

LEITE, B. et al. Design and characterization of CMOS millimeter-wave transformers. In: **SBMO/IEEE MTT-S International Microwave and Optoelectronics Conference (IMOC), 2009**. [S.l.: s.n.], 2009. ISSN 1679-4389.

LI, C.-C. et al. A 0.2V Trifilar-Coil DCO with DC-DC Converter in 16nm FinFET CMOS with 188dB FOM, 1.3kHz Resolution, and Frequency Pushing of 38MHz/V for Energy Harvesting Applications. In: 2017 IEEE International Solid-State Circuits Conference (ISSCC). [S.l.]: IEEE, 2017. p. 332 – 334.

LIU, H. et al. A 265-uW Fractional-N Digital PLL With Seamless Automatic Switching Sub-Sampling/Sampling Feedback Path and Duty-Cycled Frequency-Locked Loop in 65-nm CMOS. **IEEE JOURNAL OF SOLID-STATE CIRCUITS**, v. 54, p. 3478–3492, 12 2019.

LONG, J. R. Monolithic Transformers for Silicon RF IC Design. In: IEEE JOURNAL OF SOLID-STATE CIRCUITS. [S.l.]: IEEE, 2000. p. 1368–1382.

LOO, X. S.; WIN, M. Z.; YEO, K. S. fT Enhancement of CMOS Transistor Using Isolated Polysilicon Gates. In: 2018 IEEE RADIO FREQUENCY INTEGRATED CIRCUITS SYMPOSIUM (RFIC). [S.l.]: IEEE, 2018.

LU, Q.; LIU, H.; LI, Q. Charge Pump Based PLL Design for IEEE 1394b PHY. In: 2014 12th IEEE International Conference on Solid-State and Integrated Circuit Technology (ICSICT). [S.l.]: IEEE, 2014.

MASI, G. D. The impact of topology on internet of things: A multidisciplinary review. In: 2018 ADVANCES IN SCIENCE AND ENGINEERING TECHNOLOGY INTERNATIONAL CONFERENCES (ASET). [S.l.]: IEEE, 2018.

OKADA, K. et al. A 0.114-mW Dual-Conduction Class-C CMOS VCO with 0.2-V Power Supply. In: 2009 Symposium on VLSI Circuits Digest of Technical Papers (VLSI). [S.l.]: IEEE, 2009. p. 228 – 229.

PAALA, N. M. A. et al. Android controlled lawn mower using bluetooth and wifi connection. In: 2019 IEEE 4TH INTERNATIONAL CONFERENCE ON COMPUTER AND COMMUNICATION SYSTEMS (ICCCS). [S.l.]: IEEE, 2019.

RADER, J. T. C. M.; GOLD, B. A Digital Frequency Synthesizer. **IEEE Journal of Solid-State Circuits**, v. 19, n. 1, p. 48 – 57, 1971.

RAZAVI, B. A 1.8GHz CMOS Voltage-Controlled Oscillator. In: 1997 IEEE International Solid-state Circuits Conference (ISSCC). [S.l.]: IEEE, 1997. p. 338–339.

RAZAVI, B. **RF Microelectronics**. [S.l.]: Prentice Hall PTR, 1998.

SAFKHANI, M. et al. On the Traceability of Tags in SUAP RFID Authentication Protocols. In: IEEE 2012 International Conference on RFID -Technologies and Applications (RFID - TA). [S.l.]: IEEE, 2012. p. 292–296.

SCHIMPF, K.; BENNA, B.; PROETEL, D. A new approach to characterize substrate losses of On-Chip inductors. In: **IEEE 2001 Int. Conference on Microelectronic Test Structure**. [S.l.: s.n.], 2001. v. 14, p. 115–118.

SOUZA, B. et al. System-level Design of an ULP ADPLL-based Frequency Synthesizer for IEEE 802.11ah. In: **10th Workshop on Circuits and Systems Design**. [S.l.: s.n.], 2020.

SRINIVASAN, R.; ARUMUGAM, J. Internet of things: Issues in using mobile communication network. In: 3RD INTERNATIONAL CONFERENCE ON ELECTRICAL, ELECTRONICS, ENGINEERING TRENDS, COMMUNICATION, OPTIMIZATION AND SCIENCES (EEECOS 2016). [S.l.]: IEEE, 2016.

STASZEWSKI, R. B.; BALSARA, P. T. **ALL-DIGITAL FREQUENCY SYNTHESIZER IN DEEP-SUBMICRON CMOS**. 1. ed. New Jersey: John Wiley and Sons, 2006. ISBN 0-471-77255-0.

STASZEWSKI, R. B. et al. A First Digitally-Controlled Oscillator in a Deep-Submicron CMOS > Process for Multi-GHz Wireless Applications. In: 2003 IEEE Radio Frequency Integrated Circuits Symposium (RFIC). [S.l.]: IEEE, 2003. p. 81 – 84.

STRAAYER, M.; CABANILLAS, J.; REBEIZ, G. M. A Low-Noise Transformer-Based 1.7GHz CMOS VCO. In: 2002 IEEE International Solid-state Circuits Conference (ISSCC). [S.l.]: IEEE, 2002.

TOUMAZOU, C.; MOSCHYTZ, G. S.; GILBERT, B. **Trade-offs in analog circuit design: the designer's companion**. [S.l.]: Springer Science & Business Media, 2004.

VOLKAERTS, W.; STEYAERT, M.; REYNAERT, P. 118ghz fundamental vco with 7.8tuning range in 65nm cmos. In: 2011 IEEE RADIO FREQUENCY INTEGRATED CIRCUITS SYMPOSIUM (RFIC). [S.l.]: IEEE, 2011.

WANG, T.-P. et al. Phase-noise reduction of x-band push–push oscillator with second-harmonic self-injection techniques. **IEEE TRANSACTIONS ON MICROWAVE THEORY AND TECHNIQUES**, v. 55, p. 66–77, 1 2007.

WU, L. An Ultra-Low-Power ADPLL for BLE Applications. **Master Thesis**, 2014. ISSN 0378-1119.

YANG, S. et al. A 0.2-V Energy-Harvesting BLE Transmitter With a Micropower Manager Achieving 25% System Efficiency at 0-dBm Output and 5.2-nW Sleep Power in 28-nm CMOS. **IEEE JOURNAL OF SOLID-STATE CIRCUITS**, v. 54, p. 1351–1362, 5 2019.

YU, J.-J. et al. A 1V 1.8GHz Low Power Differential Colpitts VCO. In: **2006 8th International Conference on Solid-State and Integrated Circuit Technology Proceedings**. [S.l.: s.n.], 2006.

YU, W.-H. et al. A 0.18v 382μw bluetooth low-energy (ble) receiver with 1.33nw sleep power for energy-harvesting applications in 28nm cmos. In: 2017 IEEE INTERNATIONAL SOLID-STATE CIRCUITS CONFERENCE (ISSCC). [S.l.]: IEEE, 2017.

ZHUANG, J.; STASZEWSKI, R. B. A low-power all-digital PLL architecture based on phase prediction. In: . [S.l.: s.n.], 2012. c, p. 797–800. ISBN 9781467312615.

APPENDIX A — LIST OF PUBLICATIONS BY THE AUTHOR

A.1 Conference Papers

M. Moreira, L. Ferreira, B. Souza, S. B. Ferreira, F. D. Baumgratz,and S. Bampi, "Low power 380 μ W energy efficient 1.8 ghz digitally controlled oscillator for iot applications," in 2019 *26th IEEE International Conference on Electronics, Circuits and Systems (ICECS)*, 2019, pp. 763–766.

L. Ferreira, **M. Moreira**, B. Souza, S. Ferreira, F. Baumgratz, and S. Bampi, "Review on the evolution of low-power and highly-linear time-to-digital converters - tdc," in *(LASCAS 2020)*, 2020, pp. 1–4.

B. Souza, L. Ferreira, **M. Moreira**, F. Baumgratz, S. Ferreira, and S. Bampi, "System-level Design of an ULP ADPLL-based Frequency Synthesizer for IEEE 802.11ah," in *WCAS 2020*, 2020.

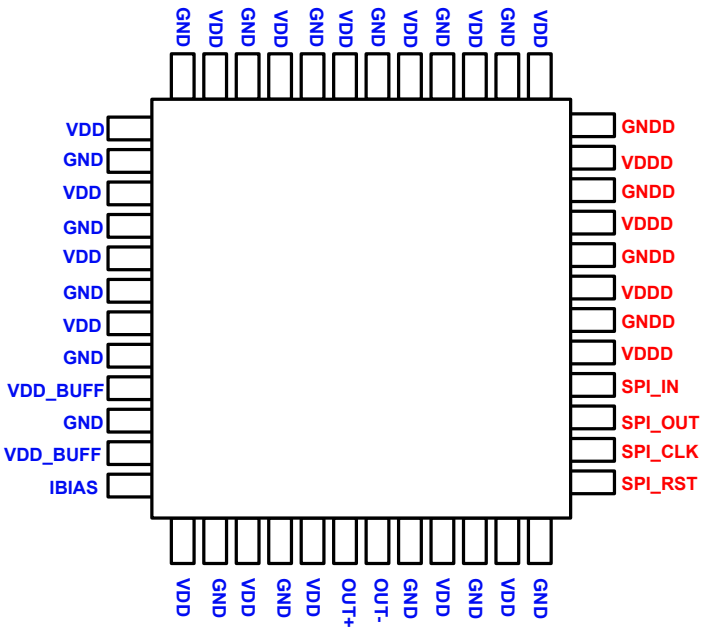
APPENDIX B — DOCUMENTATION FOR MEASUREMENTS

The last design presented in this M.Sc. thesis, which is the transformer-based DCO, is targeted for future validation through the measurements after fabrication. To serve this purpose, the layout of the proposed DCO presented on the figure 5.18 contains a serial to parallel interface to control the bits of the varactors and then control the operational frequency of the oscillator. The layout also includes decoupling capacitor on all the bias sources for filtering noise that can be inserted inside the die. The supply voltage of the DCO is different from the buffers, as discussed previously, to increase the output power and to measure the own DCO power consumption separately. All voltages and bias currents will be provided by appropriate laboratory equipments.

The main equipment necessary for DCO measurements is the Spectrum Analyzer. In the measurements of oscillators, the main required results are the output power and the phase-noise. Both are obtained from the Spectrum Analyzer by the measurement of the frequency versus the power spectrum of the measured output. The pad ring of the DCO is made for PCB measurements. The PCB allows the decrease in the number of cables connected on the system, which results also in the decrease in the number of cables if the biases come from the PCB. Furthermore, the bondwire does not interfere significantly on the perform due to the goal of the circuit is the measurement of the power consumption and the phase-noise of the oscillator when it has reached a stable oscillation. Moreover, as the output oscillator is differential, there is a necessity of a balun placed at the output to transform the signal into a single-ended one. Hence, in a PCB, an SMD balun can be used to also decrease the number of cables.

In the pad ring of the DCO, the analog signal and digital signals are separated. Hence, the signal must remain separated in the PCB, in order to avoid sources of noise. In addition, decoupling capacitors are always necessary to filter the unwanted noises. The signal to control the serial parallel interface, in the test setup, is coming from an output port of a FPGA. Hence, the serial connection between the PCB and the FPGA is necessary. Figure B.1 presents the PAD ring organization, with its corresponding signal names. The digital pins come from a serial to parallel interface placed on the right side of the die to avoid interferences. Furthermore, the digital power supply and ground are separated from the analog ones to avoid noise induced by digital circuits switching. Two analog power supplies are required to measure the power consumption of the DCO without the buffer contribution.

Figure B.1: Die Pin Diagram.



Source:Author