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Influence of CO annealing in metal-oxide-semiconductor capacitors with SiO_2 films thermally grown on Si and on SiC

E. Pitthan,[1,a)] R. dos Reis,[2] S. A. Corrêa,[3] D. Schmeisser,[3] H. I. Boudinov,[1,4] and F. C. Stedile[1,5]
[1]*PGMICRO, UFRGS, 91509-900 Porto Alegre, RS, Brazil*
[2]*National Center for Electron Microscopy, The Molecular Foundry, LBNL, Berkeley, California 94720, USA*
[3]*Applied Physics and Sensors, Brandenburg University of Technology Cottbus-Senftenberg, Konrad-Wachsmann-Allee 17, 03046 Cottbus, Germany*
[4]*Instituto de Física, UFRGS, 91509-900 Porto Alegre, RS, Brazil*
[5]*Instituto de Química, UFRGS, 91509-900 Porto Alegre, RS, Brazil*

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Understanding the influence of SiC reaction with CO, a by-product of SiC thermal oxidation, is a key point to elucidate the origin of electrical defects in SiC metal-oxide-semiconductor (MOS) devices. In this work, the effects on electrical, structural, and chemical properties of SiO_2/Si and SiO_2/SiC structures submitted to CO annealing were investigated. It was observed that long annealing times resulted in the incorporation of carbon from CO in the Si substrate, followed by deterioration of the SiO_2/Si interface, and its crystallization as SiC. Besides, this incorporated carbon remained in the Si surface (previous SiO_2/Si region) after removal of the silicon dioxide film by HF etching. In the SiC case, an even more defective surface region was observed due to the CO interaction. All MOS capacitors formed using both semiconductor materials presented higher leakage current and generation of positive effective charge after CO annealings. Such results suggest that the negative fixed charge, typically observed in SiO_2/SiC structures, is not originated from the interaction of the CO by-product, formed during SiC oxidation, with the SiO_2/SiC interfacial region. © *2016 AIP Publishing LLC*. [http://dx.doi.org/10.1063/1.4939836]

Silicon carbide (SiC) is a semiconductor with suitable properties to replace Si in devices that require high power, high frequency, and/or high temperature applications. Besides, a dielectric film of silicon dioxide (SiO_2) can be thermally grown on it, in a similar way as on Si.[1,2] However, the SiO_2/SiC density of interface states (D_{it}) of films thermally grown is orders of magnitude higher than those on SiO_2/Si, limiting the electrical quality of SiC-based metal-oxide-semiconductor field effect transistors (MOSFETs).[3] Although several methods to reduce these defects have been applied, the origin of electrically active defects in SiO_2/SiC interfacial region has yet to be fully understood. Typically, negative fixed charge is observed in Metal/SiO_2/SiC MOS capacitors when SiO_2 films are thermally grown on SiC.[4–6] In the case of SiO_2/Si capacitors, fixed oxide charges are positive[7,8] and are due to oxygen vacancies.[9] Noborio *et al.*[10] observed that the amount of negative effective charge in SiO_2/SiC is inversely related to the channel mobility in SiC transistors. It is also known that this negative charge is present mainly in the SiO_2/SiC interfacial region.[11,12] A previous work of our group[6] reported that neither the interfacial region thickness nor the amount of residual oxygen on the SiC surface—after removal of the silicon dioxide—increases with the increment of the negative effective charge in Al/SiO_2/4H-SiC capacitors. Ebihara *et al.*[13] theoretically suggested that the negative fixed charges formed during SiC thermal oxidation are from CO_3-like moiety, which results from the interaction of the SiO_2 film with residual carbon atoms. If so, it is very likely that such residual carbons have their origin in the oxidation by-products, such as carbon monoxide (CO), and/or solid carbon.[14] Experimental results evidence that oxidation by-products, most likely CO, interact with the SiO_2 film during SiC oxidation[15] and that higher SiC oxidation temperature results in a reduction of D_{it}[16–18] by enhancing CO out-diffusion, supporting such theory. CO appears to play a major role in the properties of SiO_2/SiC but, up to now, there are no experimental data confirming that this SiC oxidation by-product is responsible for such effects. Therefore, we aim to enlighten this issue by investigating the interaction of CO with the SiO_2/SiC structure.

In this work, we investigate the consequences of the interaction of CO, one of the main SiC oxidation by-products, with SiO_2/SiC and with SiO_2/Si structures, determining their structural and chemical properties, as well as the electrical properties of the correspondent MOS capacitors. SiO_2 films were thermally grown on Si and on SiC. By using Si as substrate, we are able to identify the carbon presence from CO annealing, otherwise undistinguishable from the carbon in the substrate in the SiC case by typical analytical methods such as X-ray photoelectron spectroscopy (XPS). SiO_2/Si annealed in CO has been already widely investigated and used as a route to form SiC nano-crystals in the SiO_2/Si interfacial region due to the reaction of CO with the Si substrate.[19–21] A comparison of this effect in the electrical properties in SiO_2/SiC structures could clarify the origin of SiC electrical degradation during thermal oxidation.

Silicon-faced n-type 4H-SiC (0001) wafers on-axis doped with nitrogen ($3.1 \times 10^{15}\,cm^{-3}$) from Cree, Si wafers doped

[a)]Electronic mail: eduardo.pitthan@ufrgs.br

with phosphorous ($2.5 \times 10^{13}\,cm^{-3}$), and Si wafers with epitaxial layer doped with boron ($1.5 \times 10^{15}\,cm^{-3}$) were used as substrates. They were cleaned with standard Piranha and RCA (Radio Corporation of America) routines,[22] etched in a 5% HF solution, rinsed in deionized water, and dried in N_2 flux. For thermal oxidation, samples were then immediately loaded in a static pressure, resistively heated quartz tube furnace, which was pumped down to 2×10^{-7} mbar before being pressurized with oxygen. SiO_2 films (~24 nm) were thermally grown under 100 mbar of dry natural O_2 at 1000 °C for 1 h in Si case, and 1100 °C for 8 h in SiC case. CO annealing was performed in 100 mbar of CO (99.99% purity) at 1000 or 1100 °C for different times. In all thermal treatments, a N_2(L) trap was used to help base pressure reduction, mainly due to H_2O molecules condensation. Aluminum was thermally evaporated to obtain MOS structures using a mechanical mask aiming at forming circular capacitors with a diameter of 200 μm. InGa eutectic was used as back contact. C-V curves were taken from inversion to accumulation at 100 kHz with a 0.25 V/s rate using a HP4284A Precision LCR Meter. A computer-controlled HP4155A Semiconductor Parameter Analyzer was used for the I-V curves. XPS measurements were carried out using an Omicron-UHV-System with hemispherical analyzer (EA125) and a non-monochromatic Mg Kα radiation (1253.6 eV). Lines were fitted with 70% Gaussian + 30% Lorentzian functions. The Si 2p doublet was simulated by two lines with a branching ratio $2p_{1/2}/2p_{3/2}$ of 0.5 and a spin-orbit splitting of 0.6 eV. Transmission electron microscopy (TEM) was used to determine the microstructure in the SiO_2/Si interface region and at the SiC surface. Cross-sectional specimens were prepared by mechanical polishing and dimpling, followed by Ar^+ ion polishing at shallow angles (~5°). Low-resolution micrographs were acquired by JEOL3010, while High-Resolution micrographs were acquired by a FEI F20 UT Tecnai.

Fig. 1 presents I-V and C-V curves for Al/SiO_2/(Si and SiC) MOS capacitors annealed or not in CO at 1000 °C. From the I-V curves, it can be observed higher leakage currents compared to the samples not submitted to CO annealing in all oxide films on both kinds of substrates. Thus, results indicate deleterious effects in the oxide film dielectric strength due to the CO annealings. It is known that during CO annealing, oxygen exchange between the oxide film and the CO molecule occurs in all depths of the SiO_2 film, while no carbon from CO is introduced in the oxide.[20] It is possible that such O exchange could introduce defects in the oxide film, being responsible for the higher leakage currents observed. Considering CO annealing time, no influence on the I-V curves was observed. Concerning C-V curves for samples not submitted to CO annealing, a negative shift compared to the ideal theoretical curve is observed in the SiO_2/Si case, while a positive shift is observed in the SiO_2/SiC case, indicating, respectively, the presence of positive and negative effective charges, in good agreement with what is typically observed in these structures.[6,7] No major difference is observed after the CO annealing for 0.3 h in the Si-case. However, after the 4 h CO annealing, a significant negative shift is observed, indicating the generation of positive effective charge. In the SiC case, a similar positive effective charge generation is observed, independent of the

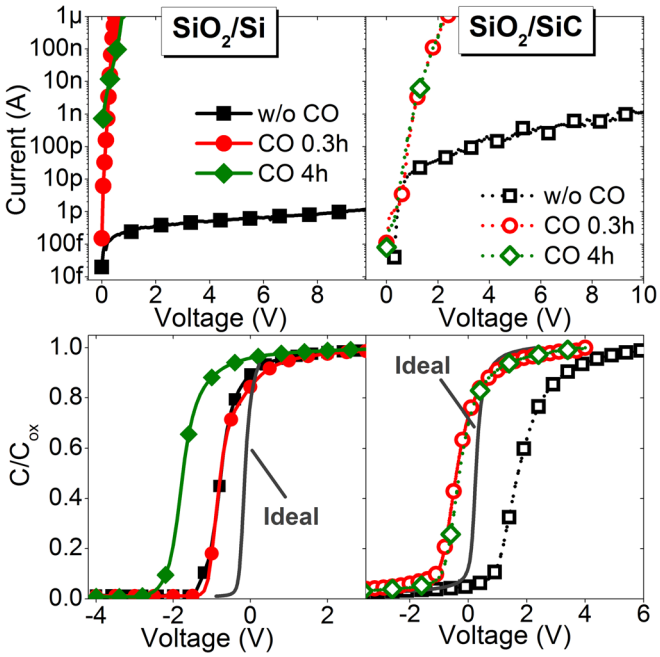

FIG. 1. I-V and C-V curves of Al/SiO_2/(Si and 4H-SiC, both n-type) capacitors submitted or not to annealing in 100 mbar CO at 1000 °C for the indicated times. Ideal theoretical C-V curves are also presented for comparison.

annealing time, which compensated the negative charges present in the Al/SiO_2/SiC capacitor not submitted to CO annealing. Such result suggests a similar electrical effect of CO annealing in both SiO_2/Si and SiO_2/SiC samples, namely, generation of positive charge.

To ensure that the positive effective charge observed in Fig. 1 after the CO annealing in samples is an effect of the carbon monoxide interaction, and not due to a thermal effect, similar annealing conditions were used for SiO_2/SiC capacitors in argon ambient instead of CO. I-V and C-V curves obtained for these samples are presented in Fig. 2. It is possible to observe distinct properties of MOS capacitors depending on the annealing ambient: the inert ambient, for both temperatures, induced a shift towards the ideal theoretical C-V curve compared with the SiC sample only oxidized, indicating a reduction of the negative effective charge, as previously observed by another group.[12] Besides, a reduction in the leakage current is observed which is attributed to a thermally induced decrease of the concentration of defects. On the other hand, when the CO annealing was performed, the increase in the leakage current and the generation of positive effective charge was clearly observed. Even when a post-oxidation-annealing (POA) in argon was performed previous to the CO annealing, the same deleterious effects are observed. This confirms the influence of CO interaction with the SiO_2/SiC structures.

The influence of the dopant in the electrical properties due to the CO annealing was also investigated for the Si substrates. Differently from the behavior of Si n-type samples (Fig. 1), no increase in the leakage current was observed after the CO annealing at 1000 °C in the SiO_2/Si doped with boron, as shown in Fig. 3. Only when the CO annealing was performed at 1100 °C, a significant increase in the leakage current was observed. Such difference in the oxide quality

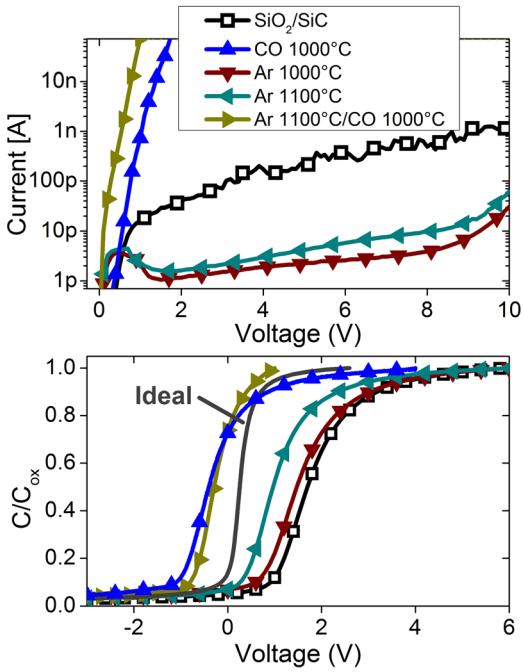

FIG. 2. I-V and C-V curves of Al/SiO_2/4H-SiC capacitors submitted or not to annealings in 100 mbar of CO and/or 100 mbar of Ar for 1 h at the indicated temperatures. Ideal theoretical C-V curves are also presented for comparison.

between n and p-type samples can arise from the presence of an epitaxial layer in the p-type samples,[23] which resulted in oxides less susceptible to degradation. The clear influence of CO annealing time can be observed for both temperatures in C-V curves, where longer annealing times induced larger negative shift as compared to the ideal C-V curve, again

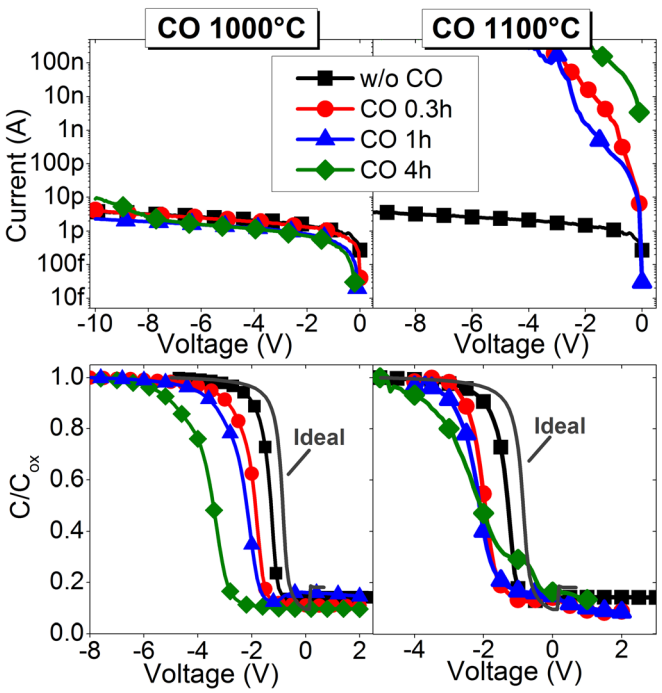

FIG. 3. I-V and C-V curves of Al/SiO_2/(Si p-type) capacitors submitted or not to annealings in 100 mbar CO at 1000 and 1100 °C for the indicated times. Ideal theoretical C-V curves are also presented for comparison.

indicating generation of positive charge due to the CO interaction, in agreement with what was observed in the SiO_2/SiC and in the SiO_2/Si n-type capacitors. Besides, the irregularly-shaped C-V curve obtained when CO annealing was performed at 1100 °C for 4 h indicates carbon crystallization in the SiO_2/Si interfacial region, as will be further analyzed below.

In general, independent of the condition tested, CO interaction induced positive charge in MOS capacitors. It is particularly interesting the generation of positive charge in the SiC case: such results are in disagreement with the hypothesis that the negative charge typically observed in SiO_2/SiC based MOS capacitors are from the interaction of the CO, a SiC oxidation by-product, with the SiO_2/SiC structure. If that was the case, higher concentration of negative effective charge would probably be observed after the CO annealing. This suggests that CO interaction during the annealing of SiC based structures does not play a major role in the SiO_2/SiC electrical degradation. Concerning the formation of positive charge due to the CO interaction, it could be an effect from the oxygen exchange between the CO and the oxide film,[20] or the modification in the oxide/semiconductor interfacial region during the annealing (as will be presented and discussed below). A similar oxygen exchange, between the gas and the solid phase, in all depths of the oxide film was already observed in SiO_2/SiC samples annealed in $D_2{}^{18}O$,[24] but no positive charge was induced. Thus, it is more likely that the positive charge originates from modifications in the interfacial region due to the CO annealing. To further investigate how CO interacts with SiO_2/Si and with SiO_2/SiC causing the electrical effects observed, TEM and XPS analyses were performed.

Fig. 4 presents a set of cross-section TEM micrographs acquired from SiO_2/Si p-type after different annealing times under CO at 1100 °C in comparison with a reference SiO_2/Si sample not annealed in CO. These samples were chosen in order to evidence the strong influence of C in the surface microstructure as the CO annealing time increases. A very flat interface of the reference SiO_2/Si sample is observed in Fig. 4(a), which is detailed at atomic level in the magnified HRTEM micrograph of Fig. 4(b). After annealing for 1 h (Figs. 4(c) and 4(d)), the evolution of carbon incorporation in the Si substrate is denoted by an increase of the surface irregularity compared with the reference sample. Presence of darker regions near interface on both Figs. 4(c) and 4(d) correspond to agglomeration of carbon species that was corroborated by Energy Filter TEM, using the carbon peak on Electron Energy-Loss Spectrometry (image not shown). However, a stable SiC structure is not observed either by HRTEM or electron diffraction (not shown). A faster local oxidation (that does not reflect an overall significant increase in the oxide film thickness) of {111} planes is evident in Fig. 4(e) by the formation of V-shaped defects on the Si surface (see drawn lines). These defects appear to be a stable diffusion path for carbon at this annealing stage.

After 4 h under CO environment at 1100 °C (Figs. 4(f) and 4(g)), an additional substrate oxidation occurred, in agreement with Ref. 21, generating a slightly thicker SiO_2 film (from 23.7 to 25.3 nm) and a new interface without the

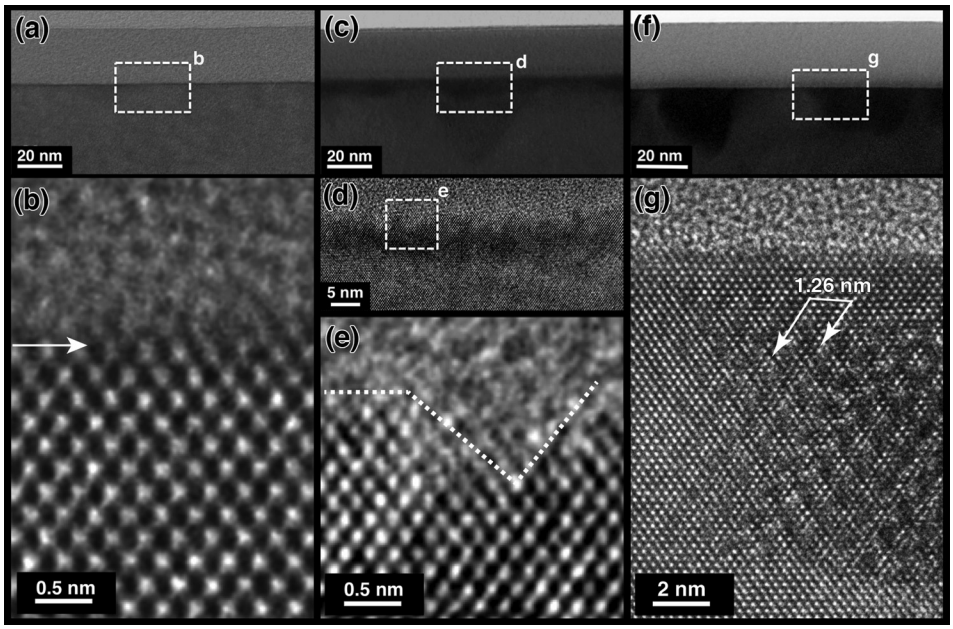

FIG. 4. (a) TEM micrograph of a reference SiO_2/(Si p-type) not annealed under CO. Its interface is detailed in (b) (arrow points surface termination). (c)–(e) Set of TEM micrographs of SiO_2/(Si p-type) samples submitted to annealing under 100 mbar of CO at 1100 °C for 1 h. Detailed HTEM in (e) presents a V-type surface termination. (f) and (g) Illustrate the formation of beta-SiC crystalline phase for a structure annealed for 4 h. Arrows in (g) denote the spacing of Moirè patterns. All micrographs were taken oriented to [011] direction of Si substrate.

defects observed due to 1 h annealing. A stabilization of carbon in β-SiC structure is also observed. This can be confirmed by the presence of Moirè fringes (Fig. 4(g)) as a clear evidence of superposition of two rigid lattices. The length of Moirè patterns (D) depends on the angle and the lattice mismatch between precipitate and matrix. Given the interplanar spacings d_1 and d_2 of Si and β-SiC, respectively, for two cubic lattices, D can be calculated by $D = d_1 d_2/(d_1\text{-}d_2)$. By using the plane spacings for Si and SiC, the spacing D of (222) Moirè fringes should be 1.26 nm, which is equal to the spacing of the Moirè repeat measured from HRTEM image. This observation agrees with the formation of cubic SiC that was previously reported in the literature 19, 20, and 21 and with the observation of diffraction peaks corresponding to cubic-SiC (not shown).

Fig. 5 presents XPS spectra of SiO_2/Si (p-type) samples annealed in CO at 1100 °C for different times compared to a SiO_2/Si sample not annealed, being all samples etched in HF in order to remove the silicon dioxide film. It can be observed an increase in the intensity of the SiC component in the C 1s region as the CO annealing progresses in time when compared to the hydrocarbon component from contamination (named CH). The observation of SiC evidences that, at least partially, the SiC formed due to the CO annealing becomes "unetcheable." The SiC formation is confirmed comparing the binding energy difference between the C1s and the Si2p components corresponding to the SiC. In the sample annealed in CO, the energy difference is 182.5 eV, while in our SiC clean wafer measured in the same conditions, it is 182.2 eV. The difference observed between the binding energies can be attributed to a possible stoichiometric difference being richer in Si in the case of the Si annealed substrate.[25] A small increase in the amounts of compounds assigned to carbon bonded to oxygen in two different states, compared to the hydrocarbon compounds, can also be observed after CO annealing. They are attributed to the formation of carbonate/carboxylate compounds, due to CO interaction, that were not removed during etching.[26]

In the SiC case, comparing the HRTEM image of a sample submitted to CO annealing (Fig. 6) to another one not submitted to CO annealing (not shown) it is noticeable the degradation of the SiC surface region due to the CO annealing. In Fig. 6(b), a closer view evidences the formation of steps on {0111}-type planes. This type of stack rearrangement

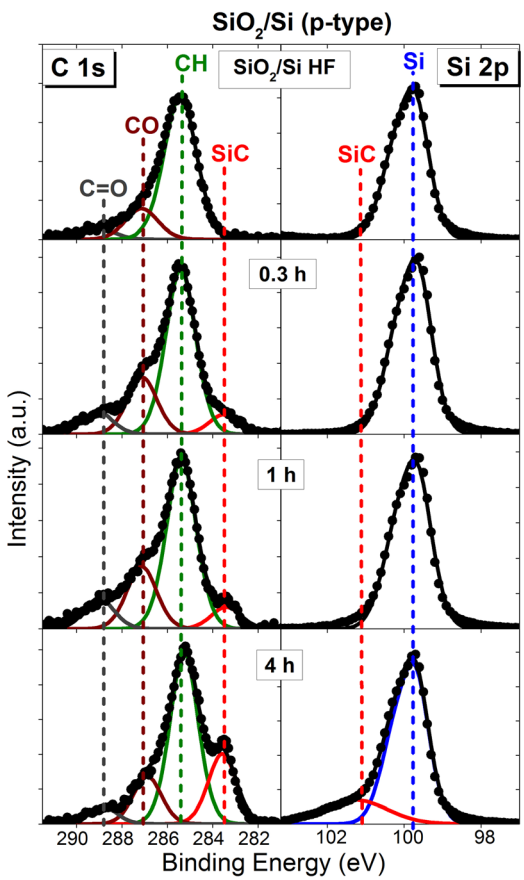

FIG. 5. C 1s and Si 2p photoelectron spectra (a.u. stands for arbitrary units) of SiO_2/(Si p-type) samples submitted or not to annealing in 100 mbar CO at 1100 °C for the indicated times and then etched in aqueous HF in order to remove the silicon dioxide film.

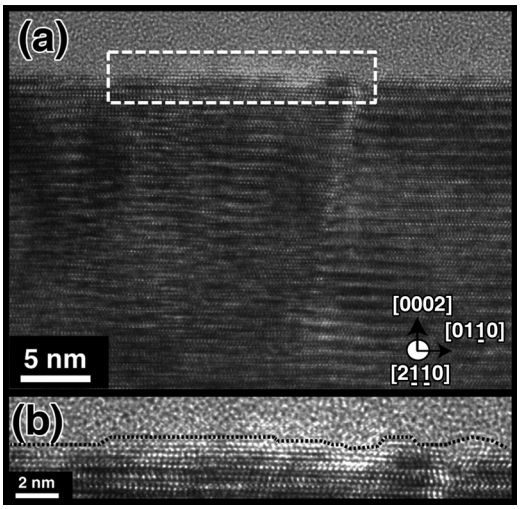

FIG. 6. (a) TEM micrograph of SiO_2/SiC sample submitted to annealing under 100 mbar of CO at 1000 °C for 4 h and etched in aqueous HF in order to remove the silicon dioxide film. A magnified view of the surface is shown on (b) with its termination traced out by a dotted line. Micrograph was taken on [2$\underline{1}$10] direction of SiC.

has been observed for 4 H-SiC substrates thermally treated under excess of Si flux.[27] To understand this surface modification, XPS analyses were performed. It can be observed in the C 1 s region photoelectron spectra of Fig. 7 that in the clean SiC sample, the component from the SiC substrate is present besides another one less intense around 286.2 eV. A significant increase in intensity of the signal around the binding energy of 286.2 eV occurs after the CO annealing. This region is typically assigned to carbon bonded to oxygen, although some hydrocarbon contamination can also be present around similar energies (typically around 285 eV, as can be observed in Fig. 5, but some reports suggest that contamination peaks around 286 eV on SiC[4]). It is possible that the annealing in CO could have introduced some contamination that was not removed by HF etching, as observed in the Si-case and as suggested by Miller *et al.*[26] No significant modifications were observed in the Si 2 p region (not shown), suggesting that the compounds observed in the C 1s region around 286.2 eV are

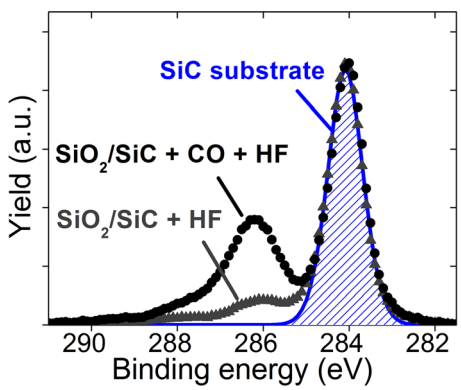

FIG. 7. C 1s photoelectron spectra (a.u. stands for arbitrary units), normalized by the SiC substrate peak signal, of SiO_2/SiC samples submitted or not to annealing in 100 mbar CO at 1000 °C for 4 h (as indicated) and then etched in aqueous HF in order to remove the silicon dioxide film. The contribution from the SiC component (in blue) is hatched.

mainly due to carbon bonded to carbon and/or to oxygen (and not to Si).

In conclusion, the consequences of CO annealing of SiO_2 films thermally grown on Si and on SiC in their electrical, structural, and chemical properties were investigated. For the SiO_2/Si case, the CO annealing induced carbon incorporation in the Si substrate surface region and led to the formation of SiC nano-crystals, as previously reported in the literature. In the SiO_2/SiC case, it was possible to observe a rough surface in the SiC surface region due to the CO annealing. The consequences in electrical properties of CO annealing were the same on both substrate structures: increase in both oxide film leakage current and in the formation of positive charge. Such results have a major impact in the understanding of SiC electrical degradation due to thermal oxidation, since several explanations about the origin of negative fixed charges in the SiO_2/SiC interfacial region rely on the interaction of the by-products formed during SiC thermal oxidation (such as CO) with the SiO_2/SiC structure. From this work, such interaction could be ruled out as the main cause of this degradation.

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