UNIVERSIDADE FEDERAL DO RIO GRANDE DO SUL
INSTITUTO DE INFORMÁTICA
PROGRAMA DE PÓS-GRADUAÇÃO EM COMPUTAÇÃO

THIAGO ROCHA DE ASSIS

Analysis of Transistor Sizing and Folding Effectiveness to Mitigate Soft Errors.

Thesis presented in partial fulfillment of the requirements for the degree of Master in Computer Science

Prof. Dr. Ricardo Augusto da Luz Reis
Advisor

Prof. Dr. Fernanda Gusmão de Lima Kastensmidt
Co-advisor

Porto Alegre, March 2009.

CIP – CATALOGAÇÃO NA PUBLICAÇÃO

Assis, Thiago Rocha de

Analysis of Transistor Sizing and Folding Effectiveness to Mitigate Soft Errors / Thiago Rocha de Assis – Porto Alegre: Programa de Pós-Graduação em Computação, UFRGS 2009.

102 f.:il.

Thesis (Master) – Universidade Federal do Rio Grande do Sul. Programa de Pós-Graduação em Computação. Porto Alegre, BR – RS, 2008. Advisor: Ricardo Augusto da Luz Reis; Co-Advisor: Fernanda Gusmão de Lima Kastensmidt.

1.Fault Tolerance. 2.Radiation Effects 3.Single Event Transient. 4. Single Event Effect. 5. Soft Errors. 6. Transistor Sizing. 7. Folding. I. Ricardo Augusto da Luz Reis, II. Fernanda Gusmão de Lima Kastensmidt.

ACKNOWLEDGMENT

I would like to thank my father (Ailton Assis) and my mother (Telma Assis) for all support that they gave me during undergrad and graduate courses. Without their help this journey would certainly had become much harder. I also thank my brother (Ailton Junior) and sister (Milla Assis) for their patience during the last years. I also thank my girlfriend (Reginara Souza) for her understanding and supporting during the last years.

I'm very grateful to advisor Prof. Dr. Ricardo Reis for this great opportunity to prepare a master at UFRGS. I wish to thank Prof. Dr. Fernanda Kastensmidt and Prof. Dr. Gilson Wirth for their outstanding contribution to the developing of this work. Without their help this research would never be possible.

I wish to thank all my teachers and friends from the Universidade Federal do Rio Grande do Sul that somehow had contribute to the development of this work. I also wish to thank the great teachers that I had at the Universidade Salvador were I did my undergrad course.

Thanks!

TABLE OF CONTENTS

LIST OF ABBREVIATIONS

ASIC	Application Specific Integrated Circuit
ASU	Arizona State University
AUGER	Auger Recombination Model
BGN	Band Gap Narrowing
CCSMOB	Carrier-Carrier Scattering Mobility Model
CME	Coronal Mass Ejection
CMOS	Complementary Metal Oxide Silicon
DD	Displacement Damage
DMR	Double Modular Redundancy
ELG	Enclosed Layout Geometry
ELT	Enclosed Layout Transistor
EPI	Epitaxial Substrate
FPGA	Field Programmable Gate Array
GND	Ground
IC	Integrated Circuit
LDD	Light Doped Drain
LET	Linear Energy Transfer
MBU	Multiple Bit Upset
MIT	Massachusetts Institute of Technology
MOS	Metal Oxide Semiconductor
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
NIEL	Non-Ionizing Loss Energy
OS	Operating System
PTM	Predictive Technology Model
RPP	Rectangular Parallelepiped

SAA	South Atlantic Anomaly
SBU	Single Bit Upset
SEE	Single Event Effect
SEFI	Single Event Functional Interruption
SEGR	Single Event Gate Rupture
SEL	Single Event Latchup
SET	Single Event Transient
SER	Soft Error Rate
SEU	Single Event Upset
SRAM	Static Random Access Memory
SRH	Schockley-Read-Hall Model
SSR	Super Step Retrograde
TID	Total Ionizing Dose
TMR	Triple Modular Redundancy
UFRGS	Universidade Federal do Rio Grande do Sul

LIST OF FIGURES

LIST OF TABLES

ABSTRACT

In this work the transistor sizing and folding techniques were evaluated for SET robustness in a 90nm MOSFET technology using a 3D device model. A n-type MOSFET transistor using a 90nm technology predictive profile was modeled and functional behavior compared with PTM level 54 model showing a fit of the device with the PTM. During simulations the modeled device was irradiated in a simulation environment using particles with the profile of sea and space level ions. The radiation effects simulation had indicated that the transistor sizing can be more or less efficient to reduce SET according to the collected charge. It was found that for environments with high energy particle, transistor sizing was not able to reduce soft errors intensity. The use of folding has shown significant reduction of the amplitude and duration of the transient pulse, making this technique very useful to reduce soft errors. For alpha particles and heavy ions the combination of transistor folding and sizing had shown to be an effective combination to enhance the reliability of the circuits. A 6T SRAM cell was modeled to evaluate transistor sizing and folding techniques and the results confirmed the efficiency of folding plus sizing to reduce the effects of radiation.

Keywords: Radiation effects, Single Event Effect, Transistor Sizing, Folding, Microelectronics, Fault Tolerance, Soft Errors.

Análise da influência do dimensionamento e partição de transistores e na proteção de circuitos contra efeitos de radiação.

RESUMO

Este trabalho apresenta uma avaliação da eficiência do dimensionamento e particionamento (folding) de transistores para a eliminação ou redução de efeitos de radiação. Durante o trabalho foi construído um modelo de transistor tipo-n MOSFET para a tecnologia 90nm, utilizando modelos preditivos. O transistor 3D modelado foi comparado com o modelo de transistor elétrico PTM level 54 da Arizona State University e os resultados mostraram uma coerência entre os dispositivos. Este transistor modelado foi irradiado por uma série de partículas que caracterizam ambientes terrestres e espaciais. Foi descoberto que a técnica de redimensionamento de transistores tem sua eficiência relacionada ao tipo de partícula do ambiente e não é aplicável em ambientes com partículas com alta energia. Descobriu-se também que aplicando o particionamento de transistores é possível reduzir a amplitude e a duração de erros transientes. A combinação do dimensionamento e o particionamento de transistores pode ser utilizada para a redução de efeitos de radiação incluindo partículas leves e pesadas. Por fim um estudo de caso foi realizado com uma célula de memória estática de 6 transistores utilizando as técnicas mencionadas anteriormente. Os resultados da célula de memória indicaram que a combinação das duas técnicas pode de fato reduzir e até impedir a mudança do estado lógico armazenado na célula.

Palavras-chaves: Efeito de radiação, Evento de efeito único, Dimensionamento de transistores, Microeletrônica, Tolerância a falhas, Erros transientes.

1 INTRODUCTION

Integrated Circuit (IC) is a semiconductor device consisting of electrical components such as transistors, diodes and capacitances (REIS, 2002). The main component of an IC is the transistor, an electric device made by the overlaying of semiconductor materials with doses of positive and negative ions. These ICs are used to build devices that will be used at televisions, cellular phones, computers, medical equipments, avionic instruments and military instruments (RABAEY, 2003).

The use of an IC is transparent to users, but it is becoming even more present to their lives. One of the factors that had contributed to the success of ICs is the scaling of the technology to nanometer scale which had allowed to build ICs with higher computational power, lower area occupation and smaller energy consumption. The usage of IC's in more applications had also allowed a reduction in their price, since a larger production reduce the unit price.

The constant increases of the use of electronic devices with their constant scale to nanometer range made a common phenomenon dangerous to IC functionality. The Earth is constantly bombarded by radiation particles from sources of radiation like cosmic rays and the sun. Most part of this radiation is turned away by Earth Magnetic Field or filtrated by Earth Atmosphere, and what can pass has too lower energy and generally can't harm humans and animals. But unfortunately the radiation that is able to pass through earth atmosphere is able to harm electrical devices such as the IC, making rise pulses of energy that can provoke transient effects or even permanent problems (BOUDENOT, 2007).

The same technology scale that had contributed to the diffusion of ICs in many applications had also contributed to the reduction of the tolerance of these devices to radiation effects. The correlation of technology scale and radiation tolerance has been the focus of many works that will be briefly approached at the following.

Johnston (2000) makes a review over the increase of error rate for alpha particles and heavy ions in memory cells. Technology issues about supply voltage, lithography resolution, channel length, and density of devices are discussed and correlated to the soft error rate. Basically, increasing the frequency imposes that transient pulses of small duration are able to disturb the device and small supply voltages indicates that smaller amplitude changes of transient pulses are able to disturb the device which also make it more susceptible to soft error. The reduction of the device thickness contributes to the reduction of the soft error. The work also makes a briefly discussion about the behavior of neutrons at Silicon-on-Insulator devices.

Another work done by Baumann, (2005) does an extensive evaluation of radiation effects and the increase of soft errors in advanced semiconductor technologies focus in memory cells. In figure 1.1 the author analyses the number of embedded SRAM cells

per chip correlated with the soft error rate. The author concludes that SER in single chips system is not a main reliability problem instead of chips with multiples SRAM cells. The author also analyses the reaction of heavy ions inside the silicon evaluating the energy generated by these events correlating the results with the critical charge of the device.

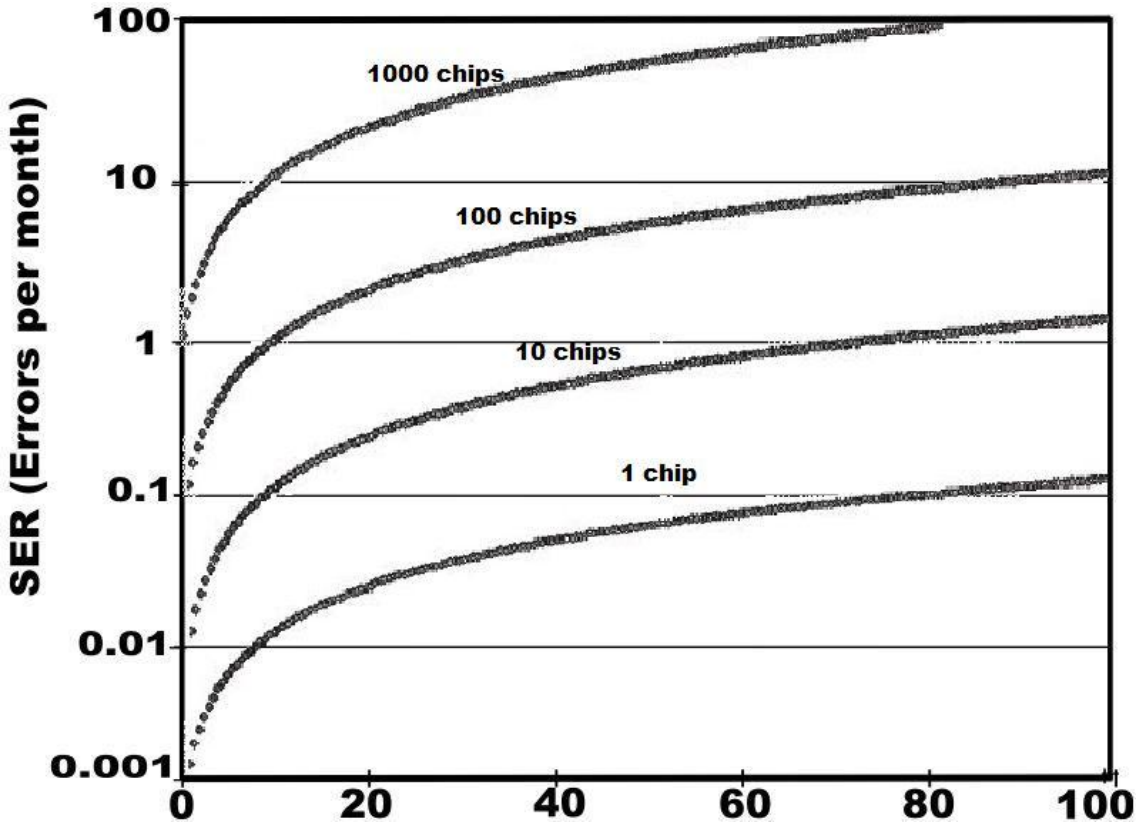


Figure 1.1: SRAM Integration vs. Soft Error Rate (BAUMANN, 2005)

Another important issue about the usage of ICs is that they are fabricated to operate at different environments that also result in different doses of radiation. This is an important point because the common radiation at zero altitude is different from those founded at higher altitudes. Issues about environment conditions will be discussed at chapter 2.

The work done by Hazucha, (2003) evaluates supply voltage scale correlated with the SER generated by neutrons. In figure 1.2 the author presents results for test chips using 90nm, 0.13um, 0.18um and 0.25um technologies. It is clear that for all technologies the supply voltage scaling for smaller values imposes increases at the soft error rate, as also mentioned by (BAUMANN, 2005). The author had analyzed this behavior for PMOS and NMOS diode and has found similar results for the devices.

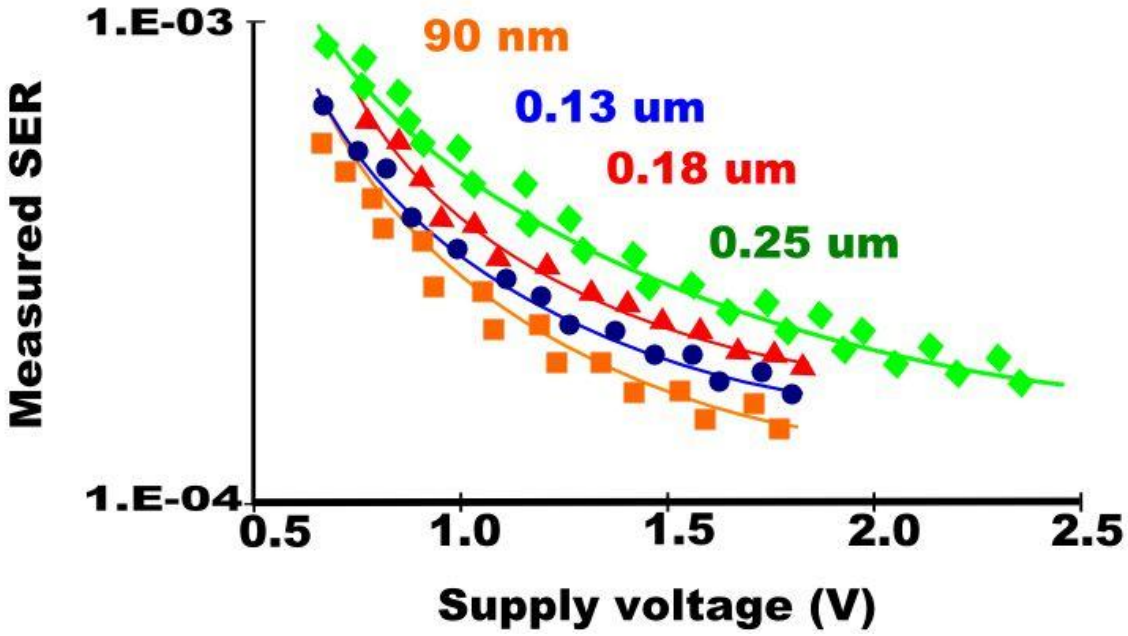


Figure 1.2: PMOS Diode SER vs. Supply voltage (HAZUCHA, 2003)

The industry and academic institutions have been studying the problems caused by radiation in ICs and some approaches are already know to reduce the problem and make the components less vulnerable to some doses of radiation. The space and avionics industry have a particular interest in research about radiation effects because of the higher doses of radiation that are founded in higher altitudes and space.

The necessity of allowing circuits to tolerate radiation effect, has promoted researches about fault tolerance of radiation effects field at many abstraction levels. Techniques to enhance circuits tolerance to these effects may be applied at all levels of the development of a circuit going from early project decisions and specifications, to techniques applied at fabrication level. One important issue about radiation effects is that they can be permanent or transient and each of them requires different approaches to reduce their effects on devices.

The main motivation of this work is the necessity to evaluate transient radiation effects at nanometer technologies. The analyses of the effectiveness of mitigation techniques like transistor sizing using an accurate simulation tool is required since geometry properties of regions that are impacted by the ion are changed. The transistor folding technique was also evaluated since it is a common layout decision applied by designers to allow the regularity of layout cells with the same width. One important point of this work is that this research field is considered a key area of investigation to all countries that expect to develop a space industry or even avionics instruments which must be also hardened against radiation.

The transistor sizing technique which will be discussed in Chapter 3 is a technique applied at electrical level. The use of the technique to mitigate SET was first proposed by (ZHOU, 2006) and consists of an increase in the transistor width to allow an increase of the total capacitance of the node which contributes to the reduction of the injected pulse. Since this technique is applied and tested at electrical level, no information's about the ion that impact the device and none of geometry and doping characteristics of the device are evaluated. This dissertation is the first work that evaluates the technique at device level.

Other technique that was also evaluated for SET robustness for the first time is the Transistor Folding. The technique is not applied with the purpose of mitigating radiation effects and is used by layout designers to allow the regularity of cells using a same width having a directly impact during the floor planning and placement of the cell. This dissertation is also the first work to evaluate transistor folding impact for transient radiation effects.

1.1 Methodology

In figure 1.3 the complete methodology used in this work is shown. The first step was the research of technology specifications to build a model of the device that would be used during simulations. At this step the main issues were to obtain device and geometry profiles of the transistors to be used in simulations.

The second and third step consist in the generation of the MESH and simulations to evaluate if the device has the desired behavior. The following step is done simulating predictive models at spice level and comparing the behavior of the modeled device. If the device doesn't have the desired behavior it must return to possible refinements.

After the device is validated, analyses of radiation simulations are done. The tool Stopping and Range of Ions in Matter - 2008 (ZIEGLER, 2008) is used to obtain ion profiles and those are injected at the device by Davinci (SYNOPSYS, 2006). Once these simulations are done the results can be evaluated.

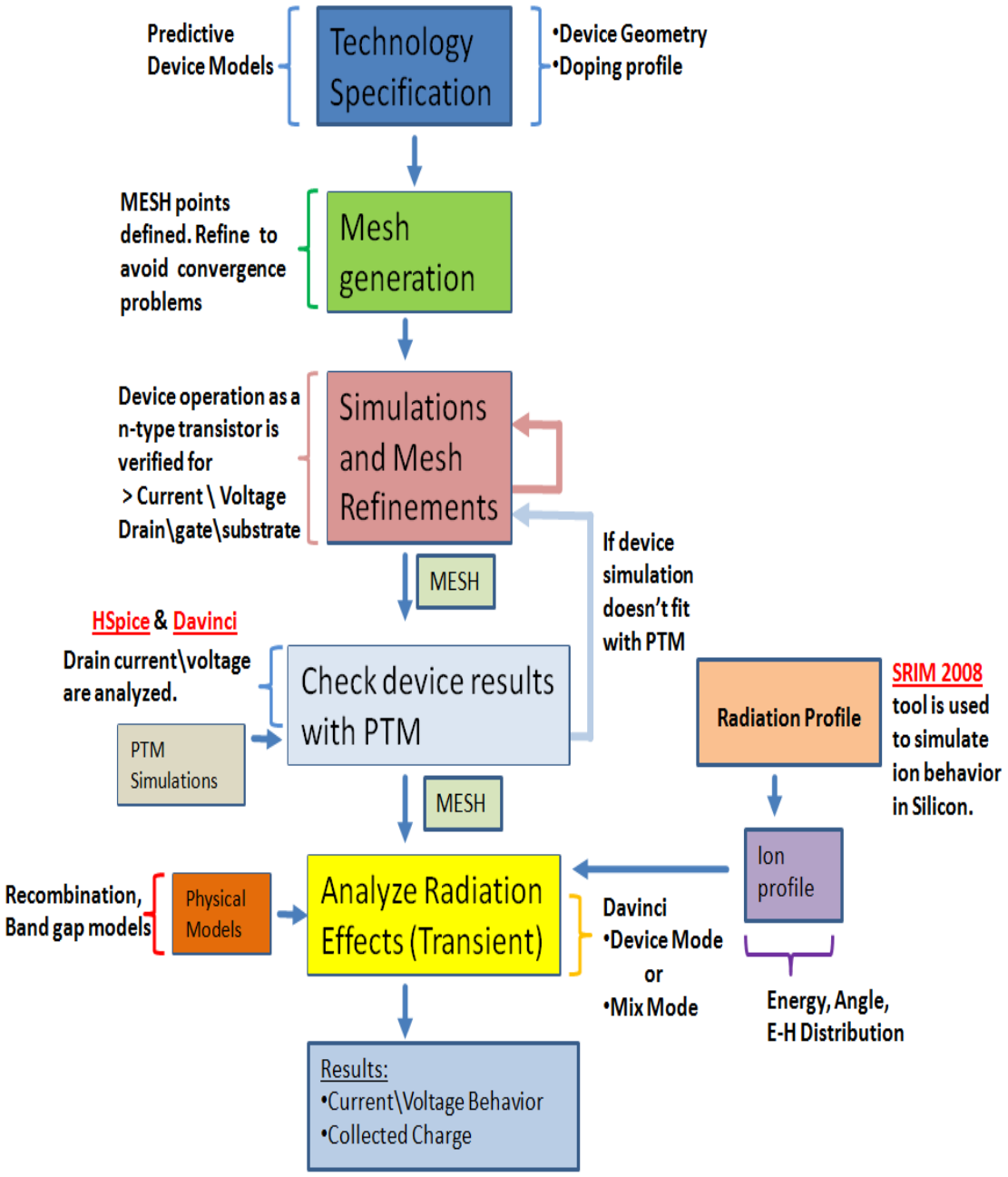


Figure 1.3: Methodology of simulations

Notice that for standalone electrical simulations the HSpice tool from Synopsys is used to evaluate transistors behavior. For device simulations and mix-mode simulations the tool Davinci also from Synopsys is used. For radiation profile and the evaluation of the linear energy transfer of ions the tool SRIM 2008 is used. At next section the thesis organization is detailed.

1.2 Dissertation Organization

This dissertation is organized as follows. In chapter 2 the main radiation sources and Earth environment is discussed. Radiation effects and main mechanisms to the generation of transient effects are approached in section 2.2, and in section 2.3 techniques used to detect and mitigate transient and permanent effects are briefly discussed. In section 2.4 the main radiation equations and models are briefly presented.

In Chapter 3 predictive models used to build the test device is presented. In Chapter 4 issues about ion profiles are discussed. In section 3.4 ion profiles used to irradiate the devices are presented with the tool used to evaluate the interaction of each ion with silicon.

In chapter 5 the transistor sizing technique is presented and the devices used during irradiation are showed. In section 4.2 and 4.3 results and main conclusions are approached.

In chapter 6 the folding technique is discussed and the devices modeled to simulations are presented. Section 5.2 and 5.3 include results and main conclusions. In chapter 7 main conclusions of the dissertation are discussed.

2 RADIATION OVERVIEW

Radiation is defined as energy in transit as high-speed particles or electromagnetic waves (YAVORSKY, 1972). Its classified as ionizing and non ionizing radiation. Ionizing radiation has sufficient energy to create charged particles (ions) from atoms by removing electrons. Non ionizing radiation has low energy and cant strip electrons from the orbit of other atoms, so it's not able to create ions, besides that non ionizing radiation is only able to disturb others atoms when collide with another atom. The ionizing radiation is able to interact with other particles by Coulomb interaction which allows this kind of particle to disturb a higher number of atoms of the lattice structure of the device (TEODORESCU, 2005).

When analyzing radiation effects, the kind of ion that is most common at the environment will have strong impact on simulations. For example, simulations with neutrons deal with a non ionizing radiation that creates energy by the impact of the neutron with ions used at the doping of the device as shown in equation 2.1. This reaction may also create an ionizing radiation which makes this simulation more complex to simulate and requires specific tools.

$$^{10}B + n \rightarrow Li^{7}(0.84\,MeV) + He^{4}(1.47MeV) + Gamma(0.48MeV) \quad (2.1)$$
$$(ZIEGLER, 2004)$$

At the following section the main radiation sources are presented and Earth environment is briefly approached. Understand these environments are a key factor to allow a proper evaluation of radiation effects at Earth and surround space.

2.1 Radiation Sources and Earth Environment

Earth receives constantly radiation from different sources from space. The three major sources of radiation are: Sun, Cosmic Rays and Radiation Belts (on earth referred as *Van Allen Belts*). Each of these sources has their own characteristics that will be briefly discussed on the following paragraphs. Figure 2.1 shows the main sources of radiation in Earth surround space.

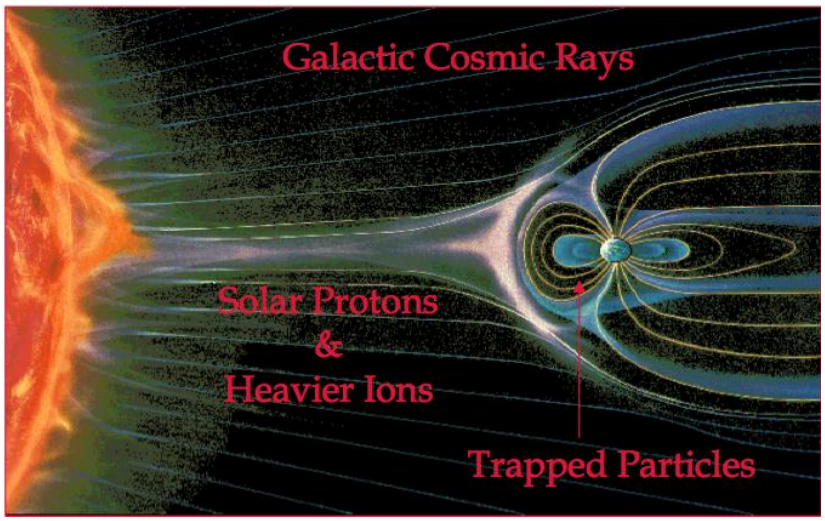


Figure 2.1: Cosmic radiation and Solar Events (BOUDENOT, 2006)

The Sun is a star at solar system with a mass of about *1.989e30 kg* with a temperature of about *5800 K* that is in constantly on activity (SEDS, 2007). The activity in the Sun generates solar winds and coronal mass ejections that continue emit particles into space. Solar Wind is a stream of particles generated by the sun and is mainly composed of protons and electrons of about *1 keV*. A coronal mass ejection (CMEs) is a sudden energy release from the Sun, generating a cloud of charged particles and is preceded by a shock wave. These particles are ejected from the atmosphere of the sun with a very high velocity.

Another important factor that contributes to the rate of upsets caused by radiation is the Sunspot Cycle as shown in figure 2.2. The Sun has a cycle of about 9 to 13 years in which the solar activity varies through a high and low period of emission of particles on the space.

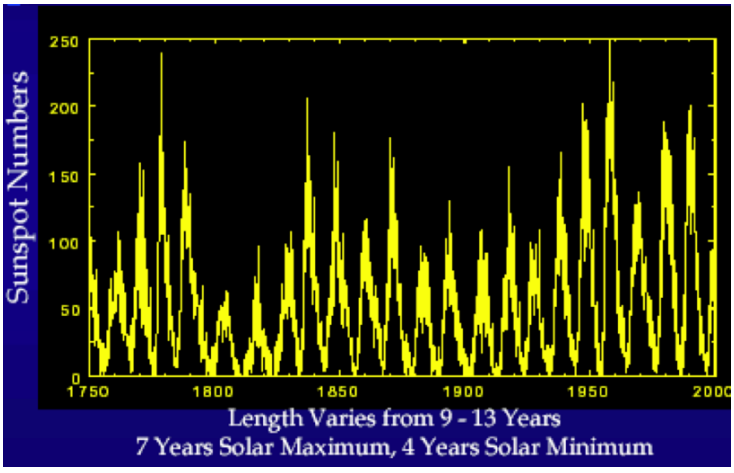


Figure 2.2: Sunspot Cycle (BOUDENOT, 2006)

The information provided by the Sunspot Cycle is used to control missions schedule and the necessary hardening to be used by satellites and space missions. The higher number of Sunspot indicates a higher number of activities and implies on higher doses of radiation that will affect electronics.

Cosmic radiation can also provoke failure in a circuit. It is composed of a mixture of interstellar material from stars, supernovae and *Wolf-Rayet Stars*. *Wolf-Rayet Stars* are massive stars that are losing mass rapidly in the form of stellar wind (BOUDENOT, 2007). *Supernovae* is a stellar explosion that creates plasma (ionized matter) and spread most part of the material of the star through the galaxy (TEODORESCU, 2005). The composition of cosmic ray is about 90% of *protons*, 9% of *alpha particles* (*He nuclei*) and about 1% of *electrons* (TEODORESCU, 2005).

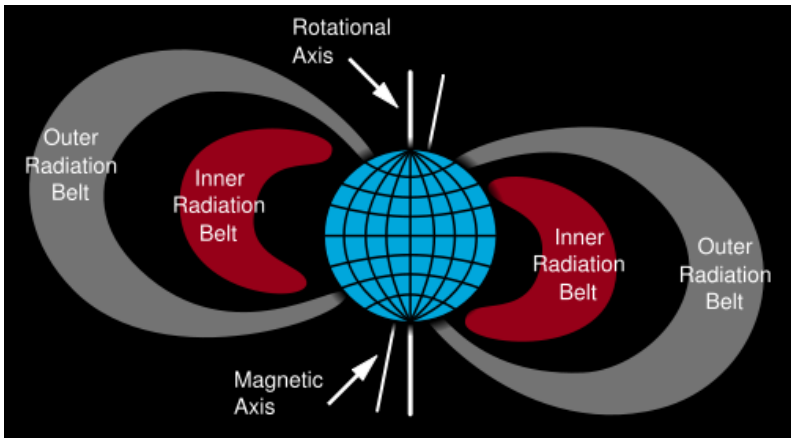


Figure 2.3: Van Allen Belts (BOUDENOT, 2006).

Particles generated from outer space and solar winds when near earth are influenced by earth magnetic field. This influence captures some of these materials and creates belts called *Van Allen Belts* (TEODORESCU, 2005). Earth *Van Allen Belts* are composed of two belts each one with their own characteristic. In figure 2.3 the Van Allen Belt. The outer belt is at about *13.000 km* and *65.000 km* of altitude and is mainly composed of *electrons* and some *ions*. The major range of energy of these particles is between *0.1-10.0 MeV*. The inner belt extends from *700 km* and *10.000 km* of altitude and the major composition is of *protons* and some *electrons*. The *protons* from inner belt can reach *100 MeV* and the *electrons* about *100 keV* (TEODORESCU, 2005).

Understanding of the *Van Allen Belts* is critical to space programs of space industry. Commercial and Military satellites must avoid areas of high radiation to make possible the property work of their system, and to increase their lifetime. In space travels the *Van Allen Belts* are also critical. Besides the problems that high doses of radiation can cause on electrical devices, astronauts also suffer effects and must be preserved of this kind of exposure.

The interaction of particles from the sources discussed before with Earth magnetic field has not the same influence for all regions of the planet. In figure 2.4 it is showed what is called *South Atlantic Anomaly* (SAA), a region of high incidence of radiation particles from the space. The red zone indicates a high number of incident particles and blue zones a low number of particles. This anomaly is justified due to the asymmetry of Earth magnetic field which drives a large number of particles for the red zones. This asymmetric behavior is not constant and the anomaly moves with changes in the magnetic field.

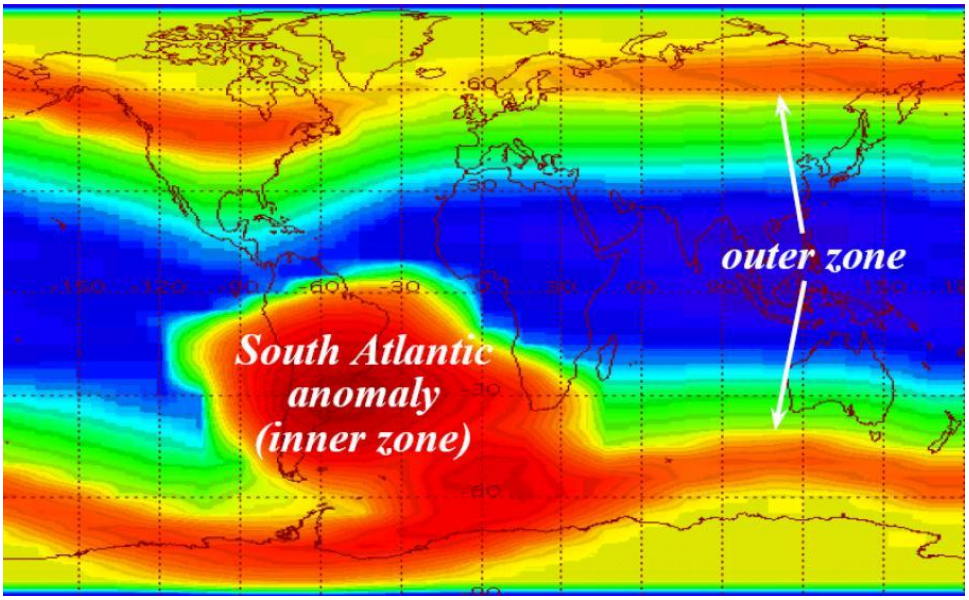


Figure 2.4: South Atlantic anomaly (BOUDENOT, 2006)

The confirmation of the effect of the SAA in electronics came with the analysis of the number of measured soft errors at experimental tests over the environment using memory cells. At (DYER, 96) the author brings the measurements of SEE at different environments including SAA region. In figure 2.5 the SAA and measured soft error rate.

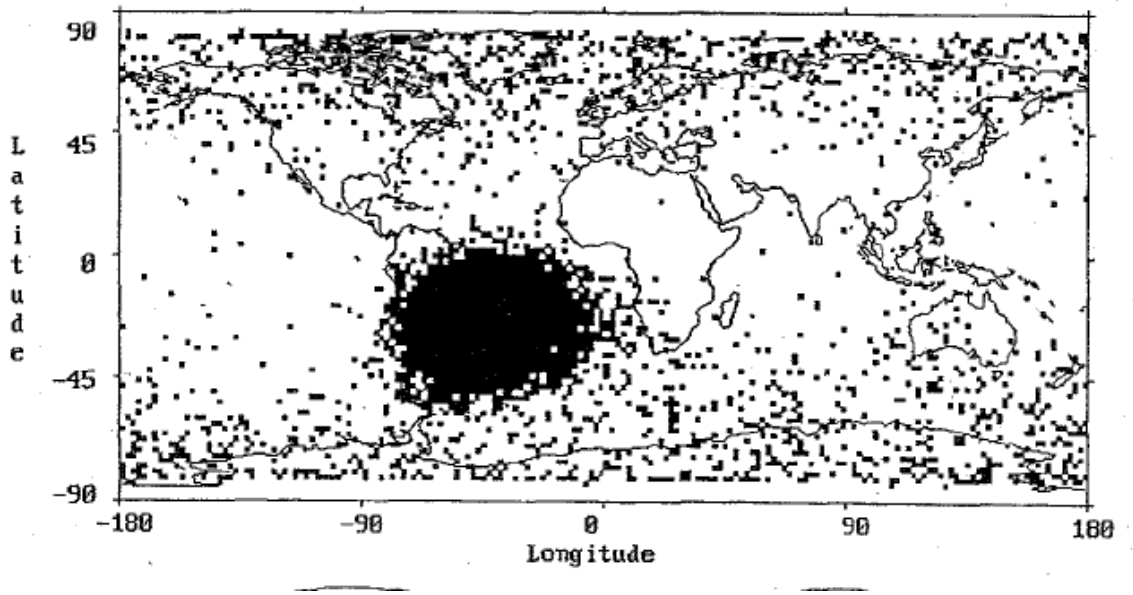


Figure 2.5: Soft Error Rate at Earth (BOUDENOT, 2006)

Besides these primary sources of radiation there are also secondary radiation sources that are the result of radiation interaction (of primary sources) with earth environment. This interaction generates other range of particles kind and energy making this study more important to understand the radiation environment at Earth atmosphere. In figure 2.6 it is showed the interaction of particles from the space with earth atmosphere.

When interacting with the atmosphere the radiation particle suffers collisions with atoms, liberating *electrons, protons, neutrons* and streams of *alpha, beta and gamma* decay. But the main component generated by these collisions is the *neutron*, which is

the main cause of upsets in ICs at sea level. In the Figure 2.6 electromagnetic component are the *electrons* and *gamma decay*. *Hadronic* components are *hadrons*, a subatomic particle composed by *quarks* and *antiquarks*. *Measonic* component are *measons* a kind of *hardron* with high force of interaction. *Hardrons* and *measons* are all subatomic particles generated by nuclear reactions. For currently technology hardrons and measons does not have significant effect in ICs, as they have a too low energy, to interact with MOS transistors elements.

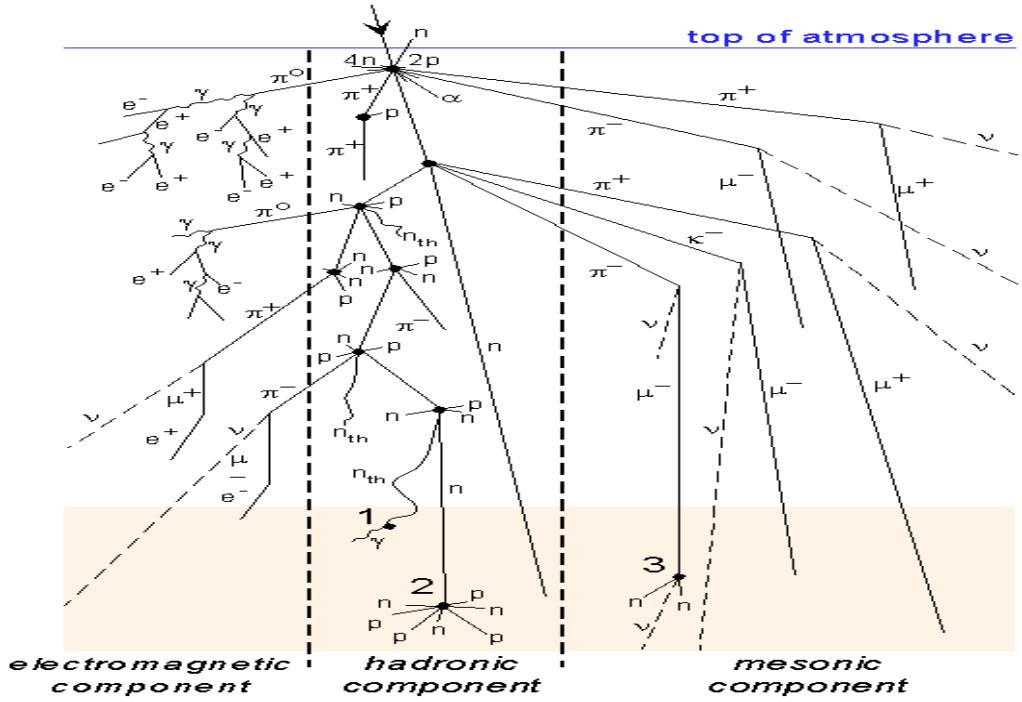


Figure 2.6: Radiation interaction with atmosphere (DALHOUSIE, 2008)

As mentioned before, neutrons are the main concern type of radiation at Earth atmosphere therefore studies are done to model these environments. At (BAKER, 1993) the author creates Neutron Flux model to evaluate the rate of neutrons at different altitudes and latitudes. At (LERAY, 2004) the effects of Neutron on IC are approached.

The *Neutron Flux* is studied to create a profile of regions with lower and higher doses of neutrons. These data are important to detect the places on Earth with higher probability to suffer effects of radiation. The atmospheric neutron model (equation 2.2) proposed by BAKER using altitude and latitude informations is presented at the following. In figure 2.7 is presented the relation between altitude and neutron flux.

The rate of neutrons increases with the altitude indicating the necessity of a higher protection to electronics operating in these environments. This increase has directly impact in soft error rate since with more particles the probability of errors increases, besides the fact that increasing the altitude the range of the energy of the particles at these environments also increases. The following equation is proposed by BAKER to obtain the neutron flux using altitude informations.

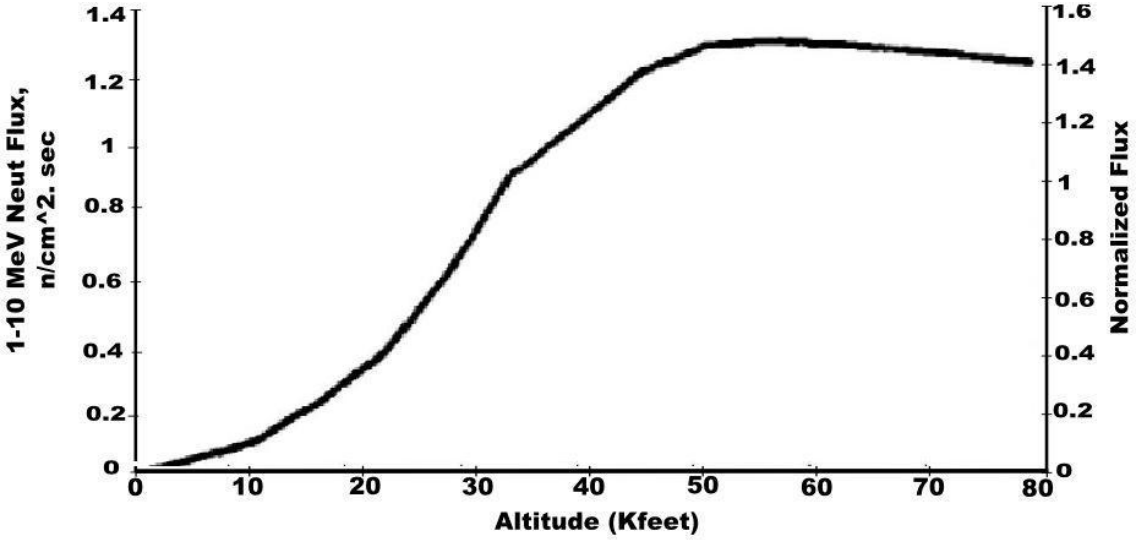


Figure 2.7: Altitude vs. Neutron Flux (BAKER, 1993)

$$x = 1033exp\left[\begin{Bmatrix} -0.04534 - (1.17E-9)x \\ |(A-1.05E5)/1E3|^{3.58} \end{Bmatrix}(A/1000)\right] \quad (2.2)$$

The neutron flux and its relation with the latitude is also modeled by BAKER. The Neutron flux also increases with higher altitudes. This difference can be understood by the studied of the asymmetric magnetic field of Earth which concentrates the radiation particle at higher latitudes (BAKER, 1993). In figure 2.8 it is shown the relation between the latitude and the flux of neutrons. The equation 2.3 represents the model proposed by BAKER to latitude.

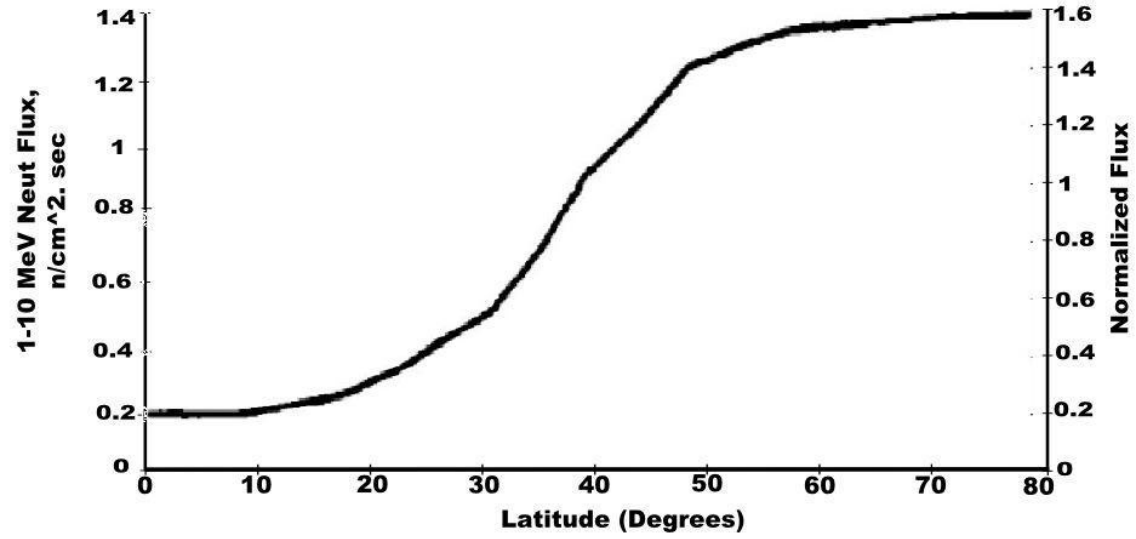


Figure 2.8: Neutron flux vs. latitude. (BAKER, 1993)

$$\emptyset_{1-10}(Lat) = 0.6252exp\begin{Bmatrix} -0.461[\cos(2xLat)]^2 \\ -0.94\cos(xLat) + 0.252 \end{Bmatrix} \quad (2.3)$$

Using models of the radiation environment like the presented BAKER it is possible to predict the radiation level and the expected upset rate for electronic devices. These informations are useful to understand the ion profile in the environment on which the electrical device will be exposed.

There are other resources that models space environment. For space weather information and detailed flux of electrons, protons and heavy ion flux consult NASA space weather site at (NASA, 2008b). For specific information about environments and measurements of radiation in Earth consult the Cosmic Ray Energetic and Mass (CREAM) project of NASA and University of Maryland at (NASA, 2008a). In next section the main radiation effects in circuits are discussed.

2.2 Radiation Effects

Radiation effects can be classified as transient or permanent effects. Transients effects are those that have a specific duration of time and will eventually disappear. Permanent effects are not related with the time and will not disappear with the time. Some of the main radiation effects in integrated circuits are classified as follows (Kastensmidt, 2003):

a) Permanent effects
    a. *Total Ionizing Dose* (TID)
    b. *Displacement Damage* (DD).
b) Transient effects
    a. *Single Event Transient* (SET)
    b. *Single Event Upset* (SEU)
    c. *Single Bit Upset (SBU) and Multiple Bit Upset* (MBU).

There are other effects that will not be approached in this work like: *Single Event Functional Interruption* (SEFI), *Single Event Gate Rupture* (SEGR) and *Single Event Latchup* (SEL). In the following paragraphs it is presented a briefly discussion about each permanent and transient effect listed before.

A Total Ionizing Dose occurs in a semiconductor or insulating material during the creation of electron-hole pairs. In the gate and in the substrate the electron-hole pairs quickly disappear since these are conductive materials with low resistance, but in the oxide which is an insulator (high resistance) only a fraction of electron-hole pairs recombine immediately after creation allowing the appearance of void regions that will degrade the device. When a positive bias is applied to the gate, the electrons are attracted to the gate and holes are moved towards the dioxide of silicon interface creating trap regions (LIU, 2007). This continuo ionization makes the threshold-voltage of the device shift and provokes also the mobility degradation of the gate (DUSSEAU, 2007). In figure 2.9 the TID mechanism is shown.

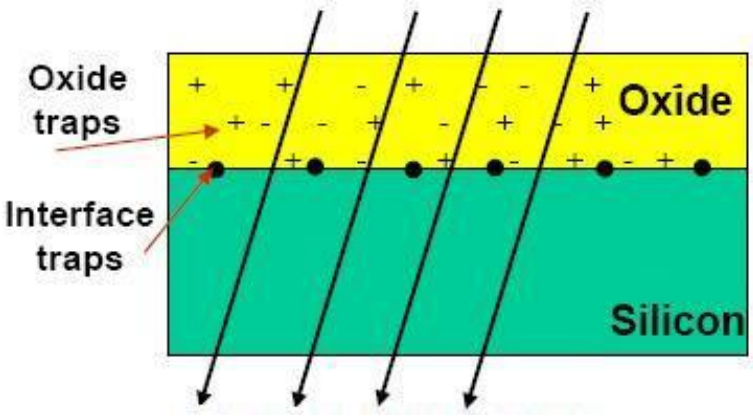


Figure 2.9: Total Ionizing Dose mechanism (ECOFFET, 2007)

It is important to notice that the main effect of TID is over the oxide and interface. In figure 2.9 the recombination of electron-hole pairs is low and so the electrons and holes are free to move when a bias is applied at the gate. In figure 2.10 it is shown the increase of the radiation dose and the effect of TID in device threshold.

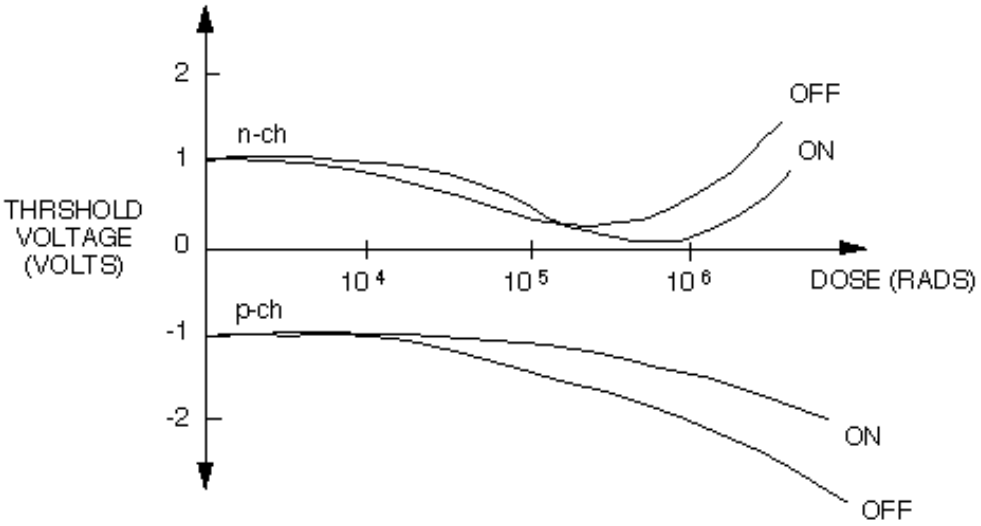


Figure 2.10: Threshold shift during radiation (NASA, 1993)

In the test done by (NASA, 1993) the n/p-channel are irradiated and the threshold is evaluated during the test. Since this is a cumulative event, it is expected that the shift of threshold increase over the time. The leakage current will also increase due TID effect. The TID must be mitigated to ensure the lifetime of electronics in space environment. To ensure that an electrical device is able to be used in a space project, the device pass through a qualification test in which each device is irradiated with incremental doses of radiation (COCHRAN, 2005).

Another permanent effect is the Displacement Damage, which is the result of nuclear interaction of the incident particle, causing the displacement of atoms of the device to other regions. This kind of interaction can be done by the primary particle or other secondary particles that were generated through the interaction of the primary

particle with the device material (SROUR 2003). At DD most of energy is transferred when an atom is knocked (DUSSEAU, 2007). The DD mechanism is shown in figure 2.11.

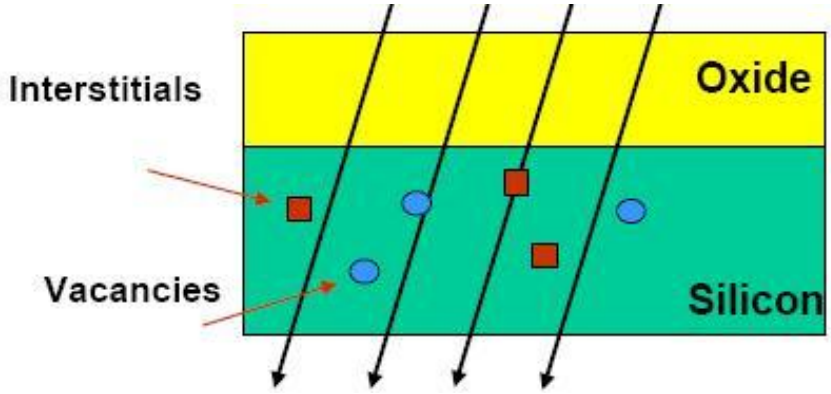


Figure 2.11: Displacement Dose mechanism (ECOFFET, 2007)

In figure 2.11 interstitials are atoms dislocated by the radiation particle to regions between atoms of the lattice structure of silicon. Vacancies are unoccupied regions of the lattice structure of silicon (ECOFFET, 2007). The DD cause permanent defects over the device and it main effects are the degradation of gain and leakage current in bipolar transistors. In figure 2.12 the Non-Ionizing Energy Loss (NIEL) is shown. NIEL is the rate in which a non-ionizing energy is lost at the device. The picture shows the decreasing of device lifetime during the radiation of Protons.

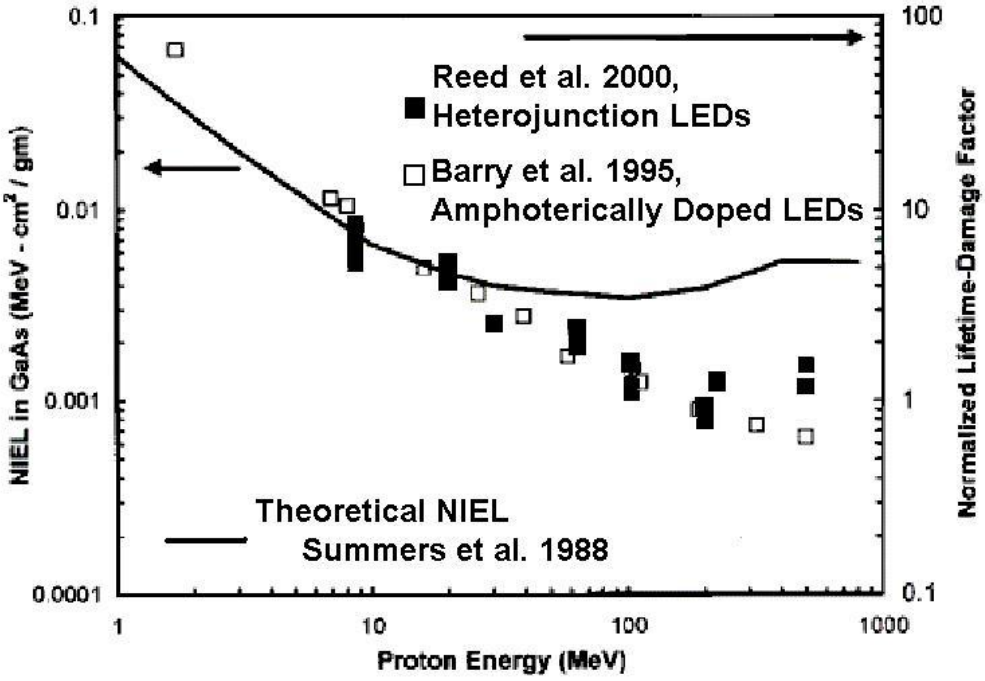


Figure 2.12: DD effect on lifetime. (DYER, 2006)

Besides permanent effects, there are also transient phenomena. In figure 2.13 the mechanism of soft error generation is shown. In the picture it is seen a cross-section of the Drain of a transistor. A p-type substrate with an active region of n-type is showed, as a part of a n-type transistor. In the figure it is considered an abrupt-junction to simplify the mechanism. The mechanism of generation of a single event effect occurs during the passage of the ion over the drain (*pn junction*). During this event the ion generates a burst of electron-hole pairs that will be distributed over the device. This passage makes the funneling of the electric field of the charged region. This funneling will be able to collect e-h pairs that will be generated out of the drain volume (HU, 1982). Basically carriers will move to the charge region by drift due to electric field and diffusion due to the large concentration of carriers during the ionization. The distribution of carriers will have a directly impact over the collected charge since carriers concentration will have impact on carrier recombination that will also have an effect over the collected charge.

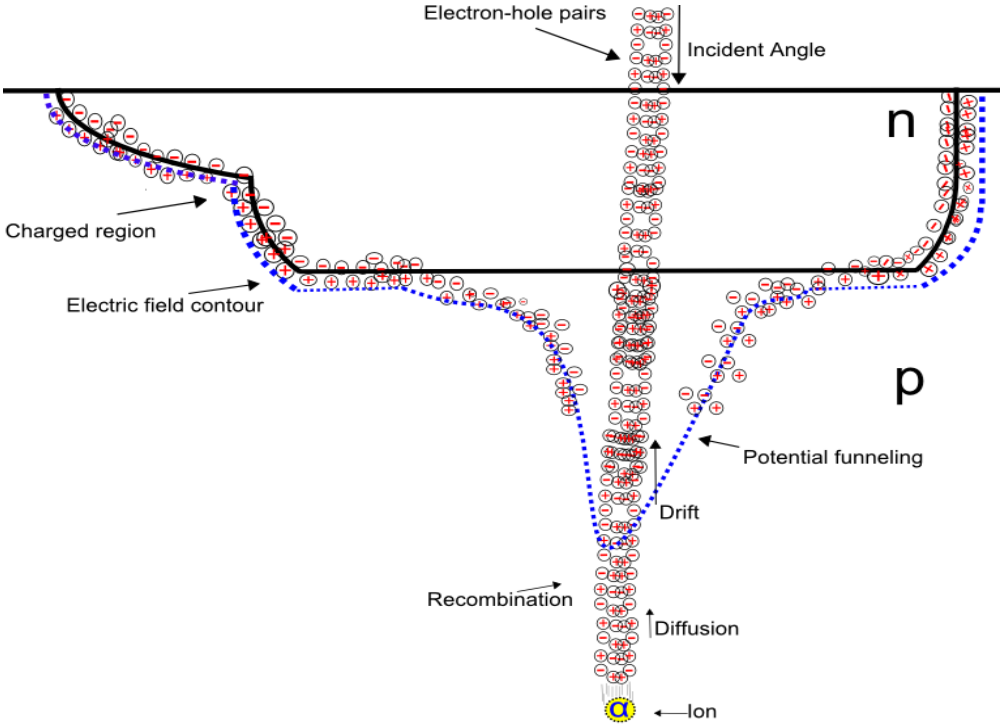


Figure 2.13: Soft error mechanism

The mechanism described before can generate an effect that is called single event effect (since generally occur in just one device) or even referred as a soft error. When this event occurs in a sequential circuit it is called Single Event Upset (SEU) and when it happens in a combinational circuit and is able to turn into a pulse similar to the logical "0" or logical "1" it is called Single Event Transient (SET). A *SEU* is an upset caused on a memory cell and when this value become permanent (until it is written again) it is called Single Bit Upset (SBU). A *MBU* is an occurrence of multiples *SBU* by different particles or even by the interaction of one single event with multiple devices. SEU and SET events are showed in figure 2.14. In figure 2.14 it is shown a SEE generated at the combinational logic provoking a SET, and a SEE generated at the memory element provoking a SEU.

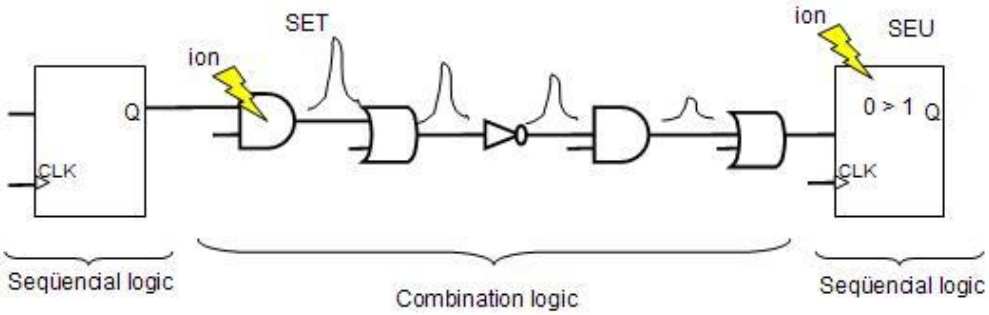


Figure 2.14: SET and SEU at logic

These events (SET and SEU) can be mitigated by different approaches at high abstraction levels. A SET depends on factors like electrical/logic/window masking factors to cause an upset in the flip-flop. An electrical masking occurs when the transient pulse is degraded by electrical characteristics of the circuits and is not able to reach a storage device. A logical masking is when the transient pulse is masked by the logic of the cell, this is shown in figure 2.15. A window masking is when the transient pulse generated in the combinational logic reaches a sequential logic element which is using a clock and at that time the clock signal was not indicating to the sequential element to store the input value.

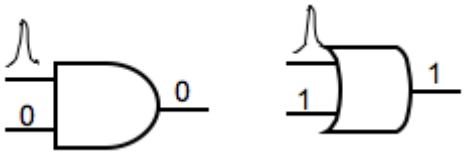


Figure 2.15: Logical Masking factor

The view of transient effects generated by a single burst of one interaction is a typical modeling for single event effects that is widely used by research community and most supported by TCAD tools. However researches have been conducted to show that more phenomena occurs inside the device having strong difference with the simplify model. It has been showed that a particle passing through the integrated circuit can provoke a chain reaction generating different kinds of events with different magnitudes. In (SCHRIMPF, 2007) the author show experimental works in which the reaction of the particle inside the silicon generates secondary reactions that will affect the device. In figure 2.16 and 2.17 it is showed two different analysis of the path of the same particle.

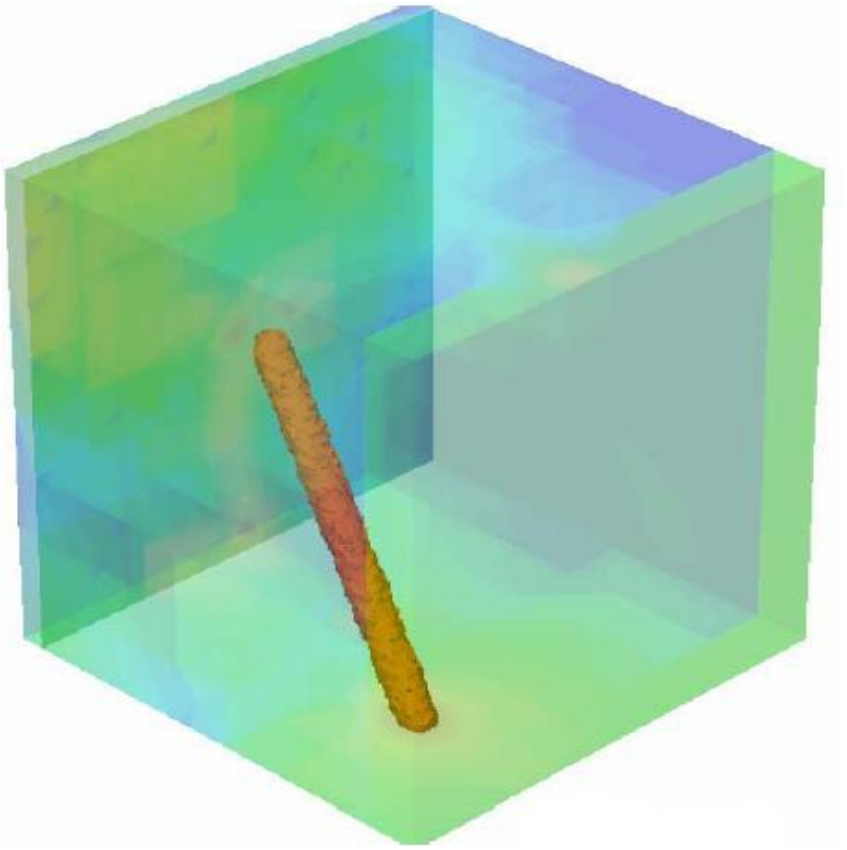


Figure 2.16: Path of a particle inside the silicon (SCHRIMPF, 2006)

The picture shows an incident particle with the generation of electron-hole pairs almost uniformly over the path without considering the possibility of second interactions. The calculation of electron-hole pair generation in this kind of situation is trivial and is the most used approach. For the event with this path and reaction interpretation the equation (2.4) of the *LET* has a great agreement with the model.

In figure 2.17 the path of the particle inside the silicon is considered using a model to analyze the secondary reactions of the primary particle.

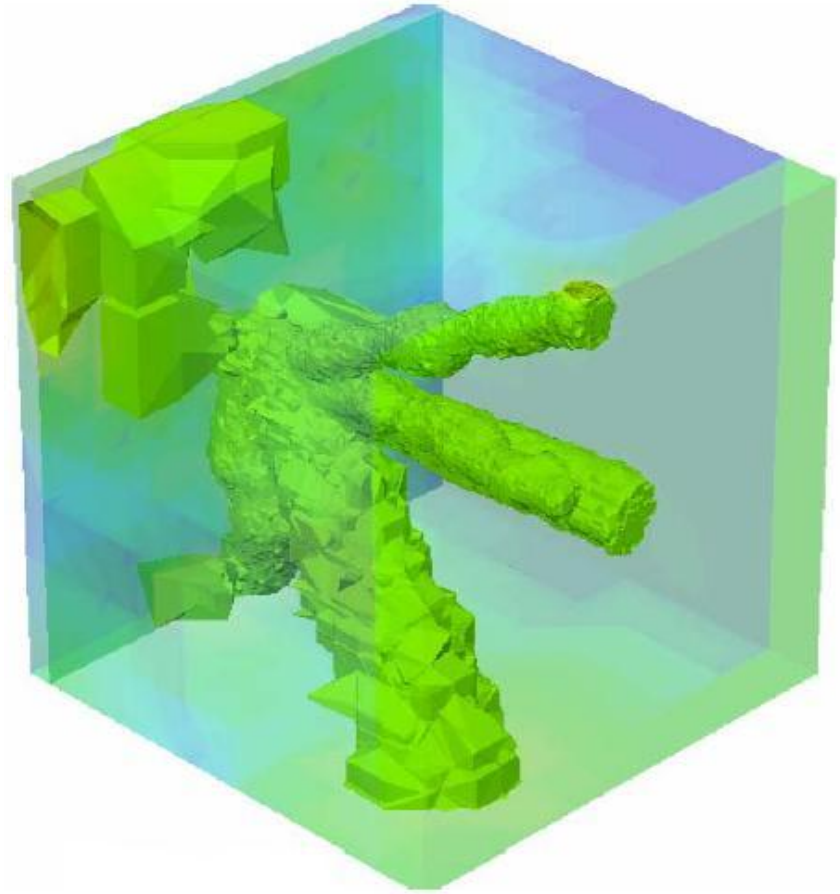


Figure 2.17: Multiple interaction of the particle (SCHRIMPF, 2006)

This picture show how complex the system can behave with a single particle. The electron-hole generation is increased with the reaction of secondary particles and with multiple paths that occur when a secondary particle moves inside the silicon generating more electron-hole pairs and maybe other nuclear reactions with more interactions.

For this kind of event the model using the basic LET equation doesn't fit anymore and it is necessary to expand the interpretation of the event to have a better agreement of the event with the basic equations. The industry is starting to know more about this kind of event and there is no much information about the calculation of the energy transference and prediction of it.

Unfortunately simulating these multiples interactions imposes the necessity of using specific tools that are very rare and most of them closed for internal use of specific research groups. In this work multiple interactions were not considered and simulations are done using the model of one single interaction. In the next section the main techniques to mitigate radiation effects will be briefly discussed.

2.3 Techniques to Mitigate Radiation Effects

Techniques to mitigate radiation effects on IC and specially ASICS can be applied in the following levels of abstraction: process, layout, electric, logic, architecture and software. In figure 2.18 a brief diagram of the abstractions levels is shown.

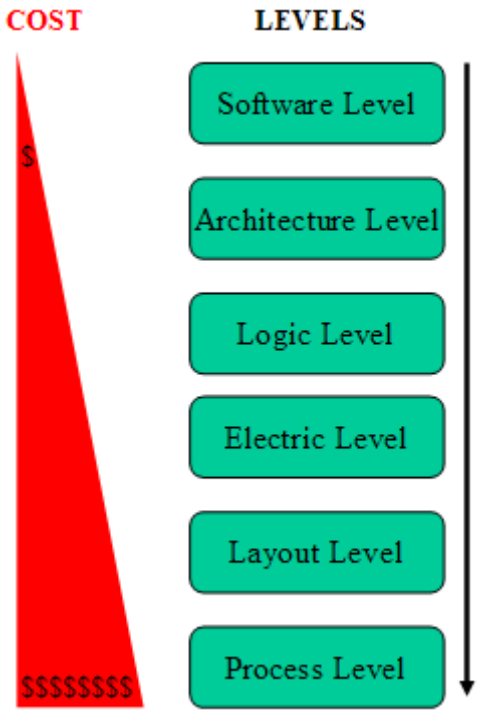


Figure 2.18: Abstraction Levels

Notice that techniques applied at higher levels generally have a lower cost of time and money when compared with lower level techniques. This occurs because higher abstraction level techniques take advantage on the simplification of the problem which they propose to solve. At higher abstraction levels the radiation effect can be seen as a simple change in a variable of a program making the resolution of the problem less complex than in lower levels. Be aware that this doesn't necessary means that higher level techniques are easier to implement since there are other considerations of the problem like the size of the system to be harden and its complexity. At the following paragraphs a brief review about each level of abstraction and the major techniques used by each one.

For process level some techniques are buried-layer implant and EPI substrate. At (ZIEGLER, 2004) these techniques are discussed and at this work they will be briefly explained. The buried-layer implant consist in a highly defect or doped layer below the device. The idea is to reduce the mobile electrons or holes concentration at this layer. As mentioned in chapter 3 the high doped area will suffer more electron-hole recombination, this will leave the other layer suffering less effects from the particle interaction.

The *Epitaxial Substrate* (EPI) is similar to the buried-layer presented before. The technique is based on using a highly doped substrate which will allow a quickly recombination of radiation particles when interacting with the layer. Consult (ZIEGLER, 2004) to an extensive discussion about these techniques.

At layout level the major techniques are: guard rings and enclosed geometries. In (CHEN, 2005) the efficiency of Enclosed Layout Transistor (ELT) to mitigate TID and

SEL is studied with n-type transistors in 0.18 um technology. As showed in the latter section one of the main effects of the Total Ionizing Dose is the shift of the threshold of the device which is a permanent effect. The ELT technique changes the design of the basic transistor layout reducing the effect of radiation to change the threshold of the device. With this new configuration showed in figure 2.19 it is required a larger number of collisions to make a significant shift in the threshold of the device.

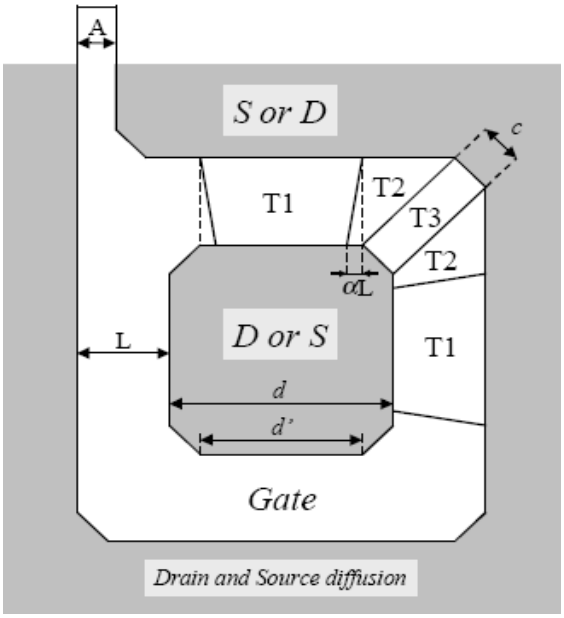


Figure 2.19: Enclosed Layout Transistor Design

The other common technique used at layout level is the guard ring. The guard ring technique (figure 2.20) consists in making a ring over the transistor and biasing this ring with the supply voltage (for p-type) and ground (for n-type). This polarization will create a dummy collector that will capture (electrons or holes) depending on the polarization. This technique will reduce the collected charge of the device and also reduce the current in the substrate. In (CLARK, 2007) the technique Guard Rings and ELT are used to reduce the leakage current of irradiated devices.

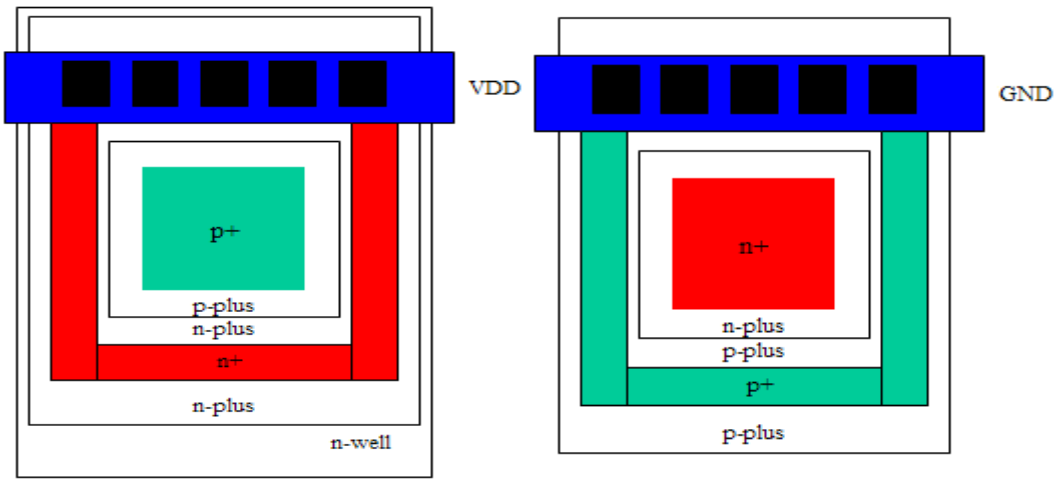


Figure 2.20: Guard Ring layout structure (RABAEY, 2003)

The techniques presented before (ELT and Guard rings) are used by (ANELLI, 2000) to mitigate TID and reduce the collected charge. This work evaluates both techniques and its efficiency to reduce errors. Note that in the layout of the figure 2.21 the ELT is not made with the same geometry showed in figure 2.19. Designers don not need to follow that geometry because the main idea of the technique is to enclose the drain/source regions inside a gate "ring" allowing the existence of an inversion channel at all the ring.

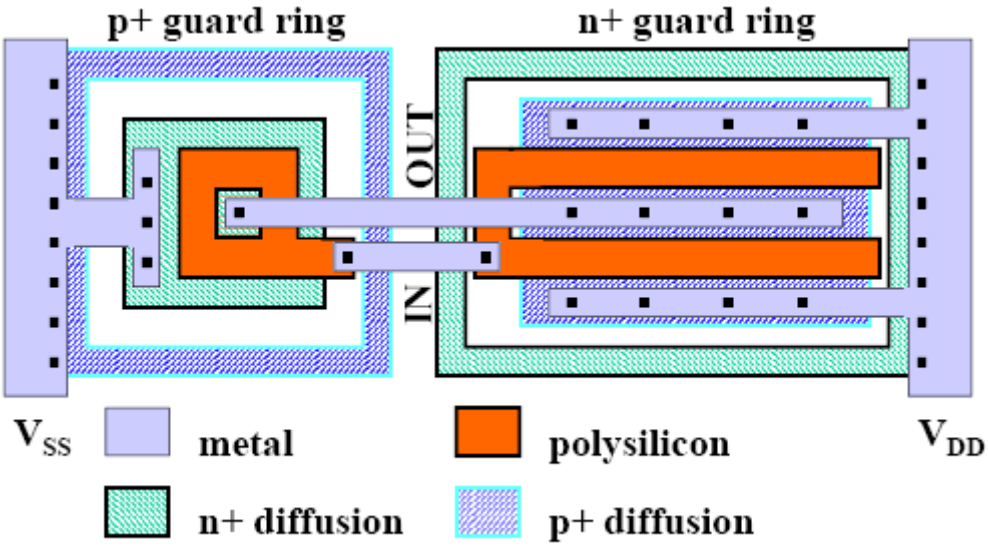


Figure 2.21: Inverter using ELT and Guard Rings (ANELLI, 2000)

At electric level many organizations of transistors are studied to avoid the propagation of the transient. In (ROCHE, 96) it is presented a not gate tolerant to total ionizing dose using a set of auxiliary transistors to control the threshold of the transistors that are damaged during the ionization.

In (ZHOU, 2006) the transistors are resized to avoid the appearance of transients, this is done increasing the width of the transistor which contributes to the increase of the critical charge of the node. In (LAZZARI, 2007) a method to use synchronous and asynchronous resizing is presented and a tool to automatic evaluate circuits is developed.

Logic level techniques can be based on space or temporal redundancy. Space redundancy techniques also called hardware redundancy are based on making copies of the protected hardware and use a voter to select the output that appears more times.

The Double Modular Redundancy technique is a detection technique since it is not able to identify the correct value. The technique proposes that two modules of the circuit should be replicated and a cell is used to compare their results. If the results are not the same, a signal must be sent to the control block to notify that an error had occurred as shown in figure 2.22. The main overhead of DMR technique is in the area of the circuit.

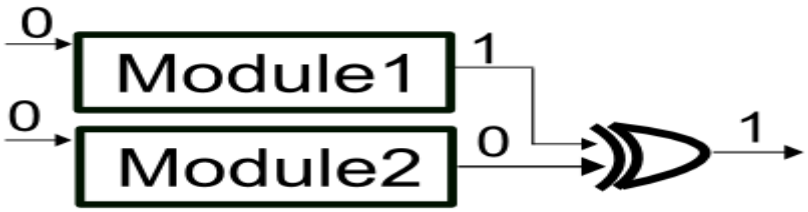


Figure 2.22: DMR (Kastensmidt, 2003)

Other hardware redundancy technique is the Triple Modular Redundancy (TMR) described at (RUI, 2006) and (CHEN, 2006) shown in figure 2.23. The technique is similar to the DMR but includes other module and a voter. The technique is able to detect the correct value since it votes for the dominant result. The technique will not vote correctly if there are more than one error of if the error occurs at the voter. There are specific techniques to protect the voter, these will not be approached at this work.

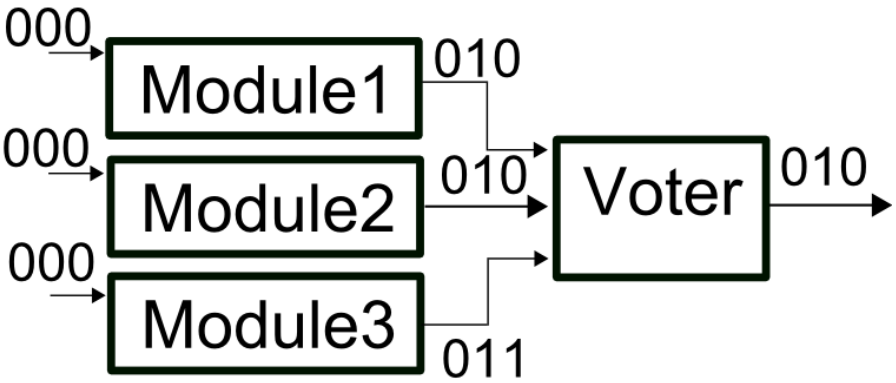


Figure 2.23: Triple Modular Redundancy technique

Another commonly used technique at logic level is the Temporal Redundancy (TR) which is based on the use of a delay inside the circuit to compare samples of the signal that is being transmitted with the possibility to filter the transient. Using the architecture showed in figure 2.24 the technique is able to detect the error, but not to correct it.

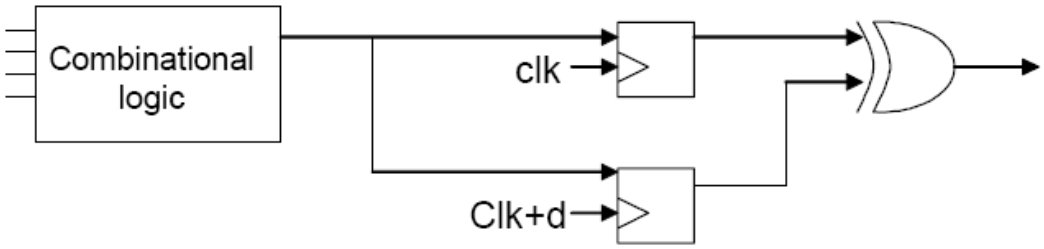


Figure 2.24: Time Redundancy Technique (KASTENSMIDT, 2003)

The TR technique can be extended to compare more than one sample of the signal. Using another module to have one more sample of the signal allows TR detects the correct value. This will decrease the performance of the circuit but will allow the mitigation of the soft error, as seen in figure 2.25.

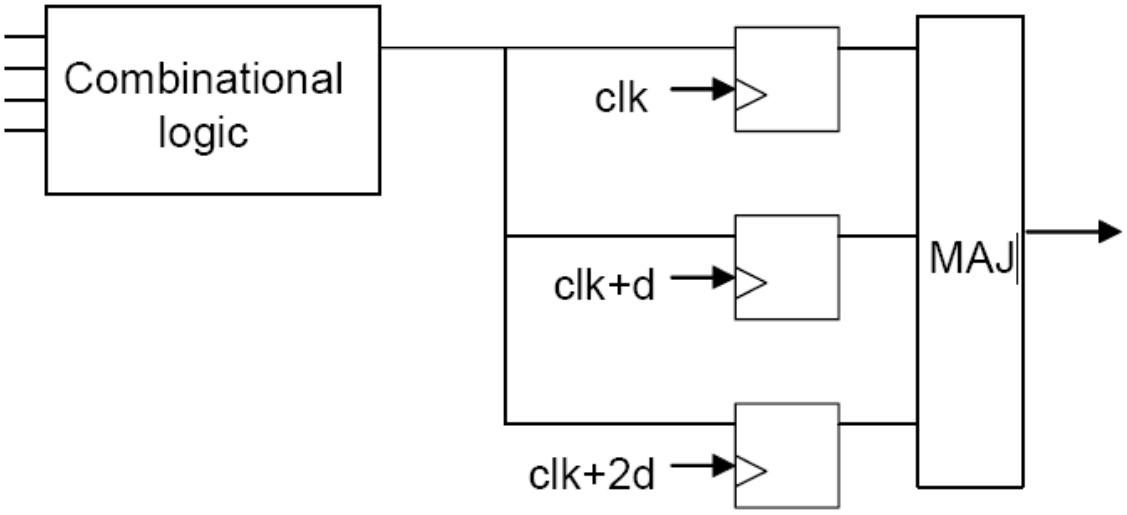


Figure 2.25: Full Time Redundancy (KASTENSMIDT, 2003)

At architecture level the techniques are closed related with the system architecture and can combine a mixture of hardware, software and temporal redundancy. In (FRIEND, 92) the author approaches the design of critical real time applications tolerant to soft errors. In the work of FRIEND the processor of the architecture was designed to verify the integrity of the data using triggers to detect possible faults. The author had also used a software layer to verify the correct operation of the application.

At software level the techniques take the concepts of space and temporal redundancy and apply the techniques at the software level. The techniques can be directly applied at the code that must be protected or can be used an Operating System (OS) to protect the application. In (ANDERSON, 85) the author analyses different software level approaches like redundancy use of variables and recomputation to mitigate transient effects.

Other approaches protect devices without direct contact with the integrated circuit. In (TRIPATHI, 2006) the author describes techniques that use electric-static fields to protect the integrated circuit against ionizing radiation. Other techniques related to the detection and mitigation of soft errors in FPGAs were not approached in this section since this is not the focus of this work. For FPGA mitigation and detection techniques consult (KASTENSMIDT, 2006; KASTENSMIDT, 2007).

2.4 Main Equations and Models

The main value used to refer to ion profile during radiation simulations is the Linear Energy Transfer (LET). The LET is the measurement of energy transferred from the ion to the material per unit distance (FACCIO, 2007) and is given by equation (2.4).

$$LET = \frac{dE}{dX} \quad (2.4)$$

where *dE* is the average energy locally transmitted to the medium by a charged particle in traversing a distance of *dx* and its unit is given by keV/um. The impact angle

of the ion also contributes to characterization of the energy transfer. The Effective LET is the effective energy that is transferred to the material and is given by (2.5).

$$LET_{effect} = \frac{LET}{Cos\theta} \quad (2.5)$$

Where LET is the Linear Energy Transfer calculated by (2.4) and $Cos\theta$ is given by the angle between the vector of the ion, and an orthogonal line to the plane of the device. In radiation effects works the LET is generally expressed in MeV/(mg/cm^2), this value is obtained by equation (2.6) given by

$$\left[\frac{MeVcm^2}{mg}\right] = \left[\frac{MeV}{cm}\right] \div \left[\frac{mg}{cm^3}\right] (2.6)(SCHIRMP, 2006)$$

where [MeV/cm] is the LET of the ion and [mg/cm^3] is the mass density of the device. The reader must understand that when using this kind of unit the LET is now dependent of the target material. The number of electron-hole pairs generated by the ion inside the silicon can be obtained by equation (2.7) given by

$$\left[\frac{\#EHPs}{cm}\right] = \left[\frac{MeVcm^2}{mg}\right] \times \left[\frac{mg}{cm^3}\right] \div \left[\frac{3.6eV}{EHP}\right] \quad (2.7)(SCHIRMP, 2006)$$

where the $\left[MeVcm^2/_{mg}\right]$ is the LET of the ion, $\left[mg/_{cm^3}\right]$is the mass density of the material and $\left[3.6eV/_{EHP}\right]$ is the quantity of energy that is required to create an electron-hole pair in the silicon.

In electric abstraction level other approach is generally used to refer to ions. The energy of the ion is commonly expressed in the form of deposited charge which can be calculated by (2.8) and is expressed in Coulombs. To convert typical LET units to Coulombs for Silicon (Si) devices use (2.9)

$$[pC] = \left[\frac{pC}{um}\right] * [d] \quad (2.8)$$

$$\left[\frac{pC}{um}\right] = 0{,}0446 * \left[\frac{MeV}{um}\right] \quad (2.9)$$

In equation (2.8) the deposited charge is given in [pC], the [pC/um] is the LET of the ion that can be obtained in this unit using (2.9) and [d] is the ion range at the device and is given in [um].

Another parameter that is generally evaluated is the Critical Charge. The Critical Charge is defined as the minimum quantity of energy that is needed to disturb a transistor or a cell and is calculated by measuring the capacitances of the device which is been evaluated. The critical charge can be calculated by equations 2.10a and 2.10b (ZIEGLER, 2004):

$$Q_{crit} = \int_0^{V_{TRIP}} (C_{TOTAL} + 2C_{COUPLE})dV + n \times I_{N,P} \times T_{PULSE} \quad (2.10a)$$

$$C_{TOTAL} = C_{GON} \times A_N + C_{GOP} \times A_P + (C_{GDON} + C_{GDLN}) \times w_N + (C_{GDOP} + C_{GDLP}) \times w_p + \left(C_{JAN} \times A_{DN} + C_{JSWN} \times w_N\right) + (C_{JAP} \times A_{DP} + C_{JSWP} \times w_p) \quad (2.10b)$$

Where V_{TRIP} is the standard voltage of technology, C_{TOTAL} is the total front-end capacitor, C_{GON} and C_{GOP} are gate capacitances of N/P transistors, A_N and A_P are gate area of N/P transistors respectively, C_{GDON} and C_{GDP} are bias-independent part of the overlap capacitance, and C_{GDLN} and C_{GDLP} are bias-dependent overlap capacitance. Source and drain junction capacitance are C_{JAN} and C_{JAP}, and sidewall capacitances are C_{JSWN} and C_{JSWP} respectively (ZIEGLER, 2004).

The relation between Threshold Effective LET and critical charge (Q_{critic}) can be obtained by equation (2.11).

$$Q_c = \frac{(L_{Th} * T * d * e)}{x} \quad (2.11)$$

where L_{th} is the *Threshold Effective LET*, T is the *device thickness* (*2.32 g/cm^3 for Si*), d the *material density* and e the *electronic charge* ($e = 1.602 \cdot 10^{-7}\, pC$) , and x is the energy needed to create an electron-hole par, x = *3.6 eV* in *Si*.

To simulate the current generated by the particle strike the double exponential equation of (MESSENGER, 1982) is used. The equation is given by equation (2.12)

$$I_{in}(t) = I_0 \left(e^{\frac{-t}{\tau_\alpha}} - e^{\frac{-t}{\tau_\beta}} \right) \quad (2.12)$$

where I_0 is the maximum current, t is the simulation time, τ_α is the collection time constant of the junction and τ_β is the ion-track establishment time constant. The last two parameters are process dependent. In (NASEER, 2007) authors analyze different equations to model the soft error and compare their results with physical simulations. The results of NASEER have shown that the equation (2.12) fits with device simulation behavior for low energy particles. In Figure 2.26 the equation I_{in} is used to plot the behavior of the ion for different charges (Q) over the time.

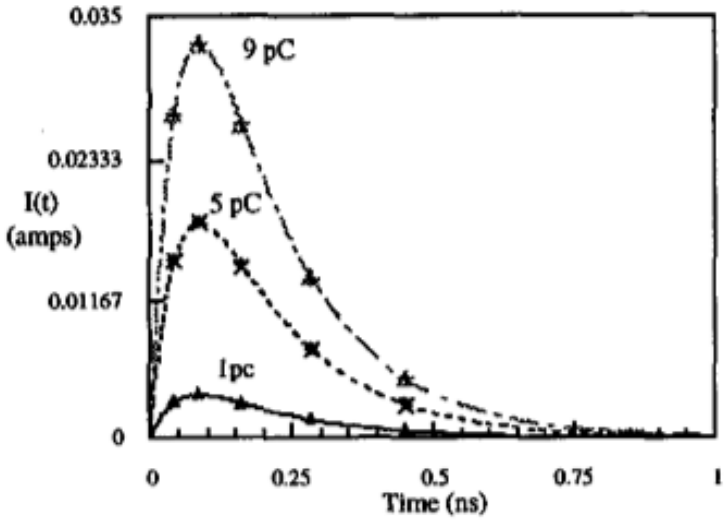


Figure 2.26: Current for different charges. (DHARCHOUDHURY, 1994)

To estimate the vulnerability of a given circuit at circuit level the error-cross section is calculated using equation 2.13. This information is used to estimate the vulnerability of circuits to different LETs. This is generally a form to evaluate the effectiveness of techniques to mitigate errors at different environments (KARNIK, 2004).

$$\sigma_{SEE} = [\#events] \div \left[\frac{\#\ particles}{cm^2} \right] \quad (2.13)$$

The error cross-section is the ratio of upsets with the number of incident particles by the area. It is calculated by (2.13) in which *#events* is the number of measured upsets in the circuit and *#particles* is the number of particles that had been irradiated. In figure 2.27 the error cross section of a circuit is shown, indicating that a LET of more than 10MeV/(mg/cm^2) is required to upset the circuit . It is noticed that with the increase of the LET the number of errors increase from many orders of magnitude. The error cross-section is a common method used to analyze the effect of hardening technique.

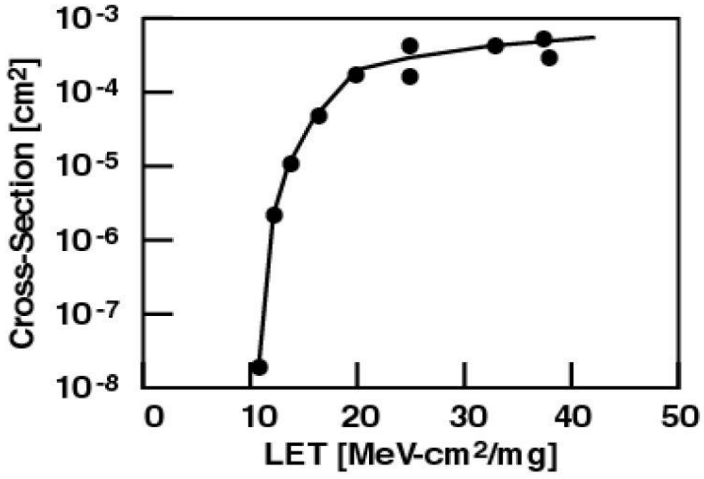


Figure 2.27: Cross Section of a circuit (SCHRIMPF, 2006).

Besides modeling the ion profile there is the necessity of modeling the transient pulse shape generated by the radiation. In (WIRTH, 2007a) the author developed a model to analyze the transient pulse duration (2.14) the time on which the transient pulse reaches its peak (2.15) and the transient pulse peak (2.16) over the node. These equations take into account the resistance and capacitance of the node and the current obtained from the equation (2.12).

$$T_D = t_{peak} - RC\ln\left(\frac{V_{DD}/2}{V_{peak}}\right) - \tau_\alpha \ln\left(\frac{V_{DD}/2}{V_{peak}}\right) \quad (2.14)$$

$$t_{peak} = \frac{\ln(\frac{\tau_\alpha}{RC})\tau_\alpha RC}{\tau_\alpha - RC} \quad (2.15)$$

$$V_{peak} = \frac{I_0 \tau_\alpha R}{\tau_\alpha + RC} \quad (2.16)$$

where R and C are the effective resistance and capacitance of the node. The τ_α is the collection time constant of the junction. With these information, in (WIRTH, 2007b) the author presents a model to analyze the propagation of transients. The model is used to analyze the behavior of the transient signals through the combinational logic. The model is able to determinate if the transient pulse will be electrically masked by the circuit. The model can be briefly understood by the following equations that models different situations for the pulse and the stage of the logic. The equation (2.17) defines the case in which the transient pulse is not propagated. Equation (2.18) the pulse is propagated and degraded in amplitude and duration. Equation (2.19) the transient is propagated and degraded in duration. Equation (2.20) pulse is propagated but not degraded.

$$if\ (\tau_n < k \cdot tp)$$
$$\tau_{n+1} = 0 \quad (2.17)$$

$$if\ (k \cdot tp < \tau_n < (k+1) \cdot tp)$$
$$\tau_{n+1} = (k+1) \cdot tp(1 - e^{2.5-(\tau_n/tp))}) \quad (2.18)$$

$$if\ ((k+1)\cdot tp < \tau_n < (k+3)\cdot tp)$$
$$\tau_{n+1} = (\tau_n^2 - tp^2)/\tau_n \qquad (2.19)$$

$$if\ (\tau_n > (k+3)\cdot tp),$$
$$\tau_{n+1} = \tau_n \qquad (2.20)$$

where *tp* is the propagation delay of the gate, τ_n the transient duration at stage *n* and τ_{n+1} the transient duration at stage *n+1*. *K* is a fitting parameter that is equal to the minimum ratio of τ_n / tp needed by a transient to be propagated into the next stage of a combinational logic. The *K* is obtained through a stage of characterization of the technology process that will be used. This model is important because it can provide valuable information about the behavior of the transient pulse inside the circuit. In figure 2.28 the electrical masking of the transient pulse that is propagated over the combinational logic is shown. The model proposed before has as target model this behavior.

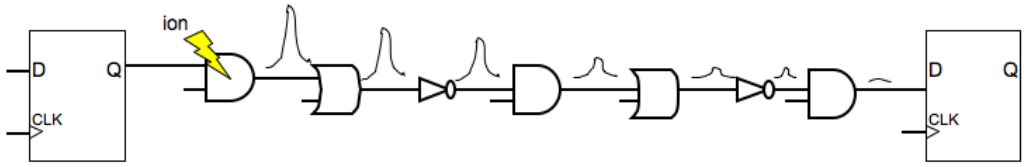


Figure 2.28: Transient propagation over logic (LAZZARI, 2007)

The information provided by equation (10-12) can be used to analyze the propagation of the ion showed in figure 2.28. With gate delays and information about resistance and capacitance of the nodes it is possible to verify if the transient will reach the sequential element. These equations where used by (LAZZARI, 2007) to analyze the propagation of a transient in a combinational logic to define the necessity to size the transistors to increase the critical charge.

3 DEVICE MODELING

As mentioned in the previous chapter, the simulation of transient radiation effects inside semiconductors devices can be done considering a single or multiple interaction event. Due to software technology limitations this work will be done using a traditional approach used to simulate soft errors considering a single interaction event. This work will be conducted using the TCAD tool Davinci from Synopsys. The tool Davinci allows the creation of semiconductors devices and the simulation of soft errors using a function of generation of electron-hole pairs. This has been the approach to simulate soft errors at researches group that don't have specific tools (generally created by the own group) to simulate soft errors. One example of a specific tool to evaluate transient radiation effects is the Soft-Error Monte Carlo Model 2 (SEMM-2) from IBM, to obtain more information about the tool consult (TANG, 2008).

In this work the semiconductor device used during radiation tests was a n-type MOSFET transistor with a 90nm channel length. It was not necessary to build a p-type transistor because the effect that was analyzed in this work has the same behavior for both devices. When simulations required a p-type transistor at the pull-up logic of the gate, a Predictive Technology Model - PTM from ASU electrical model was used. The tool Davinci allows the execution of both device and electrical transistor running in a mode called mix-mode simulation. It must be noticed that to evaluate the soft errors in transistors some works like (HAZUCHA, 2003) do not build the entire transistor, instead they build, just the diode of the device to represent the drain of the transistor. This approach simplifies the simulation but can't be used to evaluate different impact angle of the ion, since other parts of the device (transistor) can influence the behavior the collected charge. In figure 3.1 the electrical symbol of a n-type MOSFET transistor.

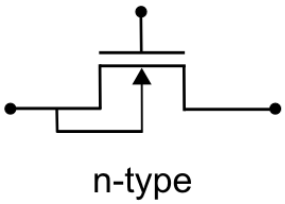


Figure 3.1: NMOS transistor symbol

The device modeled in this work was based on data extracted from the models of the Microsystems Technology Laboratory of MIT (DIMITRI, 2008) that has also used information of doping profile of (HU, 1995) suggesting the topology showed in figure 3.2. The model presents a NMOSFET using a Super Steep Retrograde (SSR) channel doping, source/drain halo and a Light Doped Drain (LDD) structure. The SSR technique described at (SRINIVASAN, 2005) and (TIAN, 1994) consists of a channel engineering technique used to prevent short channel effects on nanometer MOS devices. The technique proposes to increase the doping of the substrate (prevent short channel effects) and to create a thin layer with a lower doping near the surface of oxide and silicon to control the threshold of the device.

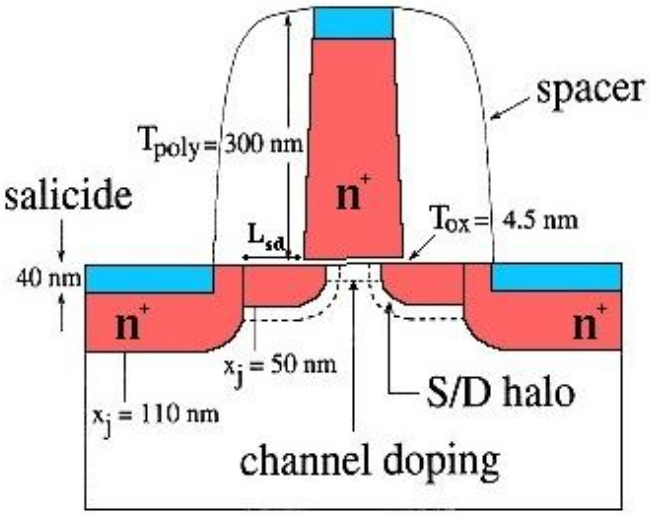


Figure 3.2: NMOSFET device (DIMITRI, 2008)

Another technique applied at the model showed in figure 3.2 is the use of halos. The halo implant is also a channel engineering technique used to control short channel effects. The halo is able to reduce the effect of the high doping profile of the device that is able to increase hot carriers effects, which consist of the high acceleration of the carrier due to the high electric field produce at the junction. This structure will not be used in this work, for more details about halo implants consult (SRINIVASAN, 2005). Other structure used is the LDD. The LDD structure consists of creasing a small active region that will be overlapped by the channel using a thickness smaller than the active region (Source\Drain) and with a smaller doping concentration (TSIVIDIS, 1999). The technique (LDD) is used to reduce the electrical field strength near the gate channel, making a reduction in hot carrier effect.

Another work presented by (DASGUPTA, 2007) also gives valuable information about a 90 nm NMOS model. Information about n-type and p-type transistors for high performance and low power are presented by the author. There are differences with the model presented before by the MIT. These differences are more aggressive to the substrate doping profile and oxide thickness. For MIT model it is presented a generic transistor with an oxide of 4.5 nm instead of (DASGUPTA, 2007) high performance transistor with an oxide of 1.4nm and low power model with 2.8nm. The substrate doping for both devices is uniform presenting for MIT model about 7e19atm/cm^{-3} and for (DASGUPTA, 2007) about 1e16atm/cm^{-3}. Both models present similar geometry profiles for the other regions of the device. In next section the modeled device used in this work is presented.

3.1 Modeled Device – 3D NMOSFET

The device the design of the 3D MESH used to model the transistor in Davinci will be briefly described. The 3D MESH is a structure where the device regions are created with the MESH points indicating where physic calculations are done to evaluate the simulations. If the MESH is defined with too much simulation points it will lead to many hours of simulation even if the device is small, but if the number of simulation points is small the results will loose accuracy. This balance between simulation time and accuracy should be adjusted interactively.

An strategy to define the MESH is presented at (DASGUPTA, 2007) where the author suggests the creation of a MESH divided in regions with higher and lower concentration of simulation points and with the refinement of the points in areas where a simulation is more important. Dasgupta (2007) also suggests the creation of the 3D MESH from the top to the bottom. These indications were followed as it will be described.

The Y axis was defined with two regions, the first from *0.0* to *0.5um* with the spacing from mesh points of about 50 nm. The second region was defined from *0.5* to *1.5 um* with an increase in the spacing between mesh points to 2*um*. Over active regions MESH is refined to receive more simulation points allowing a more accurate simulation. The refinement of the active region was used to reduce the spacing for 10nm. This kind of refinement can be done at any time during simulations. In figure 3.3 the cross-sectional view of the NMOSFET 3D MESH that was designed.

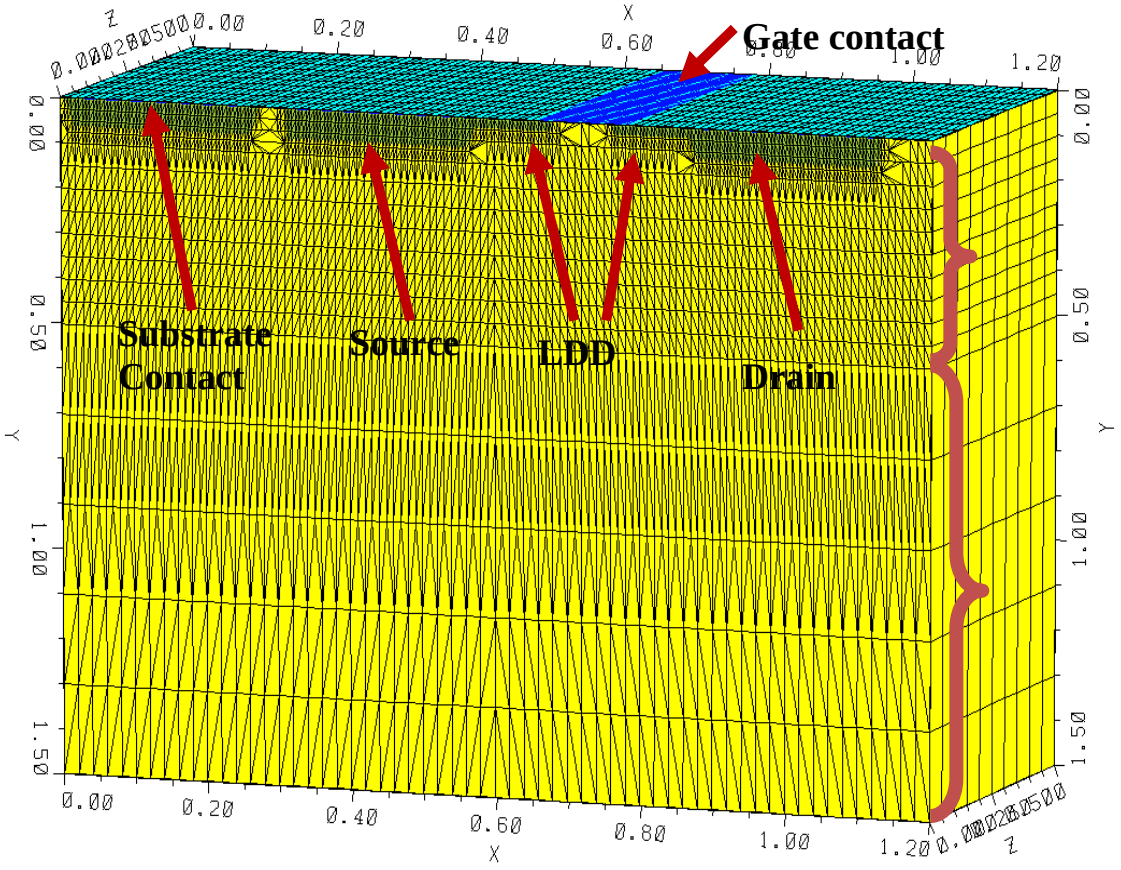


Figure 3.3: Developed NMOS 90nm device

Detailed information about doping and geometry profiles of the device is shown in table 3.1. Notice that these dimensions are based on (DASGUPTA, 2007) and (DIMITRI, 2008).

Table 3.1: Dimensions and doping profiles

Region	Width (x)	Width(y)	Width (z)	Doping
LDD	*115 nm*	*30 nm*	*240 nm*	*n-type. Peak: 1e19*
Source\Drain	*240 nm*	*60 nm*	*240 nm*	*n-type. Peak:1e20*

SSR	*90 nm*	*5 nm*	*240 nm*	*n-type. Peak:1.5e18*
Gate	*136 nm*	*300 nm*	*240 nm*	*n-type. Peak:2e20*
Oxide	*136 nm*	*1.4 nm*	*240 nm*	*None*
Substrate	*0.9*	*1.5*	*0.3 um*	*p-type. Peak:5.5e18*

The doping of both active regions and SSR has Gaussian distribution. The doping of the substrate is uniform. To control the threshold of the device the SSR was used. The oxide was not adjusted to control the threshold voltage and this value is the same that (DASGUPTA, 2007) had used to 90 nm high performance devices.

3.2 NMOSFET Device Simulations

To validate the NMOS transistor modeled in Davinci, device mode simulations were conducted to analyze the behavior of the device when a bias is applied over the terminals (substrate\source\gate\drain). These simulations were done to compare the device behavior with a 90nm Predictive Technology Model (PTM) from (ZHAO, 2007) Arizona State University (ASU, 2008). The threshold voltage of the device was also compared with ST 90nm transistor model. For the simulations results presented in figure 3.4 and 3.5 the numerical method of Newton was used as recommended by Davinci Manual. For all simulations a standard temperature of T=300K was used.

In figure 3.4 and 3.5 the substrate and source are grounded (V_S=V_B=0V). Notice that simulations of the device are done in Davinci and the spice models (PTM) are simulated in HSpice. In figure 3.4 the V_{GS} vs. I_{DS} behavior is evaluated for both devices. It is possible to verify that the PTM model and the device have similar results. The threshold of the device modeled was extracted using the "MOS PARAMETER EXTRACTION" command of Davinci and was found to be V_T=0.31V. The threshold voltage of the PTM level 54 device, is about V_T=0.29V. The documentation of the design rule kit from ST 90nm (ST, 2002) indicates a V_T=0.32V. These data confirms that the modeled device fits with the results of PTM.

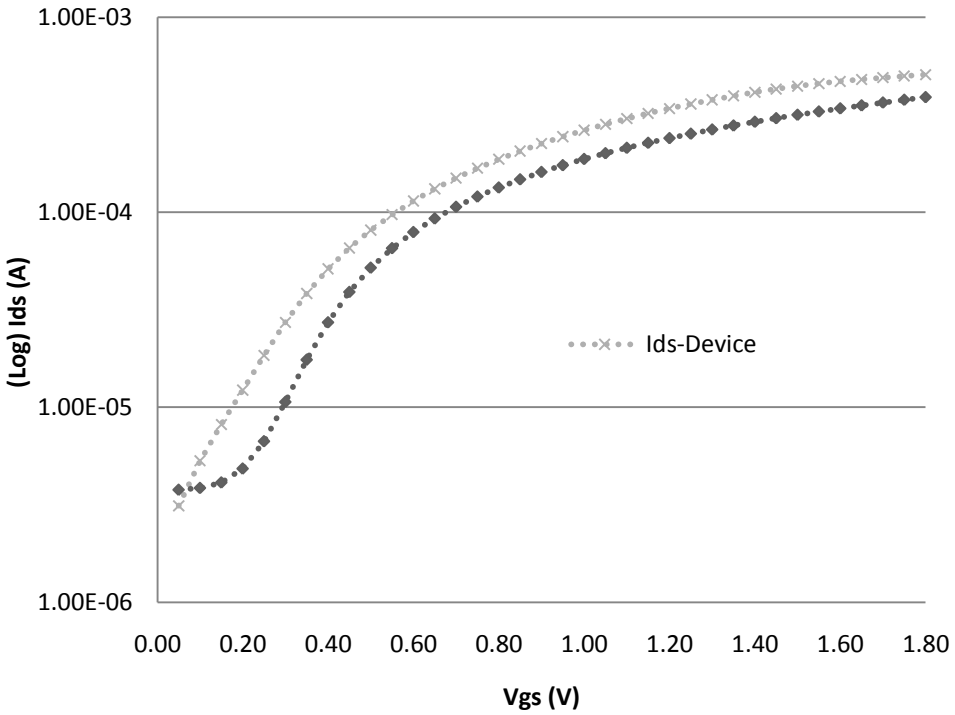


Figure 3.4: I_{DS} vs V_{GS} for PTM and the device modeled

In figure 3.5 the I_{DS} *vs* V_{DS} behavior of both devices are evaluated. The V_{GS} is fixed on 1.2 V and the drain bias is varied. The result also shows similar results for both devices, indicating a fit for the device with the PTM.

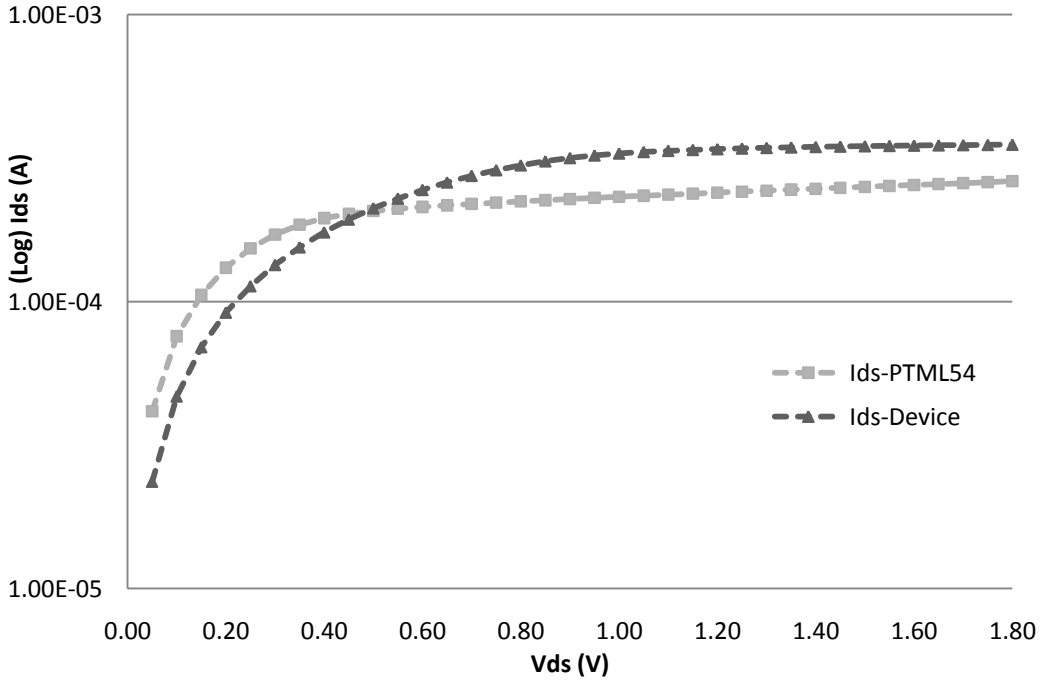


Figure 3.5: I_{DS} *vs* V_{DS} for PTM and the device modeled

With the previous simulations the functional behavior of the device was verified also showing the similarity of the device with the PTM model. Other evaluation was done to evaluate the tunneling effect mechanism in the gate of the device, due the small oxide thickness (T_{OX}.=1.4 nm) used in the transistor.

Simulations for tunneling analysis were solved using the Numerical Integration of the Gundlach Tunneling Coefficient. The Direct Tunneling Analysis (Using *FE(Gate)* function), which was done in this work combines with both direct tunneling regime and the Fowler-Nordheim regime. Simulations were conducted at a temperature of 300 Kelvin.

In figure 3.6 which is in logarithmic scale, it is shown the current flowing through the channel to the gate and gate to channel, due to the tunneling effect. At the left part of the figure from V_{DS}=0.2 V to V_{DS}=1.0 V is possible to notice that the current starts to drawn until a certain point near the V_G = V_{DS}. Until this point the current is negative and is flowing from channel to the gate. After this point the current becomes positive what means that the current is flowing through the gate to the channel. The inversion of the current signal in the figure 3.6 is explained by the increase of the gate current. When Vds bias is greater than Vgs the current is passed from the substrate (channel) to the gate, this behavior is changed when the bias of Vgs reaches Vds and the current starts to take the inverse path, which can be seen as a variation of the electric field strength signal at oxide region.

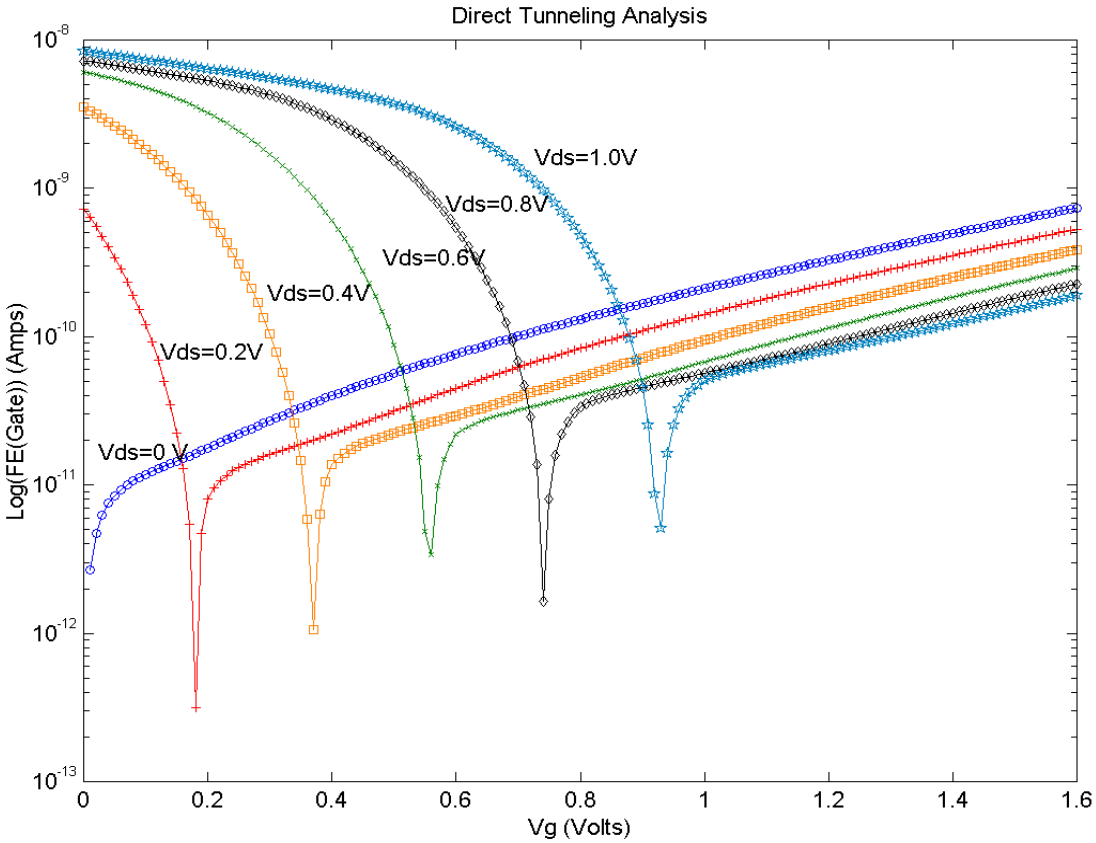


Figure 3.6: Direct Tunneling Analysis

For an extended study of the components of the gate tunnel current consult (TSIVIDIS, 1999). Once the behavior of the modeled device was validated, in next chapter the methodology used to simulate soft errors in this work is presented.

4 SOFT ERRORS MODELLING

With the device model presented and validated in previous chapter, this chapter is dedicated to issues about soft errors simulation in device level. As mentioned in Chapter 3 transient simulations in this work will be modeled considering a single interaction event. Simulating single interaction events for radiation particles in TCAD tools consists of determining specific property of the ion to be used. The properties of the ion that must be used in simulations are: Linear Energy Transfer, radial distribution of electron-hole pairs, impact angle, ion range and trajectory.

Issues about the ion impact angle and trajectory are generic parameters that are not related to specific properties of the ion. These parameters don't require specific tools to their evaluation. The impact angle of the ion with in respect to the surface of the device is shown in figure 4.1. The main effect of the variation of the ion impact angle is the increase or decrease of the path of the ion inside the device and the change in the direction of the funneling of the electric field during the irradiation.

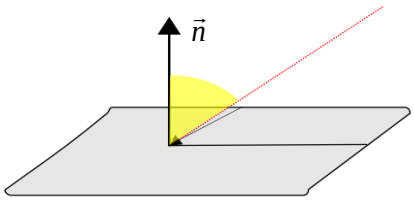


Figure 4.1: Surface Impact Angle Dependence

Another aspect is the trajectory of the particle inside the device. This parameter is closely related with the angle since it can be increased or reduced depending of the impact angle. In figure 4.2 the worst case trajectory using a Rectangular Parallelepiped (RPP) model is shown.

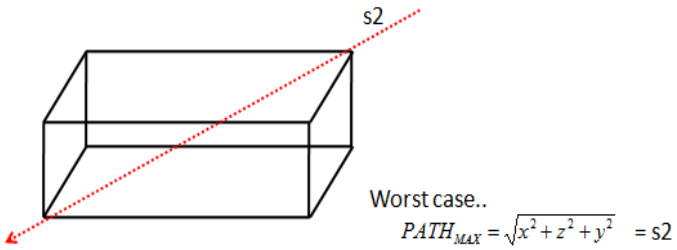


Figure 4.2: Worst case impact. (HASS, 99)

The other parameters like Linear Energy Transfer which was already described in chapter 2 as the rate of energy transfer to the device, and radial distribution of electron-holes pairs generated during the ionization requires specific tools to their evaluation.

The radial distribution of electron-hole pairs is defined as the radial distance of the spatial distribution of carriers generated during ionization inside the device. In figure 4.3 the radial distribution inside the device is shown. The radial distribution has a direct impact in carriers concentration inside the device having an important influence in carriers recombination rate.

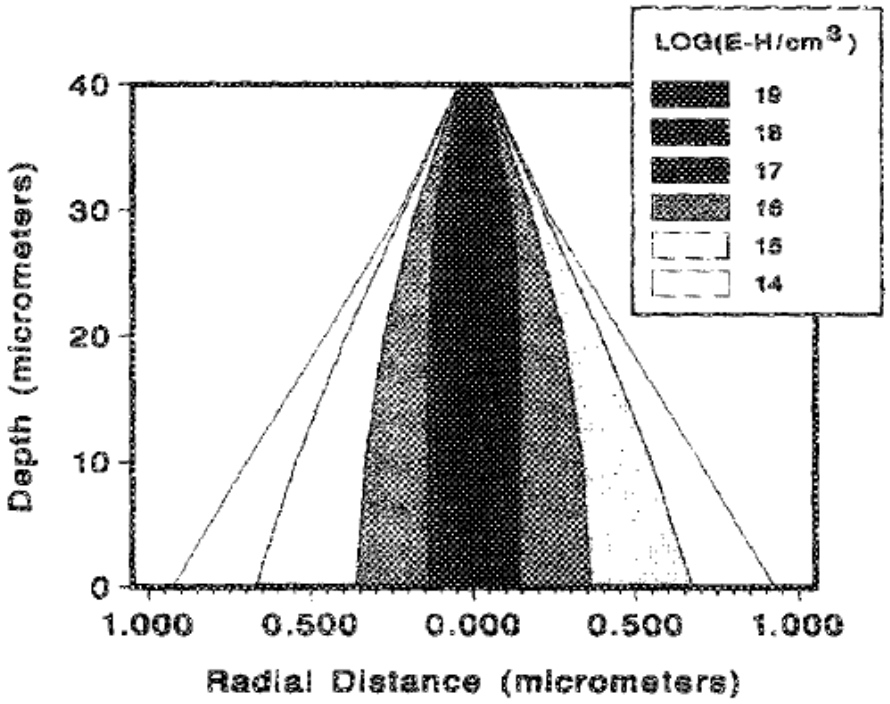


Figure 4.3: Radial distribution of an Ar ion of 180 MeV in Si (STAPOR, 1988).

With the main parameters explained at next section the characterization of ions used in this work are approached. Notice that the last two parameters mentioned before will be approached at the following section.

4.1 Ion Profiles

The tool The Stopping and Range of Ions in Matter (ZIEGLER 2008) is used to analyze ion behavior inside the device. The tool which was designed by (ZIEGLER, 2008) allows the irradiation using different ions hitting different materials. An example of an irradiation of an Hydrogen (H) ion with 1 MeV hitting a silicon (Si) layer with 2.32g/cm^3 density and 2um thickness is shown in the following. In figure 4.4 the trajectory of the H ion inside the device is presented. Notice that these radiation simulations are conducted with a large number of ions to allow a proper evaluation of the behavior of the particles inside the target material. All simulations presented at this section were done considering a 90º impact angle and for each ion five thousand ions were used to build each profile. Notice that for H trajectory near surface most ions follows the same trajectory with a larger scattering at more depth regions of the device.

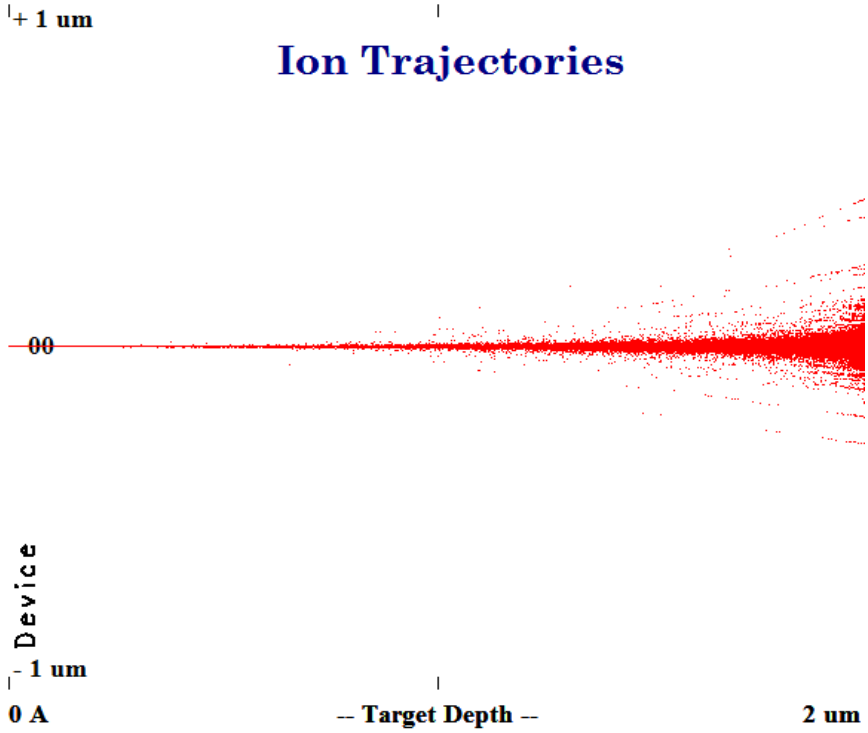


Figure 4.4: Hydrogen hitting silicon layer

The spatial distribution of the ion inside the device can also be evaluated as seen in figure 4.5. These results show the scattering of the particles during the simulations. By correlating these results with the trajectory it is possible to verify at which depth this phenomenon is more intense.

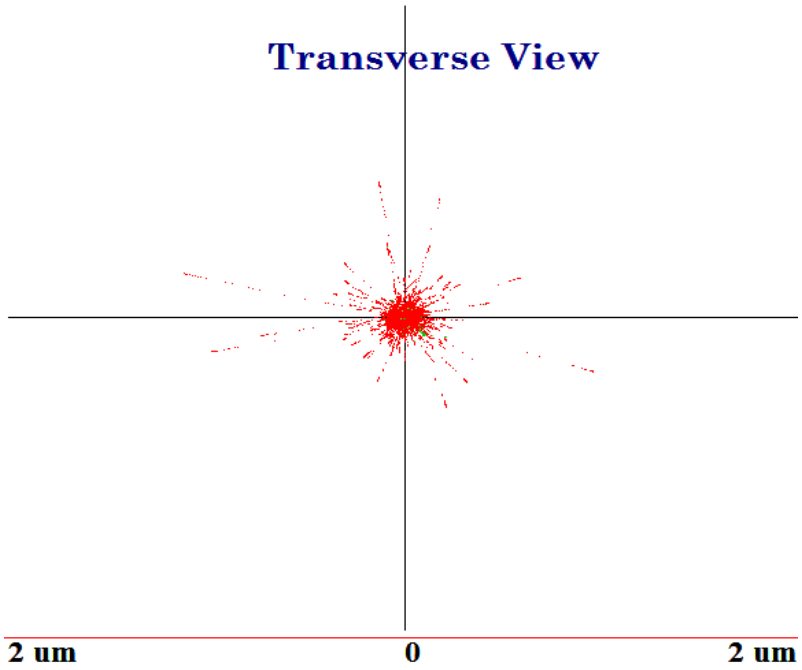


Figure 4.5: Spatial distribution of H in silicon

The result of the energy loss of a particle which can be also referred as the ionization is shown in figure 4.6. It can be noticed in figure 4.6 that the rate of energy loss along this device thickness is very similar along the device thickness.

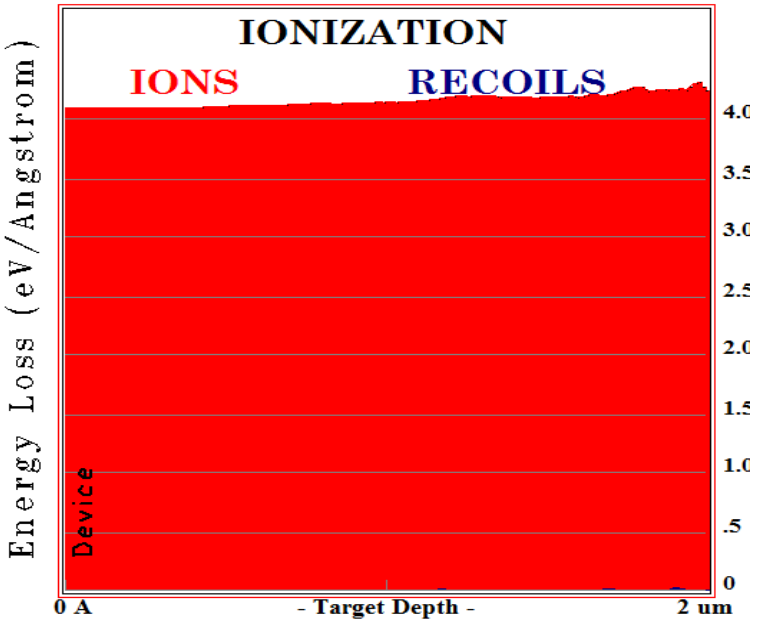


Figure 4.6: LET profile of H ion.

An interesting functionality of SRIM allows obtain LET tables for a specific ion particle a range of LET for different energies. In table 4.1 the LET table for the H ion with different energies.

Table 4.1: LET table for H ion.

Ion Energy	dE/dX Elec.	dE/dx Nuclear	Projected Range	Longitudinal Straggling	Lateral Straggling
450.00 keV	2.696E-01	2.596E-04	5.18 um	2727 A	3908 A
500.00 keV	2.554E-01	2.379E-04	5.99 um	3098 A	4373 A
550.00 keV	2.430E-01	2.197E-04	6.85 um	3468 A	4857 A
600.00 keV	2.321E-01	2.043E-04	7.75 um	3838 A	5360 A
650.00 keV	2.224E-01	1.911E-04	8.69 um	4209 A	5881 A
700.00 keV	2.137E-01	1.795E-04	9.67 um	4582 A	6418 A
800.00 keV	1.986E-01	1.604E-04	11.74 um	5719 A	7542 A
900.00 keV	1.861E-01	1.452E-04	13.97 um	6806 A	8728 A
1.00 MeV	1.755E-01	1.328E-04	16.33 um	7871 A	9972 A
1.10 MeV	1.663E-01	1.225E-04	18.84 um	8926 A	1.13 um
1.20 MeV	1.571E-01	1.137E-04	21.48 um	9986 A	1.26 um
1.30 MeV	1.492E-01	1.062E-04	24.28 um	1.11 um	1.40 um
1.40 MeV	1.423E-01	9.965E-05	27.22 um	1.21 um	1.55 um
1.50 MeV	1.361E-01	9.392E-05	30.29 um	1.32 um	1.71 um
1.60 MeV	1.305E-01	8.886E-05	33.50 um	1.44 um	1.87 um
1.70 MeV	1.253E-01	8.434E-05	36.85 um	1.55 um	2.03 um
1.80 MeV	1.207E-01	8.029E-05	40.33 um	1.66 um	2.20 um
2.00 MeV	1.124E-01	7.331E-05	47.69 um	2.04 um	2.56 um
2.25 MeV	1.037E-01	6.620E-05	57.61 um	2.56 um	3.03 um
2.50 MeV	9.644E-02	6.042E-05	68.32 um	3.07 um	3.54 um
2.75 MeV	9.023E-02	5.562E-05	79.80 um	3.56 um	4.08 um
3.00 MeV	8.486E-02	5.156E-05	92.05 um	4.06 um	4.66 um

Other aspects can be evaluated by the tool, but since they are not the main concern in the simulations done in this work they will not be addressed. The radial distribution of carriers is not directly calculated by SRIM 2008. To obtain the correct value of this parameter for the ions used in this work, others works were consulted and these will be indicated for each particle in the following paragraphs.

At this work ions of Helium (He), Copper (Cu), Krypton (Kr) are used. The ions were selected based on information related to the environment. One important point in the selection of the ion is the existence of computational tools to obtain specific energy profiles. The tool used in this work to obtain ion profiles is not able to simulate sub-particles profiles like neutrons, electrons or protons irradiation.

The alpha particles simulations were done using a Helium ion. The alpha particle is a helium ion positively double ionized, which means that is a helium nucleus without electrons. This approach has been used by radiation effects community to obtain alpha particles profile using SRIM. For alpha particles simulations were conducted using a Helium (He) ion of 1MeV with a LET of 1.31MeV/(mg/cm^2). The table 4.2 shows the LET table of He ions with energy going from 450KeV to 3MeV.

Table 4.2: LET table of He ion

Ion Energy	dE/dx Elec.	dE/dx Nuclear	Projected Range	Longitudinal Straggling	Lateral Straggling
450.00 keV	1.448E+00	3.523E-03	1.83 um	1859 A	2332 A
500.00 keV	1.452E+00	3.238E-03	1.98 um	1891 A	2389 A
550.00 keV	1.449E+00	2.999E-03	2.13 um	1921 A	2443 A
600.00 keV	1.441E+00	2.795E-03	2.27 um	1951 A	2495 A
650.00 keV	1.430E+00	2.619E-03	2.42 um	1979 A	2545 A
700.00 keV	1.416E+00	2.466E-03	2.57 um	2007 A	2594 A
800.00 keV	1.384E+00	2.211E-03	2.88 um	2084 A	2689 A
900.00 keV	1.349E+00	2.007E-03	3.19 um	2160 A	2782 A
1.00 MeV	1.312E+00	1.839E-03	3.51 um	2237 A	2874 A
1.10 MeV	1.276E+00	1.700E-03	3.84 um	2314 A	2967 A
1.20 MeV	1.240E+00	1.581E-03	4.18 um	2392 A	3060 A
1.30 MeV	1.206E+00	1.479E-03	4.53 um	2471 A	3153 A
1.40 MeV	1.172E+00	1.390E-03	4.89 um	2551 A	3249 A
1.50 MeV	1.141E+00	1.312E-03	5.26 um	2633 A	3345 A
1.60 MeV	1.111E+00	1.243E-03	5.65 um	2716 A	3444 A
1.70 MeV	1.082E+00	1.181E-03	6.04 um	2801 A	3544 A
1.80 MeV	1.055E+00	1.126E-03	6.44 um	2888 A	3647 A
2.00 MeV	1.005E+00	1.030E-03	7.27 um	3176 A	3858 A
2.25 MeV	9.495E-01	9.320E-04	8.37 um	3605 A	4135 A
2.50 MeV	9.002E-01	8.522E-04	9.53 um	4031 A	4426 A
2.75 MeV	8.564E-01	7.857E-04	10.75 um	4456 A	4732 A
3.00 MeV	8.172E-01	7.294E-04	12.04 um	4883 A	5053 A

The trajectory of the He 1MeV ion was evaluated as shown in figure 4.7 the ion trajectory near surface is similar to all injected particles, the scattering becomes larger

near 1um depth. This result indicates that a linear approach of the device track near the surface is consistent to a 90º impact at the device.

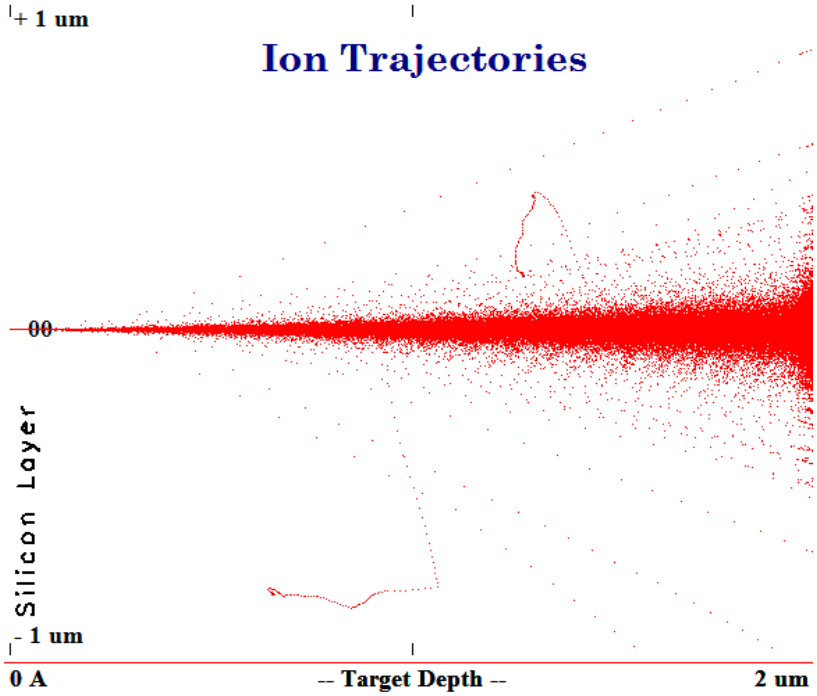


Figure 4.7: He Range of the particle inside the device

The transverse view in figure 4.8 allows to observe the scattering of the particles through another angle.

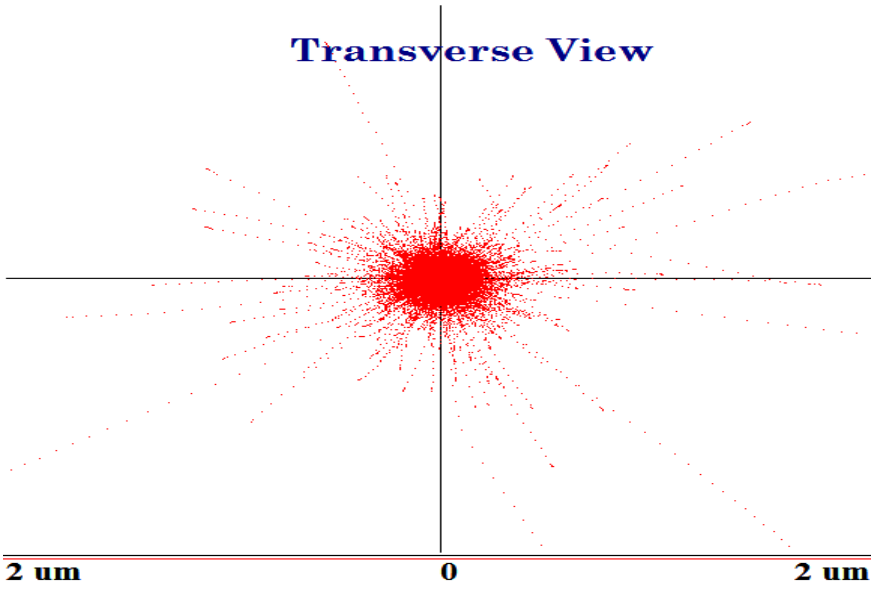


Figure 4.8: He Spatial profile inside the device.

The LET of 1MeV He is obtained as shown in figure 4.9. The LET was found to be around 30.46eV/A which is about 1.31MeV/(mg/cm^2) in Si. This is a very typical LET at sea level environment due this reason it was used in this work.

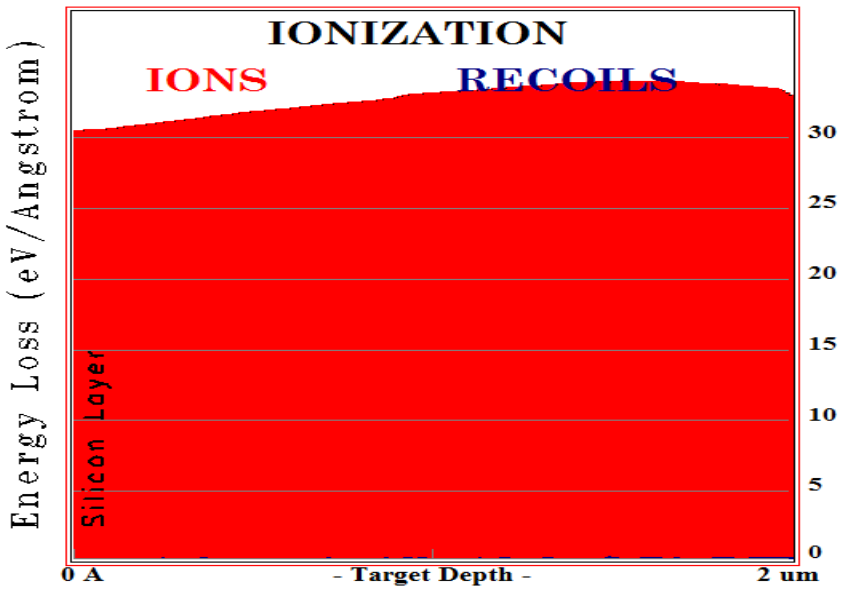


Figure 4.9: He Ionization profile inside the device.

The radial distribution of alpha particles was found to be about 50nm as indicated by (OLDIGES, 2000).

The ion of Cu with 395MeV was used to simulate LET profiles in high altitudes environments. In figure 4.10 the trajectory of the ion is seen. As desirable to simulate linear trajectories near the surface the ions follow the same path.

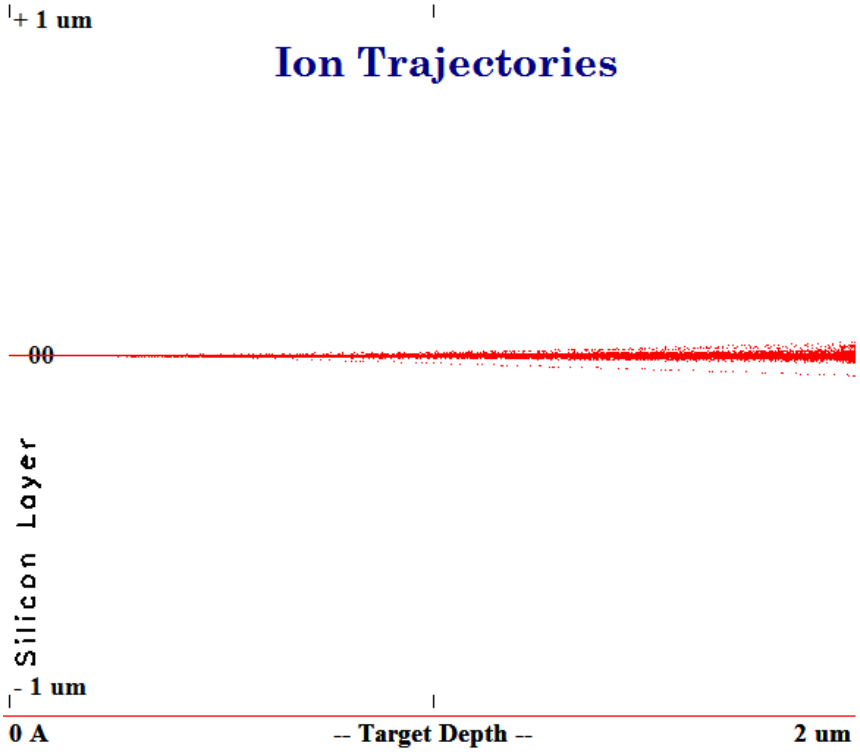


Figure 4.10: Copper trajectory

The scattering of the particles was also verified as seen in figure 4.11. The green cascade indicates the interaction of the particle with the device material generally resulting in the change of the ion direction and possible more interactions.

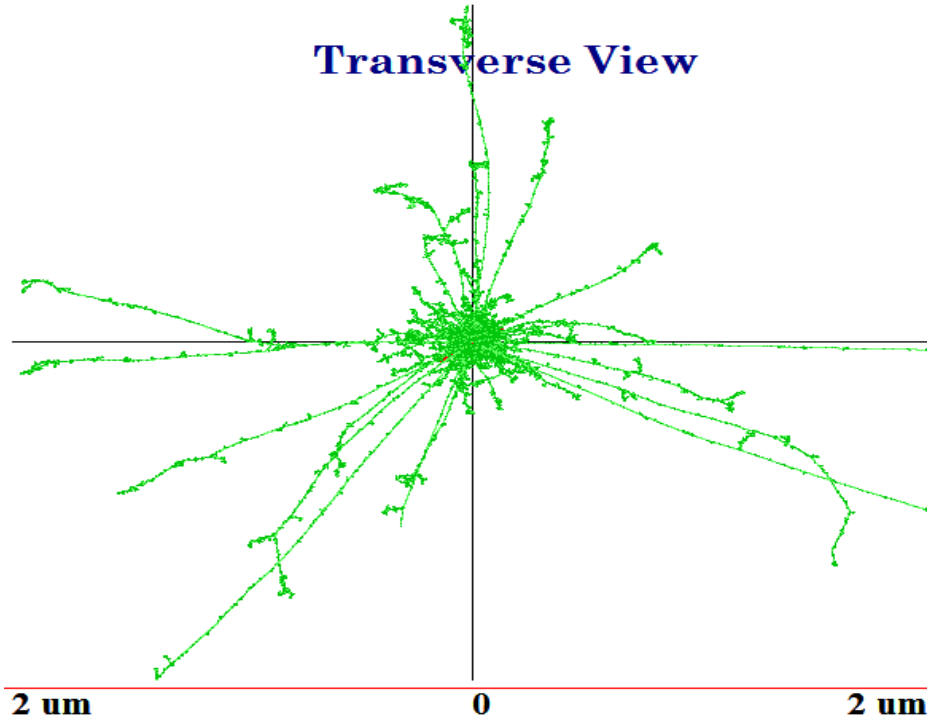


Figure 4.11: Copper spatial distribution..

The LET of Cu is obtained as shown in figure 4.12. The LET was found to be around 616eV/A which is about 26.5MeV/(mg/cm^2) in Si.

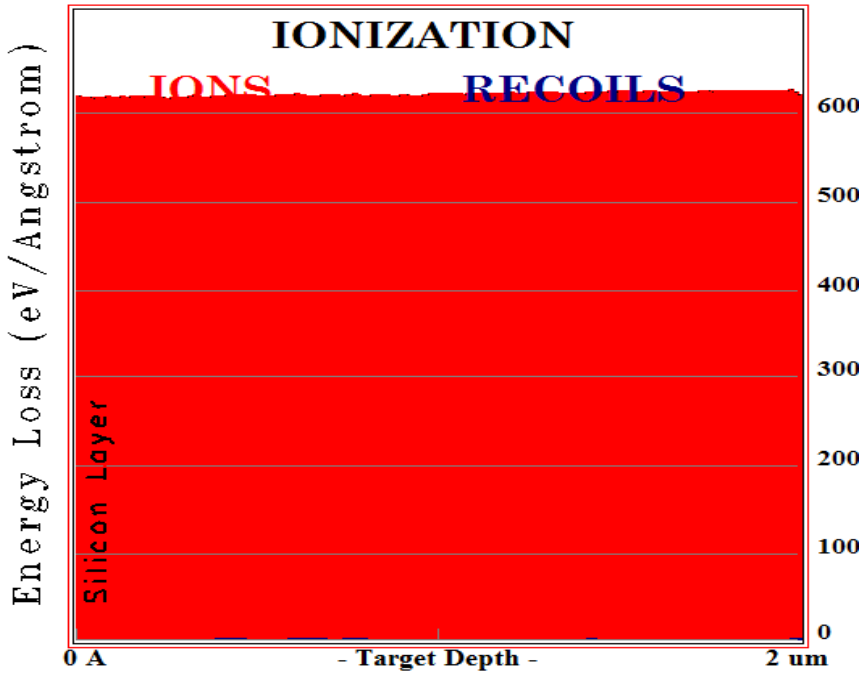


Figure 4.12: Copper ionization..

The radial distribution of Cu with 26.5MeV was found to be about 0.50*um* (STAPOR 1988).

To evaluate more aggressive environments the ion of Kr with 270MeV was used to simulate typical space environment LETs. In figure 4.13 the trajectory of the ion is seen. As desirable to simulate linear trajectories near the surface the ions follow almost the same path in the region near the surface.

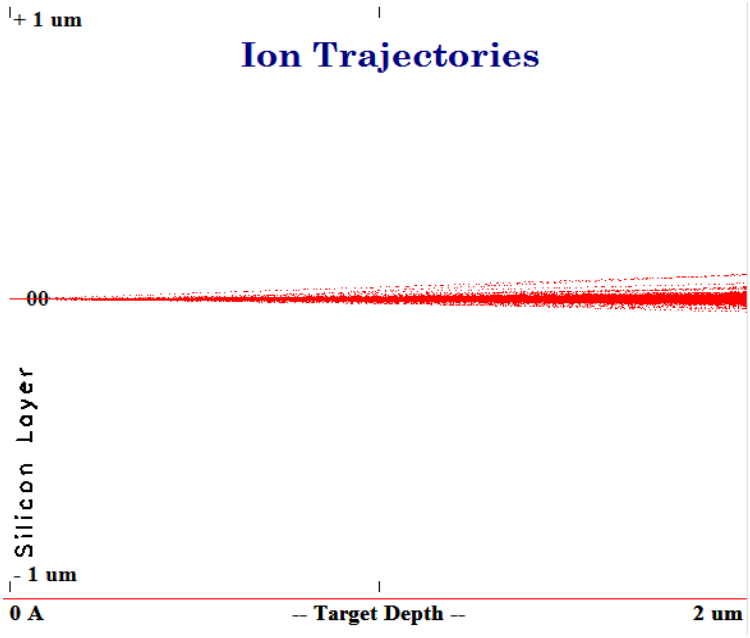


Figure 4.13: Krypton trajectory

The Kr ion also showed a large number of second interactions as seen in figure 4.14. The large energy of the ion allows to disturb large areas of the device. Also notice that most of the vacancies generated during the ionization of Cu and Kr are generated by recoil that are elastic collisions generated by the ion.

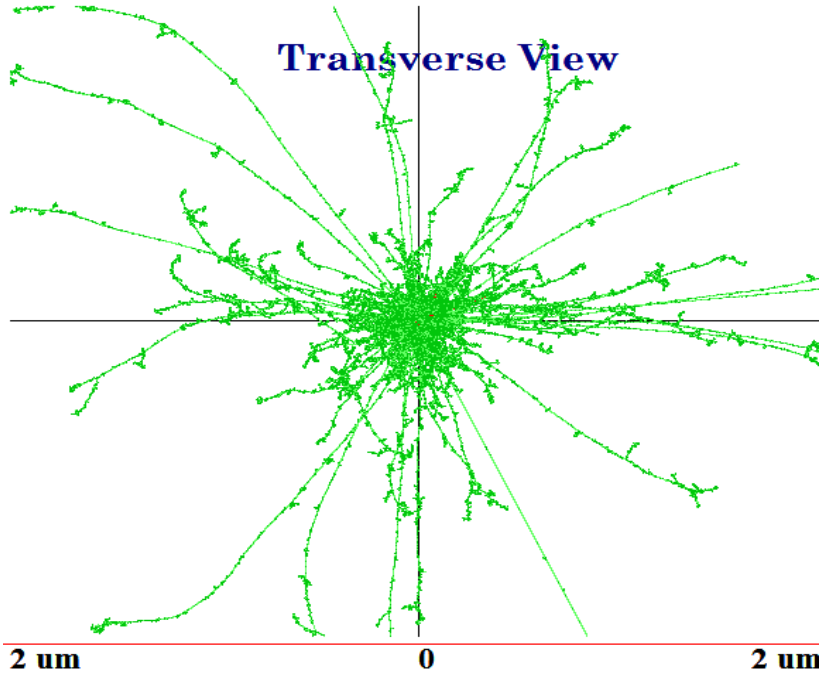


Figure 4.14: Krypton spatial range

The LET of Kr is obtained as shown in figure 4.15. The LET was found to be around 940eV/A which is about 40.5MeV/(mg/cm^2) in Si.

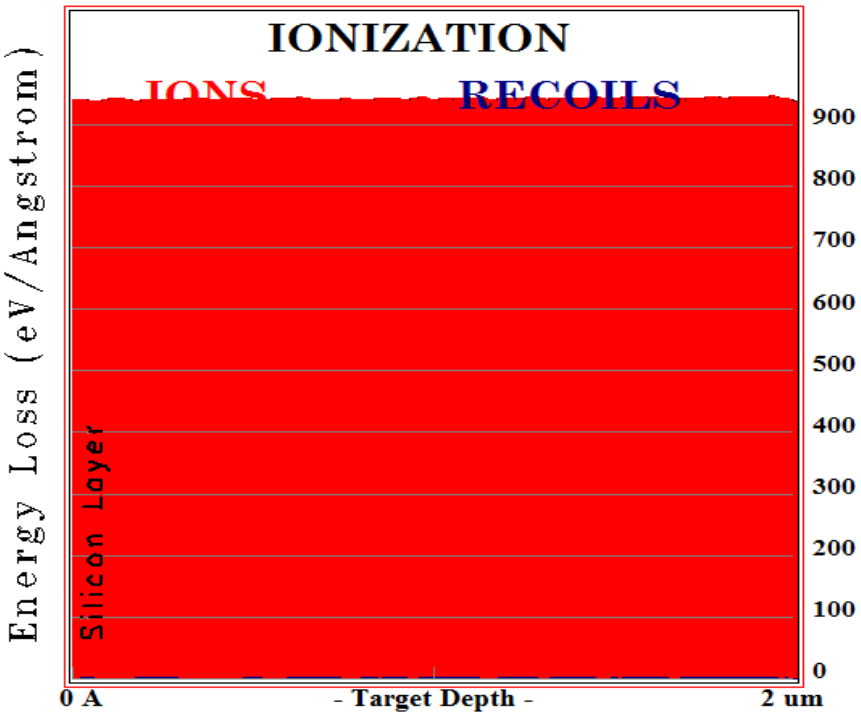


Figure 4.15: Krypton ionization profile

The radial distribution of Kr 270MeV at Si was found to be about 0.65um as indicated by the work of (STAPOR, 1988). In figure 4.16 the radial distribution of Kr 270MeV.

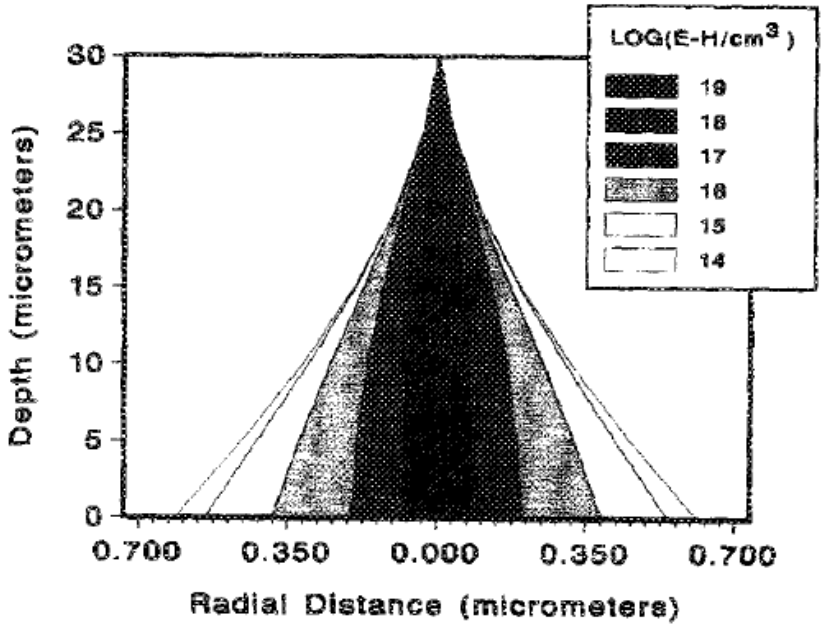


Figure 4.16: Kr radial distribution of e-h pairs (STAPOR, 88)

The table 4.3 summarizes the main parameters of the alpha particle, Cu and Kr ion that were presented in this section.

Table 4.3: Ion Profiles

Element / Energy	LET(dE/dX) MeV/(mg/cm²)	Radial (r) μm
Alpha – 1 MeV	1.31	0.05
Cu, 395 MeV	26.5	0.50
Kr, 270 MeV	40.5	0.65

At next section the physical models used for radiation effects simulations are approached.

4.2 Physical Models Used in Davinci Simulations

The following physical models are used at Davinci simulations to allow the proper evaluation of ion effects inside the device.

- Shockley-Read-Hall Model - SRH
- Auger Recombination Model - AUGER
- Carrier-Carrier Scattering Mobility Model - CCSMOB
- Bang-Gap Narrowing Model - BGN

The first two models presented before are recombination models. Recombination is a process in which an e-h pair is eliminated. The process occurs when an electron falls from the conduction band (E_c) to the valence band (E_v) with an empty state making both electron and hole disappear. The radial distribution has a strong impact in carrier's density and those at recombination rate since it allows more or less numbers of electron-hole pairs at the same device region. At the following the SRH and AUGER models will be briefly discussed.

The Shockley-Read-Hall (4.1) was presented by (SCHOCKLEY, 1952) and models the recombination of carriers that falls to trap energy level between the E_c and $E_{v.}$ This energy band also mentioned as trap region is generated due defects, irregularities or impurities in the semiconductor. The equation of the SRH is given by (4.1) and (4.2)

$$U = \frac{C_n C_p (pn - n_i^2)}{[C_n(n + n_1) + C_{p(}p + p_1)} \quad (4.1)$$

and,

$$n_i^2 = N_c N_p \exp\left({}^{-E_g}/_{kt}\right) \quad (4.2)$$

Where U is the recombination rate, p is the density of holes at valence band, n is the density of electrons in conduction band, C_n and C_p are the probability per unit time that an electron\hole in the conduction\valence band will be captured by a trap. The term n_i^2 (2) is the electron or hole concentration in an intrinsic sample, and n_1 and p_1 are the number of electrons\holes in the conduction\valence band for the case in which the Fermi levels falls at the trap band.

The AUGER (4.3) model is a band-to-band recombination (LANDSBERG, 1964) with the release of energy to another pair of e-h. The model equation is given by (4.3)

$$U_{Auger} = \Gamma_n n(np - n_i^2) + \Gamma_p p(np - n_i^2) \quad (4.3)$$

Where U_{Auger} is the recombination rate using Auger model and $\Gamma_n = C_n$ and $\Gamma_p = C_p$ .Notice that the released energy of the recombination is given to another e-h pair in form of kinetic energy. Beside these two recombination models, a carrier scattering model is also used. .

The Carrier-Carrier Scattering Mobility Model (LUNDSTROM, 2000) deals with carriers transport phenomenon due the interaction of carriers with electrical potentials, carrier to carrier interaction and temperature effect at the mobility of these carriers. The book of LUNDSTROM gives a detailed fundamental of carriers transport phenomenon.

The Band-Gap Narrowing Model (BGN) used in simulations is the Slotboom model [SLOTBOOM, 1977] that models the behavior of the band gap of the silicon through high impurity concentrations. For detailed information of the model consult the article referenced in this paragraph. At next section the measurements used to evaluate the effect of the ions in the device are approached.

To analyze the effect of the radial distribution of carriers to the ions used in this work it was conducted simulations changing this parameter. The results shown that small radial distributions limits the collected charge due the increase of the recombination rate that is increased due the large concentration of carriers that are generated using small radial distributions. These results are shown in appendix B. The results allow to understand that LET is not the only metric that matters when evaluating soft errors because high LET with low radial distributions will not generate more critical ionizations than high LET and high radial distributions.

4.3 Pulse Measurements

Measurements to evaluate the effects of the ions presented before are done to characterize current and voltage behavior in the drain of the transistor. The parameters used to evaluate these effects are: SET pulse width, SET pulse peak, current peak and collected charge.

The current behavior shown in figure 4.17 indicates two important values that are used to evaluate soft errors. The current peak showed in the figure represents the maximum current value achieved by the pulse generated by the ion. The other value extracted in this graph is called here as "*Tf*" and indicates the end of the pulse. This last measurement is used to calculate the collected charge.

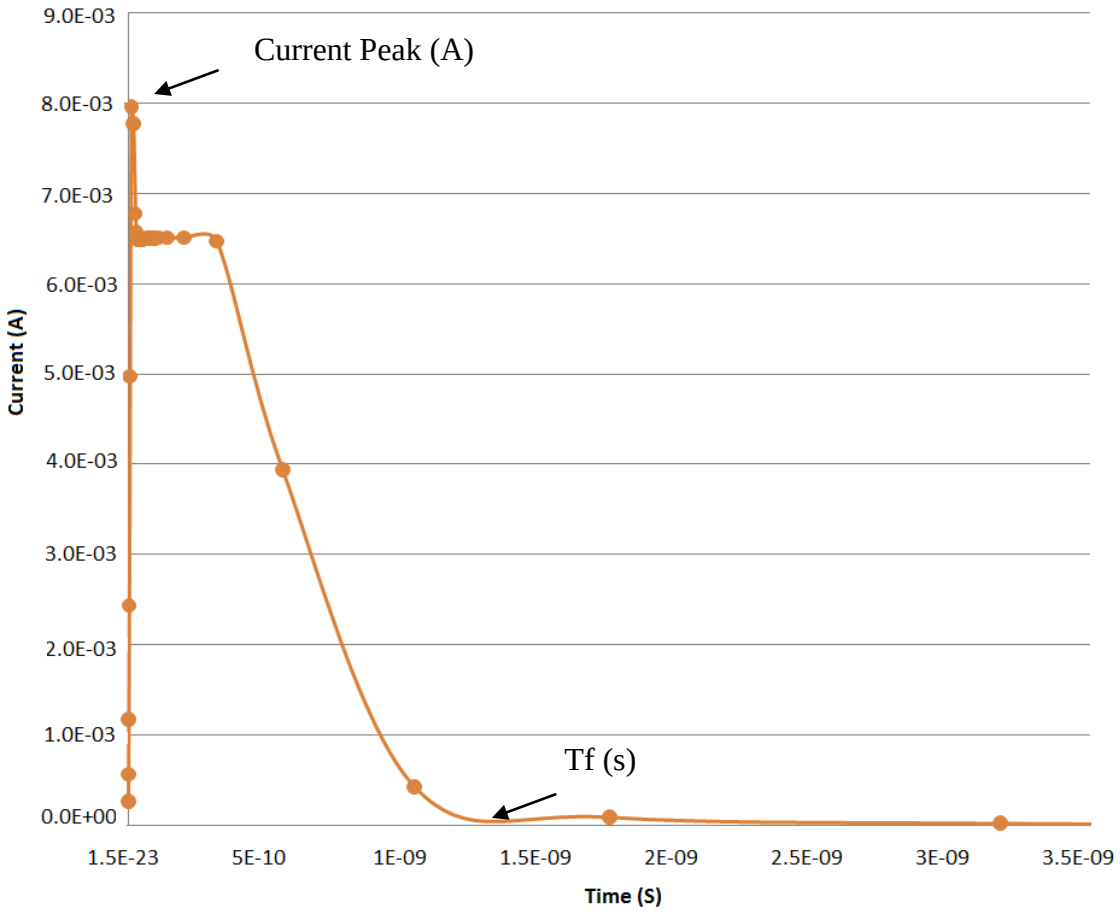


Figure 4.17: Measurements of the current generated by the ion

The second parameter, characterize the SET pulse behavior. The SET pulse is measured in respect to the voltage of the device as indicated in figure 4.18. The SET pulse width can also be called as the "pulse duration" and is measured as the time interval between the time in which the pulse signal falls above VDD/2 and when the signals rise over VDD/2 as shown in the figure 4.18. The other parameter, the SET pulse peak is the maximum amplitude variation during the irradiation and is also indicated in the figure. Note that for a PMOS transistor the drain output state is going from about 0V to VDD and for NMOS transistor the drain state goes from about VDD to 0V during ionization. Also considering that both devices are in off-state during the ionization. As all this work was done in a NMOS transistor using a VDD=1.2V all the measurements are done with the falling of this value. So if a SET pulse peak measurement is equal "0.1V" it means that the ionization has changed the bias condition from about "1.2V" to "0.1V".

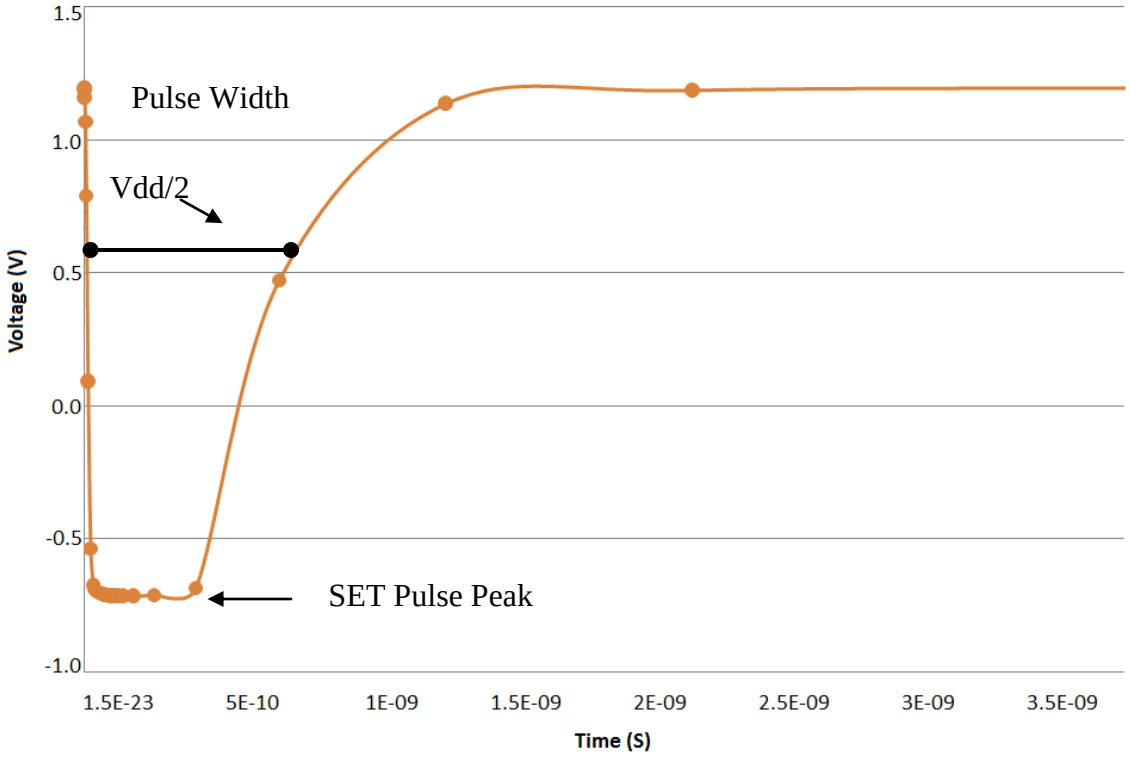


Figure 4.18: SET pulse width and peak

Other important parameter is the collected charge which is defined as the total charge collected by the device during irradiation. It is calculated by the integration of the current shown in figure 4.19 from the start time of the ionization to the end of the current "glitch" generated.

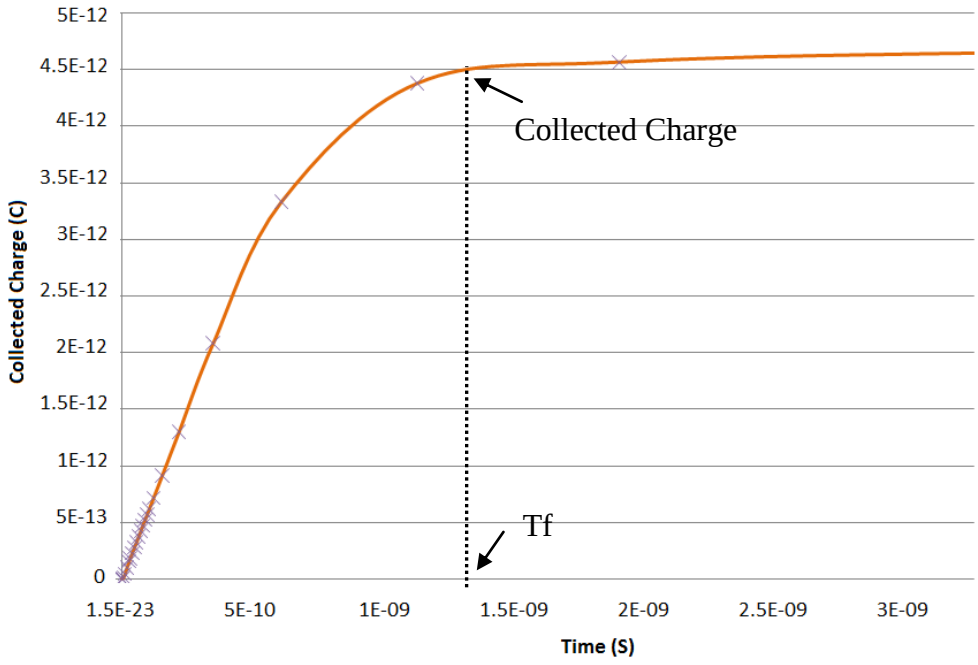


Figure 4.19: Collected Charge

At next chapter the evaluation of transistor sizing technique is approached to evaluate the behavior of the technique during the ionization.

5 TRANSISTOR SIZING TECHNIQUE

The use of transistor sizing technique to harden circuits against radiation effects was first proposed by (ZHOU, 2004) and latter described also in (ZHOU, 2006). The technique is applied increasing the node capacitance by increasing the drain width of the transistor, resulting in a higher critical charge. In the work of ZHOU the technique was evaluated at electric level with results indicating that the technique works. In (LAZZARI, 2008a) the sizing methodology was explored at electric level proposing not only the use of a symmetric sizing (both P/N type transistor) but also an asymmetric sizing in which just one type of transistors is sized.

The charge deposition mechanism which was discussed at chapter 2 is simplified and presented as an electrical representation in figure 5.1. When a charged particle strikes a sensitive site in a CMOS circuit, it generates a current that flows between the drain of the transistor and the bulk. The sensitive sites are the surroundings of the reverse-biased drain junctions of a transistor biased in the off state, as for instance the drain junction of the n-channel transistor in Figure 5.1. The current I_P that flows through the pn-junction of the struck transistor arises from the discharge of the node capacitance (I_C) and from the current conducted by the transistor in the on-state (I_D of the p-channel transistor in Figure 1). The direction of the current depends if the particle is discharging the logic node, or is charging the logic node. The peak current induced by an energetic particle strike is more intense at the drain-bulk junction than at the connection to the power lines.

At the figure 5.1 the particle hit is modeled by a transient current pulse (I_P) that flows between the reverse biased drain-bulk pn-junction of the n-transistor in the off-state. Part of the transient current flow comes from the node capacitance (I_C). The other part comes from Vdd through the p-transistor in the on-state (I_D). The figure depicts the situation for a particle hit at the drain junction of the n-transistor in the off-state (WIRTH, 2007).

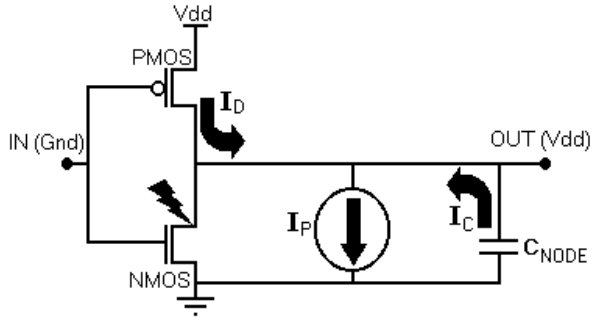


Figure 5.1: Circuit level representation of the charge deposition (WIRTH, 2007b).

The transistor sizing technique aims to increase I_C and I_D in such a way that it is necessary a larger collected charge or current I_P to provoke a SET. In other words, it has as main target the increase of the transistor critical charge.

The problem with the approach used by (ZHOU, 2006; LAZZARI, 2007) is that the transistor sizing technique has a directly impact on the topology of the transistor and due to this reason a more accurate simulation using physical models must be taken into account. Notice that the transistor sizing technique increases the width of the transistor drain which is also the most susceptible part of the transistor to soft errors.

The simulation of the ionization at electric level is done inserting a transient current at the output node of the transistor. This approach is generally done using the double exponential equation (2.12) to model the current. This kind of approach is limited and can't be used to evaluate changes in the topology of the transistor because no simulation is done to evaluate physical characteristics of the topology. At a physical level simulation (which is done in this work) the transistor (shown in the last chapter) is modeled in a 3D structure and physical models are used to allow a proper evaluation of the changes in the topology.

5.1 Devices and Simulations

Simulations of the ionization were taken using a mix mode simulation. The mix mode is a mixture of electrical and device simulation to allow the proper evaluation of the transistor sizing technique. In this simulation, the ionization is done in device mode with the physical models presented in previous chapter, and an electrical simulation is done to simulate the others transistor of the schematic. In this work, a NOT, 2-NAND, 2-NOR gates based on the size of a ST 90 nm standard cell library were evaluated. These simulations are taken using Davinci. Figures 5.2 (a), (b), (c) and (d) show the mix-mode scheme of gates NOT, NAND1, NAND2 and NOR gates. Note that at each of the figure the TCAD device model (n-type transistor) is connected in a different way. This was done to evaluate the possible output conditions that the transistor could have during the ionization. The reader must also be aware that the irradiated device must be at off-state since this is the condition that allows the ion disturbing the operation of the device.

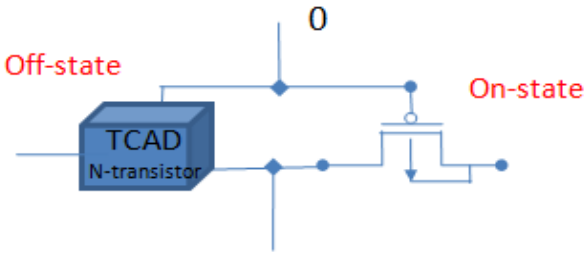


Figure 5.2 (a): NOT gate, input:0, 3D NMOS at off-state.

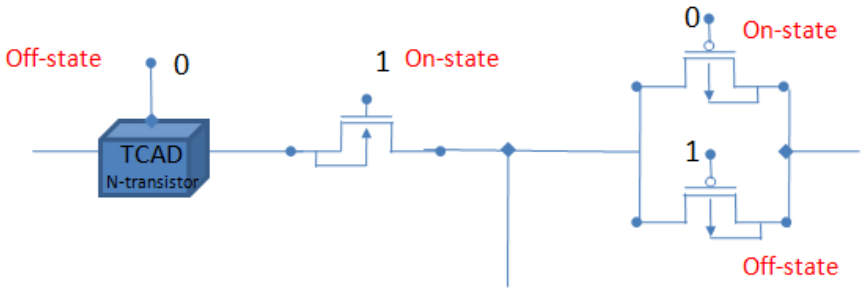


Figure 5.2 (b): NAND gate, input:10, 3D NMOS at off-state connected to gnd.

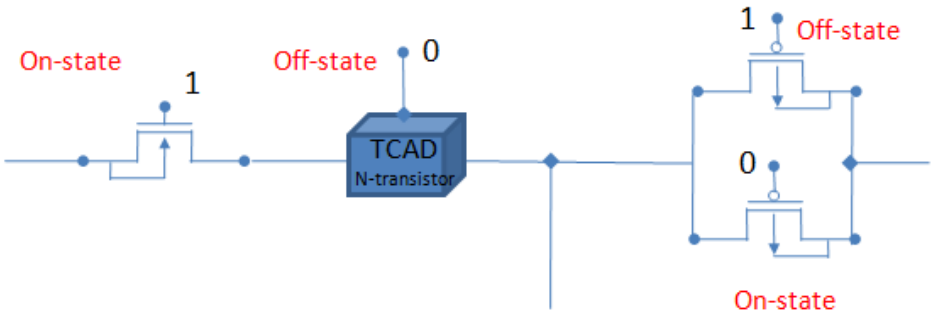


Figure 5.2 (c): NAND gate, input:01, 3D NMOS at off-state at the output.

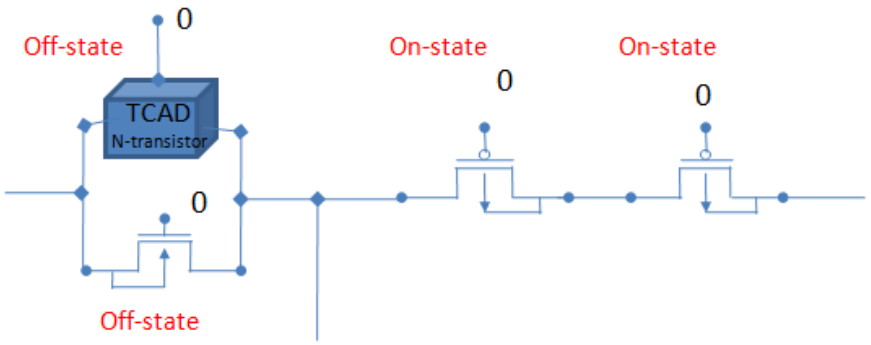


Figure 5.2 (d): NOR gate, input:00, 3D NMOS at off-state.

A load capacitance of 10 fF is added at each cell output. This value was found to be the average drive capacitance of cells from the ST 90nm cell library. The transistors widths of each logic gate during simulations are described in table 5.1 and 5.2.

Table 5.1: 3D NMOS Asymmetric Sizing

Sizes	NMOS transistors Wn(nm)	PMOS transistors Wp(nm)
W0	220	880
W1	510	880
W2	1.020	880

Table 5.2: 3D NMOS Symmetric Sizing

Sizes	NMOS Wn(nm)	PMOS Wp(nm)
W0	220	390
W1	510	880
W2	1.020	1.760
W2_3	2.040	3.508
W3	3.060	5.263
W4	4.080	7.017
W5	5.100	8.772

For all simulations, the output of the irradiated device is at the logical value ‘1’ (VDD=1.2 V). Once the ion is injected, the voltage may drop, which can characterize a SET occurrence. A SET is considered when the gate output voltage drops to VDD/2 or

bellow. The effect of sizing the gate that is at the output of the irradiated device was also verified. Table 5.3 shows the output capacitances used with the irradiated device to simulate the sizing of the next gate stage.

Table 5.3: Output Capacitances placed at the target gate output

Name	Capacitance	Name	Capacitance
C1	10f F	C6	500f F
C2	20f F	C7	1p F
C3	40f F	C8	10p F
C4	80f F	C9	20p F
C5	160f F		

The selected ions which were already indicated at chapter 4 are summarized at table 5.3 with their energy, LET and radial distribution. For sea level-alpha particles, the chosen LET is around 1 MeV/(mg/cm^2), while for heavy ions, LETs up to 20 MeV/(mg/cm^2) were used.

Table 5.4: Ion profiles used at simulations

Element / Energy	**LET(dE/dX) MeV/(mg/cm^2)**	**Radial (r) μm**
Alpha – 1 MeV	1.31	0.05
Cu, 395 MeV	26.5	0.5
Kr, 270 MeV	40.5	0.65

Two impact vectors were simulated. The first one is an impact at the center of the device with a total path of 60 nm inside the drain; and the second a vector called worst case was mentioned at chapter 4 and showed in figure 4.2. During simulations it was noticed that no difference was seen in the behavior of sizing simulations of both angles. So the results that will be presented at next section will focus on the 90º impact vector. In figure 5.3 a 90º impact at the center of the drain structure is showed. Colors indicate potential contour of electron current.

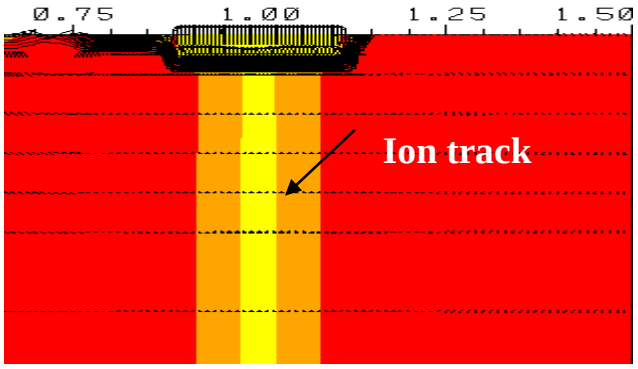


Figure 5.3: 3D NMOS transistor during ionization

This image illustrates the difference between electrical and device simulation. Note that the ionization is really simulated instead of using a transient current that is directly injected at a specific node of the circuit. In next section the results of the simulation are presented.

5.2 Transistor Sizing Results

The alpha particle was the first ion injected in the 3D NMOS transistor drain using three transistor dimensions (W0, W1 and W2) for each symmetric and asymmetric case. In this case, the NOT gate was evaluated. Alpha particle analysis is very important for ground level applications due to the higher flux of these particles in this level when compared with other particles.

The primary analyzed parameter is the collected charge of the irradiated device. The collected charge is the integration of the transient current pulse that is generated by the ionization particle. By increasing the transistor width, the collected charge increases due to the increase of the ion-current, as shown in figure 5.4(a) for the NOT gate. The NAND and NOR gate have shown similar results. By analyzing the model presented in figure 5.1, this means that when the transistor size increases, the current I_P tends to increase as well. This means that although I_C and I_D may increase because of the transistor resize, the collected charge also increase (I_P). The symmetric and asymmetric sizes may differ at this time due to the currents I_D that are able to restore the upset and the asymmetric sizing effect can be beaten observed when analyzed the transient voltage pulse peak.

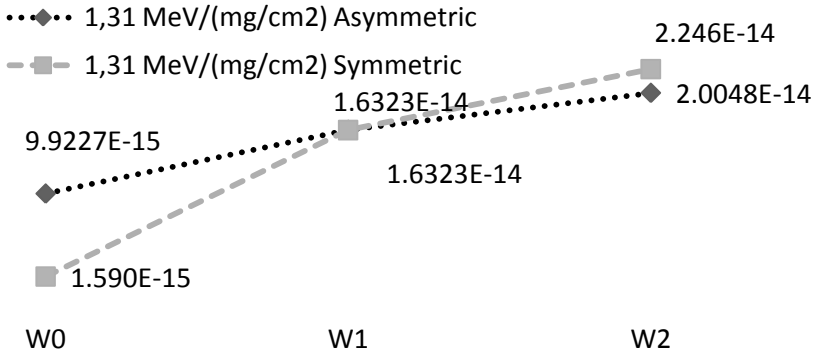


Figure 5.4 (a): Alpha Particle, NOT, Collected Charge (C)

The second analyzed parameter is the drain voltage peak presented in figure 5.4(b). The figure shows a possible reduction of the SET pulse peak during the symmetric sizing. The asymmetric sizing can present a better result compared to symmetric sizing in case of W0 and a worst result in case of W2. Note that when an asymmetric sizing is done, the current I_C and I_D are not well balanced anymore. This results in a faster or slower restoring time. W0 has a faster restoring time, while W2 presents a slower restoring time.

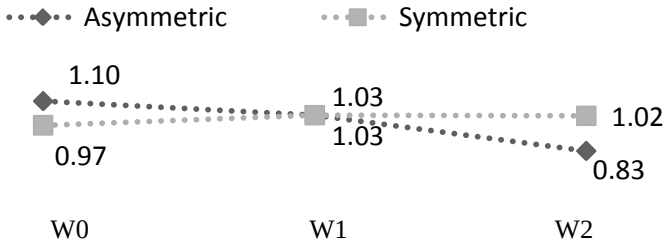


Figure 5.4 (b): Alpha Particle, NOT, SET Pulse Peak (V)

Notice that the collected charge for both sizing techniques shows an increase, as shown in figure 5.5(a), with a higher rate in the asymmetric case because Wn increases in a higher proportion than the Wp. Results for NOR cell are also similar. Notice the behavior of the asymmetric sizing allowing worst pulses for wider transistors, as also shown before for the NOT cell.

The collected charge showed in figure 5.5 (a) the sizing had the same behavior seen for the NOT cell. For both symmetric and asymmetric sizing the increase of the drain width results in the collection of more charge.

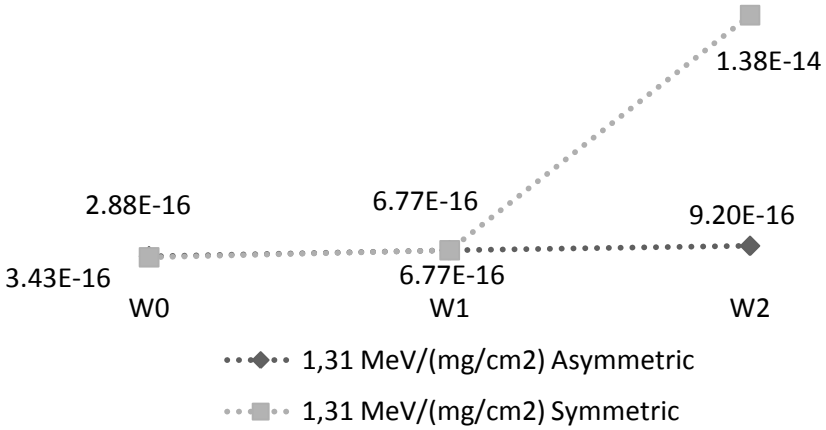


Figure 5.5 (a): Alpha Particle, NOR, Collected Charge (C)

For the transient voltage pulse peak of the NOR cell, similar results were seen. In symmetric sizing a possible recovery is shown and in asymmetric sizing no recovery is noticed as shown in figure 5.5 (b).

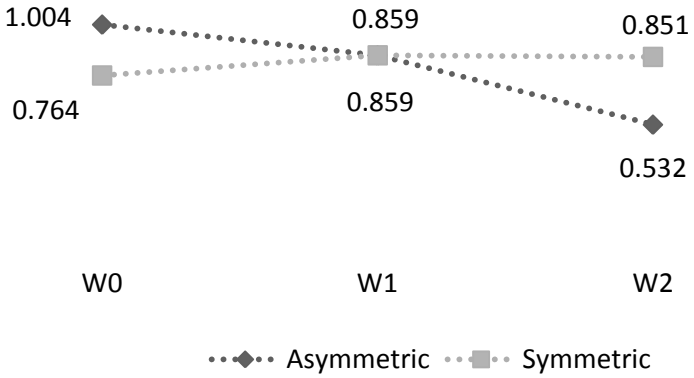


Figure 5.5 (b): Alpha Particle, NOR, SET Pulse Peak(V)

With the NAND (01) cells the results also shown the same behavior notice for the NOR and NOT cells as seen in figure 5.6 (a) for the transient voltage pulse peak and (b) for the collected charge.

For the collected charge seen in figure 5.6 (a) both sizing increases the collected charge going from 3.63fC to 5.5fC to symmetric sizing and from 3.09fC to 27.3fC in asymmetric sizing.

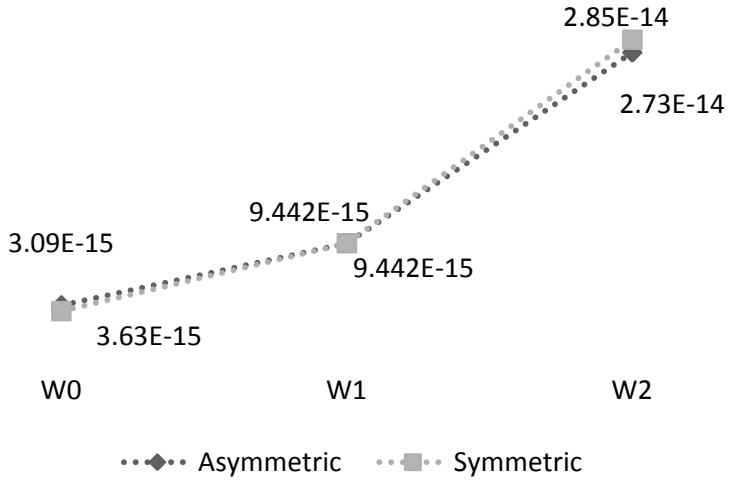


Figure 5.6 (a): Alpha Particle, NAND 01, Collected Charge (C)

For the transient voltage pulse peak in figure 5.6 (b) it is observed the same behavior noticed for the others cells. A possible recovery is also noticed for the symmetric sizing.

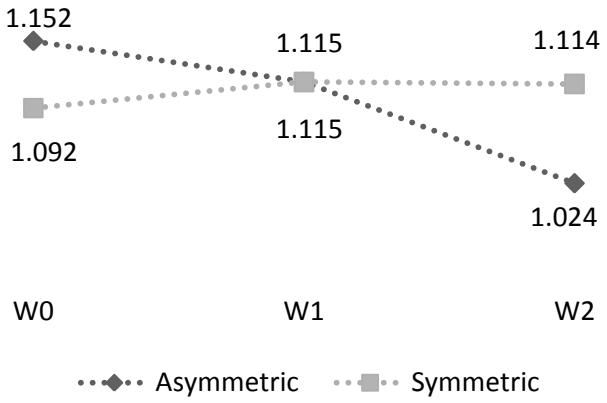


Figure 5.6 (b): Alpha Particle, NAND 01, SET Pulse Peak (V)

In simulations using a NAND with the input (10) in which the irradiated device is connected to the ground, any of the ions were able to disturb the output to a value close to VDD/2 (0.6 V). This means that none of the ions were able to cause a SET at the device output.

Simulations of alpha particle were extended using the NOT gate topology and results are presented at the following. In Figure 5.7(b) more alpha particle results when the transistor sizing is increased (W2_3, W3, W4 and W5). One can see that for a large transistor width, the SET pulse amplitud reduces significantly. For example, comparing W5 to W0, the voltage drop has reduced from 0.245V to less than 0.1V. Although, the collected charge increases with the transistor size, this does not implies in a higher SET because of the symmetric sizing. The PMOS transistor current also increases, which allows a faster and more efficient SET recovery. The current continues to get worst until W4 where its starts to saturate.

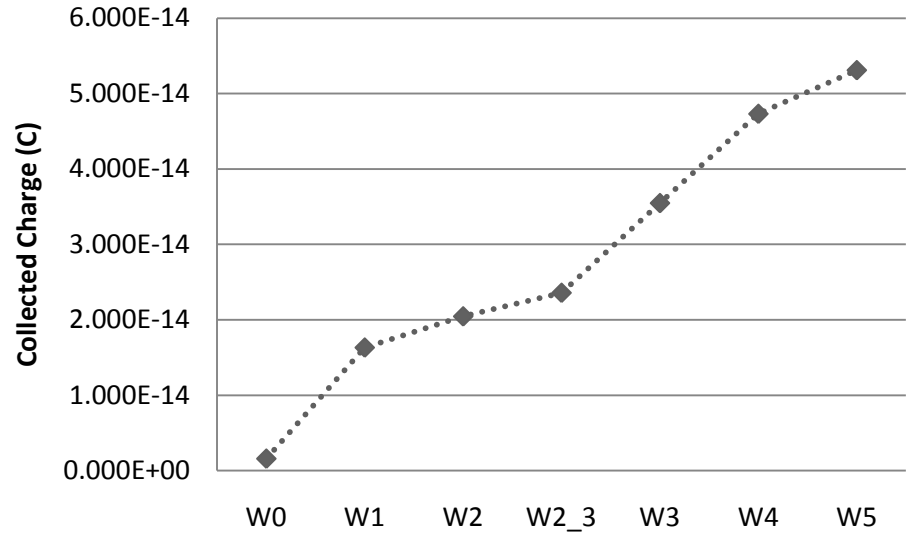


Figure 5.7 (a): Alpha particle -NOT – Collected Charge (C)

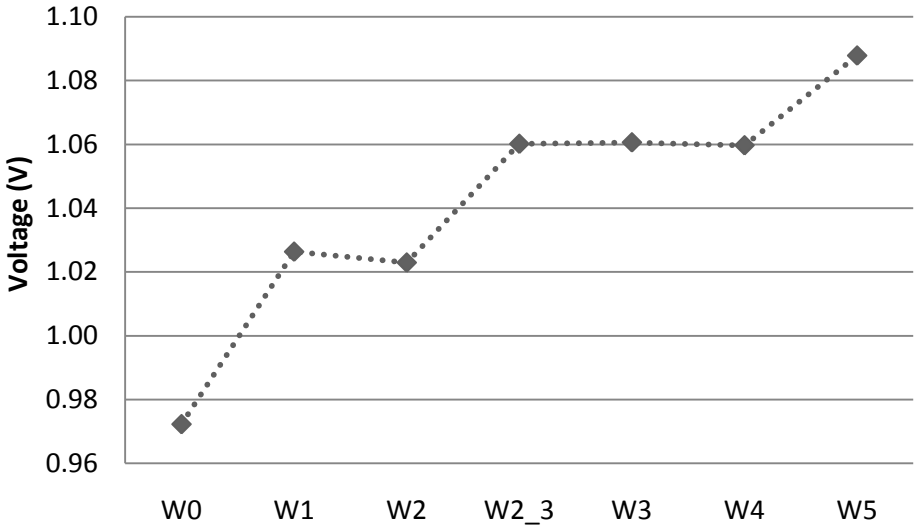


Figure 5.7 (b): Alpha particle- NOT- SET Pulse Peak (V)

In figure 5.7(a) it is possible to notice the saturation of the collected charge. This is expected since a certain drain width most of the charge injected by the particle is collected. This saturation will depend on several factors like the particle LET and radial distribution of carriers and geometry and doping profile of the transistor.

It is important to observe that the alpha particles did not provoke a SET in the logic gates because the output voltage did not reach VDD/2. This means that there was no enough charge collected in the NMOS drain node able to provoke a significant voltage swing for that specific transistor sizes.

To improve the study the effect of sizing the cells that are connected in their input of the irradiated cell were also evaluated as shown in figure 5.8. The drain voltage results for alpha particles (1.31MeV/(mg/cm^2)) irradiating a NOT gate sized as Wn=3.060um and Wp=5.293um. Results show that the increase of the capacitance reduces the transient pulse amplitude generated by the particle. The variation of the pulse peak goes from 1.06V to 1.13V when the capacitance of the output is increased from 10fC to 160fC respectively. This shows that for low energy particles, the gate

sizing and the sizing of the next gate stages connected to the target node can be efficient to reduce or mitigate the SET.

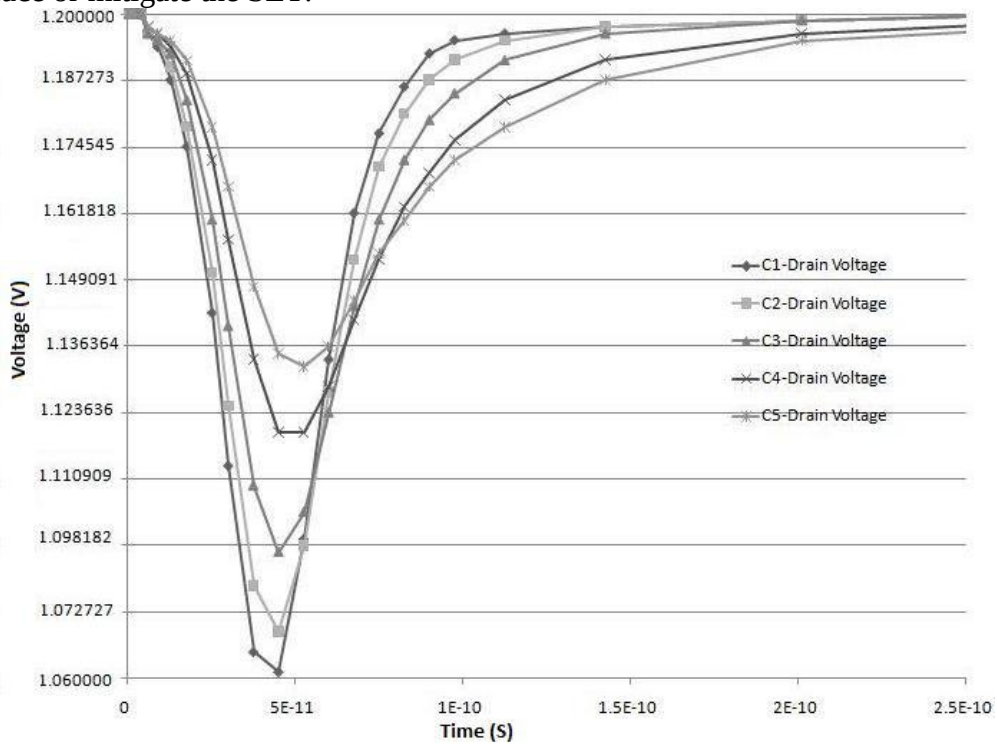


Figure 5.8: Alpha particle - Transient voltage pulse to different capacitances

Aiming at increasing the ion LET (MeV/mg/cm^2), ions of Kr and Cu were injected at the same gates. This analysis is important for space applications due the high LET of particles in space. The transient current has presented the same behavior for ions Kr and Cu compared to alpha particle. However, when analyzing the transient voltage peak, the behavior of the higher LET ions was not the same compared to the alpha particle. For both symmetric and asymmetric sizing, the SET increases with an increase on the transistor width, as shown in figure 5.9 (a) for Cu and (b) the Kr ion.

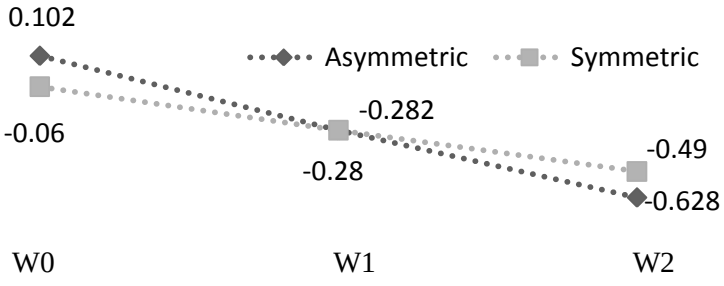


Figure 5.9 (a): Cu ion, NOT, SET Pulse Peak (V)

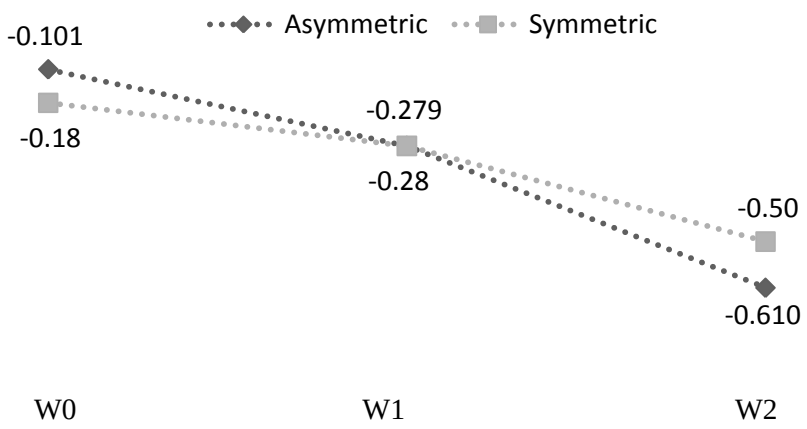


Figure 5.9 (b): Kr ion, NOT, SET Pulse Peak (V)

The Collected charge for both ionizations increases with the sizing of the device. In figure 5.10 (a) is presented the collected charge of Cu and (b) for the Kr ion.

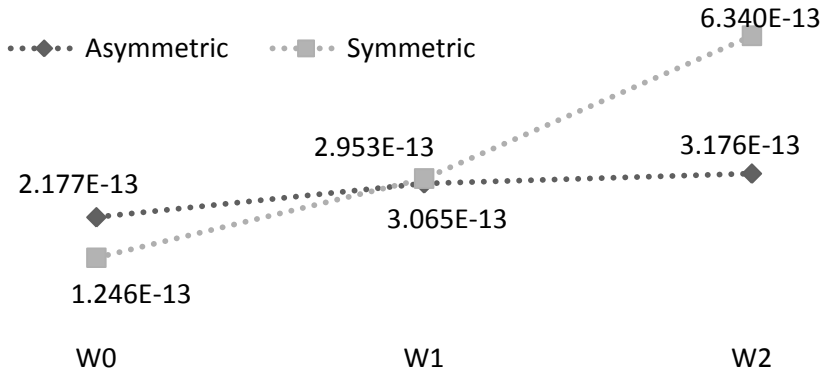


Figure 5.10 (a): Cu ion, NOT, Collected Charge (C)

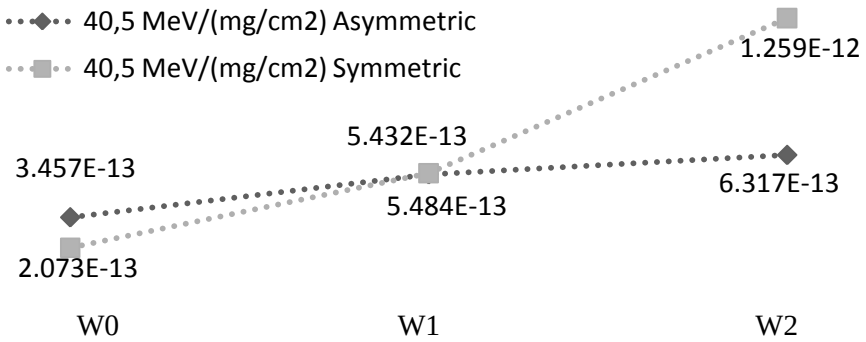


Figure 5.10 (b): Kr ion, NOT, Collected Charge (C)

The sizing of the device had also shown increases in the transient voltage pulse width, as notice in figure 5.11(a) for Cu and 5.11 (b) for Kr ion. The pulse width goes from 1.85ns to 5.35ns in symmetric sizing and from 0.48ns to 11.34ns in asymmetric sizing.

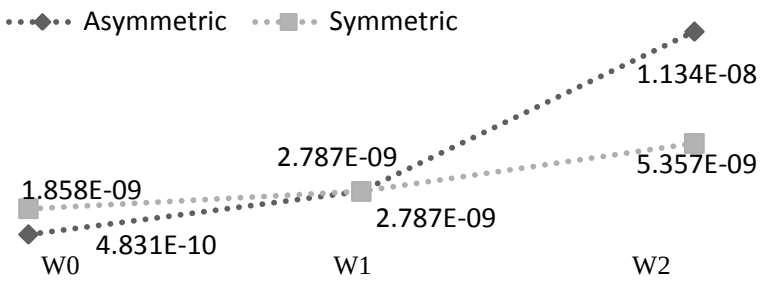


Figure 5.11 (a): Cu ion, NOT, Pulse Width (s)

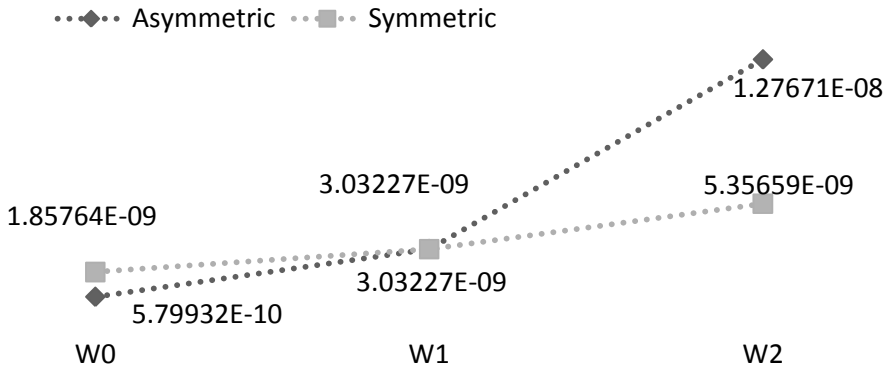


Figure 5.11 (b): Kr ion, NOT, Pulse Width

Simulations of NOR cell had also shown the same behavior seen for the NOT cell. In figure 5.12 (a) is shown the collected charge of the Cu and in figure 5.12 (b) for the Kr ion.

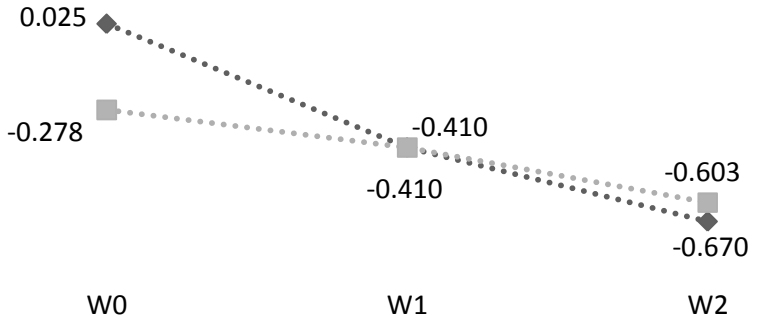


Figure 5.12 (a): Cu ion, NOR, SET Pulse Peak (V)

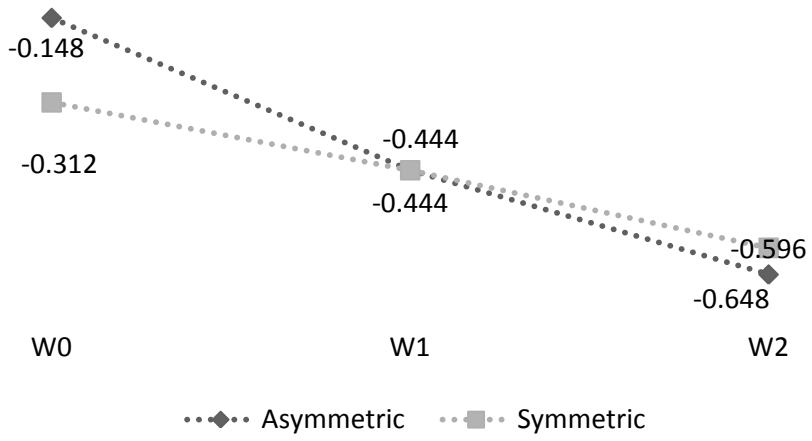


Figure 5.12 (b): Kr ion, NOR, SET Pulse Peak (V)

The transient voltage pulse width had shown similar results presented for the NOT cell as seen in figure 5.13 (a) for Cu and (b) for Kr ion. The pulse width ranged from 5.06ns to 10.88ns to Cu symmetric and 1.09ns to 6.48ns to Cu asymmetric. For the Kr the range was from 5.19ns to 12ns in symmetric sizing and 1.21ns to 9.21ns to asymmetric sizing.

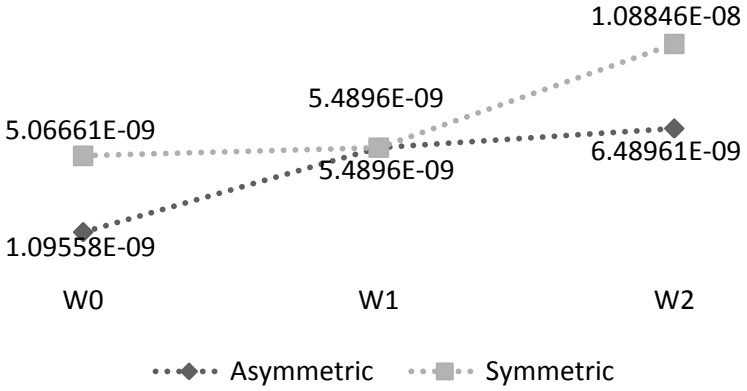


Figure 5.13 (a): Cu ion, NOR, Pulse Width (s)

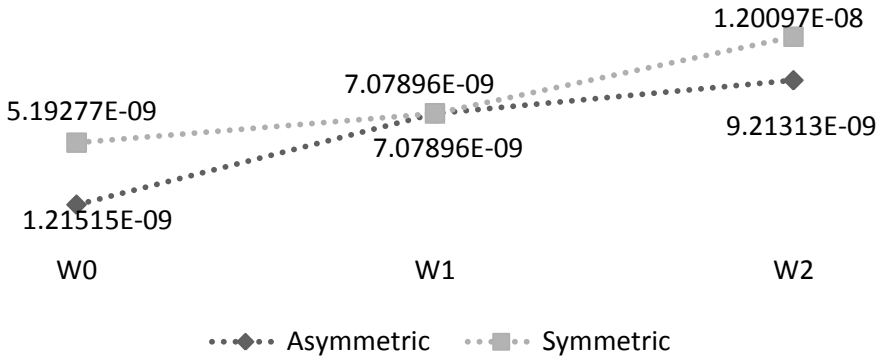


Figure 5.13 (b): Kr ion, NOR, Pulse Width (s)

For the NAND 01 cell similar results were obtained. The NAND 10 cell as indicated before for alpha particle has not shown to be a concern since no pulse was propagated.

The effect of the sizing of the next gate stage was also evaluated to the 26.5MeV/(mg/cm^2) ion. In figure 5.14, it is possible to verify the reduction of the amplitude of the transient pulse with the increase in the output capacitance. However, it must be also notice that the pulse width duration in this case increases, making the transient more significant to the device. This happens because with the increase of the capacitance the restore time also increases making the transient voltage pulse width to increase as well.

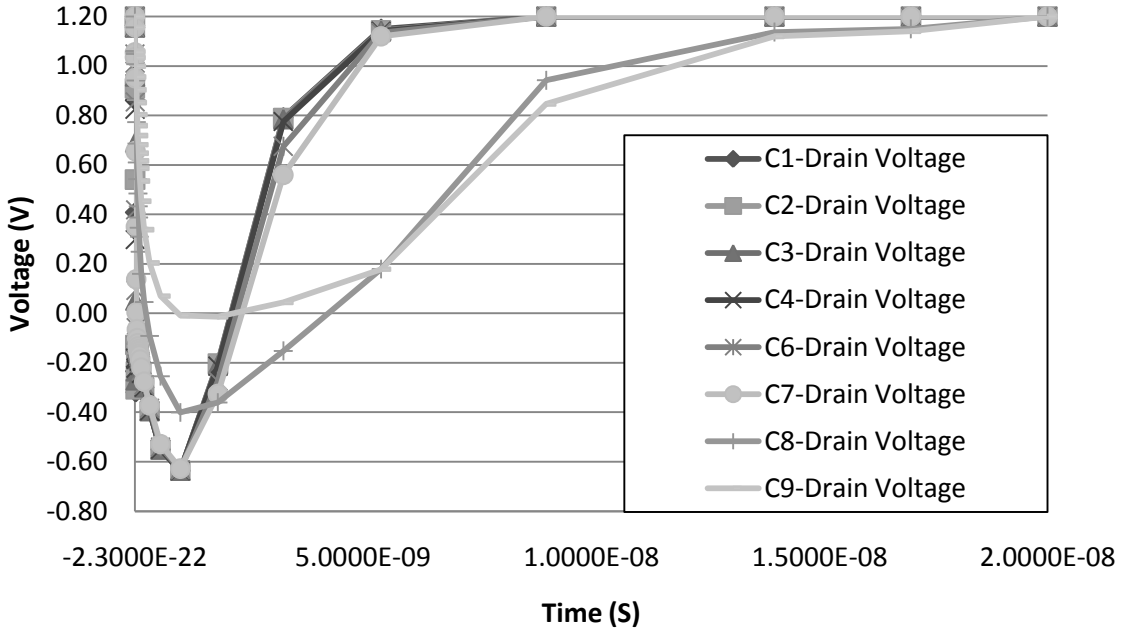


Figure 5.14: 26.5MeV/(mg/cm^2) - Transient voltage pulse to different output capacitances

When concerning about asymmetric sizing, the output voltage transient pulse can be degraded when dealing with high LETs. This can occur when increasing the size of the pull-up transistor, the one responsible to restore the SET. Table 5.5 shows the SET (Cu and Kr) pulse duration results when the NOT PMOS transistor was sized to Wp=390nm and Wp=880nm keeping Wn=220nm in both cases.

Table 5.5: Pull-up transistor is sized

Using a fixed Wn=220nm	**Cu Ion Pulse Width**	**Kr Ion Pulse Width**
Wp=0.390nm	5.066e-9	5.193e-9
Wp=0.880nm	1.095e-9	1.215e-9

These results shows that the SET that is generated from ‘1’ to ‘0’ can be degraded when the PMOS transistors are larger than the NMOS transistor. However, if we consider the PMOS transistor as the ion target, the chosen asymmetric sizing in this case

would increase the SET duration from ‘0’to ‘1’. This shows that there is no good solution for asymmetric transistor resizing when considering SETs in both PMOS and NMOS transistors according to the input logic vector.

5.3 Related Work

The results showed before contradict the results of the evaluation of transistor sizing against radiation effects made at electric level. As it was already mentioned there are a great number of differences between these simulations that could make these results differ. Researching possible justifications to the increase of the current generated by the ion when the device is sized, some references were found.

The first work from (HYUNGSOON 1999) at IEEE TRANSACTIONS ON ELECTRON DEVICES in 1999 reports the modeling of alpha-particle soft error rate in DRAM. The work shows that the increase of the junction area imposes an increase of the funneling of the electric field during the ionization. In the figure 5.15 the collected charge and junction area are correlated.

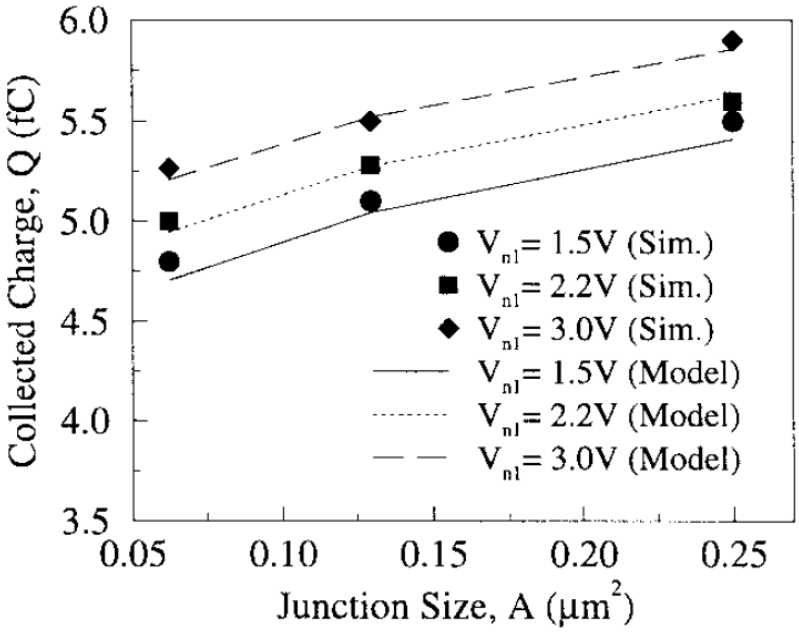


Figure 5.15- Collected charge vs. junction size (HYUNGSOON, 1999)

The work of HYUNGSOON is also supported by (JOHNSTON, 2000). Notice that the junction area of the drain is close related with the drain area. The junction area is increased with the same ratio of the increase of the drain during the transistor sizing.

Another work of (BAUMANN, 2005) published at IEEE TRANSACTIONS ON DEVICE AND MATERIALS RELIABILITY (2005) reports that large area junctions are efficient in collecting radiation induced charge.

Besides these aspects, a work done by (HAZUCHA, 2003) from Intel Corporation shows the effect of the scaling of the diode area for both PMOS and NMOS diodes. These results showed in figure 5.16 (a) and (b) indicate that sizing the devices had produced more soft errors. These tests were done using a particle accelerator in a circuit with a 90nm CMOS Process.

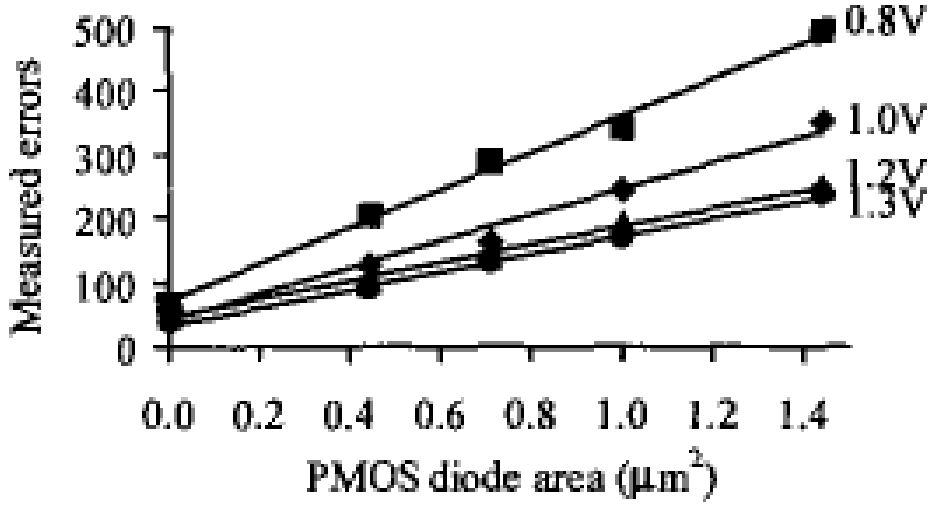


Figure 5.16 (a): PMOS Diode area vs. Errors (HAZUCHA, 2003)

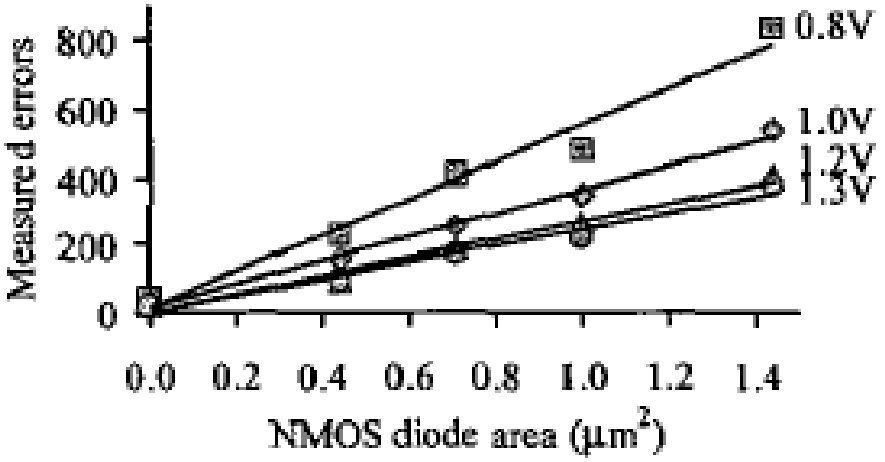


Figure 5.16 (b): NMOS Diode area vs. Errors (HAZUCHA, 2003)

The results showed in this section clearly indicates that sizing of the drain area produces more errors and allows the increase of the collected charged.

5.4 Transistor Sizing Conclusion

The transistor sizing technique was evaluated for a 90nm technology and the results show that the technique depends on the radiation environment profile.

For alpha particles, the transistor symmetric sizing technique is able to degrade the transient pulse due to the lower LET of the particle. However, for higher LET the technique showed not to be efficient. In this last case, the SET can increase in amplitude and duration when transistors are increased in size. This can make the SEE phenomena even worse. Results also showed that asymmetric transistor sizing of the device that is not hit can reduce SET amplitude and duration for low and high LETs, but while they improve in one side the SET generated at the NMOS transistors, they aggravate the SET generated at the PMOS transistors.

SET mitigation solutions may first try to reduce the SET generation and next reduce the probability of them to propagate into the circuit. Results presented here can guide

transistor sizing using CAD tools. As it has been observed, for SET generation (amplitude and duration), it is important to analyze the gate sizing and the next gate stage sizing as well. But the sizing of each gate level stage may also impact the entire circuit concerning the SET propagation that can be broadening or filtered according to the gate delays. Transistor sizing techniques should take into account all these effects.

6 TRANSISTOR FOLDING

The transistor folding technique is used to make tall transistors folded into shorter ones to cope with a standard cell height providing regularity to a strip of cells (HER, 1993). This approach allows a layout area minimization and contributes to the cell placement since the cells is fixed. A symbolic example of folding is shown in figure 6.1 to connect 2 not cells together, each of them with different sizes. The approach used at the 2 NOT cells of the right part of figure 6.1 allows the connection of both NOT cells been regular without wasting area as will be done to connect the cells of the left part of the figure.

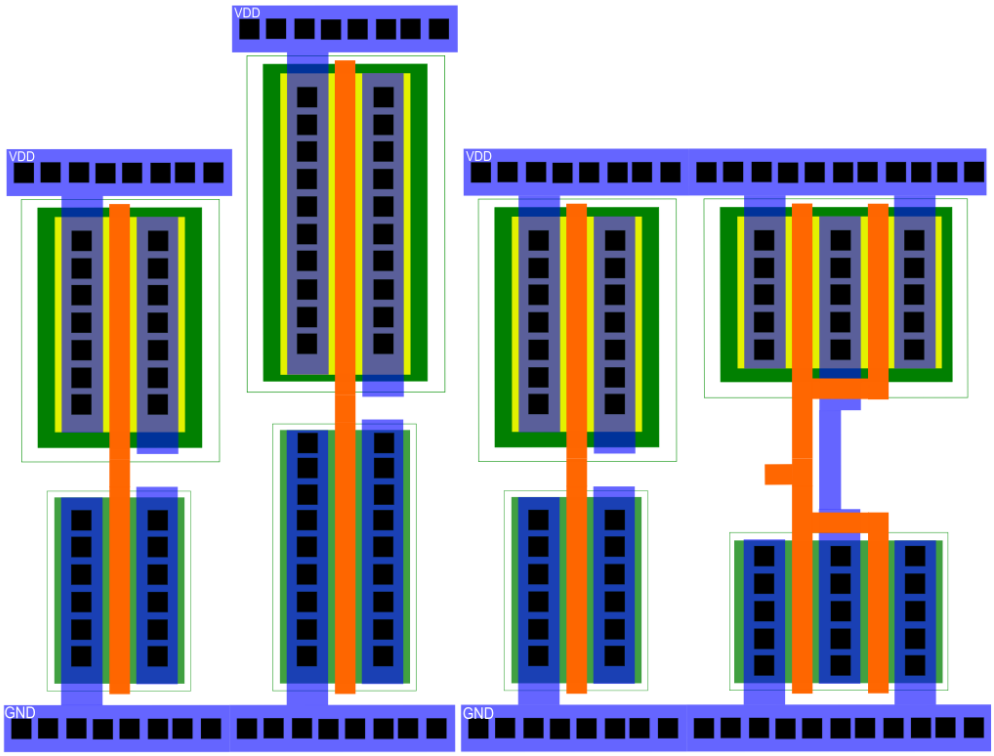


Figure 6.1: Layout not folded and folded.

In this chapter transistor folding technique is used to divide the stroke node into many other nodes according to the number of parallel transistor segments used in the folding. These nodes are connected usually by metal layers, which present some resistance. So, when a particle hits one the nodes of the folded transistors, the other nodes remain untouched for a certain period of time according to the resistance that connects them. This may help with the recover process. Transistor folding and transistor-sizing technique can be applied at both, electrical and layout levels. The device representation of the folded n-type transistor is shown in figure 6.2

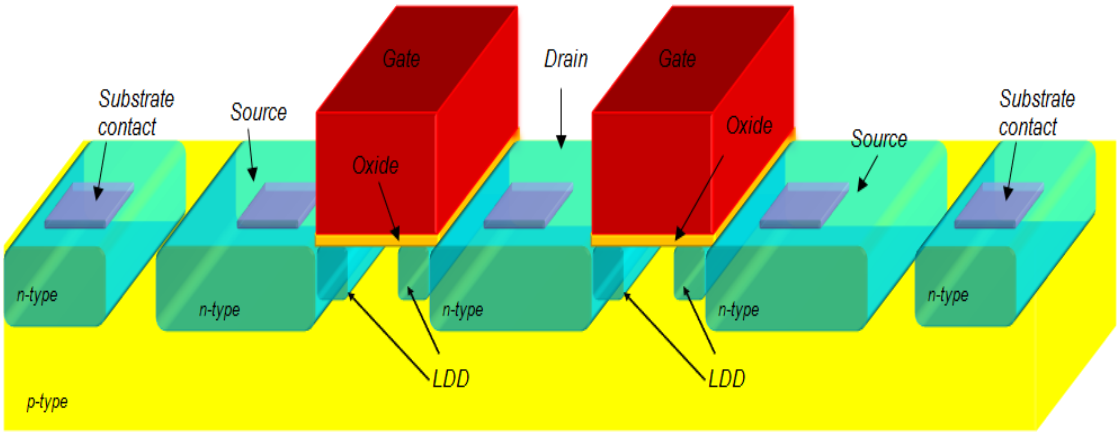


Figure 6.2: NMOS with folding

Notice that with the results presented in the last chapter it is possible to increase the width of the cell without increasing the junction area because this region will be broken into small ones by the folding.

6.1 Transistor Folding Device Simulations

The susceptibility of the device to SET was evaluated by three main parameters: transient pulse amplitude peak, transient duration and collected charge. The devices are irradiated with the 3 particles mentioned previously and showed in table 5.4. All measurements were done at the drain of the n-type device. The transistor widths of each logic gate used during simulation are described in table 6.1. In table 6.1 the numbers of parallel segments used at the folded devices are indicated by a number (n) that is multiplied by the standard transistor width used in simulations. Example: for the gate W2_S the NMOS transistor has four parallel segments for both P/N transistors each of them with 1.760 um and 1.020 um respectively. Notice that the table shows devices that were also sized but not folded.

Table 6.1: 3D NMOS Symmetric Sizing

Sizes	PMOS Wp(um)	NMOS Wn(um)	Sizes Folding	PMOS Wp(um)	NMOS Wn(um)
W0	3.52	2.040	W0_S	2x1.760	2x1.020
W1	5.28	3.06	W1_S	3x1.760	3x1.020
W2	7.04	4.08	W2_S	4x1.760	4x1.020
W3	8.8	5.1	W3_S	5x1.760	5x1.020
W4	10.56	6.12	W4_S	6x1.760	6x1.020

To have a better evaluation of the effectiveness of folding, the number of parallel segments during the folding was also evaluated. The devices sizes are shown in table 6.2. This helps to evaluate the behavior of the ratio of folding at the device. The devices are named as *Wni*, where “i” indicates the number of devices in parallel.

Table 6.2: 3D NMOS varying number of parallel devices

Sizes	PMOS Wp(um)	NMOS Wn(um)
Wn1	1x8.8	1x5.1
Wn2	2x4.4	2x2.55
Wn3	3x2.933	3x1.7
Wn4	4x2.2	4x1.275

In all simulations, the output of the irradiated device is at the logical value '1' (VDD=1.2 V). Once the ion is injected, the voltage may drop, which can characterize a SET occurrence. A SET is considered when the gate output voltage drops to VDD/2 or bellow. Note that in the next figures the devices at the horizontal axis are named W0,1,2,3,4 and the legend inside the figure indicates if the device is folded or not.

6.2 Transistor Folding Results

Irradiating the devices with alpha particle profile of 1.31 MeV/(mg/cm^2) had shown similar results for devices with and without folding as seen in figure 6.3(a) for the pulse amplitude peak. The sizing of the transistor with folding or not was able to reduce the peak of the transient pulse. Note that for the W4 device the alpha particle was not able to disturb the device. The variation of the peak ranged from 1,01V to 1.2 V as is seen in figure 6.3(a). The measured collected charge was found to be higher at devices which are not using folding as seen in figure 6.3(b).

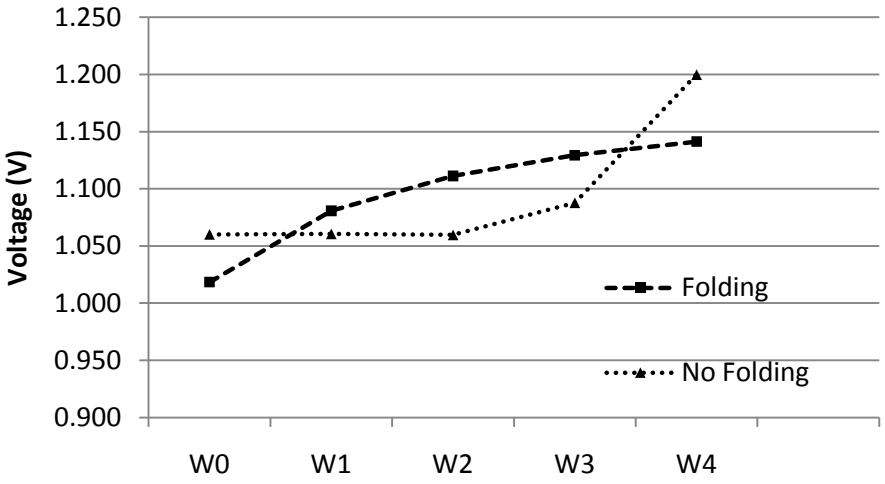


Figure 6.3 (a): Alpha Particle, SET Pulse Peak (V)

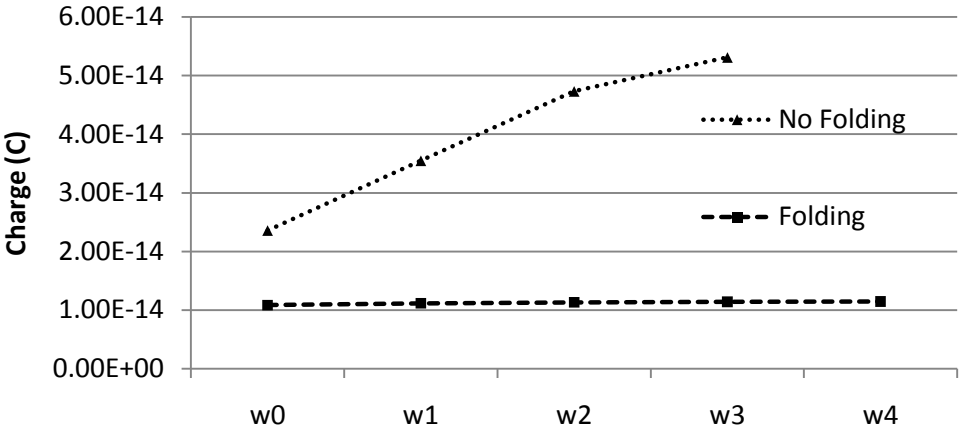


Figure 6.3 (b): Alpha particle, Collected Charge (C)

Using a high energy profile of 26.5MeV/(mg/cm^2) simulations had shown different results over the behavior of the transient pulse. The measured amplitude peak of the transient pulse for folded devices had shown a signal recovery when the device is sized as shown in figure 6.4(a). The sizing without folding was not able to improve the tolerance of the devices and had the opposite behavior noticed with folded devices. The pulse amplitude peak is increased with the increase of the device without folding.

The width of the transient pulse was also evaluated as shown in figure 6.4(b). A similar behavior is noticed for folded devices, reducing the pulse width and not folded devices increasing the pulse until a certain point (w4 device). After this point (W4) the sizing without folding starts to reduce the pulse width.

The collected charge has the same behavior noticed with alpha particles as seen in figure 6.4(c). Devices without folding presents higher collection when compared with devices folded.

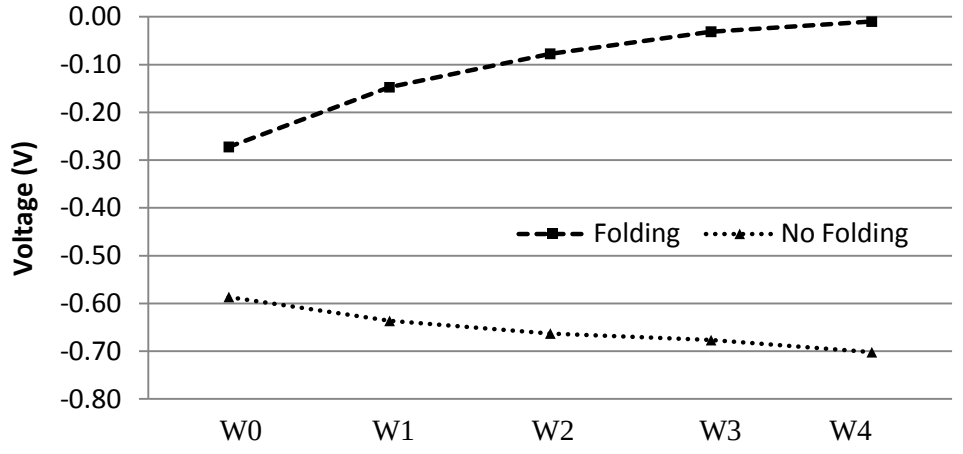


Figure 6.4 (a): 26.5 MeV/(mg/cm^2) ion – SET Pulse Peak (V)

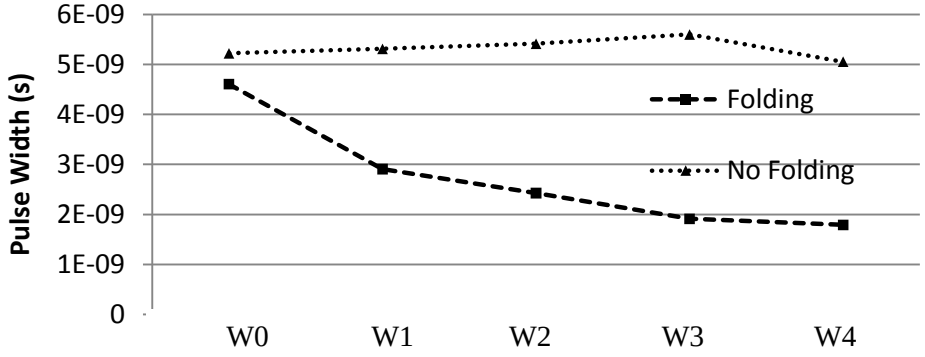


Figure 6.4 (b): 26.5 MeV/(mg/cm^2) ion - Pulse Width (s)

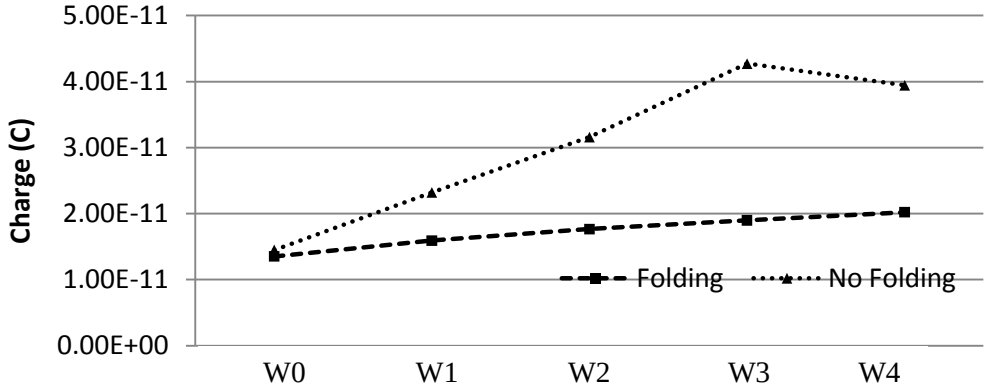


Figure 6.4 (c): 26.5 MeV/(mg/cm^2) ion – Collected Charge

The profile of a heavy ion of 40.5MeV/(mg/cm^2) was also used to irradiate the device. In figure 6.5(a) the amplitude pulse peak is evaluated having the same behavior presented for 26.5MeV/(mg/cm^2). The recovery of folded devices and the increase of the SET pulse for devices not folded are noticed in the figure.

The pulse width and collected charge are shown in figure 6.5(b) and 6(c). The same behavior is obtained for both devices when compared with results for the 26.5MeV(mg/cm^2) particle.

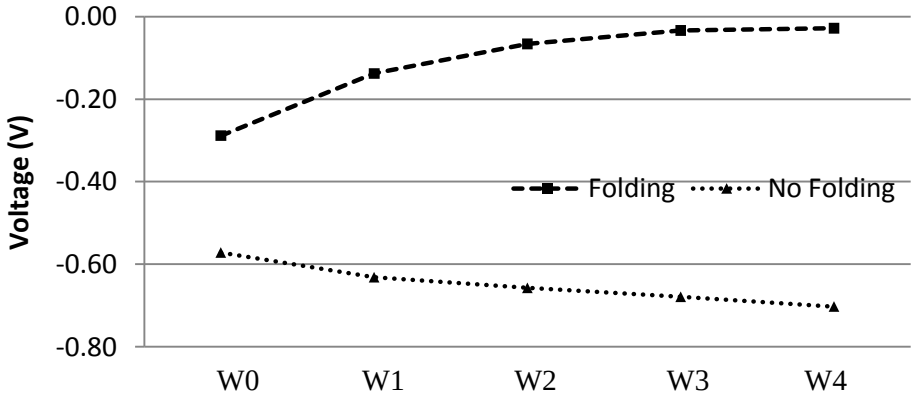


Figure 6.5 (a): 40.5 MeV/(mg/cm^2) ion – SET Pulse Peak (V)

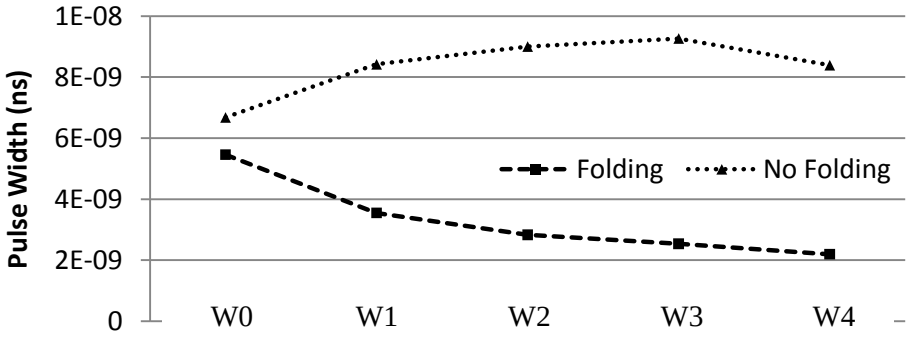


Figure 6.5 (b): 40.5 MeV/(mg/cm^2) ion - Pulse Width (s)

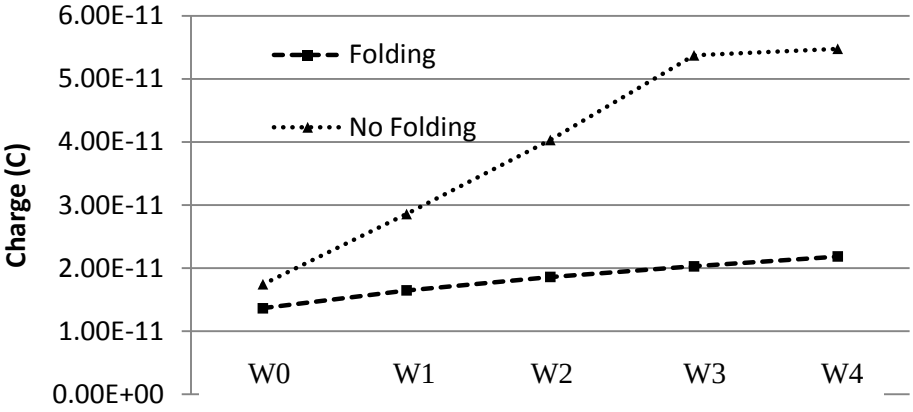


Figure 6.5 (c): 40.5 MeV/(mg/cm^2) Ion – Collected Charge (C)

Willing a better evaluation of the effectiveness of folding, the number of parallel devices during the folding was also evaluated. The devices properties were shown in table 6.2. The irradiation using alpha particles with 1.31MeV/(mg/cm^2) had the pulse amplitude peak shown in figure 6.6. The recovery is noticed when the devices is folded in more partitions.

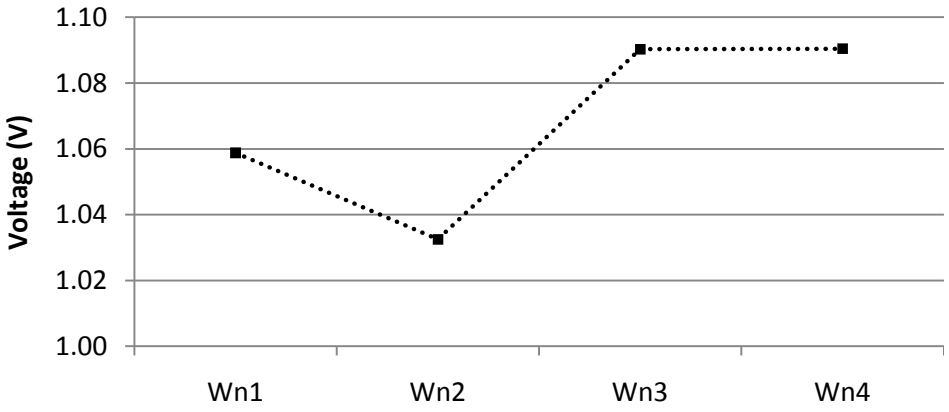


Figure 6.6: Alpha Particle – SET Pulse Peak (V) for 1.31 MeV(mg/cm^2)

For 26.5MeV/(mg/cm^2) particles the collected charge the folding had allowed a reduction of 42.7pC to 30.7pC as seen in figure 6.7 (a).

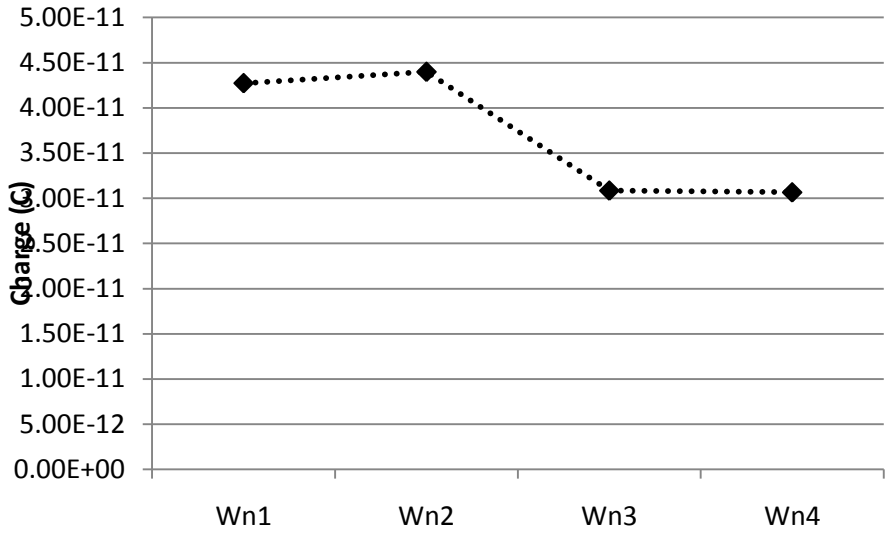


Figure 6.7 (a): 26.5MeV/(mg/cm^2) ion- Collected Charge (C)

The pulse amplitude peak is shown in figure 6.7(b). A consistent recovery is seen when the ratio of devices is increased with the peak of the transient going from 0,68V to about 0,13V.

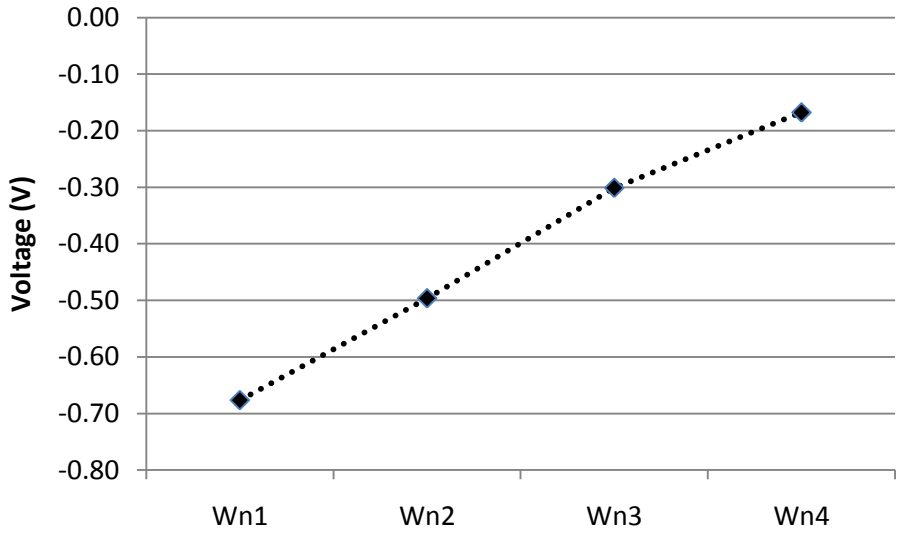


Figure 6.7 (b): 26.5MeV/(mg/cm^2) ion- SET Pulse Peak (V)

The pulse width is reduced from about 5.6 ns to about 3.2ns just folding the device in 4 small transistors. As seen in figure 6.7 (c).

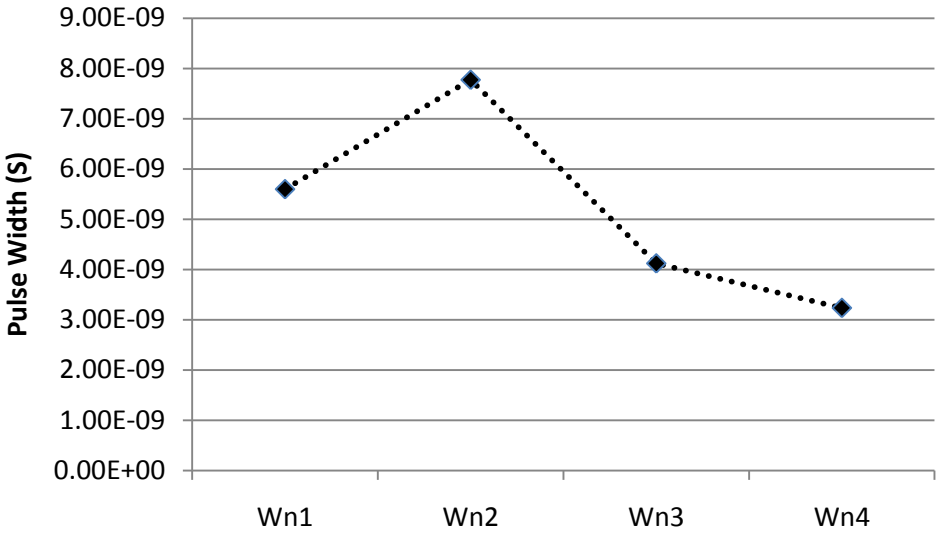


Figure 6.7 (c): 26.5MeV/(mg/cm^2) ion- Pulse Width (s)

For the Kr ion of 40.5MeV/(mg/cm^2) the collected charge had shown also a reduction as seen for Cu results. The collected charge for Kr is seen in figure 6.8 (a) with the charge going from 53.7pC to 29.9pC for a folding rate of 4 transistors.

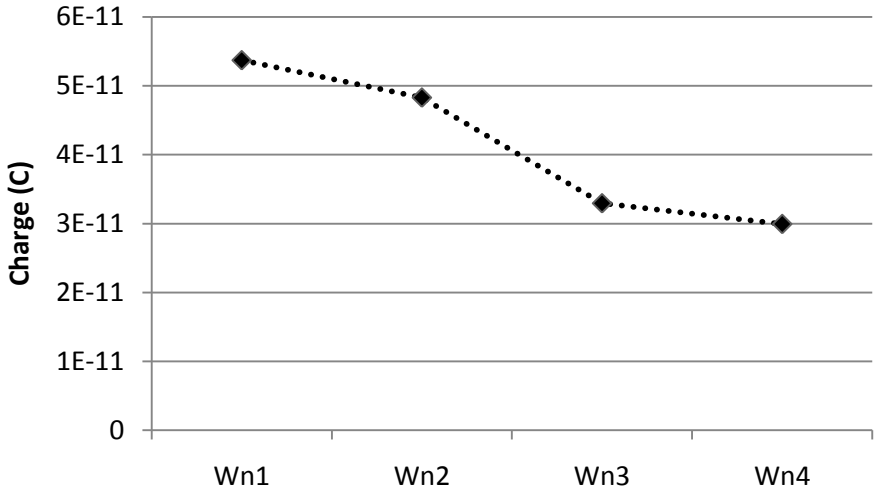


Figure 6.8 (a): 40.5MeV/(mg/cm^2) ion- Collected Charge (C)

The transient voltage pulse peak had shown a recovery when the device is folded. The peak gone from -0.67V to -0.12V as seen in figure 6.8 (b).

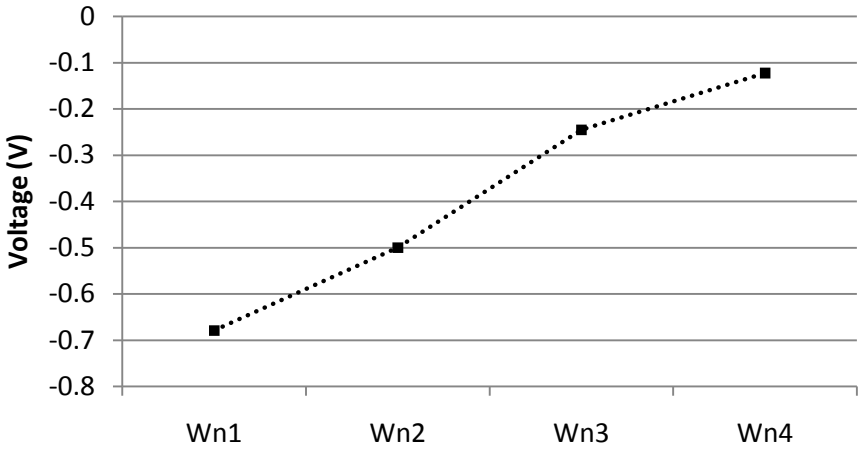


Figure 6.8 (b): 40.5 MeV/(mg/cm^2) ion -SET Pulse Peak (V)

The transient voltage pulse width had also shown significant reduction going from 9.2ns to 3.9ns as seen in figure 6.8 (c).

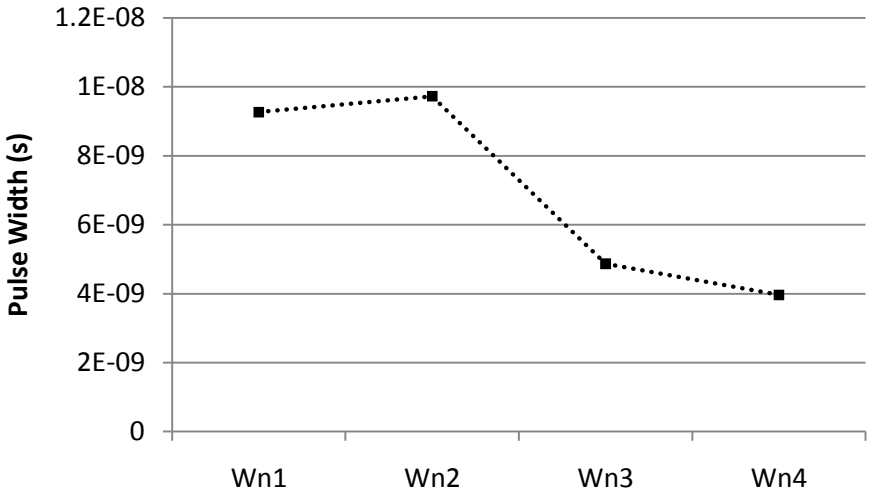


Figure 6.8 (c): 40.5 MeV/(mg/cm^2) ion – Pulse Width (s)

The effectiveness of folding in the reduction of the effect caused by the ions presented before was clear in all simulations. The pulse amplitude peak and the pulse width were measured in folded devices and the transistor folding had shown to be efficient in making the devices more tolerant to soft errors.

Notice that there is a particularity at the results for the Wn2 device. The Wn1 is a device without partition and Wn2 is the first device folded. In this device the drain region is reduced but this region is used for both transistors instead of 2 drain regions. After the simulations it was noticed that these could be done in another way changing the drain region to become source and put both sources to become two drain regions. With this modification there will be two drain regions, one helping with the recovery of the other, as it happens when the device receive more partitions.

6.3 Transistor Folding Conclusion

The transistor folding technique was evaluated for a 90nm technology and results show that the technique enhances circuit tolerance to soft errors due its contribution to reduce junction area of the device.

The use of transistor folding to size a device had shown that it is effective in mitigating errors for both alpha particles and heavy ions profile. When the folding was executed without sizing the device the technique also show it effectiveness reducing the effect of low and high energy particles.

7 CONCLUSIONS

In this work a 90 nm MOSFET transistor (n-type) was modeled and compared with data extracted from predictive models. The model behavior was compared with PTM electrical model showing an agreement with the modeled device.

The analysis of the transistor sizing technique has shown that the technique should not be used when the main particles of the environment are heavy ions. When the technique was exposed to alpha particle profile (1.31MeV/(mg/cm^2)) it has shown to be able to reduce the effect of the particle. It was also verified that both sizing methodologies (symmetric an asymmetric) have similar results with the asymmetric been less effective to reduce soft errors.

The results of ionization for transistor sizing contradict the basic idea that the increase of the width of the transistor is enough to deal with ion particles. This occurs due to the lack of physical models when the technique was evaluated at electric level by others works. Other works also noticed the behavior observed in this work but their correlation and verification with the transistor sizing technique for the best of our knowledge was never done before.

Besides transistor sizing, the folding technique was also evaluated for SET robustness. The folding approach, which consists in the partition of a transistor, has shown to be efficient to mitigate soft error. The technique reduces the junction area allowing a smaller junction collection during the ionization.

It was also verified that the combination of transistor sizing and folding may be an alternative to the application of the idea of increasing the node collected charge since the transistor is increased and spitted avoiding the increase of the junction area.

The first conclusion of this work is that the transistor sizing technique alone is not suitable to protect integrated circuits against radiation effects due the necessary increase of the junction area which allows higher collection of charge during ionization.

The second conclusion is that the transistor folding allows the reduction of the junction area, which contributes to a lower collected charge. The transistor folding study to cope with soft errors for the best of our knowledge was never done before.

The final conclusion is that the combination of both techniques (sizing and folding) allows the reduction of soft error due the evident increase of the critical charge (sizing) and the split of the transistors (folding) that will avoid the increase of the junction area.

As future works there are the studies of soft errors effects in transistor like: silicon-in-insulator (SOI) and FinFET transistor. There is also the study of techniques to

prevent multiple collected charges which maybe the concern for the next generation integrated circuits.

REFERENCES

AGARWAL, K.; NASSIF, S. Statistical Analysis of SRAM Cell Stability. **ACM/IEEE Design Automation Conference,** [S.l.:s.n], Sep. 2006.

ANDERSON, T. et al. Software Fault Tolerance: An Evaluation. **IEEE TRANSACTIONS ON SOFTWARE ENGINEERING,** [S.l.:s.n], v.11, n.12, Dec. 1985.

ANELLI, G.M. **Conception et Caracterisation de Circuits Integres Resistants Aux Radiations Pour Les Detecteurs De Particules Du LHC En Technologies CMOS Submicroniques Profondes**. 2000. Thesis (PhD in *Laboratoire Européen pour la Recherche Nucléaire - INSTITUT NATIONAL POLYTECHNIQUE DE GRENOBLE. Grenoble, France.*

ASU. Predictive Technology Model. **ASU - Nanoscale Integration and Modeling.** Arizona, [s.n], 2008, Available at: <http://www.eas.asu.edu/~ptm/>. Visited in Feb. 2008.

BAKER, T.J, NOMAND, E. Altitude and Latitude Variations in Avionics SEU and Atmospheric Neutron Flux. **IEEE TRANSACTIONS ON NUCLEAR SCIENCE**,[S.l.:s.n] vol.40, n.6, Dec. 1993.

BAUMANN, R. Radiation-Induced Soft Error in Advanced Semiconductor Technologies. **IEEE TRANSACTIONS ON DEVICE AND MATERIALS RELIABILITY.** [S.l.:s.n], v.5, n.3, Sep. 2005

BOUDENOT, J.C. Radiation Space Environment. **2nd International School on the Effects of Radiation on Embedded Systems for Space Applications.** Sevilla, Nov. 2006.

BOUDENOT, J.C. Radiation Space Environment. In: VELAZCO, R. FOUILLAT, P. REIS, R. (Ed.) **Radiation Effects on Embedded Systems.** Netherlands: Springer, 2007. P. 1-9.

CHEN, L. GINGRICH, M. Study of N-Channel MOSFETs With an Enclosed-Gate Layout in a 0.18 um CMOS Technology. **IEEE TRANSACTIONS ON NUCLEAR SCIENCE**,[S.l.:s.n], vol.52, no.4. Aug. 2005.

CHEN, W.; Cong, R.; Dai, K. **Two New Space-Time Triple Modular Redundancy Techniques for Improving Fault Tolerance of Computer Systems. 6th IEEE International Conference on Computer and Information Technology**, Seoul, Sep. 2006 .

CLARK, L.T.; MOHR, K.C. Reverse-body Biasing for Radiation-Hard by Design Logic Gates. **IEEE 45th Annual International Reliability Physics Symposium**, Phoenix, [s.n], 2007.

COCHRAN, D.J. et al. Recent Total Ionizing Dose Results and Displacement Damage for Candidate Spacecraft Electronics for NASA. **IEEE Radiation Effects Data Workshop**,[S.l.:s.n]. 2005.

DALHOUSIE University Department of Earth Sciences. **Source of the Primary Radiation.** Available at: <http://cnef.earthsciences.dal.ca> Visited in Nov. 2008.

DASGUPTA, S. **Trends in Single Event Pulse Width and Pulse Shapes in Deep Submicron CMOS.** 2007. Master Thesis (Electrical Engineering) - Graduate School of Vanderbilt University. Nashville, Tennessee - USA.

DHARCHOUDHURY, A.; KANG, S.M. Fast Timing Simulation of Transient Faults in Digital Circuits. **IEEE International Conference on Computer-Aided Design,** [S.l.:s.n], 1994.

DIMITRI, A. A.; IHSAN, D. J.; KEITH, J. M.; MILLER, S. Well-Tempered" Bulk-Si NMOSFET Device . **MIT-** ***Microsystems Technology Laboratory***. *[S.l.:s.n]*, 2008, Available at: <http://www-mtl.mit.edu/researchgroups/Well/>. Visisted in Jan. 2008.

DUSSEAU, L. Basic Mechanisms of Radiation Effects. 3nd International School on the Effects of Radiation on Embedded Systems for Space Applications. Buenos Aires, Nov. 2007.

DYER, C.S.; HOPKINSON, G.R. **Space Radiation Effects For Future Technologies and Missions.** [S.l.:s.n], Report Number TR010690/1.1. QINETIQ Space Departament and Sira Electro-Optics Ltd, 2006.

DYER, C.S.; SIMS, A.; UNDERWOOD, C. Measurements of the SEE Environment from Sea Level to GEO Using CREAM and CREDO Experiments. **IEEE TRANSACTIONS ON NUCLEAR SCIENCE.** [S.l.;s.n], vol.43, n.2, Apr. 1996.

ECOFFET, R. A Review of Some Space Anomalies Attributed to Radiation Effects on Electronic Devices. **3nd International School on the Effects of Radiation on Embedded Systems for Space Applications.** Buenos Aires, Nov. 2007.

FACCIO, F. Design Hardening Methodologies for ASICs. **2nd International School on the Effects of Radiation on Embedded Systems for Space Applications.** Sevilla, Nov. 2006.

FACCIO, F. Design Hardening Methodologies for ASICs. In: VELAZCO, R. FOUILLAT, P. REIS, R. (Ed.) **Radiation Effects on Embedded Systems.** Netherlands: Springer, 2007. P. 1-9.

FRIEND, S.; ADAMS, S. An Architecture for Modular Hardware and Software Fault Tolerance in Critical Real Time Appliacations. **IEEE Digital Avionics Systems Conference**. Seattle, 1992.

HASS, J.K.; GAMBLES, J.W**.** Single Event Transients in Deep Submicron CMOS. **IEEE Circuits and Systems 42nd Midwest Symposium on Circuit and Systems.** [S.l.:s.n], 1999.

HAZUCHA, P. et al. Neutron soft error rate measurements in a 90-nm CMOS process and scaling trends in SRAM from 0.25-um to 90-nm generation. **IEEE Electron Devices Meeting**. [S.l:s.n], 2003.

HER, T.W.; WONG, D.F. Cell Area Minimization by Transistor Folding. **IEEE Design Automation Conference**, [S.l.:s.n], 1993.

HU, C. Alpha-Particle-Induce Field and Enhanced Collection of Carriers. **IEEE ELECTRON DEVICE LETTERS,** [S.l.:s.n]. v.3, n.2, Feb. 1982.

HU. H. et al. A study of deep-submicron MOSFET scaling based on experiment and simulation. **IEEE TRANSACTIONS ON ELECTRON DEVICES,** [S.l.:s.n], p.669-677, 1995.

HYUNGSOON, S. Modeling of Alpha-Particle-Induced Soft Error Rate in DRAM. **IEEE TRANSACTIONS ON ELECTRON DEVICES**, [S.l.:s.n], v.46, n.9, Sep. 1999.

JOHNSTON, A. Scaling and Technology Issues for Soft Error Rates. **4Th Annual Research Conference on Reliability**, Stanford, Oct. 2000.

KARNIK, T.; HAZUCHA, P.; Patel, J. Characterization of Soft Errors Caused by Single Event Upsets in CMOS Process. **IEEE TRANSACTIONS ON DEPENDABLE AND SECURE COMPUTING.** [S.l.:s.n], v.1, n.2, Apr. 2004.

KASTENSMIDT, F.G.L. **Designing Single Event Upset Mitigation Techniques for Large SRAM-Based FPGA Components.** 2003. 137 f. Thesis (PhD in Computer Science) – Instituto de Informática, UFRGS, Porto Alegre

KASTENSMIDT, F.G.L.; CARRO, L.; REIS, R.A.L. **Fault-Tolerance Techniques for SRAM-Based FPGAs.** [S.l.], Springer, 2006.

KASTENSMIDT, F.L. REIS, R. Fault Tolerance in Programmable Circuits. In: VELAZCO, R. FOUILLAT, P. REIS, R. (Ed.) **Radiation Effects on Embedded Systems.** 1.ed.Netherlands: Springer, 2007. P. 1-9.

LANDSBERG, P.T.; RHYS-ROBERTS, C.; LAL, P. Auger Recombination and impact ionization involving traps in semiconductors. **Proceedings Physical Society**, [S.l.:s.n], v.84, 1964.

LAZZARI, C. ASSIS, T.R.; KASTENSMIDT, F.G.L.; WIRTH, G.; ANGHEL, L.; REIS, R.A.L. An Analysis and Design Tool to Reduce SET Sensitivity in Integrated Circuits. **IEEE European Test Symposium**, Lago Maggiore, [s.n], 2008b.

LAZZARI, C. ASSIS, T.R.; KASTENSMIDT, F.G.L.; WIRTH, G.; REIS, R.A.L.; ANGHEL, L. An Analysis and Design Technique to Reduce SET Sensitivity in Combinational Integrated Circuits. **16th IFIP/IEEE International Conference on VLSI-Soc**, Greece, [s.n], 2008a.

LAZZARI, C.; ASSIS, T.R.; KASTENSMIDT, F.G.L.; ANGHEL, L.; REIS, R. Efficient Transistor Sizing for Soft Error Protection in Combinational Logic Circuits. **IEEE DECIDE Proceedings**, Buenos Aires,[s.n], 2007.

LERAY, J. BAGGIO, J. Atmospheric Neutron Effects in Advanced Microelectronics, Standards and Applications. **IEEE International Conference on Integrated Circuit Design and Technology.**[S.l.:s.n], 2004.

LIU, T.; et al. Total Ionization Dose Effect Studies of a 0.25um Silicon-On-Sapphire CMOS Technology. **9th European Conference Radiation and Its Effects on Components and Systems.** Deauville, [s.n]. Sep. 2007

LUNDSTROM, M. **Fundamentals of Carrier Transport.** 1ed. Cambridge, Cambridge University Press, Nov. 2000.

MESSENGER, G.C. Collection of charge on junction nodes from ion tracks. **IEEE TRANSACTIONS ON NUCLEAR SCIENCE.** [S.l.:s.n], 1982.

NASA. CREAM: Cosmic Ray Energetics and Mass. **NASA**. [S.l.:s.n], Nov. 2008a, Available at:<http://cosmicray.umd.edu/cream> Visited in Nov. 2008.

NASA. NOAA/Space Weather Prediction Center. **NASA**. [S.l.:s.n], Nov 2008b, Available at:<http://www.swpc.noaa.gov> Visited in Nov. 2008.

NASA. The NASA ASIC Guide: Assuring ASICS for Space. Draft 0.6 Jet Propulsion Laboratory. **NASA**. California, 1993, Available at: <http://parts.jpl.nasa.gov>. Visited in Nov 2008.

NASEER, R. et. al. Critical Charge Characterization for Soft ERROR Rate Modeling in 90nm SRAM. **IEEE International Symposium on Circuits and System**, [S.l.:s.n], 2007.

OLDIGES, P. et. al. Theoretical Determination of the Temporal and Spatial Structure of Alpha Particle Induced Electron-Hole Pair Generation in Silicon. **IEEE TRANSACTIONS ON NUCLEAR SCIENCE**, [S.l.:s.n], v.47, n.6, Dec. 2000.

ZHOU, Q.; MOHANRAM, K. Cost-Effective Radiation Hardening Technique for Combinational Logic. **ICCAD**, [S.l:s.n], Nov. 2004

RABAEY, J.M.; CHANDRAKASAN, A.; NIKOLIC, B. **Digital Integrated Circuits.** 2.ed. [S.l.], Prentice Hall, 2003.

REIS, R.A.L. **Concepção de Circuitos Integrados.** 2.ed. Porto Alegre. Sagra Luzzatto, 2002.

ROCHE, F.M.; SALAGER, L. CMOS Inverter Design-Hardened to the Total Dose Effect. **IEEE TRANSACTIONS ON NUCLEAR SCIENCE**,[S.l.:s.n], v.43, n.6, Dec. 1996.

RUI, C. WEI, C. Fang, L. Kui, D**.** Modified Triple Modular Redundancy Structure based on Asynchronous Circuit Technique. **IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems**, Washington, Oct. 2006.

SCHOCKLEY, W.; READ, W.T.J. Statistics of the Recombinations of Holes and Electrons. **IEEE Physical Review.** [S.l.:s.n], v.87, n.5, 1952

SCHRIMPF, R. D. Radiation Effects in Microelectronics. In: VELAZCO, R. FOUILLAT, P. REIS, R. (Ed.) **Radiation Effects on Embedded Systems.** Netherlands: Springer, 2007. P. 11-29.

SCHRIMPF, R.D. Radiation Effects in Microelectronics. . **2nd International School on the Effects of Radiation on Embedded Systems for Space Applications.** Sevilla, Nov. 2006.

SEDS. The SUN. **Students For The Exploration And Development of Space**. 2007. Available at: <http://seds.lpl.arizona.edu/nineplanets/sun.html>. Visited at: Nov. 2007.

SLOTBOOM, J.W.; GRAAFF, H.C. Bandgap Narrowing in silicon bipolar transistors. **IEEE TRANSACTIONS on Electron Devices.** [S.l.:s.n], v.24, n.8, Aug. 1977

SRINIVASAN, R.; BHAT, N. Impact of Channel Engineering on Unity Gain Frequency and Noise-Figure in 90nm NMOS Transistors for RF Applications. **18th International Conference on VLSI Design.**[S.l.:s.n], 2005.

SROUR, J.R.; MARSHALL, C.J. MARSHALL, P.W. Review of Displacement Damage Effects in Silicon Devices. **IEEE TRANSACTIONS ON NUCLEAR SCIENCE.** [S.l.:n.s], vol.50, n.3, Jun. 2003.

ST**. ST Microelectronics - HCMOS9_GP Design Rules Manual 013 MICRON CMOS PROCESS.** [S.l.:s.n], Apr. 2002.

SYNOPSYS**. SYNOPSYS – Taurus Medici Davinci – User Guide.** [S.l.:s.n], Jun. 2006.

STAPOR, W. J.; MCDONALD, P. T. Pratical approach to ion track energy distribution. **Journal Applied Physic.**[S.l.:s.n], Jun. 1988.

TANG, H. H. *SEMM-2: A new generation of single-event-effect modelling tool. **IBM Research,** [S.l.:s.n]*, Feb. 2008. Available at: <http://www.research.ibm.com/ journal/rd/523/tang.html>. Visisted in Feb. 2008.

TEODORESCU, H. M. Types of Radiation in Space. **NASA Space Settlement Contest.** [S.l:s.n], 2005. Available at: <http:// http://www.nss.org/settlement/nasa /Contest/Results/2005/TEMIS/Cover.htm>. Access at: dez. 2008.

TIAN, H. et al. An Evaluation of Super-Steep-Retrograde Channel Doping for Deep-Submicron MOSFET Applications. **IEEE TRANSACTIONS ON ELECTRON DEVICES**,[S.l.:s.n], v.41, n.10, Oct. 1994.

TRIPATHI, R.K; WILSON, J.W; YOUNG, R.C.; Electrostatic Active Radiation Shielding – Revisited. **IEEE AEROSPACE CONFERENCE**, Montana, [s.n], 2006.

TSIVIDIS, Y. **Operation and Modeling of The MOS Transistor.** 2ed. New York: Oxford University Press, 1999, 620 p.

WIRTH, G.I.; VIEIRA, M.G.; KASTENSMIDT, F.G.L. Accurate and computer efficient modeling of single event transients in CMOS circuits. **IEEE IET Circuits Devices Systems**.[S.l.:s.n], v.1, N.2, Apr. 2007a.

WIRTH, G.I.; VIEIRA, M.G.; NETO, E.H.; KASTENSMIDT. F.G.L. Modeling the sensitivity of CMOS circuits to radiation induced single event transients. **Microelectronic Reliability.** [S.l], Elsevier, v.48, n.1, p.29-36, Jan. 2007b.

YAVORSKY. B.; DETLAF, A. ***A. Handbook of Physics***. Moscow, MIR Publishers. 1972. p. 964.

ZHAO, W;. CAO. W. Predictive technology model for nano-CMOS design exploration. **ACM Journal on Emerging Technologies in Computing Systems.** [S.l:s.n], v.8, Apr. 2007.

ZHOU, Q.; MOHANRAM, K. Gate Sizing to Radiation Harden Combinational Logic. **IEEE TRANSACTIONS ON COMPUTER-AIDED DESIGN OF INTEGRATED CIRCUITS AND SYSTEMS**. [S.l.:s.n], v.25, n.1, Jan. 2006.

ZIEGLER, J.F. PUCHNER, H. **SER History, Trends and Challenges: A Guide for Designing with Memory ICs.** San Jose: Cypress Semiconductor Corporation, 2004.

ZIEGLER, J.F.; BIERSACK, J.P,; ZIEGLER, M.D. SRIM 2008. **The Stopping and Range of Ions in Matter.** Morrisville, December 2008. Available at: <http://www.srim.org>. Visited at: Dez 2008.

APPENDIX RADIAL DISTRIBUTION OF CARRIERS

1. Introduction

During simulations the radial distribution of electron-hole pairs generated by ions is scaled from 25nm to 300 nm to evaluate its effectiveness to cope with single event effect. Results show SEE pulses width variations ranging from 20.5ps to 1.28ns for heavy ions. The measured SEE pulse peak presents variations of about 1.2V for high LET ions. For alpha particles the same behavior of heavy ions is noticed but with a lower magnitude. These results indicates the necessity of evaluate not only the Linear Energy Transfer to the ion during ionization tests but also the spatial distribution of carriers during the ionization to achieve a better characterization of the soft error pulse.

2. Simulation Details

The used ions are shown in table 1.

Table 1- Ion profile

Ion	Energy MeV	LET (dE/dX) MeV/(mg/cm^2)
Alpha particle (He)	1	1.31
Heavy Ion (Co)	20	22,07

The radial distributions used to ionization simulations are presented at table 2.

Table 2- Radial Distribution of e-h pairs

	Radial Distribution (nm)
R1	25
R2	50
R3	100
R4	150
R5	200
R6	250
R7	300

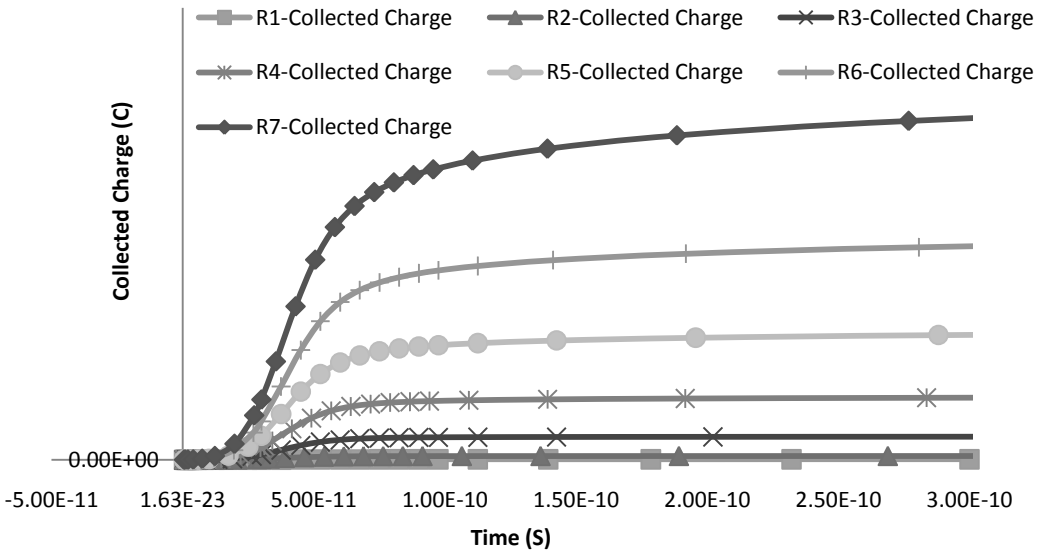
All ionization simulations were taken using the following physical models

- Shockley-Read-Hall Model - SRH
- Auger Recombination Model - AUGER
- Carrier-Carrier Scattering Mobility Model - CCSMOB
- Bang-Gap Narrowing Model - BGN

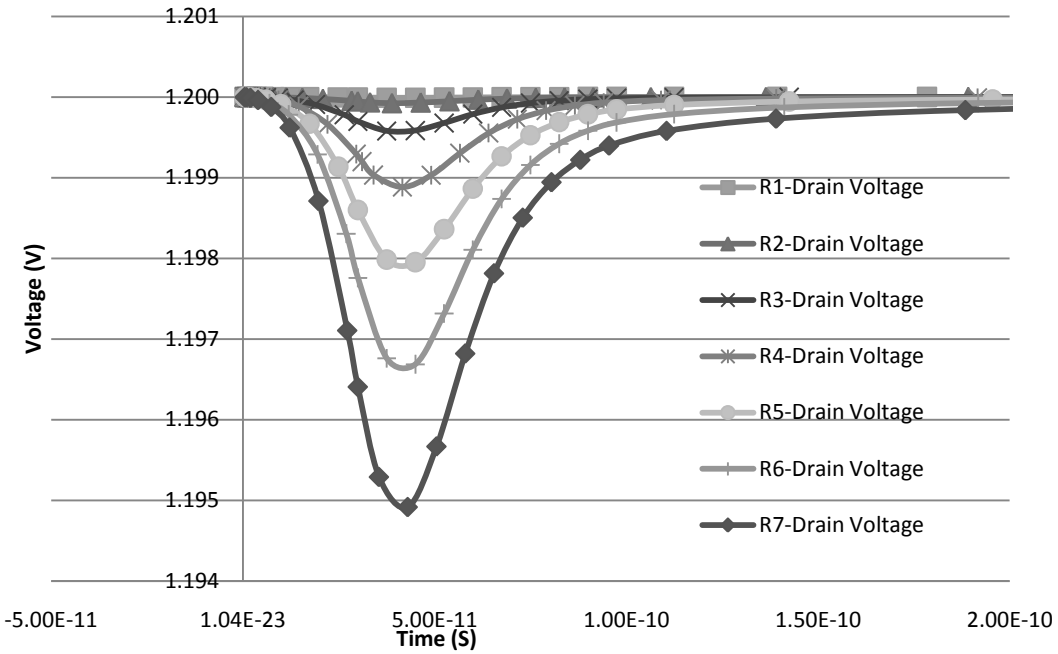
Recombination models where presented in chapter 4 section 2. In this work all impact ionizations use an impact vector of 90º hitting the device at the center of the drain, as shown in figure1.

3. Simulation Results of Ionizations

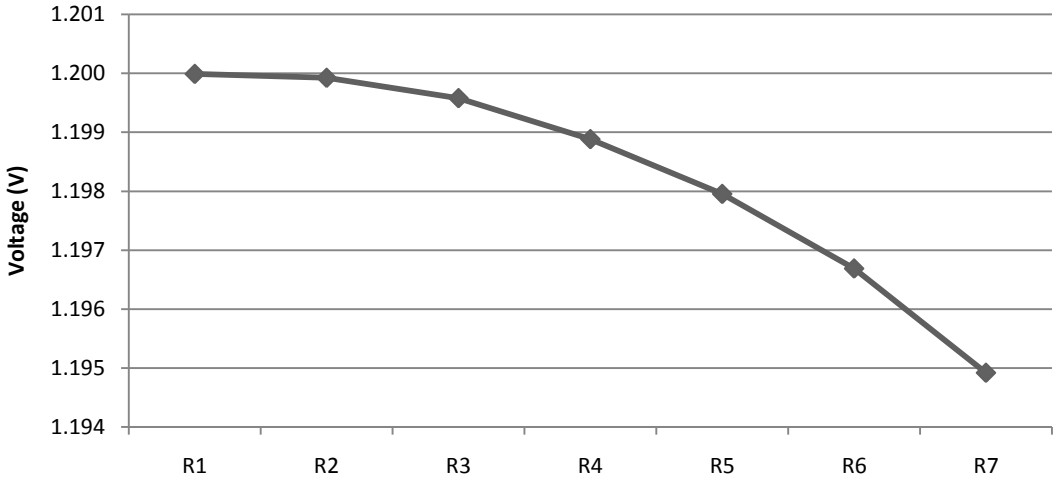
Using the LET of 1.31 MeV/(mg/cm^2) for alpha particles, simulations with the radial distributions of e-h pairs of table 2 were conducted. In figure 1a the collected charge of the SEE is presented. It were measured collected charges ranging from 10^{-18} Coulombs to 25 nm radial distribution to some 10^{-15} Coulombs for 300 nm radial distribution. The increase of the distribution allows a higher collection of charges by the device. In figure1b the SEE pulse is shown, the amplitude of the pulse ranged from 1.2 V to 1.19 V as shown in figure 1c. Notice that a low LET of 1.31MeV/(mg/cm^2) was not able to cause a Single Event Transient (SET) but the behavior of the SEE with the increase of the radial distribution is noticed.



a)- SET Collected Charge



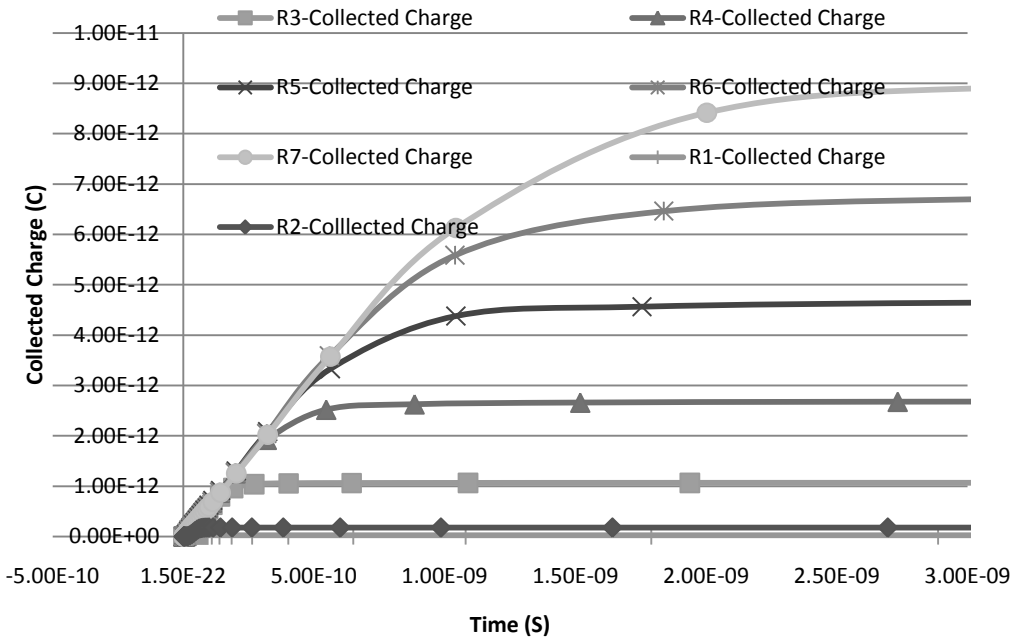
b)- SET PULSE



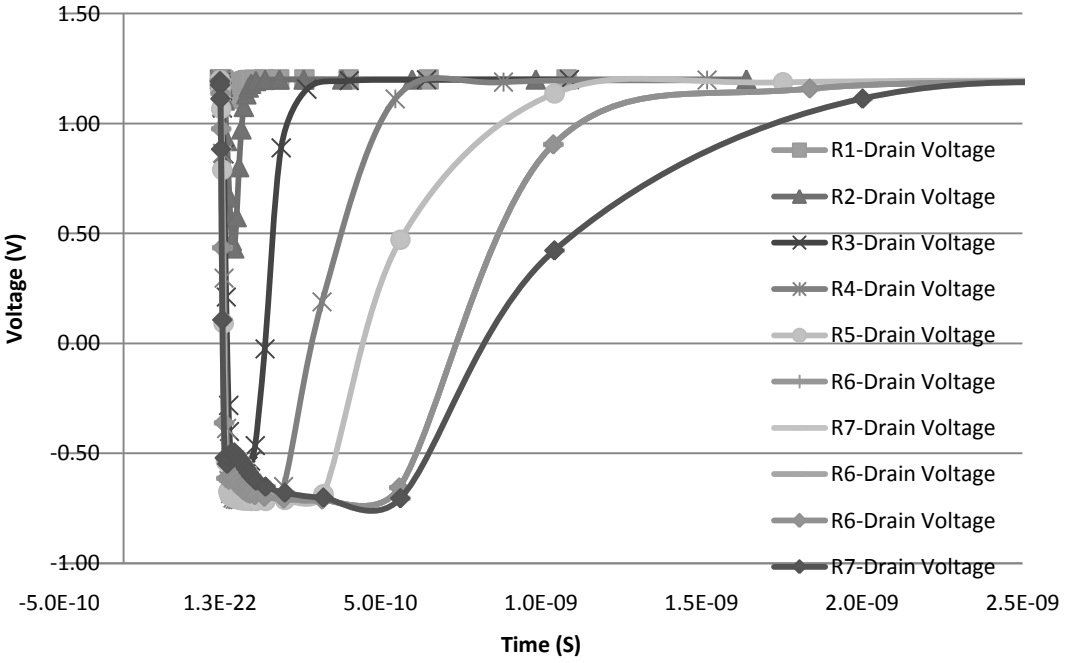
c)- SET Pulse Peak behavior

Fig 1- Simulations with alpha particle. LET= 1.31 MeV/(mg/cm^2)

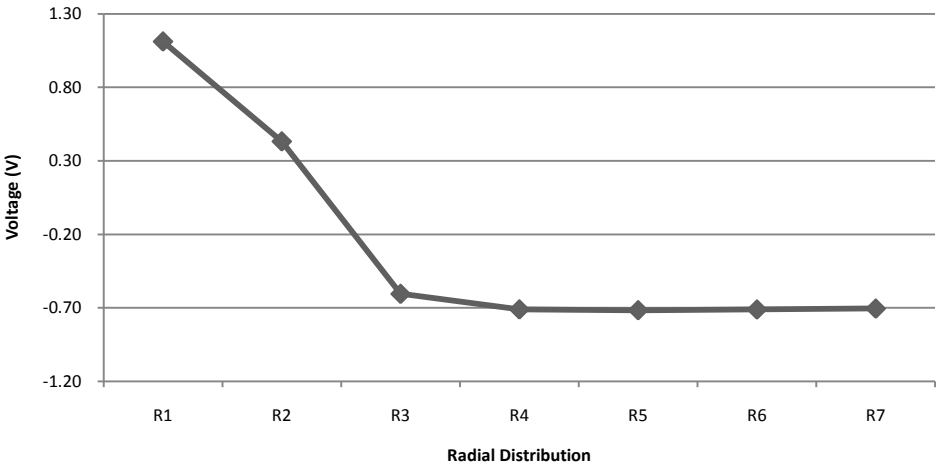
The evaluation was also done with a LET of a heavy ion using a Co ion with LET of about 26.5 MeV/(mg/cm^2). For the collected charge of figure 2a the same behavior seen for alpha particle is noticed. The increase of the radial distribution allows an increase of collection of charge by the device ranging from 10^{-15} Coulombs to 10^{-12} Coulombs. The SEE pulse in this case was able to generate a SET. In figure 2b and 2c the variation of the pulse. The SET pulse peak had shown variations ranging from 1.1 V for radial distribution of 25 nm to -0.7 V for radial distribution of 300nm. For R=25nm no SET was generated.



a) - SET PULSE



b)- SET Collected Charge



c)- SET Pulse Peak

Fig 2- Simulations with heavy ion. LET= 26.5 MeV/(mg/cm^2)

The pulse width had shows an increasing range from 20pS to 1.2ns as seen in figure 3. As indicated before for very low radial distributions of 25nm the heavy ion was not able to generate a SET. This shows the limitated effect that small spatial distributions can cause to devices.

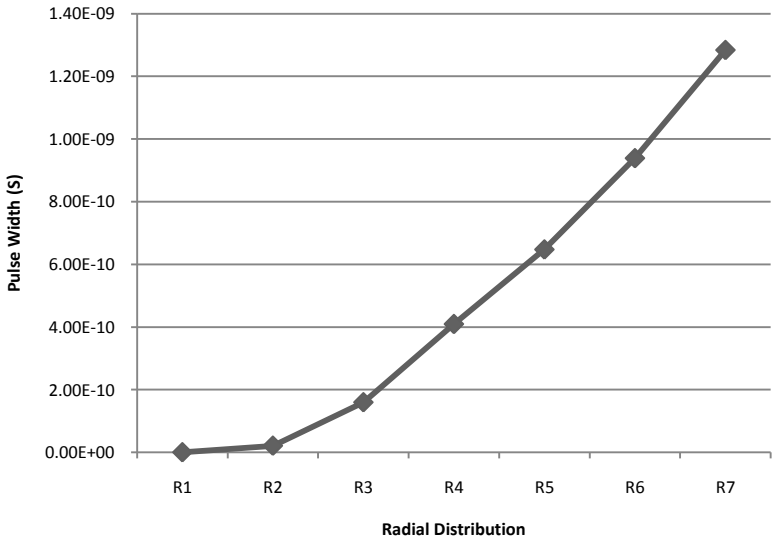


Fig. 3- SET Pulse Width

For both LET profile the same behavior with the increase of the radial distribution was noticed. The increase of the spatial distribution of carriers reduce the density of carriers allowing a reduction of the recombination rate as exposed by recombination models SRH and AUGER at section 4.2.

4.Conclusions

Radial distribution is an important parameter for soft errors simulations. Results show that increasing the radial distribution of electron-hole pairs allows a higher collection of charge by devices resulting in an increase of the SEE pulse amplitude peak and width.

Recombination models show the importance of spatial distribution (density) of carriers. With small radial distributions, high density of e-h pairs allows high rates of recombination which reduce the collected charge. Using high radial distributions with high density of e-h pairs the recombination rate is reduced allowing more charge to be collected by the device.

The LET can be suppressed by small radial distributions, making this parameter an important one on the characterization of soft errors.

APPENDIX 2 – RESUMO

Análise da influência do dimensionamento e partição de transistores e na proteção de circuitos contra efeitos de radiação.

RESUMO

Este trabalho apresenta uma avaliação da eficiência do dimensionamento e particionamento (folding) de transistores para a eliminação ou redução de efeitos de radiação. Durante o trabalho foi construído um modelo de transistor tipo-n MOSFET para a tecnologia 90nm, utilizando modelos preditivos. O transistor 3D modelado foi comparado com o modelo de transistor elétrico PTM level 54 da Arizona State University e os resultados mostraram uma coerência entre os dispositivos. Este transistor modelado foi irradiado por uma série de partículas que caracterizam ambientes terrestres e espaciais. Foi descoberto que a técnica de redimensionamento de transistores tem sua eficiência relacionada ao tipo de partícula do ambiente e não é aplicável em ambientes com partículas com alta energia. Descobriu-se também que aplicando o particionamento de transistores é possível reduzir a amplitude e a duração de erros transientes. A combinação do dimensionamento e o particionamento de transistores pode ser utilizada para a redução de efeitos de radiação incluindo partículas leves e pesadas. Por fim um estudo de caso foi realizado com uma célula de memória estática de 6 transistores utilizando as técnicas mencionadas anteriormente. Os resultados da célula de memória indicaram que a combinação das duas técnicas pode de fato reduzir e até impedir a mudança do estado lógico armazenado na célula.

Palavras-chaves: Efeito de radiação, Evento de efeito único, Dimensionamento de transistores, Microeletrônica, Tolerância a falhas, Erros transientes.

1. Introdução

Circuitos Integrado (CI) é um dispositivo semicondutor composto de componentes elétricos como transistores, diodos e capacitâncias (REIS 2002). O principal componente de um CI é o transistor, um componente elétrico feito de camadas de

materiais semicondutores dopados com íons positivos e negativos. Estes CI's são utilizados para construir dispositivos que serão utilizados em televisores, aparelhos de celular, computadores, equipamentos médicos, aniônicos, instrumentos militares e muitos outros (RABAEY, 2003).

O constante uso de dispositivos eletrônicos com a miniaturização dos componentes para a escala nano métrica tornou um fenômeno comum em um perigo para a funcionalidade destes CI's. O que acontece é que constantemente o planeta Terra é bombardeado por partículas radioativas de diferentes fontes de radiação como raios cósmicos e o sol. A maior parte desta radiação é redirecionada pelo campo magnético terrestre ou filtrada pela atmosfera e a radiação restante que atinge as cidades possui pouca energia não sendo danosa aos seres humanos e animais. Porém estes níveis de energia são capazes de perturbar dispositivos eletrônicos como os CI's fazendo com que picos de tensão surjam e provoquem efeitos transientes ou até permanentes (BOUDENOT, 2007).

A constante miniaturização dos componentes traz problemas do ponto de vista de efeitos de radiação não apenas pela maior suscetibilidade dos componentes, mas também pela utilização de tensões de alimentação menores para os dispositivos. O trabalho de Hazucha, (2003) mostra o efeito da redução da tensão de alimentação em diferentes circuitos de testes que utilizam escalas de transistores diferentes como é visto na figura 1.1. Os testes usam chips com tecnologias 90nm, 0.13um, 0.18um e 0.25um. Os testes deixam claros que a utilização de tensões menores aumenta a taxa de erros transitórios, o que também é indicado pelo trabalho de (BAUMANN, 2005).

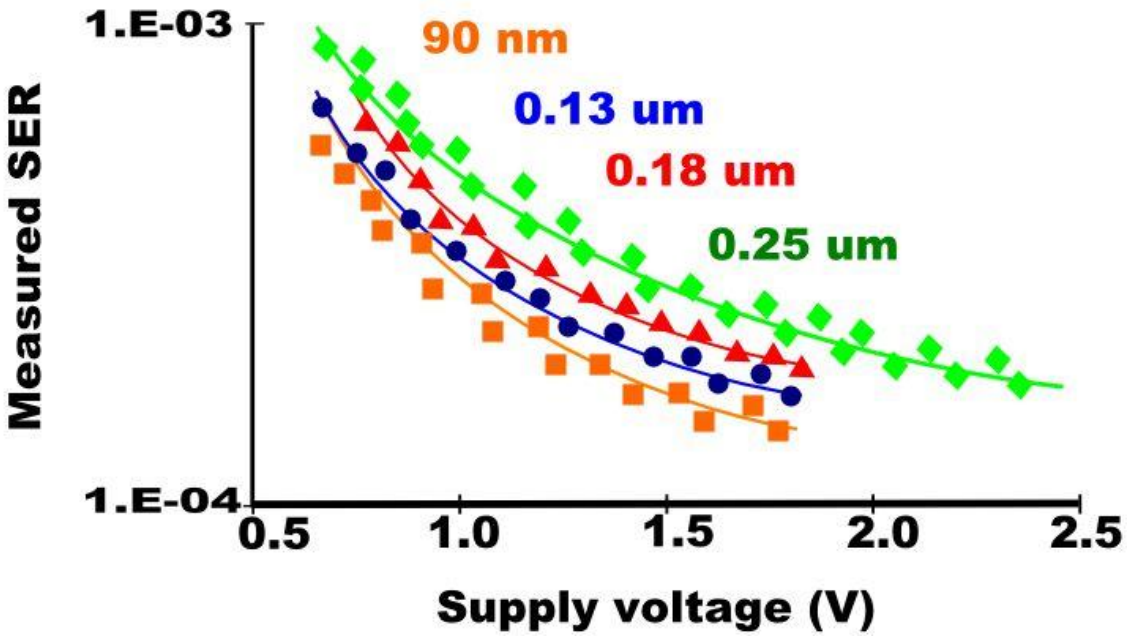


Figura 1.1: Taxa de Erros Transitórios no Diodo PMOS vs. Tensão de Alimentação (HAZUCHA,2003)

Com isto apresentamos a motivação deste trabalho, a necessidade de avaliar efeitos transientes em tecnologia nano métricas. A análise de duas técnicas de redução de transientes serão avaliadas: redimensionamento e partição de transistores. A técnica de redimensionamento de transistores foi proposta por (ZHOU, 2006) e não foi avaliada

em nível de dispositivo, tendo o autor focado em uma análise em nível elétrico. A técnica de partição de transistores é utilizada em nível de leiaute para conferir regularidade no design de células e nunca teve o impacto analisado do ponto de vista de efeitos de radiação transitório.

O importante a ser destacado é que estas técnicas vão ser analisadas em nível de dispositivo o que possibilita uma análise mais realista quando comparada a análise em nível elétrico.

2. Modelagem do Dispositivo

Para as simulações em nível de dispositivo foi utilizada a ferramenta de TCAD, Davinci da Synopsys. A ferramenta permite a criação do dispositivo semicondutor e a simulação de efeitos transitórios de radiação a partir da injeção de pares elétrons-lacunas diretamente no semicondutor. Neste trabalho os efeitos de radiação são avaliados em um transistor do tipo-n MOSFET em uma tecnologia preditiva 90nm. Em simulações que exigem um transistor tipo-p, a ferramenta Davinci foi configurada para operar em modo misto, podendo utilizar um modelo elétrico para simular o transistor tipo-p conectado com o transistor em modelo dispositivo do tipo-n. Na figura 2.1 é mostrado o símbolo de um transistor NMOS.

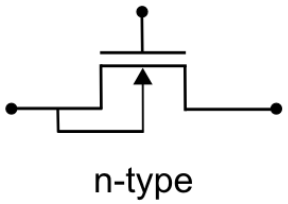


Figura 2.1: Símbolo do transistor NMOS

O dispositivo modelado foi baseado em dados extraídos de um modelo do Microsystems Technology Laboratory do MIT (DIMITRI, 2008) e para auxiliar nos dados de dopagem foram obtidas informações do trabalho de (HU, 1995) baseados na topologia mostrada na figura 2.2. O modelo mostrado na figura é um transistor NMOSFET usando as técnicas dopagem de canal Super Steep Retrograde (SSR), source/drain halo e a técnica Light Doped Drain (LDD).

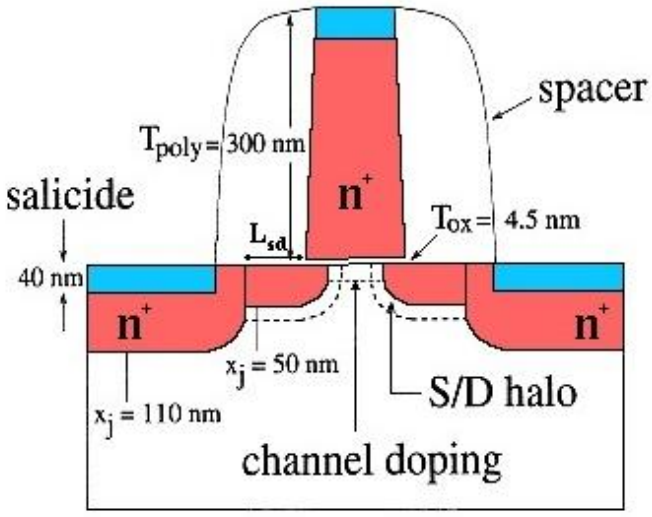


Figura 2.2: Dispositivo NMOSFET (DIMITRI, 2008)

O dispositivo modelado com estas informações é mostrado na figura 2.3.

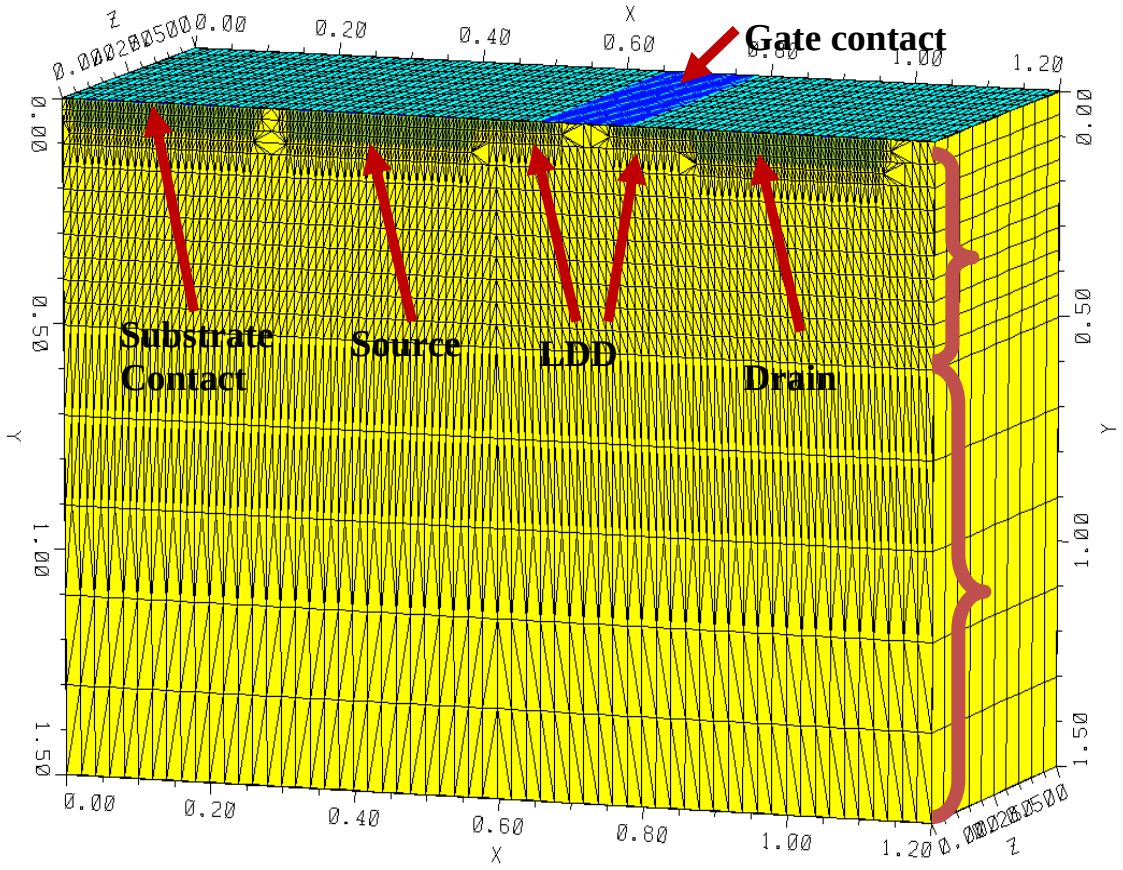


Figura 2.3: Dispositivo NMOS 90nm modelado

Informações da dopagem e da geometria do dispositivo são mostradas na tabela 2.1. Observe que o dimensionamento é baseado no trabalho de (DASGUPTA, 2007) e (DIMITRI, 2008).

Tabela 2.1: Dimensão e perfil de dopagem

Region	Width (x)	Width(y)	Width (z)	Doping
LDD	*115 nm*	*30 nm*	*240 nm*	*n-type. Peak: 1e19*
Source\Drain	*240 nm*	*60 nm*	*240 nm*	*n-type. Peak:1e20*
SSR	*90 nm*	*5 nm*	*240 nm*	*n-type. Peak:1.5e18*
Gate	*136 nm*	*300 nm*	*240 nm*	*n-type. Peak:2e20*
Oxide	*136 nm*	*1.4 nm*	*240 nm*	*None*
Substrate	*0.9*	*1.5*	*0.3 um*	*p-type. Peak:5.5e18*

A dopagem da região ativa e da SSR possui distribuição gaussiana. A dopagem do substrato é uniforme. O threshold do dispositivo foi controlado com a SSR. A espessura do óxido não foi alterada para controlar a tensão de threshold, sendo esta dimensão igual ao valor utilizado por (DASGUPTA, 2007).

2.1 Simulações do MOSFET

Para validar o transistor modelado no Davinci simulações foram realizadas comparando o resultado de simulação do transistor com modelos preditivos 90nm DE (ZHAO, 2007) da Arizona State University (ASU, 2008).

Nas figuras 2.4 e 2.5 a tensão de alimentação do substrato e da fonte foram mantidas em 0V (V_S=V_B=0V). As figuras mostram a comparação da curva dos transistores em nível de dispositivo simulados no Davinci com a curva de transistores elétricos simulados no HSpice. A tensão de threshold também foi medida. Para o modelo em nível de dispositivo a tensão medida foi de V_T=0.31V. Foi verificado que transistores ST 90nm (ST, 2002) possuem threshold similar, tento o V_T=0.32V.

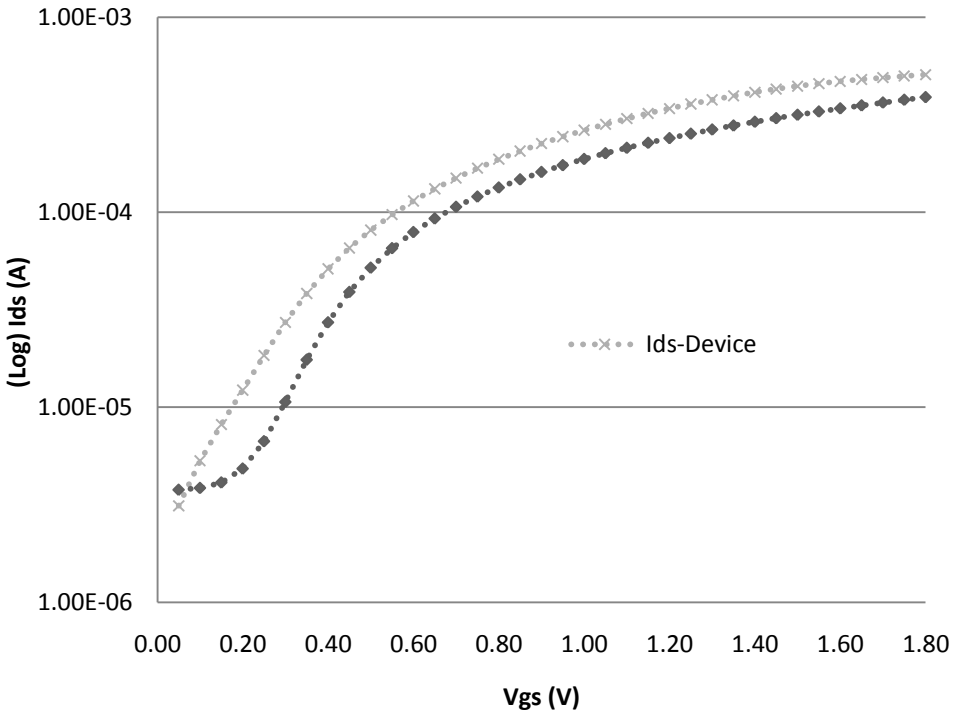


Figura 2.4: I_{DS} vs V_{GS} do modelo preditivo vs. modelo Davinci.

A figura 2.5 mostra a curva I_{DS} *vs* V_{DS}. O V_{GS} é fixado em 1.2 V e a tensão do dreno é variada. O resultado mostra comportamentos similares para ambos dispositivos.

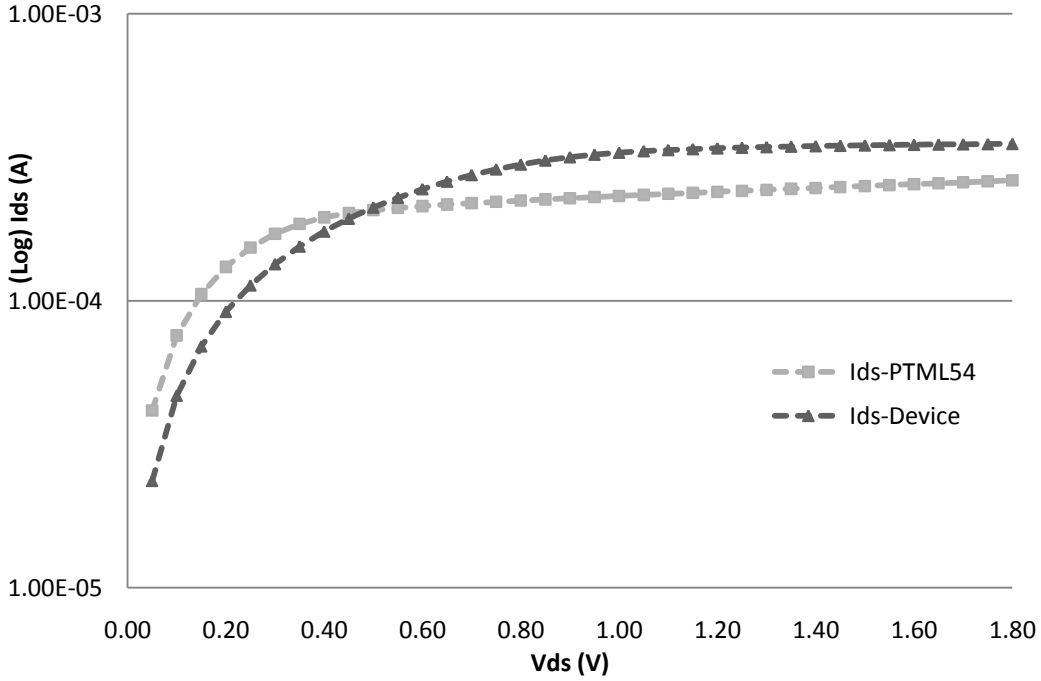


Figura 2.5: I_{DS} *vs* V_{DS} do modelo preditivo vs. modelo Davinci.

Com isto se valida o modelo utilizado e prossegue se para as simulações de erros transitórios.

3. Técnica de Redimensionamento de Transistores

A técnica de redimensionamento de transistores apresentada por (ZHOU, 2004) e posteriormente descrita em (ZHOU, 2006) em nível elétrico foi avaliada usando o modelo desenvolvido na ferramenta Davinci. Foram construídos modelos de simulação mista para portas lógicas convencionais baseadas nas figuras 3.1 (a),(b),(c) e (d), mostradas a seguir.

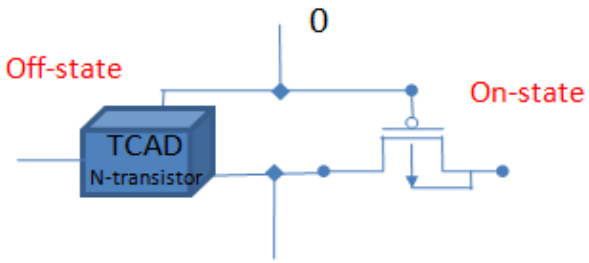


Figura 3.1 (a): Porta lógica NO, entrada:0, 3D NMOS em modo desligado.

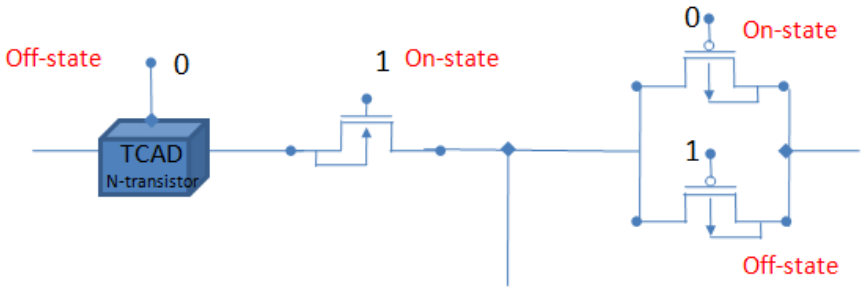


Figura 3.1 (b): Porta lógica NAND, entrada:10, 3D NMOS at em modo desligado

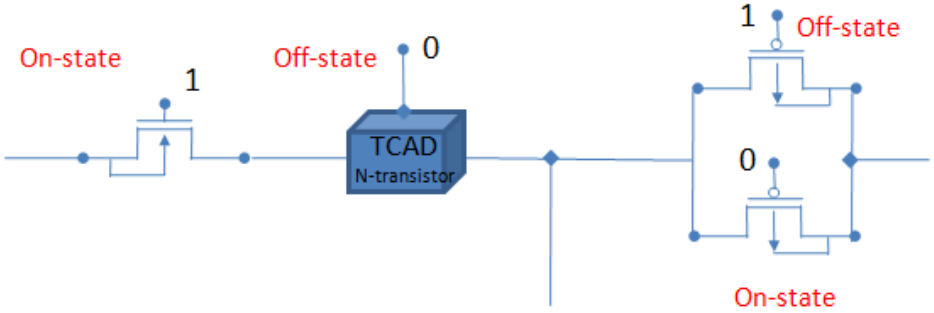


Figura 3.1 (c): Porta lógica NAND, entrada:01, 3D NMOS em modo desligado.

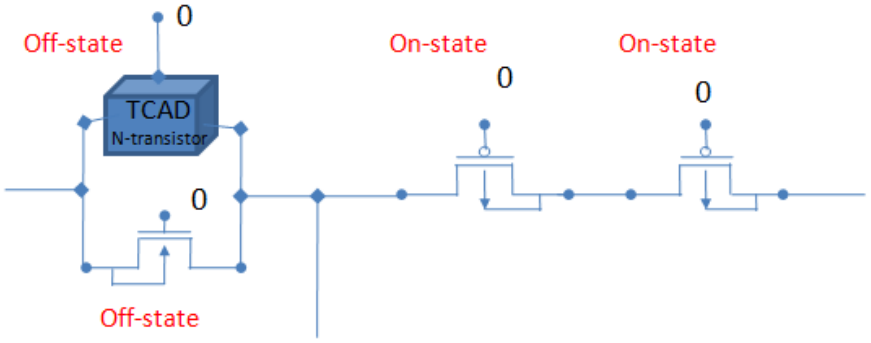


Figura 3.1 (d): Porta lógica NOR, entrada:00, 3D NMOS em modo desligado.

Uma capacitância de load de 10fF é adicionada na saída de cada célula.Este valor foi identificado como a média de capacitância de drive das células padrões da biblioteca ST 90nm. A largura dos transistores usada nas simulações é descrita nas tabelas 3.1 e 3.2.

Tabela 3.1: 3D NMOS Redimensionamento Assimétrico

Sizes	**NMOS transistor Wn(nm)**	**PMOS transistor Wp(nm)**
W0	220	880
W1	510	880
W2	1.020	880

Tabela 3.2: 3D NMOS Redimensionamento Simétrico

Sizes	**NMOS Wn(nm)**	**PMOS Wp(nm)**
W0	220	390
W1	510	880
W2	1.020	1.760
W2_3	2.040	3.508
W3	3.060	5.263
W4	4.080	7.017
W5	5.100	8.772

Para todas as simulações a tensão de saída dos dispositivos irradiados foi estimulada para o valor lógico “1” (VDD=1.2V). Uma vez que a irradiação ocorre, a tensão de saída pode cair, o que caracteriza a ocorrência de um efeito transitório. Caso a tensão caia além de VDD/2, esta irradiação é considerada um Efeito Transitório. Para avaliar também o efeito do redimensionamento de transistores na saída dos transistores irradiados, foi realizado o redimensionamento da capacitância de saída com os valores mostrados na tabela 3.3.

Tabela 3.3: Capacitância de saída.

Nome	Capacitância	Nome	Capacitância
C1	10f F	C6	500f F
C2	20f F	C7	1p F
C3	40f F	C8	10p F
C4	80f F	C9	20p F
C5	160f F		

Os íons utilizados nas simulações são indicados na tabela 3.4. Para nível terrestre foi utilizado um perfil de partícula alfa co aproximadamente 1 MeV/(mg/cm^2), para íons pesados foram usados LETs maiores que 20 MeV/(mg/cm^2).

Tabela 3.4: Perfil de íons utilizados.

Element / Energy	LET(dE/dX) MeV/(mg/cm^2)	Radial (r) μm
Alpha – 1 MeV	1.31	0.05
Cu, 395 MeV	26.5	0.5
Kr, 270 MeV	40.5	0.65

As simulações consideraram que os íons tiveram ângulo de impacto igual à 90º. Na figura 3.2 é mostrada uma imagem do impacto no dispositivo modelado

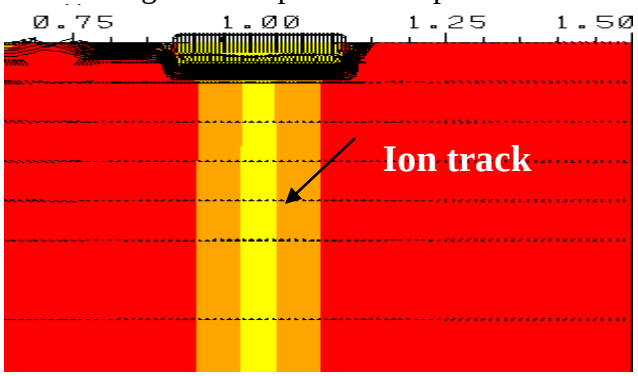


Figura 3.2: Transistor 3D NMOS durante ionização.

Baseado nestes dados os resultados das simulações são mostradas a seguir.

3.1. Resultados do Redimensionamento de Transistores

Apenas o resultado das simulações para a porta lógica NOT serão mostrados neste resumo uma vez que o comportamento não muda para as outras portas lógicas avaliadas.

Para partículas de baixo LET, com o perfil de partícula alfa temos os resultados a seguir. A avaliação da carga coletada mostra o aumento da carga coletada com o aumento dos transistores como é observado na figura 3.3 (a), porém observa-se que a amplitude do pico do transiente é reduzida na figura 3.3 (b). Isso mostra que o redimensionamento de transistores pode reduzir o efeito transiente de partículas de baixo LET.

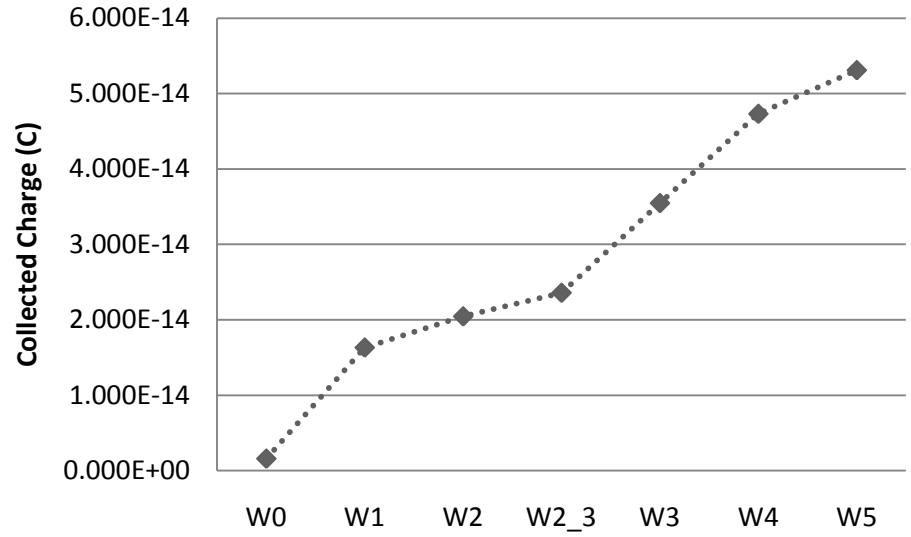


Figura 3.3 (a): Partícula Alfa-Porta NOT – Carga Coletada (C)

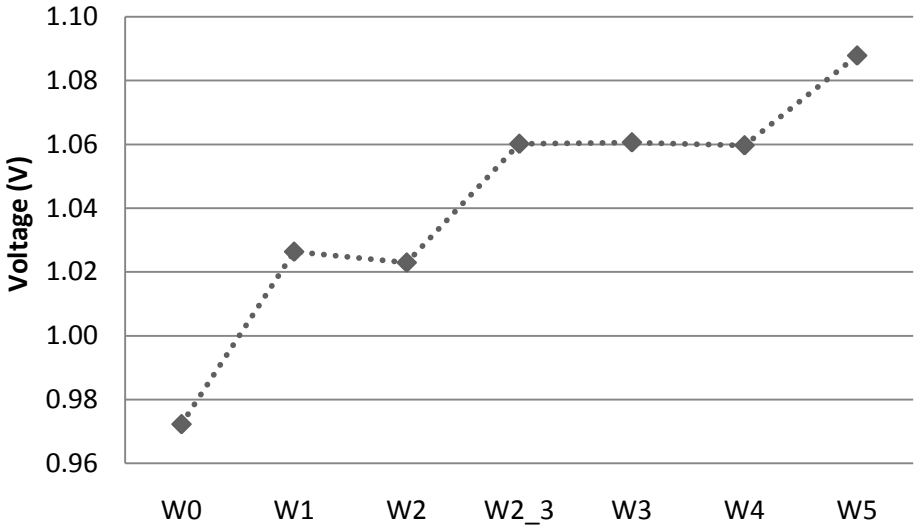


Figure 3.3 (b): Partícula Alfa-Porta NOT – Pico da Amplitude do Pulso (V)

O efeito do aumento da capacitância do transistor de saída é avaliado com o aumento da capacitância de saída. Os resultados mostram a redução do transiente como é identificado na figura 3.4. O transistor NMOS da simulação mostrada na figura possui Wn=3.060um e Wp=5.293um. O pico da tensão transiente vai de 1.06V para 1.13V com o aumento da capacitância de 10fC para 160fC. Este resultado reforça que o redimensionamento pode ajudar a reduzir o efeito transiente.

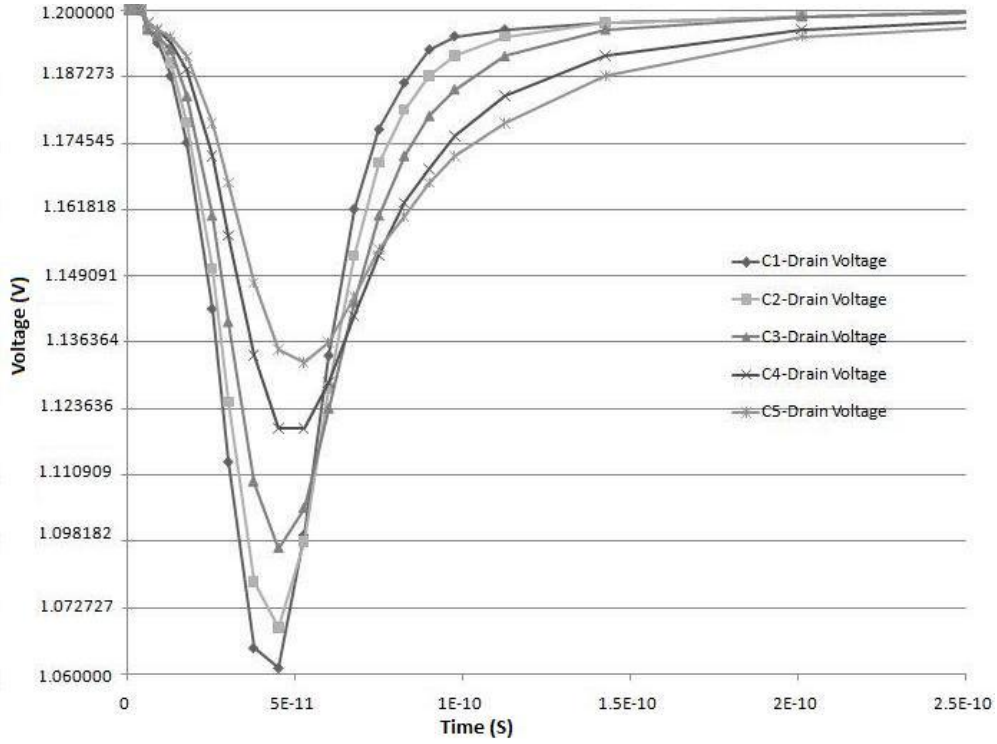


Figura 3.4: Partícula Alfa – Tensão transiente sobre diferentes capacitâncias.

As simulações também foram realizadas para partículas de alto LET, como íons pesados. Os resultados mostram um comportamento diferente indicando que o redimensionamento de transistores não é eficiente para partículas com alto nível de energia e terminam contribuindo para o aumento do efeito.

Íons de Kr e Cu foram injetados na porta NOT e seus resultados são mostrados nas figuras 3.5 (a), (b), (c) e (d). O primeiro parâmetro avaliado é a amplitude da tensão de pico. Observa-se pela figura 3.5 (a) e (b) para Cu e Kr respectivamente, que tanto para o redimensionamento simétrico como para assimétrico o redimensionamento fez com que a tensão de pico caísse, aumentando assim o efeito da radiação. Este resultado é o inverso ao encontrado para partícula de LET baixo.

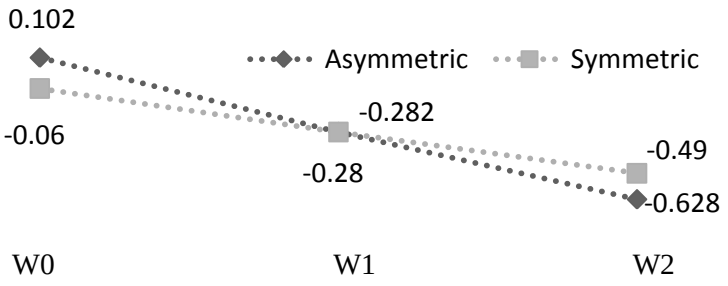


Figura 3.5 (a): Íon de Cu, Porta NOT, Pico de tensão do SET (V)

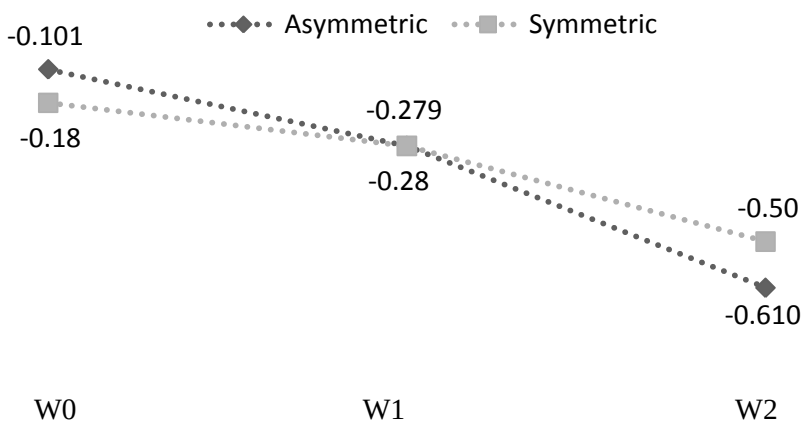


Figura 3.5 (b): Íon de Kr, Porta NOT, Pico de tensão do SET (V)

A carga coletada também foi avaliada para ambos os íons como é mostrada nas figuras 3.5 (c) e (d). Observa-se que para ambos os íons a carga coletada aumenta com o redimensionamento dos transistores.

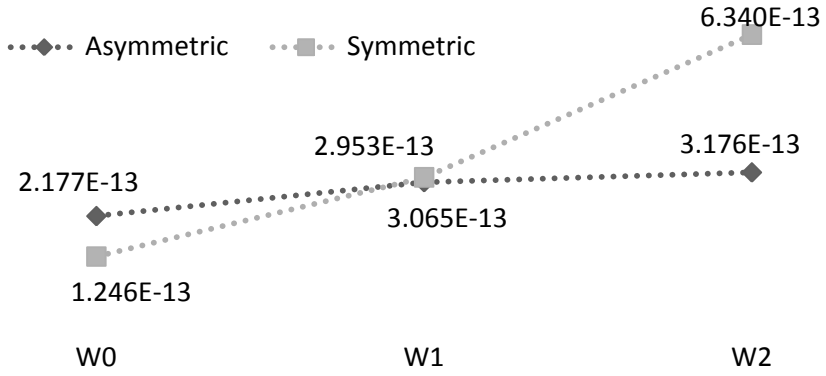


Figura 3.5 (c): Íon de Cu, Porta NOT, Carga Coletada (C)

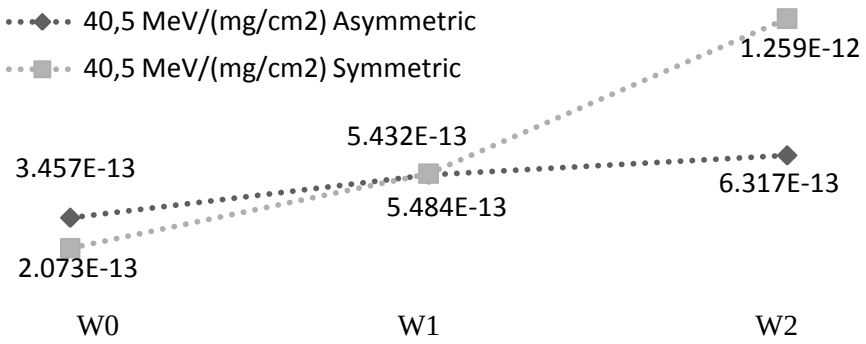


Figura 3.5 (d): Íon de Kr, Porta NOT, Carga Coletada(C)

3.2. Conclusão do Redimensionamento de Transistores

Com estes resultados podemos concluir que para partículas de baixo LET o redimensionamento de transistores pode reduzir o efeito do transiente. O que ocorre é que pequenos drenos de transistores coletam com facilidade a maior parte do LET gerado por partículas alfa devido ao baixo número de pares gerados nessa interação. Quando o LET é aumentado, muitos dos pares gerados não são coletados a tempo pelo dreno fazendo com que parte destes pares recombine. Porém para partículas de alto LET o aumento do dreno do transistor permite que parte dos elétrons-lacunas que não eram coletados pelo dreno sejam coletados com mais eficiência.

4. Técnica de Partição de Transistores

A técnica de redimensionamento de transistores é utilizada para reduzir o tamanho de transistores no intuito de dar regularidade as células permitindo uma melhor utilização da área do circuito (HER, 1993). Um exemplo simbólico da técnica de partição de transistores (folding) é mostrado na figura 4.1 onde duas portas NOT devem ser conectadas entre si.

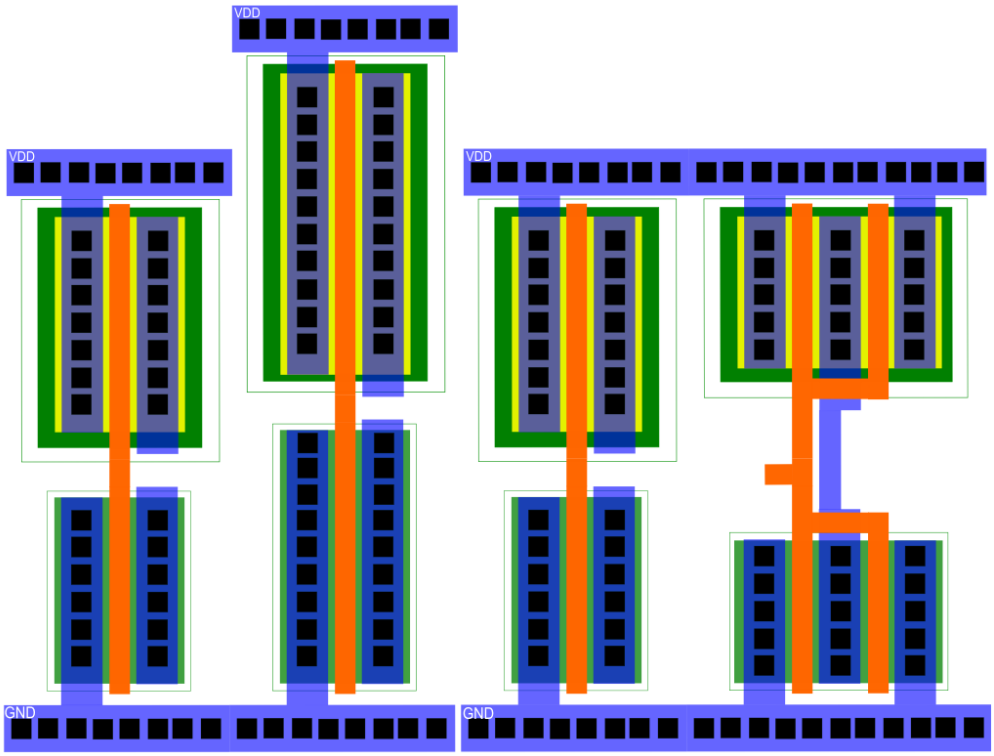


Figura 4.1: Leiaute não particionado e particionado.

Nesta sessão esta técnica é avaliada quanto a efeitos de radiação. A representação em nível de dispositivo desta técnica é mostrada na figura 4.2 para transistores tipo-n.

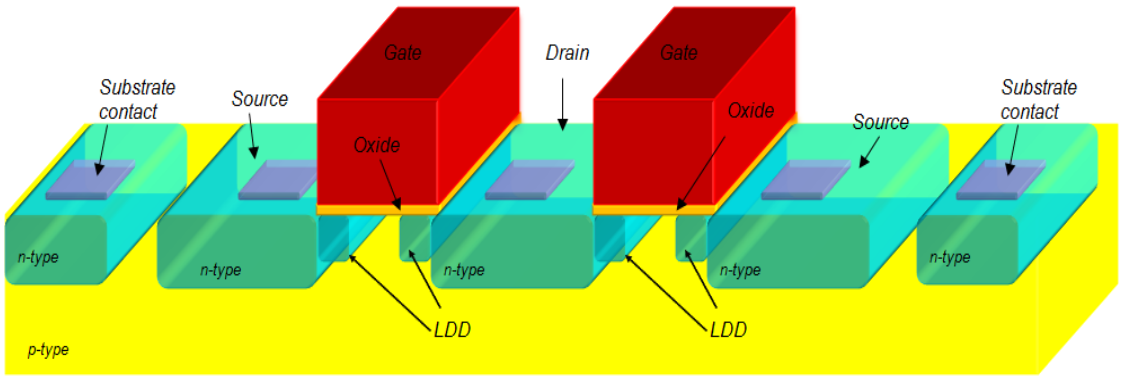


Figura 4.2: NMOS com particionamento

O importante a se notar é que com a partição de transistores podemos reduzir a área afetada pelo íon utilizando drenos pequenos sem perder a funcionalidade e as propriedades desejadas do transistor uma vez que transistores adicionais são inseridos em paralelo.

As tabelas a seguir caracterizam os dispositivos criados para as simulações. Transistores PMOS utilizados nas simulações são sempre modelos elétricos e a simulação no Davinci ocorre em modo misto. A seguir a tabela 4.1 com tamanho dos transistores.

Tabela 4.1: Transistor 3D NMOS

Sizes	PMOS Wp(um)	NMOS Wn(um)	Sizes Folding	PMOS Wp(um)	NMOS Wn(um)
W0	3.52	2.040	W0_S	2x1.760	2x1.020
W1	5.28	3.06	W1_S	3x1.760	3x1.020
W2	7.04	4.08	W2_S	4x1.760	4x1.020
W3	8.8	5.1	W3_S	5x1.760	5x1.020
W4	10.56	6.12	W4_S	6x1.760	6x1.020

Tabela com variação da taxa de particionamento mostrada a seguir.

Note que em todas as simulações a saída do dispositivo possui valor lógico "1" (VDD=1.2V). Uma vez o íon injetado, avalia-se a variação de 1.2V para valores inferiores, se o valor chegar a VDD/2 isso significa que temos o SET.

4.1. Resultados do Particionamento de Transistores

O primeiro perfil a ser analisado é o de partículas Alfa com LET de 1.31 MeV/(mg/cm^2) . Os resultados para particular alfa mostram comportamentos similares. Para a avaliação da amplitude do pico de tensão observamos a recuperação da tensão com o aumento do transistor e com as partições como é mostrado na figura 4.3 (a). Para a carga coletada observamos que o uso de partições permite que o a porta lógica aumente sem ter a carga coletada aumentada, uma vez que o tamanho do dreno não se modifica como se observa na figura 4.3 (b).

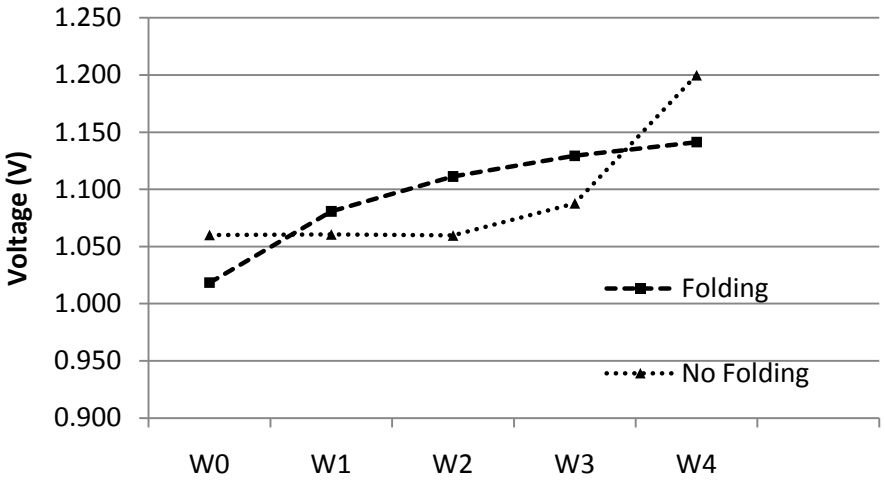


Figura 4.3 (a): Partícula Alfa, Pico da amplitude do SET (V)

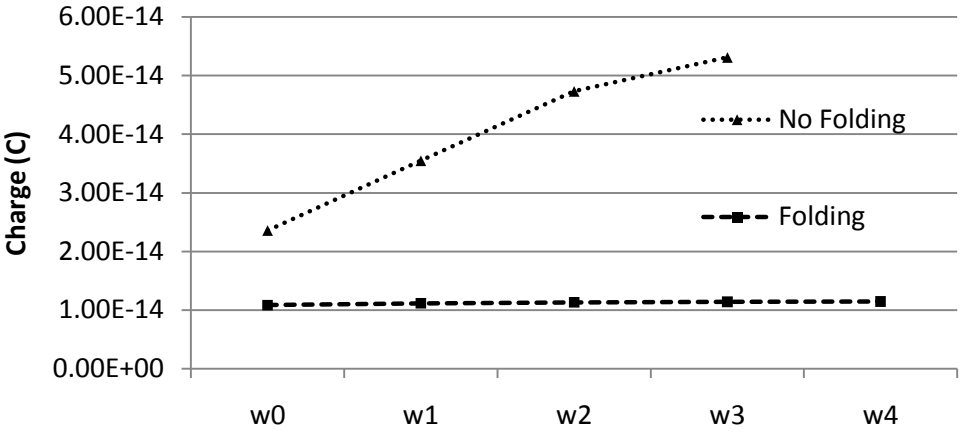


Figura 4.3 (b): Partícula Alfa, Carga Coletada (C)

Para partículas com alto nível de LET, encontramos resultados similares para Cu e Kr. Iremos resumir os resultados a seguir apenas para o íon de 26.5MeV/(mg/cm^2).

O comportamento do pico de tensão mostrado na figura 4.4 (a) mostra que o particionamento de transistor ajuda a reduzir a variação do pico de tensão quanto o aumento do transistor sem particionamento piora o efeito transiente.

A lagura do pulso também é melhorada como é mostrado na figura 4.4 (b). O particionamento de transistor junto com o aumento da porta permite que o pulso seja reduzido enquanto o aumento do transistor sem particionamento alonga o pulso tornando o efeito pior.

A carga coletada também é avaliada na figura 4.4 (c) que mostra um pequeno aumento na carga coletada da porta lógica com particionamento e uma piora significativa na porta lógica com redimensionamento sem particionamento.

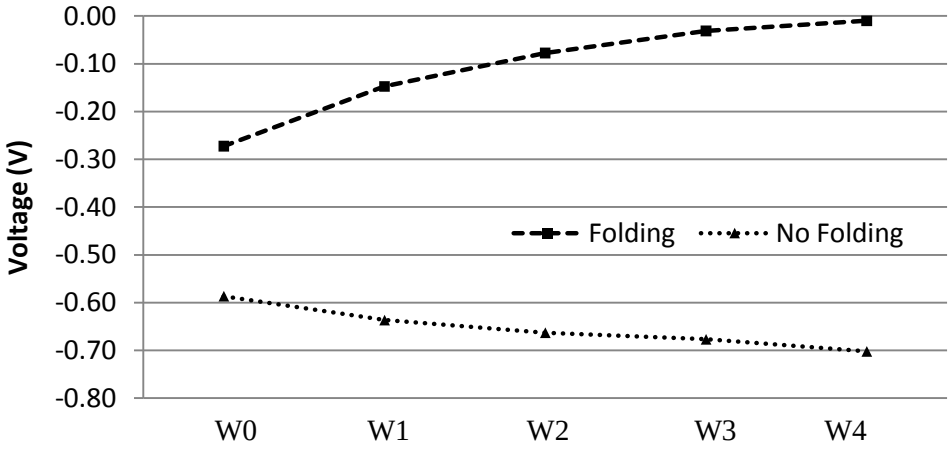


Figura 4.4 (a): 26.5 MeV/(mg/cm^2) íon – Pico de Amplitude do SET (V)

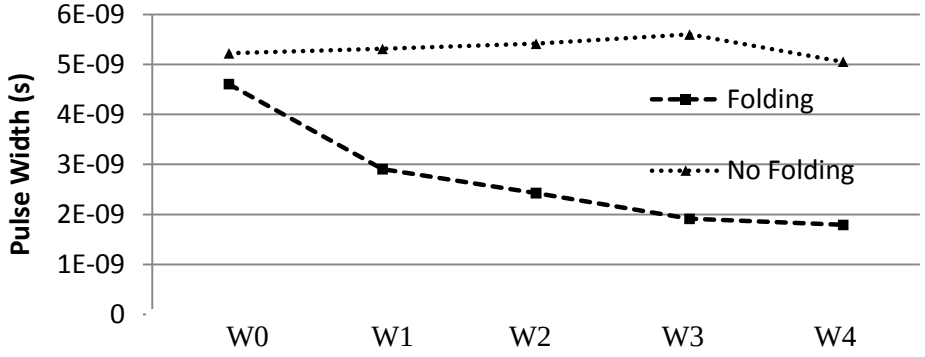


Figura 4.4 (b): 26.5 MeV/(mg/cm^2) íon – Largura do Pulso (s)

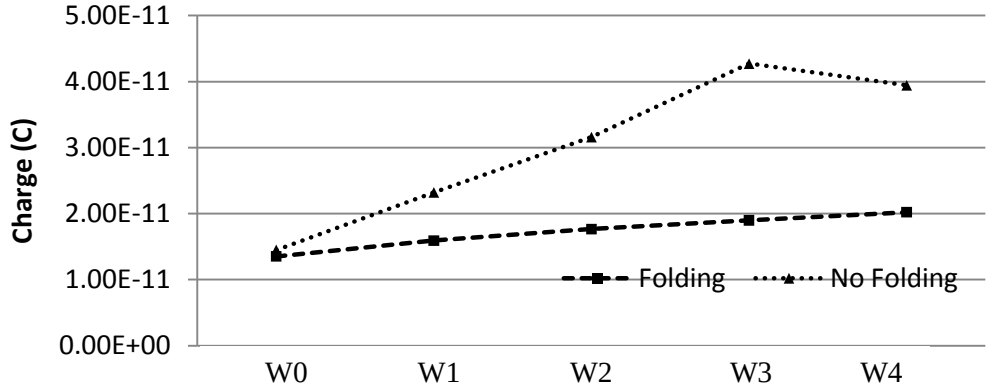


Figura 4.4 (c): 26.5 MeV/(mg/cm^2) íon – Carga Coletada

Estes resultados mostram a eficiência da técnica em reduzir o efeito transiente para partículas de alto LET. Os mesmos resultados são vistos para partículas de 40 MeV/(mg/cm^2).

4.2. Conclusão do Particionamento de Transistores

A técnica de transistores foi avaliada para a uma tecnologia 90nm e os resultados mostram que a técnica aumenta a tolerância do circuito a efeito transiente uma vez que o particionamento reduz a área de junção do dreno onde ocorre a coleta de pares elétron-lacuna na radiação.

O uso de particionamento de transistores permite que o transistor seja aumentado sem aumentar a área total do dreno, com isto a área total de coleta é reduzida.

5. Conclusão

Neste trabalho um transistor MOSFET, 90nm do tipo N foi modelado e seus resultados comparados com um modelo preditivo. Os resultados indicaram a conformidade do modelo com os transistores elétricos preditivos.

A análise da técnica de redimensionamento de transistores com o dispositivo mostrou que a eficácia da técnica depende dos níveis das partículas injetadas. Para partículas de baixo LET como partículas alfa de (1.31MeV/(mg/cm^2)) notou-se que a técnica conseguiu reduzir o efeito do transiente.

Para partículas de alto LET observou-se que o redimensionamento do transistor aumentou o efeito dos transientes. Identificou-se que isso pode ocorrer devido o aumento da área de junção do dreno que permite uma coleta mais eficiente dos pares elétrons-lacunas gerados durante a ionização.

Porém observou-se que o particionamento de transistores pode auxiliar o redimensionamento de transistores. O particionamento de transistores permite que o aumento do transistor seja realizado sem aumentar a área de dreno, adicionando transistores adicionais em paralelo. Com isto podemos reduzir drasticamente o efeito da ionização tanto para partículas alfa como para íons pesados.

A conclusão final é que a utilização conjunta de redimensionamento e particionamento de transistores auxiliam a redução de efeitos transitórios tanto para partículas de baixo como de alto LET.

Como trabalhos futuros podem se avaliar topologias de transistores do tipo Silicon-in-Insulator (SOI) e transistores FinFET. Estudos adicionais devem incluir o efeito da coleta de carga por múltiplos nós.