A HIGH-RATE FASTBUS SILICON STRIP READOUT SYSTEM *

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Abstract

This paper describes a synchronous silicon strip readout system capable of zero deadtime readout at average trigger rates in excess of 1 MHz. The system is implemented in FASTBUS, uses pipelining techniques, and includes point-to-point fiberoptic data links to transmit detector digital data. Semi-custom ASIC chips are used to amplify, discriminate, and logically combine track data before encoding. This paper describes the overall system, each major FASTBUS module, and the functional aspects of the ASIC chips.

Introduction

Extracted beams at Fermilab retain the 53 MHz RF structure of the Tevatron accelerator. Events occur in well defined "buckets" of time which are approximately 1.5 ns long and occur every 18.9 ns. We are developing a silicon strip detector readout system capable of associating all of the information from an event with a single RF bucket and completely recovering within one or two buckets. The system operates synchronously with the 53 MHz Tevatron clock. A digital memory is used to provide a trigger delay, which is adjustable in one bucket steps to a maximum of 4.8 μs.

The system consists of amplifiers mounted on the detector[1][2] and a set of FASTBUS modules that discriminate, delay, encode, and readout detector hit information.

System Overview

A block diagram of the system is shown in Figure 1. The detector signals are amplified by pre-amplifiers mounted near the detector. The amplified signals are connected to the FASTBUS data acquisition system by high density, .025 pitch, ribbon cables.

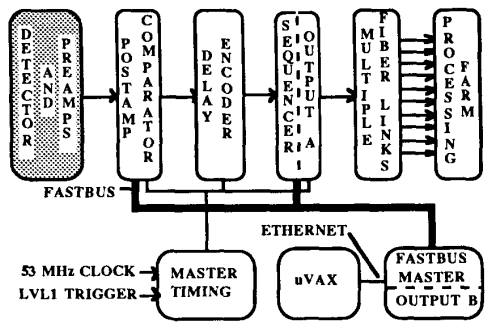

Figure 1: System Block Diagram

The Postamp/Comparator (P/C) modules discriminate the amplified signals. The discriminated signals are synchronously applied to the Delay/Encoder (D/E) modules in parallel where all channel data is delayed pending a Level 1 trigger signal. Upon the occurance of a Level 1 trigger, the hit data propagating through the memories of the D/E modules is input to the encoders. Up to 12 D/E modules simultaneously pass encoded hit data to the Sequencer (SEQ) modules. Data can be readout through a FASTBUS Master in each crate (output B), or be transmitted directly out of the Seqeuencer modules (output A), over fiberoptic cable, to individual input ports of a NEVIS [3] [4] readout and processing system.

System Board Partitioning

The FASTBUS implementation of the system is based on 128 channel increments. Each fully loaded FASTBUS crate can process a maximum of 1536 channels. Each crate can contain 12 Postamp/Comparator modules, 12 Delay/Encoder modules, a FASTBUS Smart Crate Controller, and a Sequencer module. A crate implementation is shown in Figure 2.

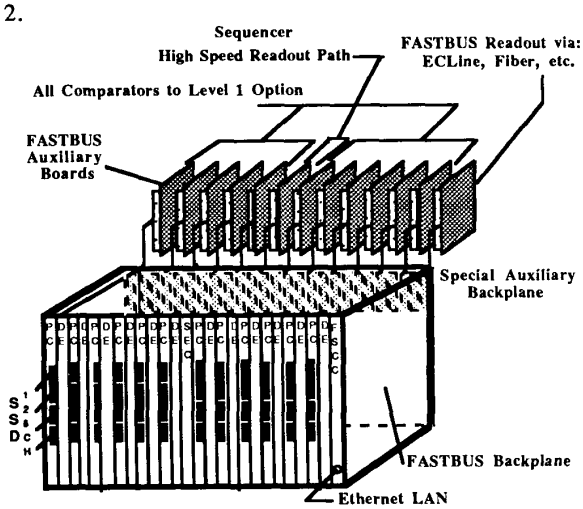

Figure 2: Crate Module Partitioning

Two different readout modes are user selectable. The FASTBUS readout path provides a relatively high bandwith output to be used with FASTBUS, VME, or CAMAC buffers on the receiving end. The Sequencer output is intended to be used to feed optical links. In the fiberoptic link case, each crate transmits data to an independent receiver buffer that is part of a high speed event processor [4]. The Data transmission rate using the fiberoptic FASTBUS Auxiliary port is 40 MBytes/Sec/Crate.

*This work performed under the auspices of the United States Department of Energy.

System Modules

Preamplifier

A silicon strip amplifier which uses a Tektronix semicustom bipolar integrated circuit has been developed [2]. It has a fast impulse response (35 ns base to base) and high gain (17 mv/fc), and is able to directly drive a differential transmission line. The amplifiers are mounted in small custom leadless chip carriers, with 25 mil pitch in order to meet density requirements. Sixteen chip carriers, or 128 channels, are mounted on a double sided printed circuit board measuring 3.5 X 4.5 inches. Each board plugs into an edge connector mounted directly on the silicon strip detector Kapton fanout. Four 64 conductor, 25 mil-pitch flat cables connect each preamplifier card to Postamp/Comparator modules. Due to the high gain-bandwidth of the amplifiers, special attention must be given to grounding and shielding [1].

Postamp/Comparator (P/C)

The P/C module amplifies, discriminates and logically combines 128 channels of silicon strip hit data. A block diagram of this module is shown in Figure 3. The major portion of the analog and digital circuitry required on this board is implemented using bipolar Application Specific Integrated Circuits (ASIC) manufactured by Tektronix. The threshold setting Digital-to-Analog Converter is implemented as a CMOS ASIC.

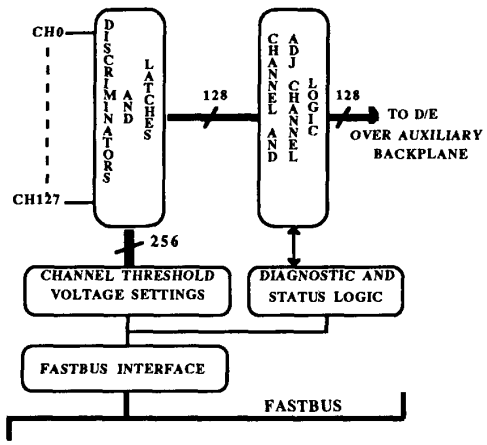

Figure 3: Postamp/Comparator Module

The following is a description of each ASIC contained on the P/C module.

ASIC 01: Two Channel Sum, Quad Latched Discriminator

A block diagram of this chip is shown in Figure 4. This ASIC receives low level linear differential signals from the preamplifiers mounted on the detector and produces analog sums of adjacent strip signals, discriminated digital signals of individual channels and discriminated signals of the analog summed adjacent channels. The **analog sum** block accepts the adjacent channel signals and provides an output proportional to the sum of its two inputs. The purpose of this block is to allow the discrimination of signals produced by particles which transverse the SSD midway between strips causing the signal to be divided between two adjacent channels.

The **discriminator** block provides an output logic level for the duration that the input signal is above a set threshold level. Each of the four discriminators has an individual threshold voltage control that allows individually set thresholds between 10 and 50 mV referred to the discriminator input. There is a built in hysteresis of 10 mV.

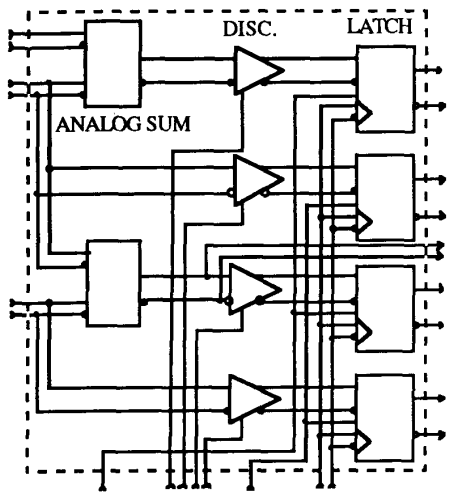

Figure 4: ASIC 01

The output of each discriminator drives a transparent **latch**, all four of which are controlled by a common 2.5 ns wide **latch** signal. In one state the latch is in the transparent mode, passing its input to the output. In the other state the output is latched ignoring input changes. There are also two Force Zero inputs, one for the individual signal latches and one for the summed signal latches that force the appropriate latch outputs to logical zeros.

ASIC 04: 5 Channel Logic and Octal NHit

The circuitry of ASIC 04 and ASIC 02 function jointly to logically combine 8 channels of track data. Block diagrams of the two ASICs are shown in Figures 5 and 6 respectively. They accept as inputs the outputs of 4 ASIC 01 chips (Two Channel Sum, Quad Latched Discriminnators). If any individual channel input is above the threshold during the latch transition, a logical high is output on that corresponding channel. If two adjacent channels have signals both of which are below threshold but the sum of the two is above threshold, a logical high is output on those two corresponding channels.

The logic can be bit sliced at any channel boundary. Chip pinout limitations on the Tektronix linear arrays dictated that of a given set of 8 channels, the lower five would be processed by ASIC 04 and the upper three by ASIC 02. Thus 16 ASIC 04/ASIC 02 pairs are capable of processing all 128 channels as one logical unit.

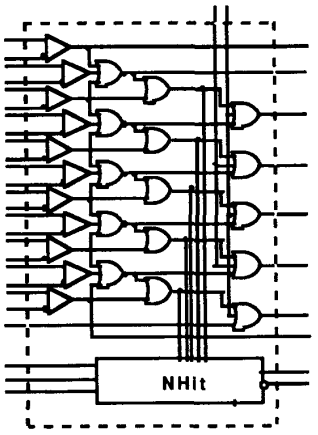

Figure 5: ASIC 04

The **NHit** circuitry provides a current output dependent on the number of channels hit. The output is approximately 100μA per strip hit. In the situation described above where individual signals are below threshold but the sum of the two is above, only 100 μA is provided thereby treating it as a single hit.

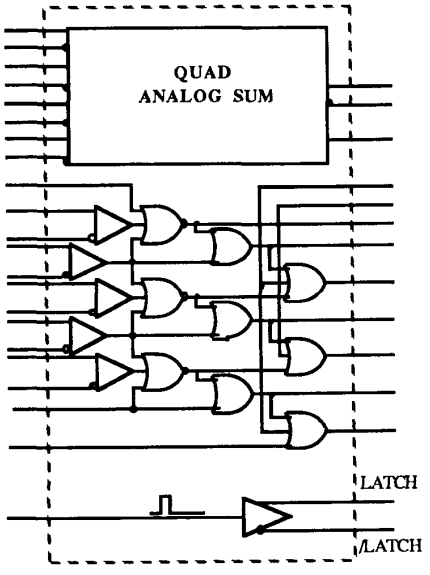

Figure 6: ASIC 02

ASIC 02: Quad Analog Sum and Latch Driver

The **Quad Analog Sum** circuit on ASIC 02 gets its inputs from analog sum outputs on ASIC 01 (two input sum circuits), thus producing an analog sum of eight adjacent channels.

The **Latch Driver** takes an ECL 2.5 ns pulse, converts it to a differential pulse which will then be used to drive the latch inputs of the four corresponding ASIC 01's.

ASIC 03: Digital to Analog Threshold Set and Readback

The chip shown in Figure 7 is a CMOS implementation of 4 D/A output channels and a single A/D readback channel. Writing and reading of this chip is accomplished through the FASTBUS system. To set a threshold for each channel and adjacent channel sum discriminator, 256 D/A outputs are required per 128 channel P/C module. 64 D/A chips are mounted on the P/C module in this case. It is optionally possible to feed more than a single channel discriminator with the same threshold level. Implementing this option minimally requires a single D/A chip with each output feeding 64 discriminators.

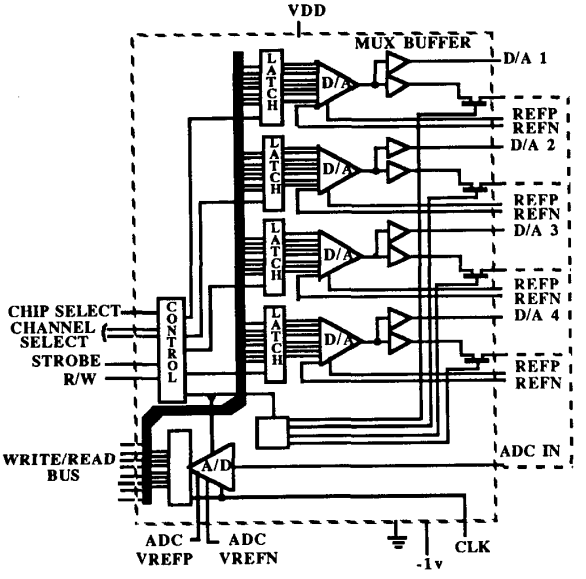

Figure 7: ASIC 03

Delay/Encoder (D/E)

The D/E module (Figure 8) accepts 128 channels of parallel data from the P/C every 18.9 ns and stores the individual channel data for up to 4.8 μsec, while a level 1 trigger decision is made. The delay is implemented using high-speed ECL memory (10422-5). The 18.9 ns time between events is split into a write cycle and read cycle.

During each 18.9 ns RF cycle, a write address counter is incremented and data is written into the delay memories. During any cycle, stored data may be read from any memory location. No detector deadtime is generated by this readout.

When a level 1 trigger occurs, the MTC generates an address that corresponds to the location in the D/E memories holding data for the RF bucket in which the triggering event took place. This address is fanned out through the SEQ modules to all of the D/E's in the readout system. Data from the RF bucket containing the triggering event and data from the previous RF bucket in time are input to a pipelined priority encoder. It takes seven clock cycles to load the encoder pipeline. After this delay, the D/E outputs an ordered list of hit strips. The address of each hit strip is encoded in a seven bit number. An adddtional bit is used to flag strips which were hit in the RF bucket previous in time to the

triggering bucket. This bit identifies hits that are likely to have been caused by an event other than the triggering event.

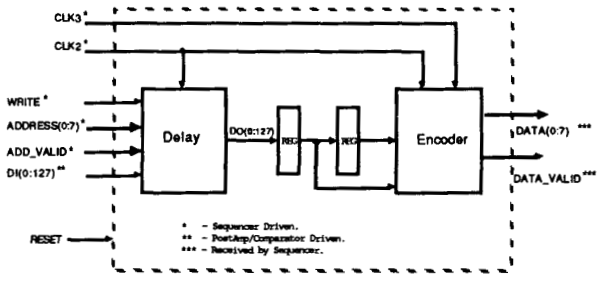

Figure 8: Delay/Encoder

Encoded data is transferred synchronously to the SEQ module over point-to-point connections on the FASTBUS auxiliary backplane. This transfer is data driven and occurs in parallel for all D/E's.

Sequencer (SEQ)

A block diagram of the SEQ is shown in Figure 9.

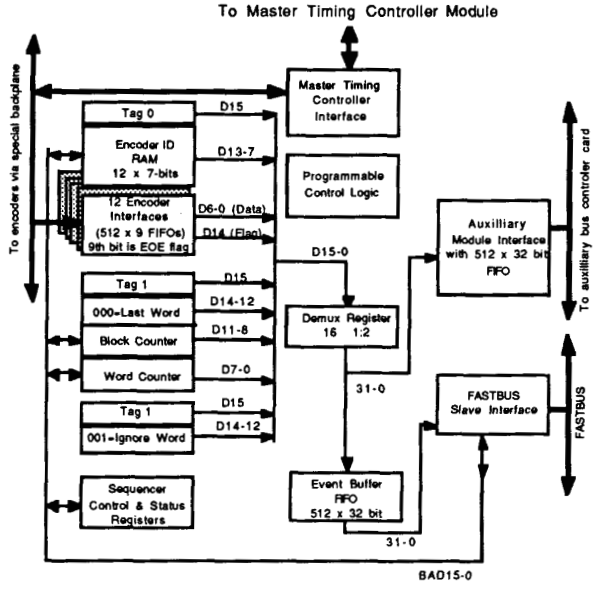

Figure 9: Sequencer Module

The SEQ module fans out triggers received from the MTC to the D/Es in the form of a hit address in the delay memories. It also accepts the conditioned 53 MHz clock from the MTC, delays it by a programmable amount, and fans out two versions of the 53 MHz clock and a 26.5 MHz clock derived from it, onto the FASTBUS auxiliary backplane. These clocks are used by the P/C to latch data, by the D/E to clock the high speed memory and the encoder pipeline, and to synchronize the data transfer from the D/E modules to the SEQ. The SEQ accepts data from the 12 D/E's in parallel and places it in 12 FIFO's. When a trigger is received, the SEQ deasserts an "Encoder Ready" signal which is input to the MTC. As soon as all D/E data has been transferred to Seqeuncer input FIFO's, the "Encoder Ready" is asserted again and the readout system is ready to process another trigger.

The Sequencer reads data out of its input FIFO's in a fixed order. The 8 bits of data from each D/E are combined with 7 bits of D/E address and stored in a FASTBUS accessible memory. A high order zero is added to distinguish data from control information. The end of event is marked by control word containing a count of the number of data words and a 7 bit "event number' that may be used to insure synchronization across the entire readout system. The sequenced data is moved two 16 bit words every 73.4 ns into a "Event Buffer FIFO" that can be accessed from FASTBUS. The data is simultaneously output through the auxiliary connector to an optional high-speed fiberoptic link. When the fiberoptic port is used, the data may still be readout of the "Event Buffer FIFO" over FASTBUS and used to compile high statistics histograms in the FSCC without reducing the readout bandwidth.

FASTBUS Smart Crate Controller (FSCC)

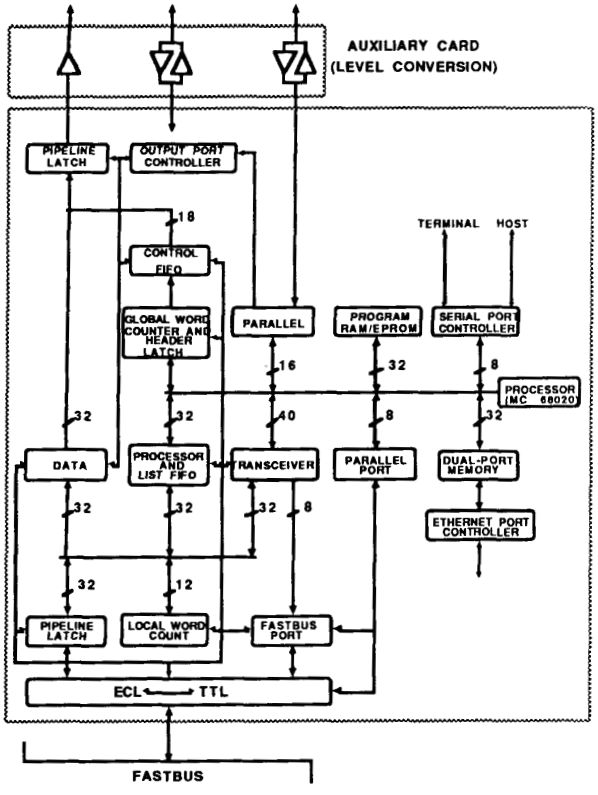

Figure 10: FSCC

The FSCC, shown in block form in Figure 10, is designed as a limited general-purpose readout device for low-occupancy front-end systems. It can execute most FASTBUS master operations directly from higher level software at normal 68020 processor speeds, typically a few hundred nsec per

instruction, and also supports faster operation through microcoded list operations. The FSCC is dual-ported from FASTBUS to the auxiliary connector to allow 100 nsec block transfers on both ports through an intermediate FIFO buffer. This buffer is designed to store the data from a single crate of front-end modules and insert a leading word count or header. The output port connects to several standard formats using an auxiliary card level adaptor. In addition to the data ports, two RS 232 lines, an Ethernet interface and trigger I/O ports are provided. The FSCC runs the PSOS real-time OS kernal and is programmable in any combination of C, assembler or microcode depending on performance requirements.

Master Timing Controller (MTC)

The Master Timing Controller generates the system clock, controls system synchronization, and generates delay memory addresses upon the receipt of Level 1 triggers from the experiments Trigger system. A block diagram of the MTC is shown in Figure 11. The MTC receives the 53 MHz Tevatron

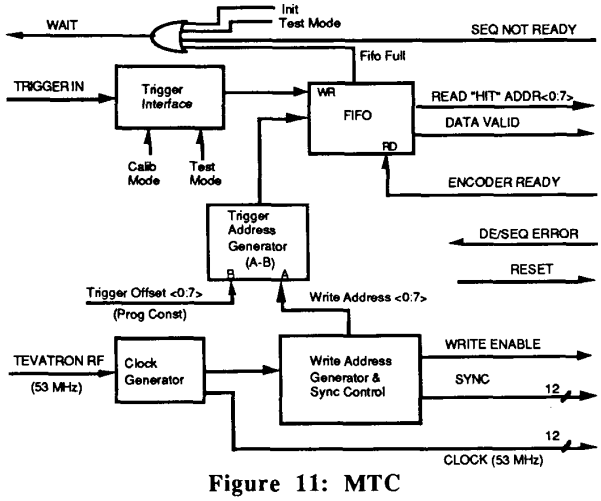

Figure 11: MTC

RF clock and establishes a 50% duty cycle clock whose phase is adjustable relative to the incoming RF. This CLOCK along with a SYNC pulse are distributed to each SEQ and eventually to all D/E's. D/E's use this clock and sync to determine write addresses for incoming data. Being synchronized, the MTC knows the current D/E write address and generates a read or "hit" address when a trigger is received. The hit address generated is offset from the write address based upon a calibration of the Trigger decision time. Hit addresses are placed into a high speed FIFO queuing up to eight trigger requests and can be accepted on successive RF buckets. The read or "hit" address output from the FIFO is broadcast to all D/E modules at a rate determined by the ENCODER READY signal summed from all D/E modules.The ability to pipeline triggers makes the system truly deadtimless at trigger rates up to the readout bandwidth. With knowledge of the read address and the D/E's current write address, the MTC detects fatal DE memory overwrite errors. However, to prevent such a condition, the system is throttled by sending a WAIT signal to the Trigger system under appropriate conditions.

Project Status

All system module logical design is complete. The FSCC is in the second prototype stage. The P/C module board layout is nearing completion. The D/E and the MTC module prototype boards are due in February 1990. The SEQ module board design has started and will be completed in February. Prototype printed circuit boards of each of the system modules are expected to be available in early March for initital integrated testing.

Acknowledgements

The authors would like to thank Garry Moore, Betty Conrin, Rick Kwarciany, John Chramowicz, Rick Van Conant, Scott Holm, Bruce Merkel, and our tireless cooperative education student, Mike Kodner for the effort they expended on this project. Ruth Pordes and Mark Bernett of the Computing Division were instrumental in developing the software needed to make the FSCC a usable product.

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