A Modified Lightly Doped Drain Structure for VLSI MOSFET's

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Abstract—**A new n-MOS LDD-like device structure (the J-MOS transistor) is proposed. Its design, simulation, and fabrication are studied in this paper. n-channel MOSFET's with L_{eff} below 2 μm suffer from high-field effects that must be overcome to secure reliable 5-V operation. LDD structures alleviate these effects, but their reliability is better than that of conventional MOSFET's only if the n^- regions have a peak doping density above 1×10^{18} cm^{-3}. To overcome this limitation and to allow constant voltage scaling for devices into the submicrometer regime, the J-MOS structure uses a series drain JFET to drop part of the supply voltage. Both 2-D device simulations and experimental results are presented to demonstrate the operation of this device and its potential for applications requiring reliable submicrometer device operation under maximum supply voltage. The major experimental findings are that the J-MOS structure can sustain 5-V operation even for submicrometer effective channel lengths. As has been the case with all LDD-like structures, improved device reliability has been achieved at the expense of some performance. However, the advantages of keeping 5-V operation in micrometer-sized devices may outweigh this performance loss.**

I. INTRODUCTION

PAST EXPERIENCE in MOSFET scaling has shown that device design has proceeded under constraints other than those suggested by constant electric field scaling principles [1]. Alternative scaling approaches [2]–[4] have been used instead, which have allowed continued scaling under constant supply voltage. The shrinking of device dimensions while keeping supply voltage constant offers circuit and system performance advantages, in addition to compatibility with the established 5-V standard. This leads inevitably to higher electric fields inside the active regions of the transistors. The operation of micrometer and submicrometer MOSFET's in the presence of high-field effects has called for innovation in their design so that acceptable device punchthrough voltage and long-term device reliability are maintained as MOSFET's are scaled. In particular, several LDD-like drain structures with the schematic cross sections of Fig. 1 have been studied and compared for use in VLSI circuits as substitutes for the conventional n^+ As drain. Careful engineering of the drain region in n-channel devices is more important than in p-channel devices because electrons in Si have a higher impact ionization rate, a lower energy barrier to injection into the oxide at the Si–SiO_2 interface, and experience drift velocity saturation at smaller fields than holes. High-field effects are then much more harmful to n-channel device performance and reliability. Since device degradation [5]–[8] is related to heating of carriers as they traverse regions of field strength in excess of 100 kV/cm, reducing electric fields at the drain end of the channel is crucial in n-channel devices. LDD designs for submicrometer p-channel devices have also been proposed [9], mostly for reasons of punchthrough prevention.

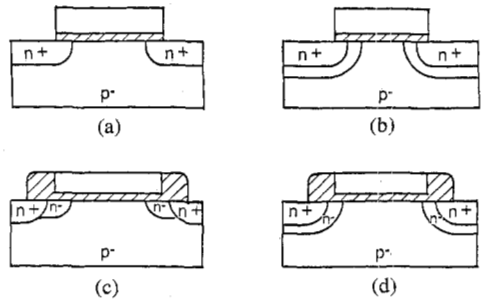

Fig. 1. Schematic cross-section of (a) conventional, (b) double diffused drain, (c) "inside" LDD, and (d) "outside" LDD n-channel device structures.

In both the LDD FET [10]–[20] and the graded S/D [21]–[27] or double-diffused drain (DDD) n-channel structures of Fig. 1, the narrow n^- regions that are introduced between the channel and the n^+ source–drain are designed to spread the high electric field at the drain into the n^- region. Other device structures using a non-self-aligned separate gate, buried channel, or lightly doped S/D have also been proposed [28]–[32]. The reduction and/or spreading of the peak E-field in self-aligned LDD-like structures normally results in an increased reliability insofar as hot-electron-induced instabilities are concerned. However, if the n^- surface doping (N_S) is too light, i.e., $N_S < 10^{18}$ cm^{-3}, the LDD FET's can actually exhibit poorer reliability than conventional arsenic-doped n^+ S/D transistors in addition to increased series resistance. This LDD related degradation has been shown to be caused by hot-carrier injection into the sidewall oxide region [33]–[36]. This is shown as process (2) in Fig. 2. It leads to excessive series resistance and degradation rates faster than conventional designs [33], [34]. At an optimum n^- doping level, process (1) of Fig. 2 should dom-

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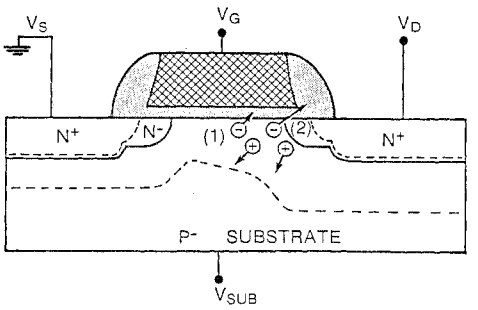

Fig. 2. n-type LDD MOSFET device structure. Hot-carrier injection occurs either (1) under the gate or (2) over the n^- region under the sidewall oxide.

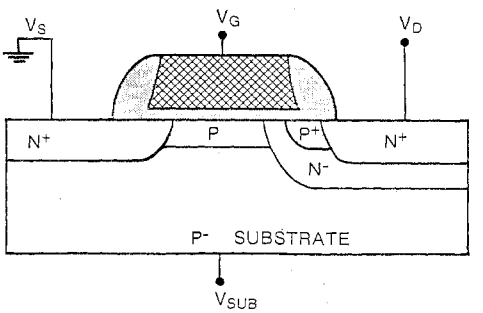

Fig. 3. The n-type JFET-MOSFET (JMOSFET) device structure.

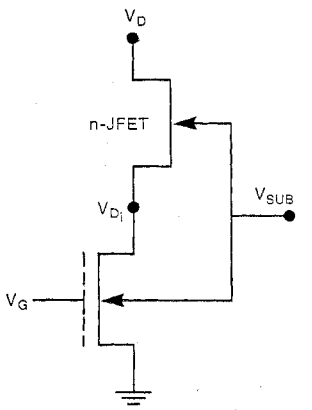

Fig. 4. Equivalent circuit model for the JMOSFET device.

inate as the longitudinal E-field peaks under the gate. The n^- resistive region of optimized LDD FET's spreads and reduces the peak value of the longitudinal electric field along the channel length, but the n^- region under the sidewall oxide must still remain undepleted for the aforementioned reliability reasons. While peak substrate current is usually reduced with a lighter n^- dose, characteristics of LDD devices can deteriorate more rapidly with n^- doses $< 10^{13}$ cm^{-2} [20], [33], [34], [36], [37]. Optimum LDD designs have been studied extensively, and for practical junction depths and S/D anneal temperatures, the optimum N_S is 1–2.5 $\times$ 10^{18} cm^{-3} [20], [38], or, alternatively, the optimum n^- dose is $\simeq$1–2 $\times$ 10^{13} cm^{-2} for "inside" LDD's of the type shown in Fig. 1 [36], [39], [40]. Other studies have proposed that a better I_{SUB} and device degradation trade-off for "inside" LDD's occurs with either a moderately doped (4–10 $\times$ 10^{13} cm^{-2}) phosphorus n^- region [41] or with an As/P graded n^- region [42]. Other studies have suggested optimum n^- implant doses of $\simeq$5–20 $\times$ 10^{13} cm^{-2} for both "outside" LDD's (Fig. 1(d)), [43], and DDD MOSFET's (Fig. 1(b)) [40], [44]. Analytical models [45], [46] have predicted breakdown voltage improvements of less than 2 and 1 V for DDD and "inside" LDD devices, respectively, for the range of optimum n^- doping levels given above.

II. JMOS Device Structure

In the search for reliable VLSI MOSFET's one should recognize the importance of both reducing high fields inside the device, and also keeping high fields as far away as possible from the most sensitive MOSFET region which is the Si–SiO_2 interface. Most device instabilities are the result of damage to the gate oxide. In the JFET-MOSFET (JMOS) structure that we have proposed [47], shown in Fig. 3, one seeks to keep the field peak away from the region under the gate, and at the same time force the electron current below the surface in the critical high field region near the drain. This should have the effect of minimizing hot-carrier trapping in the gate or sidewall spacer SiO_2 regions. Other authors have also shown that LDD's can perform more reliably by diverting the channel current away from the SiO_2 interface in the high field drain region. Techniques proposed to accomplish this include either a buried-channel device with a lightly doped drain [48] or a retrograde n^- profile for the LDD region [49]. Other MOSFET device structures have been proposed, like the buried-drain D-MOSFET [50], for which the reliability potential in VLSI has not yet been assessed.

If a more reliable device structure can be designed, then an increase in power supply voltage or a reduction in MOSFET channel length at a given voltage to achieve a performance enhancement is possible. The proposed structure in Fig. 3 has a short-channel JFET at the drain end. The JFET physically occurs because of the presence of a p^+ region acting as the JFET gate above the n^- drain region (Fig. 3). The p^+ implant connects electrically to the substrate by overlapping the channel stop implant in the transverse direction. The circuit model for such device is shown in Fig. 4. The JFET under the sidewall oxide is fully merged into the MOSFET structure and does not require extra silicon area. It does require a minimum of one extra mask in the process.

III. Device Simulation

The JMOS circuit model of Fig. 4 was simulated using SPICE and the transfer function V_{D_i} versus V_D is plotted in Fig. 5, where V_{T_J} is the JFET threshold voltage, V_{D_i} is the effective drain bias on the intrinsic MOSFET, and V_D is the externally applied drain bias. The HPSPICE MOSFET level 3 and JFET model parameters used are listed in Table I. The simulation suggests that by appropriately choosing the JFET pinchoff voltage V_p, the device designer can limit the maximum drain bias across the surface-channel MOSFET. Thus, the JMOS device provides

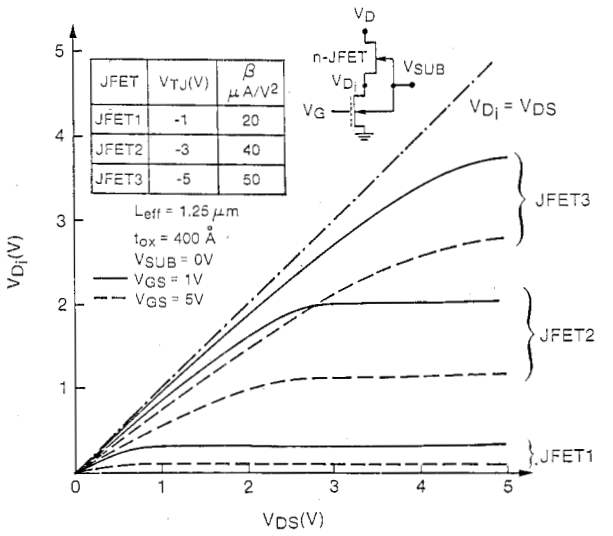

Fig. 5. Relationship between the externally applied JMOSFET drain bias (V_{DS}) and the voltage at the intrinsic drain of the surface channel MOSFET (V_{D_i}) for three different JFET designs.

TABLE I

MOSFET DEVICE PARAMETERS			
Name	*Symbol*	*Value*	*Unit*
Low field mobility	μ_o	665	$cm^2V^{-1}sec^{-1}$
Oxide thickness	t_{ox}	393	Å
Transconductance factor	K_P	58.5	μAV^{-2}
Threshold voltage	V_{T_o}	0.32	V
Effective substrate doping	N_{SUB}	9.1×10^{15}	cm^{-3}
Body factor	γ	0.515	$V^{-1/2}$
$(L_{mask} - L_{eff})/2$	L_D	0.25	μm
Gate field mobility factor	Θ (V_{NORM}^{-1})	0.061	V^{-1}
Longitudinal field mob. factor	E_{TRA}	7.3×10^4	$V\,cm^{-1}$
Critical field	E_{CRIT}	1.7×10^4	$V\,cm^{-1}$
Saturated drain conductance	DE_{SAT}	7.9×10^9	$V\,cm^{-2}$
JFET DEVICE PARAMETERS			
Threshold voltage	V_{T_J}	−1, −3, −5 *	V
Transconductance factor	β	20, 40, 50 *	μAV^{-2}
Channel length modulation	λ	0.05	V^{-1}

* JFET1, JFET2, JFET 3

a means of minimizing hot-carrier problems imposed by constant voltage scaling [7], since the series JFET can be designed to support part of the drain supply. When the MOSFET channel is conducting current, the inequality

$$V_{D_i} < (|V_p| - \phi_{bi} - |V_{\text{SUB}}|) = V_{\text{SUB}} - V_{T_J} \qquad (1)$$

holds, where V_p is the JFET region pinchoff voltage, and ϕ_{bi} is the p^+-n^- junction built-in potential. In practical designs V_p, V_{T_J}, and V_{SUB} are ≤ 0.

Limiting V_{D_i} could also be accomplished, of course, by reducing the supply voltage. However, this has important drawbacks since such a reduction leads to compatibility problems, to smaller noise margins in circuits, and to reduced $(V_{GS} - V_T)$ MOSFET drive. Less gate drive often implies slower circuits. The presence of a series drain JFET in the JMOS device allows the full supply to be used on the V_D and V_G terminals, while the internal voltage of the MOSFET drain is reduced. Conventionally designed micrometer-sized n-MOSFET's in fact need drain biases of less than 3 V in order for the channel current to saturate in the practical range $0 < (V_{GS} - V_T) < 5$ V, as shown in Fig. 6. This is simply the effect of saturation of

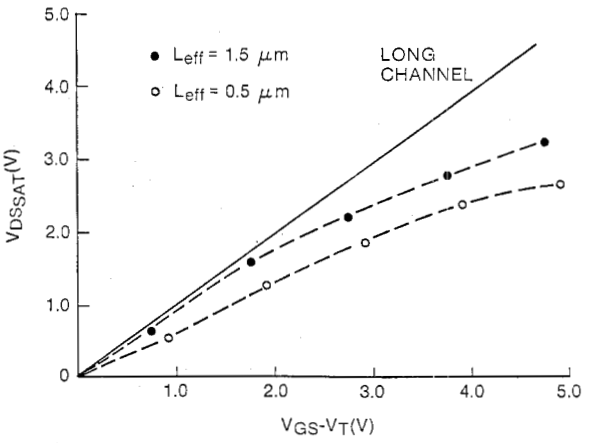

Fig. 6. Saturation drain voltage dependence on $V_{GS} - V_T$ for a conventional n-channel MOSFET.

the channel electron average velocity $\langle v \rangle$. Submicrometer devices operating in this saturated velocity regime will have a drain saturation current given by

$$I_{DS_{\text{sat}}} = W\langle v \rangle C_{\text{ox}}(V_{GS} - V_T) \qquad (2)$$

where $\langle v \rangle \simeq v_{\text{sat}}$ (the optical phonon scattering limited drift velocity for bulk transport).

The drain JFET device, once it pinches off, limits the JMOS current approximately to its first order pinchoff limit I_p [51]

$$I_p = WI_{p0}\left(1 - \left(\frac{\phi_{bi} + V_{D_i} + |V_{\text{SUB}}|}{|V_p|}\right)\right)^2 \qquad (3)$$

$$I_{p0} = \frac{|V_p|}{n\rho_s L_{sw}} \qquad (4)$$

where $n(2 < n < 3)$ accounts for the nonuniform doping profile in the n^- JFET channel, $\rho_s(\Omega/\square)$ is the buried n^- sheet resistivity, L_{sw} is the sidewall spacer width—an approximate measure of the JFET effective electrical channel length—and $V_{D_i}(V_{GS})$ is the gate-voltage-dependent effective MOSFET drain or effective JFET source voltage, according to the lumped circuit model proposed to describe the JMOS device. Equation (3) neglects short JFET channel length effects that are more important when the n^- doping is lighter. I_{p0} depends on the technology design of the vertical impurity profile of the drain JFET, as well as the sidewall spacer width.

The JMOS device was simulated by the PISCES 2-D program [52], [53] coupled to impurity profiles simulated in 1-D by SUPREM-III [54]. Two-dimensional device simulations have been widely used as useful tools to guide and better understand the deisgn of LDD devices [55]. Fig. 7 shows the depletion region boundaries for the JMOS device under a bias condition in which the JFET under the sidewall oxide is in its linear region of operation. In this mode, the n^- region behaves as a series pinched resistor, or as a buried LDD structure. In Fig. 8, calculated equipotential contours show the saturation properties of the drain JFET. For those biases in which

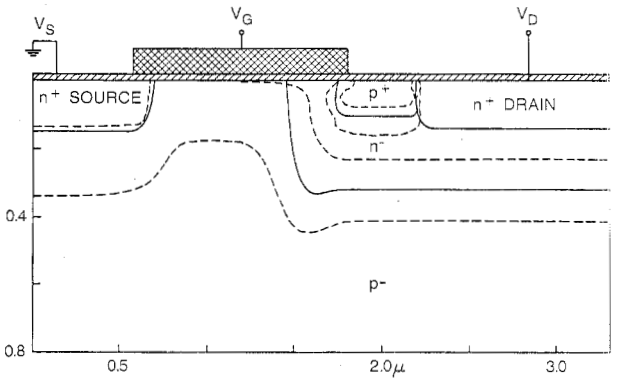

Fig. 7. PISCES simulated depletion boundaries for the JMOSFET with $L_{eff} = 0.72\ \mu m$, $t_{ox} = 200$ Å, $V_{T_j} = -1.6$ V, $V_{SUB} = 0$ V. Linear region bias of JFET. $V_{DS} = 0.1$ V, $V_{GS} = 1$ V.

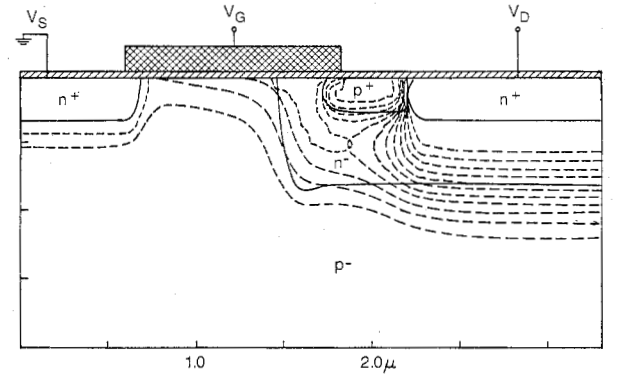

Fig. 8. PISCES simulated equipotential contours for the JMOSFET of Fig. 7. JFET is pinched off at $V_{DS} = V_{GS} = 5$ V.

the JFET is ON and pinched off, i.e.

$$(V_{DS} - V_{SUB}) \geq |V_{T_j}| \tag{5}$$

the saturated JFET limits the current in the device to the value of $I_p(V_{GS})$ given by (3). For the simulated device of Fig. 8, $V_{T_j} = -1.6$ V, $V_{DS} = 5$ V, $V_{SUB} = 0$ V. The JFET pinchoff region then supports most of the 5-V drain bias on this particular JMOS design, while the surface channel MOSFET supports less than 1 V. As suggested by the simulated potential contours under the SiO_2–Si interface, and as we shall demonstrate experimentally, this will result in a large reduction in impact ionization under the MOSFET gate compared to a conventional device structure. The electron and net donor densities, and the electrostatic potential along the Si–SiO_2 interface in the JMOS device are shown in Fig. 9(a) and Fig. 9(b), respectively. The peak longitudinal E-field at the gate SiO_2–Si interface is kept below 5×10^4 V/cm, which is one order of magnitude smaller than typical peak fields at the drain end of pinched off conventional MOSFET's [56]–[58].

PISCES simulated I–V characteristics are shown in Fig. 10 for the device of Fig. 8. In this JMOS device the onset of saturation is independent of V_{GS} since the drain JFET pinches off at the drain voltages for which (5) is an equality. In this case the JFET operates as a current-limiting device fully merged into the LDD region. The PISCES

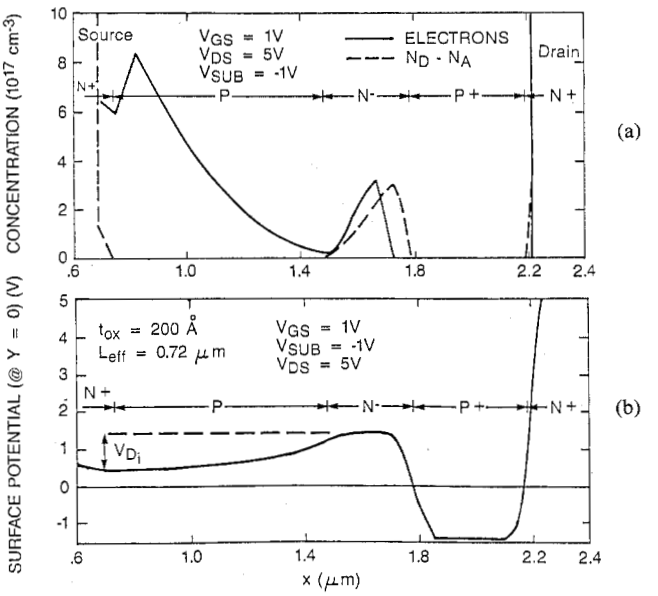

Fig. 9. PISCES simulations of the JMOS structure of Fig. 7: (a) Electron and net donor densities along the Si–SiO_2 interfaces; (b) Potential along the Si–SiO_2 interface. $V_{SUB} = -1$ V, $V_{DS} = 5$ V, $V_{GS} = 1$ V.

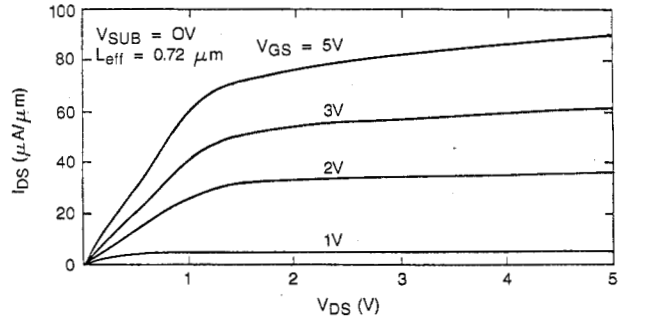

Fig. 10. PISCES simulated I_{DS} versus V_{DS} for $V_{T_j} = -1.6$ V. JMOSFET structure of Fig. 7. $V_{SUB} = 0$ V.

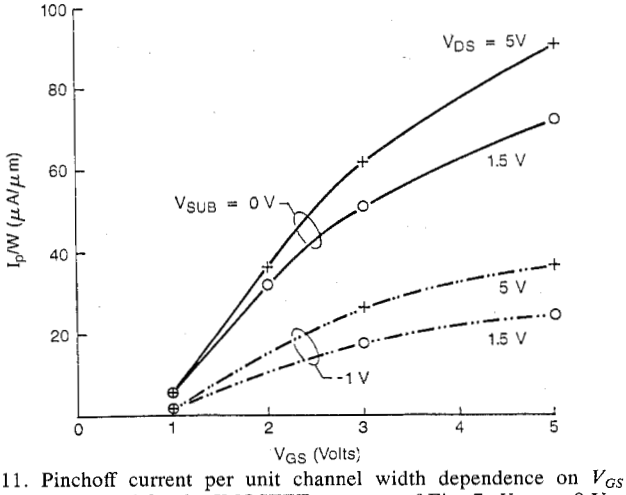

Fig. 11. Pinchoff current per unit channel width dependence on V_{GS}. PISCES simulated for the JMOSFET structure of Fig. 7. $V_{SUB} = 0$ V.

simulated transfer function (I_p/W) versus V_{GS} is shown in Fig. 11, where I_p is the pinchoff current of (3). A JFET short-channel effect is responsible for the output conductance in Fig. 10 and the variation of $I_p(V_{GS})$ with V_{DS} in

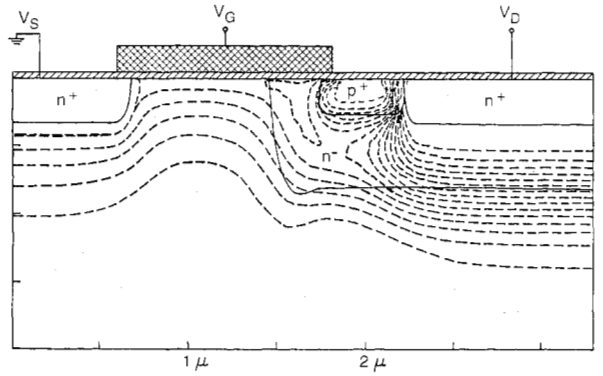

Fig. 12. PISCES simulated equipotential contours for the JMOSFET structure of Fig. 7. $V_{DS} = V_{GS} = 5$ V. MOSFET is ON and JFET is OFF at $V_{SUB} = -2$ V.

Fig. 11. This effect is quite easily seen in Fig. 8 as the drain field encroaches under the entire length of the p^+ JFET gate. Fig. 12 shows the same device under bias conditions that turn the JMOSFET off through the application of substrate bias, while the MOSFET surface is strongly inverted. In the case illustrated, $V_{GS} = V_{DS} = 5$ V and $(V_{SUB} - V_{D_i}) \leq V_{T_J}$, i.e., the drain JFET region is OFF and the MOSFET is ON. Thus, it is possible to turn off all JMOSFET's on a chip through appropriate substrate bias.

These device simulations have demonstrated the basic operation of the device. A variety of such simulations were used to suggest structural variations to optimize device performance. Control over the encroachment of high fields under the gate of the MOSFET can be achieved through proper design of the LDD region by adjusting the pinchoff voltage of the JFET region V_p to maximize device current drive while keeping short-channel effects and hot-carrier injection into the gate oxide under tolerable limits.

IV. Device Fabrication

The fabrication process used is a standard 2-μm n-MOS process using LOCOS isolation, a 400-Å gate oxide, and n^+ polysilicon gates. The starting material was ⟨100⟩, 20–25-Ω · cm boron-doped silicon. A 900-Å Si_3N_4 on 400-Å SiO_2 mask was used during the local oxidation. The boron field implant dose was 1.5×10^{13} cm^2 at 120 keV. The field oxidation was done in steam at 1000°C for 200 min.

Both conventional n-MOS devices and LDD n-MOS devices with five different variations in the source–drain regions were fabricated side by side, to test experimentally the JMOS device alongside the other better known LDD-MOSFET's. The major JMOS fabrication steps are shown in Fig. 13. By suitable combinations of the masked implants, all drain structures, including symmetrical JMOS and larger geometry JFET's, were fabricated side by side on the same chip. The asymmetric JMOS structure of Fig. 3 can be fabricated with only one extra masking step in addition to the conventional NMOS process if one were to choose an LDD-type source structure and a drain JFET structure. Lightly doped source structures should

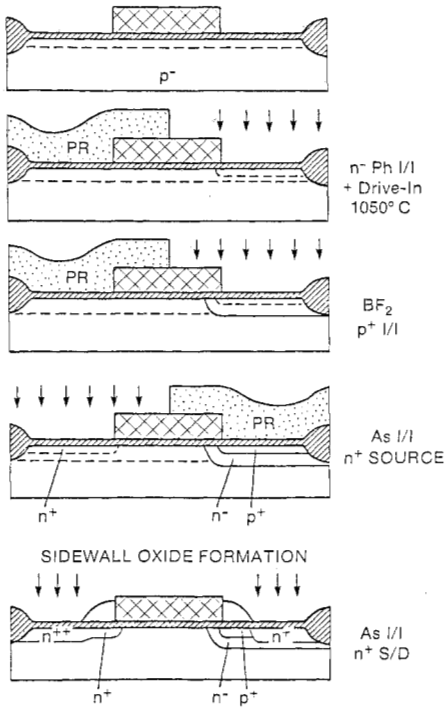

Fig. 13. Process sequence for JMOS fabrication.

either be doped above 5×10^{18} cm^{-3} or be avoided altogether if transconductance reduction due to series source resistance [59]–[62] is to be kept low. Lighter doping levels are necessary on the drain, however, if one seeks to reduce the drain high field problem. In this work, three different n^- phosphorus implant doses were used. Simulated surface concentrations for the n^- region were 8×10^{17} cm^{-3} for a low-V_p JFET, 2×10^{18} cm^{-3}, and 3×10^{18} cm^{-3} for higher V_p JFET's, after a 1050°C 60-min drive-in of the phosphorus implant. A shallow 100-keV p^+ BF_2 implant followed to form the substrate-connected JFET gate on the JMOS devices. The 1050°C anneal assured sufficient lateral diffusion of the n^- implant to guarantee merging of the surface MOSFET channel and the JFET channel after the p^+ and n^+ implant anneals that followed. LDD region definition was done with a conventional sidewall spacer technology [63]–[64] by depositing 8000-Å LPCVD oxide, followed by a 900°C/30 min oxide densification and oxide plasma etch. Final sidewall oxide spacer widths of 4100 to 4600 Å were obtained. Subsequently, a conventional n^+ As S/D implant and a 900°C/30 min anneal followed. SUPREM-III simulated profiles after all anneals for the high-V_p and low-V_p JFET designs, as well as for the n^+ As drain profile are shown in Fig. 14. Final MOSFET channel region boron surface concentration was 1.3×10^{16} cm^{-3}. Table II summarizes the relevant parameters for the two JMOS designs to be mentioned.

V. Experimental Results

A. I–V Characteristics

Fig. 15 shows the drain current versus V_{GS} characteristics for the low-V_p JMOS device at $V_{DS} = 0.1$ V, in

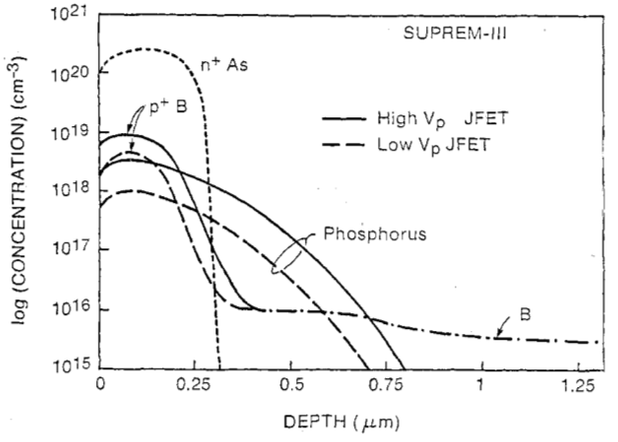

Fig. 14. SUPREM simulated impurity profiles for both JFET high-V_p and low-V_p designs.

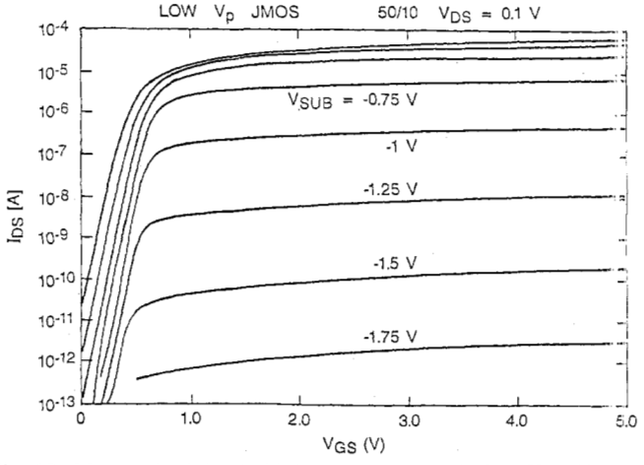

Fig. 15. Measured subthreshold characteristics for the low-V_p JMOSFET. $W = 50$ μm, $L = 10$ μm, $V_{DS} = 0.1$ V, V_{SUB} steps of -0.25 V from 0 to -2 V.

TABLE II

PROCESS PARAMETERS			
PARAMETER	*Low V_p Process*	*High V_p Process*	*Unit*
N^- Phosphorous Dose	2×10^{13}	7.5×10^{13}	cm^{-2}
Phosphorous surface conc. (N_S)	8×10^{17}	3×10^{18}	cm^{-3}
P^+ BF_2 Dose	6×10^{15}	2.2×10^{14}	cm^{-2}
N^- sheet resistance (ρ_s)	850	410	Ω/□
Pinched N^- ρ_s	5.8	1.2	kΩ/□
Oxide thickness (t_{ox})	400	400	Å
Sidewall width (L_{sw})	0.4	0.4	μm

which both the JFET subthreshold and the MOSFET subthreshold regimes are illustrated. The drain current exhibits the usual exponential turn-on [65] in the MOSFET subthreshold regime. However, due to the drain JFET gating action, the drain current can be turned off by setting $V_{SUB} < V_{TJ}$. For this low-V_p design $V_{TJ} = -(|V_p| - \phi_{bi}) = -0.8$ V. The long-channel zero-backgate-bias MOSFET threshold voltage is 0.32 V, as extracted by the TECAP2 [66] fitting of the conventional device linear region I_{DS}–V_{GS} characteristics at several substrate biases. Fully extracted conventional MOSFET parameters are shown in Table I.

A $W = 50$ μm, $L = 2$ μm JMOS device is compared to a conventional MOSFET of the same drawn gate length in Fig. 16. The JMOS effective channel length is ≈0.2 μm shorter than its conventional counterpart on the same chip. At large V_{GS} the value of I_p given by (3) saturates to a value $I_{p_{max}}$ experimentally determined for devices with $L_{gate} = 2$ μm. This saturated value of the JMOS I_{DS} for $V_{SUB} = 0$ V, $V_{GS} = V_{DS} = 5$ V is $I_p = 24$ μA/μm, and it is practically independent of MOSFET intrinsic channel length or polysilicon gate bias so that the JFET acts as a current limiter in the device structure. This value compares reasonably well with the simulated value $I_{DS_{sat}} = 37$ μA/μm for a slightly narrower sidewall spacer, and hence a shorter JFET length. The degree of current limiting by the JFET in this low-V_p design is more than what would be desired in an actual VLSI application but its characteristics are shown here to illustrate the JFET action as the two active devices are merged.

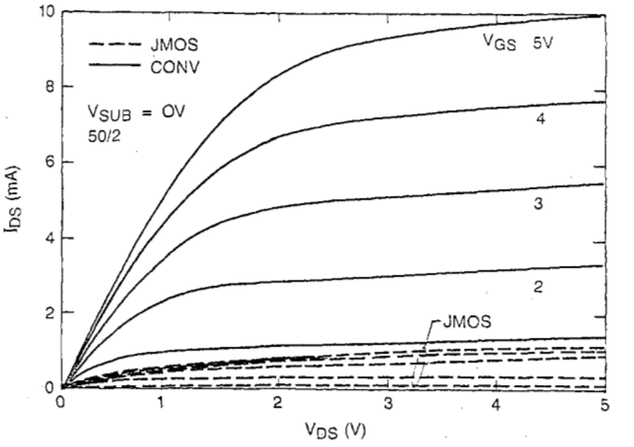

Fig. 16. Comparison of measured I_{DS} versus V_{DS} characteristics for the low-V_p JMOSFET and conventional device. Both devices have the same drawn $W = 50$ μm, $L = 2$ μm.

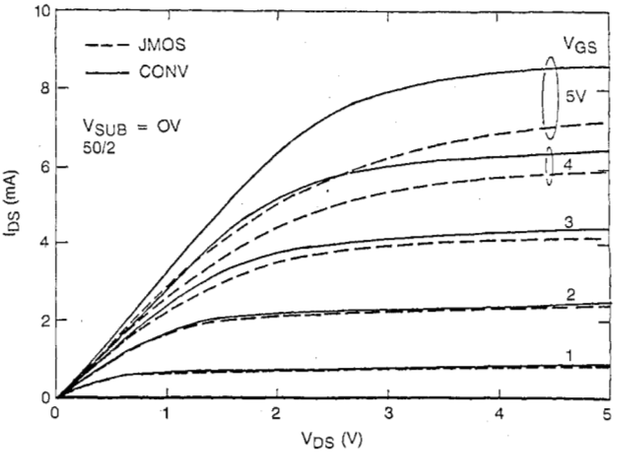

Fig. 17. Comparison of measured I_{DS} versus V_{DS} characteristics for a higher V_p JMOSFET and conventional device. Both devices have the same drawn $W = 50$ μm, $L = 2$ μm.

The I_{DS}–V_{DS} characteristics of JMOSFET's with higher V_p are compared to their conventional counterparts on the same chip in Figs. 17 and 18. These JMOSFET's have $I_{pmax} = 200$- and 320-μA/μm width, respectively. I_{pmax} for

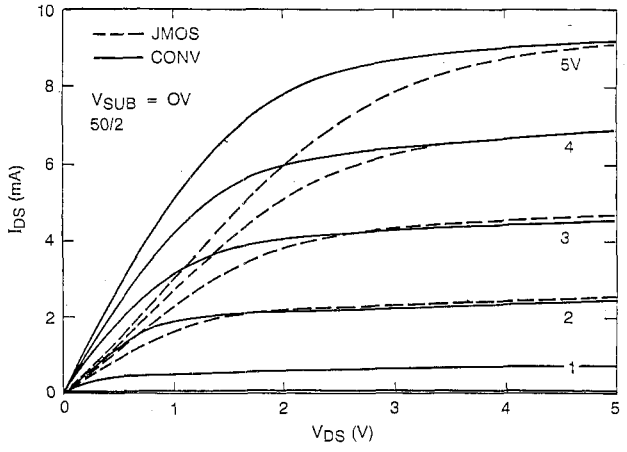

Fig. 18. Comparison of measured I_{DS} versus V_{DS} characteristics for the high-V_p JMOSFET and conventional device. Both devices have the same drawn $W = 50$ μm, $L = 2$ μm.

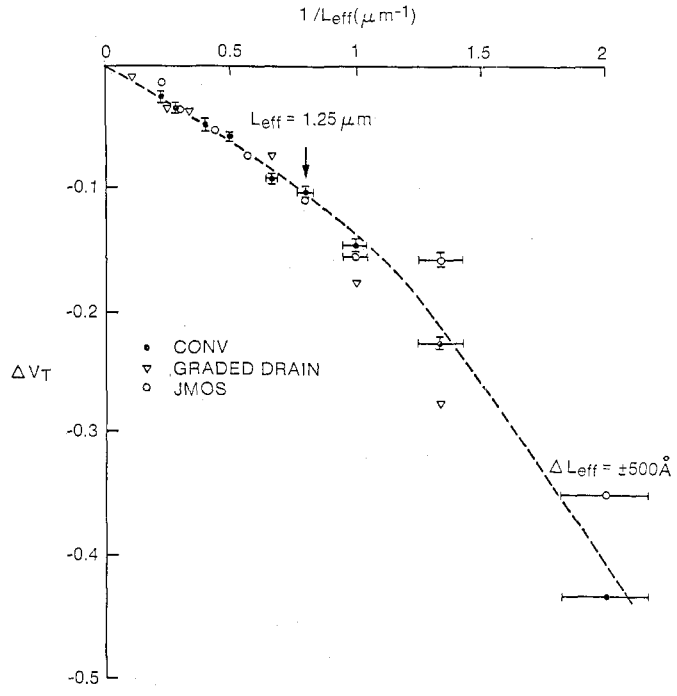

Fig. 19. Linear region threshold shift as a function of effective channel length. V_T extrapolation measurement at V_{DS} = 100 mV.

the high-V_p design of Fig. 18 is larger than the 5-V current drive capability of our conventional enhancement n-MOS devices built with a 400-Å gate oxide 2-μm technology. Hence, for large V_{DS}-bias short-channel MOSFET, the JMOSFET saturation current limit is given by velocity saturation of the MOSFET inversion carriers, according to (2). In the high-V_p case, as shown in Fig. 18, the $I_{DS_{sat}}$ values are the same for both conventional and JMOSFET devices. In this case the operation of the drain JFET is in its linear region, and the device acts as a simple buried LDD. This has the effect of increasing the linear region ON resistance of the JMOSFET. Drain series resistance for this case was extracted to be 10 kΩ · μm in excess of the conventional transistor series resistance by using the measurement procedure of [67]. Based on measured sheet resistivity data for large geometry n^- pinched resistors, one concludes that the n^- buried LDD contribution to the series drain resistance does not account for such a large series resistance increase. We believe that a sizable contribution to this ON resistance of the high-V_p JMOSFET comes from the contact resistance of the Al(1-percent Si) metallization to the n^+ drain diffused layer which is compensated by the high dose (2.2×10^{14} cm^{-2}) p^+ JFET gate implant. Further improvements of this device structure are necessary to address several detrimental effects of including a shallow p^+ implant into the drain n^- region: first, the low breakdown voltage of the p^+ substrate–n^+ drain junction; second, increased ON resistance due to impurity compensation of the surface n^- region; and third, the effect of the compensated p^+ layer on the contact resistance of the metal to n^+ region. These limitations can be overcome by more optimum design of the doping profiles in the drain region.

The 1050°C n^- drive-in step results in a fairly deep n^- junction in the high-V_p case, ≈ 0.7 μm according to the simulation results in Fig. 14. Also, considerable diffusion of the channel implants for V_T adjustment and punchthrough suppression occurs. Scaling suggests that the S/D junction depths should be kept as shallow as technologically feasible. A JMOS device optimized for technologies with $L_{eff} < 1$ μm would have to use shallower junctions. The threshold voltage shift in the short channel regime should in turn be controlled by an appropriate choice of t_{ox} and punchthrough suppression implant dose. For the technology choices in this experiment, all devices had a linear region short-channel V_T shift of less than 100 mV down to $L_{eff} = 1.25$ μm as shown in Fig. 19 for conventional (●), high-V_p (○) and graded S/D (△) devices. The V_T measurement used for Fig. 19 assumes that the threshold voltage is given by the linear region ($V_{DS} = 0.1$ V) extrapolation of the I_{DS}–V_{GS} curves at the maximum value of transconductance.

B. Substrate Current

In Fig. 20 the substrate current versus V_{GS} characteristics of both a conventional and a low-V_p MOSFET (same device as Fig. 16) are compared for devices with the same drawn $W = 50$ μm, $L = 1.5$ μm. The usual substrate current characteristics [68] are observed for the conventional MOSFET. Its bell-like shape indicates that the substrate current is mostly due to holes generated by impact ionization occurring as carriers traverse the high field region under the gate in the drain end of the device. The JMOSFET substrate current is mostly independent of gate voltage; it is not triggered by channel current; and, it is more than two orders of magnitude lower than the peak value of the conventional device. Except for the bias regime in which the conventional MOSFET is well into its linear mode of operation ($V_{GS} > V_{DS}$), i.e., the inversion layer extends from source to drain n^+ regions and decreases the longitudinal field strength in the drain end of the channel, the JMOS I_{SUB} is less than the conventional MOSFET impact ionization substrate current.

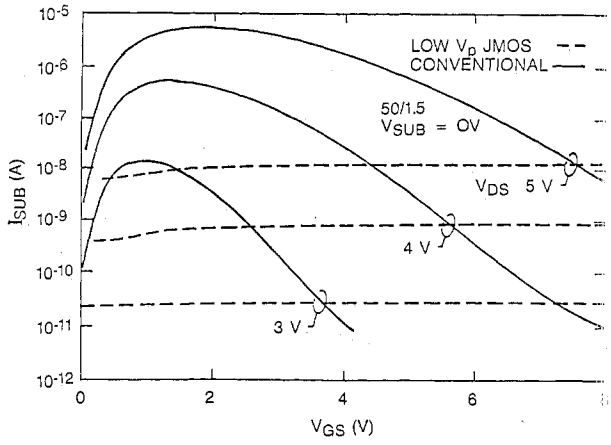

Fig. 20. Substrate current versus V_{GS} comparison for conventional (solid line) and low-V_p JMOS (dashed) at V_{DS} = 3, 4, 5 V. Drawn W = 50 μm, L = 1.5 μm for both devices. Low-V_p L_{eff} = 0.8 μm, conventional L_{eff} = 1.0 μm.

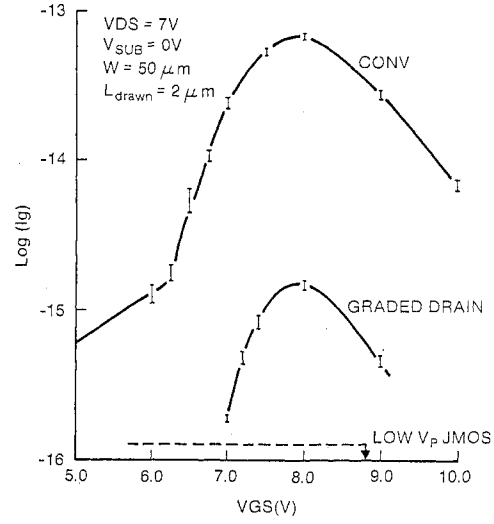

Fig. 21. Gate current versus V_{GS} comparison for conventional and low-V_p devices. Both have drawn W = 50 μm, L = 2 μm. Conventional L_{eff} = 1.5 μm, JMOS L_{eff} = 1.3 μm. V_{DS} = 7 V, V_{SUB} = 0 V. Graded S/D device with L_{eff} = 1.1 μm is also shown.

Drain diodes built on the same chip with different area/perimeter ratio confirmed that the JMOS substrate current shown in Fig. 20 is mostly p^+-n^+ sidewall diode leakage. This Zener-like drain–substrate leakage is fairly independent of channel current, hence independent of polysilicon gate length and MOSFET gate bias, and it scales with device width to a typical room temperature value of ~ 300 pA/μm at V_{DSUB} = 5 V. In JMOS designs with higher n^- and p^+ doping densities, the Zener leakage under the same conditions can increase by orders of magnitude when tunneling becomes important, to a typical maximum of ~ 500 nA/μm when both sides of the sidewall junction were degenerately doped. High sensitivity to p^+ doping levels are expected for shallow n^+(As)/p^+(boron) junctions with p^+-doping levels above 10^{18} cm^{-3} [69]. This suggests that an optimum JMOS design must pay careful attention to the p^+ doping profile in particular, if substrate current is to be minimized.

C. Gate Current

Very sensitive gate current measurements were done at the wafer level utilizing a floating-gate-induced drain current relaxation technique demonstrated in [70]. Resolution below 10^{-16} A was possible with this technique.

Gate current comparisons presented herein are for devices built side by side on the same chip, since small structural or doping variations can lead to invalid comparisons. Fig. 21 compares the gate current measured as function of V_{GS} for a conventional, and for the low-V_p JMOSFET of Fig. 16 on the same chip. The former shows the characteristic bell-shaped peak that has been attributed to lucky channel hot electrons (CHE) [7], [71], while the JMOSFET gate current is below the noise level in the measuring apparatus. This extreme reduction of the gate current in the low-V_p JMOS device can be attributed to the reduction of the internal drain voltage V_{Di} on the MOSFET due to the presence of the series JFET, even though the external V_{DS} is 7 V in this measurement. Fig. 21 also presents the gate current of the graded S/D device

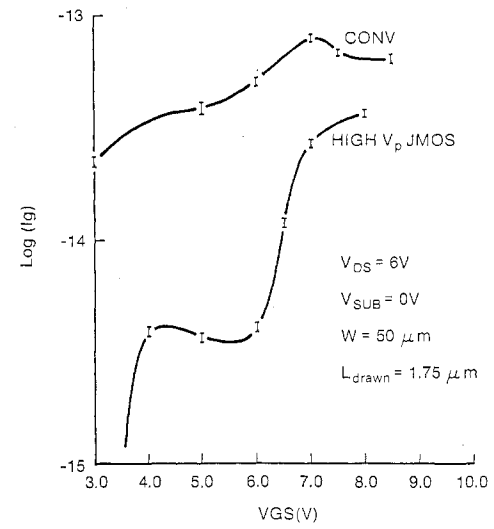

Fig. 22. Gate current versus V_{GS} comparison for conventional and high-V_p devices. Both have drawn W = 50 μm, L = 1.75 μm. Conventional L_{eff} = 1.2 μm, JMOS L_{eff} = 1.0 μm. V_{DS} = 6 V, V_{SUB} = 0 V.

on the same chip, which gives an indication of impact ionization reduction due to drain grading alone. The reduction of the JMOSFET gate current is clearly due to a reduction of V_{Di}, in addition to junction grading. This is consistent with the I–V characteristics of Fig. 16 and the substrate current characteristics of Fig. 20, which indicated that the JFET drain supported most of the drain bias and that impact ionization was negligible under the gate of the low-V_p JMOSFET, respectively.

Fig. 22 presents the gate current comparison for devices on the same chip of a high-V_p wafer, measured at V_{DS} = 6 V. Effective channel lengths are 1.25 μm for the conventional MOSFET, and 1.0 μm for the JMOSFET. In the CHE I_G peak (at $V_{GS} \sim V_{DS}$) the reduction provided by the high-V_p JMOS is relatively small. At lower gate voltages, however, where impact ionization is more in-

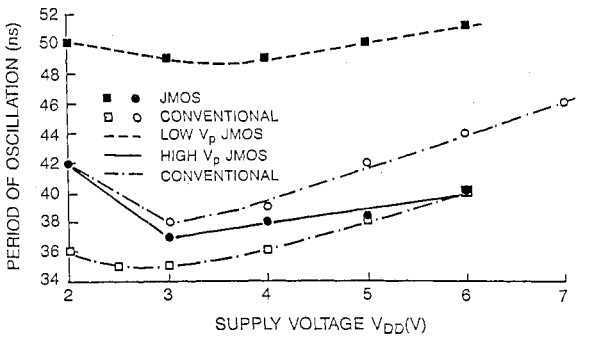

Fig. 23. E/D ring-oscillator period of oscillation versus supply voltage. Boxes (□ ■) indicate the low-V_p experiment. Circles (○ ●) indicate the high-V_p experiment.

tense in conventional devices there is about one order of magnitude reduction in I_G measured in the JMOS structure. It is clear from Figs. 21 and 22 that as the JFET pinchoff voltage is reduced, the JFET increasingly limits the overall device current but also increasingly improves the gate current due to hot carriers.

D. Speed Performance

Ring oscillators with fan-in = fan-out = 1 were built to benchmark on the same chip the speed performance of the two JMOSFET device designs against conventional designs. The 21 inverter stages were of the n-channel enhancement/depletion (E/D) type. Depletion and enhancement-mode JMOSFET's were used in the JMOS inverter stages. All ring oscillators had the same drawn geometries: (12 μm/3 μm drivers, 8 μm/8 μm loads). Fig. 23 shows the oscillation period as a function of the supply voltage for two wafers. The speed performance of the low-V_p design (dashed line) is much degraded as compared to the conventional device speed (□). This performance degradation is expected since the drive capability of the JMOS inverter stage is severely limited by the low-V_p drain JFET as shown in Fig. 16.

The high-V_p JMOS ring oscillator had a speed (solid line) comparable to the conventional design on the same chip (○). The slight speed-up for this JMOSFET design is solely attributable to the smaller L_{eff} of the transistors, (≈ 0.25 μm shorter), and it is within the wafer to wafer variation of the speed performance of the conventional devices. Usually in E/D circuits the average pull-up output current increases sublinearly with supply voltage. For this reason, the larger logic swing at larger supply voltages results in a slow down of the ring oscillator speed as V_{DD} increases, as shown in Fig. 23.

The introduction of the p^+ region in the JMOSFET drain has the positive effect of reducing the gate to n^+ drain feedback capacitance (C_{GD}) at the expense of the increasing both drain to substrate junction capacitance (C_{DSUB}) and gate to p^+ overlap/fringing capacitance (C_{GSUB}).

VI. Discussion

The JMOS structures studied have demonstrated the basic advantages of this device design. First, the maximum effective MOSFET drain bias can be set by device design, independently of the maximum externally applied drain and gate bias that can be set at effectively higher voltages. This property is advantageous in view of the pressing need for voltage reduction in conventional submicrometer MOSFET's brought on by hot-carrier effects. Second, the JMOSFET lightly doped drain region can be engineered without the usual reliability constraint imposed on conventional LDDFET's due to hot-carrier injection under the sidewall; reliable LDDFET's require $N_S > 10^{18}$ cm^{-3} in the n^- region, while the buried n^- region in the JMOSFET can be more lightly doped to meet the designer's choice for JFET V_p. Third, the advantages in channel longitudinal field reduction due to drain junction grading that are common to all LDD-like structures previously studied, are also present in the JMOSFET with the additional advantage of having the channel current driven away from the SiO_2 interface in the high-field drain region. All three features combined allow further minimization of charge injection, trapping, and instabilities associated with the gate oxide. Based on the proven correlation between gate and substrate currents and device reliability found in both conventional and LDD-like devices, we expect submicrometer JMOSFET's to have good endurance under hot-carrier stress.

Our implementations of the JMOSFET have pointed to areas that merit further improvement. First, the breakdown voltage of the sidewall n^+-p^+ junction at 6.5 V and the associated junction leakage seen at 5 V render the drain-to-substrate leakage unacceptable for dynamic circuit applications. The use of a phosphorus n^+ region self-aligned to the sidewall oxide or a slight (≈ 0.2 μm) anisotropic silicon etch-back prior to arsenic n^+ implant in order to grade or eliminate the n^+-p^+ sidewall junction are possible technology implementations that can overcome this shortcoming. Second, a symmetrical JMOSFET suffers from a further effective transconductance decrease due to an increase in series source resistance (R_S), since

$$g_{m_{\text{sym}}} = \frac{g_{mJ}}{1 + g_{mJ} R_S} \tag{6}$$

where g_{mJ} and $g_{m_{\text{sym}}}$ are the JMOSFET and symmetrical JMOSFET effective transconductances, respectively. This likely means that an extra mask must be used to eliminate the p^+ region on the source side. Third, process complexity and control are relevant issues in the comparison of the JMOSFET and more conventional designs. The presence of a self-aligned active device under the oxide spacer that controls the current drive of the JMOSFET makes oxide spacer process control even more necessary. The addition of at least one extra masking step with worst case alignment tolerance of $L_{\text{gate}}/2$ is one additional drawback of the JMOSFET in its asymmetric implementation.

VII. Conclusions

The JMOSFET, a modified LDD device structure has been proposed, designed, modeled, and experimentally

demonstrated. It provides designers with tradeoffs in performance somewhat different than LDD devices previously reported. The JMOS device can be optimized for a given technology choice of minimum effective channel length, oxide thickness, and supply voltage. It overcomes some of the reliability problems of LDD devices with peak doping densities below 1×10^{18} cm^{-3} related to injection into the sidewall oxide. By keeping the longitudinal E-field peak away from the SiO_2–Si interface, the JMOSFET structure minimizes hot-carrier injection into the oxide—as made evident through gate and substrate current characteristics—and should minimize also the reliability problems associated with that injection. The particular experimental devices described here show that the JMOS can be designed to virtually eliminate gate current, at a substantial cost in performance, or to moderately reduce gate current at a minimal cost in performance, compared to conventional devices. Our results suggest that with proper optimization of the drain JFET this new structure can perform well in VLSI applications, while maintaining its hot-carrier-resistant properties in submicron 5-V supply circuits. Further work is needed, however, to demonstrate quantitatively the trade-offs that exist in circuit performance and reliability. As has been the case with all LDD-like structures, improved device reliability has been achieved at some expense in performance. However, the advantages of keeping 5-V operation in micron sized devices can outweigh this performance loss.

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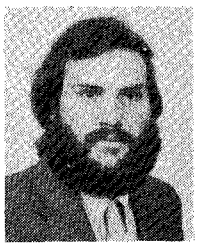

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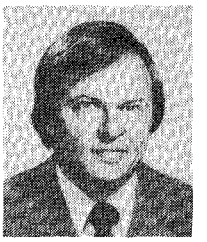

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