UNIVERSIDADE FEDERAL DO RIO GRANDE DO SUL
DEPARTMENT OF ELECTRICAL ENGINEERING
UNDERGRADUATE PROGRAM IN ELECTRICAL ENGINEERING

PAULO RICARDO KLAUDAT NETO

Compact Models based on Memristive Devices for In-Memory Computing

Work presented in partial fulfillment of the requirements for the Engineering degree in Electrical Engineering

Advisor: Prof. Dr. Raphael Martins Brum

Porto Alegre
November 2022

“Do the difficult things while they are easy,
and do the great things while they are small.
A journey of a thousand miles begins with a single step.”
— Sir Lao Tzu

ACKNOWLEDGEMENTS

I would like to express my deepest gratitude to my supervisor, Dr. Raphael Brum, for your patience, guidance, and support. I was significantly benefited from your wealth of knowledge during the time as a research assistant, where I learned many things I am proud of in this degree. Also, to Dr. Gilson Wirth, who is a great source of inspiration. Thank you to my parents for your endless support in making it possible, and I extend these acknowledgments to my family and friends that I left after entering this stage in my career.

ABSTRACT

The recent development of non-volatile memory technologies based on memristive devices has triggered new concepts of design, which were otherwise inconceivable. Hybrid technology, including CMOS plus magnetic materials, may circumvent the limits presented by pure technologies and von Neumann-based architectures. In this context, this work aimed to introduce and explore different compact designs that realize the memristor device using golden standard circuit simulation tools. For this purpose, the models were ported to Spectre simulator, and *Python* scripts were developed to treat the output data. The different technologies of memristors were presented, and their suitability with CMOS integration to realize logical computation in NVM crossbar arrays, which is intended for the in-memory computing.

Keywords: Memristor, STT, SPICE, In-Memory Computing, Imply.

RESUMO

O desenvolvimento recente de tecnologias de memória não voláteis baseadas em dispositivos memristivos desencadeou novos conceitos de projeto, que de outra forma seriam inconcebíveis. Tecnologias híbridas, que por sua vez, incluem CMOS e materiais magnéticos, podem contornar os limites apresentados por tecnologias puras e arquiteturas baseadas em von Neumann. Nesse contexto, este trabalho teve como objetivo apresentar e explorar diferentes projetos compactos que realizam o dispositivo memristor usando ferramentas de simulação de circuitos padrão ouro. Para isso, os modelos foram portados para o simulador Spectre e foram desenvolvidos scripts *Python* para tratar os dados de saída. As diferentes tecnologias de memristores foram apresentadas e sua adequação com a tecnologia CMOS para realizar computação em memória.

Palavras-chave: Memristor, STT, SPICE, computação em memória, implicação material.

LIST OF ABBREVIATIONS AND ACRONYMS

MTJ	Magnetic Tunnel Junction
MRAM	Magnetic Random Access Memory
TMR	Tunneling Magnetoresistance
STT	Spin Transfer Torque
ReRAM	Resistive Random Access Memory
FeRAM	Ferroelectric Random Access Memory
SPICE	Simulation Program with Integrated Circuit Emphasis
CIM	Compute In-Memory
IMTJ	In-Plane Magnetic Tunnel Junction
PMTJ	Perpendicular Magnetic Tunnel Junction
MR	Magnetoresistance
GMR	Giant Magnetoresistance
LRS	Low Resistance State
HRS	High Resistance State
LLG	Landau Lifshitz Gilbert
HP	Hewlett Packard
IC	Integrated Circuits
NoC	Network On Chip
WER	Write Error Rate
FM	Ferromagnetic
IN	Insulator
DNN	Deep Neural Networks
MIM	Metal/Insulator/Metal
VCMA	Voltage-Controlled Magnetic Anisotropy

IP	In-Plane
TS	Thermal-Switching
BE	Bottom-Electrode

LIST OF FIGURES

LIST OF TABLES

CONTENTS

1 INTRODUCTION

During the last few years, the miniaturization of daily technologies has attracted a great deal of attention worldwide. The growth of microelectronics allowed for the development of new applications that would otherwise be inconceivable, applications that are essential in daily life, such as smartphones, laptops, home automation devices, and others.

As a part of this development, memory research has been a challenge. These new applications require a lot of data processing; therefore, new memory designs increasingly need a higher performance in speed, power consumption, and densities. The Complementary Metal Oxide Semiconductor technology (CMOS) is steadily improving. However, it admitted that we would meet some physical limits within a few years.

New emerging applications, such as big data and internet-of-things (IoT), are extremely demanding for computing purposes. Their requirements have been difficult to fulfill with current CMOS-based computer architectures, even at the device level. Based on von Neumann architectures, conventional computers separate computing and memory units. As a result, the performance, especially the energy speed efficiency, is limited. To break the so-called "von Neumann bottleneck," it is necessary to integrate memory and computing functionalities in the same physical location.

Hybrid technology, which includes magnetic materials inside the CMOS process, like memristive devices, may circumvent a part of these limits and meet the analog behavior present in the new approach of computing, that is, in-memory computing. In addition, these emerging technologies are candidates for high-tier memory devices. They combine the best of both worlds: *i.e.,* cheap with non-volatile, and fast access with high-density information storage.

This work presents an overview of memristor topologies, switching mechanisms, and potential applications. A performance comparison is evaluated among different types of memristor devices, such as spintronic and resistive, given through an analysis of SPICE models. This work also analyzes the main characteristics, which are useful to compute in-memory architectures, using several compact models that realize the memristive technology described in the literature. This approach aims at the physical/electrical model investigation and technical detailing.

2 BASIC CONCEPTS

This section overviews the fundamental physical concepts for different families of memristor devices.

2.1 Magnetic Materials

Magnetic materials are classified based on their response to an externally applied magnetic field, revealed by their susceptibility and permeability. Magnetic susceptibility is the ratio of magnetization M over the applied magnetic field H, which describes the material magnetization response in the applied field. The permeability μ is defined as the magnetic induction B ratio over the applied magnetic field, which shows the ability to support the formation of magnetic fields within itself. When magnetic materials have a negative susceptibility, they are called diamagnetic, whereas materials with a positive susceptibility are called paramagnetic (JI, 2013).

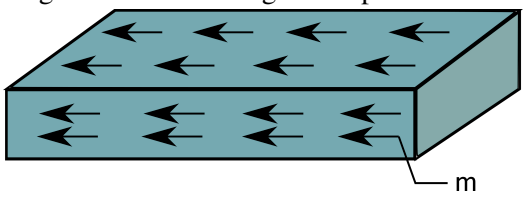
The individual magnetic moments in diamagnetic materials are magnetized oppositely under the application of an external magnetic field. It results in magnetization in the opposite direction, and its permeability is less than 1. In the absence of an external field, they do not exhibit magnetization. Thus, the total magnetization is null.

Paramagnetic materials have the resulting magnetization null lacking the presence of external magnetic fields. However, in the presence of an external field, each magnetic moment aligns along the direction of the field. This effect results in a parallel magnetization proportional to the external field's magnitude. Typically, the relative permeability is slightly bigger than 1.

The ferromagnetic materials (FM) present a net magnetization, even without external fields. Each magnetic moment tends to align parallel to the applied field when an external field is applied. Their permeability is related to the magnetic field strength and also self-magnetization. Thus the magnetization within the layer is not stationary. This behavior leads to a hysteresis loop in the $H \times M$ curve.

Typical ferromagnetic exhibits high susceptibility to the order of 10^6 and increasingly the external magnetic field. These materials reach their magnetic saturation, so the ferromagnetic can be magnetized to a determined limit. There are two critical elements of FM materials; the first one is the Curie temperature: such temperature acts like a threshold, determining the temperature at which the magnetization can disappear T_c. The

Figure 2.1 – Ferromagnetism phenomenon.



Source: Author.

second one is the magnetic domains: below the T_c, the FM materials are spontaneously divided into many small regions, and the magnetization within these small portions has a uniform direction. However, the relative magnetization direction between each other domain points may follow in different directions, depending on the shape of the material. This arrangement is known as magnetic anisotropy.

The directional preference of magnetic moments in magnetic materials permits a spontaneous self-alignment of magnetization along a particular direction. This direction is named the easy axis of magnetization. The other opposite directions along the easy axis are equivalent, and the magnetization can be along either of them due to the symmetry-breaking effect.

There are different sources of anisotropy property. One of them is the magneto crystalline anisotropy, in which the material rearrangement occurs due to a variety of magnetic behaviors along the crystallographic directions. The other is polycrystalline, in which the shape is organized due to the asymmetry of the demagnetizing field, when it is not completely spherical. Another source is magnetoelastic anisotropy, related to the tension variation and the exchange interaction between ferromagnetic and antiferromagnetic layers.

2.1.1 Demagnetizing Field

The demagnetizing field is the magnetic field generated by the magnetization of the magnetic material. This field is oriented toward the opposite direction of the magnetization, reducing the total magnetic moment. The magnetoelastic energy associated with the demagnetizing field depends on the distance of the magnetic poles, which is minimized during the division into magnetic domains.

For complicated geometries of thin films, the demagnetizing field cannot be calculated analytically (TANG; LEE, 2010). For a given geometry, the magnitude of demagne-

tizing field increases as the saturation magnetization increases, as shown below.

$$H_D = M_s N \tag{2.1}$$

Where N is the demagnetizing factor, which is computed along the three coordinates.

$$N = N_x + N_y + N_z \tag{2.2}$$

This relationship concludes that this field mainly depends on the film's shape and magnetization direction.

In the case of an elliptic-shaped film with a uniform distribution of magnetization, the demagnetizing field is also uniform (TANG; LEE, 2010). Therefore, in a thin film, in which the thickness t is significantly smaller than the length a and width b, the demagnetizing field is approximated to the Equations 2.3, 2.4 and 2.5.

$$N_a = \frac{4t}{\pi a} \cdot \left[1 - \frac{1}{4}\frac{a-b}{a} - \frac{3}{16}(\frac{a-b}{a})^2\right] \tag{2.3}$$

$$N_a = \frac{4t}{\pi a} \cdot \left[1 + \frac{5}{4}\frac{a-b}{a} + \frac{21}{16}(\frac{a-b}{a})^2\right] \tag{2.4}$$

$$N_c = 1 - N_a - N_b \tag{2.5}$$

For a circular layer ($a = b$) and $N_a = N_b = 1$, the shape does not introduce a preferred direction to the magnetization. When the ratio between the length and width is larger, the demagnetizing field is larger along the smaller axis. Thus, the shape, in addition to the crystalline anisotropy, affects the magnetization direction, providing a "shape anisotropy" to the magnetization.

This shape anisotropy is a relevant feature in the design of magnetic devices. It admitted that the neighboring produce overlapping fields for small arrays of cells close to each other. Therefore, fields in the same direction partially cancel the demagnetizing field from the air. Oppositely, this field is enhanced when the fields of neighboring cells are in opposite directions.

2.1.2 Magnetoresistance

Magnetoresistance (MR) is the change of electrical resistance in magnetoresistive materials due to the presence of external magnetic fields. The first MR discovered, called Anisotropic Magnetoresistance, is tied to the anisotropic scattering of electrons. This effect occurs due to the spin-orbit interaction between the applied magnetic field and the electric current density. An AMR device reaches its maximum resistance when the electric current aligns in parallel with the magnetic field, whereas it reaches the minimum resistance when the relative direction is perpendicular. The AMR ratio is given as a function of the electrical resistances as follows below:

$$AMR = \frac{R_{\parallel} - R_{\perp}}{\frac{1}{3}R_{\parallel} + \frac{2}{3}R_{\perp}} \times 100\%, \tag{2.6}$$

Where $R_{\parallel}$ is the resistance when the magnetic field is parallel to the current direction, and $R_{\perp}$ is the resistance when it is perpendicular.

The MR has been explored in a variety of applications related to magnetic sensors, where higher MR is usually desired. In past decades, other forms of MR were discovered with higher resistance than AMR, such as GMR and TMR. Giant Magnetoresistance (GMR) was discovered using thin films of ferromagnetic layers separated by non-magnetic conductive materials like Cr.

When a current passes through a GMR device, the scattering effect leads to the spin-polarized current. When the two FM layers have the magnetization aligned in parallel, this current can easily pass beyond both layers, resulting in a lower resistance. Oppositely, the alignment in antiparallel results in higher electrical resistance. The GMR ratio can be measured according to the differences in the resistances values in parallel and antiparallel states, as shown below:

$$GMR = \frac{R_{AP} - R_P}{R_P} \times 100\%, \tag{2.7}$$

Here, R_{AP} and R_P are the resistances in antiparallel and parallel configurations. The values observed in GMR qualified their use in biosensors and hard disk driver applications (JI, 2013).

2.2 Memristors

The memristor, known as the fourth fundamental circuit element (MLADENOV, 2014), was discovered by Leon Chua from the University of California, Berkeley, in 1971. From his standpoint, a memristor was a two-terminal device with a non-linear relationship between electric charge and magnetic flux. In addition, its resistance is susceptible to variation depending on the amount of charge that flows through the device. This relationship is described mathematically in the following equation:

$$d\phi = Mdq, \tag{2.8}$$

where M is a property equivalent to the electrical resistance, termed memristance. This generalized perspective of memristive systems highlighted that they strongly depend on their given state. Nevertheless, still being susceptible to variation.

The first proposed topology used operational amplifiers and discrete non-linear resistors to build the memristive function. However, this device was bulky while active due to the power supply.

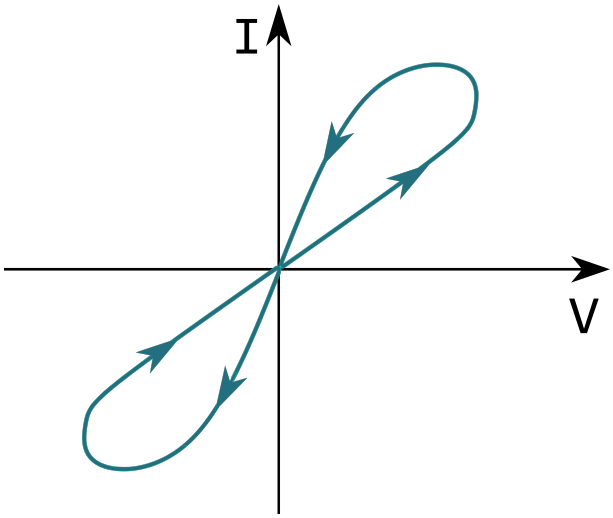
In 2008, Strukov and other researchers proposed a nanoscale TiO_2 device model to implement the memristive behavior theoretically. This factor started a massive wave of research in this field (STRUKOV et al., 2008). Behind this scene, the memristor concept was extended due to a variety of systems, including unipolar, bipolar resistive switches, magnetic spin-torque transfer devices, and phase-change memories. Chua has expanded the scope to any two-terminal device that exhibits a pinched hysteresis loop in the v-i plane when the device is driven by a bipolar periodic current or voltage waveform.

Thereafter the standard attribute to define a device as a memristor became its current-voltage curve shape, depicted by the hysteresis loop, as shown in the figure below.

2.2.1 Resistive Memristor

Resistive materials have been widely utilized in resistive random access memories (ReRAM). The storage function observed in ReRAM occurs according to the intrinsic physical behavior called resistive switching. Following this behavior, the resistive material is susceptible to switching between a low resistance state (LRS) and a high resistance state (HRS).

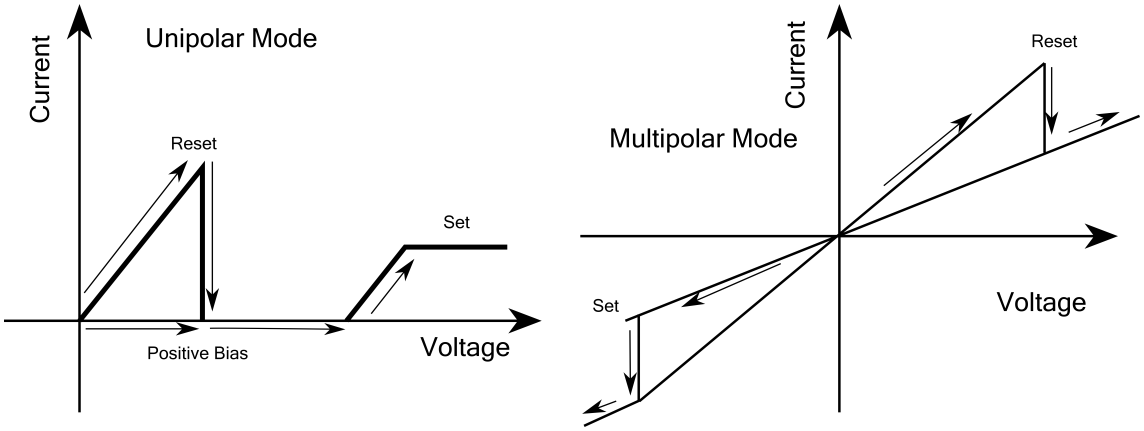
Figure 2.2 – Typical hysteresis loop of a memristive device.



Source: Author.

Usually, the switching voltage is named V_{SET} when the resistance turn from HRS to LRS, and changing from LRS to HRS, the required voltage is called V_{RESET}. In most cases, the current arising from the voltage applied is restricted to the region with higher conductance in the 'SET' process, whereas it is uniform through the 'RESET'. There are usually two switching modes in bistable resistive materials: unipolar switching, and bipolar switching, as shown in Figure 2.3.

Figure 2.3 – Switching modes of bistable resistive materials.



Source: Author.

The unipolar switching is independent of voltage or current polarity. Therefore, the 'SET' and 'RESET' states are achieved with the same polarity, whereas the multipolar mode requires a different polarity to perform the switching processes properly. The curves presented in multipolar mode clearly show that the resistive material, when operated in the bipolar switching, exhibits a hysteresis loop typical of memristors.

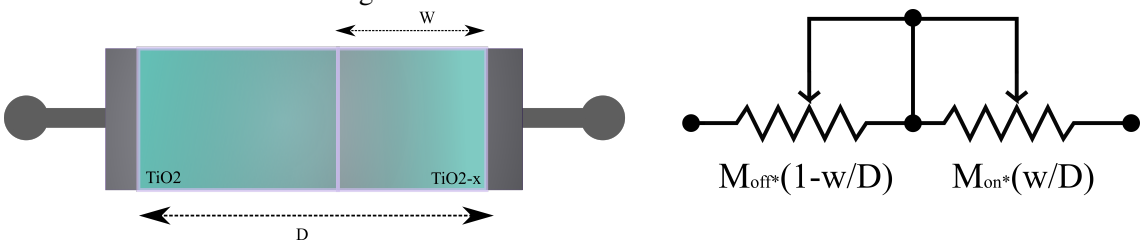
Some efforts in the research and development field have been dedicated to real-

ize the memristor using resistive materials, such as T_iO_2, Z_nO, and TaO_x, in typical architectures that consist of two metals sandwiching an insulator, usually called as MIM.

2.2.1.1 Titanium Dioxide Memristors

Titanium dioxide-based memristors are the most popular used structure. It consists of two TiO_2 layers between two platinum electrodes. One of these layers has missing oxygen, called the doped region $TiO_2{-}x$, and the other layer, which is pure, is the undoped region, as shown in Fig. 2.4.

Figure 2.4 – HP TiO2 Memristor Model.



Source: Author.

A positive voltage on the device repels the oxygen deficiencies in the metallic doped region (positive), sending them into the pure region. The boundary caused by the oxygen movement between the two layers increases the percentage of conductivity of the entire device (DUAN et al., 2014).

This device's conductivity becomes higher as the positive applied voltage gets high values. Oppositely, a negative voltage decreases the conductivity of the device. As a result, the total memristance of a TiO_2 memristor follows the math model presented below:

$$M(t) = M_{on}x(t) + M_{off}(1 - x(t)), \tag{2.9}$$

where

$$x(t) = \frac{w(t)}{D} \in [0, 1]. \tag{2.10}$$

Here, D specifies the TiO_2's thickness, w(t) is the doped region, M_{on} and M_{off} are the memristance for each region within x(t) = 0 and x(t) = 1, respectively. In addition, the entire device also obeys Ohm's Law. Thus, the applied voltage is the product between the electric current and the memristance, as follows below.

$$v(t) = M(t) \cdot i(t), \tag{2.11}$$

Many suggested mechanism based on T_iO_2 devices have been proposed (STRUKOV et al., 2008). The most popular suggested mechanisms are separated into two groups: ionic and thermal.

2.2.1.2 Ionic Migration

The ionic mechanism involves the migration of oxygen vacancies. This movement creates auto-doped phases, metallically conducting for the device, depending on the undoped region size. The oxygen ions may combine at the anode and evolve O_2 gas.

This phenomenon has been seen in ReRAM (GALE, 2014), and most physical models reproduce the flow of oxygen vacancies, as described in the previous subsection, which suggests that the switching occurs due to ionic motion rather than charge trapping. In addition, a mixed mechanism has been reported in the literature, which involves the oxygen vacancy assisted by thermal effect (BORGHETTI et al., 2009).

2.2.1.3 Thermal Effect

T_iO_2 atomic deposition thin films can form conducting filaments as extended defects along grain boundaries (GALE, 2014). The ions flow can form a path that breaks with excess heat (i.e., when a high voltage is applied). When the Joule heating exceeds a specific value, the thermal effect may lead to the rupture of filaments and even change the structure of MIM. This mechanism occurs for both HRS and LRS changes, known as thermal switching (TS).

The thermal dissipation in the electrode can also influence the switching behavior. The literature shows that for the bottom electrode (BE), for a thickness smaller than 30 nm, in $P_t/N_iO_2/P_t$ structures, the switching behavior especially changes from resistive switching to thermal switching (WANG et al., 2020). In this case, the heat dissipation is decreased as the BE is thinner, and thus the conductive filaments are easily ruptured.

2.2.2 Spin-based Memristors

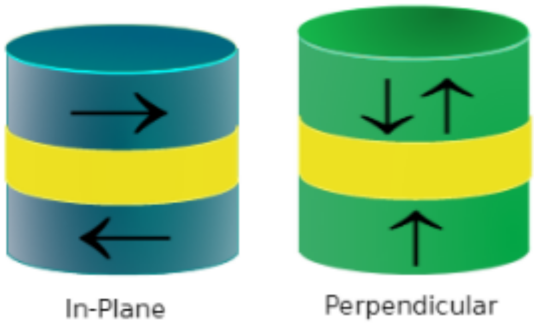
These types are based on nanostructured devices within the field of magneto electronics or spin electronics, called spintronics. The experimental observation of tunable magnetoresistance is intimately connected to spin motion. This effect moves the magnetic domain to separate the polarities in multilayered ferromagnetic films. A typical example

of a spin-based memristor is the Magnetic Tunnel Junctions (WANG et al., 2015).

2.2.2.1 Magnetic Tunnel Junctions

The standard Magnetic Tunnel Junction (MTJ) is composed of two ferromagnetic layers: one has a large coercive field, and the other is susceptible to external magnetic fields, called the easy axis, which can be easily rotated. The parallel or antiparallel alignment of magnetization results in an electrical resistance variation. Two popular FM materials used within an MTJ are in-plane MTJ (IMTJ) and out-of-plane or perpendicular MTJ (PMTJ). Usually, IMTJs are elliptical structures where the magnetization stays along the long axis (x-y plane). In contrast, the PTMJs, are cylindrical structures, as depicted in Figure 2.5.

Figure 2.5 – Magnetic Tunnel Junctions.



Source: Author.

When the magnetization of both FM layers is aligned (i.e., the parallel mode), the MTJ reaches the highest conductance or the lowest electrical resistance. Oppositely, when the relative magnetization is in a different direction (i.e., the antiparallel mode), the MTJ reaches the lowest conductance. In addition, a quantum tunneling effect may arise when the insulator is ultra-thin, like a few nanometers. This phenomenon allows electrons to transfer from one of the layers to the other.

MTJs are also MR devices. However, they comprehend a higher MR ratio than other MR devices. This high ratio occurs due to the tunneling effect phenomena called Tunneling Magnetoresistance. Usually, this effect is measured in terms of resistance variation or the polarization factor of FM layers, using the following equation (TANG; LEE, 2010).

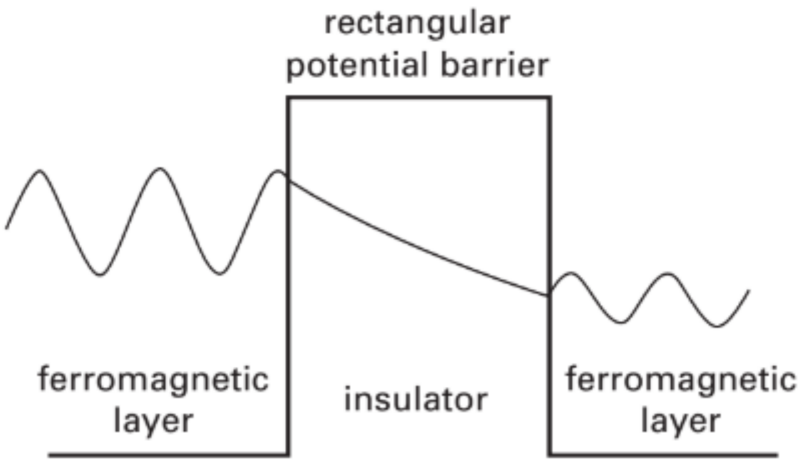
$$TMR = \frac{\Delta R_p}{R_p} = \frac{R_{ap} - R_p}{Rp} = \frac{2P_1P_2}{1 - P_1P_2}, \tag{2.12}$$

Where the R_{ap} is the electrical resistance in antiparallel mode and R_p is the resistance in parallel mode. P_1 and P_2 are the spin polarization factor for each ferromagnetic layers. Nowadays, the TMR ratio of a FM/I/FM junction with a M_gO barrier is larger than 300% (TANG; LEE, 2010).

2.2.2.2 Slonczewski Model

In 1989, Slonczewski proposed a theory to analyze the spin polarized movement through a tunneling barrier, this theory aimed to have a better measurement of FM/I/FM conductance in terms of spin polarized electrons TANG; LEE. Considering the FM layers are identical, the insulator (tunnel) is represented by a rectangular potential barrier, which is depicted in the figure below.

Figure 2.6 – Potential barrier in a FM/I/FM structure and wave function of tunneling electron.



Source: Tang and Lee (2010).

Moreover, using the free-electron model and Schrödinger equation to achieve the conductance as a function of the relative position of the magnetization vector. The conductance model is shown below.

$$G(\theta) = G_0(1 + P_F^2 \cos\theta) \tag{2.13}$$

The parameter G_0 is the average conductance over θ (mean surface conductance and independent of θ). P_F is the polarization factor in terms of the effective spin polarization, given by:

$$P_F = \frac{k_\uparrow - k_\downarrow k^2 - k_\uparrow k_\downarrow}{k_\uparrow + k_\downarrow k^2 + k_\uparrow k_\downarrow} \tag{2.14}$$

Where $k_\uparrow$ is the Fermi wave vector in the up-spin band, and $k_\downarrow$ in the down-spin band in the barrier. The absolute value of k is determined by the potential barrier V_b, and E_F is the Fermi energy.

$$k = \frac{1}{\hbar}\sqrt{2m(V_b - E_F)} \tag{2.15}$$

The TMR decreases as the potential barrier presents low values. From that perspective, Slonczewski's theory concluded that conductance is not only a property of FM, but also depends on the insulator's quality.

Consider two identical FM layers ($P_1 = P_2$) and the two states of MTJ, antiparallel and parallel, nominally associated with $\theta = 0^o$ and $\theta = 180^o$. It is possible to measure the magnetoresistance in terms of spin-up and spin-down quantities using the Julliere and Slonczewski model, as shown below.

$$TMR = \frac{2P_1P_2}{1 - P_1P_2} = \frac{2P^2}{1 - P^2} \tag{2.16}$$

2.2.2.3 Spin Dynamics

Due to the multipolar state in MTJs, magnet orientation has an essential role in data storage. However, the magnetization course is complicated. One of the valuable resources to comprehend the spin activity is the Landau-Lifshitz Gilbert equation, which describes the dynamic spin motion based on the macroscopic extension of the spin Hamiltonian (TANG; LEE, 2010), written as follows:

$$\frac{\partial\overrightarrow{M}}{\partial t} = -\gamma\mu_0\overrightarrow{M}\times\overrightarrow{H}_{eff} + \frac{\alpha}{M_{sat}}\overrightarrow{M}\times\frac{\partial\overrightarrow{M}}{\partial t} - \frac{\nu}{M_{sat}^2}\overrightarrow{M}\times(\overrightarrow{M}\times\jmath.\nabla\overrightarrow{M}) - \frac{\xi\nu}{M_{sat}}\overrightarrow{M}\times\jmath.\nabla\overrightarrow{M} \tag{2.17}$$

Here, $\overrightarrow{M}$ is the material's magnetization. $\overrightarrow{H}_{eff}$ is the effective magnetic field, α is the damping factor, μ_0 is the vacuum permeability, and M_{sat} is the saturation magnetization. The gyromagnetic factor γ is given in terms of the Bohr magneton constant μ_B, and the Landré factor g, which is approximately 2 for almost all magnetic materials, as shown:

$$\gamma = \frac{g\cdot\mu_B}{\hbar}, \tag{2.18}$$

The term $\jmath\cdot\nabla$ is the derivative along the current direction. ξ is the non-adiabaticity degree, and ν follows below:

$$\nu = \frac{Pj\mu_B}{eM_{sat}(1+\xi^2)}, \tag{2.19}$$

This time-dependent vector $\overrightarrow{M}$ couples three essential elements of spin motion: the precession, damping process, and spin torque.

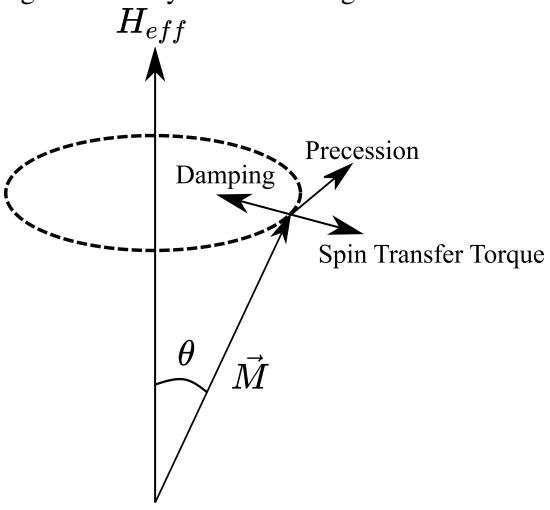
$$\mu_0\overrightarrow{M} \times \overrightarrow{H_{eff}} \rightarrow Precession \tag{2.20}$$

$$\frac{\alpha}{M_{sat}}\overrightarrow{M} \times \frac{\partial\overrightarrow{M}}{\partial t} \rightarrow Damping \tag{2.21}$$

$$\frac{\nu}{M_{sat}^2}\overrightarrow{M} \times (\overrightarrow{M} \times \jmath.\nabla\overrightarrow{M}) - \frac{\xi\nu}{M_{sat}}\overrightarrow{M} \times \jmath.\nabla\overrightarrow{M} \rightarrow STT \tag{2.22}$$

The first term $\mu_0\overrightarrow{M} \times \overrightarrow{H_{eff}}$ represents the spin-field interaction, which promotes the torque emanated from Zeeman energy. It tends to align the magnetization direction with the effective field, resulting in a precessional motion of $\overrightarrow{M}$ around $\overrightarrow{H_{eff}}$. The damping term, that is $\frac{\alpha}{M_{sat}}\overrightarrow{M} \times \frac{\partial\overrightarrow{M}}{\partial t}$, describes the energy loss of the magnetization precession around the applied field by the damping constant α. The last terms include the non-adiabaticity circumstance and the spin-transfer torque effect.

Figure 2.7 – Dynamics of Magnetization Vector.



Source: Author.

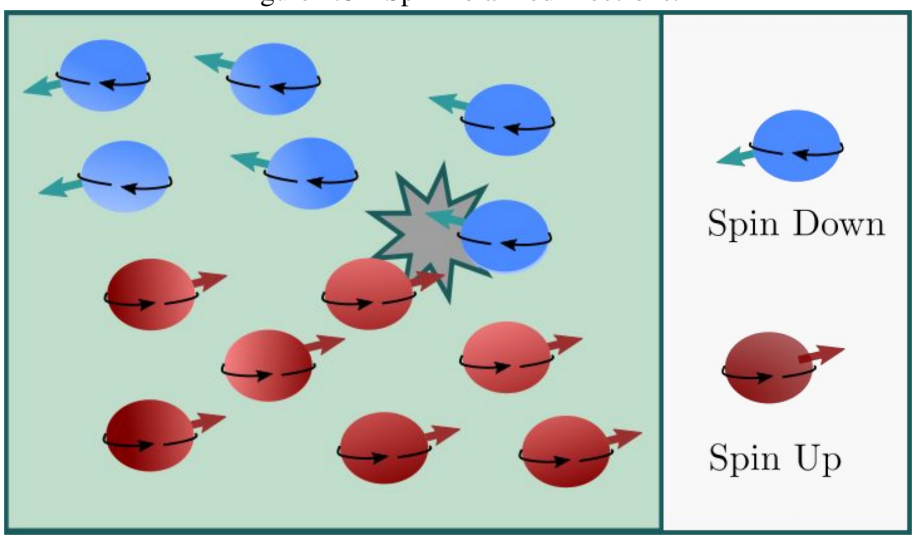
According to the LLG, the magnetization vector precesses around the effective field while it damps toward itself as shown in Fig 2.7, and in the stable state, $\overrightarrow{M}$ is aligned with H_{eff}.

2.2.2.4 Spin Torque

Slonczewski stated that, in ferromagnetic multi-layers, the charge carriers, such as electrons, have properties defined as spins with a small quantity of angular momentum. These carriers contain portions of spin-up and spin-down electrons, as illustrated in Figure 2.8.

When a spin-polarized current, i.e., a carrier with more spins of one type, travels directly beyond a thick ferromagnetic layer to the thinner magnetic free layer. The angular momentum promotes exciting oscillations, even the magnet flipping. As a result, a torque is applied to the magnetization caused by the angular momentum conservation, a phenomenon called Spin Transfer Torque (STT).

Figure 2.8 – Spin Polarized Electrons.



Source: Author.

The sum of applied torques on the magnetization layers is the rate of changes in the angular momentum of electrons. The angular momentum of each electron is equal to $\hbar/2$ when the spin is in the direction of magnetic moment (spin-up) and $-\hbar/2$ when the electron is against (spin-down). Therefore, the rate of total angular momentum through the magnetic layer due to current $\overrightarrow{I}$ is proportional to $\hbar I/(2e)$.

2.3 Memristor-based Logic

As previously mentioned, memristors provide an opportunity to supply the limits we meet in pure CMOS technology. They have the capabilities to adapt to specific applications, even to fulfill digital designs based on logic operations. Many design styles

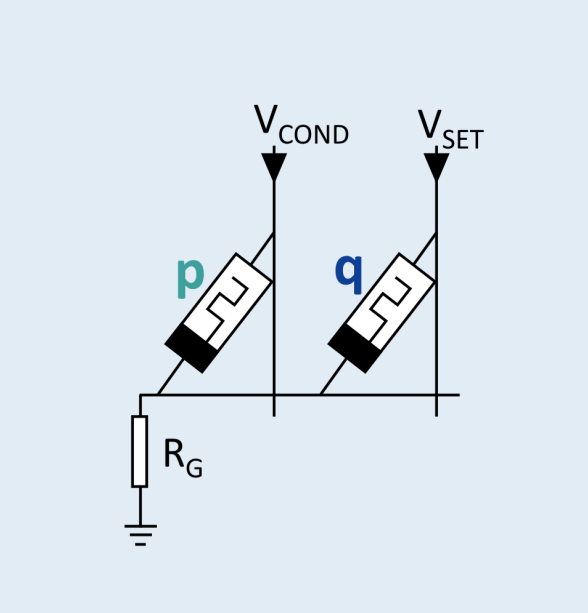
in this field have been reported. They show the memristor device in memory designs from a different perspective, not only for storage purposes but for logic computation.

Regarding that different perspective, the literature presents the Memristor Rationed Logic (MRL), which implements memristors and CMOS transistors to realize combinational blocks; the Material Implication (IMPLY) and Memristor Aided Logic (MAGIC), which are intended for in-memory computing (ALI, 2020). This section covers the fundamentals of the last two designs.

2.3.1 IMPLY – Material Implication

Imply is a type of memristive logic, where the states R_{ON} and R_{OFF} represent logic '1' and '0', respectively. It assumed that the memristor holds the logical states p and q, and a reference resistance known as R_G, must have the absolute resistance between the two logical states. The standard cell of IMPLY using memristors is depicted in Figure 2.9.

Figure 2.9 – Schematic memristor-based IMPLY.



Source: Ali (2020).

Table 2.1 – IMPLY Logic.

p	**q**	**p → q**
0	0	1
0	1	1
1	0	0
1	1	1

Source: Author.

Three voltage levels V_{SET},V_{COND}, and V_{CLEAR} control the gate. When V_{SET} and V_{COND} are applied simultaneously, the IMPLY occurs ($p \rightarrow q$). This execution leads to the truth table 2.1. Thus, the value $\overline{p} + q$ is written as an output into the memristor q (ALI, 2020).

Typically, the read and compute mechanisms take place via a separated CMOS circuit, and the standard IMPLY cell needs to meet the following requirements:

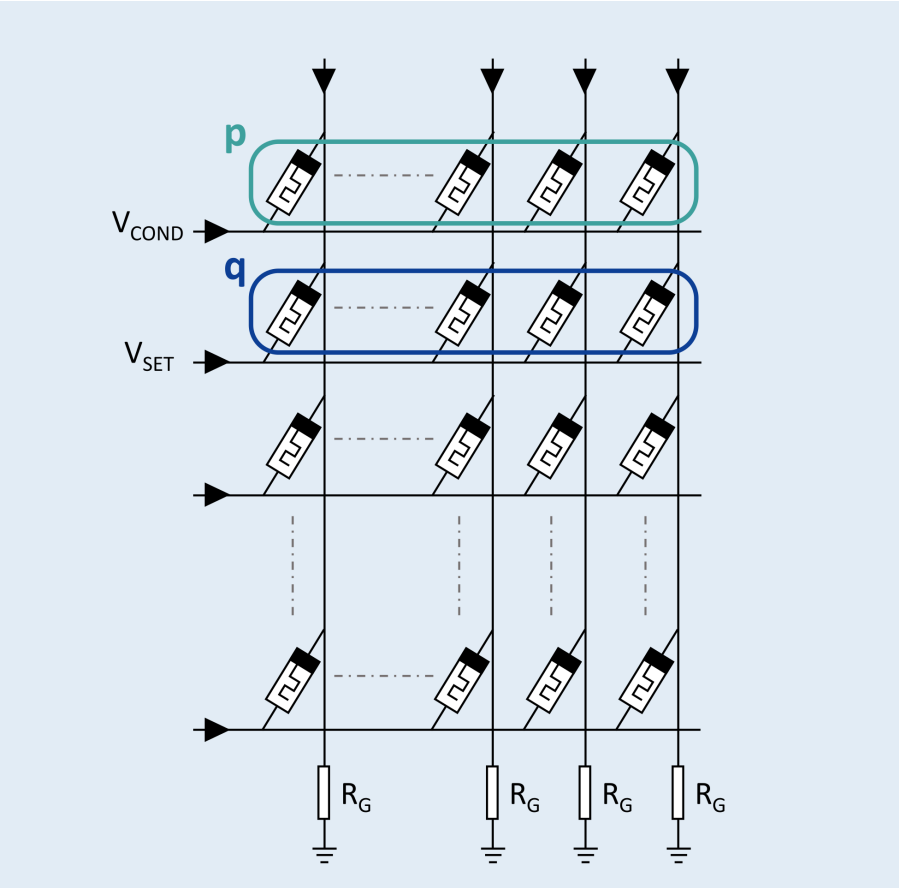
$$R_{ON} < R_G < R_{OFF} \tag{2.23}$$

$$V_{SET} - V_{COND} < V_{CLEAR} \tag{2.24}$$

$$V_{COND} < V_{CLEAR} < V_{SET} \tag{2.25}$$

Where V_{CLEAR} is the minimum value required to turn on/off the memristor's state. In NVM crossbar arrays, p and q are the states of memristors in the same row or column within the array. The control voltages V_{SET} and V_{COND} are applied to the word lines, whereas the bit line is attached to R_G as shown below.

Figure 2.10 – NVM crossbar-based IMPLY.



Source: Ali (2020).

This logic family can extend to perform additional logic functions. As $p \rightarrow q$ is the same as the boolean operation: $\bar{p} + q$. Borghetti et al. (2010) reported that a NAND operation is also feasible, and (KVATINSKY et al., 2013) shows that the other primitive boolean functions such as NAND, OR, and XOR can be implemented with sequential applications of the implication computation.

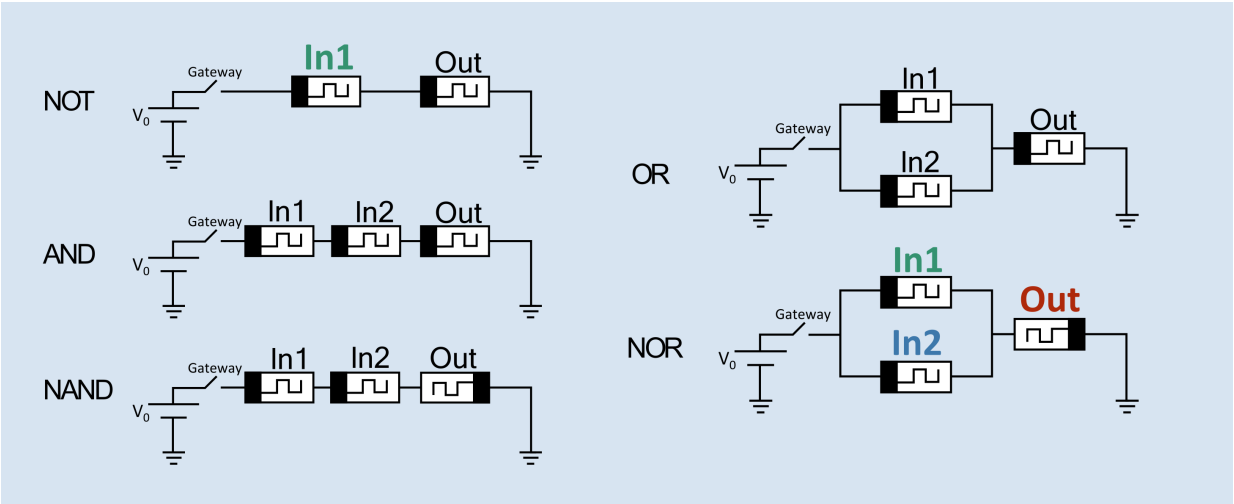
2.3.2 MAGIC – Memristor Aided-Logic

Similarly to the material implication, MAGIC presents the resistance values as the logic states. This logic family uses isolated memristors to store the input data, and a third memristor implements the output bit. All standard gates, such as NOT, AND, OR, NOR, and NAND, can be implemented by MAGIC logic, as shown in the figure 2.11. In addition, this design style requires two steps:

- Output initialization with a specific logic state
- Voltage V_0 applied to the input port

When the output is initialized with '0', it corresponds to non-inverting gates such as AND/OR. For inverting gates, like NOT, NOR, and NAND, the output memristor should be initialized with '1'.

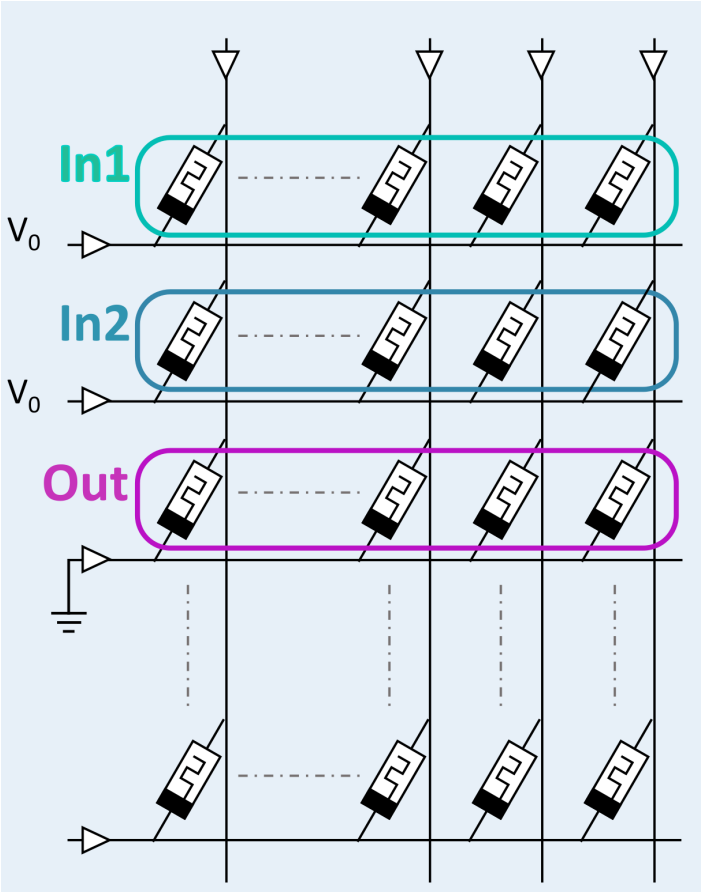
Figure 2.11 – Schematic of primitive gates using memristor-based MAGIC design.



Source: Author.

Although the primitive gates are achievable using MAGIC, only NOR and NOT are feasible to NVM crossbar arrays, as depicted in Figure 2.12. Therefore, more complex boolean functions are implemented in terms of NOR and NOT operations. Hence,

Figure 2.12 – Magic NOR in crossbar Array.



Source: Ali (2020).

peripheral circuits control the sequential operations to realize them.(ALI, 2020).

2.4 Compute In-Memory

Compute In-memory (CIM) explores the structural alignment between a dense array of bit cells, mainly in the data flow, with high-dimensionality matrix-vector multiplication (MVM), which has been used for signal processing and machine-learning-based applications. Recent prototypes presented capabilities to cover the computational energy and throughput metrics at least ten times. However, fitting computation within an array of constrained bit cells imposes complex challenges, which include the requirements for analog behavior, and the efficient virtualization of the hardware to map software.

In traditional von Neumann architectures, the processing and memory units are separated subsystems connected via a system bus or Network-on-Chip (NoC). These systems are inefficient while realizing modern computing workloads such as machine learning, deep learning, and data analytics. Usually, this gap, due to the data transferring between

the core memory and the arithmetic unit, leads to a significant fraction of the overall system energy and time, which is not feasible and helpful for large-scale computations. We can consider that all this time lost, and even the energy, reduces the whole system's efficiency.

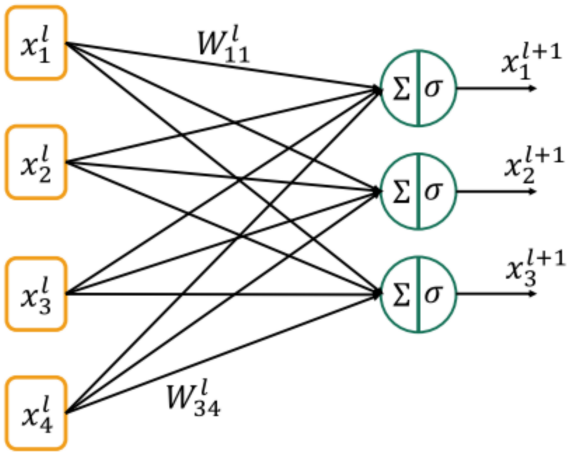
2.4.1 Deep Neural Networks

Deep neural networks (DNNs) have attracted increasing attention due to the wide range of deep learning applications in computer vision, such as image segmentation and object detection in autonomous vehicles. To accomplish such complex tasks, DNNs tend to have profound models to explore a large amount of data, which represents a challenge to the conventional Von Neumann architecture regarding memory access and energy cost. Thus, CIM represents an alternative to mitigate the von Neumann bottleneck.

Deep Neural Networks are constructed from layers of neurons, the fundamental computation element. The structure of a single layer is depicted in Figure 2.13. Each layer determines its value from a set of inputs connected to the neuron through a weighted connection called a synapse. The weighted sum of the inputs gives the value of the output (GREENBERG-TOLEDO et al., 2019).

$$\sum_{m=1}^{M} W_{nm} X_m \tag{2.26}$$

Figure 2.13 – Single layer of an Artificial Neural Network.



Source: Greenberg-Toledo et al. (2019).

Where M is the total number of input neurons, X_m is the value of the input neuron

m, W_{nm} is the synapse weight between the neuron n and neuron m, and finally, r_n is the output n. Therefore, the output vector $\overrightarrow{r_n}$ is determined by a matrix-vector multiplication.

$$\overrightarrow{r_n} = W\overrightarrow{X} \tag{2.27}$$

Here, the elements of matrix W are the synapse weights, and the vector $\overrightarrow{X}$ refers to the input neurons. Therefore, the next computation nominated as $\overrightarrow{X}^{l+1}$ is calculated by passing the output of the previous layer $\overrightarrow{r}^{l}$ through an activation function $\sigma(.)$ as shown below.

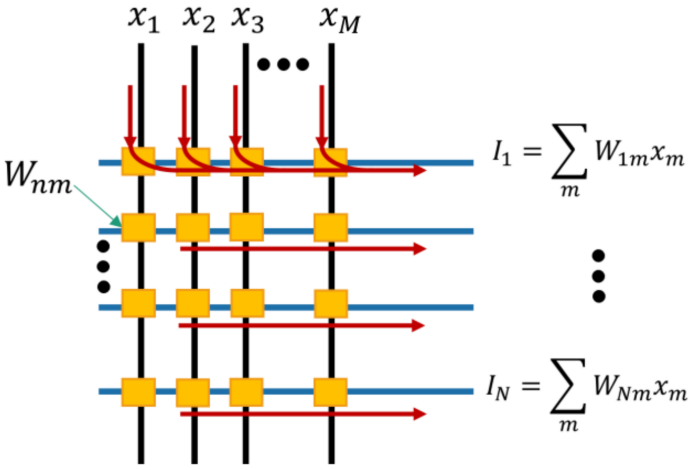
$$\overrightarrow{X}^{(l+1)} = \sigma(W^{(l)}\overrightarrow{X}^{(l)}) = \sigma(\overrightarrow{r}^{(l)}). \tag{2.28}$$

The complete network is constructed by cascading a matrix of synapses and activation functions.

2.4.2 Memristor based-Synapse

DNN models operate with a matrix of weights. In CIM, these weights are mapped to bit cell conductance, whereas the input vector is loaded in parallel as voltage to the rows, as shown in Figure 2.14. Hence, the multiplication is the product between the input voltage and the weight conductance. Furthermore, the output is given through the current summation along the columns (YU et al., 2021). This structure leverages the analog nature of this technology, improving the latency of synapse-related computation and power consumption.

Figure 2.14 – Memristor based-Synapse.



Source: Greenberg-Toledo et al. (2019).

Usually, this whole structure is arranged in crossbar arrays, and by using Ohm's Law, the weight of the synapse is the conductance of the memristor G_{nm}.

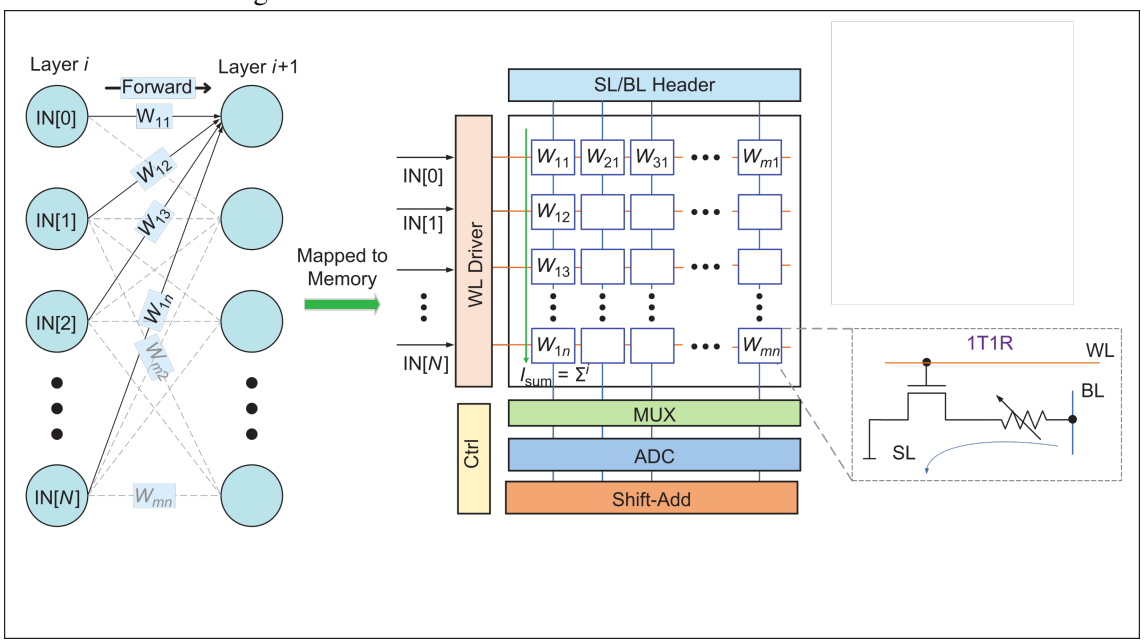
$$I_{nm} = G_{nm}\mu_m = W_{nm}X_m \tag{2.29}$$

Therefore, the current for each row is presented by

$$I_n = \sum_{m}^{M} W_{nm}X_m \tag{2.30}$$

The Analog-to-digital-converter (ADC) is used to convert the weighted sum to binary bits for the subsequent digital operations, such as accumulation, activation, shift-and-add, and polling. The CIM architecture based on memristor is depicted in Fig. 2.15, where the crossbar array uses 1T1R topology.

Figure 2.15 – Memristor Crossbar based CIM architecture.



Source: Yu et al. (2021).

3 COMPACT MODELS

Electronic circuit simulation is essential in modern Integrated Circuit (IC) development. One of the most valuable tools in this field is SPICE (Simulation Program with Integrated Circuit Emphasis). It was adopted by the IC industry, and several companies have used it as the basis for standard industrial circuit simulators. SPICE allows the simulation of complicated circuits without building a prototype and testing. In addition, it performs accurate simulations depending on the electrical model's quality, which is required to design efficient hybrid circuits using CMOS plus memristive devices.

Any conventional circuit element, such as MOS transistor, resistor, and capacitors, is considered the so-called "black box." It contains some external nodes in the circuit description that allow the interconnection between other "black boxes" forming what we know as a circuit.

Regarding the memristive devices, with their diversity of physical principals and materials. They cannot be modeled as other conventional circuit elements. Depending on the technology, the electric current that passes through the junction is closely related to its magnetization state and working temperature. Therefore, physical equations are not generally compatible with existing RLC components in SPICE.

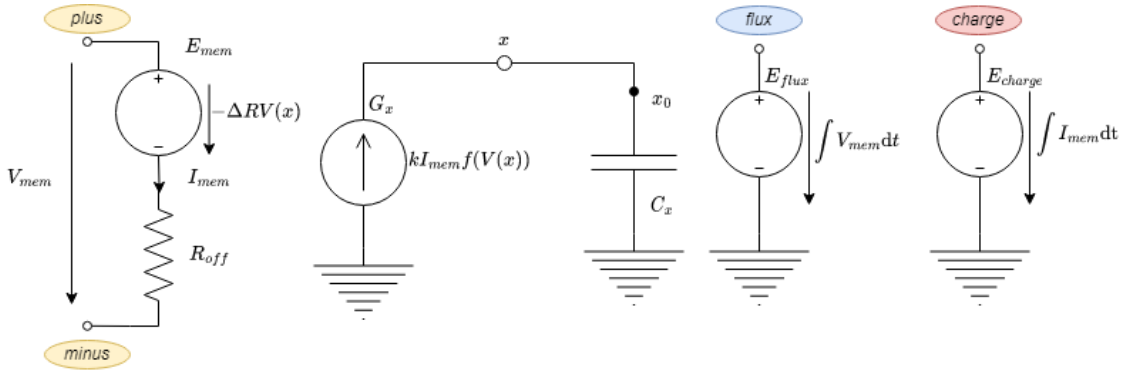
This chapter presents compact designs developed as SPICE models to realize different families of memristive devices.

3.1 Biolek Model

In 2008, a research group reported a manufacturing process of a memristor (BIOLEK; BIOLEK; BIOLKOVA, 2009). Since the authentic samples of the memristors were inaccessible to most of the researchers. A computer model that realizes the memristor speed up the analysis and development of applications through experimental simulations.

Based on a mathematical model, Biolek, Biolek and Biolkova (2009) proposed a SPICE model that implements the memristor produced by HP Labs, a T_iO_2 device with a new approach to describe the boundary effects in dopant drifts. This model uses a voltage-controlled voltage source to reproduce the oxygen vacancies depicted by the voltage across the capacitor C_x, while other E sources realize the flux and charge computation.

Figure 3.1 – Biolek SPICE model.



Source: Author.

The memory effect (LRS and HRS states) are modeled via a feedback-controlled integrator, limiting the boundary conditions through the current source G_x, which is responsible for updating the boundary position x.

3.1.1 Model Description

The normalized width x is supplied by the voltage $V(x)$ in the capacitor C_x, which acts as an integrator circuit to simulate the non-linear dopant drifts. The initial state of the doped region x_0 is determined by the initial electric resistance R_{init}, according to the formula shown below.

$$x_0 = \frac{R_{off} - R_{init}}{\Delta R}, \Delta R = R_{on} - R_{off}. \tag{3.1}$$

The main SPICE subcircuit, receives as arguments: the initial resistance R_{init}, the R_{on}, the R_{off}, the width of thin film D (size $\approx$ 10 nm), the dopant mobility μ_v, and the control parameter p.

3.1.2 Boundaries Effects

The motion speed of the boundary between the doped and undoped regions is a function of Biolek Window f(x), as shown in the equation below.

$$\frac{dx}{dt} = \frac{\mu_v M_{on}}{D^2} \cdot i(t) \cdot f(x), \tag{3.2}$$

Where $\mu_v \approx 10^{-14} m^2 s^{-1} V^{-1}$, is average drift mobility and the Biolek Window

function f(x) is defined by equation 3.3.

$$f(x) = 1 - (x - sgn(-i))^{2p}, \tag{3.3}$$

This window function proposed by JOGLEKAR; WOLF has the parameter p as a control parameter that is a positive integer. When p increases, the linear and non-linear drift differences tend to disappear. The sgn(.) is a sign function that guarantees zero speed when the coordinate x approaches the boundary.

3.2 Pershin and Di Ventra Model

Pershin and Ventra (2010) proposed an activation-type model of memristor (STRUKOV et al., 2008) based on T_iO_2 device. Inspired by experimental results, they included a voltage threshold in the mathematical model due to the differences between the current math models and the real memristor. The authors proposed a memristive system described by the following equations:

$$i_{mem} = M^{-1}\dot{v}_{mem}, \tag{3.4}$$

Where M is the memristance, v_{mem} is the bias voltage applied to the memristive device, and i_{mem} refers to the electric current flowing into the device.

$$\frac{\partial M}{\partial t} = f(v_{mem})[\theta(v_{mem})\theta(R_{off} - M) + \theta(-v_{mem})\theta(M - R_{on})] \tag{3.5}$$

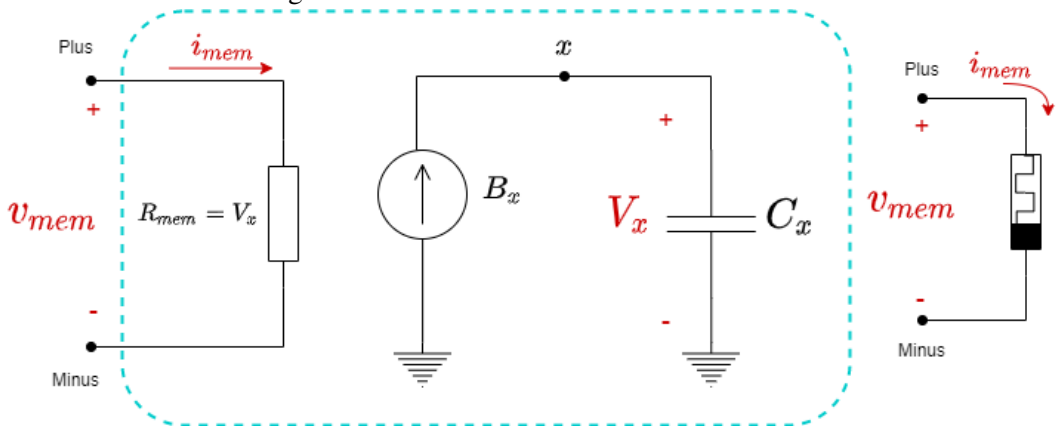
Where

$$f(v_{mem}) = \beta v_{mem} + \frac{1}{2}(\alpha - \beta)(|v_{mem} + v_T| - |v_{mem} - v_T|) \tag{3.6}$$

Here, $f(v_{mem})$ represents the ratio of memristance while meeting the boundary conditions $|v_{mem}| > 0$ and $R_{on} < M < R_{off}$, and v_T is the voltage threshold.

Increasingly the voltage above the threshold v_T, the memristor triggers the switching process, accentuated by the linear dependence of $f(v_{mem})$ with α and β. The voltage across C_x controls the magnitude of memristance through a behavioral resistor. In addition, this capacitor is connected to a current source B_x, which controls the boundary effects related to the transitions in a multipolar approach, similarly to the design presented in Biolek model (BIOLEK; BIOLEK; BIOLKOVA, 2009).

Figure 3.2 – Pershin and Di Ventra Model.



Source: Author.

Therefore, the total memristance is given below, integrating both sides of Equation 3.5.

$$M = \int_0^t [f(v_{mem})(\theta(v_{mem})\theta(R_{off} - M) + \theta(-v_{mem})\theta(M - R_{on}))]dt + R_{init} \quad (3.7)$$

Where R_{init} refers to the initial memristor resistance.

3.2.1 Current Threshold-based Model

Dias (2018) proposed changes to the Pershin and Di Ventra Model to realize the current threshold instead of the voltage threshold. As a result, the Equation 3.7 changed, and two new functions $f_1(i_{mem}, M)$ and $f_2(i_{mem}, M)$ were added to treat the multipolar transitions. According to these changes, the following equation is given:

$$\frac{\partial M}{\partial t} = f_1(i_{mem}, M)[\theta(i_{mem})\theta(R_{off} - X)] + f_2(i_{mem}, M)[\theta(-i_{mem})\theta(X - R_{on})] \quad (3.8)$$

Where θ represents the step function, this function implements the memristance ratio in the conditions presented below.

$$\frac{\partial M}{\partial t} = \begin{cases} f_1(i_{mem}, M), & i_{mem} > 0 \text{ e } X < R_{off} \\ f_2(i_{mem}, M) & i_{mem} < 0 \text{ e } X > R_{on} \\ 0 & \text{other cases} \end{cases} \quad (3.9)$$

Where f_1 and f_2 are described using the following expression:

$$f_n(i_{mem}, M) = Kp_n\beta i_{mem} + 0,5Kp_n(\alpha - \beta)(|i_{mem} + i_T| - |i_{mem} - i_T|) \quad (3.10)$$

Here, i_T is the electric current threshold. α and β control the memristance ratio according to the electric field sensibility. These parameters modify the model to assume two different types of switching.

3.2.1.1 Switching Types

The first type occurs when $\alpha < \beta > 0$, called soft switching. In this case, the electric resistance is susceptible to the electric current flowing within the device, even under small electric current values. Therefore, the function $f_n(i_{mem}, M)$ presents small tolerances according to the i_{mem} value, as shown in the equation below.

$$f_n(i_{mem}, M) = \begin{cases} Kp_n[\beta(i_{mem} - i_T) + \alpha i_T], & |i_{mem}| > i_T \\ Kp_n\alpha i_{mem}, & i_{mem} < i_T \end{cases} \quad (3.11)$$

In this type, the MR intensifies as the electric current increases above the threshold i_T. However, it is still sensitive to variation under small values.

On the other hand, the second type is called hard switching. In this case, the switching process exclusively occurs when i_{mem} reaches beyond the current threshold. In addition, $\alpha = 0$ and $f_n(i_{mem}, M)$ is given according to the following states:

$$f_n(i_{mem}, M) = \begin{cases} Kp_n\beta(i_{mem} - i_T), & |i_{mem}| > i_T \\ 0 & i_{mem} < i_T \end{cases} \quad (3.12)$$

3.2.1.2 Memristance Ratio

The aspect ratio Kp_n is the most relevant property in this model. This variable allows for faster switching as the memristance approaches to the target value. In addition, it also assumes two different expressions due to the $f_n(i_{mem}, M)\ \epsilon\ \{1, 2\}$.

According to the transitions $M \rightarrow R_{on}$ and $M \rightarrow R_{off}$, where R_{final} refers to the current state. Kp_n is described by the following criteria.

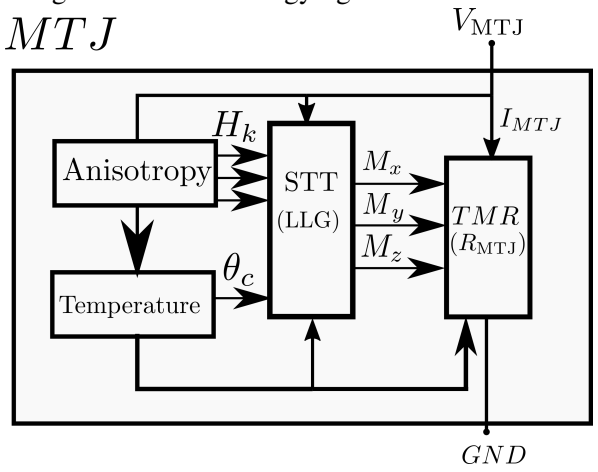
$$Kp_n = \begin{cases} (\frac{R_{off} - M}{R_{off}} + C_1), & n = 1 \\ (\frac{M - R_{on}}{R_{off}} + C_2), & n = 2 \end{cases} \quad (3.13)$$

From a different perspective, Kp_n is treated in a closed loop control system, where the memristance M is measured and fed back within the process. As a result, C_n works as an offset, increasing f_n, which controls the self memristance.

3.3 UMN MTJ Model

The proposed SPICE model (KIM et al., 2015) implements an MTJ as a box of SPICE modules or sub-circuits. Each module contains a part of physical characteristics related to the shape of MTJ, spin dynamics, and magnetoresistance. The main file, which includes all modules, is outputted within two nodes referred to the power supply, as shown in the Figure below.

Figure 3.3 – Technology-agnostic MTJ model.



Source: Author.

The anisotropy sub-circuit generates the H_{keff} based on three arguments: the MTJ dimensions, the shape anisotropy type, and the material parameters. According to the temperature module, the initial critical angle of magnetization θ_c and the probability of switching are estimated.

When a bias voltage is applied, a charge current I_{MTJ} passes through the MTJ and triggers the LLG module, returning the three magnetization components dependent on time. These three coordinates are converted to spherical coordinates in the TMR circuit, which calculates the relative angle between the pinned and the free layer.

For full compatibility with SPICE, each subcircuit was implemented using basic circuit elements, such as capacitors, resistors, voltage/current dependent sources, and voltage/current sources.

3.3.1 Anisotropy Module

Depending on the input parameters, the Anisotropy module sets the shape anisotropy field H_k. This setup occurs due to the physical origin of magnetic anisotropy MA. In this case, three options of shape are available: shape anisotropy-based in-plane (IMTJ), crystal anisotropy-based perpendicular (c-PMTJ), and interface anisotropy-based in-perpendicular (i-PMTJ).

For in-plane anisotropy, the demagnetizing field is stronger along the axis that contains the shortest dimension. The magnetization stays in the x-y plane, and the free layer is considered an elongated thin film with the shortest axis in Z direction. The anisotropy field $H_{k,shape}$ is given below.

$$H_{k,shape} = 4\pi(N_{dx} - N_{dy})M_s, \tag{3.14}$$

Where M_s is the saturation magnetization and N_d is the geometry dependent demagnetizing factor.

In contrast to IMTJ, PMTJ offers a lower switching current due to the demagnetizing field in 'z' direction. For out-of-plane MA, this demagnetizing field assists the magnetization switching, canceling partially the perpendicular anisotropy field $H_{k\perp}$. In this case, the magnetization maintains the self-orientation dependent on the high crystallographic anisotropy K_u. This is intimately related to the exploitation of materials such as C_oP_t and F_eP_d. Therefore, the effective field for perpendicular anisotropy shape is calculated using the following expression:

$$H_{k\perp eff} = H_{k\perp} - H_{dz} = \frac{2K_\perp}{M_s} - 4\pi N_{dz}M_s, \tag{3.15}$$

The parameter $K_\perp$ is equivalent to K_u of the specific material in c-PMTJ's. For iPMTJ, $K_\perp$ is replaced by $K_i/tF(= 2\pi M_s^2 t_c/t_F)$, where t_F measures the free layer thickness and K_i is the anisotropy interface.

3.3.2 Landau Lifshitz Gilbert

In this model, the magnetization within the free layer is treated as uniform, as a single magnetic domain. Therefore, this approach uses the Landau Lifshitz Gilbert

equation to describe the magnetization as a time-dependent vector, as shown below:

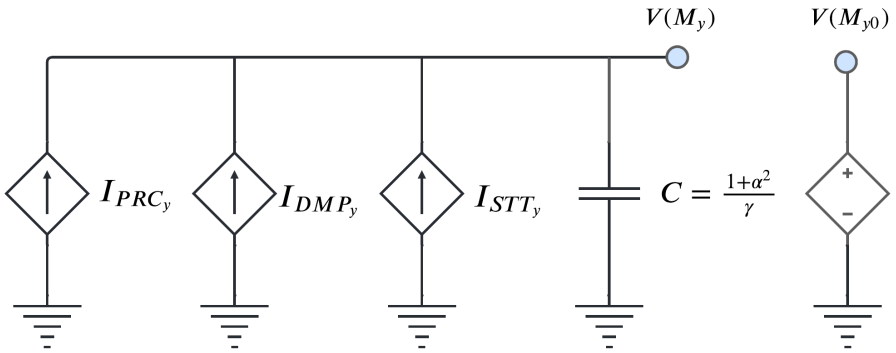
$$\overrightarrow{M(t)} = [M_x(t), M_y(t), M_z(t)] \tag{3.16}$$

Here, the spin direction of polarized current is related to the magnetization of the coercive side in the multilayered film $\overrightarrow{M_p}$. For in-plane anisotropy, H_{keff} is mainly governed by H_d, as shown below:

$$\overrightarrow{H_{keff}}(t) = -4\pi M_s[N_{dx}M_x(t), N_{dy}M_y(t), N_{dz}M_z(t)] \tag{3.17}$$

As previously mentioned, this SPICE subcircuit was implemented using basic elements of circuits. Therefore, the three components of spin dynamics expressed on top of LLG were converted into electric current sources, as shown below.

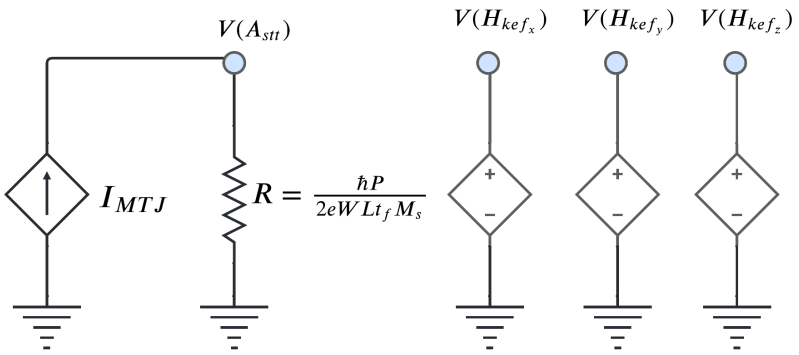
Figure 3.4 – LLG in terms of basic circuit elements.



Source: Author.

Where I_{PRC} is the precession movement [2.20], I_{DMP} is the damping process [2.21] and I_{STT} computes the spin transfer torque within the free layer [2.22]. Each coordinate (M_x, M_y and M_z) has the same topology, thus the anisotropy modules send the MA field to compute the H_{keff}, which is given through three voltage-dependent sources.

Figure 3.5 – Effective field computation with basic elements of circuits.



Source: Author.

Figure 3.5 shows that spin torque magnitude is computed using the current flowing into the MTJ module in parallel to a resistor, which updates the torque in terms of MTJ dimensions and the polarization factor.

3.3.3 Tunneling Magnetoresistance

This model considers the MTJ as a voltage-controlled variable resistance. The resistance at zero bias TMR_0 is defined using the previous expression for TMR, which is $(R_{ap} - R_p)/R_p$. Since the TMR depends not only on bias voltage but also the temperature. This model uses TMR's voltage and temperature dependency to capture the TMR_{eff}, which is a better measurement for read/write evaluation.

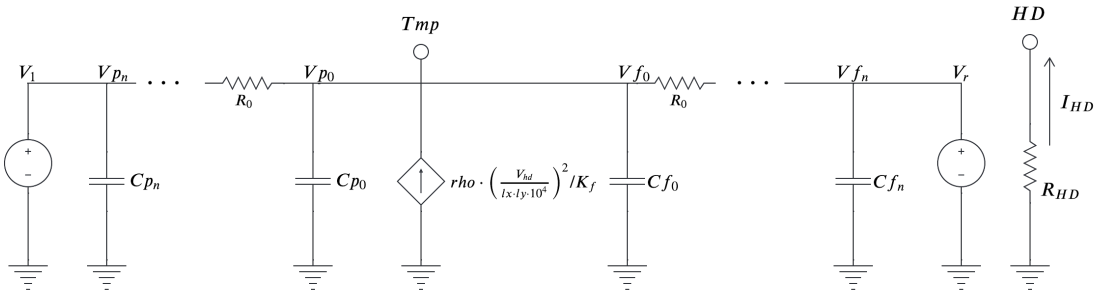
$$TMR(T,V) = \frac{2P_0^2(1-\alpha_{sp}T^{3/2})^2}{1-P_0^2(1-\alpha_{sp}T^{3/2})^2} \cdot \frac{1}{1+(V/V_0)^2} \tag{3.18}$$

P_0 is the Polarization Factor at 0 Kelvin, and V_0 is a fitting parameter. Once the resistance-area product is measured using the MTJ area, R_p and R_{ap} are calculated.

3.3.4 Non-deterministic Switching

The thermal effect in this model uses the I_{MTJ} as input to update the internal temperature due to Joule heating. This behavior is expressed in terms of an RC model depicted in Figure 3.6.

Figure 3.6 – Heat Difusion Module.



Source: Author.

The initial temperature T_{mp0} is set as an input parameter, and this RC network generates a current I_{HD}, which is used to update the temperature. In addition, this temperature (coupled in the node Tmp) is fed back to the other modules, such as TMR and STT, modifying parameters that contain temperature dependency, such as the saturation magnetization and the polarization factor, as follows:

$$M_s(t) = M_{s0}(1 - T/T_c)^{\beta}, \tag{3.19}$$

$$P(t) = P_0(1 - \alpha_{sp}T^{3/2}), \tag{3.20}$$

As a result, the model presents a non-deterministic transient behavior. This behavior is caused by a random thermal field, leading to a non-deterministic switching with easy axis deviation.

This stochastic behavior can be monitored by the switching probability P_{sw}, which is given as a function of the initial angle and the thermal stability as follows:

$$P_{sw} = 1 - \int_0^{\theta_c} \frac{sin\theta e^{(-\Delta^2\theta)}}{\int_0^{\pi/2} sin\theta e^{(-\Delta sin^2\theta)} d\theta} d\theta, \Delta = \frac{E_b}{k_B T}. \tag{3.21}$$

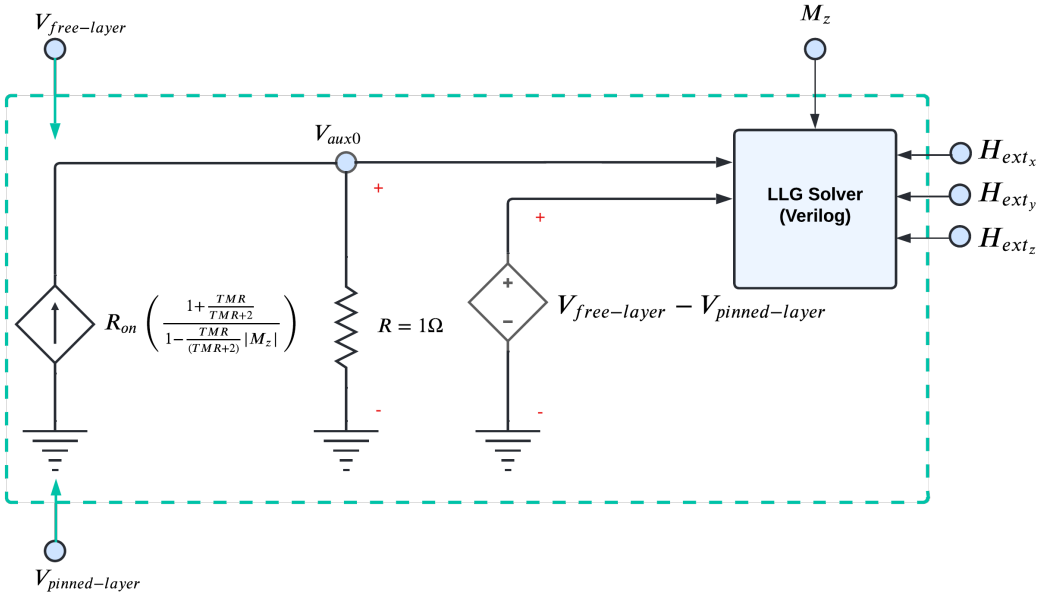
Here, T is the current temperature, E_b is the energy barrier, and k_B is the Boltzmann constant. Δ is known as thermal stability. The thermal field excited for long pulses (i.e., > $10ns$) may reduce the switching current, which is preferred today in high-speed applications.

3.4 PMTJ Model

Garcia-Redondo et al. (2021) proposed a model that realizes the spintronic memristor using naive Euler method to integrate the magnetization vector. The model uses spherical reference to solve the s-LLG through the circular integration, which was implemented using the *idtmod*, feature of Spectre simulator. This feature adapts the integration according to the multiple evaluations of differential terms at different time steps. As a result, the errors are reduced, and it avoids a lot of unnecessary computation.

Therefore, it avoids the critical angle θ_c to exceed the domain $[0, 2\pi]$, preventing unnatural voltages and convergence errors.

Figure 3.7 – PMTJ SPICE Subcircuit.



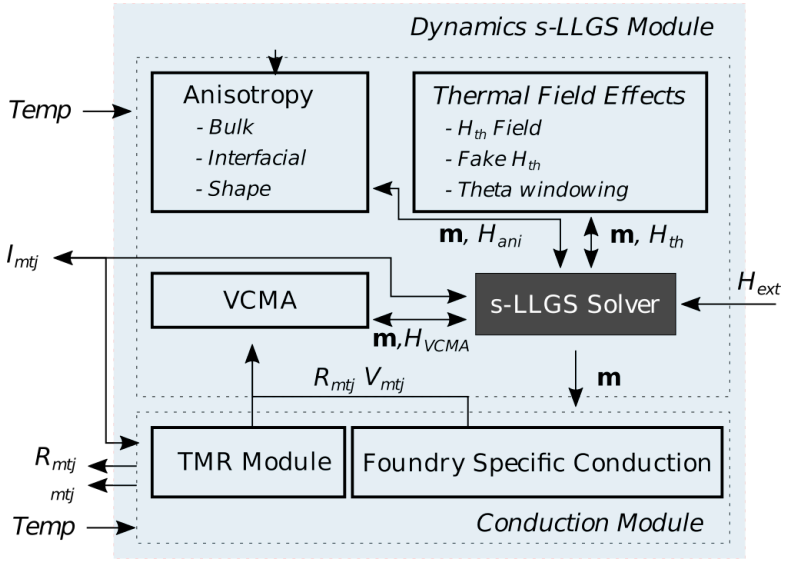
Source: Author.

3.4.1 Model Structure

In a standard MRAM cell, the easy axis of magnetization $\overrightarrow{M}$ is converted to the binary state of the data bit, which is the most critical component to accomplish an accurate model. In this model, the naive integration encodes the magnetization movement in a Verilog-A description, in which two fundamental characteristics are divided within modules: the conductance and spin dynamics. The model structure is depicted in Figure 3.8.

The conductance module sets the physical constants and defines the smallest

Figure 3.8 – STT PMTJ – Compact Verilog Model.



Source: Garcia-Redondo et al. (2021).

resistance (R_{on}). The basic TMR is calculated in terms of the polarization factor, which is also granted by the foundry-specific properties. In this case, it admitted a symmetric structure ($P_1 = P_2$), as presented below.

$$TMR(P) = \frac{2 \cdot P^2}{(1 - P^2)} \tag{3.22}$$

Here, P refers to the polarization factor. Unlike the UMN model, in this model, the thermal noises do not affect the tunneling magnetoresistance. Therefore, R_{off} just becomes higher as the polarization increases close to 1 and in the case of R_{on} is higher.

$$R_{MTJ} = R_{on} \left(\frac{1 + \frac{TMR}{TMR+2}}{1 - \frac{TMR}{(TMR+2)}|M_z|} \right) \tag{3.23}$$

The temporal evolution of magnetization as a mono domain nanomagnet consider the influences of anisotropy, thermal, external magnetic field and STT effect. Therefore, by referring to a perpendicular anisotropy shape, the effective field is calculated as shown below.

$$H_{eff} = H_{ext} + H_{uniaxial} + H_{demag} + H_{vcma} + H_{thermal} \tag{3.24}$$

The anisotropy constants are shared with the s-LLG solver, which computes the shape demagnetizing field and also the spherical solution for the s-LLG equation (2.17).

3.4.2 Thermal Effect

The random magnetic field H_{th} is affected by thermal fluctuations, leading to a stochastic switching behavior. This factor increases the Write Error Rate (WER) upon switching events (GARCIA-REDONDO et al., 2021). For FM/I/FM structures, the thermal field may reproduce the Brownian motion, where each direction is independent. This fact implies a large independent variation between the steps, which restricts the solver from guaranteeing signal continuity under small tolerances.

This model supports two features to replicate the thermal effect; the first is the Tukey window function, as shown below.

$$\omega(m_\theta) = \begin{cases} 0 & m_\theta < \theta'_0 \\ 0.5 - \frac{cos}{2}\frac{4\pi(m_\theta - \theta')}{\theta'_0} & m_\theta - \theta'_0 < \theta'_0/4 \\ 0 & otherwise \end{cases} \tag{3.25}$$

It provides a mechanism for m_θ saturates naturally to the equilibrium value given by H_{th} upon the switching events, by redefining the evolution of m related to the easy-axis deviation.

$$\frac{\partial m'_\theta}{\partial t} = \omega(m_\theta, \theta_0)\frac{\partial m_\theta}{\partial t} \tag{3.26}$$

Although the window function prevents artificial saturation of m_θ, this approach does not implement the mean effect of H_{th} during transient events such as a low current excitation (read operation). Therefore, the second feature is implemented, which is a fake thermal field in the effective field computation H_{eff}. This thermal field reproduces a Gaussian noise like magnetic field, as shown in the Equation below.

$$H_{th} = \overrightarrow{\sigma}\sqrt{\frac{2K_B T\alpha}{\mu_0\gamma' M_s V\Delta t}} \tag{3.27}$$

Where $\overrightarrow{\sigma} = \{\sigma_x, \sigma_y, \sigma_z\}$ is the unit coefficient vector, and their components are Gaussian random variables with a mean of 0 and standard deviation of 1 (ZHANG et al., 2020). V is the free-layer volume and Δt is the time-step of magnetization evolution.

3.4.3 VCMA

Recently, voltage-controlled magnetic anisotropy (VCMA) has been introduced to improve energy-delay efficiency and enhance the robustness of non-volatile writing control through an electric field or switching voltage. In this model, the VCMA is set up through a boolean input parameter. As a result, the effective field receives an additional component in the z-axis direction when it is turned on, given by the VCMA equation below.

$$H_{vcma} = \frac{2\beta(V_{pinned} - V_{free})}{\mu_0 M_s t_{ox} t_f} m_z \hat{e}_z \tag{3.28}$$

Here, β is the VCMA coefficient, which is a material-dependent parameter that quantifies the change of interfacial anisotropy energy according to the applied electric field ($V_{pinned} - V_{free}$). t_{ox} is the thickness of the tunnel barrier. Note that the VCMA field also depends on the easy-axis magnetization in this implementation. Therefore, the VCMA effect may reduce or enhance the interfacial PMA depending on the polarity of the voltage applied to the MTJ (ZHANG et al., 2020).

4 METHODOLOGY

Based on the compact models presented, this work is divided into three steps: model verification, evaluation of simple cell operation using the proposed memristors SPICE models, and a comparison in terms of usage and performance.

As standard, the Cadence Spectre simulator was chosen. This software offers one of the leading solutions for analog simulation in the IC industry. Cadence Spectre platform contains multiple solvers that allow a designer to move easily and seamlessly between circuits, blocks, and system-level simulation, guaranteeing consistent and accurate evaluation methods (SYSTEMS, 2004).

4.1 Model Verification

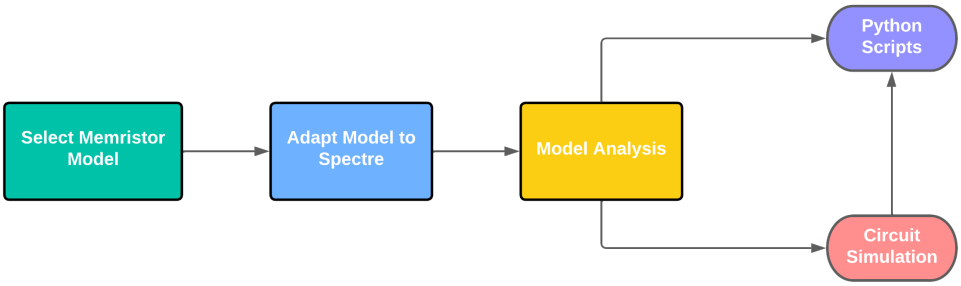
This step consists of a brief verification of the compact designs, described in the last chapter, three models were chosen: the current threshold-based Pershin (T_iO_2), the UMN Model using the IMTJ anisotropy, and PMTJ Verilog Model.

This verification mainly aims to validate the pinched hysteresis loop and measure the memristance ratio in the selected models. Some of them will not be easily interpreted by Cadence Spectre Simulator, depending on the SPICE language they are based on, or even may present convergence issues. Therefore, they will be adapted to Spectre language or standard SPICE to allow the use of Spectre Simulator.

After understanding the basic concepts and the differences between those implementations, this work aimed to create an environment of SPICE, Verilog, and *Python* code, which allows simulating and extracting design parameters of different technologies of memristive devices intended for in-memory computing.

In order to achieve the hysteresis loop, DC simulations were performed, fixing the bias voltage/current to ensure that every model was working correctly. For the other measurements, transient simulations were performed using target nodes to store the results. The simulation outputs are treated through *Python* scripts with a set of libraries to retrieve the waveform vector from Cadence PSF files and plot them. The entire flow is shown in the flowchart below.

Figure 4.1 – Workflow.



Source: Author.

The list of required packages is shown below.

- ***Lipsf*** - a *Python* library for reading Cadence PSF data, such as waveforms, time series, AC-analysis, DC, and more kinds of data from proprietary binary Cadence-PSF file format.
- ***Numpy*** - is the fundamental package for scientific computing in *Python*, it provides a multidimensional array object and other derived objects, such as matrices and masked arrays (HARRIS et al., 2020). *Numpy* includes an assortment of routines, enabling fast operations with these objects, such as basic linear algebra, statistical operations, random simulations, and much more.
- ***Matplotlib*** - a comprehensive library for creating static, animated, and interactive visualizations in Python. It produces publication-quality figures in a variety of formats, and interactive environments across platforms (HUNTER, 2007).

4.2 Performance Analysis

The performance analysis is given through the measurements of classical parameters in circuit design, such as switching time and average power consumption. A sweep analysis was performed to compute these measurements for different source thresholds among the compact models.

The average power required for a single switch is measured by multiplying the electric current and voltage across the device during the switching time. For this purpose, the switching time is defined from the beginning of write mode (the source changes its logical state from $0 \rightarrow 1$) until the reaching 90% of R_{final}. For spintronic devices, instead of 90% of final resistance, it is counted when the free layer magnetization is totally reversed

($M_{easy-axis} = 0$).

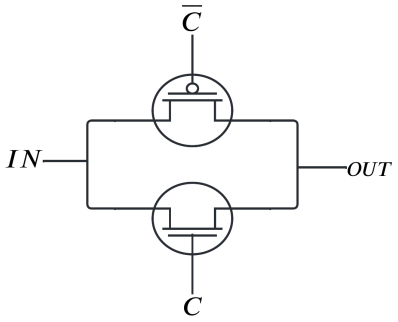
The obtained data were compared to verify the differences among the validated memristor models.

4.3 CMOS Integration

In this step, the compact designs were integrated with a CMOS circuit to perform a unique implication $p \rightarrow q$ using two-bit cells. This simulation aims to confirm that there are no convergence issues in designing circuits using a hybrid approach. For this purpose, the Predictive Technology Model of 16nm for high performance (16nm PTM-HP) was chosen, provided by Nanoscale Integration and Modeling (NIMO) Group at ASU.

PTM offers accurate, customizable, and predictive model files for future transistors, which are compatible with standard circuit simulators and scalable with a wide range of process variations. The control signals for implication V_{SET} and V_{COND} were converted into two CMOS transmission gates (TG), as depicted in Figure 4.2 and Table 4.1.

Figure 4.2 – CMOS Transmission Gate.



Source: Author.

C	IN	OUT
1	1	1
1	0	0
0	x	Z

Table 4.1 – CMOS Transmission Gate - Control Signal

TGs are CMOS-based switches, in which the PMOS pass a strong logic '1' and a poor logic '0', and NMOS pass a strong logic '0' and a poor '1'. Therefore, this switch enables and blocks the input signal using the PMOS and NMOS at the same time (XU; FRIEDMAN, 2002).

5 RESULTS

This section discusses the results obtained in Cadence Spectre simulation, and the data analysis through the *Python* scripts.

5.1 SPICE Syntax

Some models presented convergence issues due to the simulator interpreter. The Current Threshold model is one model that had to be refactored to the Spectre syntax. The code extract below shows part of this implementation.

```
real Im(real vmem, real vx) {
  return (vmem/vx)
}
subckt memristor (plus minus)
  Cx x 0 capacitor c=1 ic=Rinit
  Bx 0 x bsource i=((Im(v(plus),v(x)) > 0) && (v(x) < Roff)) ? f1(Im(v(
   plus),v(x)),v(x)) : ((((Im(v(plus),v(x))  < 0) && (v(x) > Ron)) ?
   f2(Im(v(plus),v(x)) ,v(x)) : 0))
  Rmem plus minus resistor r=v(x)
ends memristor
```

This model contains only one sub-circuit file, which implements the whole behavior given by the behavioral current source B_x and the capacitor C_x.

Although the Spectre simulator can interpret a HSPICE-based description, the IMTJ model presented errors to interpret the boundary definitions of the relative angle between the pinned and the free layer θ; it is in the process of converting the magnetization into spherical coordinates. This computation is made through the voltage-dependent source E_{th}.

```
subckt RA (n_plus n_minus Mx My Mz Tmp thi)
parameters lx=65n ly=130n P0=0.715 RA0=5.4 MA=0.0

//*** Spherical coordinate ***

E_thip (thip 0) bsource v=(1-MA)*acos((1-MA)*0.999*v(My)/pow(pow(v(Mx)
   ,2)+pow(v(My),2),0.5))
E_thp  (thp 0) bsource v=MA*acos(MA*0.999*v(Mz)/pow(pow(v(My),2)+pow(v(
   Mz),2),0.5))
E_th   (th 0) bsource v=max(V(thi),min(355/113-V(thi),V(thip)+V(thp)))
```

```
E_phi  (phi 0) bsource v=(1-MA)*atan(v(Mx)/v(Mz))+MA*atan(v(My)/v(Mx))
```

Therefore, this SPICE sub-circuit was ported to standard Spectre language to avoid errors in the analysis.

5.2 Model Verification

Transient simulations were performed to achieve the memristance change, which exposes the model's switching shape and the hysteresis loop. As proposed, the models were not adapted to present the same properties, as they are different technologies of memristors. Therefore, the physical parameters for each one were kept as default. The list of inputs is shown in Table 5.1.

Table 5.1 – Compact Designs Input Parameters.

Parameter	**Description**	TiO_2	**IMTJ**	**PMTJ**
$R_{on}[\Omega]$	Lower Resistance	5.0k	1.63k	6.0k
$R_{off}[\Omega]$	Higher Resistance	30.0k	3.41k	21.43k
W [m]	Free Layer Width	-	32.0n	50.0n
L [m]	Free Layer Length	-	96.0n	50.0n
t_f [m]	Free Layer Thickness	-	2.44n	1.0n
P_0	Polarization Factor	-	0.69	0.75
T_0 [K]	Initial Temperature	-	358	300
H_{ext}	External Magnetic Field	-	0	0
$VCMA$	VCMA Effect	-	-	0
$\omega(m_\theta)$	Thermal Window	-	-	false
α	Damping Factor/Factor	-	0.0062	0.01
α_x	Control Parameter	0	-	-
β_x	Control Parameter	1e18	-	-
M_s [A/m]	Saturation Magnetization	-	1210	1200
i_T [A]	Current Threshold	25u	-	-
V_{bias} [V]	TMR Bias Voltage	-	0.65	-

Source: Author.

This verification aimed to review the primary behavior of the presented technologies. The TiO_2 presented above refers to the Current Threshold model, and the results are detailed in the following subsections.

5.2.1 Switching Shape

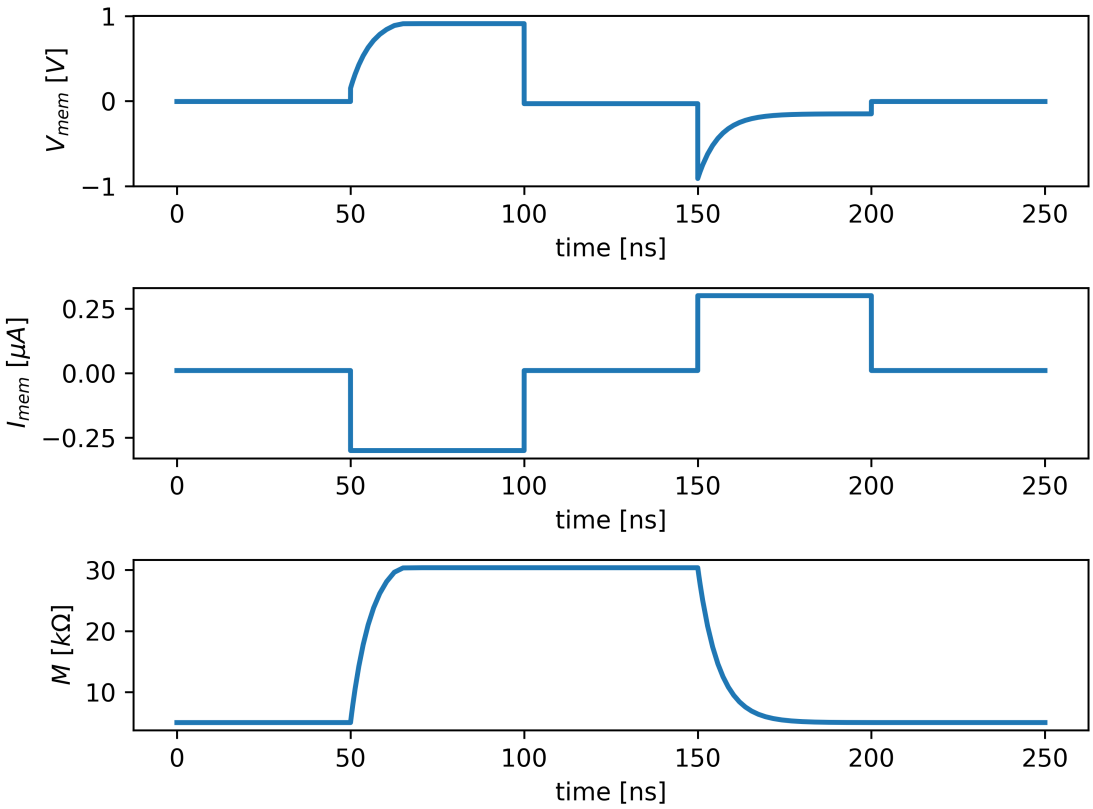
As the memristor behaves like the bit value in NVM memories, a piece-wise linear (PWL) source was introduced to reproduce the same waveform desired in digital

applications. The results obtained for each model are shown in the following subsections.

5.2.1.1 T_iO_2 Model

The results for the transient analysis of the T_iO_2 model are displayed in Figures 5.1 and 5.2. The PWL signal is the current source I_{mem}.

Figure 5.1 – Switching Shape – Current threshold-based Pershin Model



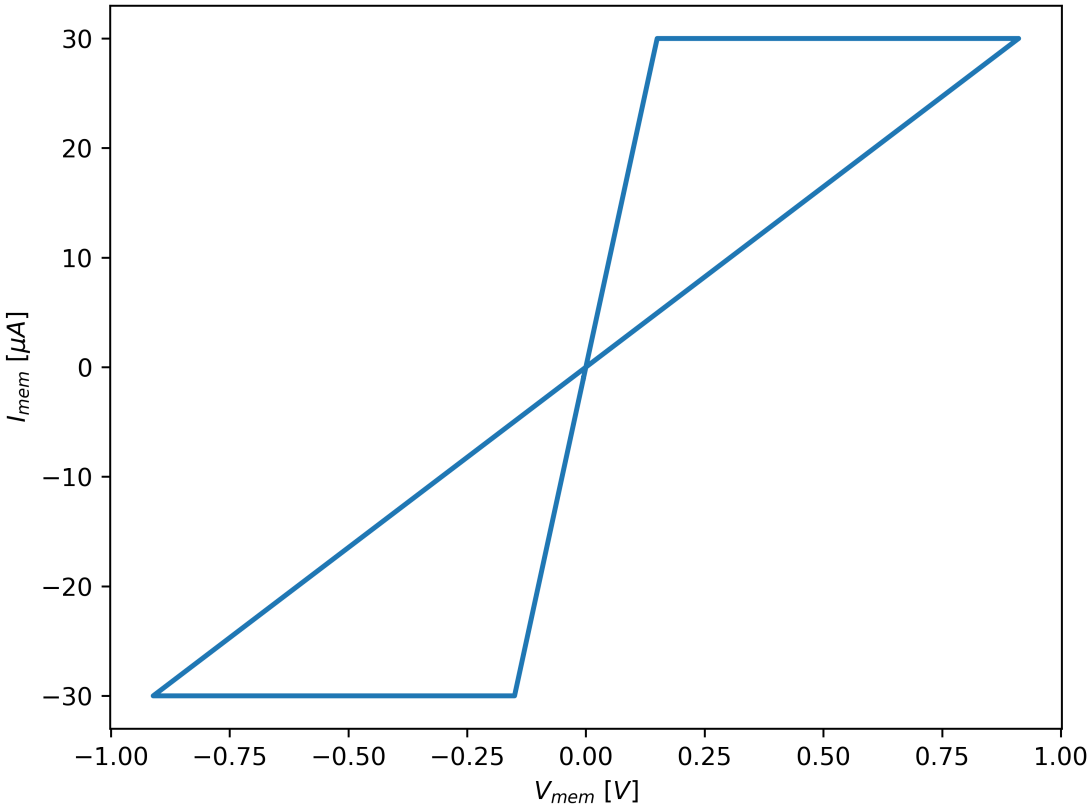
Source: Author.

Peeking the voltage and memristance form, we can ensure that this model is replicating the equation 2.11. When the current threshold is reached ($\approx 50ns$), the internal electric resistance is governed by Kp_1 with the highest resistance R_{off} of $30.0k\Omega$. In this transition, the dopant-drifts $x(t)$ are controlled via the f_1 function in a hard threshold course ($\alpha = 0$ and $\beta > 0$); hence, the squared waveform works flawlessly due to the magnitude of the PWL source beyond the threshold and the memristance changes only above the threshold value.

The other transition occurs at $t = 150ns$, when the memristor reaches the transition $R_{off} \rightarrow R_{on}$. In this case, the memristance is controlled via f_2 function and Kp_2 with R_{on} of $5.0k\Omega$.

As predicted, both transitions will not present fluctuations due to the order and continuous effect of the f_n equations. The dual behavior becomes more evident, treating the results in the $V \times I$ plane, as shown in the hysteresis loop presented in Figure 5.2.

Figure 5.2 – Pinched Hysteresis Loop – Current threshold-based Pershin Model.



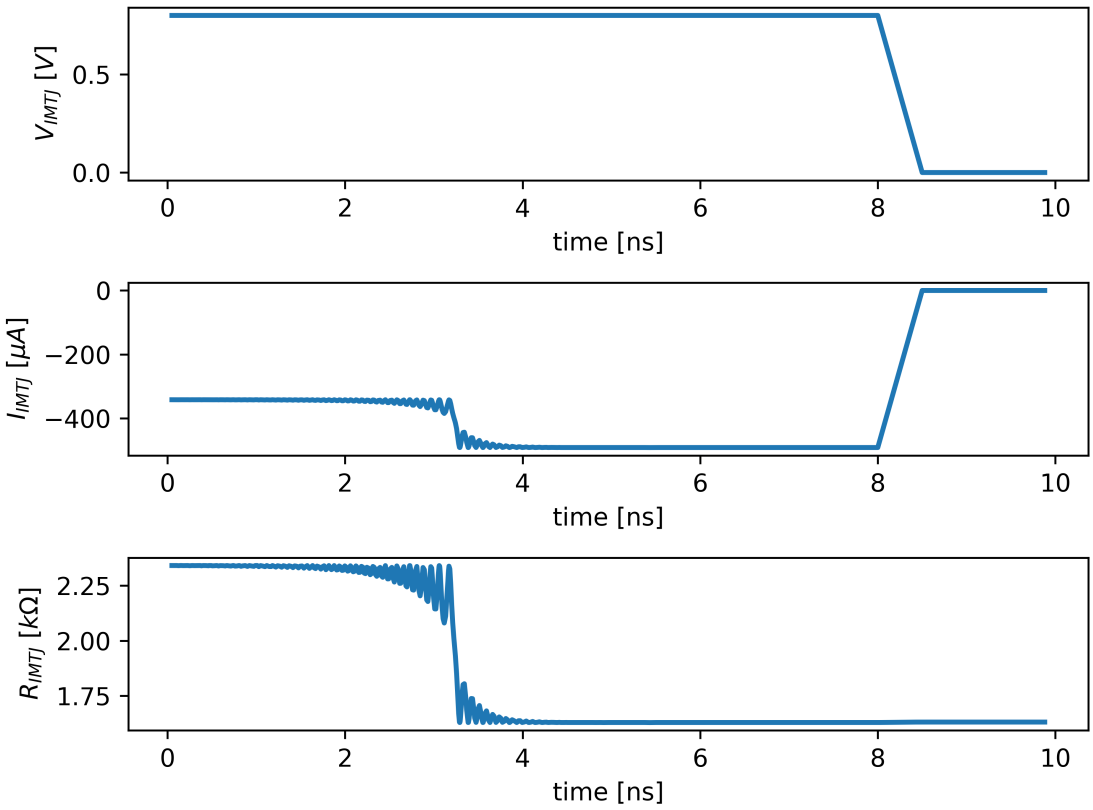
Source: Author.

The pinched hysteresis loop shows a symmetric switching, which is expected due to the f_1 and f_2 implementations, as they have the identical value for the current threshold I_t.

5.2.1.2 UMN IMTJ

The switching form for the IMTJ model is given in terms of the easy-axis deviation calculated via the LLG solution. At this point, it may present some oscillations due to the effective demagnetizing field arrangement in In-Plane based-anisotropy, shown in the Figure below.

Figure 5.3 – Switching Shape - UMN IMTJ Model.

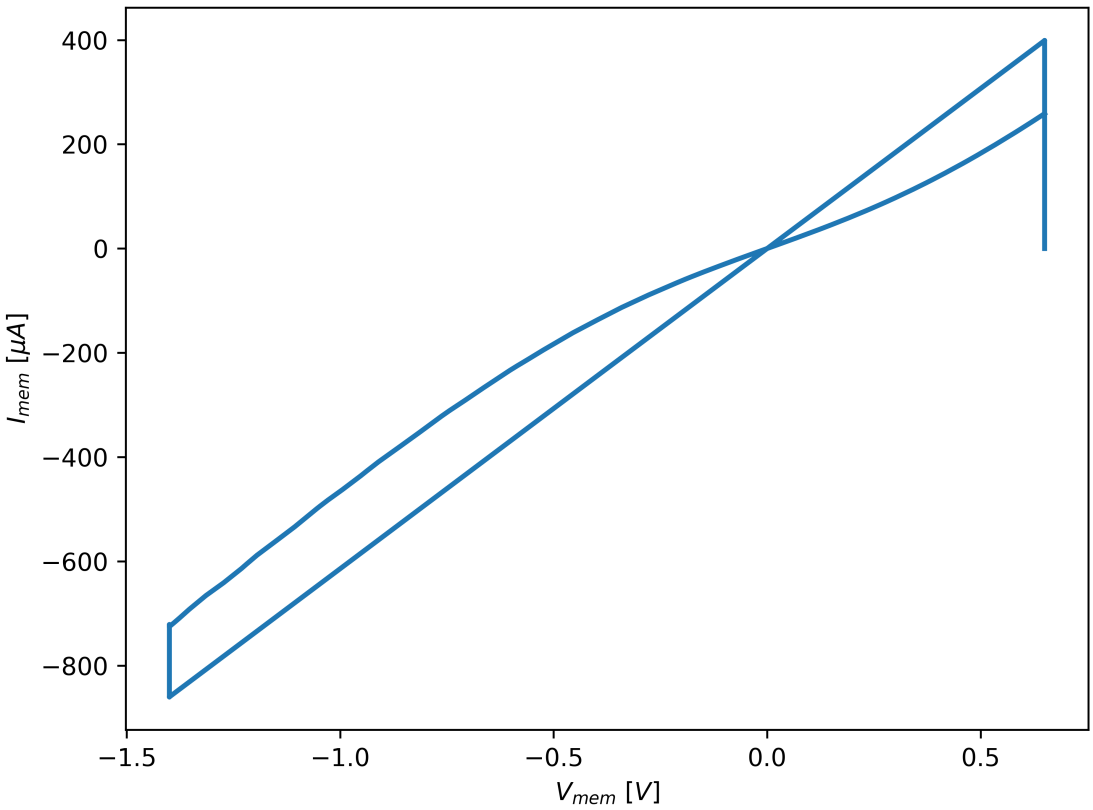


Source: Author.

In this model, the main sub-circuit converts the voltage across the MTJ electrodes in a current source I_{IMTJ}, which is depicted in Figure 5.3. Therefore, the PWL source was a voltage source illustrated in V_{MTJ} signal.

In order to avoid the thermal-assisted effect, this simulation was performed using a pulse width smaller than 10ns with the TMR bias voltage ($V_{bias} = 0.65V$. The results show that the electric current to switch from $R_{off} \rightarrow R_{on}$ is higher than 250μA. The instability presented in the easy-axis trajectory during the switching time are replicated in the electric current waveform. In addition, it presents an asymmetric switching shape; thus, the current threshold to revert the magnetization from $R_{on} \rightarrow R_{off}$ is higher than R_{off} to R_{on} transition.

Figure 5.4 – Pinched Hysteresis Loop - UMN IMTJ Model.



Source: Author.

This asymmetric switching, depicted in Figure 5.4, is related to the differences between the spin torque current when the MTJ turns from parallel state to antiparallel. In this case, the behavior is mainly governed by the voltage-dependent source I_{as}, which is fed back to the LLG module to compute the spin torque A_{stt}. A current sensor within the TMR module and the external nodes of MTJ implements the absolute ratio between these thresholds, as shown below.

$$I_{as} = \left(1 + \frac{V_{plus} - V_{minus}}{|V_{plus} - V_{minus}|}\right)\left(\frac{I_{atp} - I_{pta}}{2}\right) + I_{pta} \tag{5.1}$$

I_{atp} is the electric current to change the state from HRS to LRS, and I_{pta} refers to the change from LRS to HRS. When $I_{as} = I_{pta}$ the spin torque current becomes smaller due to the condition $I_{pta} = 2I_{atp}/3$.

$$R_{Is} = \frac{\hbar P J_{c0}}{2eM_s}, J_{c0} = \frac{I_{as}}{l_x l_y l_z} \tag{5.2}$$

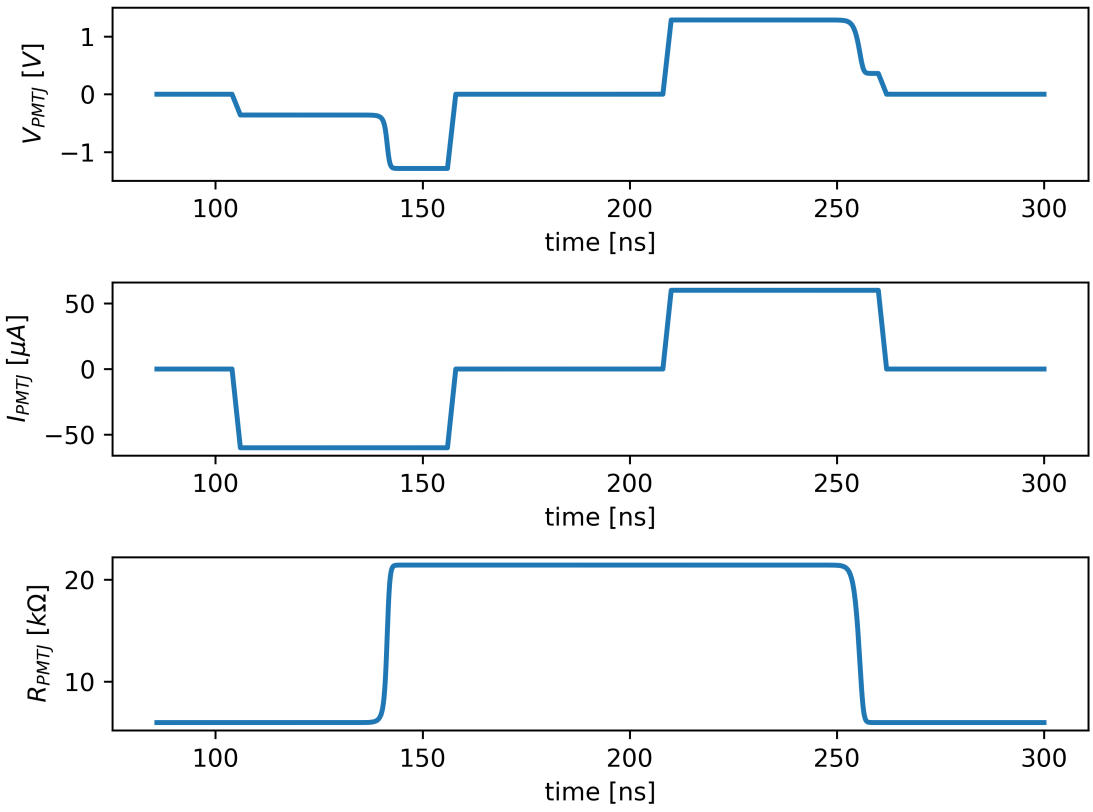
Where R_{Is} is the resistance connected to the current flowing into the MTJ, through the external nodes of the main sub-circuit.

5.2.1.3 PMTJ

Figure 5.5 exhibits the results of transient analysis for the PMTJ Model. In this case, the PWL source is a current source presented in the signal I_{PMTJ}. In this simulation, the thermal windowing was disabled, and the VCMA effect was turned off ($H_{vcma} = 0\ \hat{e}_z$) to accomplish better measurements of STT effect along the switching process.

Due to the partial field canceling in the MA, the total energy to change the memristance in this technology of MTJ is smaller compared to in-plane anisotropy.

Figure 5.5 – Switching Shape - PMTJ Model.



Source: Author.

As a result, the electric current required to change the memristor state is smaller than in IP anisotropy. This effect is better depicted in the critical current density expression shown below.

$$J_{c0} = \frac{1}{\eta}\frac{2\alpha e}{\hbar}(M_s t)(\frac{1}{2}4\pi M_{eff} + H_K) \tag{5.3}$$

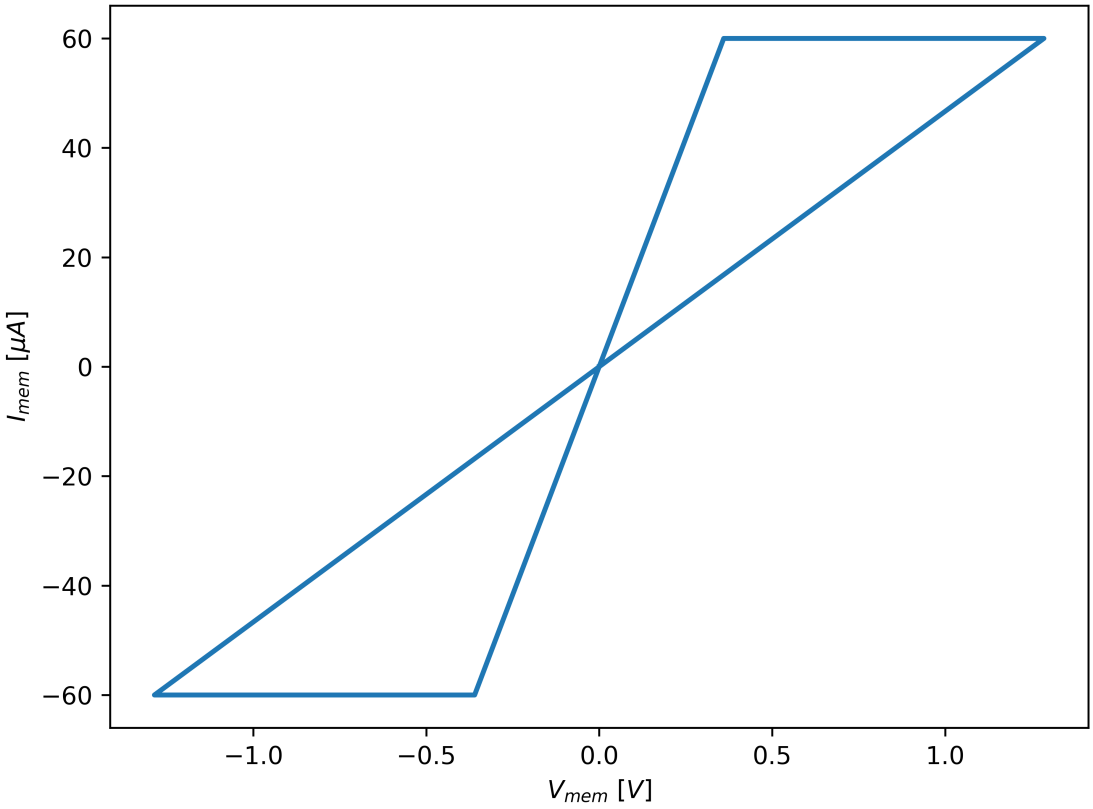
Where J_{c0} is the current density at which the STT overcomes the damping term, resulting in a magnetization excitation (ZHANG et al., 2020). The term $4\pi M_{eff}$ is the effective demagnetizing field, H_K is the shape anisotropy field. For a uniform switching

approximation, the critical current density for perpendicular MA causes $M_{eff} = 0$.

$$J_{c0} = \frac{1}{\eta}\frac{2\alpha e}{\hbar} M_s t H_K \tag{5.4}$$

In this simulation, the magnitude of I_{PMTJ} is about $50\mu A$ ($\approx 20\%$ of the value achieved with IMTJ). Figure 5.6 shows the results for the hysteresis loop simulation.

Figure 5.6 – Pinched Hysteresis Loop – STT PMTJ Model.



Source: Author.

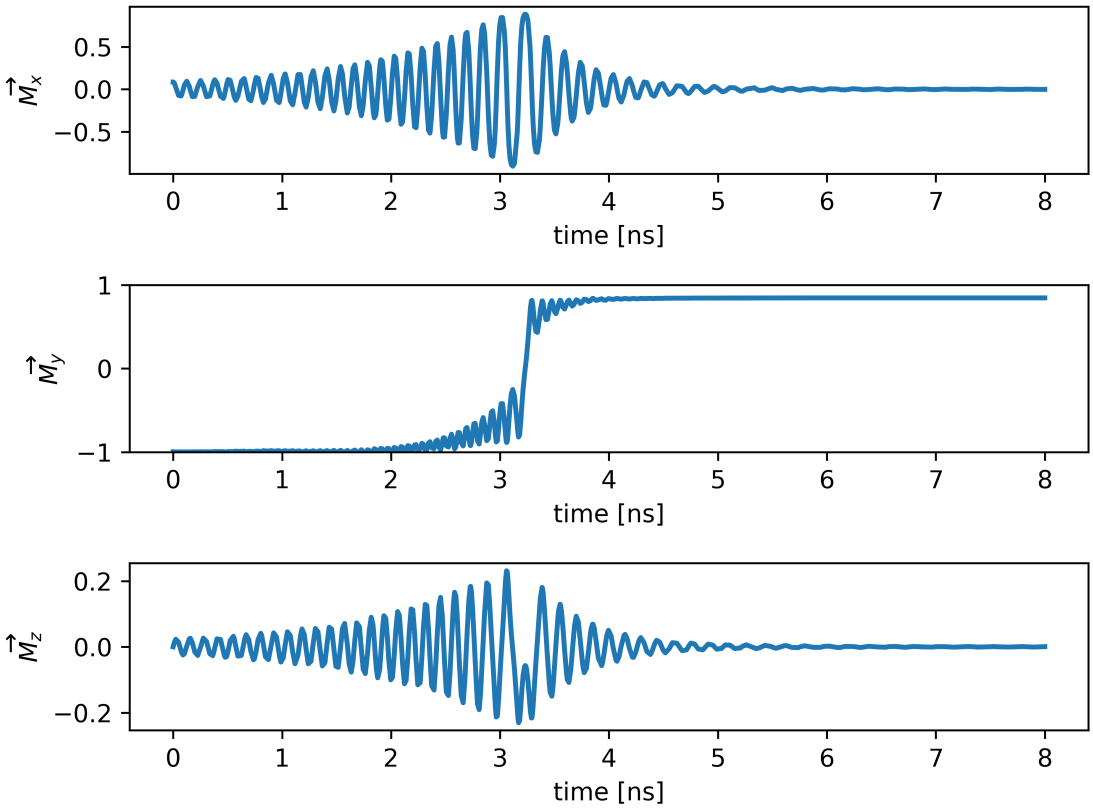
Although this model can be integrated with the micromagnetic simulation of the FM layers provided by the Object Oriented MicroMagnetic Framework (OOMMF), it does not enforce the asymmetric switching form. However, STT field can be computed in both layers, not only for the free layer.

This model endorses three options of STT constants: in the first method, the polarization of the free layer is different from the pinned layer. The second one explores the exact approximation given in UMN Model, in which both polarization factors have identical values. The last one, the STT factor, uses fitting parameters, although the polarization factor for both layers is considered the same.

5.2.2 Magnetization Motion

As previously mentioned, the magnetization stays in a different direction depending on the MA of the material. In the last subsection, the switching shape was presented, and it was assumed that the current/voltage shape might present the same pattern shown in the easy-axis deviation.

Figure 5.7 – UMN IMTJ – Magnetization trajectory in a single switching.



Source: Author.

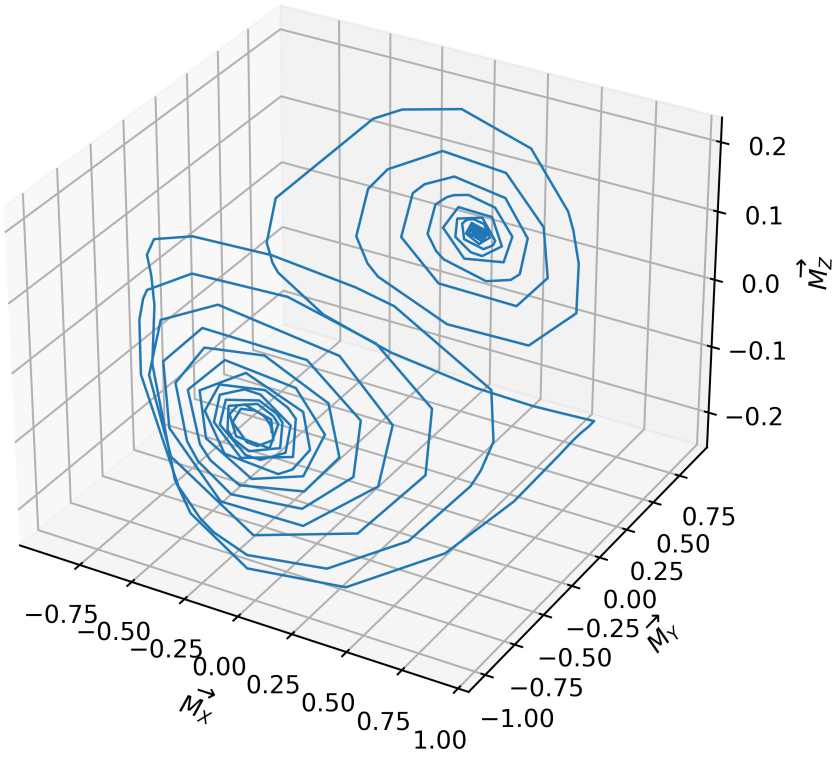
The results of Figure 5.7 show that the voltage waveform demonstrated in the last subsection is comparable to the temporal magnetization trajectory on the easy axis ($\hat{e}_y$). When starting the switching process, $\overrightarrow{M_y} = -1$ and once completed, it is totally flipped $\overrightarrow{M_y} = 1$. The other components may present oscillations around each other. However, they return to steady state $\overrightarrow{M_x} = \overrightarrow{M_z} = 0$.

When the spin torque field is much higher than the minimum required to revert to the easy axis, the magnetization along the hard axis can achieve the highest/lowest value, i.e. $M_z = M_x = 1$ or $M_z = M_x = -1$. However, only the easy axis will maintain the reversed state. This behavior is depicted in Figure 5.9.

The 3D view of magnetization motion for a single switching ($HRS \rightarrow LRS$) is

represented in Figure 5.8. It shows that the precession effect is higher when the easy-axis of magnetization gets closer to the boundaries $\theta = 180$ or $\theta = 0$, and this effect decreases when it get closer to reverse.

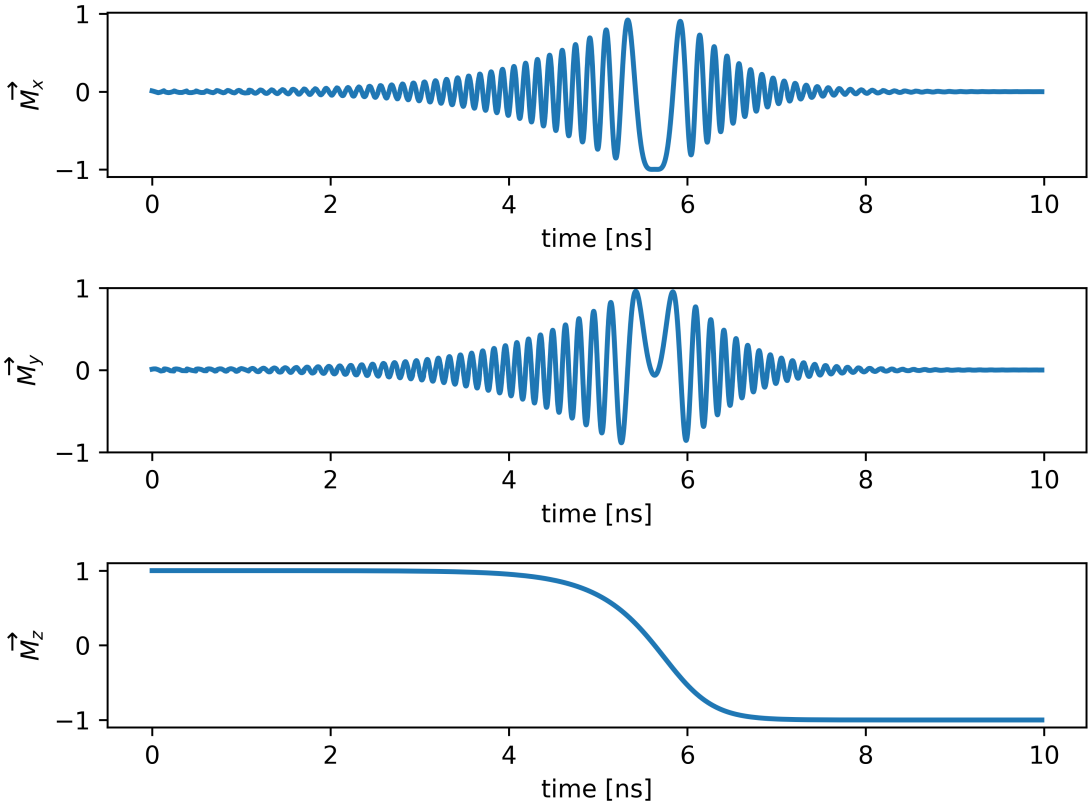
Figure 5.8 – UMN IMTJ – Reversal of magnetization in a single switching.



Source: Author.

For the PMTJ, the easy-axis stays out-of-plane ($\hat{e}_z$ direction). As predicted, the easy axis presents fewer oscillations. This behavior is related to the perpendicular field and the thermal stability, which is usually more elevated in PMAs. The writing current is also expressed in terms of relative angle deviation, with the DC offset presented by Ohm's Law dependency.

Figure 5.9 – PMTJ – Magnetization trajectory in a single switching.

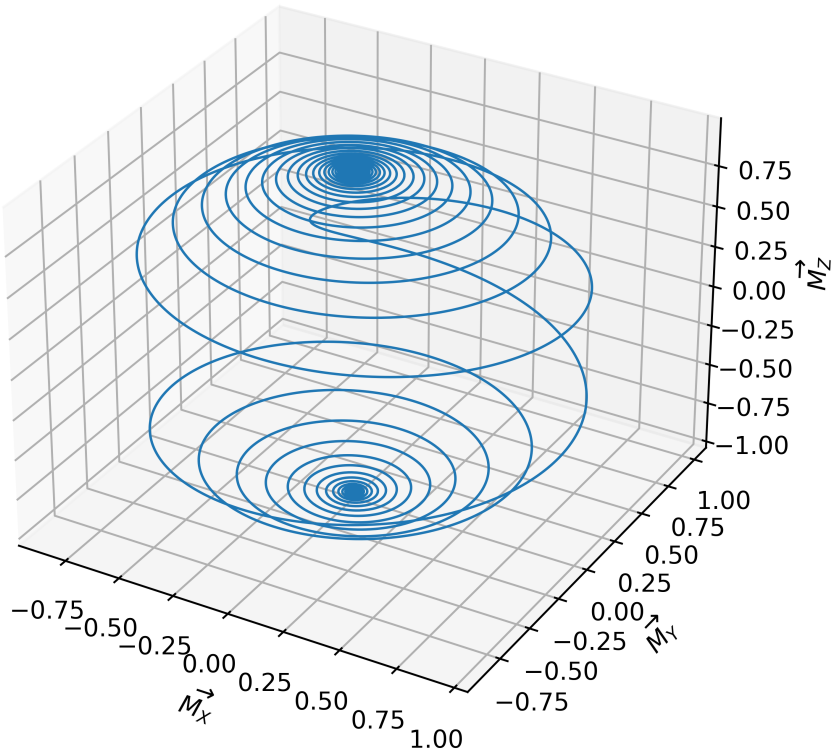


Source: Author.

In this simulation, I_{PMTJ} is much higher than the critical current. Therefore, M_x and M_y reach the values 1 and -1, but they return to a steady state, while the easy axis M_z keeps the fully reversed, as shown in Figure 5.9.

The results for the magnetization trajectory in a single switching (3D view) are depicted in Figure 5.10.

Figure 5.10 – PMTJ – Reversal of magnetization in a single switching.



Source: Author.

The Pershin based Current threshold model is inspired on TiO_2 memristor, there is no magnetization motion presented, and the ionic migration $x(t)$ is depicted in the previous memristance waveform.

5.2.3 STT Efficiency versus TMR

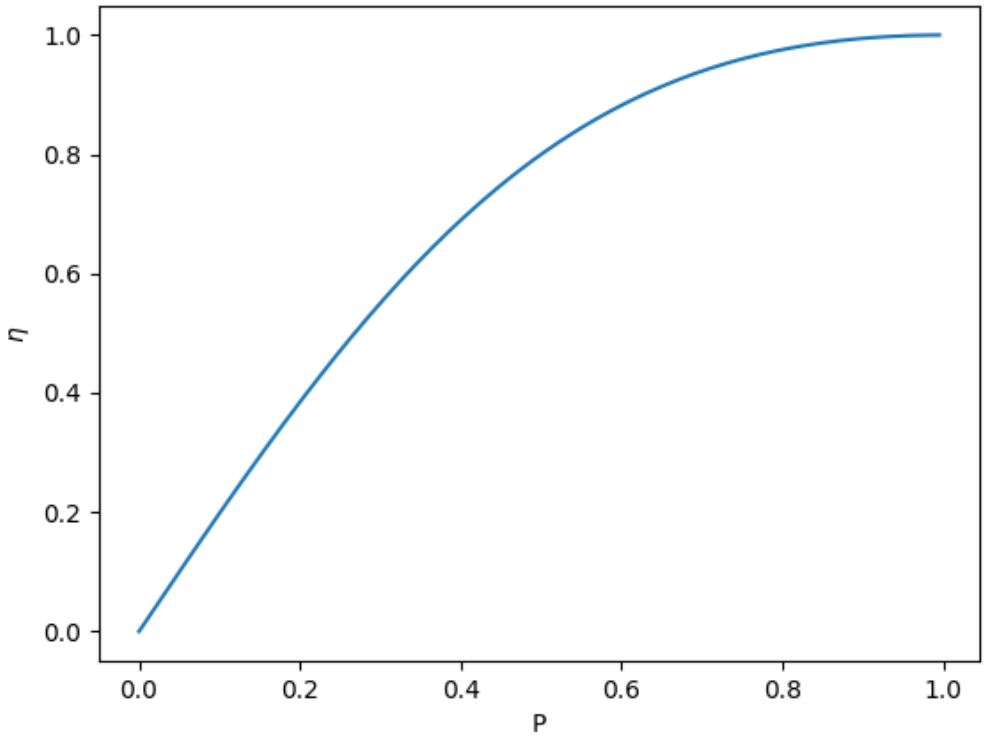
The STT Efficiency η is a function of the band structure of both electrodes, and the barrier, including the bias and the micromagnetic structure (KHVALKOVSKIY et al., 2013). However, it is often considered a function of the barrier and the current polarization beyond the multilayered films. Assuming a symmetric junction and inelastic tunneling. The STT efficiency is predicted in terms of the polarization factor P, as shown in the equation 5.5.

$$\eta = \frac{2 \cdot P}{(1 + P^2)} \tag{5.5}$$

Increasing the polarization factor, the spin torque efficiency increases, as shown

in figure 5.11. However, this relationship can be more complicated due to the heat diffusion and the significant flow of electrons from the pinned layer into the free layer (KHVALKOVSKIY et al., 2013). This typical characteristic contributes to the asymmetric threshold, which means that the electric current to revert the easy axis may be smaller depending on the flow direction. In addition, the TMR depends on polarization; thus, all characteristics are mutually exploited as a fundamental part of the conductance. This analog behavior is the core feature of memristor applications for CIM architectures.

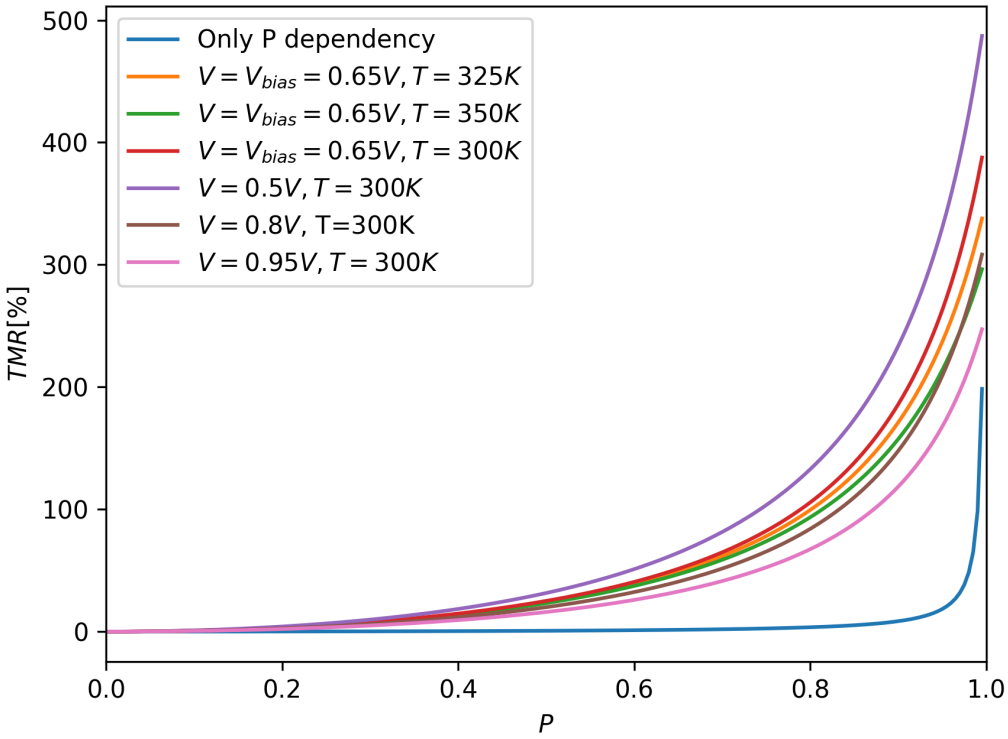
Figure 5.11 – STT efficiency in terms of polarization factor.



Source: Author.

The analytical implementation of the TMR-related polarization, depicted in the figure 5.12, explores the equation 3.18 presented in chapter 2, which realizes the TMR in terms of temperature and the applied voltage. Similarly, the PMTJ model is implemented using a similar equation, although it does not account for the bias voltage and the thermal fluctuations.

Figure 5.12 – Polarization versus TMR.



Source: Author.

Figure 5.12 shows that the TMR effect implemented in PMTJ model has lower susceptibility to the polarization factor due to the absence of thermal and TMR bias effects. Therefore, it will present almost the same ratio for lower polarization values. On the other hand, we can consider that the accounting of bias and temperature enables the memristor model to achieve higher TMR and STT efficiency.

The IMTJ model has a TMR bias voltage of $0.65V$, and the iteration (T=300K, T=325K, and T=350K) is depicted in Figure 5.12. This figure shows that the thermal effect does not significantly affect the MTJ conductance. Nevertheless, it induces the memristance change with the assisted switching (larger pulses of electric current $t_{width} >> t_{width-stt}$).

The Current Threshold model does not have the TMR effect, and does not even consider the thermal noises. However, the same memristance ratio may be replicated by Kp_n parameter when M reaches the boundaries R_{on} and R_{off}.

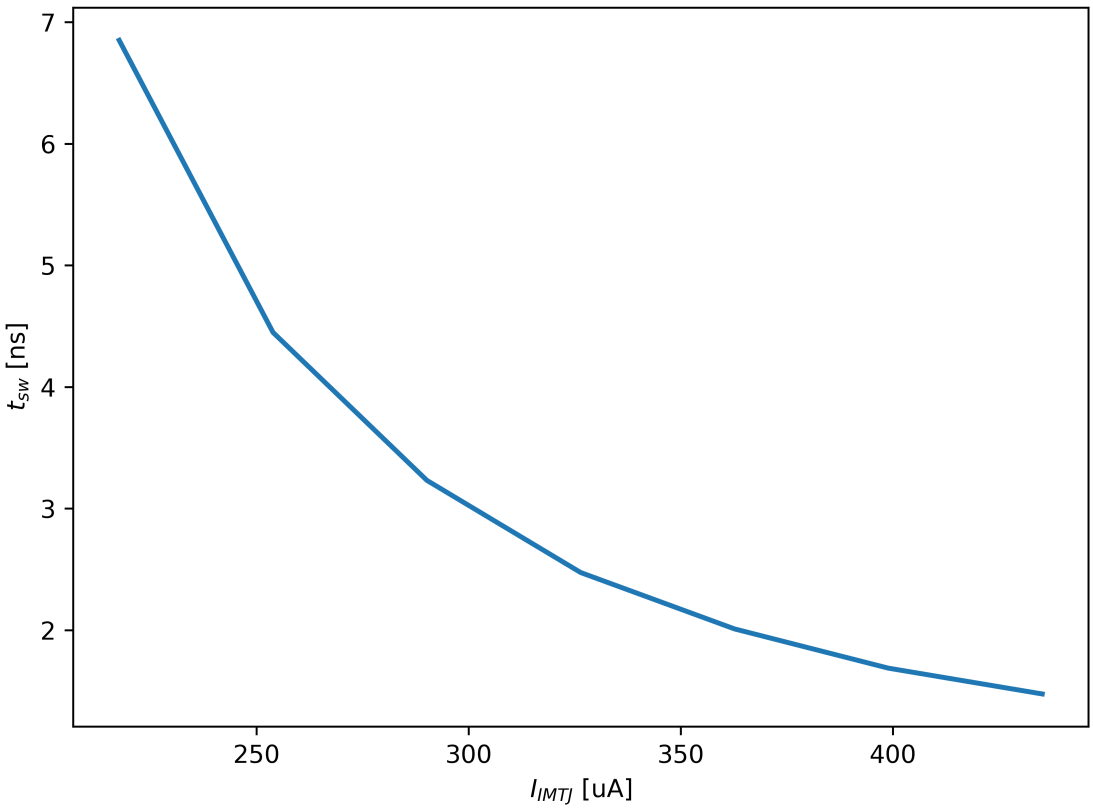
5.3 Power and Timing Measurements

This section covers the results related to the performance analysis of the selected models.

5.3.1 Switching Time

For the IMTJ model, increasing the source magnitude, the switching process becomes faster. This phenomenon is depicted in the Figure 5.13, which is a result of sweep analysis over the bias voltage.

Figure 5.13 – STT IMTJ - switching time x electric current



When the bias voltage is higher, the current flowing through the MTJ is also higher, producing a more spin-polarized current. This effect occurs because the spin torque is a function of current density (KHVALKOVSKIY et al., 2013), as follows:

$$\Gamma_{STT} = -\gamma\eta\frac{\hbar}{2}\frac{J}{e}\frac{1}{M_s t}\hat{m}\times\hat{m}\times\hat{m_{RL}} \tag{5.6}$$

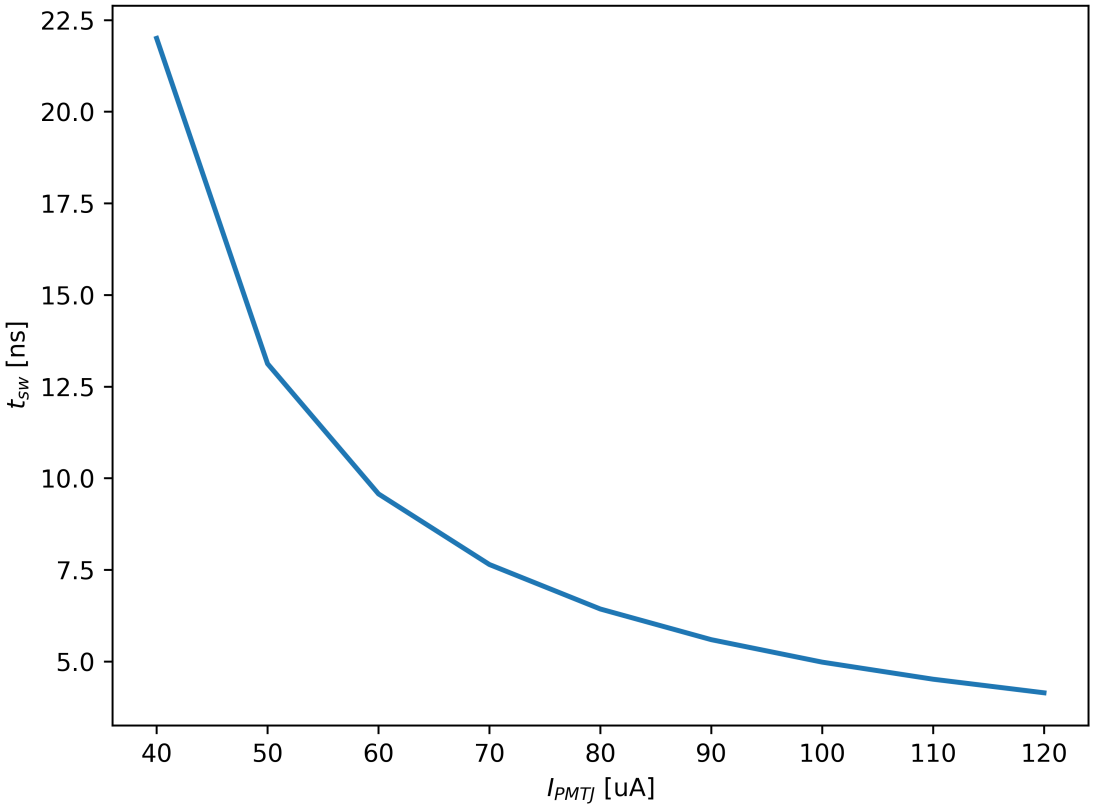
Where $\eta/(\hbar/2)$ is the average carrier angular momentum, η is the STT-efficiency, J/e is the number of electrons per unit area that enters the FM layer. γ is the gyromagnetic ratio. The term $\gamma\eta\frac{\hbar}{2}\frac{J}{e}$ is the total net flow of magnetization into a unit area, and its ratio multiplied by the magnetic moment $M_s t$ results in the torque magnitude. $\hat{m_{RL}}$ is the normalized magnetization of the pinned layer, which accounts for the fact that the free layer can absorb only the transverse part of the incoming angular momentum (KHVALKOVSKIY et al., 2013).

For the IMTJ model, the absolute torque value is computed by the voltage across R_{Is}. Similarly, one of the resources to revert the magnetization in the PMTJ model is the Spin Transfer Torque. This model also uses the current density to measure the STT effect. For this approach, the simple STT factor was chosen, and therefore the spin torque factor is implemented using the following expression:

$$STT_{factor} = \frac{\hbar}{\mu_0 e M_s V} \tag{5.7}$$

Where V refers to the free layer volume. This choice enables the computation of STT using physical fitting parameters provided by previous micromagnetic simulation.

Figure 5.14 – STT PMTJ - switching time x electric current

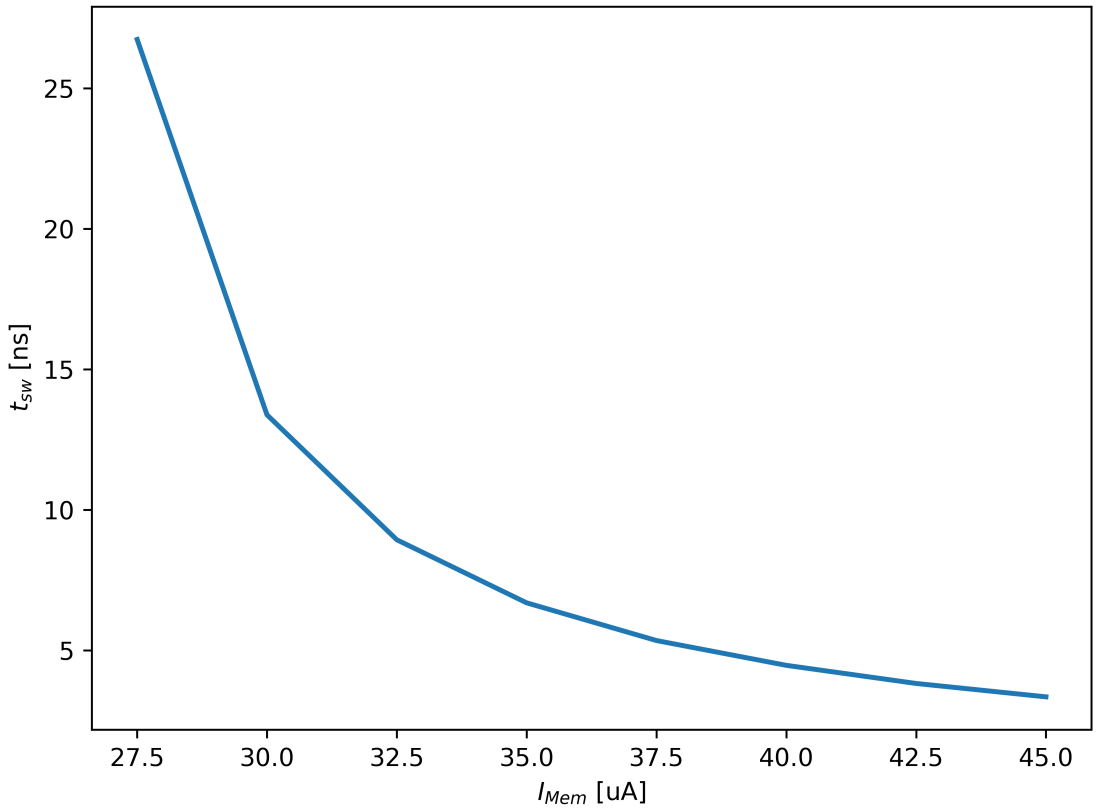


The Equation 5.7 works similarly to the resistor R_{Is} in IMTJ model (see Equation 5.2), and the s-LLG solver computes the STT magnitude using the current through the MTJ multiplied per STT factor. Nevertheless, they may be different once the effective field is calculated using an approximation of STT efficiency by the polarization factor (IMTJ model has $\eta \approx P$), which is not the case for the PMTJ.

As a result, the spin torque may be higher for small polarization factor values due to this relationship's order. Also, the switching time becomes faster as the STT field achieves higher values. The Figure 5.14 shows that for a ratio of $50\mu A$ there is a significant reduction in time, and for a $t_{sw} \approx 5ns$, the critical current is almost half compared to the IMTJ.

The measurements for the T_iO_2 model shows that the switching time approaches faster than the other STT-based technology models, this faster switching occurs due to the f_n function that increases faster as the i_{mem} is higher.

Figure 5.15 – Current threshold - switching Time x electric current



When $i_{mem} >> I_t$ the absolute value returned by f_n increases, the current through B_x approaches high values faster and as a result, the voltage across the capacitor is higher.

For small steps of $2.5\mu A$, this model achieves less than $5ns$ of switching time with

almost $40\mu A$, which combines the best of both worlds, high-performance and low-power consumption.

5.3.2 Average Power Consumption

The Table 5.2 presents the results for the sweep analysis for the average power measurements. As expected, the PMTJ model presented lower measurements than the IMTJ, mainly related to the anisotropy shape that affects the critical current.

Table 5.2 – Average Power required for a single switching.

$\mathbf{T_iO_2}[\mu A]$	***Power*** $[\mu W]$	***PMTJ*** $[\mu A]$	***Power*** $[\mu W]$	***IMTJ*** $[\mu A]$	***Power*** $[\mu W]$
30.00	9.49	60.00	40.87	230	140.29
32.50	10.40	70.00	57.91	280	201.71
35.00	13.12	80.00	77.96	340	275.97
37.50	15.39	90.00	100.06	400	364.25
40.00	16.03	100.00	125.58	460	465.55
42.50	19.28	110.00	154.71	530	580.04
45.00	22.47	120.00	185.32	600	708.46

Source: Author.

The measurements of the T_iO_2 model show that the power required to switch the memristor is significantly smaller than the other models due to the current threshold of $25\mu A$.

5.4 IMPLY

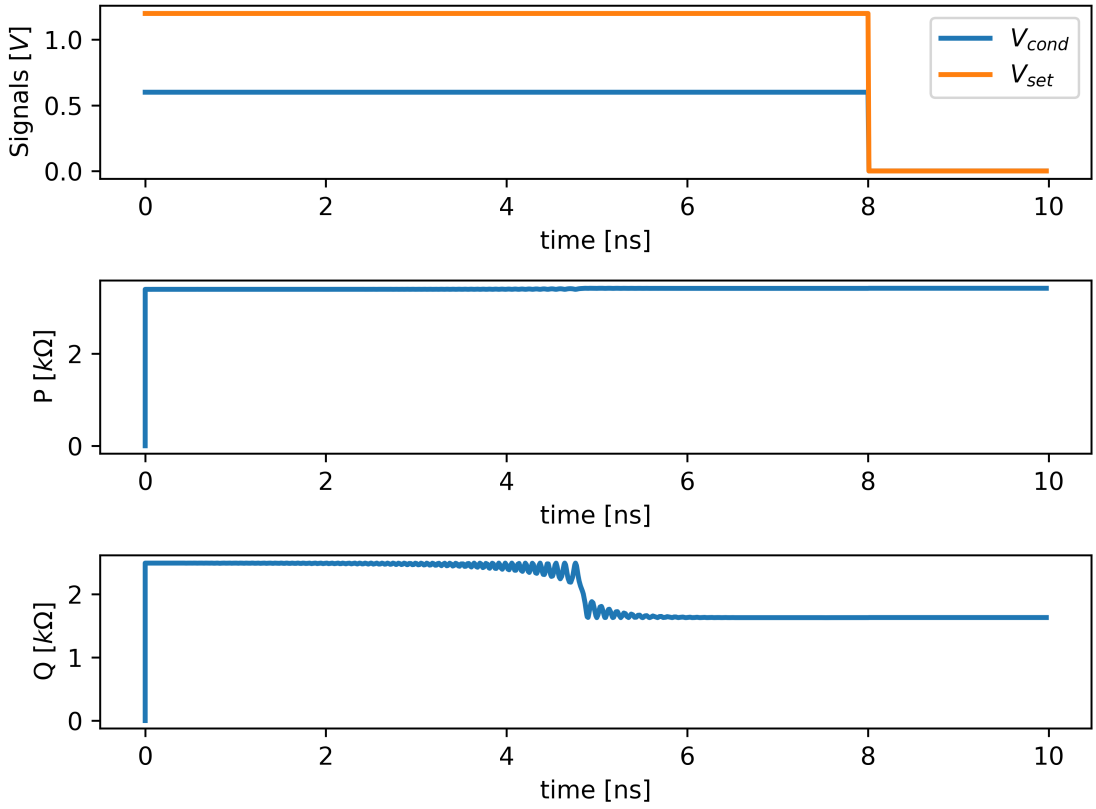
According to chapter 2, the material implication is one of the logic families for in-memory computing. In order to realize a basic imply operation using two NVM bit cells, a new SPICE sub-circuit with two memristors for each model was created. Where the R_G, V_{SET} and V_{COND} were dimensioned to meet the following requirements:

- $R_{on} < R_G < R_{off}$
- $V_{SET} - V_{COND} < V_{CLEAR}$

For the IMTJ model, $R_G = 1.8k\Omega$, as it must be between the R_{off} and R_{on} value. This choice can be more complicated when turning into larger circuits, as the TMR

showed a dependency on the applied voltage and the temperature. To attend the second item, $V_{SET} = 1.2V$ and $V_{COND} = 0.6$ were implemented through the transmission gates described in chapter 4, and therefore, V_{CLEAR} has the minimum value required to turn on/off the memristor state.

Figure 5.16 – P→Q - IMTJ Model.

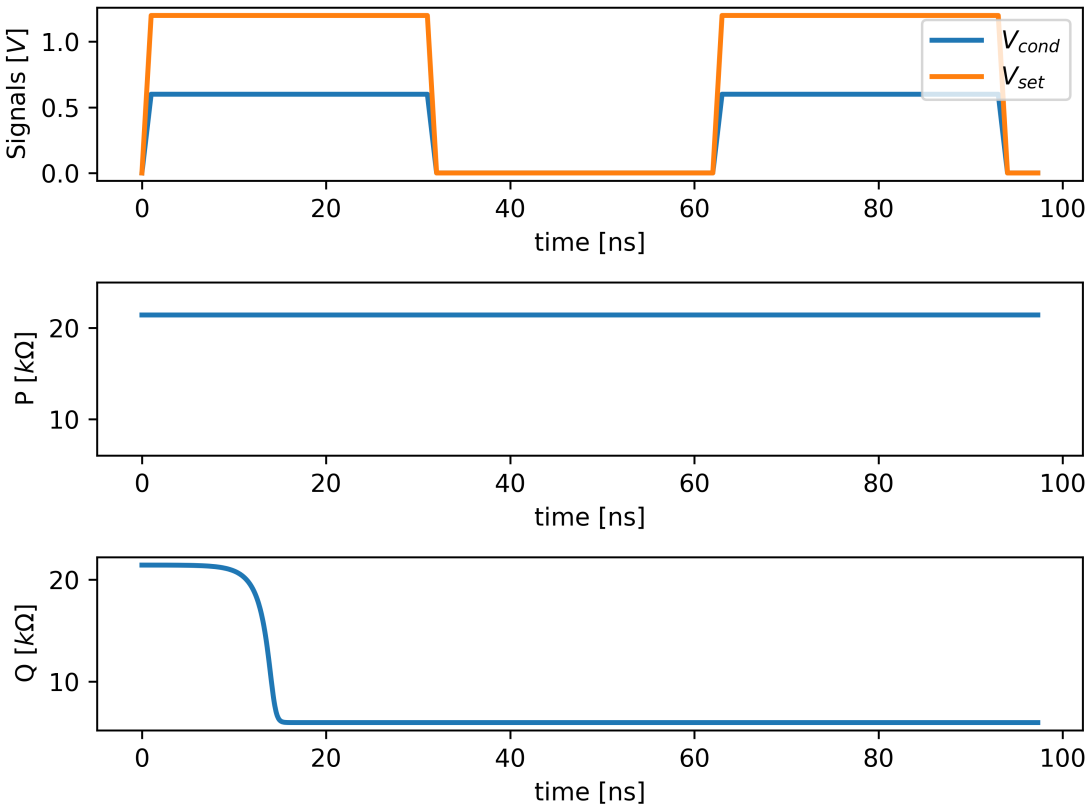


Source: Author.

The result depicted in Figure 5.16 shows the first case of the truth table presented in Chapter 2 (2.1). The result of $p \rightarrow q$ is written in the memristor Q at $\approx 5ns$. Here, R_{off} is the logic '0', whereas R_{on} is the logic '1'.

For the PMTJ model, the results are depicted in Figure 5.17. The first and second cases of the truth table (2.1) are shown below. In this simulation, the IMPLY sub-circuit has $R_G = 10k\Omega$, the controls signals $V_{SET} = 1.2V$ and $V_{COND} = 0.6V$.

Figure 5.17 – P→Q - PMTJ Model.

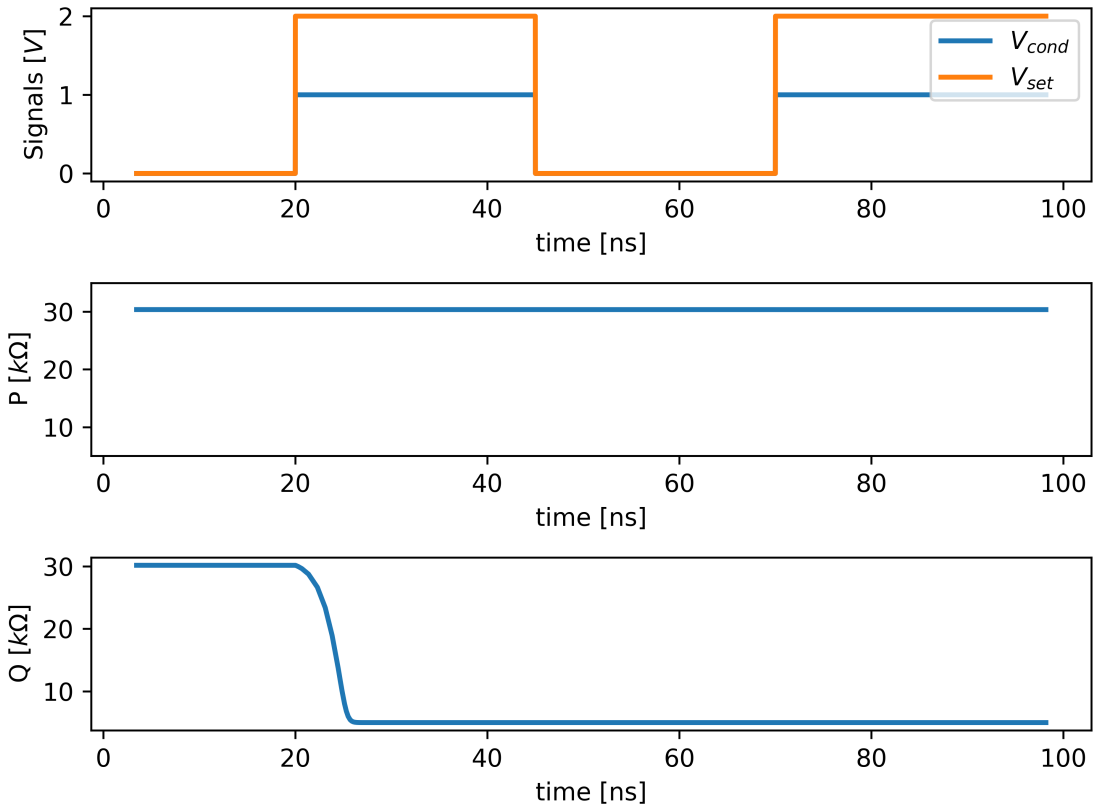


Source: Author.

At $\approx 15ns$ the implication changes the memristor Q to the logical state '1' (R_{on}). When the signals V_{SET} and V_{COND} rise again (at $\approx$ 60ns), the memristor P and Q store, respectively, the logic '0' and '1'. Therefore, the memristor Q will not change the memristance, and the result of the implication can be read again in the memristor Q.

To realize the next step of the truth table, the memristor P and Q require overwriting the internal logic. This refresh or logic overwrite command in the material implication leads to complex peripheral circuits when we treat multiple implication operations with larger crossbar arrays.

Figure 5.18 – P→Q - Current threshold-based Pershin Model.



Source: Author.

The results for the sub-circuit using two bit cells with T_iO_2 model are shown in Figure 5.18, where $R_G = 10k\Omega$ and the case 1 and 2 occurs, respectively, in $\approx 20ns$ and $70ns$.

6 CONCLUSION AND FUTURE WORKS

The current work aimed to create an environment of SPICE models to allow circuit designs using memristive devices with commercial tools. For this purpose, the compact models of different NVM technologies were detailed, and they were evaluated in terms of implementation, performance, and usage. The UMN MTJ Model required some changes to avoid convergence issues; therefore, all sub-circuits were ported to the Spectre language, and a similar refactoring process was required for the Current threshold-based Pershin model (KLAUDAT, 2022).

In addition, *Python* scripts were developed to provide a separate view of specific steps of those implementations, such as the STT efficiency versus the polarization factor and the TMR effect, which are essential elements in the presented models. These scripts help design hybrid systems, as both models present customizable input parameters such as the polarization factor, initial temperature, and resistance.

The presented results show that the perpendicular-based anisotropy has better power and performance metrics than the in-plane shape. This finding is expected behavior due to the MA anisotropy field H_k. Although the PMTJ does not enforce asymmetric switching, it is still feasible to design circuits once the free-layer modeling is the most critical part of building memristors within the circuit simulators. The Verilog description of PMTJ offers a customizable analysis with different implementations, leading to a reliable model for building different hybrid systems. The T_iO_2 presented the best measurements for both worlds: power consumption and high-speed applications. However, it is less detailed in physical components and offers less customizable input properties, which can lead to non-real scenarios of design.

REFERENCES

ALI, K. A. **New design approaches for flexible architectures and in-memory computing based on memristor technologies**. Thesis (PhD) — Ecole nationale supérieure Mines-Télécom Atlantique, 2020.

BIOLEK, Z.; BIOLEK, D.; BIOLKOVA, V. Spice model of memristor with nonlinear dopant drift. **Radioengineering**, v. 18, n. 2, 2009.

BORGHETTI, J. et al. 'memristive'switches enable 'stateful'logic operations via material implication. **Nature**, Nature Publishing Group, v. 464, n. 7290, p. 873–876, 2010.

BORGHETTI, J. et al. Electrical transport and thermometry of electroformed titanium dioxide memristive switches. **Journal of Applied Physics**, American Institute of Physics, v. 106, n. 12, p. 124504, 2009.

DIAS, C. d. S. **Aplicação da tecnologia memresistiva ao projeto de sistemas digitais através da exploração de circuitos híbridos e implicação material**. Dissertation (Master), 2018.

DUAN, S. et al. Analog memristive memory with applications in audio signal processing. **Science China Information Sciences**, Springer, v. 57, n. 4, p. 1–15, 2014.

GALE, E. Tio2-based memristors and reram: materials, mechanisms and models (a review). **Semiconductor Science and Technology**, IOP Publishing, v. 29, n. 10, p. 104004, 2014.

GARCIA-REDONDO, F. et al. A compact model for scalable mtj simulation. In: VDE. **SMACD/PRIME 2021; International Conference on SMACD and 16th Conference on PRIME**. [S.l.], 2021. p. 1–4.

GREENBERG-TOLEDO, T. et al. Supporting the momentum training algorithm using a memristor-based synapse. **IEEE Transactions on Circuits and Systems I: Regular Papers**, IEEE, v. 66, n. 4, p. 1571–1583, 2019.

HARRIS, C. R. et al. Array programming with NumPy. **Nature**, v. 585, p. 357–362, 2020.

HUNTER, J. D. Matplotlib: A 2d graphics environment. **Computing in Science & Engineering**, IEEE COMPUTER SOC, v. 9, n. 3, p. 90–95, 2007.

JI, Y. **Modeling, Dynamic Simulation and Design of Magnetic Sensors Based on Magnetic Tunnel Junction Technology**. Thesis (PhD) — Carleton University, 2013.

JOGLEKAR, Y. N.; WOLF, S. J. The elusive memristor: properties of basic electrical circuits. **European Journal of physics**, IOP Publishing, v. 30, n. 4, p. 661, 2009.

KHVALKOVSKIY, A. et al. Basic principles of stt-mram cell operation in memory arrays. **Journal of Physics D: Applied Physics**, IOP Publishing, v. 46, n. 7, p. 074001, 2013.

KIM, J. et al. A technology-agnostic mtj spice model with user-defined dimensions for stt-mram scalability studies. In: IEEE. **2015 IEEE custom integrated circuits conference (CICC)**. [S.l.], 2015. p. 1–4.

KLAUDAT, P. **Memristors**. 2022. Available from Internet: <https://github.com/pklaudat/memristors>.

KVATINSKY, S. et al. Memristor-based material implication (imply) logic: Design principles and methodologies. **IEEE Transactions on Very Large Scale Integration (VLSI) Systems**, IEEE, v. 22, n. 10, p. 2054–2066, 2013.

MLADENOV, V. The fourth element or the missing memristor. In: IEEE. **12th Symposium on Neural Network Applications in Electrical Engineering (NEUREL)**. [S.l.], 2014. p. 1–1.

PERSHIN, Y. V.; VENTRA, M. D. Practical approach to programmable analog circuits with memristors. **IEEE Transactions on Circuits and Systems I: Regular Papers**, IEEE, v. 57, n. 8, p. 1857–1864, 2010.

STRUKOV, D. B. et al. The missing memristor found. **nature**, Nature Publishing Group, v. 453, n. 7191, p. 80–83, 2008.

SYSTEMS, C. D. **SPICE Reference Guide**. [S.l.]: Cadence Design Systems Inc San Jose CA, 2004.

TANG, D. D.; LEE, Y.-J. **Magnetic memory: fundamentals and technology**. [S.l.]: Cambridge University Press, 2010.

WANG, L. et al. Overview of emerging memristor families from resistive memristor to spintronic memristor. **Journal of Materials Science: Materials in Electronics**, Springer, v. 26, n. 7, p. 4618–4628, 2015.

WANG, R. et al. Recent advances of volatile memristors: Devices, mechanisms, and applications. **Advanced Intelligent Systems**, Wiley Online Library, v. 2, n. 9, p. 2000055, 2020.

XU, W.; FRIEDMAN, E. G. Clock feedthrough in cmos analog transmission gate switches. In: IEEE. **15th Annual IEEE International ASIC/SOC Conference**. [S.l.], 2002. p. 181–185.

YU, S. et al. Compute-in-memory chips for deep learning: Recent trends and prospects. **IEEE Circuits and Systems Magazine**, IEEE, v. 21, n. 3, p. 31–56, 2021.

ZHANG, K. et al. Compact modeling and analysis of voltage-gated spin-orbit torque magnetic tunnel junction. **IEEE Access**, IEEE, v. 8, p. 50792–50800, 2020.