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Design of a Near-Threshold Digital Library at 0.3 V in CMOS 28 nm

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Introduction

- To design a digital standard-cell library capable of operating at the Minimum Energy Point (MEP) (Voltage Supply around 300mV).
- To explore new Near-Threshold Voltage (NTV) library design methods.

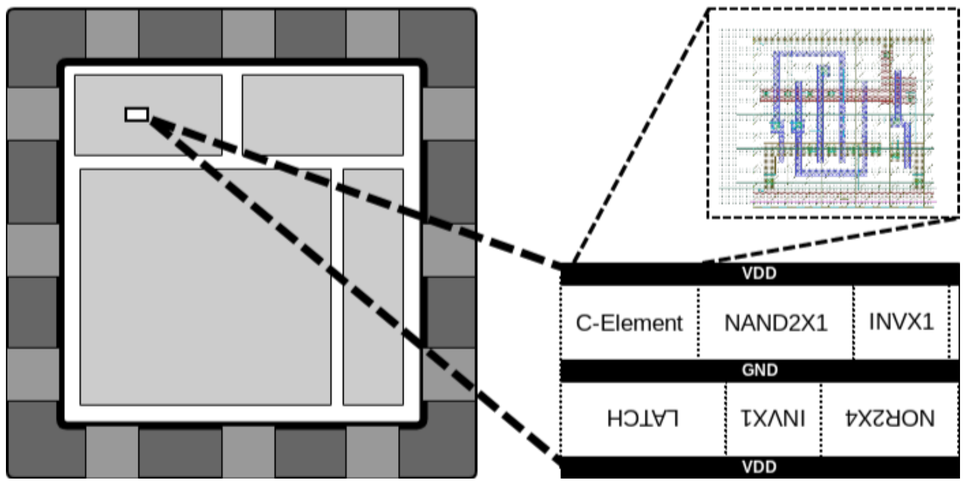

Figure 1: Representation of a cell-based design.

Library Development Workflow

- **State of the Art Review ✓**
- **Evaluate Transistor Sizing Methodologies ✓**
- **Develop Library SPICE Descriptions ✓**
- **Cell Library Characterization - In Progress**
- **Layout Generation**
  - Design Rules Check - DRC
  - Layout Versus Schematic - LVS
  - Parasitic Extraction - PEX
- **Multi-Corner Characterization**

Table 1: Target Corners

Corner	Temperature (C)	Supply Voltage (V)	Process
NTV - Worst Case	-40	0.27	Worst
NTV - Nominal Case	25	0.30	Nominal
NTV - Best Case	125	0.33	Best
Worst Case	125	0.81	Worst
Nominal Case	25	0.90	Nominal
Best Case	-40	0.99	Best

- **Test Library under a vast amount of Test Setups**
  - HDL Development and Test
    - ISCAS Benchmarks
  - Logical Synthesis
  - Physical Synthesis
  - SPICE Simulation of the Extracted Circuit
- **Tape-out (fabrication) of Test VLSI Circuits**

Table 2: Library Main Characteristics

Technology / Process Node	TSMC 28 nm
Nominal Supply Voltage	0.9 V
Target Library Supply Voltage	0.3 V
Compatibility Features	9-track commercial cells
Number of Logic Cells	31 + 7 extra*
Number of Different Functions	14

*Extra Cells are Composed by Asynchronous-friendly Cells (e.g. C-Elements)

Results

- Rodrigo N. Wuerdig, Vitor G. Lima, Filipe Baumgratz, Rafael Soares, and Sergio Bampi, **"Evaluating Cell Library Sizing Methodologies for Ultra-Low Power Near-Threshold Operation in Bulk CMOS"**, 26th IEEE ICECS, 2019, submitted.
- Rodrigo N. Wuerdig, Filipe D. Baumgratz, and Sergio Bampi, **"A 1 GHz 64b Serial Peripheral Interface for 40 nm Bulk CMOS Technology"**, 19th SForum, 2019.

$$F_1(\xi) = \frac{K_1 * std(\overline{U}) + K_2 * std\,(T_{min})}{2}, \quad (1)$$

$$F_2(\xi) = \frac{K_1 * std(Ac) + K_2 * std\,(T_{min})}{2}, \quad (2)$$

$$F_3(\xi) = \frac{K_1 * \xi + K_2 * (\overline{t_{rise}(\xi)}/\overline{t_{fall}(\xi)})}{2}, \quad (3)$$

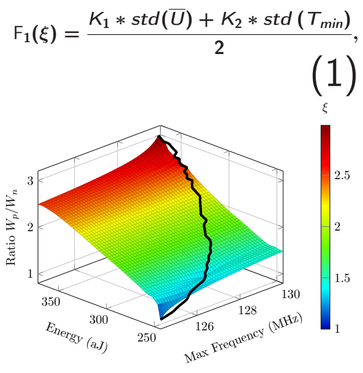

Figure 2:

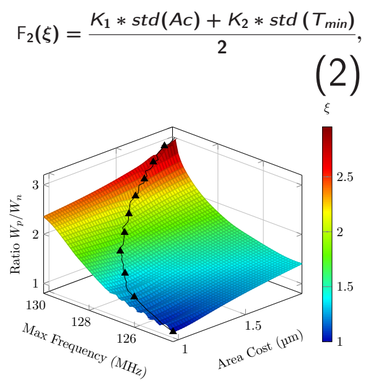

Figure 3:

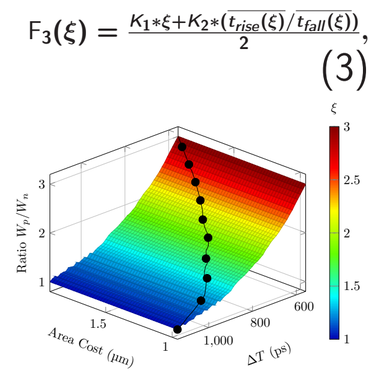

Figure 4:

Design space exploration values used to set the trade-off functions (TOFs 1,2, and 3), and TOF trajectory, for specific drive strengths and supply voltage (0.3 V in this case).

Conclusion & Future Work

The Trade-off functions (TOFs) method, proposed by Rodrigo et al., provided a transistor size that increases library cells energy efficiency relatively to commercial equivalents, and they can be used to explore bi- and three-dimensional search spaces, towards even more advanced optimization algorithms.

- Future Work
  - Improve the presented Workflow
  - Evaluate the use of dynamic threshold transistors for performance improvement under low V_{DD} regimes
  - Tape-out under a MPW program
  - Evaluate Impacts of Aging and Variability of FETs

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