A MODIFIED LIGHTLY DOPED DRAIN MOSFET FOR VERY LARGE SCALE INTEGRATION

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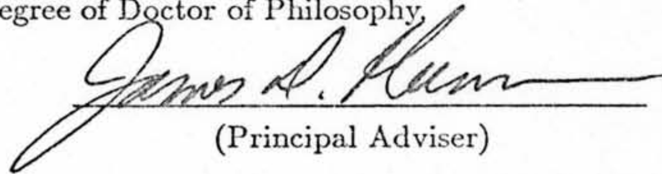

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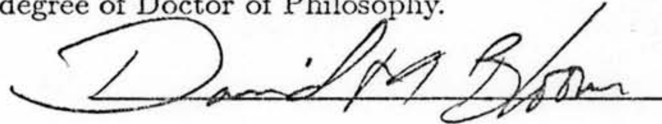

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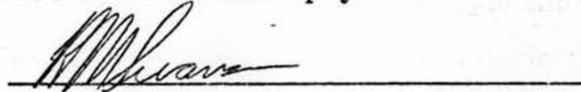

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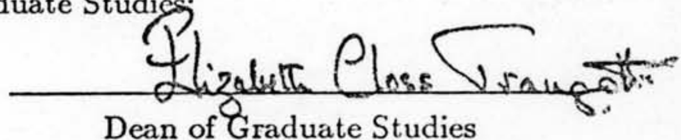

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ABSTRACT

Reducing MOSFET dimensions while maintaining a constant supply voltage leads to higher electric fields inside the active regions of VLSI transistors. Operation of micron and submicron MOSFETs in the presence of high-field effects has required design innovations so that a constant supply voltage, acceptable punchthrough voltage, and long-term reliability are possible as device scaling continues.

Drain engineering is necessary to cope with the susceptibility of MOSFETs to hot-carrier-related degradation. Reducing the electric fields at the drain end of the channel is critical to device reliability because degradation is related to carrier *heating* as they traverse regions with field strength in excess of 100 kV/cm. Optimized lightly doped drain (LDD) structures that spread the high electric field at the drain ensure the reliable 5 V operation of micron-sized n-channel MOSFETs. Recent experimental evidence revealed that LDDFETs are less reliable than conventional transistors if the n^- region is too lightly doped.

The JMOS transistor, a new n-MOS structure, is introduced to resolve the reliability problems in LDD devices with peak doping densities below $1 \times 10^{18}\text{cm}^{-3}$. A JFET is merged into the n-MOS structure to reduce the high fields under the gate. Two-dimensional simulations and experimental results demonstrate for the first time the operation of this device and its potential for VLSI applications requiring maximum supply voltage. A major experimental finding is that the JMOS can sustain 5 V operation even for submicron effective channel lengths because of the designer-controlled reduction of the maximum electrical field in the region under the gate traversed by carriers. The modification introduced in the LDD design is advantageous in terms of lower gate and substrate currents. Reliability can potentially be improved but at the expense of performance; however, the advantages of 5 V operation in micron-sized devices can outweigh this performance loss.

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List of Symbols

a width of the JFET channel

A proportionality constant for empirical scaling

d_{jd} drain junction depletion-layer width

d_{js} source junction depletion-layer width

dt infinitesimal time step

D n^- impurity dose

E_i intrinsic Fermi energy level

E_{CRIT} critical field for velocity saturation

E_f Fermi level

f_g MOSFET-JFET linear region conductance ratio

f_J S/D junction depth scaling ratio

g_{D_o} JFET linear region conductance

g_m MOSFET transconductance

g_{m_J} JMOSFET transconductance

$g_{m_{sym}}$ symmetrical JMOSFET transconductance

g_{mO} MOSFET transconductance at $t = 0$

g_{max} maximum conductance of the undepleted JFET

I_D,I_{DS} drain current

I_G gate current

I_p JFET pinchoff current

I_{p_o} JFET pinchoff current proportionality constant per unit width

I_{P_o} JFET pinchoff current proportionality constant

I_{pmax}	maximum JMOS pinchoff current
I_{SUB}	substrate current
$I_{SUB_{MAX}}$	maximum substrate current at fixed V_{DS}
κ	MOSFET scaling factor
κ_s	supply-voltage scaling factor
K_P	MOSFET transconductance factor
L_{DRAWN}	drawn mask channel length
L,L_{eff}	MOSFET effective electrical channel length
L_J	JFET effective electrical channel length
ΔL	difference between the drawn and electrical channel lengths
L_{min}	minimum effective channel length
L_{sw}	sidewall-spacer oxide length
y	space coordinate in the depth direction
n	nonuniform JFET channel doping factor
N	net impurity concentration in the JFET channel
N_{Deff}	net impurity concentration in the equivalent uniformly-doped JFET channel
N_{SUB}	effective substrate doping concentration
P	power dissipation
q	elemental charge ($= 1.6 \times 10^{-19}$ C)
Q_B	depletion-layer charge per unit area
Q_m	inversion-layer mobile charge per unit area
Q_{net}	net n^- impurity dose in the JFET channel
r_J	undepleted-channel JFET resistance per unit width
R_D	drain parasitic series resistance
R_S	source parasitic series resistance
R_T	total parasitic series resistance
t	variable time

t_{eff}	effective JFET channel thickness for uniform doping
t_{ox}	silicon-dioxide thickness
V_{DD}	supply voltage for MOS circuits
V_{D_i}	drain voltage at the intrinsic MOSFET
V_{DS}	drain-to-source external voltage
V'_{DS}	effective drain-to-source voltage
$V_{DS_{Sat}}$	drain-to-source saturation voltage
V_{FB}	metal-oxide-semiconductor flatband voltage
V_{GS}	gate-to-source external voltage
V'_{GS}	effective gate-to-source voltage
V_p	JFET pinchoff voltage
V_{p_o}	pinchoff voltage of the equivalent uniformly doped JFET
V_{SUB}	substrate-to-source external voltage
V_T	MOSFET threshold voltage
ΔV_T	threshold voltage shift in short channel MOSFETs
V_{T_J}	JFET threshold voltage
V_{T_O}	MOSFET threshold voltage at zero substrate bias
$\langle v \rangle$	average inversion-layer carrier velocity
v_{sat}, v_{max}	bulk scattering-limited velocity
x_j	junction depth
$x_{j_{n^-}}$	n^-/p metalurgical junction depth
$x_{j_{n^+}}$	n^+/p metalurgical junction depth
$x_{j_{p^+}}$	p^+/n^- metalurgical junction depth
W_{DRAWN}	drawn-mask channel width
W, W_{eff}	effective electrical channel width
W_J,	JFET effective electrical channel width
β	JFET transconductance factor
ϵ_{ox}	silicon-dioxide dielectric constant

ϵ_s	silicon dielectric constant
ϕ_f	bulk Fermi potential
ϕ_{bi}	p-n junction built-in potential
γ	body factor
λ	JFET channel-length modulation parameter
μ	carrier mobility
μ_{eff}	average effective inversion-layer carrier mobility
μ'_{eff}	effective inversion layer mobility under a low longitudinal field
μ_o	low-field inversion-layer carrier mobility
ρ_s	sheet resistivity of a diffused layer
τ_D	average circuit delay
Θ	transversal field mobility-degradation factor
Θ'	linear region transconductance reduction factor

Chapter 1

Introduction

For over two decades silicon integrated circuits have been a driving force leading to the widespread use of electronic systems. Silicon technology has been established as the vehicle for the integration of complex systems into a faster and more reliable and economical unit – the monolithic integrated circuit. As a result of this technological revolution, the number of active components on a silicon chip has increased exponentially over the last 25 years, as illustrated in Fig.1.1 [1.1], and is expected to reach over 10^7 components on a single die before 1990. Extrapolations beyond 1985 in Fig. 1.1 are based upon a number of possible future scenarios. In terms of system integration, silicon MOS technology has been and will continue to be, the leader that makes possible new and higher degrees of system integration.

This evolution to higher levels of integration is the result of the superposition of three contributions – reduced feature size, greater die area, and increased packing efficiency. The historical evolution of minimum feature size λ and die area of state-of-the-art commercial chips is shown in Fig. 1.2 [1.2]. In the past, minimum feature size has decreased by 50 percent every six years [1.3] as a result of the technological advances in optical lithography, etching, process control, and defect-density reduction.

1.1 MOSFET Scaling

In addition to the advantages of reduced costs and increased system functionality on the same silicon area derived from higher packing density, MOS device

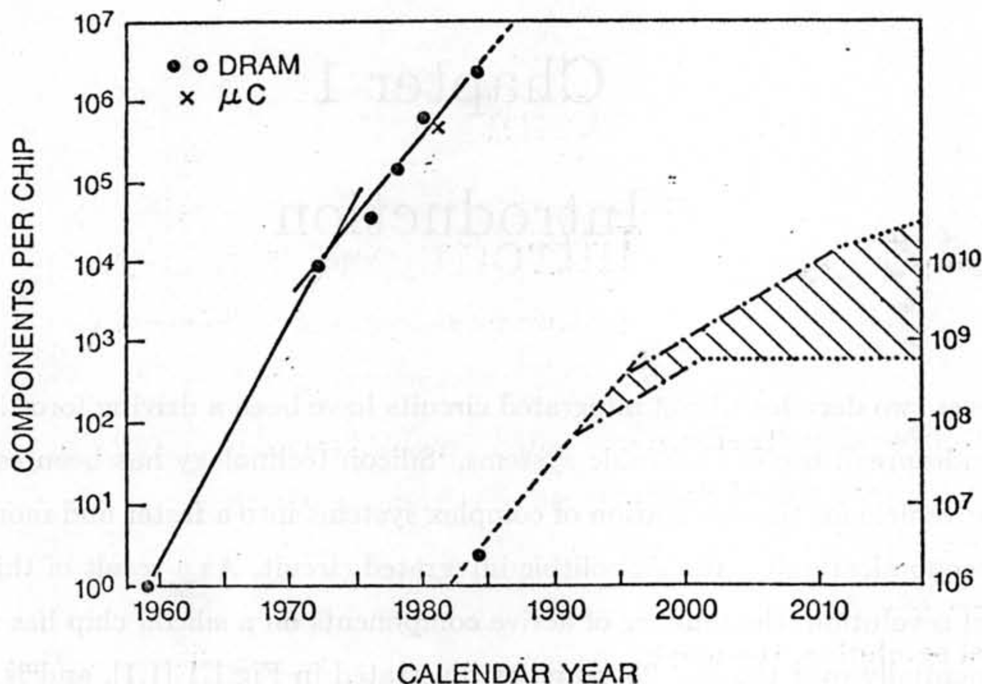

Figure 1.1: NUMBER OF ACTIVE COMPONENTES ON A SILICON CHIP vs. YEAR [1.1].

performance is greatly enhanced by down-scaling device dimensions. A set of rules for guiding MOSFET scaling [1.4] while holding the electric fields inside the device constant is summarized in Table 1.1. The circuit-performance improvements predicted by this scaling principle are based on the assumption that both supply voltage and device dimensions are scaled by the same factor $1/\kappa$ ($\kappa \geq 1$); reduction of delay and of energy dissipation associated with logic switching events are direct consequences of this scaling approach.

Experience in MOSFET scaling over the last ten years indicates that device design has proceeded under constraints other than those assumed by the constant electric-field scaling principles. Maintaining $5\,V$ compatibility in VLSI circuits has been of major importance to circuit designers, and practical considerations then led to scaling device dimensions while power supply either remained unchanged or was scaled at a slower pace. Reducing the lateral dimensions while maintaining

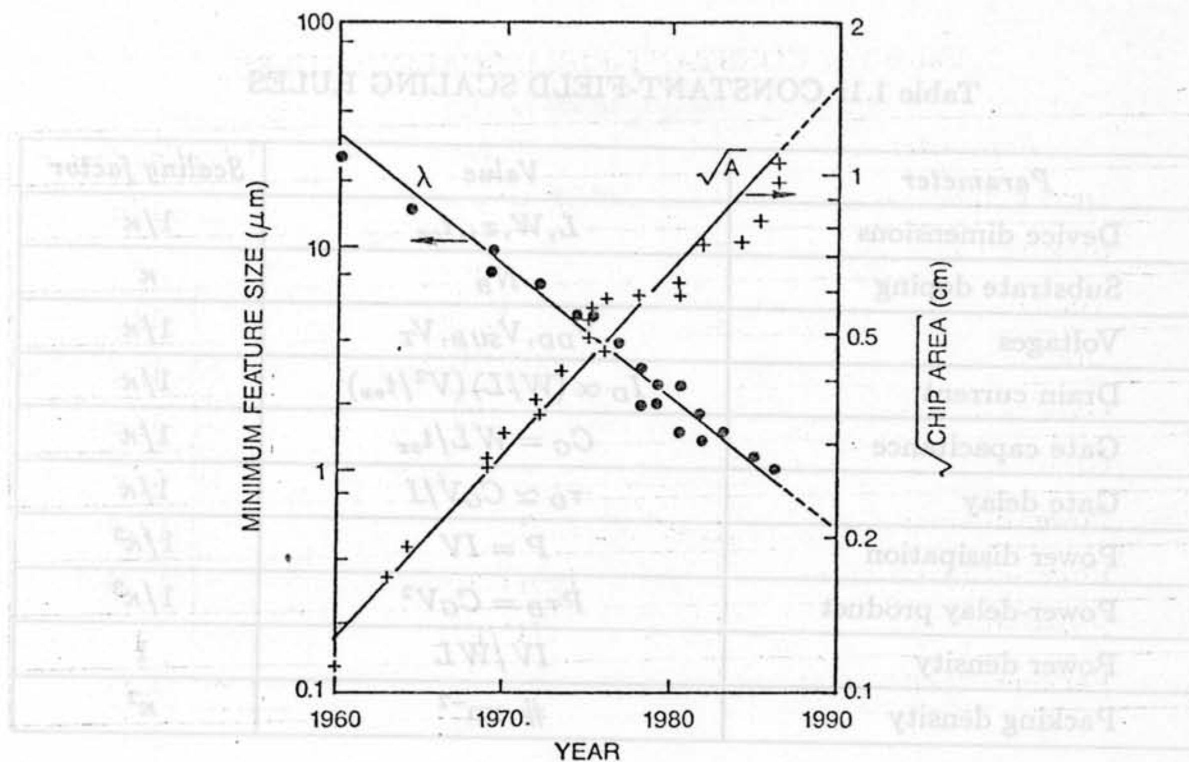

Figure 1.2: EVOLUTION OF THE MINIMUM FEATURE SIZE AND DIE SIZE OF SILICON ICs. [1.2].

a constant supply voltage, acceptable punchthrough voltage, and long-term device reliability has required innovations in device design.

Other empirical [1.5,1.6] scaling rules appear to be closer approximations to what has actually been followed in practice. Adoption of such ***constant voltage*** or ***quasi constant voltage*** scaling schemes generates larger electric fields as dimensions are further reduced.

A number of deleterious effects in device characteristics are the result of high fields. These effects include geometry-dependent device parameters (such as V_T, $V_{DS_{sat}}$ and output conductance), V_T and g_m degradations caused by hot-carrier injection into the gate oxide, and velocity saturation of mobile channel charge.

High field effects in most small-geometry MOSFETs are two- or even three-dimensional in nature and are known as DIBL [1.7,1.8] or short-channel and narrow-width effects. These effects play a critical role in determining the deviations from

Table 1.1: CONSTANT-FIELD SCALING RULES

Parameter	*Value*	*Scaling factor*
Device dimensions	L, W, x_j, t_{ox}	$1/\kappa$
Substrate doping	N_B	κ
Voltages	V_{DD}, V_{SUB}, V_T	$1/\kappa$
Drain current	$I_D \propto (W/L)(V^2/t_{ox})$	$1/\kappa$
Gate capacitance	$C_G = WL/t_{ox}$	$1/\kappa$
Gate delay	$\tau_D \simeq C_G V/I$	$1/\kappa$
Power dissipation	$P = IV$	$1/\kappa^2$
Power-delay product	$P\tau_D = C_G V^2$	$1/\kappa^3$
Power density	IV/WL	1
Packing density	$\# \text{ cm}^{-2}$	κ^2

ideal behavior of such parameters as threshold voltage, transconductance, output conductance, and source/drain breakdown voltage.

1.2 Alternative Structures for VLSI

Figure 1.3 is a cross section of a conventionally fabricated self-aligned surface channel nMOS transistor. The rectangle ABCD limits the region where the intrinsic MOS field effect occurs. The shaded areas comprise the four external electrodes of the MOSFET, three of which (bulk, source, and drain) are "contacts" that bias the intrinsic MOSFET. This investigation focuses on the design of the internal device structure, which is distinguished from the external metal–semiconductor contacts C1-C2, C3-C4, and C5-C6. In conventional MOSFETs under normal operating conditions, the potential drop across the shaded source/drain regions that comprise the internal contacts is held at a minimum level; the potential applied to the intrinsic MOSFET is nearly equal to the externally applied bias ($V'_{DS} \approx V_{DS}$ in Fig. 1.4).

When conventional MOSFETs are scaled under a constant supply voltage, the intrinsic MOSFET region in Fig. 1.3 has higher electrical fields and is affected by

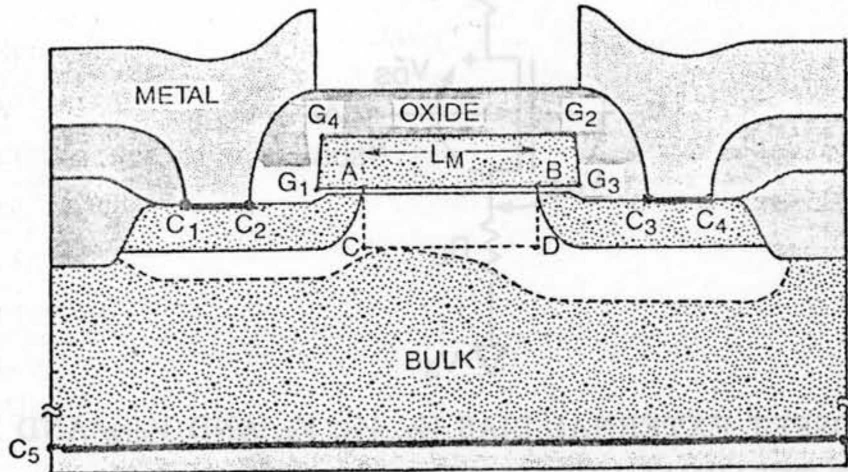

Figure 1.3: CROSS SECTION OF A CONVENTIONAL MOSFET. Shaded areas are neutral contacts to the intrinsic field effect region marked ABCD.

the resulting deleterious effects of such field strengths. Simple electrostatic theory indicates that the local gradients of the fields inside the lightly injected and noninverted space-charge regions of MOSFETs (and the amount of lateral spreading of the drain fields) are uniquely defined by the local doping concentration inside the same space-charge regions and by the geometrical structure of the device (by such parameters as gate-oxide thickness t_{ox}, source/drain junction depth x_j, and effective electrical channel length L_{eff}). To minimize the undesirable effects resulting from the lateral spreading of high fields into the intrinsic MOSFET, the devices should be tailored for each application by varying the lateral doping concentration along the direction of the channel of MOSFETs. Such tailoring yields one additional degree of freedom for the designer when coping with the negative effects of constant-voltage scaling. This is the goal and underlying principle adopted by proposers of alternative, nonconventional MOSFET device structures – whether it is the DMOS (double-diffused MOSFET or DSA-MOS) [1.9,1.10,1.11], the LDDMOS-

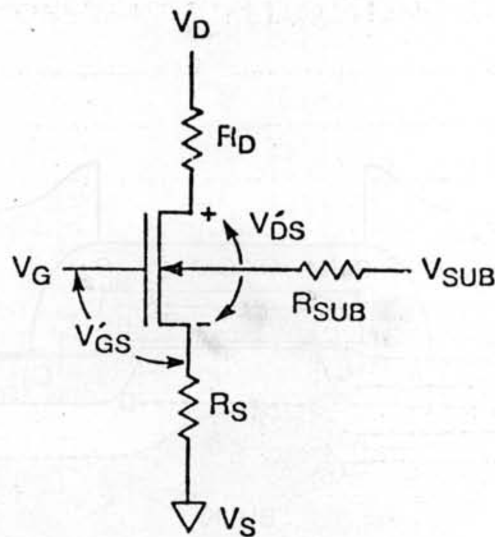

Figure 1.4: MOSFET EXTERNAL BIAS V_G, V_D, V_S, AND V_{SUB} AND EFFECTIVE MOSFET TERMINAL VOLTAGES V'_{DS} AND V'_{GS}.

(lightly doped drain/source MOSFET) [1.12]–[1.16], or the graded source/drain MOSFET (GDMOS) [1.17]–[1.20].

The unique features of the LDDMOS and GDMOS devices (here referred to as LDDFETs) are the design of the neutral regions that comprise the source and drain contacts to the intrinsic MOSFET in Fig. 1.3. In first-order MOSFET models, device behavior is independent of the design of these neutral contacts; they are simply low-resistance paths for the current from the external contacts to the intrinsic MOSFET and, as such, can be modeled as series resistors as in Fig. 1.4. The second-order effects that become important in small-geometry VLSI transistors, however depend on the shape, profile, and placement of these neutral contacts. The above effects are largely the result of two-dimensional high fields in the device and are sensitive to the design of the source and drain regions.

1.3 Scope and Objectives

This work investigates the device physics of lightly doped drain MOSFETs as they relate to their utilization in VLSI circuits. The two variant forms, the LD-

DMOS and GDMOS, are suitable VLSI devices capable of withstanding constant-voltage scaling down to the 1 μm effective channel-length integration level. A new VLSI structure, the JFET-MOSFET LDD (JMOSFET), is also simulated, modeled, and fabricated.

Chapter 2 reviews the problems encountered in MOSFET device scaling under a constant supply voltage, including the high field effects that limit the supply voltage to which the devices can be subjected and still maintain reliable operation. The hot-carrier-related reliability problems of micron-sized n-channel MOSFETs are of paramount importance and are also reviewed. Alternative MOSFET VLSI structures proposed to lessen the impact of high field effects (particularly the LDDFETs) are discussed, and the implications of their utilization for device performance are addressed. This chapter focuses on the different schemes of *"drain engineering"* and their impact on reducing the high field effects in down-scaled n-channel MOSFETs. Drain engineering is necessary for n-channel silicon devices because of their susceptibility to hot-carrier-related device degradation. Electrons in silicon have a higher ionization rate and a lower energy barrier to injection into the oxide at the Si/SiO_2 interface, and their drift velocity saturates at smaller fields than holes. High field effects, therefore, are far more deleterious to n-channel device performance and reliability. Special attention is directed toward the hot-carrier-resistant properties of nonconventional structures because these properties make them viable alternatives as VLSI devices capable of sustaining constant-voltage scaling. The LDDFETs have ensured reliable 5 V operation of n-channel MOSFETs in the range of 1 to 1.5 μm effective channel lengths in mass-produced digital ICs by introducing lighter doping in the source/drain areas adjacent to the channel. The problems related to the lightly doped drain structures (both LDDMOS and graded S/D that were proposed to minimize the high field effects) are reviewed in Chapter 2.

Chapter 3 introduces a new FET structure (the n-channel JMOSFET) designed to eliminate the still unsolved reliability shortcomings of n-channel LDDFETs, and two-dimensional simulations demonstrate its operation. The principle of operation and characteristics are analyzed, and a first-order circuit model for the JMOSFET is

developed and simulated. Appropriate design trade-offs and constraints are studied to determine the ability of JMOSFETs to down scale while holding device voltages constant.

Chapter 4 presents the experimental data obtained for the JMOSFETs implemented in an NMOS process. The reliability and performance trade-offs at both high and low pinch-off voltages are discussed and compared to conventional MOSFET drain structures. Chapter 5 describes the optimization of the JMOSFET, aiming at overcoming some of the limitations of the earlier designs and achieving a better reliability-performance trade-off. Chapter 6 summarizes the results of this study and recommends areas for future research.

Chapter 2

Lightly Doped Drain Structures for VLSI MOSFETs

The lightly doped drain (LDD) structures are reviewed in this chapter. The most relevant consequences of *constant voltage scaling* of conventional MOSFETs with respect to high field effects are first discussed, and the velocity saturation of mobile channel carriers and hot-carrier-related reliability phenomena are then analyzed because of their their severe impact on the performance of scaled devices. The reliability problems encountered when VLSI MOSFETs are scaled below 2 μm are described in terms of electric fields inside the device. The substrate and gate current characteristics of conventional MOSFETs are also explained in terms of the impact ionization and injection mechanisms. Drain-engineering schemes developed to address the reliability of MOSFET scaling are presented and compared; these schemes center on variations around the graded source/drain GD-MOSFET and the LDD-MOSFET.

2.1 Overview

Monolithic circuits in silicon have been fabricated through planar technology for over 25 years. The minimum feature size on commercially available ICs has decreased by a factor of 20 during the same time span – from 25 μm linewidths in 1960 down to 1.25 μm in 1985. The linewidth definition and control set by lithographic tools across the silicon wafer, coupled with advanced processing technologies for pattern transfer to underlying layers, have enabled increasingly smaller devices to

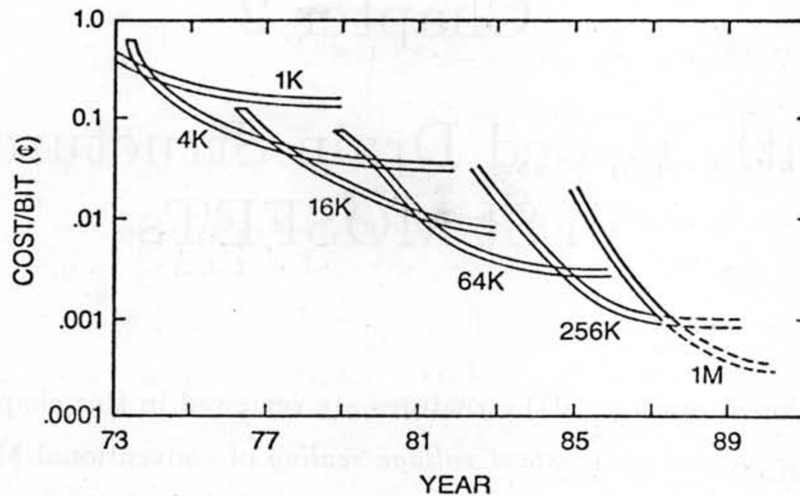

Figure 2.1: EVOLUTION OF COST PER BIT OF STORAGE IN DYNAMIC RAMs [2.1].

be more densely packed onto the substrate. As a result, the cost/performance ratio of every electronic function integrated in a silicon chip decreases as the integration level is raised. As an example, Fig. 2.1 shows the reduction of the cost per bit stored in a state-of-the-art one-transistor cell dynamic RAM [2.1] as IC technology progressed through successive levels of integration. This progression was made possible not only by advances in silicon processing technology, but also by design innovations at the device, circuit, and system levels. As the pace of down-scaling continues, major challenges must be met at all levels, in addition to the technological challenges encountered in fabricating millions of devices on a single chip.

The constant electric field (CE) MOSFET scaling rule [2.2] requires the reduction of device dimensions and the supply and threshold voltages by the same factor $1/\kappa$. More realistic scaling rules that reflect more closely the actual path followed by silicon technology are presented in Table 2.1 and are known as *constant voltage* (CV) and *quasi constant voltage* (QCV) scaling rules [2.3]. A generalized scaling rule that independently scales the physical dimensions and applied voltages of the

Table 2.1: SCALING RULES

Parameter	*Value*	*CE*	*QCV*	*CV*	*General*
Device dimensions	L, W, x_j, t_{ox}	$1/\kappa$	$1/\kappa$	$1/\kappa$	$1/\kappa$
Substrate Doping	N_B	κ	κ	κ	κ
Voltages	V_D, V_{SUB}, V_T	$1/\kappa$	$1/\kappa^{1/2}$	1	$1/\kappa_s$
Drain Current	$I_D \propto (W/L)(V^2/t_{ox})$	$1/\kappa$	1	κ	κ/κ_s^2
Gate capacitance	$C_G = WL/t_{ox}$	$1/\kappa$	$1/\kappa$	$1/\kappa$	$1/\kappa$
Gate delay	$\tau_D \simeq C_G V/I$	$1/\kappa$	$1/\kappa^{3/2}$	$1/\kappa^2$	κ_s/κ^2
Power dissipation	$P = IV$	$1/\kappa^2$	$1/\kappa^{1/2}$	κ	κ/κ_s^3
Power-delay product	$P\tau_D = C_G V^2$	$1/\kappa^3$	$1/\kappa^2$	$1/\kappa$	$1/(\kappa\kappa_s^2)$
Power density	IV/WL	1	$\kappa^{3/2}$	κ^3	κ^3/κ_s^3
Packing density	$\#\ \mathrm{cm}^{-2}$	κ^2	κ^2	κ^2	κ^2

FET was also proposed [2.4] and utilized as a guide for the design of a 0.25 μm technology; device dimensions are scaled by a factor $1/\kappa$ and the voltages are scaled by a factor $1/\kappa_s$. This generalized formulation reduces to CE scaling when $\kappa = \kappa_s$, and to CV scaling when $\kappa_s = 1$. An empirical scaling rule has also been developed [2.5] to predict the minimum allowable effective channel length L_{min} of conventionally designed MOSFETs as a function of technology-driven parameters,

$$L_{min} = \mathrm{A}[x_j t_{ox}(d_{js} + d_{jd})^2]^{1/3} \tag{2.1}$$

where A is a proportionality constant equal to 0.41 Å$^{-1/3}$, t_{ox} is the oxide thickness in angstroms, and L_{min}, x_j, and the source d_{js} and drain d_{jd} depletion-layer widths are determined in micrometers. Equation (2.1) was derived empirically through simulations and experiments, and it predicts L_{min} down to where the device maintains acceptable long-channel behavior.

Constant-voltage scaling is more desirable from a system design point of view for the following reasons:

- **System and TTL compatibility:** monolithic circuits are designed to operate as building blocks in a variety of sys-

tems and applications. Supply-voltage compatibility is demanded by system designers of a multitude of systems worldwide. Once adopted, supply-voltage standards do not change over the average lifetime of successive scaling generations; the 5 V standard, for example, has been widely accepted in digital ICs since the advent of transistor-transistor-logic (TTL) circuits at small scale integration with few tens of active elements per chip. Early MOS ICs operated at 12 V to 18 V and have steadily made the transition to 5 V. Maintaining compatibility with the current 5 V standard has then been a critical factor, therefore, to circuit designers. A new voltage standard (probably in the range of 3 to 3.3 V) [2.6,2.7], is expected to be adopted, in order to ensure that future submicron-scaled versions of MOS devices operate reliably and the power dissipation in very dense integrated circuits such as megabit DRAMs is reduced [2.8].

- **Noise margin:** noise is an integral part of the environment in which integrated circuits operate. Logic circuits are designed with voltage and current noise margins that enable them to deliver proper logic functionality in a noisy environment. In addition, the voltage margins must take into account the statistical fluctuation of process parameters and the operating temperature variations. Reduction of the supply voltage in digital circuits implies a reduction of the noise margins for their operation and, for this reason, constant-voltage scaling is more applicable. Power-supply voltages cannot be scaled at the same rate as device geometries [2.7].

- **Circuit speed:** digital-logic integrated circuits switch faster with higher supply voltage. Based on the predictions summarized in Table 2.1, the average gate delay is reduced by a factor $1/\kappa^2$ under a CV scaling scenario and by $1/\kappa$ under CE scaling. The average delay τ_D in a switching transient in which the inverter output-voltage swing is ΔV_o is a decreasing function of V_{DD} if the average charging/discharging current from the transistors has a superlinear dependence on V_{DD} and on device threshold voltages, as in scaled CMOS technology. A zeroth-order approximation for τ_D in the switching transient illustrated in Fig. 2.2 for NMOS and CMOS technology inverters is

$$\tau_D \simeq \frac{C_O \Delta V_O}{I_O} \tag{2.2}$$

In ratioed enhancement/depletion NMOS technology, the av-

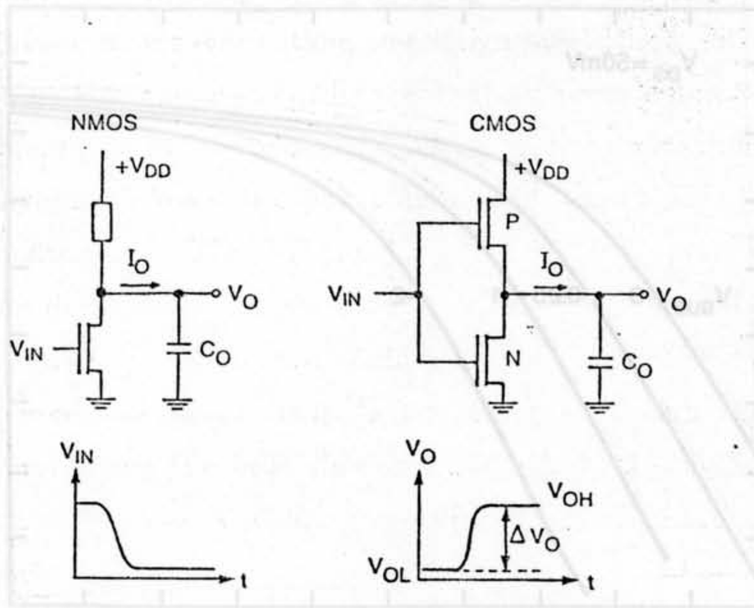

Figure 2.2: NMOS AND CMOS INVERTER CIRCUITS IN A SWITCHING TRANSIENT.

erage charging current depends to first order on the load depletion-mode transistor threshold V_{T_L}, not on V_{DD}, and the average delay normally increases with supply voltage. Altough the average delay decreases with higher supply voltage in an enhancement-load/enhancement-driver technology, the power–delay product per logic gate rises with the larger voltage.

- **On-chip power-supply drop:** this is a circuit-level solution to the contradictory requirements of lower supply voltage and integrated-system compatibility. It facilitates the input of a larger supply to the chip and a drop in dc voltage in an *on-chip* series voltage-regulating circuit from which the internal circuitry draws power. On-chip voltage converters generating a voltage lower than 5 V have been proposed [2.9,2.10] for VLSI systems whose devices must operate at lower supply voltages, such as DRAMs containing 4Mb or more [2.11]. This solution dissipates a fraction of the chip power, which could otherwise be used in logic functions, in a series voltage-step-down circuit.

At the device design level, there are also advantages in adopting a constant-

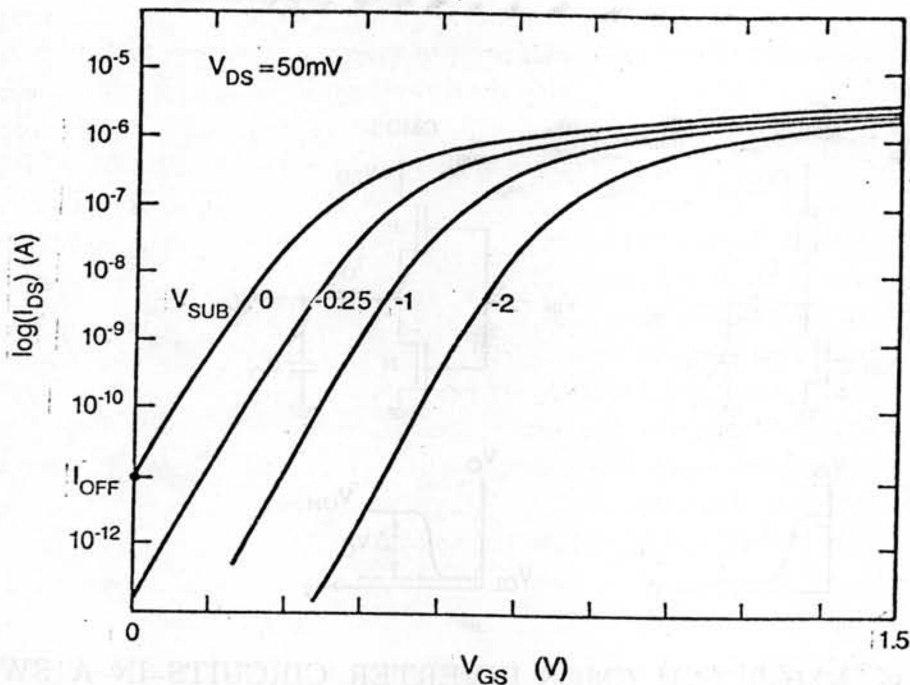

Figure 2.3: SUBTHRESHOLD I–V CHARACTERISTICS OF A MOSFET. $V_{T_O} = 0.33$ V.

voltage scaling approach. Enhancement-mode MOSFET thresholds are set to $V_T \simeq V_{DD}/10$ to $V_{DD}/4$ [2.4] so that current drive can be maximized by a maximum $(V_{GS} - V_T)$. Threshold-voltage scaling would be required if supply voltage is to be scaled, as is proposed by the CE scaling rules; however, scaling V_T to less than 0.5 V leads to further difficulties resulting from threshold-voltage control limitations. In addition, the OFF-state or subthreshold currents in MOSFETs do not scale down. The measured subthreshold current slope in the I_{DS} vs V_{GS} curves in Fig. 2.3 is typically 70 to 90 mV/decade at room temperature for a correctly scaled n-channel device. As a result, further reduction of V_T in an enhancement-mode FET lowers the ratio of the ON-state to OFF-state current; this is undesirable especially in dynamic circuits or applications requiring low dc power dissipation.

At the system and circuit levels, however, the higher speed resulting from the CV scaling of ICs is achieved but at the expense of an increase in power dissipation per unit chip area. According to Table 2.1, a CE scaling approach would lead to a

constant chip power density and CV scaling leads to an increase by a factor of κ^3. To minimize static power dissipation, the design of VLSI circuits has changed during the past several years from an NMOS technology, prevalent in VLSI chips introduced in the 1970s, to a CMOS technology. Although less dense than NMOS, the CMOS circuits have much less static power dissipation than their functionally equivalent NMOS counterparts. The designers of CMOS digital systems need only consider the average dissipation under switching conditions, and this ac power becomes a function of the system clock or switching rate. From a system design point of view, therefore, excessive power dissipation is a major concern that can be prevented by either improving the heat sinking design [2.12,2.13] or limiting the degree of integration on the chip. A seldom considered alternative to reduce power dissipation is the lowering of the system power supply.

From the device design standpoint, a CV scaling approach has the major disadvantage of leading to increased electric field strengths inside the capacitors and transistors and across the p-n junctions. Maintaining the long-channel behavior in scaled transistors is possible by an appropriate choice of technology parameters, such as N_{SUB} and t_{ox}. To minimize the short channel effects for a given effective channel length and supply voltage, substrate doping must be increased and gate oxide thickness should be reduced. The designed values of L_{min}, t_{ox}, and N_{SUB} in the next scaling generation imply that the field strengths inside the devices of the next generation will be more intense than those in the current technology.

A number of harmful effects in the device characteristics are the result of high fields in the integrated circuits. The most significant effects are reviewed in the following section, with emphasis on their role in understanding the problems related to the design of micron and submicron MOSFETs. The high field related phenomena must be prevented so that CV scaling can proceed or circumvented by adopting lower operating voltages in VLSI systems.

2.2 High Field Effects in Conventional MOSFETs

The high field effects most relevant to the design of VLSI MOSFETs are generally classified as follows

- **Geometry- and bias-dependent electrical parameters:** as devices are scaled, the most important electrical parameters become geometry and bias dependent. These phenomena include the short channel effect (SCE) on V_T and drain voltage dependence of V_T (also known as drain-induced barrier lowering, DIBL), the narrow width effect (NWE) on V_T, channel length- and width-dependent sensitivity of V_T on substrate bias, bulk punchthrough when the source and drain regions are close enough to merge their depletion regions and generate weakly gated injection from source to drain.

- **Hot-carrier-related instability of the electrical parameters:** high-energy carriers can be emitted from the semiconductor into the gate dielectric. A small fraction of these injected carriers can be trapped in the oxide or can indirectly create excess surface states, which will shift the device threshold and transconductance during the normal operating life of the transistor. Energetic carriers can be generated by carrier acceleration in very high electric fields (in excess of 100 kV/cm) and, under this condition, energy relaxation by impact ionization of the semiconductor atoms becomes an important mechanism. As a result, the generation of impact ionization current is directly correlated with the incidence of oxide degradation during device operation. Low-level impact ionization and hot carrier injection into the dielectric are processes that aid in the understanding of substrate and gate currents in MOSFETs.

- **Saturation of the drift velocity of mobile channel charge:** the scaling relationships in Table 2.1 neglect the nonlinear and saturating behavior of carrier velocity under high fields. Electrons in silicon reach their scattering-limited maximum velocity at uniform electric fields in excess of $E_{CRIT} \simeq 15$kV/cm. Submicron VLSI devices are expected to operate at drain bias above 1 V, which makes carrier velocity saturation a major limitation on device performance. This limitation is reflected in reduced current drive as the channel current saturates as a result of large longitudinal fields.

The geometrical dependence of the transistor parameters, not predicted by classical one-dimensional MOSFET theory, is the consequence of two-dimensional field effects that have been reported extensively in the literature. The short and narrow

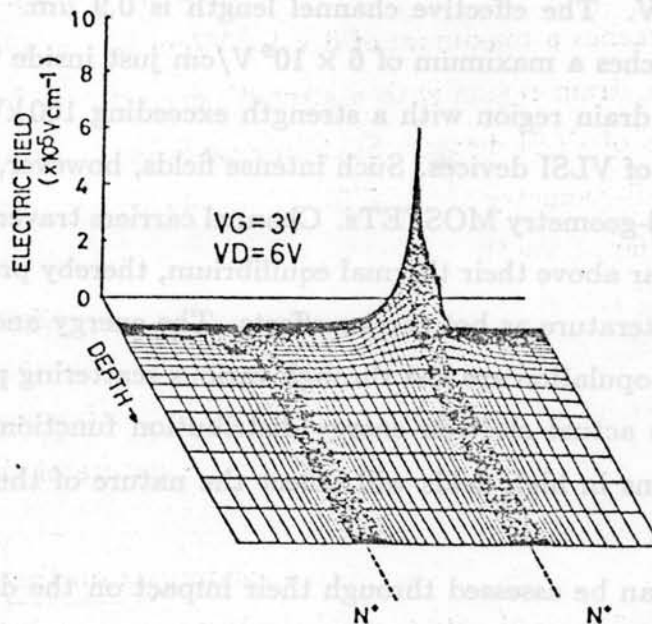

Figure 2.4: SIMULATED TWO DIMENSIONAL FIELD DISTRIBUTION IN A CONVENTIONAL MOSFET. $V_{GS} = 3\,V$, $V_{DS} = 6\,V$, $V_{SUB} = 0\,V$; $L_{eff} = 0.9\,\mu m$ [2.34].

channel effects have been studied through simple analytical models [2.14]–[2.29] to predict V_T dependence on L_{eff}, W_{eff}, x_j, t_{ox}, N_{SUB}, V_{DS}, and V_{SUB} or through empirical fitting of this dependence to experimental or two-dimensional simulated I–V data [2.30]–[2.33]. The understanding of these two-dimensional effects is complete enough so that it is possible to design MOSFETs with $L_{eff} < 0.25\mu$m and still exhibit long-channel behavior. Tailoring the channel implants and their use as punchthrough stoppers can contain the short channel effects within acceptable bounds.

The following effects impose major constraints on the constant-voltage scaling of conventional MOSFETs.

2.2.1 Hot-Carrier-Related Phenomena

Figure 2.4 [2.34] shows the two-dimensional distribution of the electric field intensity in an n-channel enhancement-mode MOSFET biased in saturation at

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V_{GS}= 3 V and V_{DS}= 6 V. The effective channel length is 0.9 μm. Under these conditions, the field reaches a maximum of 6×10^5 V/cm just inside the drain n^+ diffusion. Fields in the drain region with a strength exceeding 100 kV/cm are inherent to the operation of VLSI devices. Such intense fields, however, can degrade the performance of small-geometry MOSFETs. Channel carriers traversing the high field region are heated far above their thermal equilibrium, thereby producing phenomena known in the literature as hot carrier effects. The energy and momentum gained by the electron population are lost through various scattering processes and impact ionization. The actual electron energy distribution function (DF) under nonequilibrium conditions in high fields will reflect the nature of these scattering and ionization processes.

Hot carrier effects can be assessed through their impact on the device characteristics such as the generation of gate and substrate currents and the instabilities of such parameters as threshold voltage and transconductance. The terminal currents generated by hot carriers and the subsequent instabilities resulting from these carriers are discussed below.

2.2.1.1 Substrate Current

Of the many generation-recombination processes that can account for the energy and momentum balance of hot carriers, impact ionization is one of the most significant. The impact ionization occurring in the intense field region of a MOSFET is illustrated in Fig. 2.5. An electron-hole pair is created by the energetic electron, and low-level avalanche multiplication (with possible secondary ionization events) occurs under normal device operation. Except for a negligible hot hole current that may be injected into the oxide, the majority of the holes produced in the avalanche process are collected in the substrate and become the substrate current. Because the electron ionization rate is larger than the hole ionization rate in silicon, the magnitude of the substrate current is greater in n-channel than in p-channel MOS transistors of the same scaling generation.

In a device with $L_{eff} = 1.25\,\mu$m, typical of 2 μm NMOS technology with 400 Å

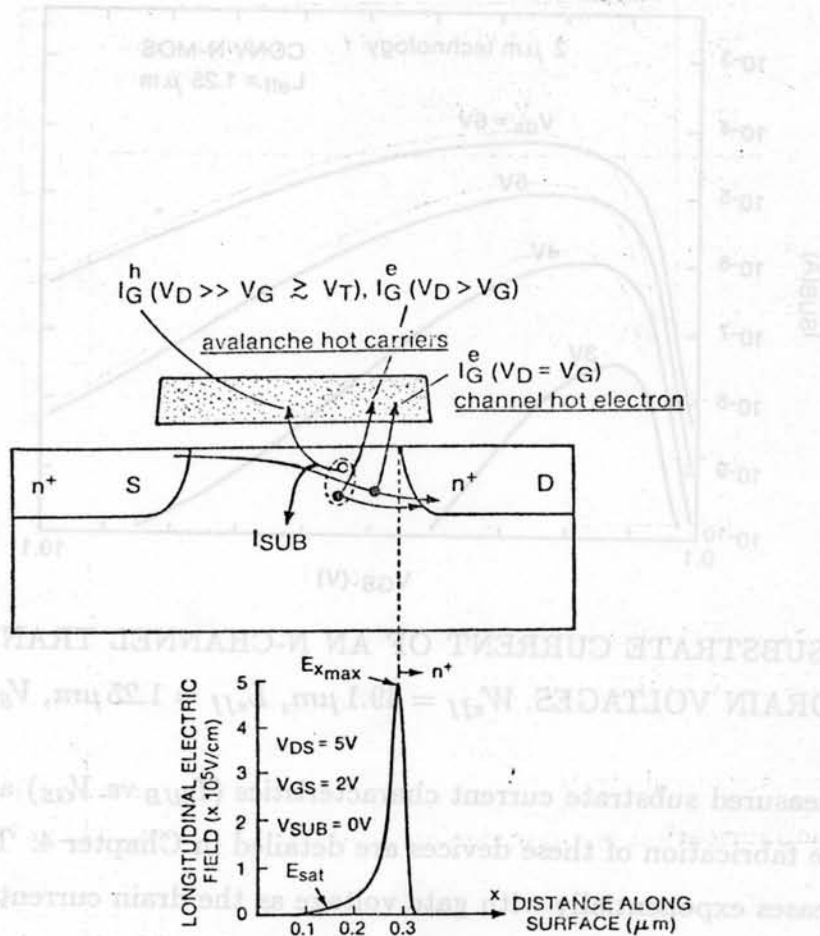


Figure 2.5: GENERATION OF SUBSTRATE AND GATE CURRENTS BY HOT CARRIERS IN THE DRAIN END OF THE CHANNEL. Position of the peak longitudinal E-field is indicated.

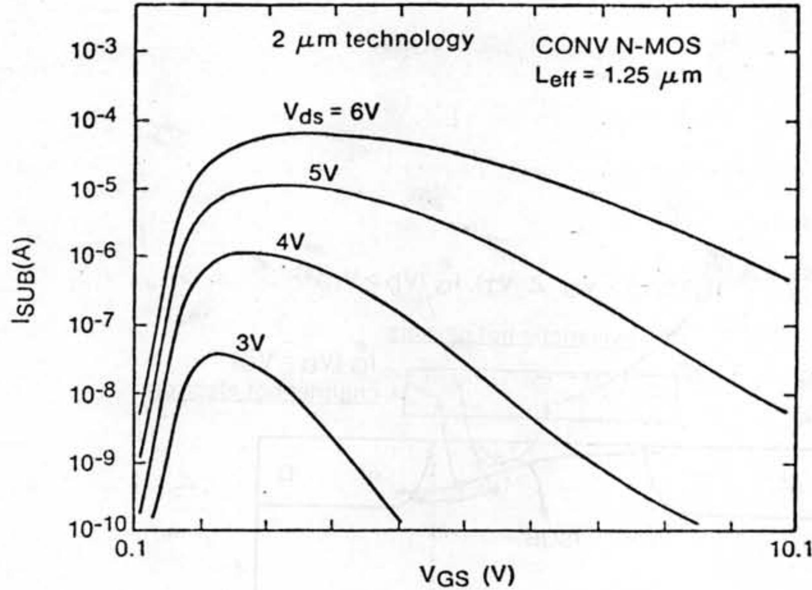


Figure 2.6: SUBSTRATE CURRENT OF AN N-CHANNEL TRANSISTOR AT SEVERAL DRAIN VOLTAGES. $W_{eff} = 49.1\,\mu m$, $L_{eff} = 1.25\,\mu m$, $V_{SUB} = 0\,V$.

oxide, the measured substrate current characteristics (I_{SUB} vs. V_{GS}) are plotted in Fig. 2.6. The fabrication of these devices are detailed in Chapter 4. The substrate current increases exponentially with gate voltage as the drain current is turned on in the subthreshold regime. For gate biases above threshold, the substrate current reaches a peak at any given V_{DS} and then decreases with V_{GS} as the device enters its linear mode of operation; this current depends exponentially on the dc V_{DS} bias.

The ratio of peak substrate current to drain current is plotted in Fig. 2.7 as a function of ${V_{DS}}^{-1}$ for devices with varying channel lengths built on the same chip with the $2\,\mu$m NMOS technology described in Chapter 4. This ratio indicates the intensity of the impact ionization process. Only a slight dependence on channel length can be seen in the maximum of the substrate current; in contrast, the ratio has an exponential dependence on drain voltage expressed as

$$\frac{I_{SUB_{MAX}}}{I_{DS}} \propto \exp\left(-\frac{V_o}{V_{DS}}\right) \tag{2.3}$$

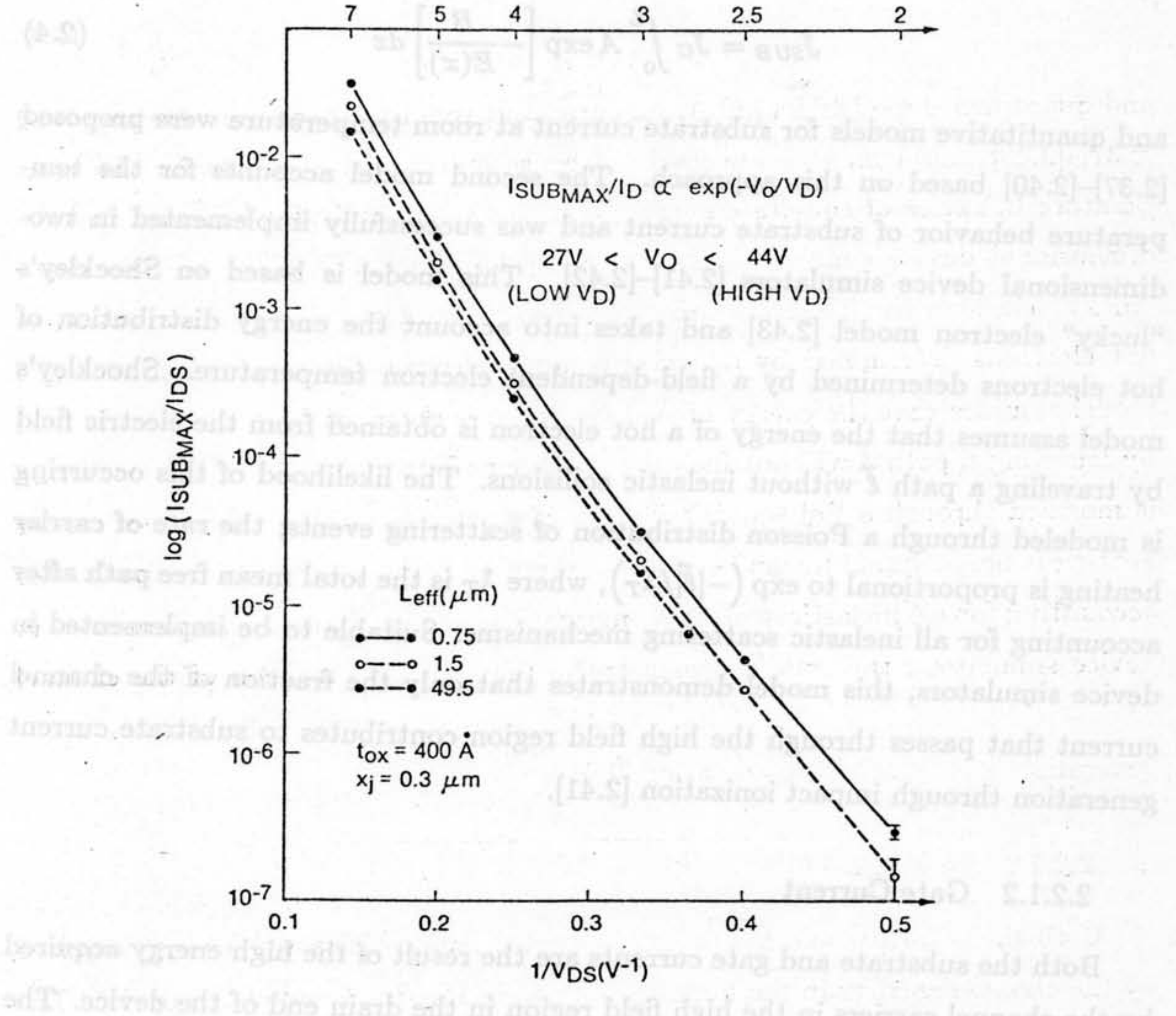


Figure 2.7: DRAIN-VOLTAGE DEPENDENCE OF THE MAXIMUM SUBSTRATE CURRENT NORMALIZED TO THE DRAIN CURRENT IN CONVENTIONAL N-CHANNEL MOS TRANSISTORS WITH THREE DIFFERENT CHANNEL LENGTHS.

where V_o varies from 27 V (for low V_{DS}) to 44 V (for high V_{DS}).

The substrate current generated by impact ionization has been modeled in two ways. The first relates substrate current density to channel current density by the empirical Chynoweth ionization integral along the current path [2.35,2.36].

$$J_{SUB} = J_C \int_0^L A \exp\left[-\frac{B}{E(x)}\right] dx \tag{2.4}$$

and quantitative models for substrate current at room temperature were proposed [2.37]–[2.40] based on this approach. The second model accounts for the temperature behavior of substrate current and was successfully implemented in two-dimensional device simulators [2.41]–[2.42]. This model is based on Shockley's "lucky" electron model [2.43] and takes into account the energy distribution of hot electrons determined by a field-dependent electron temperature. Shockley's model assumes that the energy of a hot electron is obtained from the electric field by traveling a path $\vec{\ell}$ without inelastic collisions. The likelihood of this occurring is modeled through a Poisson distribution of scattering events; the rate of carrier heating is proportional to $\exp\left(-|\vec{\ell}|/\lambda_T\right)$, where λ_T is the total mean free path after accounting for all inelastic scattering mechanisms. Suitable to be implemented in device simulators, this model demonstrates that only the fraction of the channel current that passes through the high field region contributes to substrate current generation through impact ionization [2.41].

2.2.1.2 Gate Current

Both the substrate and gate currents are the result of the high energy acquired by the channel carriers in the high field region in the drain end of the device. The measured gate current in two n-channel MOSFETs of different scaling generations is plotted in Fig. 2.8. Both have an 1.5 μm effective channel length. The device with a thinner gate oxide was fabricated and measured by Saks [2.44], and the 400 Å device was fabricated with 2μm technology as part of this work. Both were measured by the gate current measurement technique described in Chapter 4.

Two distinct regimes of gate current can be seen in the I_G vs V_{GS} plot. At

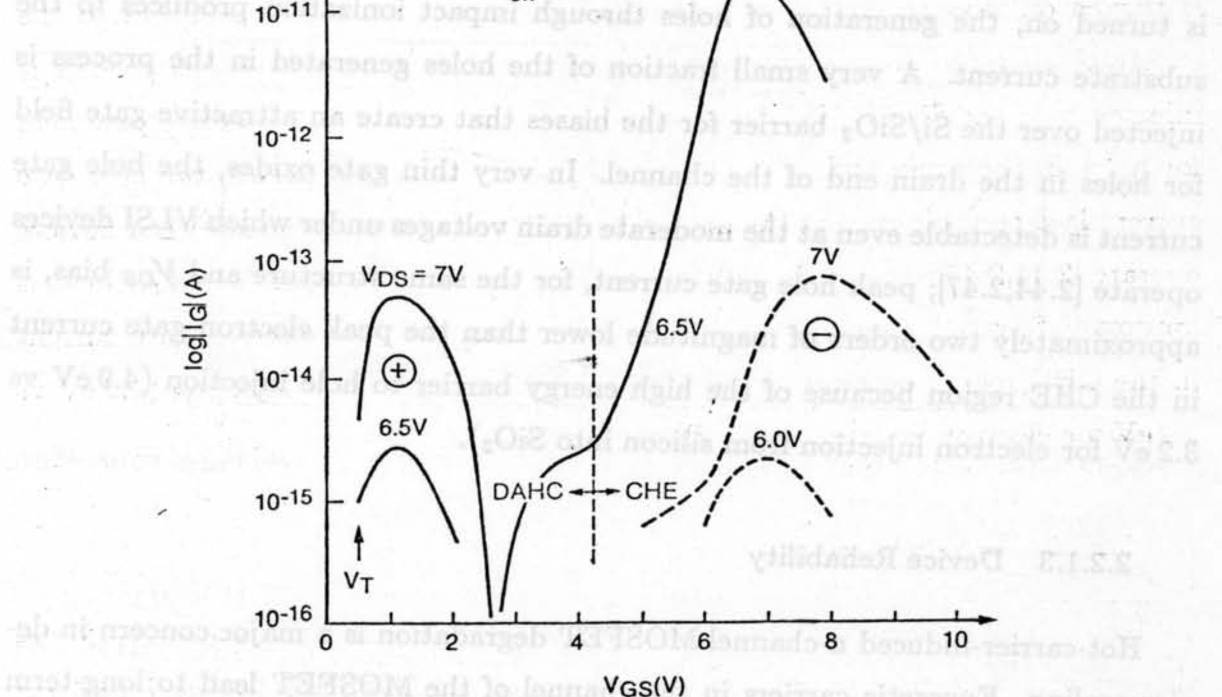


Figure 2.8: GATE CURRENT IN CONVENTIONAL N-CHANNEL MOSFETS. The solid line indicates a 1.25 μm technology and the dashed line denotes a 2 μm technology. Measured data for $L_{eff} = 1.5$ μm.

low V_{GS} bias, when substrate current generation through impact ionization is at a maximum, the gate current is composed of drain avalanche-induced hot carriers (DAHC in Fig. 2.8) that are injected into the gate oxide. At higher V_{GS}, the channel hot electrons [2.45,2.46] are injected and produce a bell-shaped gate current (CHE in Fig. 2.8) that reaches a maximum when $V_{GS} - V_T \simeq V_{DS}$.

At low V_{GS}, the gate current is comprised of holes collected in the gate electrode and, just above threshold, the field from the gate to drain favors hole injection. At an intermediate V_{GS}, the total gate current passes through a null as the hole gate current is canceled by the electron current. As the MOSFET channel current is turned on, the generation of holes through impact ionization produces to the substrate current. A very small fraction of the holes generated in the process is injected over the Si/SiO_2 barrier for the biases that create an attractive gate field for holes in the drain end of the channel. In very thin gate oxides, the hole gate current is detectable even at the moderate drain voltages under which VLSI devices operate [2.44,2.47]; peak hole gate current, for the same structure and V_{DS} bias, is approximately two orders of magnitude lower than the peak electron gate current in the CHE region because of the high energy barrier to hole injection (4.9 eV vs 3.2 eV for electron injection from silicon into SiO_2).

2.2.1.3 Device Reliability

Hot-carrier-induced n-channel MOSFET degradation is a major concern in device scaling. Energetic carriers in the channel of the MOSFET lead to long-term drift of the device characteristics [2.48]-[2.53]. The degradation of the electrical properties of the gate oxide and of the Si/SiO_2 interface [2.54,2.55] explain the drifting of the measured characteristics. The n-channel device characteristics before and after degradation induced by dc stress are plotted in Fig. 2.9 [2.56] where degradation is described in terms of the shift in the linear region threshold voltage (Fig. 2.9b) and in terms of device transconductance reduction (Fig. 2.9a). The first can be explained by the build-up of trappped charge in the gate oxide, and the second by an increase in the Si/SiO_2 interface state density. Both fixed and interface

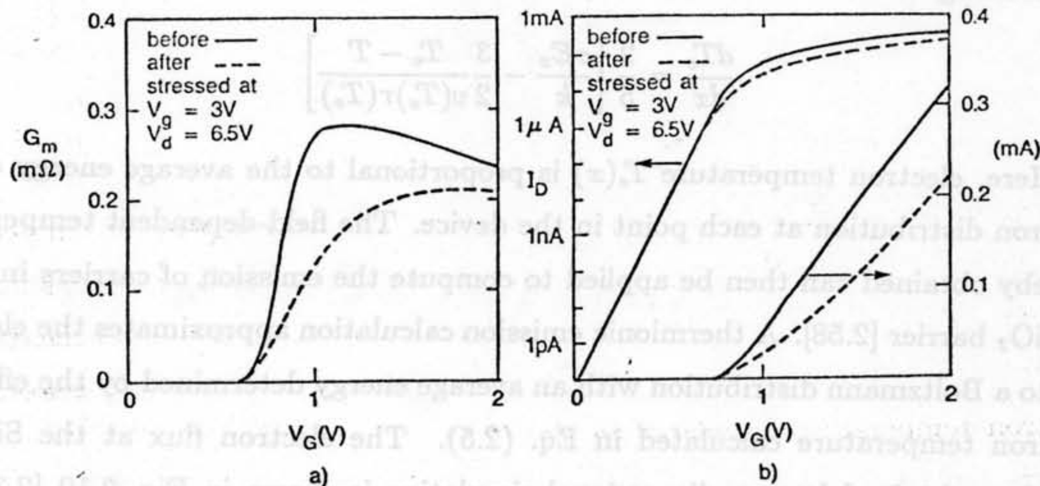


Figure 2.9: HOT-CARRRIER-INDUCED DEGRADATION OF CONVENTIONAL MOSFETS MEASURED AT V_{DS}= 50 mV BEFORE AND AFTER STRESS [2.56]. $L = 2\,\mu$m, $t_{ox} = 155$ Å. (a) Linear region transconductance degradation. (b) Linear region current degradation.

state trapped charge can further decrease the transconductance by reducing the low longitudinal field mobility of channel carriers.

The degradation of the Si/SiO_2interface is nonuniform along the channel length because carrier heating is more intense in the high field region on the drain side. Electron heating in the intense field region were calculated by applying classical kinetic theory to the energy-transport problem [2.57,2.58]. The electron temperature-dependent energy relaxation time $\tau(T_e)$ and drift velocity $v(T_e)$ were derived through Monte Carlo simulation combined with experimental high-field velocity-overshoot data and were used in the numerical computation of the electron temperature T_e, which is higher than the lattice temperature T,

$$\frac{dT_e}{dx} = \frac{2}{5}\left[\frac{eE_x}{k} - \frac{3}{2}\frac{T_e - T}{v(T_e)\tau(T_e)}\right] \tag{2.5}$$

Here, electron temperature $T_e(x)$ is proportional to the average energy of the electron distribution at each point in the device. The field-dependent temperature thereby obtained can then be applied to compute the emission of carriers into the Si/SiO_2 barrier [2.58]. A thermionic emission calculation approximates the electron DF to a Boltzmann distribution with an average energy determined by the effective electron temperature calculated in Eq. (2.5). The electron flux at the Si/SiO_2 interface obtained by two-dimensional simulation is shown in Fig. 2.10 [2.34] for the device with the bias and field distribution in Fig. 2.4. The injection of hot carriers is highly peaked at the n^+/p drain metalurgical junction and is maximum at few hundred Å inside the n^+ diffusion. The physical mechanisms involved in the process of degradation caused by hot electrons are the direct emission of channel hot carriers into the oxide, emission of carriers (both electrons and holes) generated by low-level impact ionization, emission of secondary electrons, and photon emission by brehmsstrahlung or interband transition.

Experiments on device aging accelerate the degradation process through the application of stress bias. Both dc and ac [2.59,2.60] stress experiments revealed a positive correlation between device lifetime and substrate current. Device lifetime is normally defined as the length of time required for the threshold voltage, or

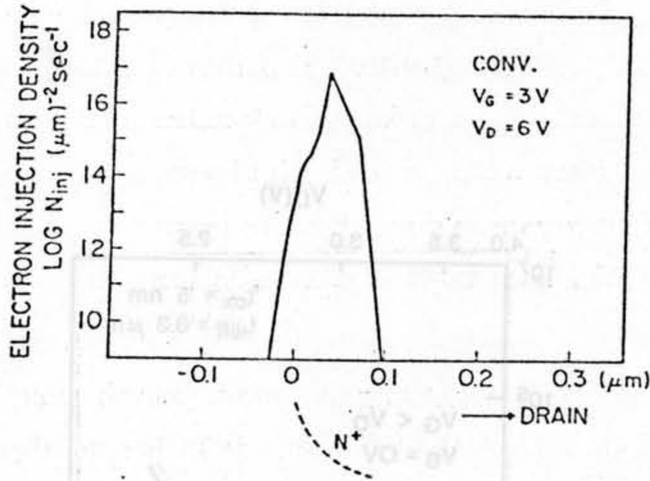


Figure 2.10: ELECTRON INJECTION DENSITY ALONG THE Si/SiO_2 INTERFACE. Two-dimensional simulation results of electron injection [2.34].

saturated current, or low field transconductance to shift by an arbitrary value (ΔV_T) or percentage, typically $\Delta V_T = 10\,\text{mV}$ and 10 percent degradation of either the current or transconductance. These values are useful in comparing similarly stressed and measured devices.

Figure 2.11 plots the lifetime of a submicron conventional MOSFET stressed under the gate bias that maximizes substrate current at the stress drain voltage [2.61]. Here, ΔV_T is defined as $\Delta V_G\,|^{V_D=0.1V}_{I_D=1\text{mA}}$, and lifetime is expressed as

$$\tau = \tau_O \exp\left(\frac{c}{V_D}\right) \tag{2.6}$$

over a small V_D range. As a result, the operation of deep submicron conventional MOSFETs under drain voltages as low as 2 V could still be constrained by reliability problems.

With the maximum substrate current dependence in Eq. (2.3), it is possible to determine empirically that device lifetime is correlated to the impact ionization substrate current such that

$$\tau \propto (I_{SUB_{MAX}})^{-n} \tag{2.7}$$

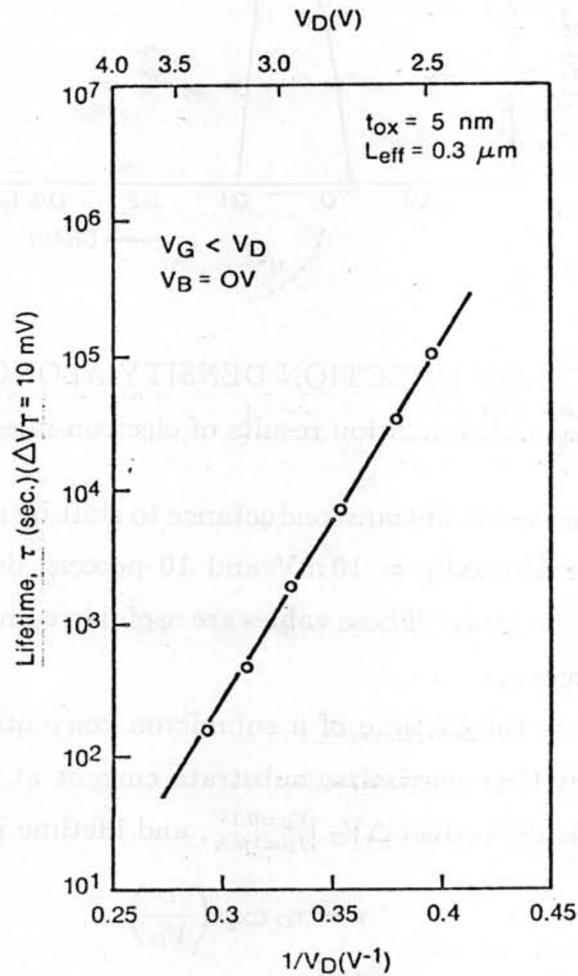


Figure 2.11: DEVICE LIFETIME UNDER DC STRESS CONDITIONS THAT MAXIMIZE SUBSTRATE CURRENT. V_D is the drain voltage used for stressing [2.61].

where n varies between 3 and 4. Experimental evidence such as in Fig. 2.11 indicates that degradation and gate current in very short n-channel MOSFETs occur at drain biases below $(\Phi_{B_e} - \Delta\Phi_B)$ [2.61]-[2.63], where Φ_{B_e} and $\Delta\Phi_B$ are the barrier potential and Schottky barrier lowering, respectively, for electron injection from silicon into SiO_2. This evidence verifies that the lucky electron model alone cannot explain the gate and substrate currents in the devices, and a quasi-thermal-equilibrium approach that takes into account the field-dependent energy distribution of the carriers as they drift in the transistor channel is a better model for the hot-carrier-related currents [2.41,2.42].

Figure 2.12 plots device lifetime as a function of the peak longitudinal electric field in the drain end of the n-channel MOSFET under stress [2.61]. The electric field was calculated by the two-dimensional simulator CADDET [2.64]. Because the MOSFET surface electrostatic potential has an exponential spatial dependence along the channel $[\Psi_S \propto \exp(x/l_c)]$ [2.65], the x-component of the electric field is linearly proportional to the electrostatic potential. In the subthreshold region, the parameter l_c is approximately defined by $3t_{ox} + W_C$, where W_C is the minimum depletion-region width along the channel [2.66]. Analytical aproximations to the electrostatic boundary-value problem inside the MOSFET indicate that $\Psi_S \propto \Phi_{DB} \simeq (V_{DS} - V_{SB})$ such that $\tau \propto \exp(V_o/V_{DS}) \propto \exp\left(a/E_{x_{peak}}\right)$.

Pseudo two-dimensional models for the electric field at the drain end of pinched-off conventional MOSFETs have also been developed [2.67,2.68] and verified through two-dimensional MINIMOS simulations [2.69]. Based on this analysis, the peak electric field can be written as

$$E_{x_{peak}} = \sqrt{\left(\frac{V_{DS} - V_{DS_{SAT}}}{l_p}\right)^2 + E_{SAT}{}^2} \tag{2.8}$$

where $V_{DS_{SAT}}$ is the drain-to-source voltage at which carrier velocity saturates, and l_p is an empirical constant. For V_{DS} larger than $V_{DS_{SAT}}$ by approximately 2 V, the maximum longitudinal electric field is on the order of 100 kV/cm and the second term in Eq. (2.8) can be neglected such that

$$E_{x_{peak}} = \frac{V_{DS} - V_{DS_{SAT}}}{l_p} \tag{2.9}$$

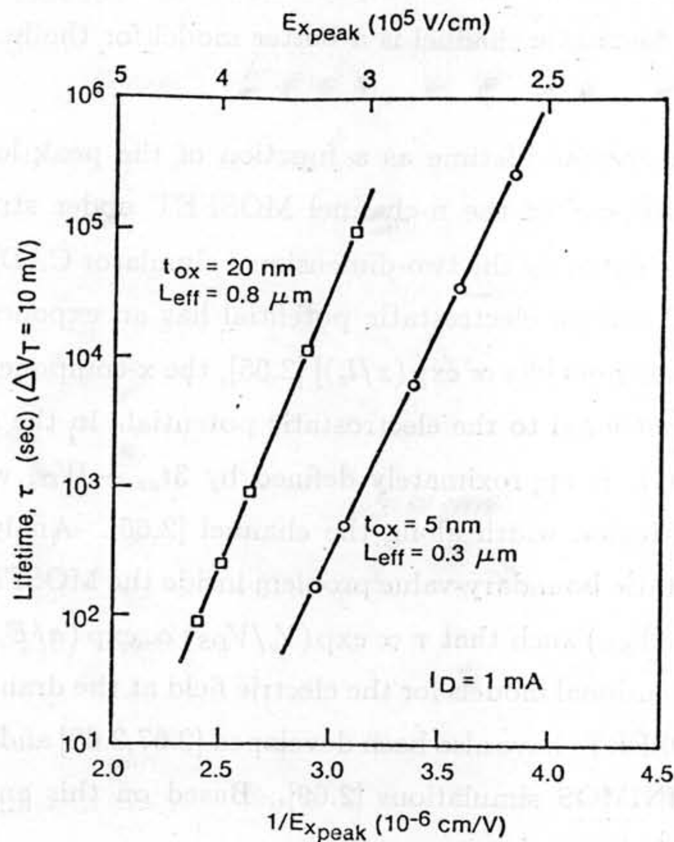


Figure 2.12: DEVICE LIFETIME UNDER DC STRESS CONDITIONS THAT MAXIMIZE SUBSTRATE CURRENT. $E_{x_{peak}}$ is the peak longitudinal electric field under stress [2.61].

The MINIMOS two-dimensional simulations for n-channel polysilicon-gate MOSFETs [2.69] demonstrated that l_p varies in the range of 800 to 2500 Å in typical VLSI devices and that it can be fitted to $l_p = 0.22 t_{ox}^{1/3} x_J^{1/2}$; it can also be interpreted as the distance from the point where $E \simeq E_{CRIT}$ to where $E = E_{x_{peak}}$. As a result, the high field drain region endures even higher field intensities as oxide thickness and junction depth are scaled at constant voltage. The impact of the high fields on the reliability of the next scaling generation of VLSI MOSFETs is evident in Fig. 2.12, where device lifetime is plotted as a function of the peak longitudinal electric field under stress.

2.2.2 Velocity Saturation

The current-drive capability of VLSI devices should increase linearly with the scaling factor according to first-order CV scaling principles; however, the high fields in scaled MOS devices result in sublinear gains in the current drive. At least along the distance l_p near the drain end, the carriers drift at their scattering-limited velocity v_{SAT}. The measured v_{SAT} values for electrons in the inversion layers are slightly less than 10^7 cm/sec and are dependent on both longitudinal and transversal fields. The mobility reduction model is described in Appendix A , and modeling-parameter extraction is explained.

The current measurement in Fig. 2.13 illustrates the impact of carrier-velocity saturation in terms of reducing the drive capability of scaled devices. The measured drain current characteristics of MOSFETs with varying channel lengths are normalized to the number of effective squares in the devices. The MOSFETs have 400 Å oxide and a full 5 V drive on the gate. The reduction of the drive capability per square is considerable in short channel devices. The drain voltage at which the drain current saturates is indicated; it can be seen that the current in micron-sized VLSI MOSFETs under 5 V operating conditions saturates at $V_{DS} \leq 3$ V. The critical field for the onset of velocity saturation in n-channel devices was determined from I-V data and is approximately 1.7×10^4 Vcm^{-1}. As a result, the carriers in the inversion layer in saturated micron and submicron MOSFETs are transported

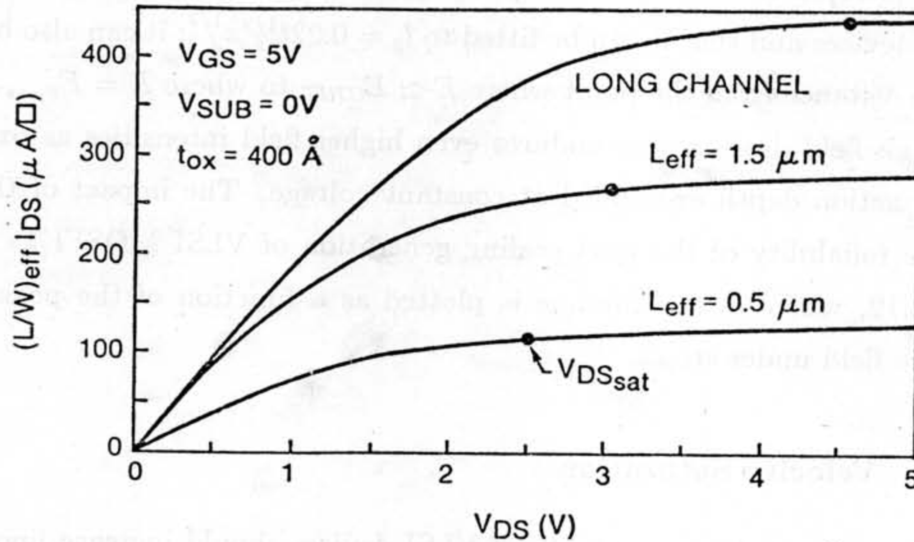


Figure 2.13: NORMALIZED DRAIN CURRENT CHARACTERISTICS OF CONVENTIONAL MOSFETS OF VARYING CHANNEL LENGTHS.

at velocities closer to v_{SAT} through a large fraction of the effective channel length.

2.3 LDDFETs Engineered for Reliability

Operation of micron and submicron MOSFETs in the presence of high field effects has required design innovation to achieve acceptable punchthrough voltage and long-term reliability as MOSFETs are scaled. The three lightly doped drain (LDD) structures in Fig. 2.14b,c,d have been studied extensively in the literature and compared as viable substitutes for the conventional n^+ arsenic drain (Fig. 2.14a) for use in VLSI circuits. Careful engineering of the drain region is more important in the n-channel rather than p-channel devices because electrons in silicon have a higher impact ionization rate, lower energy barrier to injection into the oxide at the Si/SiO_2 interface, and drift-velocity saturation at smaller fields than holes. High field effects, therefore, will greatly reduce n-channel performance and reliability. Lightly doped drain designs for submicron p-channel devices have also been proposed [2.70], mostly to prevent punchthrough.

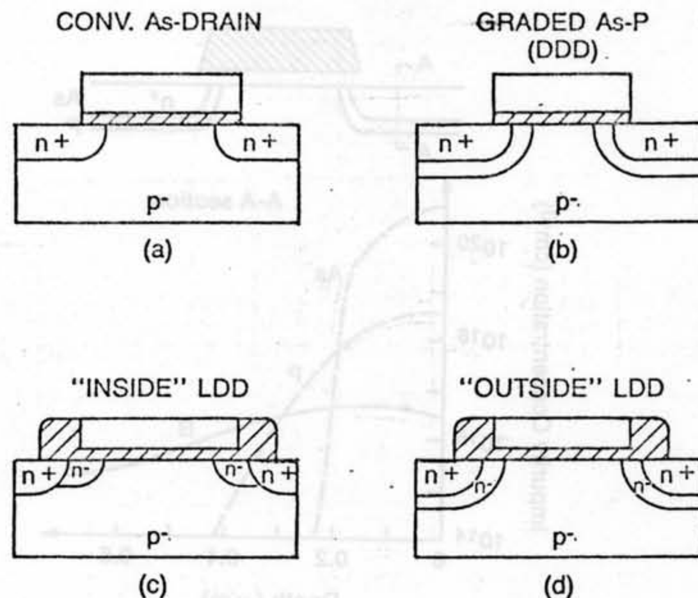


Figure 2.14: CROSS-SECTION OF N-CHANNEL STRUCTURES. (a) Conventional. (b) Double-diffused drain. (c) "Inside" LDD. (d) "outside" LDD.

In the LDD-FET and the graded S/D or double-diffused drain (DDD) n-channel structures in Fig. 2.14, the narrow n^- regions introduced between the channel and the n^+ source/drain are designed to spread the high electric field at the drain into the n^- region. The reduction and/or spreading of the peak E-field in self-aligned LDD structures normally results in an increased reliability insofar as hot-electron instabilities are concerned. This property made the LDD and DDD MOSFETs the preferred devices in VLSI MOS technologies in which the minimum effective channel length for n-channel transistors is below 1.5 μm.

2.3.1 Graded Source/Drain MOSFET

The graded source/drain device [2.71]–[2.78] in Fig. 2.14b was first proposed in 1981 as a simple self-aligned LDD structure. Its fabrication process is simpler than other LDD technologies; it consists of a double implant of a heavy dose of arsenic ions and a low dose of phosphorus ions, both self-aligned to the edge of the polysilicon gate electrode. Because the diffusivity of phosphorus is higher than

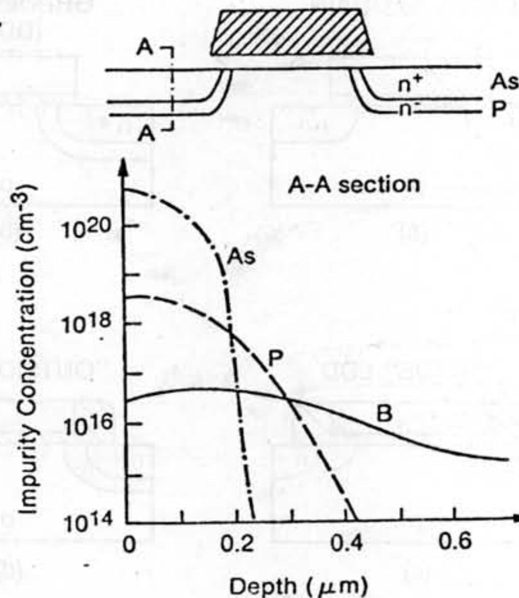


Figure 2.15: CROSS SECTION AND S/D JUNCTION PROFILE OF THE DOUBLE-DIFFUSED DRAIN MOSFET.

that of arsenic, a deeper n^-/p junction and a shallower high-low n^+/n^- junction result after implant annealing. A typical impurity profile for the S/D junction in the graded S/D device is shown in Fig. 2.15. The phosphorus profile grades the rather steep junction in conventional n^+ As S/D diffused regions. This steepness is a high-concentration diffusion effect in the anneal of heavily dosed arsenic implants.

The drain breakdown-voltage and hot-carrrier-related reliability properties of the DDD-MOSFET are improved because of the reduction and spread of the electric field intensity in the region of extremely high ($> 1\times10^5$ V cm^{-1}) fields near the drain. The simulation results in Fig. 2.16 [2.75] compare the longitudinal field intensity and the two-dimensional equipotential contours obtained by the CADDET simulator [2.64] for both the DDD and conventional MOSFETs. For the bias condition of a saturated device ($V_{GS} = 1$ V , $V_{DS} = 6$ V , $V_{SUB} = -3$ V) there is approximately a 30 percent reduction in the maximum longitudinal field intensity caused by the phosphorus grading of the S/D junction.

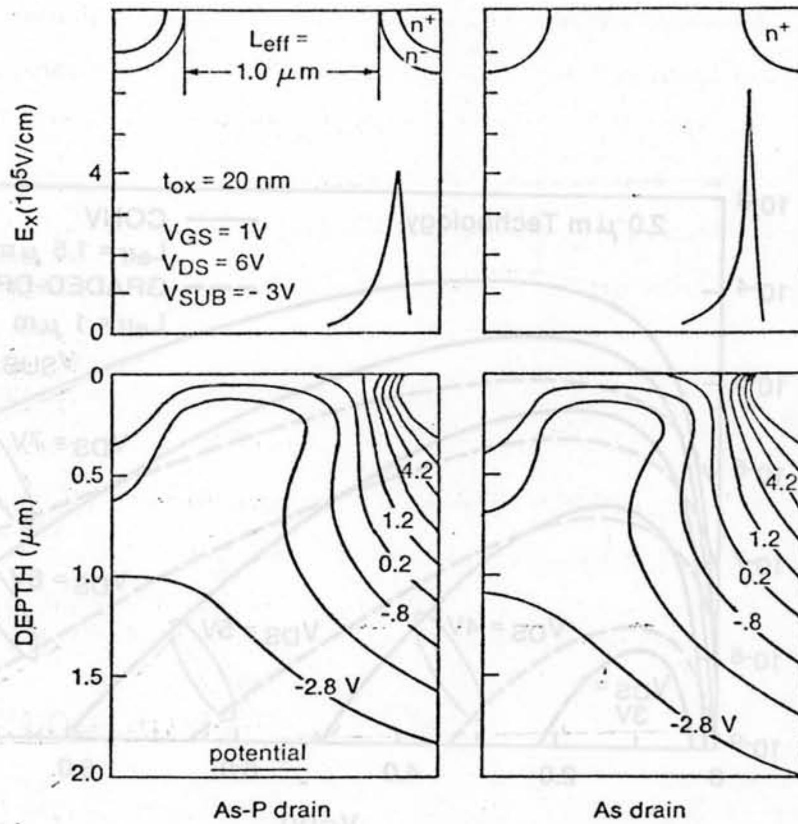


Figure 2.16: EQUIPOTENTIAL CONTOURS IN THE CONVENTIONAL AND DOUBLE DIFFUSED DRAIN MOSFETS. Longitudinal E-field profile is shown at the top [2.75].

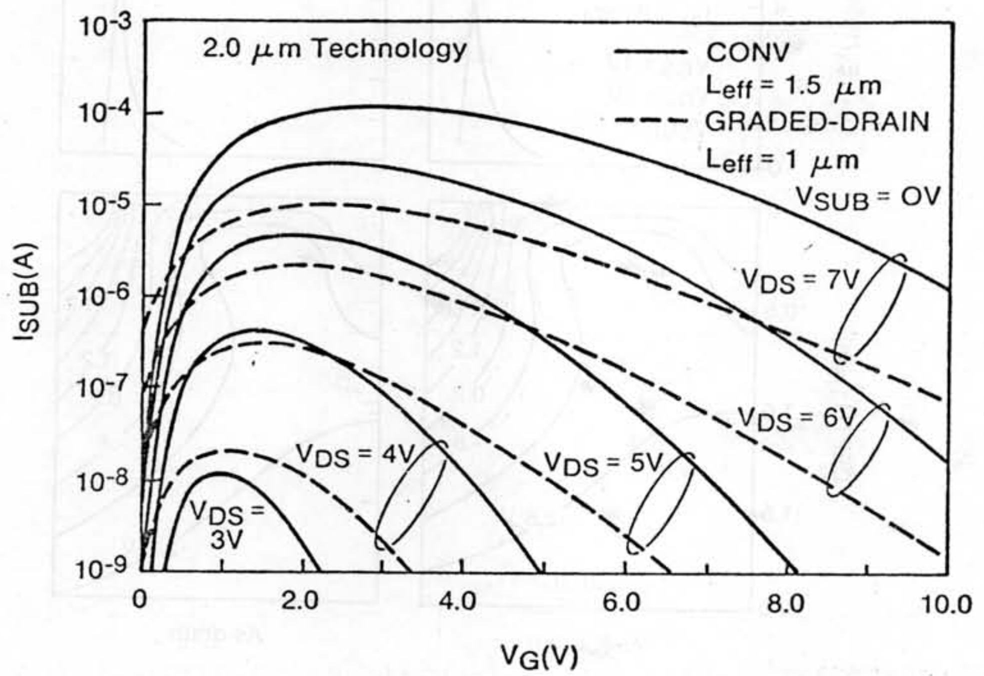


Figure 2.17: COMPARISON OF MEASURED SUBSTRATE CURRENT CHARACTERISTICS IN CONVENTIONAL AND GRADED-DRAIN MOSFETS. Both devices were fabricated with 2 μm technology.

Reduction of the intense drain fields decreases the generation of substrate current through impact ionization, as illustrated in the I_{SUB} vs V_G curves in Fig. 2.17. The substrate current was measured in conventional and graded drain devices built side by side with the 2 μm technology described in Chapter 4. The graded drain device was implanted with phosphorus (Dose=7.5×10^{13} cm^{-2}) and annealed at 1050°Cprior to n^+ arsenic implant. This anneal resulted in deep (0.7 μm) n^- junction. For the same scaling generation, it is possible to reduce the substrate current by one order of magnitude or more (depending on n^- implant dose and annealing cycle) by using a graded S/D MOSFET instead of the conventional arsenic n^+ drain.

Optimization studies of the DDD structure revealed that the optimal n^- phosphorus implant dose, annealed at 1000°C, is in the range of 5×10^{13} cm^{-2} for a 230 Å gate oxide [2.79] to 1×10^{14} cm^{-2} for a 350 Å gate oxide [2.80]. For a higher n^- concentration, the electric field near the drain edge is not sufficiently reduced and its hot-carrier-resistant properties are only slightly improved by grading the highly doped n^+/p junction; lighter doses will lower the substrate current, but the parasitic source/drain series resistance is increased.

2.3.2 LDD MOSFET

The lightly doped drain MOSFET as a VLSI device was first proposed by Saito [2.81] in 1978. The narrow n^- implanted regions were introduced between the channel and the n^+ source/drain region by aligning the n^- implant to the gate edges and the n^+ to the offset edges located a few thousand angstroms away from the gate edges. First generations of LDD devices [2.82]-[2.85] were fabricated by photoengraving a composite film of Si_3N_4 over polysilicon and then undercutting the polysilicon gates with wet etchants, using the overlaying nitride as a mask, thereby developing a self-aligned structure to offset the high-dose implant. An alternative way used to create a self-aligned offset is the oxidation of highly doped polysilicon [2.86]; this relies on the enhanced oxidation rates for highly doped polysilicon to produce a sidewall-spacer oxide. After the polysilicon oxidation step at low temperature (< 900°C), a thin oxide is grown over the lightly doped single crys-

tal source/drain region and a thicker oxide is grown on the polysilicon and its sidewalls. A high-dose source/drain implant follows the formation of the sidewall oxide. The oxide spacer process better controls the offset length than does the polysilicon-undercutting technique. As a result, a more controllable sidewall-oxide spacer approach was developed [2.87]-[2.89] and applied for the fabrication of LDD MOSFETs.

In the LDD structures in Fig. 2.14c,d, the sidewall-oxide spacer is formed by the conformal deposition of oxide in a low-pressure chemical vapor deposition system, followed by an anisotropic oxide etch in an RIE or plasma-etching system. In the "inside" LDD (Fig. 2.14c) the n^- implant precedes sidewal-oxide formation and, in the "outside" LDD (Fig. 2.14d), both n^+ and n^- are self-aligned to the sidewall-oxide edge.

The maximum drain voltage for device operation free of hot-carrier-related reliability problems, the drain breakdown voltage and the short channel effects are the major limitations imposed on the scaling of VLSI MOSFETs. Relaxing these limitations is the principal motivation for using LDDFETs in VLSI circuits. Based on studies of the "inside" LDD MOSFETs [2.90]-[2.93], they have the following advantages over conventional n^+ arsenic drain devices of comparable dimensions.

- Short channel effects are reduced and, as a result, threshold voltage sensitivity to channel length variations is minimized. These reductions stem from lighter doping and a shallower n^- junction depth.
- Drain junction breakdown and drain-to-source bulk punchthrough voltages are higher. Improvements up to 10 V have been predicted for very low ($< 10^{17}$ cm^{-3}) n^- doping [2.84].
- Impact-ionization-related currents are reduced. Peak substrate and gate currents can be substantially lowered by the appropriate design of the lightly doped region.
- Endurance against hot-carrier-related instabilities is higher, as measured under the same stress conditions.

These advantages result from the reduction and spreading of the high field in the drain pinch-off region of the device. Because of their improved device reliability, the

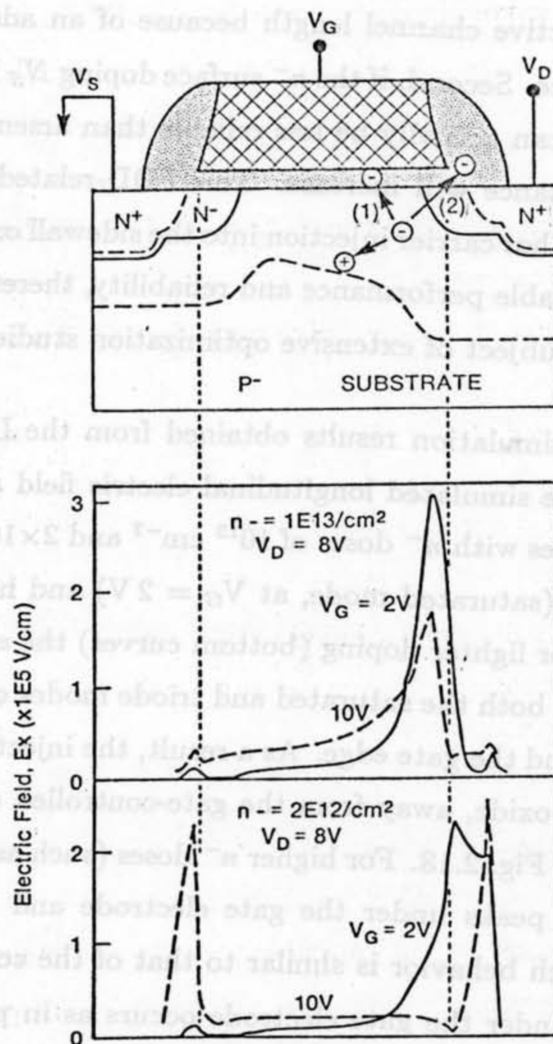


Figure 2.18: DEVICE CROSS SECTION AND SIMULATED LONGITUDINAL ELECTRIC FIELD IN THE LDDFET ALONG THE Si/SiO_2 INTERFACE. Upper E_x curve for an optimum n^- dose and bottom curve for a lighter dose [2.98].

LDD and DDD MOSFETs have become the only viable alternatives for micron-sized high-density n-channel VLSI transistors operating at 5 V. The LDDFETs, however, have two major disadvantages. First, all lightly doped drain structures are affected by reduced transconductance and current drive when compared to conventional devices with the same effective channel length because of an additional parasitic source/drain series resistance. Second, if the n^- surface doping N_S is too light ($N_S < 10^{18}\mathrm{cm}^{-3}$), the LDDFETs can actually be less reliable than arsenic-doped n^+ S/D transistors and series resistance will increase. This LDD-related degradation has been shown to be caused by hot carrier injection into the sidewall oxide region [2.94]–[2.98]. To guarantee acceptable performance and reliability, therefore, micron-sized LDDFETs have been the subject of extensive optimization studies.

Figure 2.18 plots the simulation results obtained from the LDD optimization study by Katto [2.98]. The simulated longitudinal electric field along the Si/SiO_2 interface of two LDD devices with n^- doses of 10^{13} cm^{-2} and 2×10^{12} cm^{-2} is shown for V_D = 8 V and for low (saturated mode, at V_G = 2 V) and high (triode mode, at V_G=10 V) gate bias. For lighter doping (bottom curves) the electric field peaks under the sidewall oxide in both the saturated and triode modes of operation as the n^- region is depleted beyond the gate edge. As a result, the injection of hot carriers occurs under the sidewall oxide, away from the gate-controlled channel region, as indicated by process (2) in Fig. 2.18. For higher n^- doses (such as 10^{13} cm^{-2}, upper curves), the electric field peaks under the gate electrode and is reduced as the gate voltage is raised. Such behavior is similar to that of the conventional device, for which only injection under the gate electrode occurs as in process (1). At an optimal n^- doping level, process (1) should dominate for reasons of reliability. With a lighter n^- dose, the LDDFET degradation rates are faster than in conventional designs [2.94,2.95] when stressed at the same substrate current. The proposed model for the effect of process (2) is the trapped-charge-induced modulation of the parasitic series resistance, as illustrated in Fig. 2.19, that leads to a more rapid linear region transconductance degradation. In very lightly doped LDD devices, this degradation mode correlates with the appearance of *"tails"* or *"humps"* in

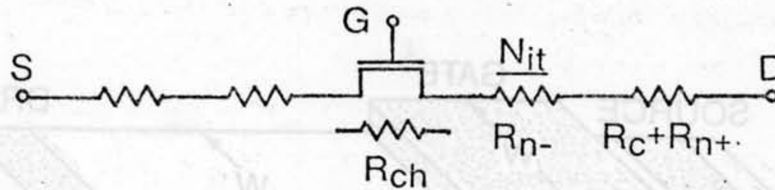


Figure 2.19: SERIES RESISTANCE MODELING OF THE TRAPPED CHARGE-INDUCED DEGRADATION OF LDDFETS.

the $\log(I_{SUB})$ vs V_{GS} characteristics [2.93,2.98,2.99] as the n^- region under the sidewall oxide is undepleted and impact ionization is strongest beyond the edge of the gate electrode. The amount of substrate current reduction in narrow-channel LDD devices has been shown to depend also on the boron implant dose in the field-isolation region [2.100]. Higher substrate dopings lead to higher electric fields near the n^+ junction and, therefore, cause higher substrate current. In narrow-channel MOSFETs, the lateral spread of the field implant encroaches on a fraction of the drawn channel width, and the resulting higher substrate concentration under the gate edges further increases electric field strengths at the drain.

Optimal LDD designs have been studied extensively and, for practical junction depths and S/D annealing temperatures, the optimum N_S is 1 to $2.5 \times 10^{18}\text{cm}^{-3}$ [2.93,2.97] or, alternatively, the optimum n^- dose is approximately 1 to 2×10^{13} cm^{-2} for "inside" LDDs in Fig. 2.14c [2.98,2.101,2.79]. Other studies have proposed that there are better I_{SUB} and device-degradation trade-off for "inside" LDDs with either a moderately doped (4 to 10×10^{13} cm^{-2}) phosphorus n^- region [2.102] or with a (shallow As)/(n^- P) profiled n^- region [2.103]. Optimum n^- implant doses were determined to be $\simeq$ 5 to 20×10^{13} cm^{-2} for both "outside" LDDs (Fig. 2.14d), which are a double-diffused type of structure self-aligned to the oxide spacer [2.104] and DDD MOSFETs (Fig. 2.14b) [2.79,2.80]. A pseudo two-dimensional analytical model [2.105,2.106] would predict breakdown-voltage improvements of less than 2 and 1 V for DDD and "inside" LDD devices, respectively, in this practical reliability-proven range of n^- doping levels. The increase in breakdown voltage is less than

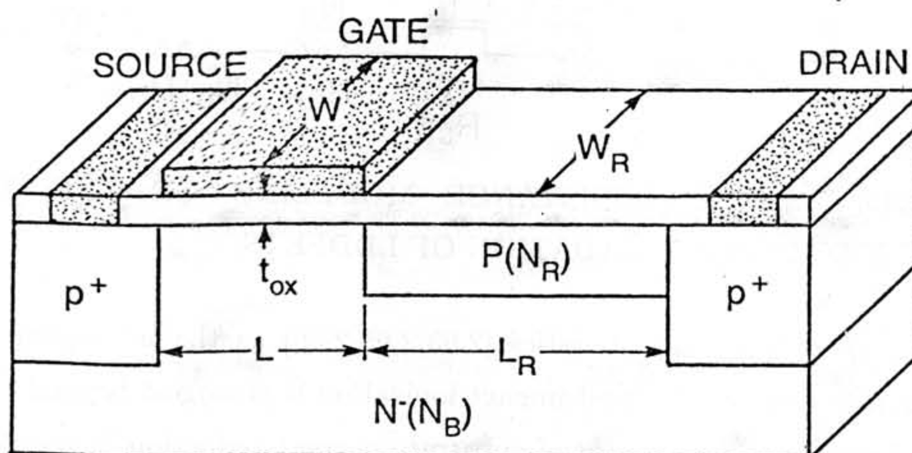


Figure 2.20: CROSS SECTION OF AN EARLY HIGH-VOLTAGE PMOS DEVICE [2.107,2.108].

the 2 to 10 V improvement over conventional designs that has been realized when LDD devices of the "inside" type were initially proposed with much lighter doping [2.84,2.85].

2.3.3 Other Nonconventional MOSFETs with Lightly Doped Drain

The forerunners of the VLSI LDDFETs were the high-voltage metal-gate PMOS devices proposed in 1971 [2.107,2.108], as illustrated in Fig. 2.20, with a lightly doped p^- extension of the drain to support the high drain voltages. This structure has a non-self-aligned lightly doped drain of several tens of microns to achieve drain breakdown voltages in excess of 200 V. The gate-controlled region of length L is in series with the drift region of length L_R, which can be slightly modulated by the substrate voltage. Figure 2.21 is the equivalent circuit model for this structure. Improved LDMOS power devices were designed later to improve the high-voltage properties of this design.

Other structures with a non-self-aligned separate gate, buried channel, or lightly doped S/D have also been proposed [2.109,2.110]. In these devices, the separation

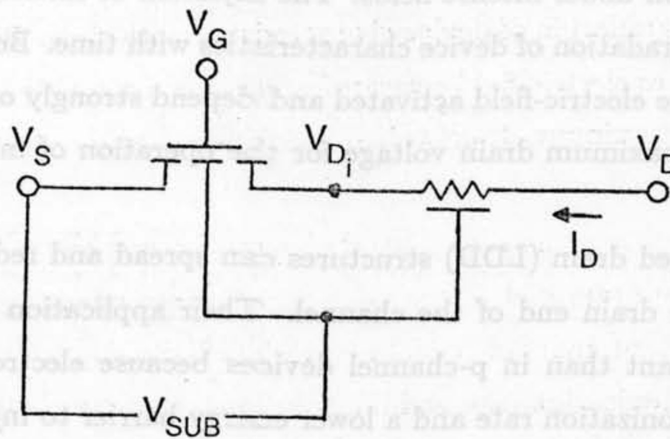


Figure 2.21: EQUIVALENT CIRCUIT MODEL OF A HIGH-VOLTAGE LDD PMOS.

between source and drain n^+ diffusions is lithographically defined rather than self-aligned to the edges of the gate electrode. Their characteristics predicted the potential for implementing MOSFETs with very short gate lengths (down to 700 Å) [2.111],[2.112] and a very low gate capacitance [2.113].

2.4 Summary

Continuing constant-voltage scaling of MOSFETs introduces serious challenges to device and technology designers. For reasons of compatibility and performance, the highest possible operating voltage is desirable for systems with micron and submicron devices. From the device design standpoint, the major consequence of CV scaling is that small devices must be designed to operate under increasingly higher electric fields. The relevant high field effects that have impacted the prformance and reliability of VLSI MOSFETs have been reviewed and were found to have a severe impact on the reliability of devices with effective channel lengths below 2 μm. The heating of carriers in the high fields in the drain pinchoff region raises the gate and substrate currents and experimental evidence indicates that the magnitude of these currents correlates directly with device instability. Substrate current is the result of

impact ionization under intense fields. The injection of carriers into the gate oxide leads to the degradation of device characteristics with time. Both impact ionization and injection are electric-field activated and depend strongly on drain voltage; they also limit the maximum drain voltage for the operation of micron and submicron MOSFETs.

Lightly doped drain (LDD) structures can spread and reduce the electric field intensity in the drain end of the channel. Their application in n-channel devices is more important than in p-channel devices because electrons in silicon have a higher impact ionization rate and a lower energy barrier to injection into the oxide at the Si/SiO_2 interface. The LDD n-channel MOSFETs are employed in virtually all circuits containing devices with effective channel length below $1.5\,\mu m$. This chapter examined several forms of lightly doping the drain of n-channel MOSFETs; the simplest forms are the LDDFETs and the graded S/D FETs. Their major limitation is that the lightly doped region must be doped above $10^{18} cm^{-3}$ to obtain the advantage of reliability in comparison to conventional MOSFETs.

Channel electrons in micron-sized devices are transported from source to drain at velocities close to their scattering-limited velocity and, as a result, the drain current saturates at 1 to 2 V below the 5 V supply voltage. An optimized LDD device should be able to drop partially the drain voltage outside the sensitive device area close to the Si/SiO_2 interface, which should impact the limitations imposed on submicron devices by high-field-related reliability problems.

Chapter 3

JMOSFET: An Alternative VLSI Structure

3.1 Overview

In this chapter, a new n-MOS LDD structure – the JMOS field effect transistor – is introduced, and its design, simulation, and principle of operation are studied. The goal of this design centers on the possibility of operating a submicron JMOSFET at a 5 V supply voltage by minimizing the voltage limitations imposed on conventional or other LDD devices. As discussed in Chapter 2, n-channel MOSFETs with L_{eff} below 2 μm are affected by high field effects that must be eliminated to secure reliable 5 V operation. The LDD structures reduce these effects, but they are more reliable than conventional MOSFETs only if the n^- regions have a peak doping density above 1×10^{18}cm^{-3}. To overcome this limitation and to facilitate constant-voltage scaling of devices down to the submicron regime, the JMOS structure employs a series drain JFET to drop part of the supply voltage. This series device must be designed to provide a trade-off between the reliability properties and performance. The design parameters and two-dimensional device-simulation results are presented to demonstrate the operation of the JMOSFET and its potential for applications requiring reliable submicron operation under a maximum supply voltage. These simulations demonstrate that the JMOS can sustain 5 V operation even for submicron effective channel lengths because of designer-controlled reduction of the maximum electrical field in the region under the gate traversed by carriers. This design should minimize the hot-carrier-related instabilities described in Chapter 2

by judiciously reducing the field strength only along the Si/SiO_2 interface, in the direction of carrier flow, where carrier *heating* potentially can damage the interface and inject and trap charge in the gate oxide layer. As in all LDD structures, device reliability can be improved but at the expense of enhanced performance; however, the advantages of maintaining 5 V operation in micron-sized devices can outweigh this performance loss.

3.2 JMOSFET and Alternative LDD Designs

As discussed in Chapter 2, it is advantageous, from the point of view of circuit and system performance and compatibility, to continue constant-voltage scaling instead of constant electric field scaling. Conventionally designed LDD MOSFETs were a technologically simple approach to scaling MOSFETs down to the L_{eff} range of 1.0 to 1.5 μm without compromising their reliability properties. Reducing the high field effects inside the active regions of the transistors was the overwhelming reason for the adoption of n-channel LDDFETs. Operation of micron and submicron MOSFETs in the presence of high field effects still requires innovative design so that acceptable punchthrough voltage and long-term reliability are maintained as MOSFETs are scaled.

The different LDDs reviewed in Chapter 2 have been studied and compared for use in VLSI circuits as substitutes for the conventional n^+ As-drain. Careful engineering of the drain region in n-channel transistors is necessary because of their strong susceptibility to hot-carrier-related device degradation [3.1]–[3.4]. High field effects are far more deleterious to their performance and reliability, and reducing the electric field strengths in excess of 100 kV/cm at the drain end of the channel is crucial.

The reduction and/or spreading of the peak E-field in self-aligned LDDFETs normally increases reliability insofar as hot-electron-induced instabilities are concerned; however, if the n^- surface doping N_S is too light ($N_S < 10^{18}\text{cm}^{-3}$) the LDDFETs can actually be less reliable than conventional arsenic-doped n^+ S/D transistors in addition to increased series resistance and higher breakdown voltage.

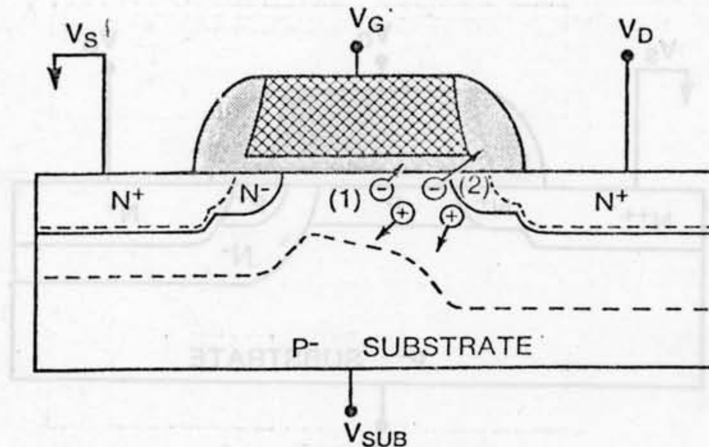


Figure 3.1: THE N-TYPE LDD MOSFET. Hot carrier injection occurs either (1) under the gate or (2) over the n^- depleted region under the sidewall oxide when the light n^- dose permits the nonoverlap of the drain depletion edge and gate electrode. The dashed lines denote depletion edges.

This LDD-related degradation, as described in Chapter 2, is caused by hot carrier injection into the sidewall oxide region [3.5]–[3.9] [process (2) in Fig. 3.1] which, in turn, leads to excessive series resistance and degradation rates faster than in conventional designs [3.5,3.6]. At an optimal n^- doping level, process (1) in Fig. 3.1 should dominate as the longitudinal electric field peaks under the gate. The optimal LDD structures are limited to dropping the entire drain voltage across the device and under the gate active region because the n^- region under the sidewall oxide must still remain undepleted for the above reliability reasons.

To obtain reliable VLSI MOSFETs, it is important to recognize the benefits of reducing high fields inside the device and keeping the high fields as far away as possible from the sensitive Si/SiO_2 interface because most instabilities are the result of damage to the gate oxide. In the JFET-MOSFET (JMOS) structure [3.10,3.11] in Fig. 3.2, the peak field can be forced to occur away from the region under the

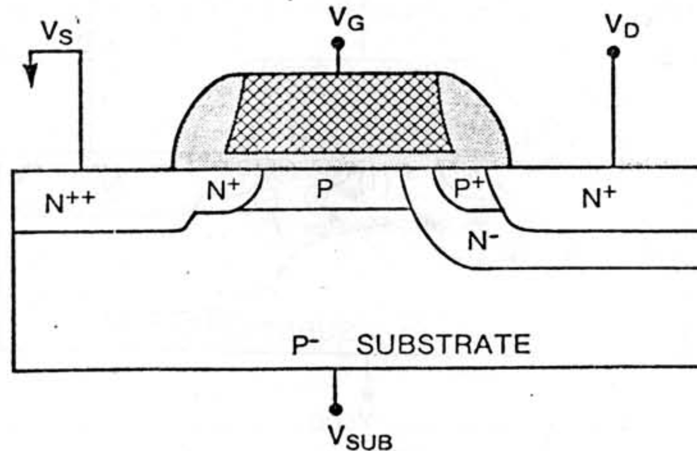


Figure 3.2: CROSS SECTION OF THE N-CHANNEL JMOSFET.

gate and the electron current flows below the surface in the critical high-field region near the drain, which should minimize hot carrier trapping in the gate or sidewall-spacer SiO_2 regions. It has been reported LDDs can perform even more reliably by diverting the channel current away from the SiO_2 interface in the high-field drain region. Techniques developed to accomplish this include either a buried-channel device with a lightly doped drain [3.12] (Fig. 3.3) or a retrogade n^- profile for the LDD region [3.13] (Fig. 3.4). Other MOSFETs have been proposed, such as the buried drain DMOSFET [3.14] whose reliability potential in VLSI has not yet been assessed. As illustrated in Fig. 3.5, the current path from source to drain is considerably two-dimensional because the n^+ drain in this DMOSFET is buried under the field oxide and the channel current must drift into the bulk. Gate action occurs at the laterally diffused p region that comprises the DMOS transistor where channel current is mostly constrained at the surface; this current is diverted by the drain fields into the bulk at the very lightly doped π region.

By construction, the JMOS circumvents the reliability problems associated with carrier injection into the sidewall oxide in more lightly doped LDD devices. The

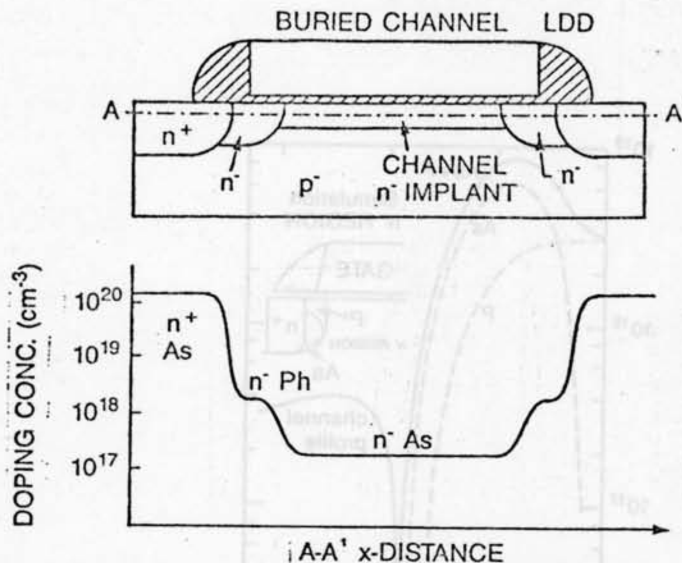


Figure 3.3: CROSS SECTION OF THE BURIED-CHANNEL DEVICE WITH A LIGHTLY DOPED DRAIN [3.12].

JMOS current is diverted into the bulk at the drain end as it drifts through the JFET n^- channel. The electron current is then buried away from the sidewall oxide to prevent carrier injection into it. The proposed n-MOS in Fig. 3.2 has a short-channel JFET at the drain end. The JFET action is the result of a p^+ region functioning as the JFET gate above the n^- drain region (Fig. 3.2). The p^+ implant connects electrically to the substrate by overlapping the channel-stop implant in the transverse direction, and the substrate bias then functions as a gate bias for the drain JFET. The circuit model of this device (Fig. 3.6) comprises a cascode-connected JFET in series with the intrinsic surface-channel MOSFET.

In addition to effectively shielding possible injection under the sidewall oxide, the role of the n-JFET is to limit the voltage applied to the drain of the intrinsic MOSFET which, in terms of a circuit model, is equivalent to limiting the voltage V_{D_i} in Fig. 3.6. The evidence presented in Chapter 2 indicates that reducing the drain voltage in conventional VLSI MOSFETs has a greatly favorable impact on their reliability.

Limitations on VLSI devices set by hot-carrier-related instabilities required the

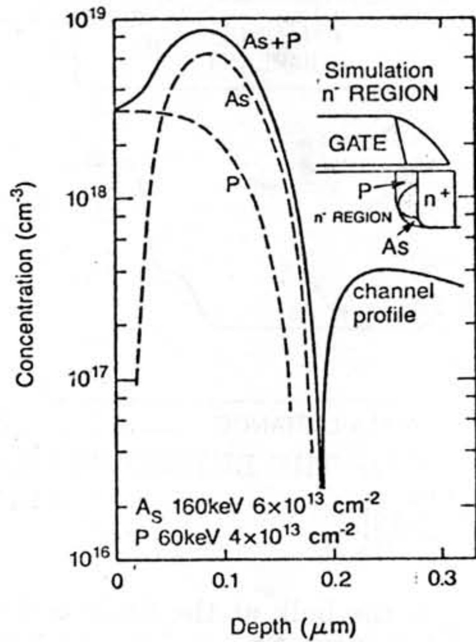


Figure 3.4: DOPING PROFILE AT THE LIGHTLY DOPED DRAIN REGION OF THE BURIED LDD [3.13].

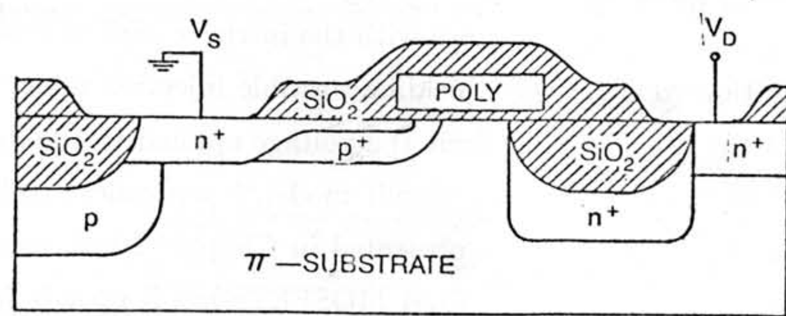


Figure 3.5: CROSS SECTION OF THE BURIED DMOS DEVICE [3.14].

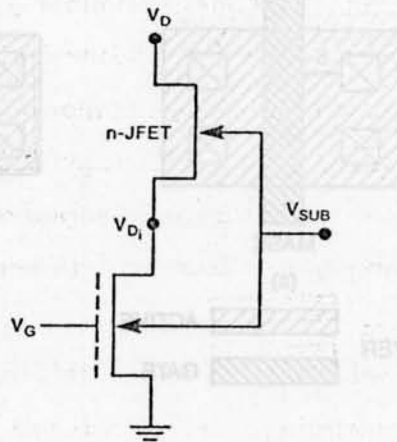


Figure 3.6: EQUIVALENT CIRCUIT MODEL OF THE JMOSFET.

adoption of LDDs as the micron-sized n-channel VLSI devices operating at 5 V. The same limitations are further requiring a lower supply-voltage standard for digital VLSI circuits which would reduce the speed performance because the gate drive would be lower. In the JMOS in Fig. 3.6, the drain voltage V_{D_i} can be limited to a maximum value that is independent of the power supply chosen for the circuit in which the JMOS is embedded. As a result, the correct design of the JMOS can effectively implement down-scaling the drain voltage of the intrinsic MOSFET without forfeiting the full V_{DD} drive on the gate of the MOSFET. Because this property is not shared by the other LDDs, the JMOS has the potential to extend the limits of constant-voltage scaling to channel lengths even shorter than those in the current LDDFETs. The field-reduction properties resulting from n^- diffusion is one of the advantages of both the LDDFET and the double-diffused lightly doped drain FETs and is equally shared by the JMOS. Gate oxide reliability is improved by reducing the intensity of the drain electric fields in the JMOS in two ways: by lowering the effective drain voltage and grading the drain junction. After gate oxide reliability is guaranteed by this designer-controlled "scaling" of drain bias, power

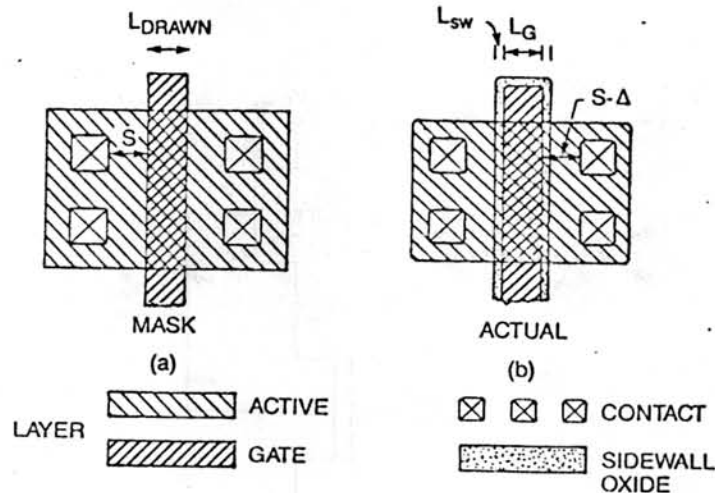


Figure 3.7: TOP VIEW OF THE JMOSFET. (a) Mask layout showing active, gate, and contact layers. (b) Actual pattern after processing

supply can be increased or the MOSFET channel length can be reduced at a given supply voltage to further enhance performance.

In the JMOS, the JFET under the sidewall oxide is fully merged into the MOSFET structure and does not need additional silicon area; however, it does require a minimum of one extra mask in the process. The area under the sidewall where the JFET is located is normally a parasitic region that comprises part of the design-rule specified distance S between the gate electrode and the source/drain contact openings as illustrated in Fig. 3.7a. The actual gate length L_G and gate-to-contact separation $S - \Delta$ (Fig. 3.7b) include the effects of mask-to-wafer pattern transfer such as resist exposure and development, gate-electrode and source-drain oxide-etching bias, and interlayer lithographic-registration errors.

In summary, one of the advantages of the JMOS over the conventional As-drain MOSFET is the reduction of the drain fields through drain junction grading. The possibility of designer-controlled reduction of the effective drain bias V_{D_i} is also a major advantage of the JMOS over other LDD and conventional designs; such reduction can be accomplished independent of the power-supply voltage chosen.

The asymmetry of the JMOS with respect to source and drain diffusions, which is not present in conventional and lightly doped drain devices, has simultaneous advantages and disadvantages. The advantage is the potential reliability improvement through the above V_{D_i} reduction, and, with heavily doped source diffusion, this reduction is accomplished without lowering the effective gate-to-source voltage drive. Lightly doping the source and drain of symmetric LDDFETs results in transconductance degradation caused by the series source resistance that reduces the effective V_{GS} drive. The major disadvantages are the additional complexity of the JMOS fabrication process and reduced circuit performance as a bidirectional switch or pass transistor.

The drain region of the JMOSFET must be designed to take advantage of the saturating properties of the JFET while minimizing the performance reduction resulting from this series device. The following section demonstrates the appropriateness of the model in Fig. 3.6 via circuit and two-dimensional device simulations and describes the principles of operation that will impact its VLSI applications.

3.3 JMOS Device Simulation

3.3.1 Circuit Simulation

The JMOS circuit model in Fig. 3.6 was simulated via SPICE, and the transfer function V_{D_i} vs V_{DS} is plotted in Fig. 3.8 for $V_{GS} = 1,5$ V and $V_{T_J} = -1, -3, -5$ V, where V_{T_J} is the JFET threshold voltage, V_{D_i} is the effective drain bias on the intrinsic MOSFET, and V_{DS} is the externally applied drain bias. Both source and substrate are grounded. The MOSFET HPSPICE and JFET parameters are listed in Table 3.1. The MOSFET parameters were extracted from measurements of conventional devices fabricated with 2 μm technology; the experimental procedures for model parameter extraction are outlined in Appendix A. The voltage-saturating properties of three JFET devices are illustrated in Fig. 3.8. For drain voltages larger than $V_{SUB} - V_{T_J}$, the JFET current saturates as does the JMOS current. As a result, V_{D_i} on the intrinsic MOSFET is pinned at a value below the V_{DS} bias externally

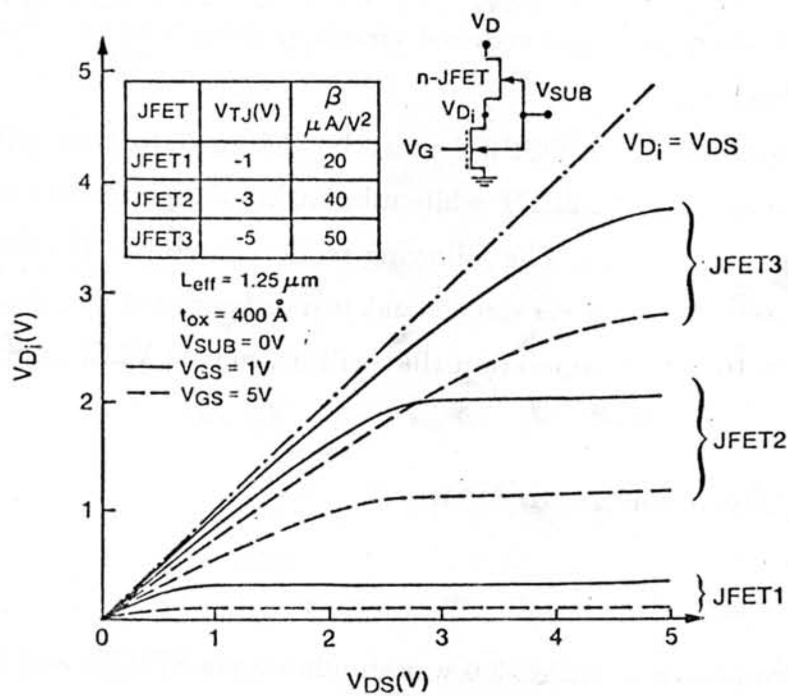


Figure 3.8: V_{D_i} – V_{DS} VOLTAGE TRANSFER FUNCTION FOR JMOSFETs WITH THREE JFET DESIGNS.

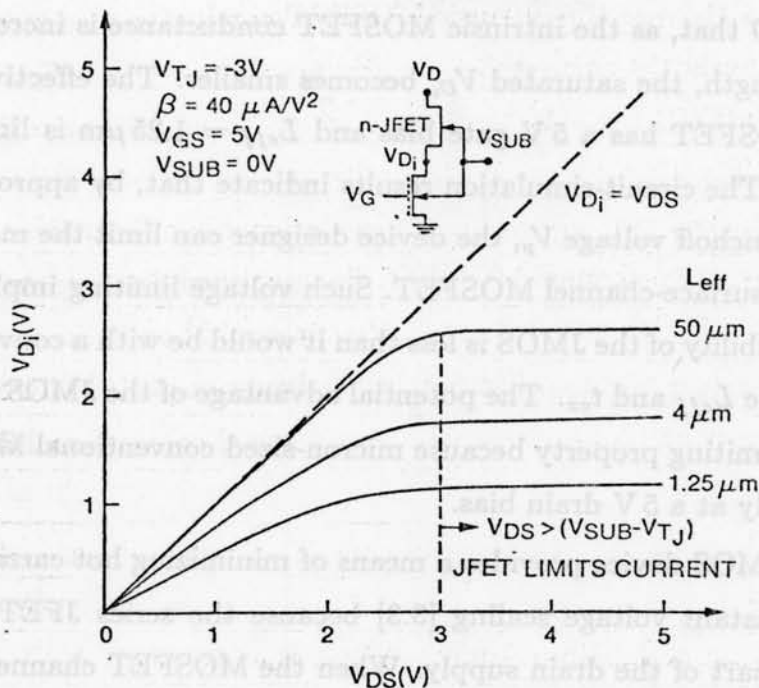


Figure 3.9: $V_{D_i} - V_{DS}$ VOLTAGE TRANSFER FUNCTION FOR THREE MOSFET CHANNEL LENGTHS.

applied to the JMOS and is limited to a maximum value as the flat portions of the curves labeled JFET2 and JFET1 indicate in Fig. 3.8. This maximum V_{D_i} decreases as the MOSFET gate bias increases. The electrical parameters for the three JFETs in Fig. 3.8 are shown in Table 3.1; these devices are modeled in SPICE by only three parameters: V_{T_J}, the transconductance factor β, and the channel-length modulation factor. The transconductance factor is proportional to the low field conductance and the width/length ratio of the channel region in the series JFET. The smaller the $|V_{TJ}|$, the lower the JFET low field conductance, and the larger the effect of the JFET on the linear-region ON-resistance of the JMOS. The optimization of the JFET pinchoff voltage V_p ($V_p = V_{TJ} - \phi_{bi}$) and of the low field conductance is discussed in Chapter 5.

The effect of varying the MOSFET channel length is plotted in Fig. 3.9 when

the MOSFET has V_{GS}= 5 V; the parameters are those of the JFET2 in Table 3.1. It can be seen in Fig. 3.9 that, as the intrinsic MOSFET conductance is increased by shortening its gate length, the saturated V_{D_i} becomes smaller. The effective drain voltage when the MOSFET has a 5 V gate bias and $L_{eff} = 1.25\,\mu$m is limited to 1.2 V by the JFET2. The circuit-simulation results indicate that, by appropriately choosing the JFET pinchoff voltage V_p, the device designer can limit the maximum drain bias across the surface-channel MOSFET. Such voltage limiting implies that the current-drive capability of the JMOS is less than it would be with a conventional MOSFET having same L_{eff} and t_{ox}. The potential advantage of the JMOS is based on its drain voltage-limiting property because micron-sized conventional MOSFET cannot operate reliably at a 5 V drain bias.

As a result, the JMOS device provides a means of minimizing hot carrier problems imposed by constant voltage scaling [3.3] because the series JFET can be designed to support part of the drain supply. When the MOSFET channel is conducting current, the inequality

$$V_{D_i} < (|V_p| - \phi_{bi} - |V_{SUB}|) = V_{SUB} - V_{T_J} \tag{3.1}$$

holds, where ϕ_{bi} is the p^+n^- junction built-in potential. In practical n-channel JMOS designs, V_p, V_{T_J}, $V_{SUB} \leq 0$ V. Limiting V_{D_i} could also be accomplished by reducing (most likely to 3 or 3.3 V) the supply voltage. As discussed in Chapter 2, lowering V_{D_i} is important from the MOSFET reliability point of view given that the reliability measurements are empirically determined to be dependent exponentially on the drain voltage in conventional and LDD structures. The maximum applicable drain voltage in submicron devices is then expected to be determined by the drain structure used in the design. The alternative of lowering the supply voltage in the entire integrated system has important drawbacks because such a reduction leads to compatibility problems, smaller noise margins, and reduced $V_{GS} - V_T$ MOSFET drive. Less gate drive often implies slower circuits. The presence of a series drain JFET in the JMOS device enables the use of the full supply on the V_D and V_G terminals while the internal voltage of the reliability-sensitive node (the MOSFET drain) is reduced. Conventionally designed micron-sized n-MOSFETs actually re-

Table 3.1: SPICE DEVICE PARAMETERS

MOSFET PARAMETERS			
Name	*Symbol*	*Value*	*Unit*
Low field mobility	μ_o	665	$cm^2V^{-1}sec^{-1}$
Oxide thickness	t_{ox}	393	Å
Transconductance factor	K_P	58.5	μAV^{-2}
Threshold voltage	V_{T_O}	0.32	V
Effective substrate doping	N_{SUB}	9.1×10^{15}	cm^{-3}
Body factor	γ	0.515	$V^{-1/2}$
$(L_{mask} - L_{eff})/2$	L_D	0.25	μm
Gate-field mobility factor	$\Theta\ (V_{NORM}^{-1})$	0.061	V^{-1}
Longitudinal field mob. factor	E_{TRA}	7.3×10^4	$V\ cm^{-1}$
Critical field	E_{CRIT}	1.7×10^4	$V\ cm^{-1}$
Saturated drain conductance	DE_{SAT}	7.9×10^9	$V\ cm^{-2}$
JFET PARAMETERS			
Threshold voltage	V_{T_J}	−1, −3, −5 *	V
Transconductance factor	β	20, 40, 50 *	μAV^{-2}
Channel-length modulation	λ	0.05	V^{-1}

* JFET1, JFET2, JFET 3

quire drain biases of less than 3 V to saturate the channel current in the practical range $0 < (V_{GS} - V_T) < 5$ V, as shown in Fig. 3.10. This is simply the effect of saturation of the channel electron average velocity $\langle v \rangle$. Submicron devices operating in this saturated-velocity regime will have a drain saturation current of

$$I_{DS_{sat}} = W \langle v \rangle C_{ox}(V_{GS} - V_T) \tag{3.2}$$

where $\langle v \rangle \simeq v_{sat}$ (optical phonon scattering-limited drift velocity for bulk transport).

After it pinches off, the drain JFET limits the JMOS current approximately to

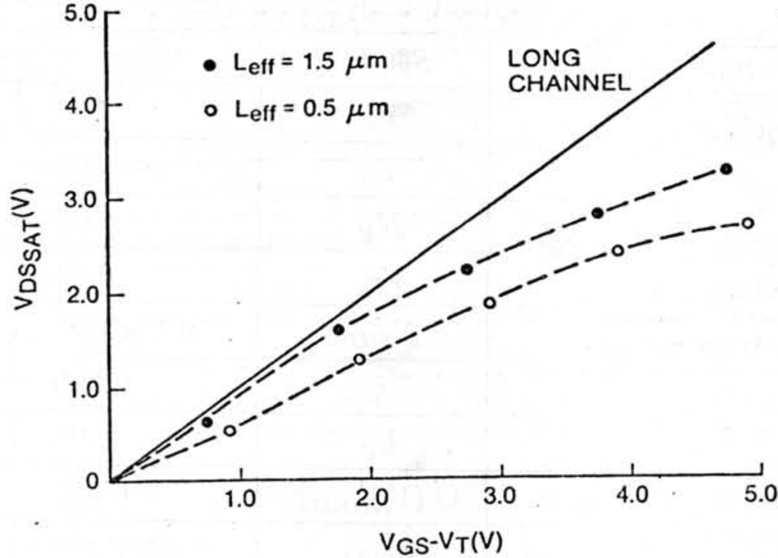


Figure 3.10: SATURATION DRAIN VOLTAGE DEPENDENCE ON $V_{GS} - V_T$ IN A CONVENTIONAL N-CHANNEL MOSFET.

its first order pinchoff limit I_p [3.15],

$$I_p = W_J I_{po} \left[1 - \left(\frac{\phi_{bi} + V_{D_i} + |V_{SUB}|}{|V_p|} \right) \right]^2 \tag{3.3}$$

$$I_{p_o} = \frac{|V_p|}{n \rho_s L_{sw}} \tag{3.4}$$

where $n (2 < n < 3)$ accounts for the nonuniform doping profile in the n^- JFET channel, $\rho_s(\Omega/\square)$ is buried n^- sheet resistivity, W_J is JFET channel width, L_{sw} is sidewall spacer width (an approximate measure of the JFET effective electrical channel length), and $V_{D_i}(V_{GS})$ is the gate voltage-dependent effective MOSFET drain or effective JFET source voltage according to the lumped circuit model proposed to describe the JMOS. The transconductance factor of the JFET SPICE model is

$$\beta = \frac{W_J I_{p_o}}{V_p^2} \tag{3.5}$$

Equation (3.3) neglects the short JFET channel-length effects which are more important when n^- doping is lighter or, alternatively, when ρ_s is larger. The I_{po}

value in $A/\mu m$ width depends on the technology design of the vertical impurity profile of the drain JFET and the sidewall spacer width; the shortest width that still forms a JFET under the sidewall oxide should be used to minimize current-drive loss.

3.3.2 Two-Dimensional Device Simulation

The JMOS was simulated by the PISCES two-dimensional program [3.16,3.17] coupled to impurity profiles simulated in one dimension by SUPREM-III [3.18]. Two-dimensional device simulations have been widely employed as useful tools to guide and better understand the design of LDDs [3.19]. Figure 3.11 presents the equipotential contours for the conventional, LDD, and JMOS devices under saturation bias conditions ($V_D = 5$ V, $V_G = 2$ V, $V_S = V_{SUB} = 0$ V). As discussed in Chapter 2, under these conditions, the maximum generation of substrate current through impact ionization occurs in the high field region near the drain. Oxide thickness is 400 Å in the conventional device and 200 Å in the others. Substrate doping has been adjusted to obtain enhancement transistors with 0.3 to 0.5 V threshold voltages in all three devices. The simulated equipotentials in Fig. 3.11 provide valuable insight into the inner operation of the proposed JMOS when compared to other MOSFET designs. The two-dimensional field distribution in the drain region of the JMOS can vary considerably from that of the conventional and LDD designs that develop the high fields in the pinchoff region near the drain; the LDDs spread and somewhat reduce the field intensity. For reliability reasons, the depletion region in the LDD cannot extend beyond the gate edge. In the JMOSFET in Fig. 3.11 the p^+/n^- region is designed such that the JFET pinches off the drain equipotentials under the p^+ JFET gate. The high field region is then buried away from the sensitive $Si\text{-}SiO_2$ interface, on which hot carriers may impinge, and the drain current is diverted into the bulk in the drain end of the surface-channel device. In this example, V_{T_J}=−1.6 V, as obtained from PISCES simulations. The JFET pinchoff voltage and low field conductance are the design parameters, in addition to those of conventional MOSFETs, that will determine the main characteristic of the JMOSFET

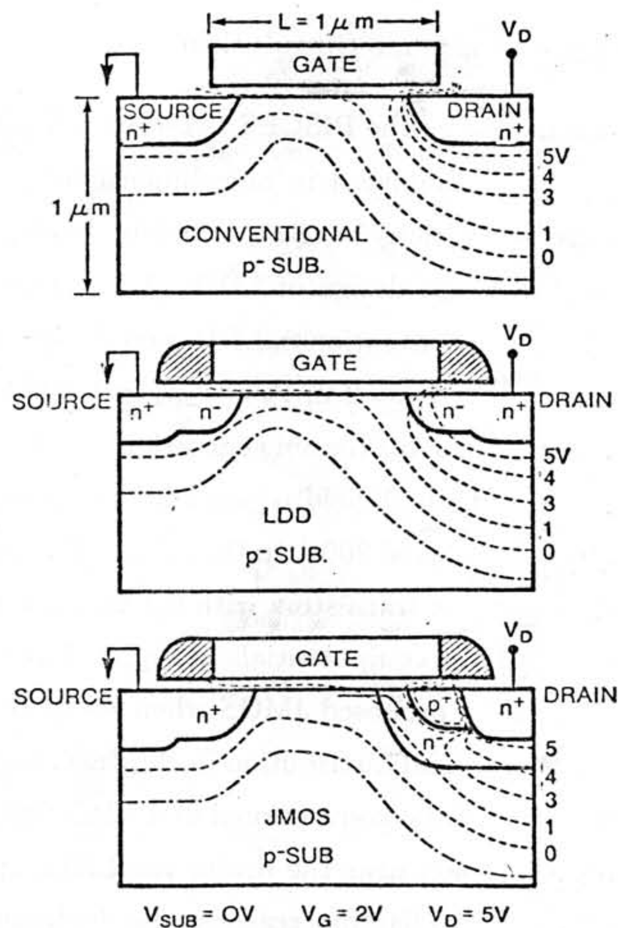


Figure 3.11: SIMULATED EQUIPOTENTIAL CONTOURS FOR THE CONVENTIONAL, LDD, AND JMOSFET TRANSISTORS WITH MICRON-SIZED L_{eff}. Saturation bias condition are V_{DS}= 5 V, V_{GS}= 2 V V_{SUB} = 0 V.

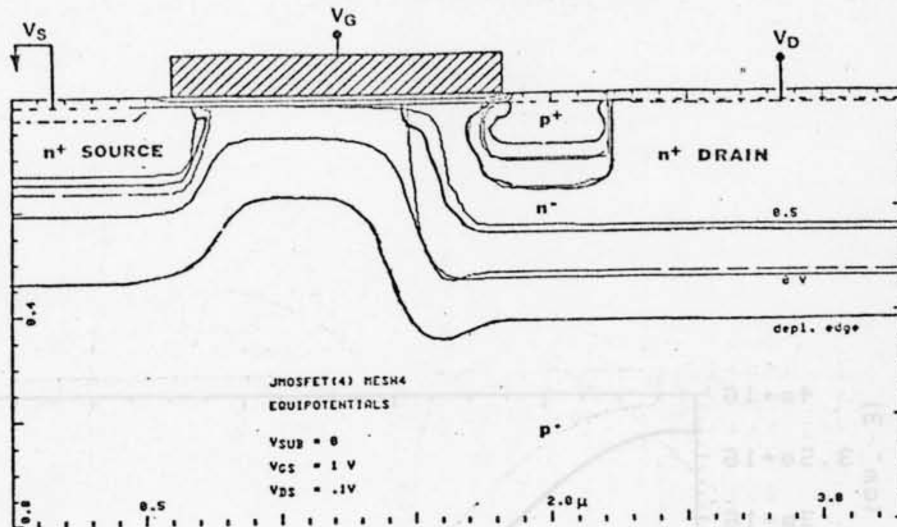


Figure 3.12: PISCES SIMULATED EQUIPOTENTIAL CONTOURS FOR THE JMOSFET WITH $L_{eff} = 0.72\,\mu m$, $t_{ox} = 200\,\text{Å}$, $V_{T_J} = -1.6\,\text{V}$, V_{SUB}=0 V. Linear region bias of JFET, V_{DS}=0.1 V and V_{GS}=1 V.

insofar as current transport is governed by two field-effect devices in series.

3.3.2.1 JMOS with Low PinchOff Voltage

A JMOS device with a submicrometer effective MOSFET channel length and a 200 Å gate oxide was simulated in the PISCES simulator to extract its I-V characteristics. The oxide thickness chosen is typical of that required for correctly scaled submicrometer technologies. Figure 3.12 shows the equipotential contours for the JMOS under a bias condition in which both the JFET under the sidewall oxide and the surface MOSFET are in their linear region of operation. In this mode, the n^- region behaves like a series pinched resistor or a buried LDD structure, and the linear region ON-resistance for the JMOS then becomes the series association of the MOSFET and JFET ON-resistances.

The gaussian impurity profiles for the JMOS simulation in Fig. 3.12 are shown in Figs. 3.13 and 3.14 for the channel and JFET regions, respectively, and are

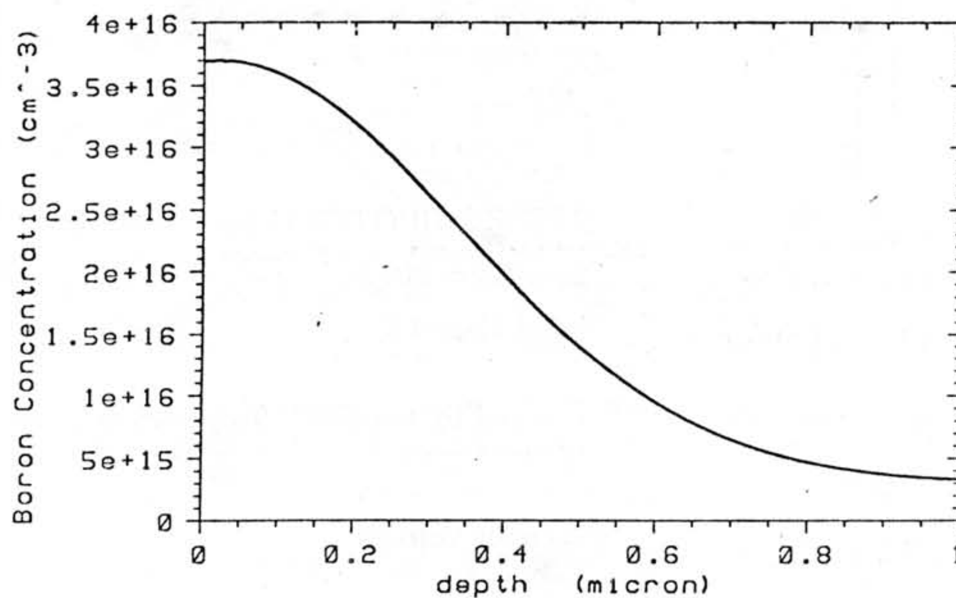


Figure 3.13: PROFILE FOR THE CHANNEL REGION OF THE JMOSFET IN Fig. 3.12.

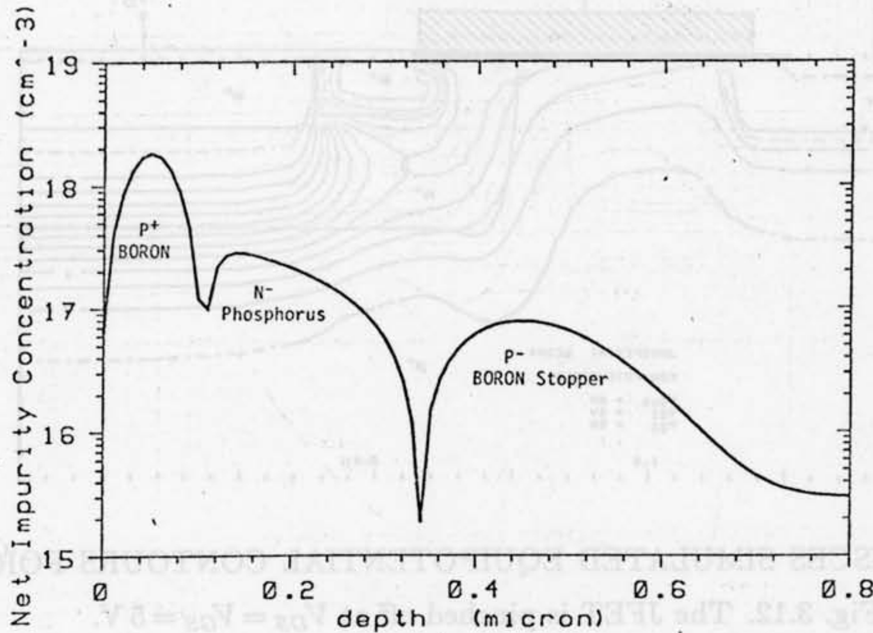


Figure 3.14: JFET CHANNEL PROFILE FOR THE JMOS IN Fig. 3.12.

analytically specified for the device simulator. The MOSFET channel-region doping of the simulated device has a boron peak concentration of $3.4\times10^{16}\text{cm}^{-3}$. The net impurity profile of the n^- JFET channel has a peak doping of $2.8 \times 10^{17}\text{cm}^{-3}$ and a total net dose of 3.6×10^{12} cm^{-2}. For such a small net dose, the JFET pinchoff voltage is low. The threshold voltage, defined as the JFET gate (or MOSFET substrate) voltage for which $I_{DS} = 0.1\,\mu A/\mu m$ at $V_{GS} = 5\,\text{V}$ and $V_{DS}= 0.1\,\text{V}$, was obtained by PISCES as $V_{T_J}= -1.6\,\text{V}$. The p^+/n^- junction depth is $x_{j_{p^+}} = 0.11\ \mu\text{m}$ and the n^-/p junction depth is $x_{j_{n^-}} = 0.34\ \mu\text{m}$. As demonstrated in the following process simulation results, it is very difficult to achieve such shallow junction depths, especially when higher pinchoff voltages are required. The deep boron implant in Fig. 3.14 (2×10^{12} at 160keV) was added to limit the $x_{j_{n^-}}$ junction depth and to serve as a punchthrough stopper to constrain the drain fields from encroaching into the MOSFET channel region.

For the bias condition in Fig. 3.15, the saturation properties of the drain JFET

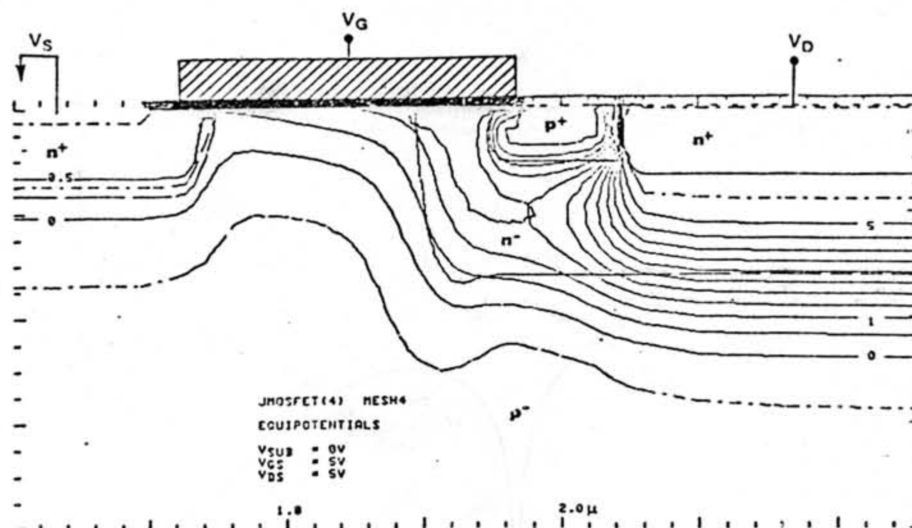


Figure 3.15: PISCES SIMULATED EQUIPOTENTIAL CONTOURS FOR THE JMOSFET IN Fig. 3.12. The JFET is pinched off at $V_{DS} = V_{GS} = 5\,\text{V}$.

are illustrated. For the biases in which the JFET is ON and pinched off, that is,

$$(V_{DS} - V_{SUB}) \geq |V_{T_J}| \tag{3.6}$$

the saturated JFET limits the current to the value of $I_p(V_{GS})$ in Eq. (3.3). The simulated device in Fig. 3.15 with $V_{T_J} = -1.6\,\text{V}$ is biased at $V_{DS} = 5\,\text{V}$ $V_{SUB} = 0\,\text{V}$. The JFET pinchoff region then supports most of the 5 V drain bias in this JMOS design, and the surface-channel MOSFET supports less than 1 V. As indicated in the simulated field pattern under the SiO_2/Si interface, this will result in a large reduction in impact ionization under the MOSFET gate, as will be demonstrated experimentally.

The electron and net donor densities and the electrostatic potential along the JMOS Si/SiO_2 interface $(A - A')$ are plotted in Fig. 3.16 for $V_{GS} = 1\,\text{V}$, $V_{DS} = 5\,\text{V}$, and $V_{SUB} = -1\,\text{V}$. Because most of the drain potential drops along the n^- JFET channel, an effectively low drain bias V_{D_i} appears to drive the MOSFET inversion layer. This bias can be inferred from the electron quasi-Fermi potential in the electron accumulation layer that forms in the n^- region under the MOSFET polysilicon

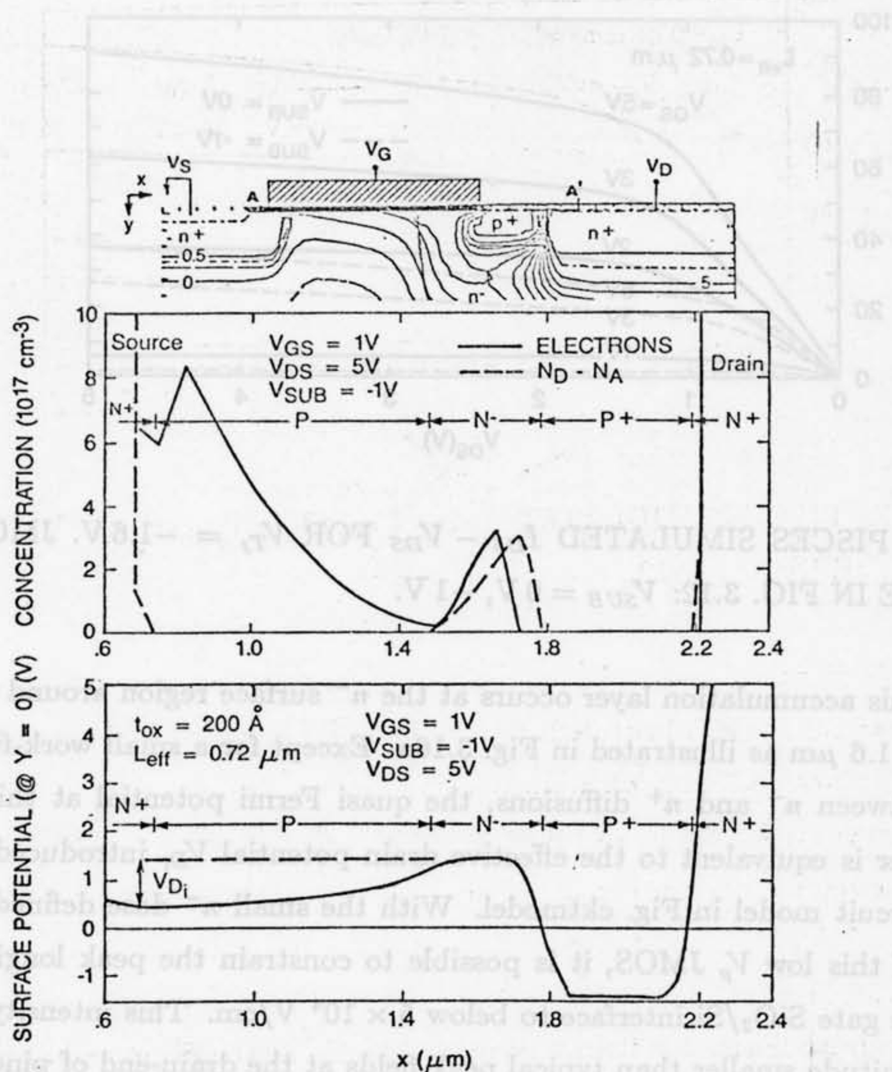


Figure 3.16: PISCES SIMULATED ELECTRON CONCENTRATION AND POTENTIAL ALONG THE Si/SiO_2 INTERFACE (line $A - A'$ in the top insert). JMOS structure in Fig. 3.12: $V_{SUB} = -1$ V, $V_{DS} = 5$ V, $V_{GS} = 1$ V. (a) Electron and (input-specified) net donor densities. (b) Electrostatic Potential.

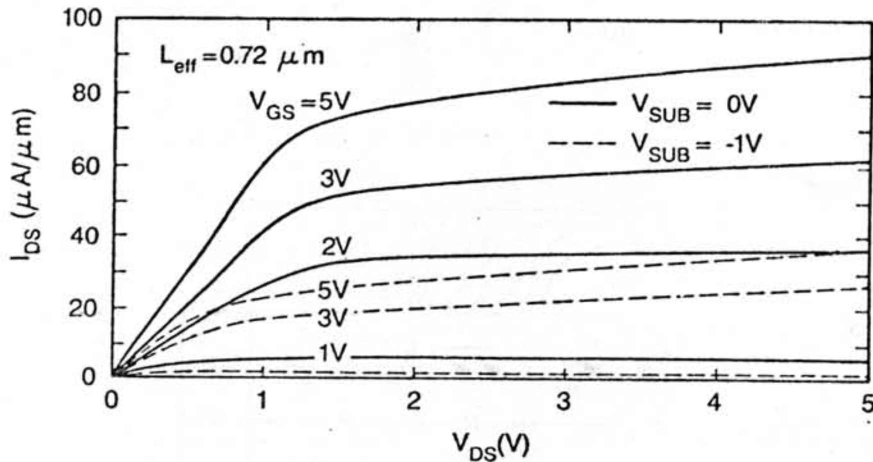


Figure 3.17: PISCES SIMULATED $I_{DS} - V_{DS}$ FOR $V_{T_J} = -1.6$ V. JMOSFET STRUCTURE IN FIG. 3.12: $V_{SUB} = 0$ V, -1 V.

electrode. This accumulation layer occurs at the n^- surface region around the coordinate $x = 1.6$ μm as illustrated in Fig. 3.16a. Except for a small work-function difference between n^- and n^+ diffusions, the quasi Fermi potential at this accumulation layer is equivalent to the effective drain potential V_{D_i} introduced in the equivalent circuit model in Fig. cktmodel. With the small n^- dose defined in the simulation of this low V_p JMOS, it is possible to constrain the peak longitudinal E-field at the gate SiO_2/Si interface to below 5×10^4 V/cm. This intensity is one order of magnitude smaller than typical peak fields at the drain-end of pinched off conventional VLSI MOSFETs [3.20]–[3.22].

The PISCES-simulated I-V characteristics are plotted in Fig. 3.17 for the JMOSFET in Fig. 3.15. In this device, the onset of saturation is independent of V_{GS} because the drain JFET pinches off at the drain voltages for which Eq. (3.6) is an equality. The gating action of the JFET through the application of substrate bias is illustrated by the reduction of drain current at lower substrate voltages and at constant V_{DS} and V_{GS} in Fig. 3.17. Here, the JFET operates as a current-limiting active device fully merged into the LDD region.

The PISCES-simulated transfer function I_p/W vs V_{GS} is plotted in Fig. 3.18

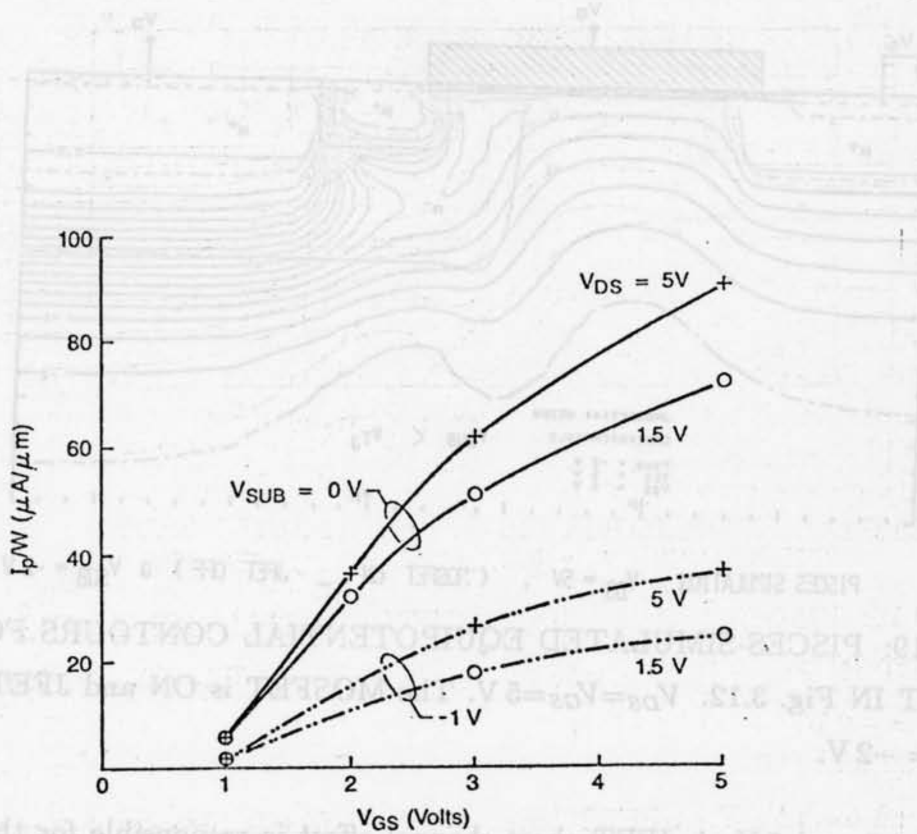
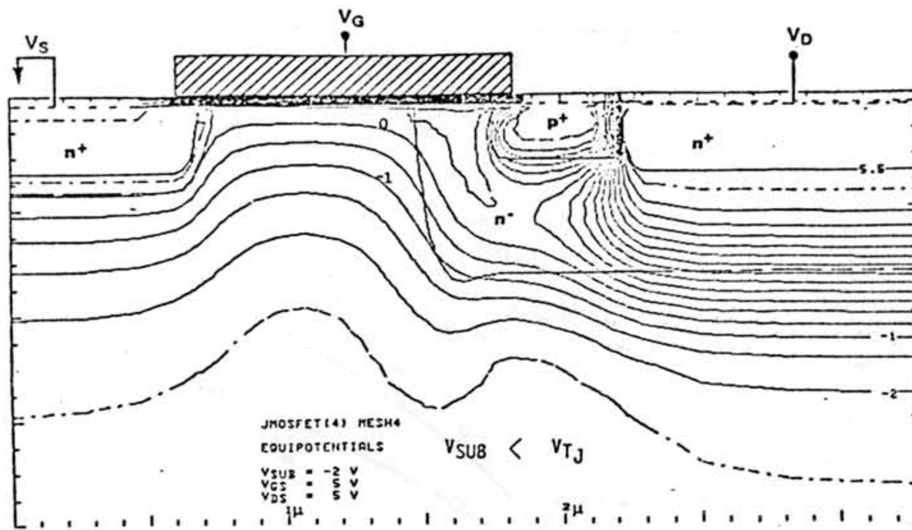


Figure 3.18: DEPENDENCE OF THE PINCHOFF CURRENT PER UNIT CHANNEL WIDTH ON V_{GS}. PISCES simulation of the JMOSFET in Fig. 3.12. $V_{SUB} = 0$ V.



PISCES SIMULATION V_{DS} = 5V . (MOSFET ON _ JFET OFF) @ V_{SUB} = -2 V

Figure 3.19: PISCES-SIMULATED EQUIPOTENTIAL CONTOURS FOR THE JMOSFET IN Fig. 3.12. V_{DS}=V_{GS}=5 V. The MOSFET is ON and JFET is OFF at $V_{SUB} = -2$ V.

for V_{DS}= 1.5 and 5 V. A JFET short-channel effect is responsible for the output conductance in Fig. 3.17 and the variation of $I_p(V_{GS})$ with V_{DS} in Fig. 3.18. This effect is apparent in the equipotentials in Fig. 3.15 as the drain field encroaches under the entire length of the p^+ JFET gate and depletes most of the n^- JFET channel.

Figure 3.19 shows the same device under bias conditions that turn the JMOSFET off through the application of substrate bias while the MOSFET surface is strongly inverted; here, V_{GS}= 5 V and $(V_{SUB} - V_{D_i}) \leq V_{T_J}$(the drain JFET region is OFF and the MOSFET is ON); it is possible, therefore, to turn off all JMOSFETs on a chip through the appropriate substrate bias. The operation of the JFET in its subthreshold regime is evident in the simulated subthreshold log(I_{DS})–V_{GS} characteristics in Fig. 3.20. The drain current when $V_{GS} \gg V_T$ flattens to a value that depends exponentially on V_{SUB} in the regime where $V_{SUB} < V_{T_J}$. The operation of the drain JFET in the subthreshold is qualitatively similar to the static-induction transistor in which a diffused region is biased such that it controls the flow of ma-

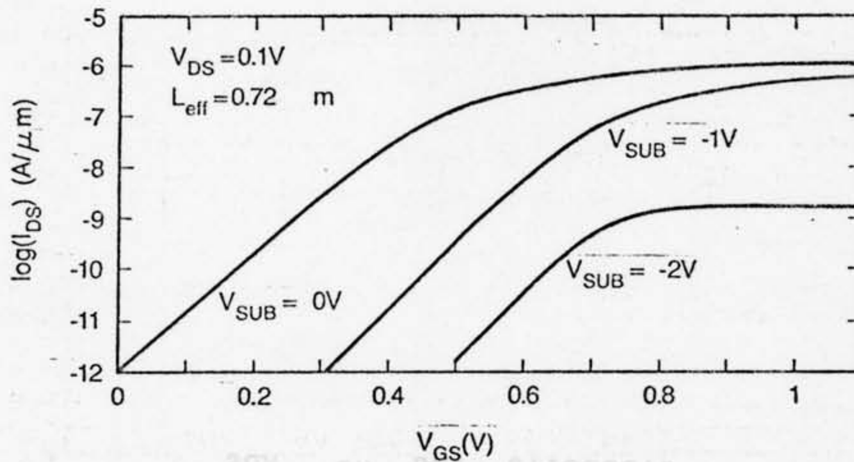


Figure 3.20: PISCES-SIMULATED SUBTHRESHOLD CHARACTERISTICS FOR THE JMOSFET STRUCTURE IN Fig. 3.12.

jority carrier current over a potential barrier in a space-charge region.

The $I_{DS} - V_{DS}$ simulated characteristics of the low V_p JMOS in Fig. 3.17 are compared to those of the conventional n^+ As drain MOS with a submicrometer channel length ($L_{eff} = 0.6\,\mu m$) in Fig. 3.21. Both devices have the same oxide thickness ($t_{ox} = 200\,\text{Å}$) and MOSFET channel doping. The substrate bias is 0 V. The PISCES-simulated low V_p characteristics (dashed lines) are shown for V_{GS}=1, 3, 5 V. The conventional device characteristics (solid lines) in Fig. 3.21 for V_{GS}=1 and 3 V illustrate the considerable drive penalty imposed by the low V_p JFET which demonstrates that, although the surface fields in the MOSFET can be minimized by a JMOS design with low V_p, this effect is accompanied by a reduced current-drive capability.

In addition to demonstrating the basic operation of the device, the PISCES simulations for the submicrometer JMOS with low V_p also identified two important design aspects. First, the profile of the JFET should be designed for a minimum performance penalty but still maintain an acceptable high-field pattern. Second, the two-dimensional merging of the JFET and MOSFET channels requires an accurate model for the two-dimensional spreading of the impurity profile. The two-

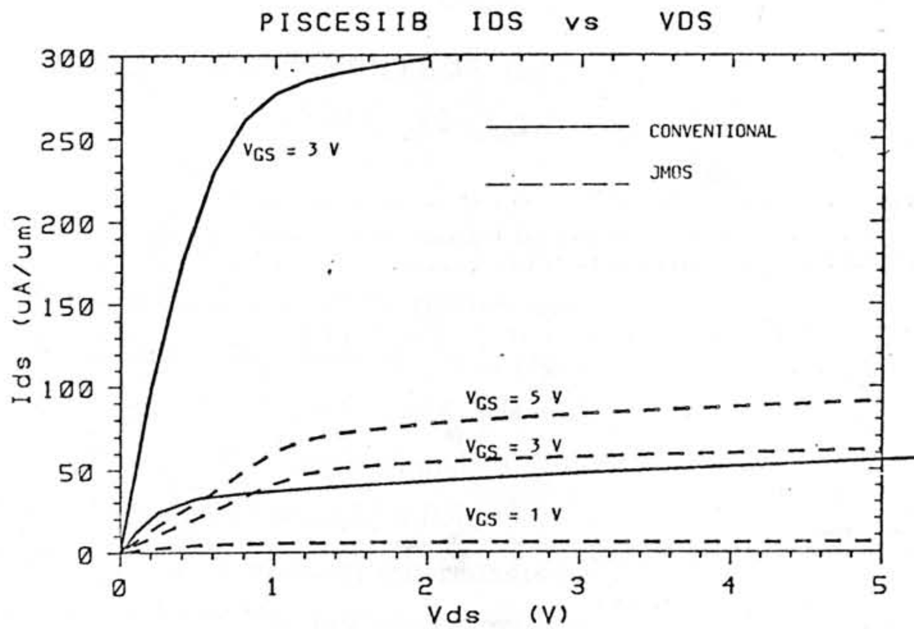


Figure 3.21: COMPARISON OF SIMULATED I–V CHARACTERISTICS FOR A CONVENTIONAL MOSFET (SOLID LINE) AND THE LOW V_p JMOS IN FIG. 3.12 (dashed line).

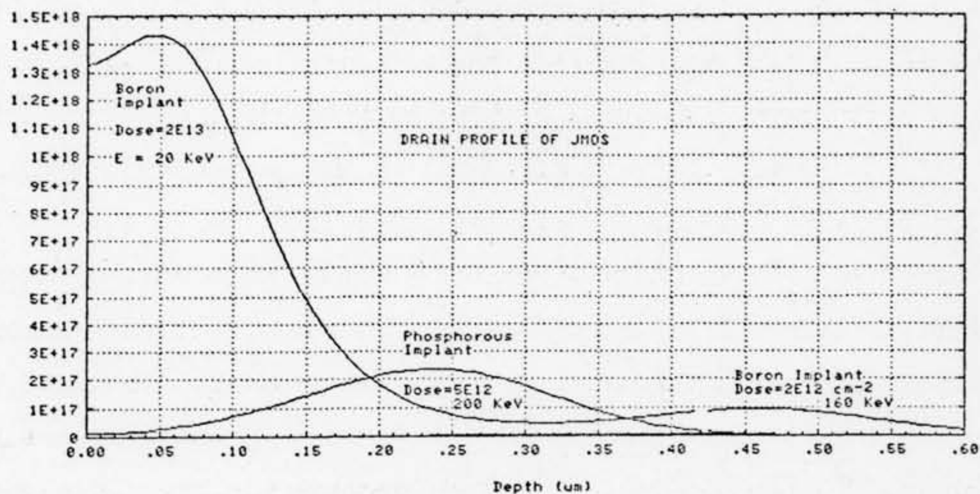


Figure 3.22: SUPRA-SIMULATED PROFILE OF THE DRAIN JFET. Deep n^- phosphorus implant annealed at 950°C for 30 min.

dimensional current path in the drain JFET region of the JMOS is affected by the lateral distribution of n^- and p^+ impurities. For the PISCES simulations of the low V_p JMOS, analytical profiles were specified and were then extended laterally by PISCES; this procedure may not accurately represent the two-dimensional distribution of impurities in the structure.

3.3.2.2 Two-Dimensional SUPRA Simulations

The merging of the MOSFET surface channel with the JFET n^- channel impurity profile in the lateral direction was studied in a two-dimensional process simulator SUPRA [3.23] and a two-dimensional device simulator GEMINI [3.24] suitable for analysis of nonplanar structures. GEMINI accepts two dimensional impurity distributions from SUPRA to obtain a solution of the Poisson equation.

For a VLSI implementation of the JMOS, only low-temperature diffusions (below 950°C) are recommended. Because this has been the trend in VLSI processes, shallow junction depths according to the scaling rules are possible. A low-temperature JMOS profile for the drain JFET, as studied with SUPRA, is triple

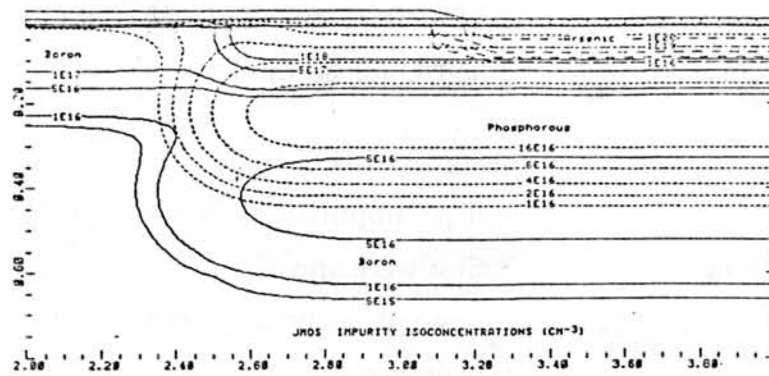


Figure 3.23: SUPRA-SIMULATED IMPURITY CONTOURS OF THE JFET IN Fig. 3.22. The boron contours are indicated by the solid lines, phosphorus contours by the short-dashed lines (- - -), and arsenic contours by the long-dashed lines (– – –).

implanted with a p^+ boron implant, a deep boron stopper implant, and a deep 200 keV phosphorus implant. The one-dimensional profile across the drain JFET region, after a 30 min inert ambient anneal at 950°C is plotted in Fig. 3.22. The resulting impurity contours in the drain JFET region are shown in Fig. 3.23 for the boron, phosphorus, and arsenic chemical concentrations. The JFET n^- region does not merge with the MOSFET Si/SiO_2 interface channel in such JFET profile with a deep phosphorus implant annealed at low temperature. The SUPRA-simulated two-dimensional profile was used as input to the Poisson-equation solver GEMINI [3.24]. Figure 3.24 shows the equipotential lines, metallurgical junctions, and depletion edges in the JMOS with the JFET profiles in Fig. 3.23. Here, the n^- region does not reach toward the surface of the MOSFET when the JFET has a deep phosphorus implant annealed at 950°C. As a consequence, the JMOS does not operate properly because no effective drain connection exists for the surface channel as can be seen in Fig. 3.24 where the surface MOS-gate-induced depletion layer does not merge with the p^+/n^- depletion layer.

Additional SUPRA simulations revealed that a retrograde n^- phosphorus profile annealed simultaneously with the p^+ implant at temperatures below 1000°C did not result in a satisfactory merging of the JFET and surface channel MOSFET. An alternative profile, simulated by SUPRA, consisted of a phosphorus implant annealed at 1050°C to provide enough lateral diffusion followed by a p^+ implant annealed at 900°C. The resultant merging of the JFET n^- region with the MOSFET is illustrated in Fig. 3.25 for V_{DS}= 5 V. The two-dimensional profiles for the GEMINI simulation in Fig. 3.25 were obtained by SUPRA simulation of the 1050°C JFET process. The GEMINI solution for the two-dimensional potential in Fig. 3.25 is incorrect, however, because GEMINI does not solve the carrier-continuity equations, and the inversion and accumulation layers along the surface, (PISCES simulation in Fig. 3.16) cannot be modeled by the GEMINI Poisson-equation solver.

The SUPRA simulations verified the adequate thermal cycling used in the implementation of the JMOSFETs to be described in Chapter 4. The major drawbacks of the 1050°C thermal cycle were that it resulted in deep n^-/substrate junction

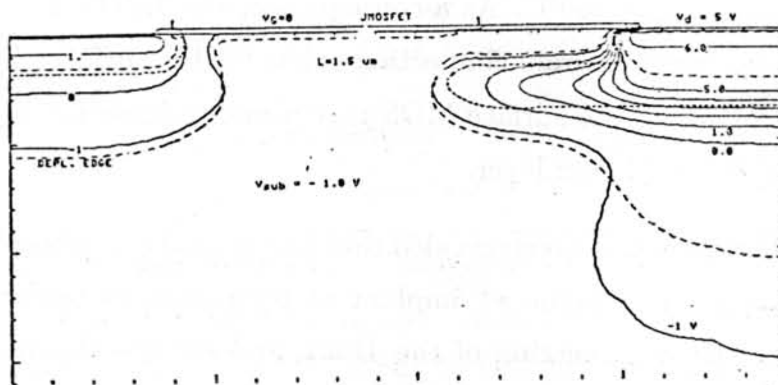


Figure 3.24: GEMINI SIMULATION SHOWING THE EQUIPOTENTIALS IN AN INCOMPLETELY MERGED JFET. The MOSFET surface depletion region does not merge with the JFET drain. Drain bias $V_{DS} = 5\,\mathrm{V}$, $V_{SUB} = -1\,\mathrm{V}$.

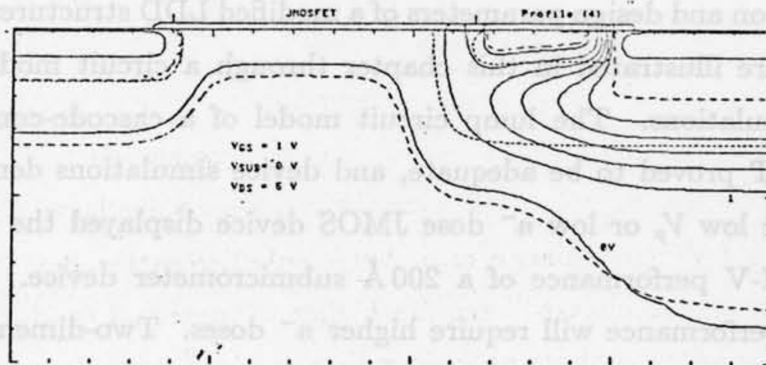


Figure 3.25: GEMINI SIMULATION OF THE LOW V_p JMOS SIMULATED BY SUPRA. The n^- implant was annealed at 1050°C. The equipotentials show an adequate merging of the MOSFET and JFET depletion regions.

depths ($> 0.5\,\mu m$) and spread the MOSFET channel threshold-adjusting implant. This annealing was employed in the implementation of both low and high V_p JMOS designs; the high V_p JMOS profiles are described in Chapter 4.

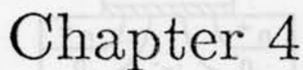
Through extensive GEMINI simulations of the JMOS, the electrical characteristics of the JMOSFETs were found to be very sensitive to the two-dimensional impurity distribution in the drain JFET region. As a result, the JMOS could well serve as a vehicle to test electrically the two-dimensional impurity-diffusion models. The two-dimensional process simulator SUPRA implements numerical models for the implantation and diffusion steps that may not be physically accurate. The vertical distribution of implanted ions is assumed to be gaussian, and the distribution in the lateral direction is weighted by an $erfc\left(x/\sqrt{2}\sigma_x\right)$ dependence where σ_x is the lateral standard-deviation constant used in the modeling. Two-dimensional diffusion phenomena relevant for JMOS lateral diffusion are not modeled, as the Si/SiO_2 interface generation and recombination of point defects. The models implemented

by SUPRA are simple enough to provide a fast simulator with first-order models.

3.4 Summary

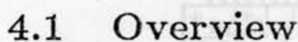
The operation and design parameters of a modified LDD structure, the proposed JMOSFET, were illustrated in this chapter through a circuit model and circuit and device simulations. The lump circuit model of a cascode-connected JFET and a MOSFET proved to be adequate, and device simulations demonstrated its operation. The low V_p or low n^- dose JMOS device displayed the impact of the JFET on the I-V performance of a 200 Å submicrometer device. Optimization of the JMOS performance will require higher n^- doses. Two-dimensional process simulations indicated a thermal cycling that would guarantee the operation of the JMOSFET as a merged JFET-MOSFET structure. The encroachment of high fields under the gate of the MOSFET can be controlled through correct design of the LDD region by adjusting the pinchoff voltage in the JFET region to maximize current drive while constraining the short channel effects and hot carrier injection into the gate oxide to within tolerable limits.

The JMOSFET provides device designers with performance trade-offs somewhat different than do the conventional LDDs. The JMOS can be optimized for a given minimum effective channel length, oxide thickness, and supply voltage. The PISCES-simulated two-dimensional potential distribution suggested that the JMOS can be designed with peak n^- doping densities below $1 \times 10^{18}\text{cm}^{-3}$, contrary to the LDDFETs whose reliability is degraded by injection under the sidewall. This injection mode can be avoided in the JMOSFET design. By keeping the longitudinal E-field peak away from the gate SiO_2/Si interface, the JMOSFET should minimize hot carrier injection into the oxide. These results imply that, by optimizing the drain JFET, this new structure can meet the need for reduced drain supply voltage in submicron channel length MOSFETs while maintaining the hot-carrier-resistant properties in 5 V external supply circuits. The advantage of 5 V operation in micron-sized devices can outweigh the drive loss caused by the series JFET device.



Chapter 4

Experimental Results



4.1 Overview

The JMOS device proposed and simulated in Chapter 3 was fabricated in a 2 μm NMOS process along with the other better known LDD MOSFETs studied in Chapter 2. This chapter discusses the experimental results obtained from the different JMOS designs investigated, and these results confirm the JFET operation predicted by the simulations described in Chapter 3 Both the substrate and gate current characteristics substantiate the voltage-limiting properties of the drain JFET embedded in the JMOS transistor. The fabrication technology employed is first explained, and the results of the dc characterization of the fabricated devices are then presented. The major experimental finding is that the JMOS can sustain 5 V operation even for submicron effective channel lengths because of designer-controlled reduction of the maximum electrical field in the region under the gate traversed by carriers. The results indicate several approaches to optimizing the device for reliable 5 V operation and to avoiding the LDD-related modes of degradation for very low doping concentrations in the n^- region (n^- surface doping below 10^{18}cm^{-3}) for which the LDDFETs are actually less reliable than conventional arsenic-doped n^+ S/D transistors. As with all LDD structures, hot-carrier-related gate and substrate currents have been improved but at the expense of some performance as evidenced by dc device characteristics and ring-oscillator speed comparisons. The correct design of the JMOS, however, can ensure 5 V operation in micron-sized devices. This 5 V capability can extend the limits of CV scaling beyond those possible with conventional

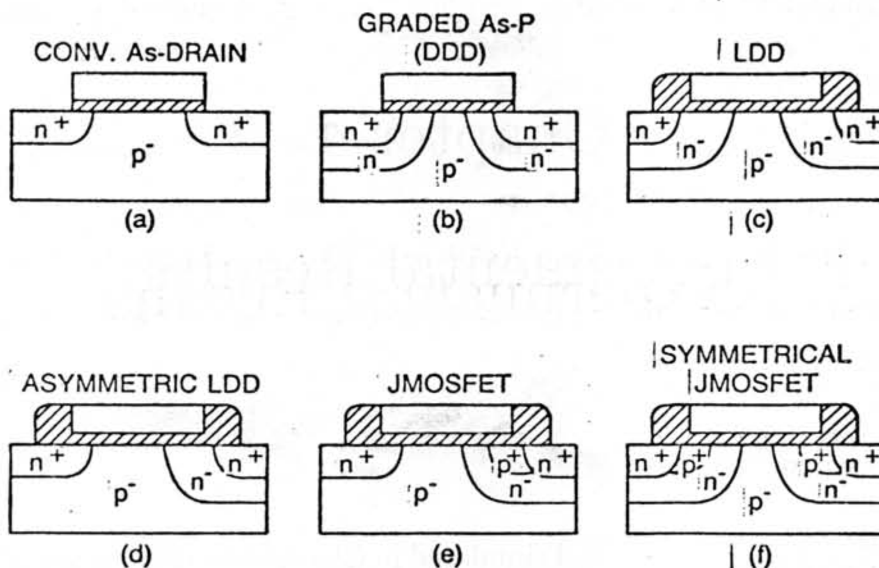


Figure 4.1: CROSS SECTION OF SIX STRUCTURES FABRICATED ON THE SAME CHIP. (a) Conventional n^+As S/D. (b) Double-diffused S/D (DDD). (c) Lightly doped S/D (LDD). (d) Asymmetric LDD. (e) JMOSFET. (f) Symmetrical JMOSFET.

LDDs, and the resulting advantages can outweigh the performance loss.

4.2 Device Fabrication

The fabrication process is a standard 2 μm n-MOS based on LOCOS isolation, a 400 Å gate oxide, and n^+ polysilicon gates. The starting material was ⟨100⟩ 20 to 25 Ω-cm, boron-doped silicon. A 900 Å Si_3N_4 on a 400 Å SiO_2 mask was used during local oxidation. The boron field implant dose was 1.5×10^{13} cm^{-2} at 120keV. Field oxide was grown in steam at 1000°Cfor 200 min.

Both conventional n-MOS and LDD n-MOS devices with five variations in the source/drain regions were fabricated side by side to test experimentally the JMOS along with other better known LDD-MOSFETs. The six S/D structures fabricated (Fig. 4.1) are the conventional As source/drain, double-diffused source/drain, sym-

Table 4.1: MASKING STEPS IN THE JMOS PROCESS.

Mask	*Process Step*	*Standard NMOS*
1	Active area patterning (LOCOS)	X
2	Depletion ion implantation	X
3	Buried polysilicon/silicon contact	X
4	Polysilicon gate patterning	X
5	Phosphorus n^- ion implantation	Maskless†
6	Boron p^+ ion implantation	
7	Arsenic (I) n^+ ion implantation	Maskless
8	Arsenic (II) n^+ ion implantation	
9	Metal-(poly)silicon contact	X
10	Metal layer patterning	X

† LDD process

metrical LDD, asymmetric LDD (n^+As source and lightly doped drain), JMOSFET, and the symmetrical JMOSFET (JFET in both source and drain ends).

Table 4.1 lists the photolithography steps followed to implement the devices and MOS circuits in enhancement–depletion logic; the steps normally appearing in the standard NMOS processes are marked. The processing steps are the same for both the JMOS and the conventional process until polysilicon-gate patterning is completed. Several implants then follow to form the drain structures. By suitable combinations of the masked implants, all drain structures, including the symmetrical JMOS and larger geometry JFETs, are fabricated side by side on the same chip. To implement both conventional n^+As and LDD-like transistors on the same chip, an additional As implant [arsenic (II)] was introduced into the process.

Major fabrication steps for the JMOS are described in Fig. 4.2. The polysilicon is heavily doped with a $POCl_3$ dopant source and then patterned with mask 4 (Table 4.1) to form the gate electrodes. The LDD process steps follow – first consisting of an n^- phosphorus masked implant. Mask 5 protects the source region

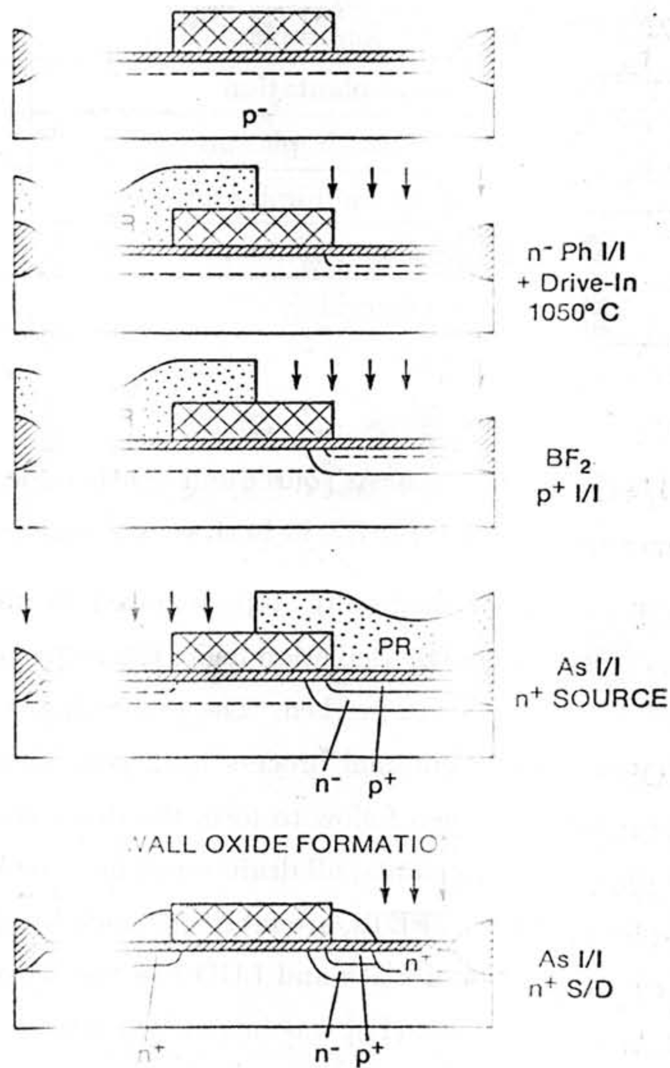


Figure 4.2: SEQUENCE O[illegible] ASKING AND THE I[illegible]PLANTS FOR THE FABRICATION OF SIX SOU[illegible] DRAIN STRUCTURES ON THE SAME CHIP.

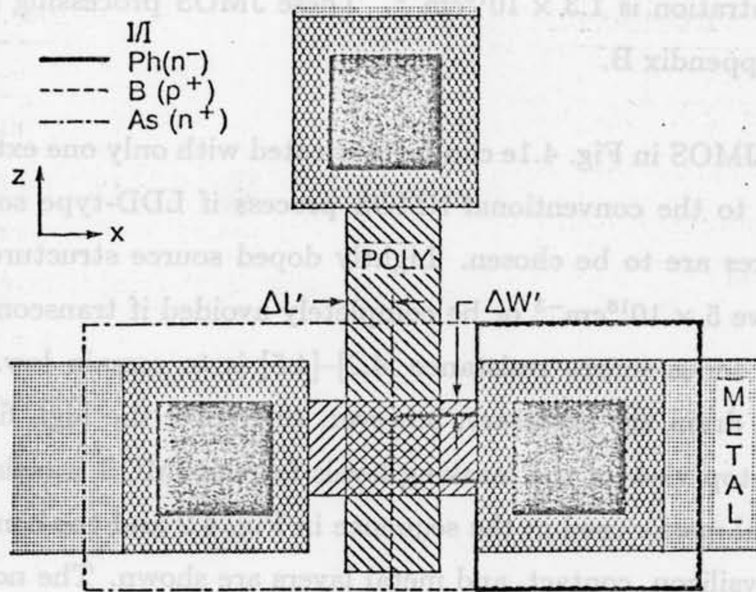


Figure 4.3: LAYOUT OF THE JMOS. DRAWN $W/L = 5/5$ μm.

of the asymmetric JMOS in addition to the other n^+As-only S/D regions of the structures in Fig. 4.1. The LDD n^- implant is then annealed at a high temperature (1050°C) for 60 min. A shallow 100 keV p^+ BF_2 implant follows to form the substrate-connected JFET gate on the JMOS devices. The 1050°C anneal ensures sufficient lateral diffusion of the n^- implant so that, in the annealing steps to follow the p^+ implant, the lateral diffusion of boron will not compromise the contact of the n^- region to the MOSFET channel. As described in Chapter 3, the two-dimensional process simulator SUPRA [4.1] assisted in the JMOS process design for the lateral diffusion of the diffused n^- and p^+ layers so that the merging of the JFET channel with the MOSFET surface channel region could be assured. Prior to sidewall oxide formation, a heavy n^+As masked implant forms the source junction of the JMOS. The sidewall oxide formation is the next step during which a furnace anneal for LPCVD oxide densification is done at 900°C for 30 min. After the sidewall oxide is

defined, an unmasked heavy n^{+}As implant forms the JMOS n^{+} drain followed by two 900°C anneals for a total time of 60 min. The final MOSFET channel region boron surface concentration is $1.3 \times 10^{16}\text{cm}^{-3}$. These JMOS processing steps are further detailed in Appendix B.

The asymmetric JMOS in Fig. 4.1e can be fabricated with only one extra masking step in addition to the conventional NMOS process if LDD-type source and JFET drain structures are to be chosen. Lightly doped source structures should either be doped above $5 \times 10^{18}\text{cm}^{-3}$ or be completely avoided if transconductance reduction caused by series source resistance [4.2]–[4.5] is to remain low. Lighter doping levels on the drain are necessary, however, to resolve the high field problem. Figure 4.3 is a top view of the masking levels for the JMOS transistor. The three nonconventional masks used in the sequence in Fig. 4.2 and the conventional n-MOS LOCOS, polysilicon, contact, and metal layers are shown. The nonconventional masks 5, 6, and 7 are aligned to the polysilicon mask and, in the channel-length direction, a $\Delta L'$ registration tolerance is allowable. The minimum tolerance is $\Delta L' = L_{gate}/2$ when the polysilicon gate has a minimum feature size. The characteristics of the JMOS are insensitive to the absolute value of the registration accuracy if the 3σ spread in the alignment process is less than half the minimum polysilicon linewidth. The n^{-} implant mask 5 is undersized by an amount $\Delta W'$ with respect to the drawn channel width in the LOCOS mask. This design rule was added to ensure electrical contact between the p^{+} JFET gate with the boron channel-stop implant in the channel-width direction. In conventional processes using LOCOS isolation, the actual channel width is smaller than that of the drawn channel because of field-oxide encroachment under the silicon-nitride mask during field oxidation. A reduction $\Delta W = W_{DRAWN} - W_{eff} = 0.9$ μm was measured in conventional MOSFETs built in the 2 μm process. As a result, the rule $\Delta W' = 0.75$ μm was adopted for the layout design so that it could accept 0.5 μm of field oxide encroachment on each side of the channel and also 0.25 μm n^{-} lateral diffusion. This lateral diffusion rule is tolerant to registration errors between the LOCOS mask and mask 5 because the the registration run-out in the z-direction enables a p^{+} JFET gate connection

Table 4.2: JMOS PROCESS PARAMETERS

Parameter	*Low* V_p	*Medium* V_p	*High* V_p	*Unit*
N^- phosphorus dose	2×10^{13}	5×10^{13}	7.5×10^{13}	cm^{-2}
Net N^- channel dose	4.2×10^{12}	9.8×10^{12}	1.4×10^{13}	cm^{-2}
P^{31} surface conc. (N_S)	8×10^{17}	2×10^{18}	3×10^{18}	cm^{-3}
P^+ BF_2 dose	6×10^{13}	1.5×10^{14}	2.2×10^{14}	cm^{-2}
N^- sheet resistance (ρ_s)	850	450	410	$\Omega/\square$
Pinched N^- ρ_s	5.8	1.7	1.2	$k\Omega/\square$
N^+ JMOS source ρ_s	34	34	34	$\Omega/\square$
N^+ JMOS drain ρ_s	61	110	68	$\Omega/\square$
N^+ polysilicon ρ_s	27	27	27	$\Omega/\square$
Oxide thickness (t_{ox})	400	400	400	Å
Sidewall width (L_{sw})	0.4	0.4	0.4	μm

to the substrate from at least one side of the channel.

The three n^- phosphorus implant doses used in the fabricated JMOS and the other relevant process parameters for the three designs here referred to as high, medium, and low V_p JMOS are summarized in Table 4.2. The implant dose parameters were chosen through one-dimensional SUPREM III process simulations to yield net n^- doses Q_{net} in the JFET channels in the 4 to 15 $\times 10^{12}$ cm^{-2} range. The low dose JMOS has a net phosphorus dose close to that of the low V_p JMOS simulated in Chapter 3 ($Q_{net} = 3.6 \times 10^{12}$ cm^{-2}, $V_{TJ} = -1.6$), and the medium and high V_p have a Q_{net} close to the optimal dose in conventional LDDs. The p^+ implant dose was also varied in each JMOS so that shallow p^+ junction could be formed. Simulated surface concentrations in the n^- region were $8 \times 10^{17} cm^{-3}$ for low V_p, $2 \times 10^{18} cm^{-3}$ for medium V_p, and $3 \times 10^{18} cm^{-3}$ for high V_p JFET after the 60 min 1050°C drive-in of the phosphorus implant. The sheet resistances measured in van der Pauw test structures built on the same chip for both the n^- and pinched n^- layers are listed in Table 4.2. The n^+ As sheet resistance ρ_s measured for the JMOS source layer is half of the ρ_s in the JMOS drain n^+ diffusion because the source

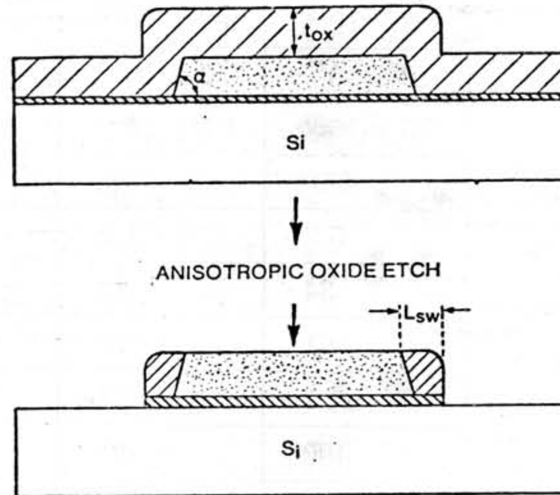


Figure 4.4: PROCESS STEPS IN THE SIDEWALL OXIDE DEFINITION.

layer is heavily implanted twice, as shown in the process sequence in Fig. 4.2.

The sidewall-spacer technology[1] [4.6,4.7] defines the LDD regions and is preferred over the polysilicon overetch [4.8] and polysilicon oxidation [4.9] because of its better controllability. The process sequence for sidewall oxide formation is shown in Fig. 4.4. A conformal oxide layer is deposited after polysilicon gate patterning. The oxide is then anisotropically etched down to the silicon surface, leaving a sidewall spacer having width L_{sw} as illustrated in Fig. 4.4. The critical process variables are the deposited oxide conformality and the anisotropic properties of both the polysilicon and oxide etchings. These variables must be determined for the equipment and process used. An ideally conformal oxide deposition should obtain the same film thickness over both planar horizontal and planar vertical ($\alpha = 90°$ in Fig. 4.4) surfaces. The C_2ClF_5:SF_6 plasma-etching process chosen for polysilicon patterning can produce nearly vertical polysilicon sidewalls if the polysilicon is undoped at the

[1] J. Riseman, U.S. Patent # 4234362, November 18, 1980

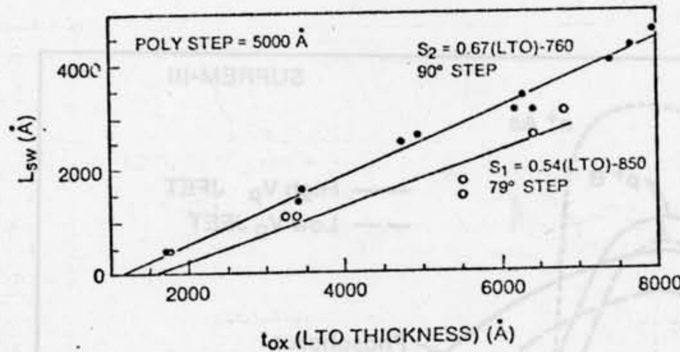


Figure 4.5: DEPENDENCE OF FINAL SIDEWALL-SPACER WIDTH ON INITIAL DEPOSITED OXIDE THICKNESS [4.10].

time of patterning. When patterned in the same process, heavily phosphorus-doped polysilicon yields sidewalls with slightly smaller slopes ($\alpha = 79°$). Figure 4.5 is a plot of the resulting sidewall-spacer width L_{sw}, measured by scanning electron microscopy, as a function of the deposited oxide thickness for the process used in the Stanford Integrated Circuits Laboratory [4.10]. Polysilicon thickness is 0.5 μm. In the undoped polysilicon ($\alpha = 90°$), L_{sw} is approximately 67 percent of the initial deposited oxide thickness over planar horizontal surfaces as a result of the non ideal conformality (less than 70 percent) of the LPCVD oxide deposition used. The final spacer width depends on the slope α of the polysilicon gate edge as illustrated in Fig. 4.5 for the heavily doped polysilicon gates. An approximately 10° deviation from the vertical walls resulted in the polysilicon etch. This deviation accounts for a 20 percent reduction in L_{sw} when compared to the vertical sidewalls. This reduction caused by the slope of the sidewalls is in agreement with the sidewall-spacer modeling of Tsang [4.7] who predicted a reduction of 17 percent in the final sidewall oxide width solely because of the slope of the polysilicon lines.

For the devices fabricated in the JMOS process, an 8000 Å LPCVD oxide was deposited, followed by a 30 min 900°Coxide densification and plasma etch. Final

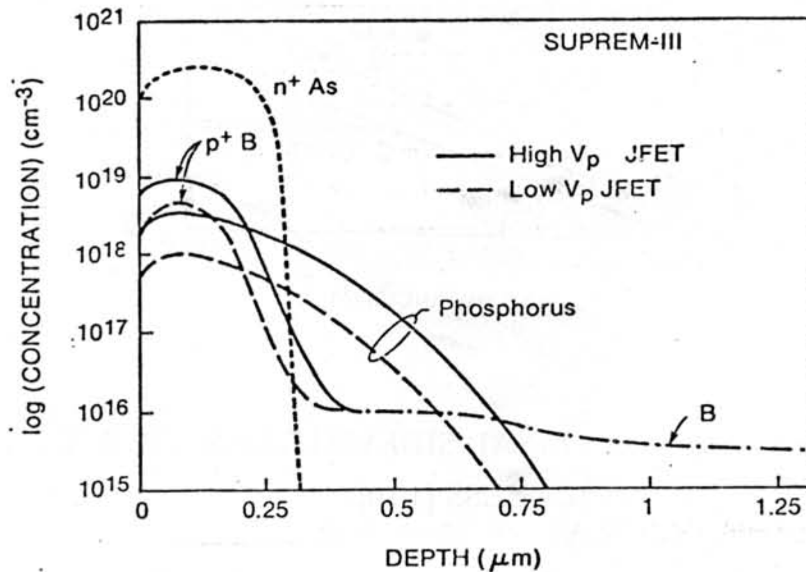


Figure 4.6: SUPREM SIMULATED IMPURITY PROFILES FOR HIGH AND LOW V_p JFET DESIGNS.

spacer widths of 4100 to 4600 Å were obtained, as measured by top-view SEMs of the actual devices during fabrication.

SUPREM-III simulated profiles after all anneals for the high and low V_p JFET designs, and for the n^+ As drain profile are shown in Fig. 4.6. The p^+ and n^- doping levels for the medium V_p design are in between the two designs illustrated in Fig. 4.6. The high-temperature anneal of the n^- implant resulted in fairly deep junctions, considering that shallow junctions of less than 3000 Å are normally used in VLSI MOS devices. The deepest $x_{j_{n^-}}$ junction for the high V_p is 0.7 μm(solid line in Fig. 4.7). The boron stopper in the JFET drain was not implemented. A 0.7 μm thick polysilicon electrode should be applied to mask the deep boron implant illustrated in Fig. 4.7 instead of the 0.42 μm polysilicon used in this process. The low V_p JMOS PISCES simulations in Chapter 3 indicated that the boron stopper can reduce the short channel effects (SCE) by constraining the drain-junction

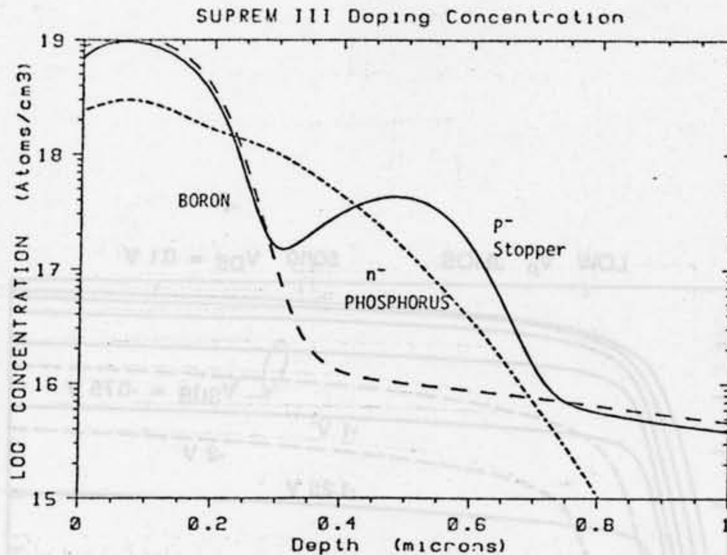


Figure 4.7: SUPREM SIMULATED IMPURITY PROFILES OF THE HIGH V_p JFET WITH (SOLID LINE) AND WITHOUT (– – –) A DEEP BORON-STOPPER IMPLANT OF 10^{13} cm^{-2} AND AN ENERGY OF 180keV.

field penetration in the lateral direction. A p^- boron stopper could reduce $x_{j_{n^-}}$ to 0.46 μm. Although its introduction in the process is advantageous in terms of reducing the SCE, the higher backgate dose in the JFET drain degrades ac performance because of the higher drain/substrate bottom junction capacitance. Additional drain/substrate junction capacitance was introduced in the JMOS through the sidewall p^+/n^+ junction.

4.3 Experimental Results and Comparisons

4.3.1 Device Characteristics

Figure 4.8 plots the measured $\log(I_{DS})$ – V_{GS} characteristics (solid lines) for a low V_p JMOS with W/L = 50/10 at V_{DS}= 0.1 V; both the JFET and MOSFET subthreshold regimes are illustrated. The drain current exhibits the expected ex-

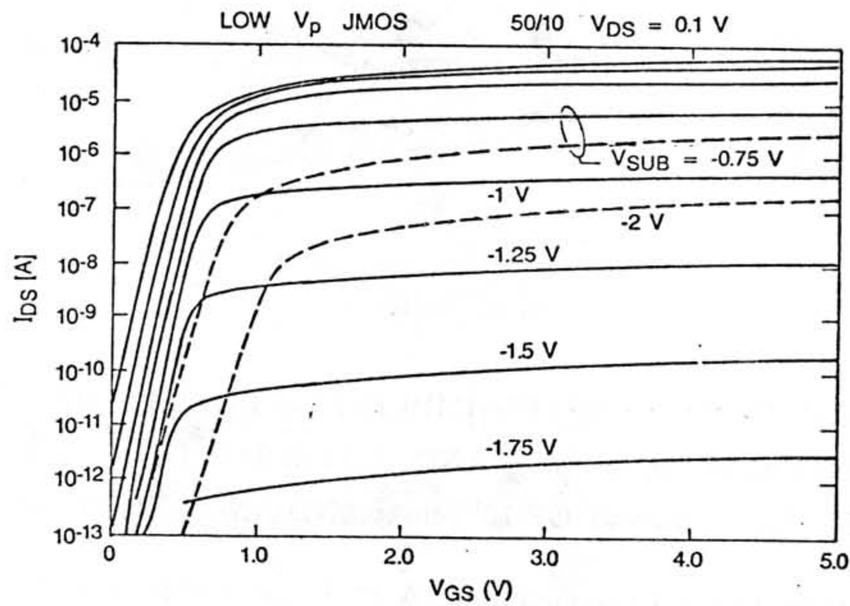


Figure 4.8: SUBTHRESHOLD CHARACTERISTICS FOR THE LOW V_p JMOSFET. Measured characteristics (solid line) at $(W/L) = (50/10)$, V_{DS}=0.1 V, V_{SUB} steps $\Delta V_{SUB} = -0.25\,V$ from 0 to $-1.75\,V$. Simulated subthreshold characteristics are denoted by the dashed lines.

Figure 4.9: EQUIVALENT CIRCUIT MODEL OF THE JMOS DEVICE. $V_{SUB} - V_{D_i}$ is the effective JFET gate-to-source voltage.

ponential turn-on [4.11] in the MOSFET subthreshold regime; however, because of the drain JFET gating action, the drain current can be turned off by setting $(V_{SUB} - V_{D_i}) < V_{T_J}$, as demonstrated in the circuit and device simulations described in Chapter 3. The flat characteristics in Fig. 4.8 indicate the exponential turn-off of the drain current by the substrate bias. The equivalent circuit in Fig. 4.9 shows that the gate-to-source voltage drive in the series JFET is $(V_{SUB} - V_{D_i})$ which is $\approx V_{SUB}$ for the MOSFET linear bias condition $V_{DS} \ll (V_{GS} - V_T)$ in the JFET subthreshold region in Fig. 4.8.

The long-channel zero backgate-bias MOSFET threshold voltage is $V_T = 0.32$ V, as extracted by TECAP2 [4.12] fitting of the measured conventional device linear region $I_{DS} - V_{GS}$ characteristics at several substrate biases. The linear region extrapolation of these characteristics at $V_{SUB} = 0$ V simulated with PISCES yielded $V_T = 0.38$ V. The 60 mV difference between the simulated and measured MOSFET threshold values is a result of an overestimation of V_T when linear extrapolation is used for the above-threshold characteristics. Fitting to the measured I-V characteristics yields the threshold voltage at the onset of inversion at the MOSFET virtual

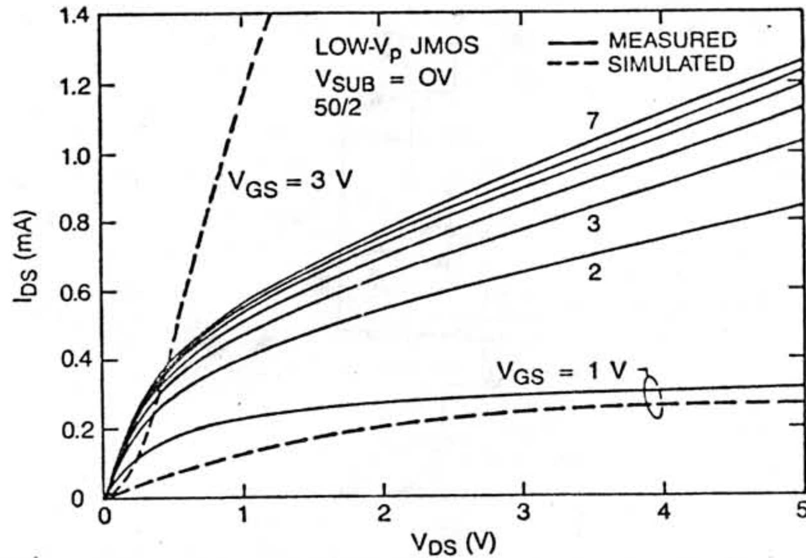


Figure 4.10: $I_{DS} - V_{DS}$ CHARACTERISTICS FOR THE LOW V_p DEVICE. Measured data (solid line) and PISCES simulated data (broken line) for the JMOS of Fig. 4.12. Drawn $(W/L) = (50/2)$. $(W/L_{eff}) = (50/1.3)$.

cathode, at which point the surface potential is a minimum and equal to $\psi_s = 2\phi_f$. Conventional MOSFET parameters obtained by curve fitting the conventional MOS device I–V characteristics are listed in Table A.1.

For this low V_p design, the measured JFET threshold voltage is $V_{T_J}= -(|V_p| - \phi_{bi})$ $= -0.8$ V. This V_{T_J} parameter was previoulsy defined as the substrate bias at which $I_{DS} = 0.1\,\mu A/\mu m$ at $V_{GS}= 5$ V and $V_{DS} = 0.1$ V. The PISCES two-dimensional device simulation for this low V_p predicts $V_{T_J} = -0.5$ V. The PISCES-simulated subthreshold device characteristics for low V_p with an $L_{eff} = 1.3$ and $W = 50$ μm are plotted in Fig. 4.8 for comparison (dashed lines). The measured subthreshold behavior of the JMOS in the JFET subthreshold region is in qualitative agreement with the simulations. The rates of JMOSFET turn-off, however, differ greatly; the PISCES-simulated JFET turn-off with substrate bias is much slower (1.1 V/decade at V_{GS}=5 V) than the measured rate (0.17 V/decade) for low drain bias. The simu-

lated and measured values are in better agreement for the MOSFET subthreshold slope (108 and 90 mV/decade, respectively, at $V_{SUB} = 0$ V). The measured V_{T_J} is in disagreement with the one-dimensional SUPREM electrical simulation of pinched n^- sheet conductivity; SUPREM predicts $V_{T_J} = -6.5$ V if V_{T_J} is assumed to be the value at which the n^- pinched-layer sheet conductance is 1 percent of its value at zero substrate bias.

The extent of the disagreement between the simulated and measured characteristics of the low V_p JMOS can be seen in Fig. 4.10 where the measured I-V (solid line) and the simulated PISCES results for $V_{GS}= 1$ V and 3 V (dashed line) are shown. This low V_p JMOS has a 2 μm drawn channel length, measured $L_{eff} = 1.3$ μm, and $t_{ox} = 393$ Å. For low gate bias ($V_{GS}= 1$ V), the simulated current is approximately 17 percent smaller than the measured current. Agreement will improve if the mobility-reduction parameter β_e in the longitudinal field-dependent mobility equation used in PISCES

$$\mu_{eff}(E) = \mu_o \left[\frac{1}{1 + \left(\frac{\mu_o E}{v_{max}}\right)^{\beta_e}} \right]^{1/\beta_e} \tag{4.1}$$

is adjusted to a value higher than 1. In the simulation in Fig. 4.10, $\beta_e = 1$ and the low-field surface mobility for electrons is $\mu_o = 665\,\text{cm}^2/\text{Vsec}$. The measured mobility-reduction parameters are presented in Appendix A.

The lack of agreement between the simulated and measured values in Fig. 4.10 at $V_{GS}= 3$ V can only be explained by the inaccuracy of the two-dimensional profiles input to the device simulator. In the measured data the JFET pinch-off effect is apparent in the low drain bias subthreshold characteristics in Fig. 4.8 and in the above-threshold saturation characteristics in Fig. 4.10. The low V_p simulations revealed that a smaller $V_{T_J} = -0.5$ V has two consequences in terms of the electrical characteristics. First, it leads to weaker substrate voltage control over current flow in the JFET subthreshold at low drain bias, as indicated by the poor turn-off rate (1.1 V/decade) in Fig. 4.8 (dashed lines). Second, the JFET channel cannot be pinched off at large V_{DS}, even for drain bias above $V_{SUB} - V_{T_J}$, as demonstrated by the simulated curve for $V_{GS}= 3$ V in Fig. 4.10. Sizable control of the drain bias over

the subthreshold characteristics of the simulated low V_p JMOS confirmed the short channel behavior of the device. The drain voltage is sufficient, therefore, to punch through the lightly doped JFET channel region, and the more adequate series device model for the n^- region is a space-charge region for current drift. Transport through this region, as simulated in Fig. 4.10 (broken line), is nonlinear at low drain bias ($V_{DS} < 0.5\,\text{V}$) because current transport through the n^- region shifts from high-resistance ohmic behavior for $V_{DS} \ll V_{SUB} - V_{TJ}$ to a space-charge-limited regime for larger drain biases. In this regime, no JFET-induced current saturation can occur, as indicated by the simulated data in Fig. 4.10.

The disagreement between the simulated results and measurements in Fig. 4.10 are related, therefore, to a lighter dose predicted in the one-dimensional process simulation or to the inaccurate estimation of the two-dimensional distributions of n^- and p^+ impurities. The PISCES results were obtained from the one-dimensional low V_p impurity profile in Fig. 4.6 extended analytically to the lateral dimension. Two-dimensional implantation and diffusion models and simulators will yield better agreement between measurement and simulation. The electrical characteristics of the low V_p JMOS are sensitive to the two-dimensional distribution of the n^- and p^+ diffusions in Fig. 4.11. Simple cylindrical aproximations to this distribution may not reflect the physical diffusion effects present in the JMOS two-dimensional channel.

As the low V_p two-dimensional device simulations in Chapter 3 indicated, a low V_p JMOS can exhibit considerable JFET short-channel effects, as is apparent in Fig. 4.10 where the measured output conductance of the saturated JMOS at large V_{GS} bias is the result of the drain potential punching through the JFET channel. This can be explained by the fact that most of the applied drain bias drops along the short length of the n^- region at large V_{GS}. Given the low doping in the channel of the low V_p JFET, this punchthrough is to be expected. The JFET channel length can be estimated as

$$L_J \simeq L_{sw} - \left(f_1 x_{j_{n+}} - f_2 x_{j_{p+}}\right) \tag{4.2}$$

where the lateral junction depths in Fig. 4.11 are a fraction f_1 and f_2 of the vertical junction depths of the n^+ and p^+ diffused layers, respectively. As discussed in Chap-

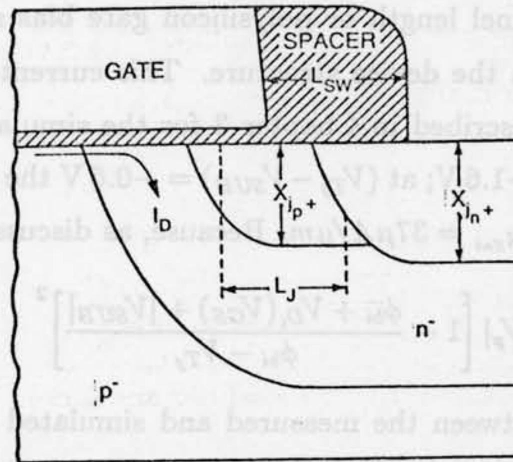


Figure 4.11: CROSS SECTION OF THE JFET DRAIN REGION.

ter 3, simulation results obtained from the analytical models of SUPRA indicated that f_1 is in the 0.4 to 0.5 range because the boron concentration at the JFET surface is higher than the background p^- concentration in the n^+/p^- source junction and that $f_2 \simeq 0.6$. The JMOS technology ensures that $x_{j_{n^+}} > x_{j_{p^+}}$ as shown in Fig. 4.6; otherwise, an n-p-n bipolar transistor would impede current flow out of the JMOS drain. Based on SUPREM estimates of $x_{j_{n^+}}$ and $x_{j_{p^+}}$ for the devices herein reported, the correction factor inside the parenthesis in Eq.(4.2) should be less than 800 Åso that the JFET channel length L_J is in the range of 0.3 to 0.4 μm. Because L_J is less than twice the p^+ and n^+ junction depths, the JFET-controlled current path in the drain region is highly two-dimensional as indicated in the geometry of the n^- region in Fig. 4.11. This geometry assigns a two-dimensional character to the electrical effective JFET channel length and pinchoff voltage.

The measured data in Fig. 4.10 are in qualitative agreement with the simulations of the low V_p device discussed in Chapter 3. At large V_{GS}, the JMOS drain current saturates as a result of the limitation of the pinched-off JFET current capability. The JFET pinchoff current I_p reaches a maximum $I_{p_{max}}$ experimentally determined for devices with $L_{gate} = 2$ μm. At $V_{SUB} = 0$ V and $V_{GS} = V_{DS} = 5$ V,

this saturated JMOSFET I_{DS} is $I_p = 24\mu A/\mu m$ and is virtually independent of the intrinsic MOSFET channel length or polysilicon gate bias so that the JFET acts like a current limiter in the device structure. This current-limiting action is qualitatively the same as described in Chapter 3 for the simulated low V_p device with t_{ox}= 200 Å and $V_{T_J} = -1.6$ V; at $(V_{T_J} - V_{SUB}) = -0.6$ V the PISCES result for this low V_p JMOSFET is $I_{DS_{Sat}} = 37\mu A/\mu m$. Because, as discussed in Chapter 3,

$$\frac{I_p}{W_J} \propto |V_p| \left[1 - \frac{\phi_{bi} + V_{D_i}(V_{GS}) + |V_{SUB}|}{\phi_{bi} - V_{T_J}}\right]^2 \tag{4.3}$$

the 50 percent difference between the measured and simulated I_p reflects mostly the 50 percent higher $|V_p|$ (2.6 V) for the low V_p device simulated in Chapter 3 than for the experimental $|V_p| \simeq 1.6$ V of the fabricated low V_p device. Both structures have similar Q_{net}, and the sidewall length is 500 Å shorter in the simulation. The structural differences (thinner gate oxide, higher substrate doping for the simulated device) do not have as strong impact on the maximum drive in the low V_p JMOS design as the JFET pinchoff voltage and n^- net impurity dose in the JFET channel.

A $W/L = 50/2$ low V_p JMOS is compared to a conventional MOSFET of the same drawn gate length in Fig. 4.12. The JMOS effective channel length is ≈0.2 μm shorter than the measured length of its conventional counterpart on the same chip. The low V_p JMOS characteristics (dashed lines) show the reduced current-drive capability caused by the introduction of the drain JFET with low pinchoff voltage. Comparing these two devices, the maximum current drive in the JMOS device at $V_{GS} = V_{DS} = 5$ V is observed to be comparable to the current drive in a conventional device at $V_{GS} = V_{DS} = 1$ V. The comparison is based on the shortest MOSFET channel length used in a 2 μm (minimum rule) technology for which the impact of the series JFET in terms of the current-drive capability is the greatest. The degree of current limiting by the JFET in the low V_p design implemented in the experiment is more than would be desired in an actual VLSI application. Its characteristics are shown here to illustrate the JFET action as the two active devices are merged into a single LDD-like drain structure.

Figure 4.13 plots the effect of JFET saturation on the measured transconduc-

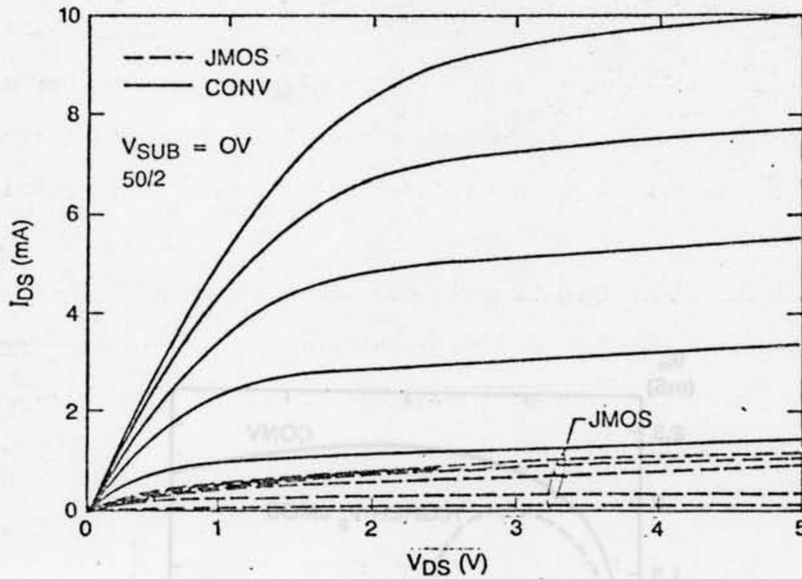


Figure 4.12: COMPARISON OF MEASURED $I_{DS} - V_{DS}$ CHARACTERISTICS OF A LOW V_p AND A CONVENTIONAL DEVICE. Both have the same drawn $(W/L) = (50/2)$.

tance of short-channel JMOS transistors by comparing their transconductance/gate-voltage characteristics to those in the conventional MOS transistor. The transconductance of devices with the same drawn channel length is measured in saturation at $V_{DS} = 6$ V. The low V_p JMOS has an n^- channel region of high sheet resistance ($\simeq 5.8\,k\Omega/\square$ measured value) and, therefore, a low pinchoff current. Saturated transconductance reaches a maximum at low V_{GS} and drops at higher V_{GS}. At increased gate voltages, JMOS transconductance is negligible which reflects the saturation of the drain JFET and its current-limiting characteristics. In the medium V_p JMOS design with a measured n^- sheet resistance of $\simeq 1.7\,k\Omega/\square$, the current-carrying capability of the drain JFET increases and transconductance is maximum at larger V_{GS}. Its saturated transconductance at V_{GS}= 5 V is still approximately half of the conventional device transconductance for the same channel geometry, as illustrated in Fig. 4.13. The effect of reduced transconductance on the I-V charac-

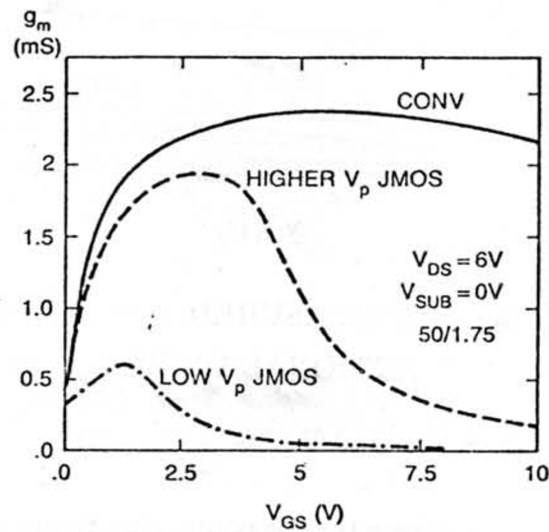


Figure 4.13: COMPARISON OF SATURATION REGION TRANSCONDUCTANCE AT $V_{DS} = 6\,V$ IN TWO JMOS DESIGNS AND A CONVENTIONAL DEVICE. Low V_p (_ . _) and medium V_p (– – –) design. Devices have the same drawn $(W/L) = (50/1.75)$.

teristics of a medium V_p structure with a drawn channel length of 2 μm can be seen in Fig. 4.14, where the medium V_p I-V is compared to that of a conventional device of same drawn channel length. For gate voltages up to 3 V, both have approximately the same current-drive capability.

Velocity saturation in micron-sized transistors is responsible for transconductance saturation in the conventional device at large drain bias. This phenomenon has an important impact on VLSI performance. The g_m–V_{GS} curve for the conventional device with L_{eff} = 1.25 μm (solid line in Fig. 4.13) deviates considerably from the first-order linear dependence on $V_{GS}-V_T$ at gate voltages as low as 1 V and reaches a maximum at V_{GS} = 5 V. The theoretical limit for MOSFET saturated transconductance is

$$g_{m_{SAT}} = W_{eff} C_{ox} \langle v \rangle \sim \frac{20}{t_{ox}(\text{Å})} \ (\text{mS}/\mu m) \tag{4.4}$$

where the average carrier velocity in the channel $\langle v \rangle$ is $\approx 6 \times 10^6$ cm/sec and t_{ox} is measured in angstroms. For correctly designed VLSI MOS transistors, the longitudinal fields along the current path must be low enough compared to the gate-induced fields to maintain long-channel behavior. Under normal operating conditions, therefore, the average saturated velocity limit in Eq.(4.4) seldom reaches the bulk scattering-limited velocity, because the channel carriers are not accelerated by fields with an intensity larger than the critical field E_{CRIT} for velocity saturation over the entire channel length. In the channel end closer to the drain, the field intensities under saturation bias are much larger than E_{CRIT} and rapidly fall off toward the source end. Measurements of g_m in a deep submicron device (L_{DRAWN} = 0.75 μm, L_{eff} = 0.3 ± 0.1 μm) saturated at V_{DS} = 5 V yielded $\langle v \rangle = 7 \times 10^6$ cm/sec for a measured saturated transconductance of 61 μS/μm width. Such a device, however, exhibits considerable short-channel effects as a result of the lateral encroachment of the drain field under the MOSFET channel because the 2 μm 400 Å technology is not properly scaled for submicron effective channel lengths. The saturation transconductance in a correctly scaled conventional device with L_{eff} = 1.25 μm (solid line in Fig. 4.13) reaches close to the limit of 2.5 mS predicted in Eq.(4.4) before beginning to decrease at large gate bias because of the effect of

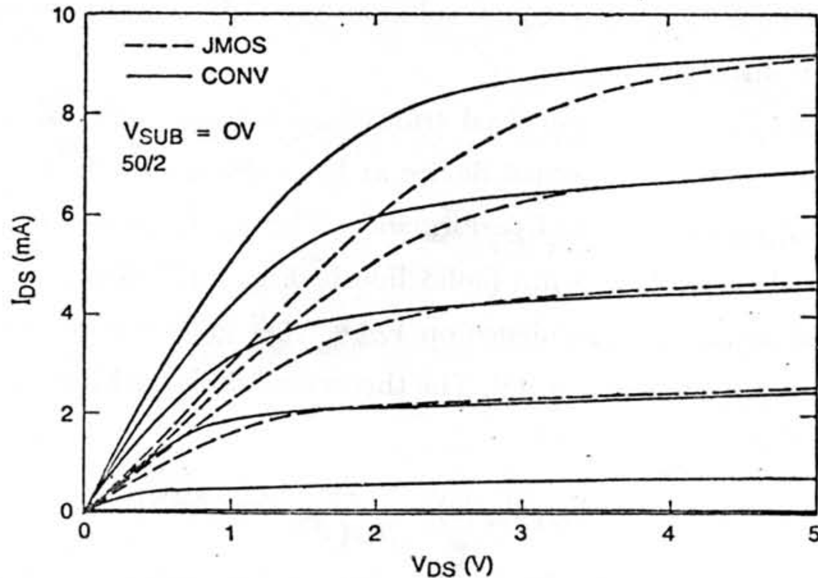


Figure 4.14: COMPARISON OF MEASURED $I_{DS} - V_{DS}$ CHARACTERISTICS FOR A MEDIUM V_p JMOSFET AND CONVENTIONAL DEVICE. Both have the same drawn $(W/L) = (50/2)$.

series source resistance at larger drain currents.

The $I_{DS} - V_{DS}$ characteristics of a high V_p JMOSFET are compared in Fig. 4.15 to those of its conventional counterpart on the same chip. The medium and high V_p JMOSFETs have $I_{p_{max}} = 200$ and $320\ \mu A/\mu m$ width, respectively. This maximum pinchoff current is measured at large V_{GS} bias ($V_{GS} = 12$ V, $V_{DS} = 5$ V) where JMOSFET transconductance becomes negligible as the JFET current-carrying limit is reached by pinning the JFET gate-to-source drive at a value $[V_{SUB} - V_{D_i}(V_{GS}, L_{eff})]$. In the high V_p design in Fig. 4.15, $I_{p_{max}}$ is larger than the best-case $200\,\mu A/\mu m$ current-drive capability of the conventional enhancement-mode n-MOS devices built with a 400 Å gate oxide, 2 μm technology, and operating at 5 V. This current drive was measured in a conventional device with a 1.5 μm effective channel length and biased at V_{GS}=V_{DS}=5 V. For large V_{DS} bias in a short-channel MOSFET, the JMOSFET saturation-current limit is determined by the velocity saturation of the

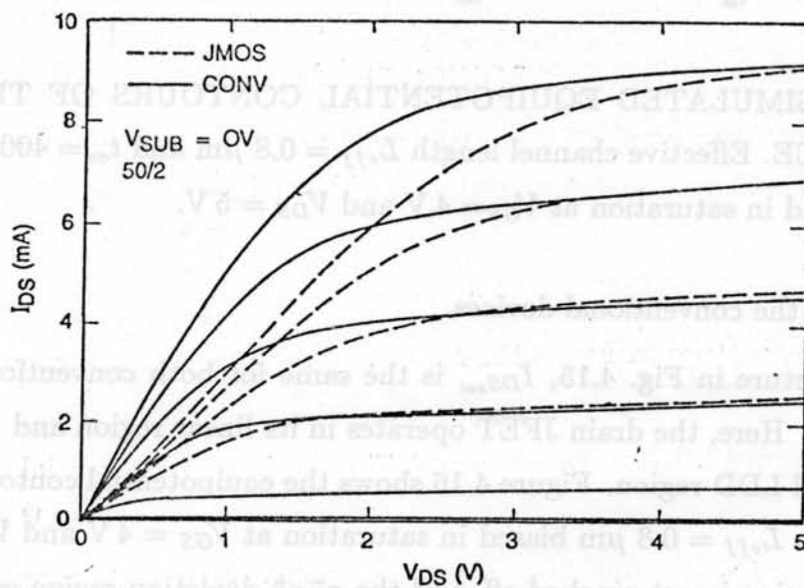


Figure 4.15: COMPARISON OF MEASURED $I_{DS} - V_{DS}$ CHARACTERISTICS FOR THE HIGH V_p JMOSFET AND CONVENTIONAL DEVICE. Both have the same drawn $(W/L) = (50/2)$.

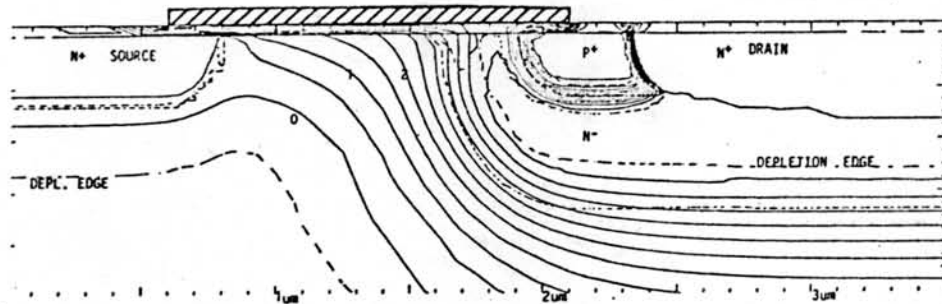


Figure 4.16: PISCES-SIMULATED EQUIPOTENTIAL CONTOURS OF THE HIGH V_p JMOS DEVICE. Effective channel length $L_{eff} = 0.8$ μm and t_{ox}= 400 Å. The JMOSFET is biased in saturation at V_{GS}= 4 V and V_{DS} = 5 V.

inversion carriers, as in the conventional devices.

In the high V_p structure in Fig. 4.15, $I_{DS_{sat}}$ is the same for both conventional and JMOSFET devices. Here, the drain JFET operates in its linear region and the device serves as a buried LDD region. Figure 4.16 shows the equipotential contours of a high V_p device with $L_{eff} = 0.8$ μm biased in saturation at V_{GS} = 4 V and V_{DS} = 5 V. The JFET n^- region is not pinched off, and the n^-p^+ depletion-region edge extends onto the surface under the MOSFET gate. Current saturation is the result of velocity saturation in the MOSFET channel as it is in conventional micron-sized devices. The considerable series-resistance contribution of the cylindrical portion of the JFET channel is indicated by the thinning of the neutral region in the lateral n^- region.

In Fig. 4.17, the simulated I-V characteristics in a high V_p JMOSFET with L_{DRAWN} = 1.5 μm are compared to those measured in a high V_p JMOSFET of the same drawn channel length. In the low drain-bias region, where the series JFET resistance most strongly affects the current drive, the simulated I-V underestimates the current by as much as 50 percent. In the saturation region where the current-limiting effect is the velocity saturation in the MOSFET channel region, the

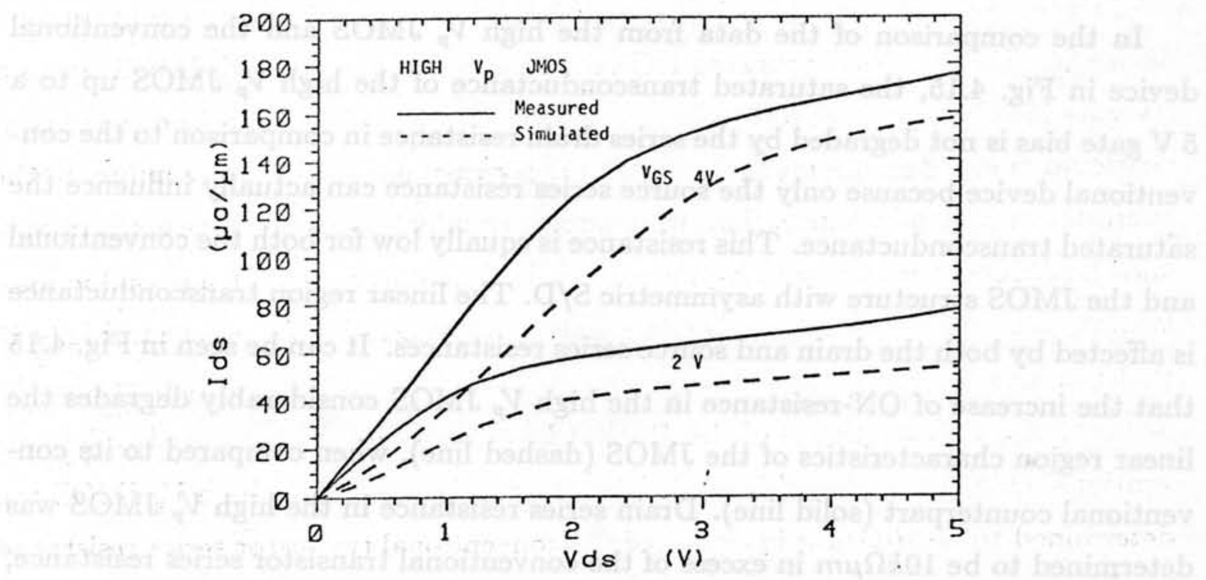


Figure 4.17: COMPARISON OF MEASURED (SOLID LINES) AND SIMULATED (DASHED LINES) I-V CHARACTERISTICS OF A HIGH V_p DEVICE WITH $L_{DRAWN} = 1.5\mu m$.

disagreement between simulated and measured data is somewhat less; they agree on the value of saturated transconductance for high drain bias which is insensitive to the actual JFET profile when device current saturation is related to carrier velocity saturation. The comparison indicates that the actual n^- doping profile in the two-dimensional JFET region is higher than that used in the simulation. A lighter n^- dose increases the linear region ON-resistance of the buried LDD region, as the simulated data indicate in the low drain-bias region in Fig. 4.17.

In the comparison of the data from the high V_p JMOS and the conventional device in Fig. 4.15, the saturated transconductance of the high V_p JMOS up to a 5 V gate bias is not degraded by the series drain resistance in comparison to the conventional device because only the source series resistance can actually influence the saturated transconductance. This resistance is equally low for both the conventional and the JMOS structure with asymmetric S/D. The linear region transconductance is affected by both the drain and source series resistances. It can be seen in Fig. 4.15 that the increase of ON-resistance in the high V_p JMOS considerably degrades the linear region characteristics of the JMOS (dashed line), when compared to its conventional counterpart (solid line). Drain series resistance in the high V_p JMOS was determined to be $10k\Omega\mu m$ in excess of the conventional transistor series resistance, by using the measurement procedure of Suciu [4.13]. In the simulated device in Fig. 4.17, such series resistance is much higher ($35k\Omega\mu m$) and, as a result of this discrepancy, the simulated current drive is lower than in the experimental high V_p JMOS. The measured sheet resistance of large-geometry n^- pinched resistors in the high V_p process is $1.2\,k\Omega/\square$, as shown in Table 4.2. For an estimated JFET length of 0.4 μm, the total calculated series resistance is approximately $\rho_s L_J = 480\,\Omega\mu m$. It can be concluded, therefore, that the n^- buried LDD contribution to the series drain resistance does not account for the series resistance increase in Fig. 4.15. The major contribution to ON-resistance originates in the lateral n^- region.

To probe further into the effect of the series JFET both the JMOS and JFET-MOSFET devices with mask-defined JFET channel lengths were fabricated on the same chip, using mask 8 (Table 4.1) to define the JFET length with the arsenic

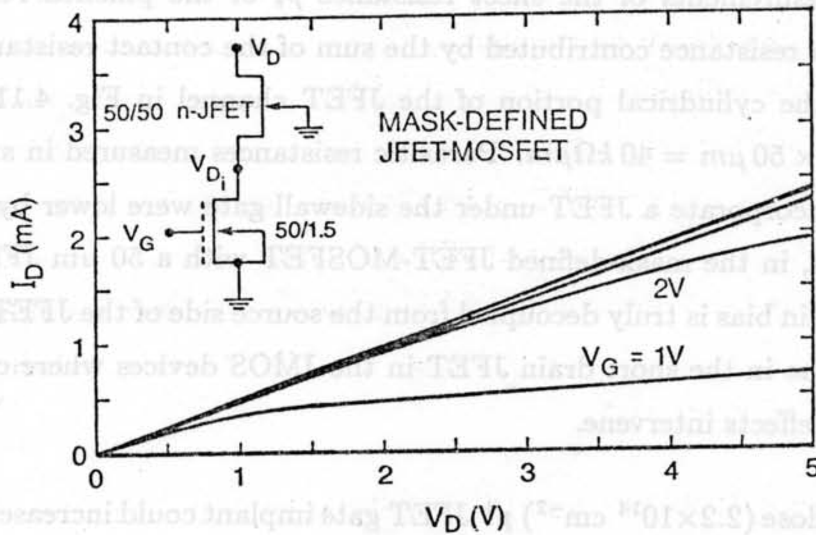


Figure 4.18: I-V CHARACTERISTICS OF A MASK DEFINED JFET-MOSFET. Drawn geometric ratios in the insert are in microns; MOSFET V_{GS} steps from 0 to 5 V, $\Delta V_{GS} = 1$ V.

(II) n^+ implantation. The length L_J for the mask-defined JFET-MOSFET is not determined by self-alignment to the sidewall edge, as illustrated in Fig. 4.11, but is set by mask layout. In other respects, the sidewall merging of the JFET and MOSFET is identical in these test devices and in the self-aligned JMOS. The I-V characteristics for a mask-defined JFET-MOSFET are shown in Fig. 4.18 where its equivalent circuit, biased at $V_{SUB} = 0$ V, appears in the insert. The mask-defined JFET has a long $L_J = 50$ μm, and the MOSFET drawn gate length is 1.5 μm; both have the same channel width. At high V_{GS}, the output resistance saturates at $R_J + R_M$, where the MOSFET equivalent resistance $R_M \approx 140\,\Omega$ was estimated from measurements in a conventional MOSFET with $L = 1.5$ μm on the same chip. The resistance attributable to the square (50/50) high V_p JFET was extracted from the I-V characteristics in Fig. 4.18 as $R_J = \left(\partial V_D / \partial I_D|_{V_{GS} \gg V_T}\right) - R_M \approx 2k\Omega$. Because the output conductance of the mask-defined JFET-MOSFET is constant at

$V_{GS} \gg V_T$, the long square JFET contribution to the mask-defined JFET-MOSFET output resistance is approximately the value of its measured ρ_s. Based on van der Pauw measurements of the sheet resistance ρ_s of the pinched resistors, the parasitic series resistance contributed by the sum of the contact resistance and the resistance of the cylindrical portion of the JFET channel in Fig. 4.11 can be as high as $800\,\Omega \times 50\,\mu m = 40\,k\Omega\mu m$. Parasitic resistances measured in small JMOS devices that incorporate a JFET under the sidewall gate were lower by a factor of 4 to 5 because, in the mask-defined JFET-MOSFET with a 50 μm JFET channel length, the drain bias is truly decoupled from the source side of the JFET. This does not occur in the in the short drain JFET in the JMOS devices where considerable short-channel effects intervene.

The high-dose (2.2×10^{14} cm^{-2}) p^+ JFET gate implant could increase series resistance beyond that of the pinched n^- series JFET through two possible mechanisms. First, a higher compensation of the n^- region in the lateral direction increases the series resistance; such an increase due to the cylindrical portion of the series JFET (Fig. 4.11) cannot be accounted for in the n^- ρ_s measurements in large-geometry test structures. In this region, the n^- doping could be lighter than predicted by the one-dimensional or two-dimensional SUPRA diffusion models. Two-dimensional diffusion effects that occur during the 900°C anneals that follow the p^+ implant could lead to overcompensation of the JFET n^- cylindrical channel region. The second possible mechanism to explain the high JMOS series resistance in the high V_p case is the increase of the contact resistance of aluminum(1%Si) metallization to the n^+ drain diffused layer. The n^+ arsenic-drain is implanted after the p^+ region so as to compensate the p^+ boron doping and to form the conventional low-resistance drain diffusion. The simulated SUPREM profile for this JFET drain, after compensation through n^+ As ion implantation, is shown in Fig. 4.6. The high-dose boron diffusion is only 1000 Å shallower than the As n^+ diffusion. The actual mechanism by which the metal contacts to this double-implanted layer could be degraded is not known. Most of the devices, even conventional n^+ As drain MOSFETs, fabricated in the high V_p JMOS experiment had higher contact resistance than devices from wafers

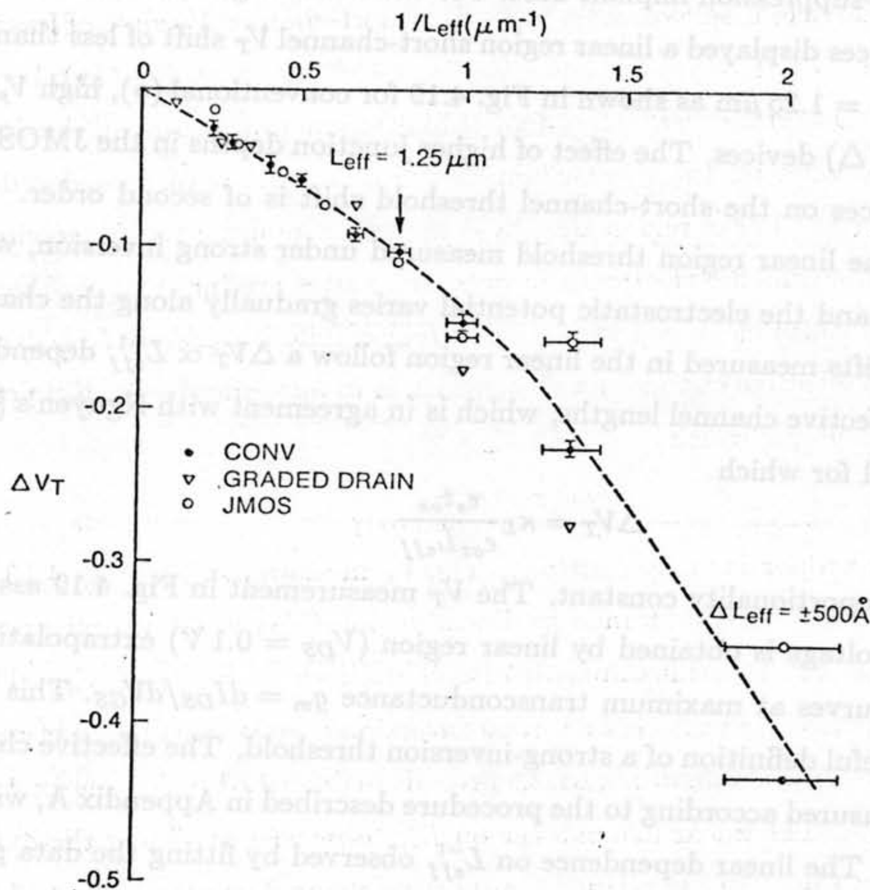


Figure 4.19: LINEAR REGION THRESHOLD SHIFT AS A FUNCTION OF EFFECTIVE CHANNEL LENGTH. V_T extrapolation measurement at V_{DS}=100 mV.

in the low V_p experiment.

The 1050°C n^- drive-in step results in a fairly deep n^- junction in the high V_p structure ($\approx 0.7\mu m$ based on the simulation results in Fig. 4.6). Considerable diffusion of the channel implants for V_T adjustment and punchthrough suppression also occurs. Scaling indicates that the S/D junction depths should be as shallow as technologically possible and provided that the diffused-region series resistance is held under acceptable limits. A JMOS optimized for technologies with $L_{eff} < 1\mu m$ must use shallower junctions. The threshold-voltage shift in the short-channel regime, in turn, should be controlled by an appropriate choice of oxide thickness

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and punchtrough-suppression implant dose. For the technologies chosen in this experiment, all devices displayed a linear region short-channel V_T shift of less than 100 mV down to $L_{eff} = 1.25\,\mu$m as shown in Fig. 4.19 for conventional (•), high V_p (o), and graded S/D (△) devices. The effect of higher junction depths in the JMOS and graded S/D devices on the short-channel threshold shift is of second order. This is expected for the linear region threshold measured under strong inversion, where drain bias is low and the electrostatic potential varies gradually along the channel. The threshold shifts measured in the linear region follow a $\Delta V_T \propto L_{eff}^{-1}$ dependence down to 1 μm effective channel lengths, which is in agreement with Nguyen's [4.14] theoretical model for which

$$\Delta V_T = \kappa_L \frac{\epsilon_s t_{ox}}{\epsilon_{ox} L_{eff}} \tag{4.5}$$

where κ_L is a proportionality constant. The V_T measurement in Fig. 4.19 assumes that threshold voltage is obtained by linear region ($V_{DS} = 0.1\,\text{V}$) extrapolation of the $I_{DS} - V_{GS}$ curves at maximum transconductance $g_m = dI_{DS}/dV_{GS}$. This is an arbitrary but useful definition of a strong-inversion threshold. The effective channel lengths were measured according to the procedure described in Appendix A, with an error of ± 500 Å. The linear dependence on L_{eff}^{-1} observed by fitting the data points (dashed line in Fig. 4.19) is verified for effective channel lengths down to 1 μm. For shorter lengths, the encroachment of the built-in source and drain fields accounts for the greatly reduced threshold voltage. In this region, V_T becomes very sensitive to L_{eff}, thereby resulting in a larger spread of the threshold-voltage distribution.

4.3.2 Substrate Current

Figure. 4.20 compares the log(I_{SUB}) vs V_{GS} characteristics of a conventional and a low V_p JMOSFET (same device as in Fig. 4.12), both with drawn $W/L = 50/1.5$. The normal substrate current characteristics [4.15] are observed in the conventional MOSFET. Its bell-like shape indicates that the substrate current is mostly the result of holes generated by impact ionization occurring as carriers traverse the high-field region under the gate in the drain end of the device. The JMOSFET substrate current is almost independent of gate voltage, is not triggered by channel

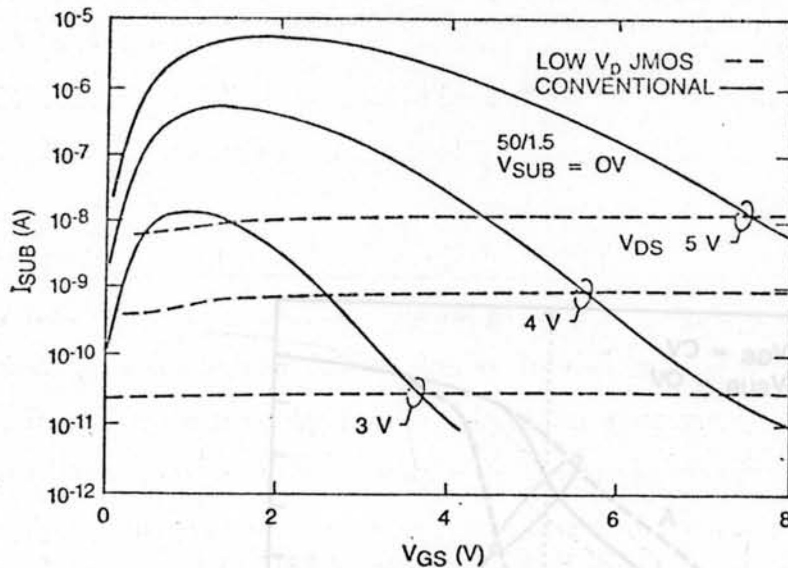

Figure 4.20: SUBSTRATE CURRENT VS V_{GS} IN CONVENTIONAL (SOLID LINE) AND LOW V_p JMOS (DASHED LINE) at V_{DS}=3,4,5 V. Drawn (W/L) = (50/1.5) in both devices. Low V_p L_{eff} = 0.8 μm and conventional L_{eff} = 1.0 μm.

current, and is more than 2 orders of magnitude lower than the peak value of I_{SUB} in the conventional device. Except for the bias regime in which the conventional MOSFET is well into its linear mode of operation ($V_{GS}>V_{DS}$, where the inversion layer extends from source to drain n^+ regions and reduces the longitudinal field strength in the drain end of the channel), the JMOS I_{SUB} is less than the impact ionization substrate current in the conventional MOSFET.

Drain diodes fabricated on the same chip with different area/perimeter ratios confirmed that the JMOS substrate current in Fig. 4.20 is predominantly p^+/n^+ sidewall diode leakage. Because the drain–substrate leakage is fairly independent of channel current, it is independent of polysilicon gate length and MOSFET gate bias and scales with device width to a typical room temperature value of $\sim$300 pA/μm at a drain-to-substrate bias V_{DB} = 5 V. In JMOS designs with higher n^- and p^+

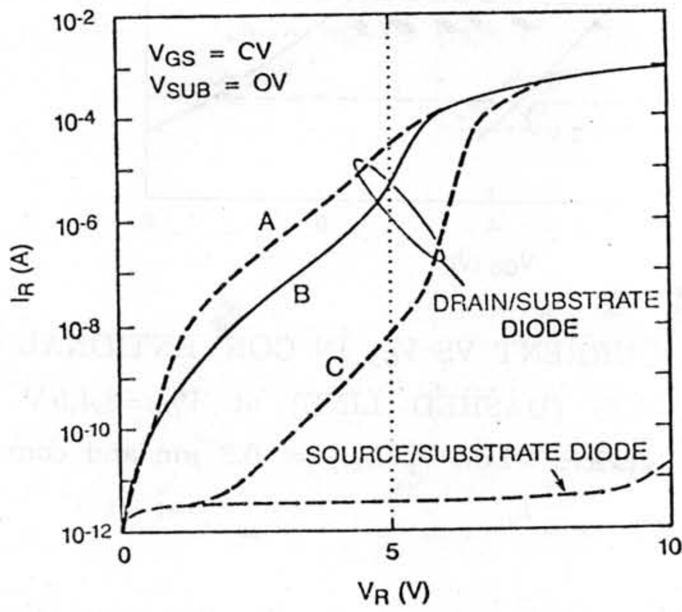

Figure 4.21: COMPARISON OF REVERSE CHARACTERISTICS OF SOURCE/DRAIN DIODES IN JMOS DEVICES. Drain diodes of high, medium, and low V_p devices are indicated by curves A, B, and C, respectively. The JMOS is in the MOSFET subthreshold regime. Channel width is 50 μm.

doping densities, zener leakage under the same conditions can increase by orders of magnitude when tunneling becomes important and can reach a typical maximum of $\sim 500\,\mathrm{nA}/\mu\mathrm{m}$ when both sides of the sidewall junction are degenerately doped. Figure 4.21 compares the n^+/substrate leakage of the diode on the source side of the high V_p JMOS with no sidewall n^+/p^+ junction and of the diode on the drain-JFET side of the high V_p JMOS (curve A), both in the same transistor structure. All transistors have a 50 μm channel width. The sidewall junction increases the leakage by many orders of magnitude and, in the drain end, it leads to the "soft" leakage characteristics of low reverse biases in the three JMOS designs studied (curves A, B, and C) caused by the field emission of carriers in the high fields of heavily doped junctions. High sensitivity to p^+ doping levels are expected in shallow n^+(arsenic)/p(boron) junctions with p-doping levels above $10^{18}\mathrm{cm}^{-3}$ [4.16]. Curve A in Fig. 4.21 denotes the drain diode of the high V_p JMOS with the highest p^+ doping level, and curves B and C represent the JMOS with medium and low V_p, respectively. These measurements confirm the sensitivity of the leakage current to p^+ doping and verify that an optimal JMOS design must pay particular attention to the p^+ doping profile if substrate current is to be minimized.

The impact of the p^+/n^+sidewall junction in the drain breakdown voltage of micron-sized JMOS devices is illustrated in Fig. 4.22. In the conventional device (dashed line) with a 0.5 μm effective channel length, the drain breaks down at V_{DB} =7.5 V and, in the high V_p device with the same L_{eff}, the breakdown occurs at V_{DB} = 6 V. There is considerable punchthrough current in the conventional device beyond 6 V because of its short channel. Drain-induced barrier lowering in both short-channel devices is indicated by the drain output conductance at V_{GS}= 0 ,−1 V. The JMOS has a more characteristic junction breakdown as a result of the p^+/n^+ sidewall junction. True junction breakdown in MOSFETs is indicated by sharp "knees" at the drain breakdown voltage V_{BD} and by the slight increase in V_{BD} with V_{GS} caused by the spreading of the drain fields in the pinchoff region as the gate voltage increases.

Device simulations with GEMINI and SUPRA profiles predicted sidewall-junction

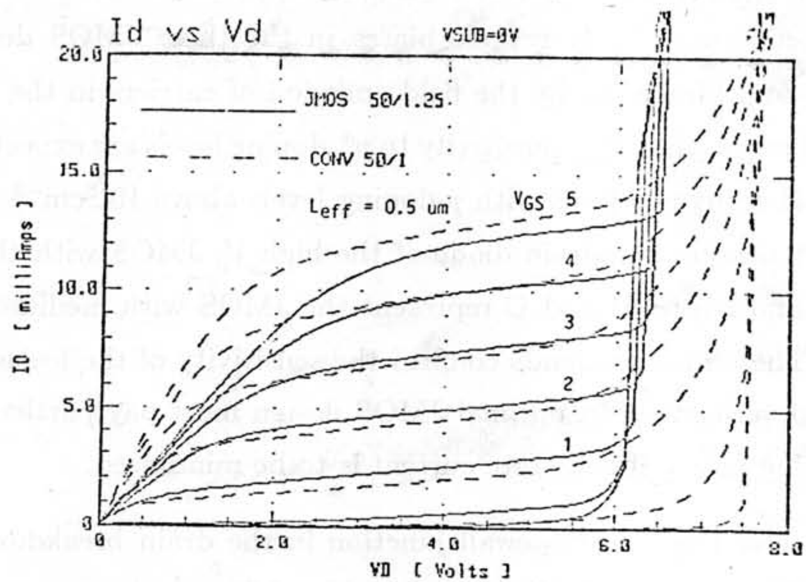

Figure 4.22: DRAIN BREAKDOWN CHARACTERISTICS IN CONVENTIONAL AND HIGH V_p JMOS. Devices with $L_{eff} = 0.5\mu$m; The V_{GS} steps are from -1 to 5 V.

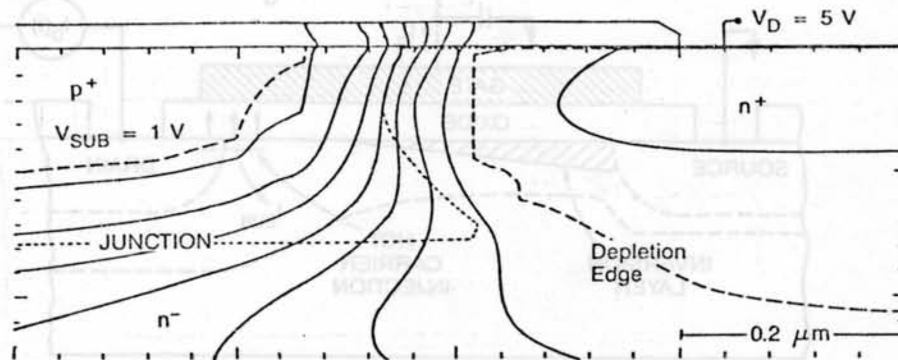

Figure 4.23: GEMINI SIMULATED EQUIPOTENTIAL CONTOURS AT THE n^+ DRAIN TO p^+ SUBSTRATE SIDEWALL JUNCTION AT BREAKDOWN.

breakdown at 6 V, which is in close agreement with the experimental results. The equipotential contours (solid lines) at the sidewall junction under breakdown bias ($V_{GS} = 0$ V, $V_{DS} = 5$ V, $V_{SUB} = -1$ V) are shown in Fig. 4.23. Field intensities in excess of 600kV/cm leading to breakdown develop in the n^+ drain to p^+ substrate sidewall junction.

4.3.3 Gate Current

Very sensitive gate current measurements were obtained at the wafer level by utilizing a floating-gate-induced drain-current relaxation technique [4.17] as illustrated in Fig. 4.24. The MOSFET is probed and biased. At time $t = 0$, the gate probe is lifted which leaves the gate electrode floating. The decay of the source-drain current with time is monitored by the amperemeter while the drain bias is held constant. The typical I_D decay with time in Fig. 4.25 indicates the discharge of the gate-electrode capacitance. Applying this technique, the hot-carrier-induced current collected at the gate electrode can be measured. When the electron current

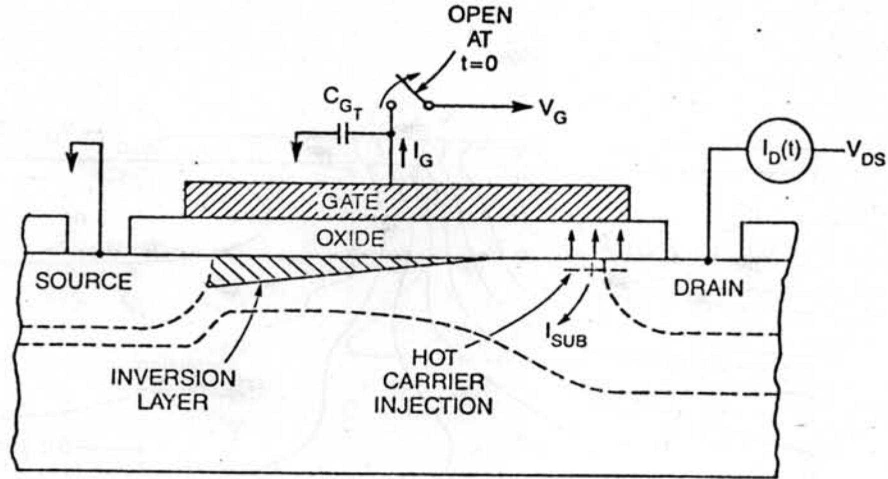

Figure 4.24: SETUP FOR THE FLOATING -GATE INDUCED DRAIN CURRENT RELAXATION MEASUREMENT. Lifting the gate probe opens the switch, and $I_D(t)$ is monitored.

originating in the high-field region in the drain is collected at the floating gate, the drain current decays with time. Hot-hole gate current has also been measured in a conventional n-MOS biased at low V_{GS} just above threshold [4.18,4.19]; in this case $I_D(t)$ actually increases instead of decaying as illustrated in Fig. 4.25.

The relation

$$I_G = C_{G_T}\frac{dV_G}{dt} = C_{G_T}\frac{dV_G}{dI_D}\frac{dI_D}{dt} \tag{4.6}$$

enables the determination of $I_G(t)$ from the decay $I_D(t)$ at any given V_{DS} bias after the functional dependencies $C_{G_T}(V_G)$ and $I_{DS}(V_{GS})|_{V_{DS}}$ are measured; here, C_{G_T} is the total capacitance on the gate electrode. The characteristics $I_{DS}(V_{GS})|_{V_{DS}}$ in a conventional device with $W/L_{eff} = 50/1.5$ are plotted in Fig. 4.26. In small transistors, the total capacitance of the gate electrode is

$$C_{G_T}(V_G) = C_{GATE} + C_p \simeq C_{G_o} \tag{4.7}$$

where C_{GATE} is the MOSFET polysilicon-gate capacitance and C_p is the parasitic capacitance of the gate electrode, consisting of the pad and the wiring capacitance.

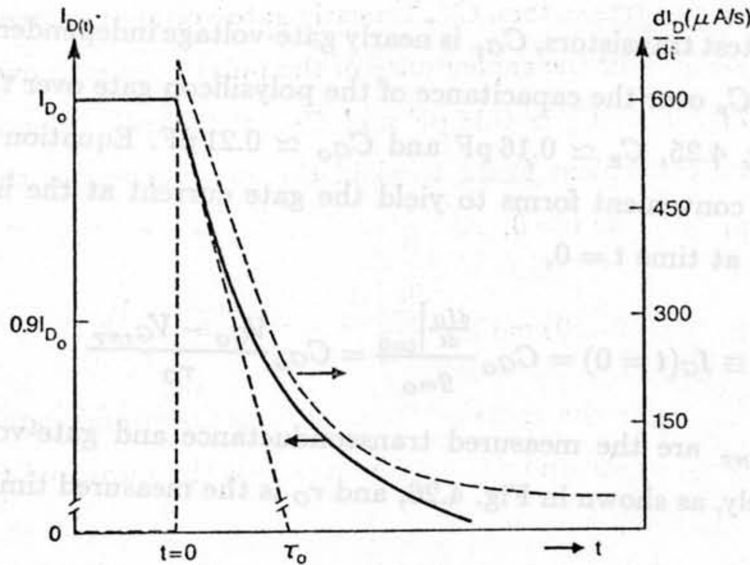

Figure 4.25: TYPICAL DRAIN CURRENT DECAY AFTER THE GATE ELECTRODE IS LEFT FLOATING.

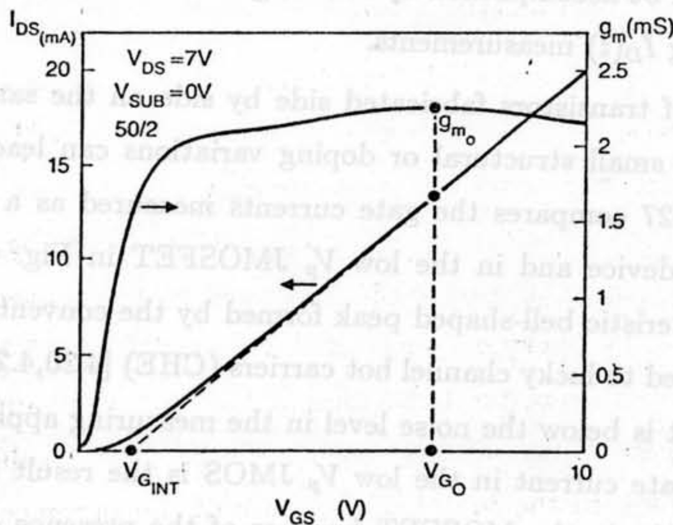

Figure 4.26: DRAIN CURRENT AND TRANSCONDUCTANCE DEPENDENCE ON V_{GS}. These characteristics were measured to obtain the value of g_{mo} used to estimate the gate current $I_G(t=0)$.

In the short-channel test transistors, C_{G_T} is nearly gate-voltage independent because of the dominance of C_p over the capacitance of the polysilicon gate over thin oxide. In the device in Fig. 4.25, $C_p \simeq 0.16\,\text{pF}$ and $C_{G_O} \simeq 0.21\,\text{pF}$. Equation (4.6) can be rewritten in two convenient forms to yield the gate current at the initial bias condition (V_{DS},V_{G_O}) at time $t = 0$,

$$I_{G_O} \equiv I_G(t=0) = C_{G_O} \frac{\left.\frac{dI_D}{dt}\right|_{t=0}}{g_{m_O}} = C_{G_O} \frac{V_{G_O} - V_{G_{INT}}}{\tau_O} \tag{4.8}$$

where g_{m_O} and $V_{G_{INT}}$ are the measured transconductance and gate-voltage axis intercept, respectively, as shown in Fig. 4.26, and τ_O is the measured time constant in Fig. 4.25.

Resolution below $10^{-18}A$ is possible with this technique if C_{G_O} is kept small and the slow drain-current decay rates can be measured down to 10^{-9} A/sec. To measure the low drain-current decay rates, even small variations in the contact resistance over several minutes must be minimized in the probe-to-wafer source and drain contacts. This can be accomplished by reducing the mechanical vibrations in the probe station during $I_D(t)$ measurements.

The gate currents of transistors fabricated side by side on the same chip are compared here because small structural or doping variations can lead to invalid comparisons. Figure 4.27 compares the gate currents measured as a function of V_{GS} in a conventional device and in the low V_p JMOSFET in Fig. 4.12 on the same chip. The characteristic bell-shaped peak formed by the conventional device curve has been attributed to lucky channel hot carriers (CHE) [4.20,4.21] while the JMOSFET gate current is below the noise level in the measuring apparatus. This extreme reduction in gate current in the low V_p JMOS is the result of the lower internal drain voltage V_{D_i} in the MOSFET because of the presence of the series JFET even though the external V_{DS} was 7 V in this measurement. In Fig. 4.27, the gate current in the graded S/D device on the same chip is an indication of reduced impact ionization caused by drain profile grading only. The drop in JMOSFET gate current is clearly the result of a lower V_{D_i} in addition to junction grading. This is consistent with the I–V characteristics in Fig. 4.12 and the substrate current

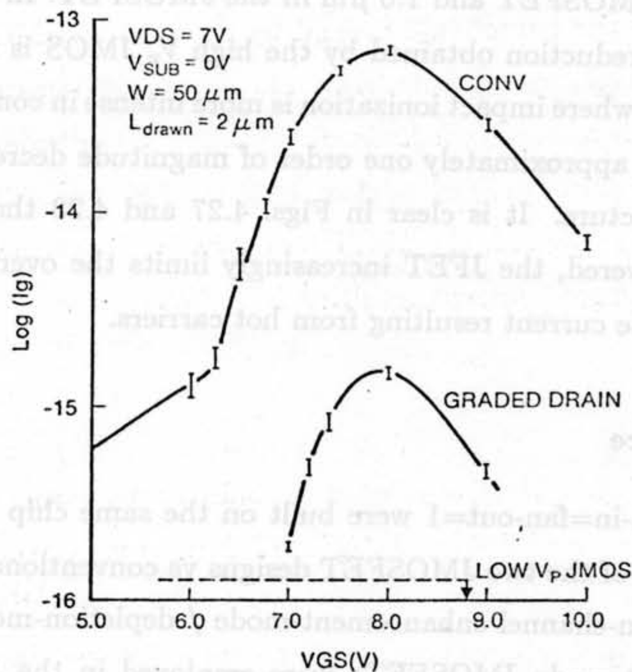

Figure 4.27: GATE CURRENT VS V_{GS} IN CONVENTIONAL AND LOW V_p DEVICES. Both have drawn (W/L) = (50/2). Conventional L_{eff} = 1.5 μm, JMOS L_{eff} = 1.3 μm; V_{DS}=7 V and V_{SUB} = 0 V. The graded S/D device with L_{eff} = 1.1 μm is also shown.

characteristics in Fig. 4.20; both of which indicated that the JFET drain supported most of the drain bias and that impact ionization was negligible under the gate of the low V_p JMOSFET, respectively.

Figure 4.28 compared the gate currents of devices on the same chip of a high V_p wafer measured at V_{DS}= 6 V. This drain bias is a few hundred mV lower than V_{BD} in the high V_p transistor, as indicated in Fig. 4.22. Effective channel lengths are 1.25 μm in the conventional MOSFET and 1.0 μm in the JMOSFET. In the CHE I_G peak (at $V_{GS} \simeq V_{DS}$) the reduction obtained by the high V_p JMOS is relatively small. At lower gate voltages where impact ionization is more intense in conventional devices, however, there is an approximately one order of magnitude decrease in I_G measured in the JMOS structure. It is clear in Figs. 4.27 and 4.28 that, as the JFET pinchoff voltage is lowered, the JFET increasingly limits the overall device current but improves the gate current resulting from hot carriers.

4.3.4 Speed Performance

Ring oscillators with fan-in=fan-out=1 were built on the same chip to benchmark the speed performance of the two JMOSFET designs vs conventional devices. The 21 inverter stages were n-channel enhancement-mode / depletion-mode types. Depletion- and enhancement-mode JMOSFETs were employed in the JMOS inverter stages. All ring oscillators had the same drawn geometries (12/3 drivers, 8/8 loads). Figure 4.29 plots the oscillation period as a function of supply voltage in two wafers. The speed performance of the low V_p design (dashed line) is much degraded compared to the speed of the conventional device (□). This degradation is expected because the drive capability of the JMOS inverter stage is severely limited by the low V_p drain JFET as demonstrated in Fig. 4.12.

The speed of the high V_p JMOS ring oscillator (solid line) is comparable to the conventional design on the same chip (o). The slight speed-up of this JMOSFET is solely attributable to the smaller L_{eff} of the transistors ($\approx$ 0.25 μm shorter) and is within the wafer-to-wafer variation of the speed performance of conventional devices; wafers in the low V_p experiment had better contact resistance than those

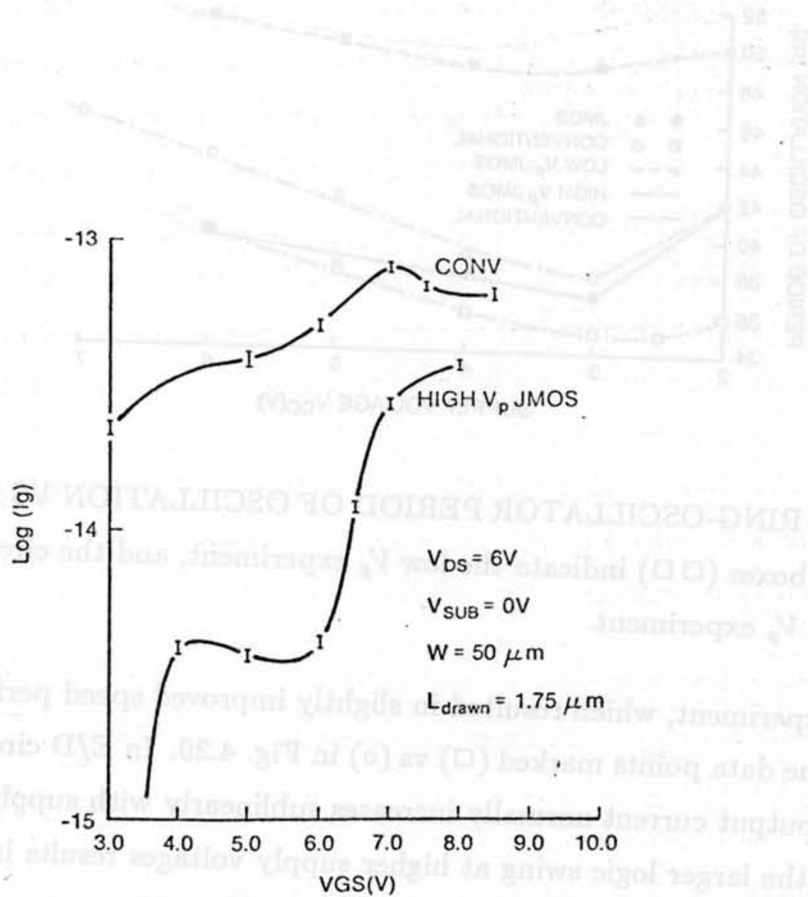

Figure 4.28: GATE CURRENT VS V_{GS} IN CONVENTIONAL AND HIGH V_p DEVICES. Both have drawn $(W/L) = (50/1.75)$. Conventional $L_{eff} = 1.2\,\mu m$, JMOS $L_{eff} = 1.0\,\mu m$; V_{DS}=6 V and $V_{SUB} = 0$ V.

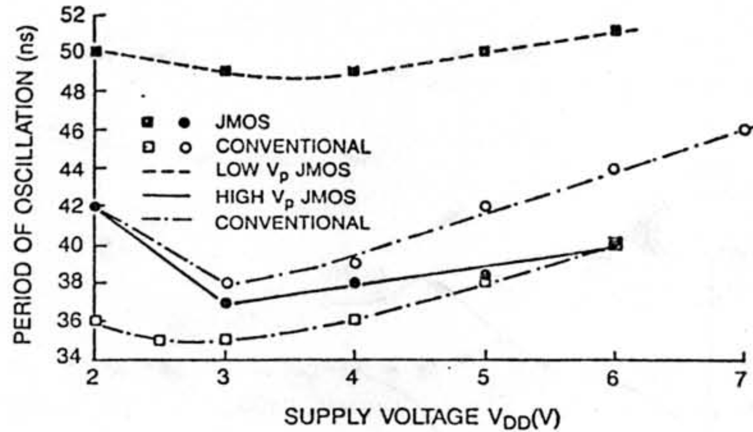

Figure 4.29: E/D RING-OSCILLATOR PERIOD OF OSCILLATION VS SUPPLY VOLTAGE. The boxes (□ □) indicate the low V_p experiment, and the circles (○ ●) indicate the high V_p experiment.

in the high V_p experiment, which resulted in slightly improved speed performance, as indicated in the data points marked (□) vs (○) in Fig. 4.29. In E/D circuits, the average pull-up output current normally increases sublinearly with supply voltage. For this reason, the larger logic swing at higher supply voltages results in a slower ring-oscillator speed as V_{DD} increases as illustrated in Fig. 4.29.

The introduction of the p^+ region in the JMOSFET drain has the positive effect of reducing the gate-to-n^+-drain feedback capacitance C_{GD} but at the expense of increasing both drain-to-substrate junction capacitance C_{DB} and gate-to-p^+ overlap/fringing capacitance C_{GSUB}.

4.4 JMOS Structure Evaluation

The JMOS structures studied have demonstrated the basic advantages of this design. First, the maximum effective MOSFET drain bias can be set, independent of the maximum externally applied drain and gate bias that can be set at effectively higher voltages. This property is advantageous because of the pressing need, caused

by hot carrier effects, for voltage reduction in conventional submicron MOSFETs. Second, the JMOSFET lightly doped drain region can be engineered without the normal reliability constraint imposed on conventional LDDFETs because of hot carrier injection under the sidewall; reliable LDDFETs require $N_S > 10^{18}\text{cm}^{-3}$ in the n^- region, and the buried n^- region in the JMOSFET can be more lightly doped to meet the designer's choice of JFET V_p. Third, the advantages of channel longitudinal field reduction by drain junction grading are common to all LDD structures; they are also common to the JMOSFET plus the additional advantage of driving the channel current away from the Si/SiO_2 interface in the high-field drain region. These three features also further minimize charge injection, trapping, and instabilities associated with the gate oxide. Based on the proven correlation between gate and substrate currents and device reliability in both conventional and LDD devices, submicron JMOSFETs are expected to have good endurance under hot carrier stress.

The implementations of the JMOSFET device have revealed other areas that require further improvement so as to address the detrimental effects of a shallow p^+ implant in the drain n^- region. First, the breakdown voltage of the sidewall $n^+ p^+$ junction at 6.5 V and the associated junction leakage observed at 5 V make drain-to-substrate leakage unacceptable for dynamic circuit applications. A phosphorus n^+ region self-aligned to the sidewall oxide or a slight ($\approx 0.2\mu m$) anisotropic silicon etch-back prior to arsenic n^+ implant to grade or eliminate the $n^+ p^+$ sidewall junction are possible technology implementations that could resolve this problem. The alternative of a silicon etch-back to remove the p^+ diffusion after sidewall formation also prevents other potential problems caused by the compensation of the p^+ BF_2 implanted layer on the resistance of the metal to the n^+ drain contact. Second, a symmetrical JMOSFET is negatively affected by a further reduction of effective transconductance resulting from an increase in series source resistance R_S because

$$g_{m_{sym}} = \frac{g_{m_J}}{1 + g_{m_J} R_S} \tag{4.9}$$

where g_{m_J} and $g_{m_{sym}}$ are the JMOSFET and symmetrical JMOSFET effective

transconductances, respectively. This implies that an additional mask is required to eliminate the p^+ region on the source side. Third, process complexity and control are relevant factors in the comparison of the JMOSFET and more conventional designs. A self-aligned active device under the oxide spacer that controls the current drive of the JMOSFET makes oxide spacer process control even more necessary. Cross-sectional scanning electron microscopy is not a pratical process monitor, and test structures have been developed only recently to monitor electrically the effective sidewall-spacer width [4.22]. The addition of at least one extra masking step with worst-case alignment tolerance of $L_{gate}/2$ is another drawback of the JMOSFET in its asymmetric implementation.

4.5 Summary

The JMOSFET, a modified LDD structure, has been successfully implemented and experimentally demonstrated. It provides device designers with performance tradeoffs somewhat different than earlier LDD devices. The comparison of measured and simulated results revealed that the critical parameter in optimizing the JMOS is the doping profile of the drain JFET region. Although low V_p devices with light n^- dose show poorer dc and ac performance, they substantially reduce the high-field-related currents. Experimental higher V_p JMOS devices share the advantages of the LDDFETs in terms of junction grading, and they also bury the drain current away from the Si/SiO_2 interface. By constraining the longitudinal E-field peak away from the SiO_2/Si interface, the JMOSFET minimizes hot carrier injection into the oxide (evident in the gate and substrate current characteristics) and should reduce also the reliability problems associated with that injection.

The JMOS can be optimized for a given minimum effective channel length, oxide thickness, and supply voltage. It resolves some of the reliability problems in LDD devices with peak doping densities below $1 \times 10^{18} cm^{-3}$ related to injection into the sidewall oxide.

The results indicate that, with optimization of the drain JFET, this new device can perform well in VLSI applications and can maintain its hot-carrier-resistant

properties in submicron 5 V supply circuits. An improved JMOS structure should address the need for a shallower JFET and for the elimination of the sidewall substrate leakage. As in all LDD structures, improved device reliability has been achieved but at some expense in performance. There are advantages in maintaining 5 V operation in micron-sized devices, however, and the advantages of CV scaling can then outweigh this performance loss.

Chapter 5

JMOSFET Optimization

5.1 Overview

The experimental results described in Chapter 4 demonstrated that the JMOSFET minimizes hot carrier injection into the oxide. The earlier experimental devices proved that the JMOSFET can be designed to virtually eliminate gate current at a substantial cost in performance or to moderately reduce it at a minimal cost, compared to similarly fabricated conventional devices. It is important, therefore, that the JMOSFET be designed for the most favorable trade-off between reliability and performance for any given scaled technology and supply voltage. This chapter introduces methods developed to maximize the benefits of the drain voltage-limiting properties and performance of JMOSFETs as they are scaled to submicron channel lengths.

5.2 Optimization Methodology

The first step in the optimization procedure is the selection of MOSFET parameters in accordance with known constant-voltage scaling principles. The technology constraints normally imposed on VLSI MOSFETs to ensure their correct long-channel behavior are taken into account. The second step is to design the JMOS in such a way as to optimize its reliability and performance for the gate oxide thickness, minimum gate length, and supply voltage selected in the first step. As indicated by the experimental and simulation results, the two basic dc indicators of JMOS

performance are its saturated-current capability and its linear region ON-resistance. The two parameters to be optimized are the JFET V_p and the pinchoff current I_{p_o}; they are dependent on the impurity profile $N(y)$ in the JFET channel, the side-wall oxide length, and the two-dimensional distribution of impurities in the lateral portion of the JFET. The reliability of MOSFETs is strongly correlated to the maximum electric field strength in the current path of channel carriers in the vicinity of the Si/SiO_2 interface; the field strengths in excesss of $100k$V/cm are proportional to $(V_{DS} - V_{DS_{Sat}})$ in saturated MOSFETs. Based on these empirical findings, the purpose of optimization is to reduce the electric fields close to the MOSFET drain by limiting its effective drain bias V_{D_i} at a small cost in performance.

This second step in the optimization process has two points of departure. First, the one-dimensional JFET profile is optimized by determining the maximum current capability for a given V_p. Second, the one-dimensional profile that yields good JFET characteristics must be tested in two-dimensional device simulations to verify the effect of the two-dimensional distribution of the n^- profile on the current capability and ON-resistance of the JMOS.

5.3 Scaling of MOSFET Parameters

The MOSFET parameters must be scaled appropriately to satisfy the requirement of long-channel behavior for devices with a minimum effective channel length; These parameters are t_{ox}, N_{SUB}, and x_j. In the JMOS, the drain $n^- p^-$ junction is deeper than the source junction. The maximum n^- junction depth must be a fraction f_J of the minimum effective channel length to minimize two-dimensional field effects; that is,

$$x_{j_{n^-}} \leq f_J L_{min} \tag{5.1}$$

The practical values for f_J in VLSI devices range from 0.1 to 0.5. The n^- junction depths in the experimental JMOS discussed in Chapter 4 are particularly deep because of the 1050°C n^- phosphorus drive-in step. The requirement for a p^+ JFET gate on top of the lightly doped n^- region in the JMOS drain leads to

deeper $x_{j_{n-}}$ than those in conventional LDDFETs. Creating shallow p^+ junctions is difficult with conventional implant and furnace-anneal technologies and, for this reason, f_J in JMOS devices ranges from 0.4 to 0.5. The experimental data for short channel threshold shifts and effective channel lengths measured in Chapter 4 yielded $f_J = 0.53$ for the deepest junction (high V_p design). Heavily doped shallow p^+ and n^+ junctions where $x_j < 0.1$ μm and with device-worthy sheet resistance and leakage properties can be achieved with rapid thermal annealing or with more recently developed techniques such as laser doping [5.1,5.2]. These techniques could reduce considerably the f_J parameter in the JMOSFETs

The maximum gate oxide thickness should be a fraction of the bulk depletion-region depth in the virtual-cathode plane of the device under strong inversion, and this depth depends on the effective channel length, channel doping, S/D depletion-region width, and the depth of the S/D junctions. As a result, the maximum V_{SB} and V_{DB} biases, substrate doping, junction depth, and oxide thickness must be established at any given scaling generation to ensure long-channel behavior. The empirical scaling rule of Brews [5.3] presented in Chapter 2 sets the minimum effective channel length as a function of the technology-driven parameters at

$$L_{min} = A\left[x_j t_{ox}(d_{js} + d_{jd})^2\right]^{1/3} \qquad (5.2)$$

This relationship was empirically fitted to simulated and measured data in conventional MOSFETs. The definition of acceptable short-channel behavior is somewhat arbitrary; in Eq. (5.2) its principal definition is the $I_{DS} - V_{GS}$ shift in the subthreshold characteristics. Using a less stringent definition of L_{min} below which short-channel behavior is unacceptable, the empirical constant A was recalculated. Based on the linear region $\Delta V_T = 100\,\text{mV}$ criterium instead of the subthreshold current-shift criterion, $A = 0.25\,\text{Å}^{-1/3}$ fits the data point $L_{min} = 1.25$ μm, $t_{ox} = 395\,\text{Å}$, $x_j = 0.3$ μm (the 2 μm technology parameters of the process described in Chapter 4). The ΔV_T data for this 2 μm technology and the computer-simulated values for d_{js} and d_{jd} determined $L_{min} = 1.25$ μm in Eq. (5.2). Effective substrate doping N_{SUB} can be used to calculate the depletion-region widths in n-channel

devices

$$d_{js} = \sqrt{\frac{2\epsilon_s \Phi_{SB}}{qN_{SUB}}} \tag{5.3}$$

$$d_{jd} = \sqrt{\frac{2\epsilon_s (\phi_{bi} + V_{DB})}{qN_{SUB}}} \tag{5.4}$$

where $\Phi_{SB} = \phi_{bi} + V_{SB}$ is the electrostatic potential difference between the source and substrate, and ϕ_{bi} is the source/drain n^+/substrate junction built-in potential. The empirical scaling rule in Eq. (5.2) can be rewritten for the $\Delta V_T = 100\,\text{mV}$ criterion as a function of V_{SB} and V_{DB} and taking into account the worst-case (maximum) d_{jd} when $V_{DB} = V_{SB} + V_{DD}$

$$L_{min} = 116 \left[x_j t_{ox} \frac{2\epsilon_s \Phi_{SB}}{qN_{SUB}} \left(\sqrt{1 + \frac{V_{DD}}{\Phi_{SB}}} + 1 \right)^2 \right]^{1/3} \tag{5.5}$$

where L_{min} and x_j are in microns, and t_{ox} is in angstroms.

Technology scaling under constant supply voltage constraints dictates the choices of t_{ox}, f_J, and N_{SUB} that enable transistors with a minimum effective channel length to maintain long-channel behavior. The value of L_{min} in Eq. (5.5) as a function of the t_{ox}/N_{SUB} ratio is plotted in Fig. 5.1 for two V_{DD} values. In the calculation in Fig. 5.1 the set of curves A assumes a deep-junction process in which $x_j = L_{min}/2$ ($f_J = 0.5$ in Eq. (5.1)), such that an upper bound for L_{min} is estimated. The set of curves B assume a shallow junction process ($f_J = 0.2$ in Eq. (5.1)). The solid lines denote $V_{DD} = 5\,\text{V}$, and the dashed lines represent $V_{DD} = 3\,\text{V}$. Experimental L_{min} values are indicated by the points in Fig. 5.1, for three technologies with $L_{eff} = 0.25$ μm [5.4]-[5.6] and two technologies with $L_{eff} = 1.25$ μm. Their parameters are listed in Table 5.1. As a general rule, the empirical relationship in Eq. (5.5) yields a conservative estimate of L_{min} for the short channel effects.

The maximum V_{DD} applicable in micron- and submicron-sized conventional and LDD devices is not limited, however, by DIBL phenomena; instead, it is determined by the hot-carrier-induced instabilities [5.7] that depend strongly on applied drain bias. The maximum V_{DD} that tolerates hot-carrier instabilities in the quarter-micron technologies listed in Table 5.1 for conventional devices is not known. These hot-carrier problems are compounded by raising N_{SUB} and scaling the lateral and

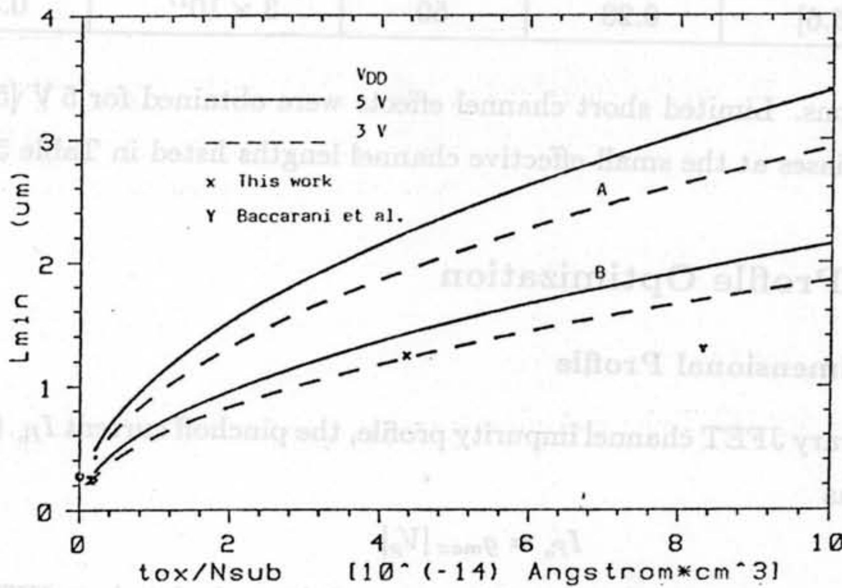

Figure 5.1: MINIMUM EFFECTIVE CHANNEL LENGTH DEPENDENCE ON TECHNOLOGY PARAMETERS. L_{min} is estimated for short channel criterion – at $V_{DD} = 5$ V (solid lines) and $V_{DD} = 3$ V (dashed lines) as determined in Eq. (5.5). Curves A for $f_J = 0.5$, and curves B for $f_J = 0.2$; $V_{SUB} = 0$ V.

Table 5.1: TECHNOLOGY PARAMETERS

Author	$L_{min}(\mu m)$	t_{ox} (Å)	N_{SUB} (cm^{-3})	f_J
This work	1.25	400	9×10^{15}	0.22
Baccarani [5.4]	1.3	250	3×10^{15}	0.27
Klaassen [5.5]	0.25	100	5×10^{16}	0.36
Baccarani [5.4]	0.25	50	3×10^{16}	0.40
Kobayashi [5.6]	0.28	50	3×10^{17}	0.54

vertical dimensions. Limited short channel effects were obtained for 5 V [5.5] and 4 V [5.6] drain biases at the small effective channel lengths listed in Table 5.1.

5.4 JFET Profile Optimization

5.4.1 One-Dimensional Profile

For an arbitrary JFET channel impurity profile, the pinchoff current I_{P_o} ($= W_J I_{p_o}$) can be written as

$$I_{P_o} = g_{max} |V_p| \tag{5.6}$$

where g_{max} is the maximum low-field conductance of the undepleted n^- JFET channel region. For a JFET with a W_J/L_J aspect ratio and $\langle\mu\rangle$ effective carrier mobility,

$$g_{max} = \left.\frac{\partial I_D}{\partial V_D}\right|_{max} = \frac{W_J}{L_J} q \langle\mu\rangle Q_{net} = \frac{W_J}{r_J} \quad (\Omega/\Box)^{-1} \tag{5.7}$$

Here, $r_J = L_J / q \langle\mu\rangle Q_{net}$ is the undepleted-channel JFET resistance normalized per unit width.

For a given JFET V_p, the primary concern in the design of the one-dimensional profile is the maximization of g_{max} and I_{P_o} based on Eq. (5.6). This requirement minimizes the series ON-resistance of the JFET at the drain end of the JMOS. The pinchoff voltage is dependent on the channel charge density and on the first moment of the channel charge distribution [5.8]; for an n-channel JFET,

$$V_p = -\frac{q}{\epsilon_s} \int_o^a y N(y) dy \tag{5.8}$$

where $a = \left(x_{j_{n^-}} - x_{j_{p^+}}\right)$ is the width of the buried diffused n^- region under the p^+ gate. Equation (5.8) incurs a small error caused by neglecting the JFET back bias that slightly reduces V_p. The effective carrier mobility in the JFET channel is expressed as

$$\langle\mu\rangle = \frac{\int_0^a \mu_{(N)} N(y)dy}{Q_{net}} \tag{5.9}$$

and the total net impurity dose (Q_{net}) in the JFET channel is

$$Q_{net} = \int_0^a N(y)dy \tag{5.10}$$

Equation (5.8) can be rewritten in terms of the design parameters of an equivalent uniformly doped JFET channel having doping density N_{Deff} and channel width t_{eff} and with the same net impurity dose in the channel

$$Q_{net} = \int_0^a N(y)dy = N_{Deff} t_{eff} \tag{5.11}$$

such that Eq. (5.8) becomes

$$V_p = V_{p_o} \frac{\langle y \rangle}{a} \tag{5.12}$$

where V_{p_o} is the pinchoff voltage of the equivalent uniformly doped channel JFET, and $\langle y \rangle$ is the first moment of the channel impurity distribution. V_{p_o} is given by

$$V_{p_o} = \frac{qN_{Deff} t_{eff}^2}{2\epsilon_s} \tag{5.13}$$

Equations (5.7), (5.12), and (5.13) provide the two basic JFET profile design parameters to be optimized to maximize the product of Eq. (5.6) — Q_{net} in the channel and the first moment of the channel impurity distribution

$$\langle y \rangle = \frac{\int_0^a yN(y)dy}{Q_{net}} \tag{5.14}$$

As demonstrated through simulations and experiments in Chapters 3 and 4, the series JFET serves as a current and voltage limiter thereby drastically reducing the high-field-induced phenomena. Device performance in terms of drive and speed is affected by the series JFET, as demonstrated in the low V_p results in Chapter 4. A rise in the JFET pinchoff voltage requires either increasing the distance $\langle y \rangle$ by using a retrograde profile [Eq. (5.12)], raising the n^- impurity dose [Eq. (5.13)], or increasing both; this voltage increase has the following implications.

- **Short channel effects.** The heavier the n^- doping, the deeper the n^-/p junction depth. The short channel effects (SCE) will be higher in deeper junctions. A practical limit on L_{min} dictated by SCE would be $L_{min} = 2x_j$ and, as a result, $x_{j_{n^-}}$ should be less that 0.5 μmin the submicron JMOS.

- **Device drive.** The saturated JFET current increases, and the n^- sheet resistance decreases with rising JFET pinchoff voltage. The lower the n^- sheet resistance, therefore, the less current limiting.

An ideal series device should have voltage-limiting properties and impose no current-drive penalty, which is equivalent to requiring a saturating device with zero ON-resistance (a device with finite V_p and infinite I_{P_o}). Because the JFET and MOSFET have the same channel width, the JFET pinchoff current per unit width I_{p_o} must be maximized. Based on Eq. (5.6), the maximum I_{p_o} is obtained by maximizing the low-field conductance of the JFET channel profile. It is possible to raise g_{max} (or Q_{net}) while maintaining the same V_p by using shallower n^- profiles with higher N_{Deff} (reducing t_{eff} and $\langle y \rangle$ simultaneously with increases in N_{Deff}). The technological limitations of ion implantation and annealing set a practical limit on how large the N_{Deff}/t_{eff} ratio can be.

As a general scaling rule, S/D junctions of MOSFETs should be as shallow as possible. It is recommended that the JFET profiles in the JMOS devices be implemented at the lowest implant energies and annealed at a cost of minimum diffusion. Two SUPREM-simulated JFET profiles are compared in Fig. 5.2. Here, HT indicates the high-temperature (1050°C) annealed phosphorus n^- low-V_p profile used in the experiment in Chapter 4, and LT is the low-temperature (900°C) annealed arsenic n^- low-V_p profile. The LT process avoids the n^- drive-in step by implanting n^- arsenic at high acceleration (400 keV). The HT and LT process parameters are summarized in Table 5.2. Their net n^- doses are 4.2×10^{12} and 4.3×10^{12} cm^{-2}, respectively. It can be seen that, for the same V_p as the HT profile, the LT profile has a shallower $x_{j_{n^-}}$ (0.45 μm) and a lower p^+ peak concentration, which should lead to better SCE characteristics and lower n^+/p^+ leakage as indicated by the reverse-diode characteristics described in Chapter 4.

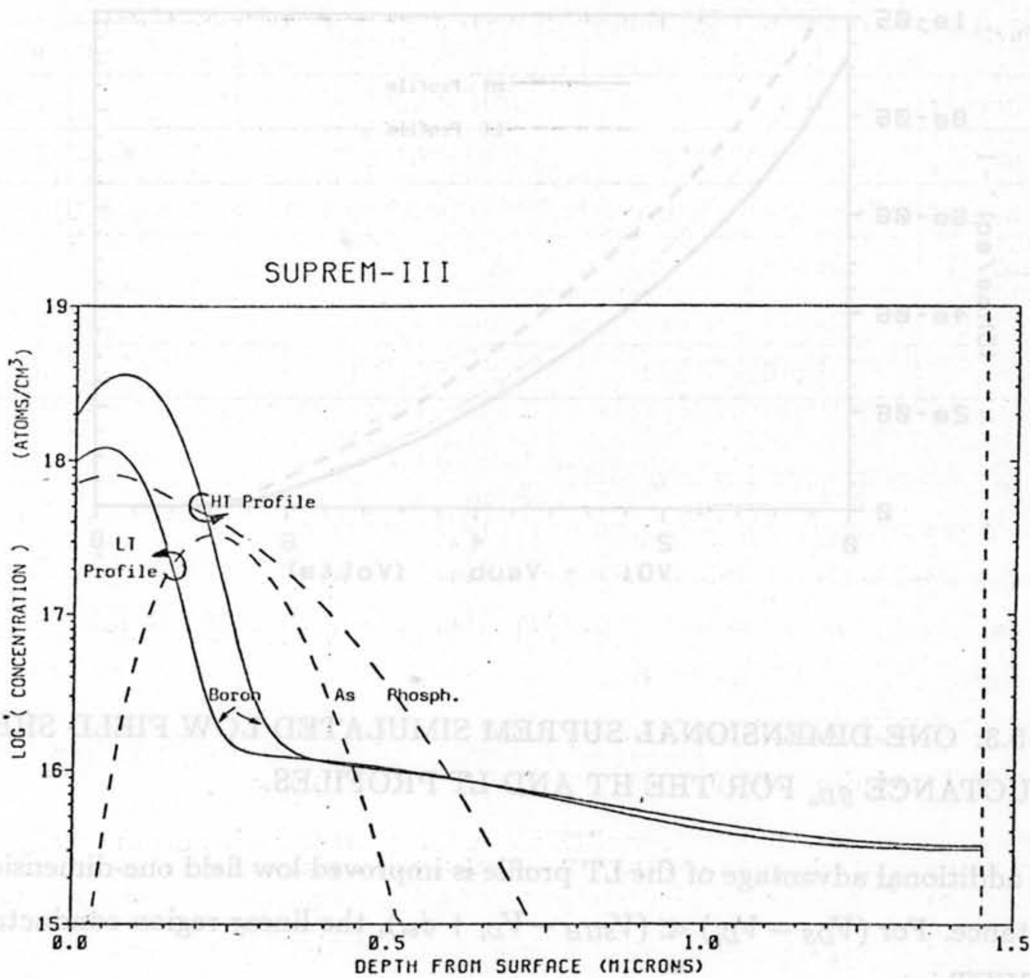

Figure 5.2: SUPREM SIMULATED LOW V_P JFET PROFILES FOR HIGH-TEMPERATURE (HT) AND LOW-TEMPERATURE (LT) PROCESSES.

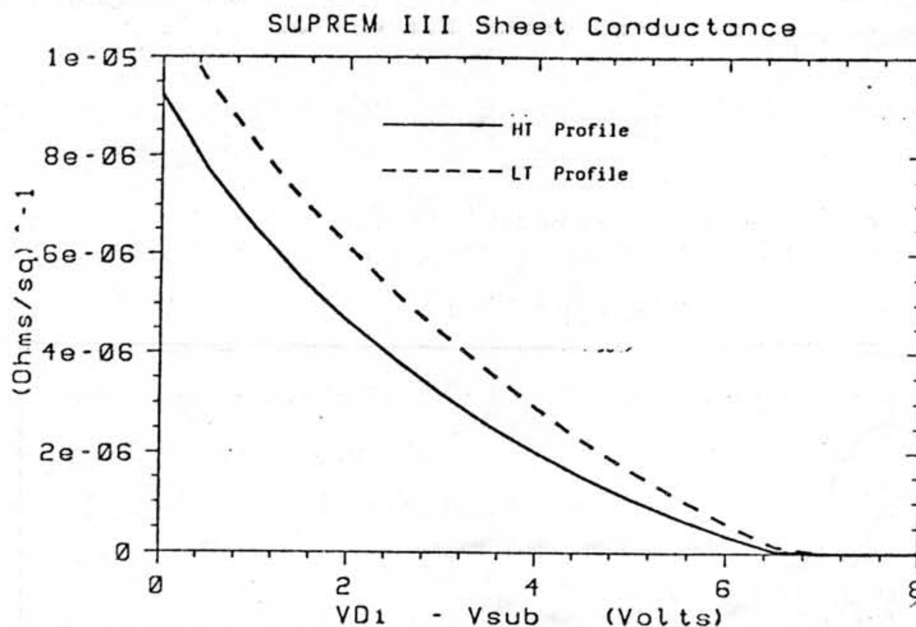

Figure 5.3: ONE-DIMENSIONAL SUPREM SIMULATED LOW FIELD SHEET CONDUCTANCE g_{D_o} FOR THE HT AND LT PROFILES.

An additional advantage of the LT profile is improved low field one-dimensional conductance. For $(V_{DS} - V_{D_i}) \ll (V_{SUB} - V_{D_i} + \phi_{bi})$, the linear region conductance of the JFET is

$$g_{D_o} = g_{max}\left(1 - \sqrt{\frac{V_{D_i} - V_{SUB} + \phi_{bi}}{|V_p|}}\right) \tag{5.15}$$

Figure 5.3 is the one-dimensional SUPREM-simulated conductance for the two profiles plotted against the substrate-to-n^- reverse bias $V_{D_i} - V_{SUB}$. This is the zero field value of g_{D_o} calculated in one dimension (that is, $V_{DS} = V_{D_i}$). The maximum g_{D_o} of the LT profile (at zero reverse bias) is 19 percent higher than in the HT profile. This indicates that I_{P_o} in the LT profile is also slightly larger than in the equivalent HT profile with the same pinchoff voltage. The advantage of the n^- LT profile in terms of g_{D_o} is the result its retrograde characteristics. From a one-dimensional standpoint, the HT type used in the implementation described in Chapter 4 is not

Table 5.2: PROFILE PARAMETERS FOR HT AND LT JFETS

Parameter	*HT Profile*	*LT Profile*	*Unit*
Q_{net}	4.2×10^{12}	4.3×10^{12}	cm^{-2}
n^- Dose	$2 \times 10^{13}(P^{31})$	$6 \times 10^{12}(As^{75})$	cm^{-2}
BF_2 p^+ Dose	6×10^{13} 100KeV	1.8×10^{13} 50keV	cm^{-2}
$x_{j_{n^-}}$	0.60	0.45	μm
n^- anneal	1050°C/60 min.	None	°C
p^+ n^- anneal	900°C/90 min.	900°C/90 min.	°C

optimum. Implementation of the low V_p JMOS yielded experimental values for V_p and g_{D_o} that are in disagreement with the simulated HT curve in Fig. 5.2. The relative merits of these profiles with respect to their low-field conductance properties are illustrated, however, by the simulated values.

5.4.2 Two-Dimensional Profile Optimization

Implementation of a low-temperature JMOS with the shallower profile in Fig. 5.2 requires careful consideration of the two-dimensional n^- arsenic and p^+ boron distributions. Based on SUPRA simulations discussed in Chapter 3, it is difficult to ensure the merging of the JFET and MOSFET channels for a retrograde n^- profile of the LT type shown in Fig. 5.2. In addition to the energy and doses of the n^- and p^+ implants, the actual two-dimensional distribution will depend on the edge profile of the gate electrode that self-aligns the drain implants to the MOSFET gate and the temperature of the anneals that follow these implants. The diffusion of these impurities can be affected also by the high doping diffusion effects that occur during the anneal of the n^+ drain.

Accurate physical models are necessary to account for these two-dimensional effects. The SUPRA simulator is limited in its ability to model the lateral distribution of implanted impurities. A full two-dimensional Boltzmann-transport model for the implant steps would provide the necessary insight to optimize the JFET

design in two dimensions. A low-temperature JMOS process would need to rely as much as possible on the two-dimensional distribution of as-implanted ions to merge the n^- region to the MOS surface channel. One-dimensional profile optimization alone may produce profiles with insufficiently low series resistance when the lateral n^- region is considered. In a two-dimensional JFET design suitable for submicron JMOSFETs, n^- arsenic and p^+ implants should be very shallow. The lateral spread of the p^+ implant must be minimum and enable the n^- region to reach toward the Si/SiO_2 interface in the lateral direction.

A more complex low-temperature JMOS process can also guarantee the merging of the JFET and MOSFET channels, which would require the formation of a thin sidewall oxide (less than 1500 Å) after the n^- implant and prior to the p^+ implant. In this structure, thermal cycling can be maintained low, the slow-diffusing arsenic is offset from the fast-diffusing p-type impurity in the lateral direction, and the lateral n^- region resistance is minimized. Although this approach adds more complexity to the JMOS process, it does reduce the parasitic effects caused by the lateral n^- region. A second sidewall formation would still be necessary prior to the n^+ implant.

5.5 JMOS Design Optimization

The choice of optimal JFET g_{D_o} and V_p is determined by two criteria for maximum performance degradation caused by the series device. The first is the reduction in the saturated current capability, which was determined to be minimum in the experimental JMOS when $Q_{net} \simeq 10^{13}$ cm^{-2} (the medium and high V_p devices discussed in Chapter 4). The second is the increase in the ON-resistance of the JMOS when compared to its conventional counterpart; the experimental data indicated that this criterion is more difficult to meet and requires detailed optimization.

5.5.1 Saturation Current Considerations

The optimization of the JMOS with respect to its saturation current-drive capability is described in this section, and the method is summarized as follows.

- Given a choice of V_{DD}, V_{SB}, and L_{min}, Eq. (5.5) is used to determine the ratio $f_J t_{ox}/N_{SUB}$ that guarantees long-channel behavior and drain junction breakdown voltage V_{BD} higher than V_{DD}. The value of V_{BD} should not be a limiting factor because it can be maintained above 5 V for very thin (> 60 Å) gate oxides and high N_{SUB} [5.9].

- The saturation voltage model of Moll and Sun [5.10] is used to determine the maximum drain saturation voltage in conventional MOSFETs with a minimum channel length.

$$V_{DS_{Sat}}(V_{GS_{max}}) = f(V_{GS})|_{V_{GS}=V_{DD}} \qquad (5.16)$$

- The JFET parameters g_{max} and V_p are chosen such that the saturation current for the minimum channel length is determined by MOSFET velocity saturation; that is equivalent to imposing a minimum V_{D_i} voltage at a given MOSFET V_{GS} drive.

$$V_{D_i}(L_{min}, V_{GS}) \geq V_{DS_{Sat}}(V_{GS}) \qquad (5.17)$$

This method establishes the values for the JFET parameters g_{max} and V_p that maximize current drive. The one-dimensional profile is then calculated and the maximum longitudinal peak field derived through computer simulations. The reliability constraint can be evaluated either through the magnitude of the resulting substrate current or through the magnitude of $E_{x_{peak}}$, the first is the better approach. As a simple rule, an upper limit on $E_{x_{peak}}$ guarantees that impact ionization is contained under a threshold value. The empirical substrate current model of Tam [5.11] predicts that in conventional devices, $(I_{SUB_{max}}/I_{DS}) \simeq 1.3 \times 10^{-3}$ at a peak field intensitity of $E_{x_{peak}} = 2 \times 10^5$V/cm. This maximum substrate current generation is approximately the maximum I_{SUB} generation level measured in the conventional devices operating at $V_{DS} = 5$ V and with an effective channel length of 1.5 μm The relationship of substrate current to $E_{x_{peak}}$, however, is expected to be structure dependent.

In the JMOSFETs, the effective V_{D_i} is a measure of the reduction of peak field intensity in the MOSFET channel region. Figures 5.4 and 5.5 show the equipotential contours and current density vectors for the low and high V_p structures, respectively, as described in Chapter 4. Both devices are biased under conditions

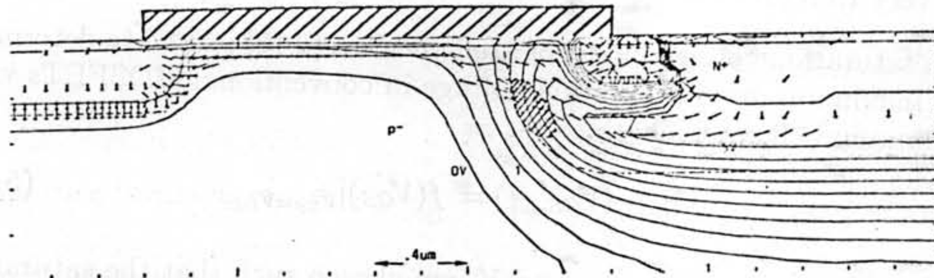

Figure 5.4: EQUIPOTENTIAL CONTOURS FOR LOW V_p JMOS. Vectors indicate current density, and the cross-hatched area is the region where E_x is larger than 100kV/cm; V_{GS}= 1 V, V_{DS}= 5 V and $V_{SUB} = 0V$. Electrostatic potential contours appear in 0.5 V steps.

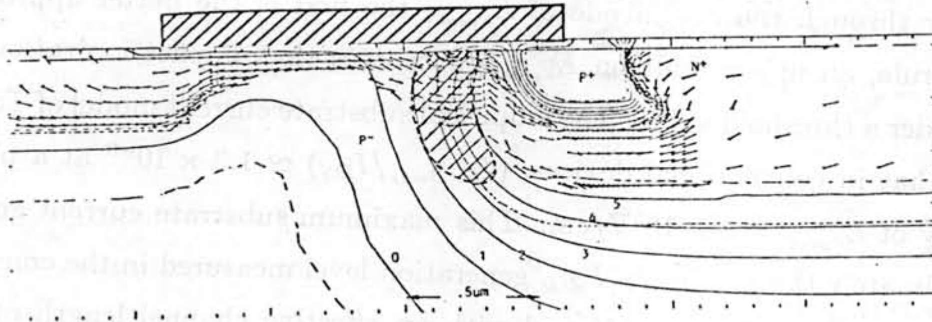

Figure 5.5: EQUIPOTENTIAL CONTOURS FOR HIGH V_p JMOS. Vectors indicate current density, and the cross-hatched area is the region where E_x is larger than 100KV/cm. V_{GS}= 1 V, V_{DS}= 5 V, $V_{SUB} = 0V$. Electrostatic potential contours appear in 1 V steps.

that normally create intense fields in the pinchoff region of conventional devices (V_{GS}= 1 V and V_{DS}= 5 V). The low V_p JMOS limits V_{D_i} to 2 V only. Under this condition, $E_{x_{peak}} = 110$kV/cm occurs 0.3μm away from the oxide/silicon interface. The region over which E_x is larger than 100kV/cm is cross-hatched in Figs. 5.4 and 5.5. For the effective V_{D_i} potential applied in the MOSFET channel region (2 V in Fig. 5.4 and 4 V in Fig. 5.5), the channel current is already saturated. In the high V_p JMOS in Fig. 5.5, the peak field has moved to the interface and has reached $E_{x_{peak}} = 450$kV/cm because of the higher effective V_{D_i}. Most of the current still flows through the bulk region where $E_{x_{peak}}$ is between 100 and 200 kV/cm. Although increasing with V_{D_i}, $E_{x_{peak}}$ may not be an adequate parameter for comparing the reliability improvement of the JMOS to other devices because the current path is structure dependent and only the fraction of the current that flows through the higher intensity field region contributes significantly to impact ionization.

To the extent that V_{D_i} is a measure of the intensity of the drain fields, it can be correlated to the hot-carrier-related phenomena experienced by the JMOS. The V_{D_i} potential in excess of $V_{DS_{Sat}}$ is the parameter to gauge any improvement in the high-field effects. The peak field intensity in the MOSFET drain was described in Chapter 2 as $\approx(V_{DS} - V_{DS_{Sat}})/l_p$ in the saturation region where $V_{DS} = V_{D_i}$ in JMOS transistors.

The empirical model of Moll and Sun [5.10] for $V_{DS_{Sat}}$ in MOSFETs is

$$V_{DS_{Sat}} = L_{eff}E_{CRIT}\left(\sqrt{1 + \frac{2(V_{GS} - V_T)}{L_{eff}E_{CRIT}}} - 1\right) \tag{5.18}$$

where E_{CRIT} is the critical field for mobility degradation. This expression can be rewritten [5.12] in terms of effective MOS channel mobility and v_{sat} as

$$V_{DS_{Sat}} = \frac{v_{sat}L_{eff}}{\mu_{eff}}\left(\sqrt{1 + \frac{2\mu_{eff}(V_{GS} - V_T)}{v_{sat}L_{eff}}} - 1\right) \tag{5.19}$$

as plotted in Fig. 5.6 as a function of V_{GS} for two mobility-degradation models. The solid lines take into account the mobility degradation related to gate-induced fields by computing $\mu_{eff} = \mu_o/(1 + \theta(V_{GS} - V_T))$. The dashed lines represent a two-region approximation of the velocity-field characteristics of the MOSFET that does not

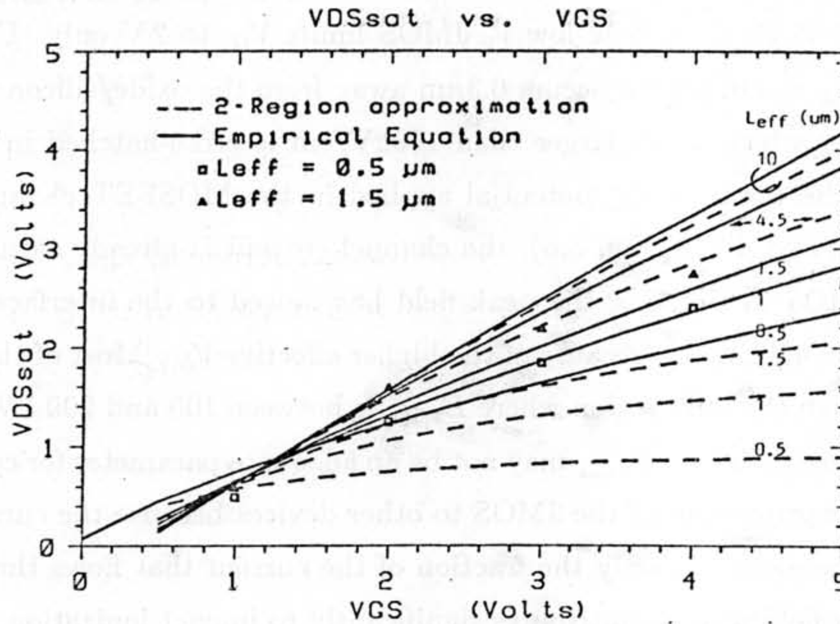

Figure 5.6: DEPENDENCE OF THE MOSFET DRAIN/SOURCE SATURATION VOLTAGE ON V_{GS}. Equation (5.19) is plotted in solid lines. A simpler two-region approximation to the electron $v-E$ dependence results in $V_{DS_{Sat}}$ shown in dashed lines. The data points are measured in conventional devices with $t_{ox} = 400\,\text{Å}$.

account for gate-induced mobility reduction; effective mobility is $\mu_{eff} = \mu_o/(1 + V_{DS}/(L_{eff}E_{TRA}))$. The parameters μ_o, θ, E_{CRIT}, and E_{TRA} are determined for the conventional devices in Appendix A. The measured points of $V_{DS_{Sat}}$ for two effective channel lengths are also shown in Fig. 5.6. Neglecting mobility degradation caused by the transversal field leads to an underestimation of $V_{DS_{Sat}}$ or an overestimation of E_{CRIT} in Eq. (5.18). Empirically Eq. (5.19) is a reasonable approximation of the saturation voltage resulting from velocity saturation; for the maximum $V_{DS_{Sat}}$ in the device with a minimum channel length, it becomes

$$V_{DS_{Sat}} = L_{min}E_{CRIT}\left(\sqrt{1 + \frac{2(V_{GS} - V_T)}{L_{min}E_{CRIT}}} - 1\right)\Bigg|_{V_{GS}=V_{DD}} \qquad (5.20)$$

The MOSFET saturation current in devices with length L_{min} is determined by the velocity-saturation limit which is only weakly dependent on L_{min}. An estimate of the maximum saturation current $I_{DS_{Sat}} = g_{m_{SAT}}(V_{GS} - V_T)$ is used in the design of the JMOSFET. Based on the average channel carrier velocity, this is expressed as

$$I_{DS_{Sat}} = WC_{ox} \langle v \rangle (V_{GS} - V_T) \tag{5.21}$$

It was shown in Chapter 4 that an average channel carrier velocity $\langle v \rangle = 6 \times 10^6$ cm/sec in a conventional MOSFET results in $g_{m_{SAT}} \simeq 20/t_{ox}$ (mS/μm), where t_{ox} is in angstrom; this establishes an upper bound on $I_{DS_{Sat}}$ at $V_T = V_{DD}/10$:

$$max(I_{DS_{Sat}}) = \frac{18V_{DD}}{t_{ox}} \quad (mA/\mu m) \tag{5.22}$$

Optimization of JMOS current drive mandates that the MOSFET with L_{min} must have an effective V_{D_i} greater than $V_{DS_{Sat}}$ in Eq. (5.20). The JMOS saturation current determined by the JFET pinchoff was defined in Chapter 3 as

$$I_p = I_{P_o}\left[1 - \left(\frac{\phi_{bi} + V_{D_i} - V_{SUB}}{|V_p|}\right)\right]^2 \tag{5.23}$$

for $(\phi_{bi} + V_{D_i} - V_{SUB}) \leq |V_p|$ and can be rewritten by substituting for I_{P_o} given in Eqs. (5.6)- (5.7) as

$$I_p = \frac{W_J}{L_J} g'_{max}|V_p|\left(1 - \left(\frac{\phi_{bi} + V_{D_i} - V_{SUB}}{|V_p|}\right)\right)^2 \tag{5.24}$$

where $g'_{max} = q\langle \mu \rangle Q_{net}$ from Eq. (5.7).

The reduction of carrier heating in MOSFETs, as indicated by substrate current measurements, has been correlated to the lower excess drain bias beyond $V_{DS_{Sat}}$ [5.13]. Experimental results indicated that in the JMOS devices where the JFET is pinched off, there is a reduction in the currents generated through impact ionization. This is the effect of lowering the effective drain bias V_{D_i}. To improve the reliability of an optimal JMOS over its operating-voltage range ($V_{DS} \leq V_{DD}$) , therefore, JFET and MOSFET saturation are required to occur at $I_{DS} = I_{DS_{Sat}}$. This is equivalent to requiring that the JFET pinchoff current I_p in Eq. (5.24) at $V_{D_i} = V_{DS_{Sat}}$ be

Table 5.3: DESIGN PARAMETERS IN Fig. 5.7

CURVE	L_{min} (μm)	t_{ox} (Å)	μ_o ($cm^2/V.sec$)
A	0.5	150	550
B	0.75	200	600
C	1.5	400	665

equal to the MOSFET saturation current in the short-channel regime as predicted in Eq. (5.21); that is,

$$I_{DS_{Sat}}(V_{GS}) = I_p|_{V_{D_i}=V_{DS_{Sat}}(V_{GS})} \tag{5.25}$$

$$WC_{ox}\langle v\rangle (V_{GS} - V_T) = \frac{W_J}{L_J} g'_{max}|V_p| \left[1 - \left(\frac{\phi_{bi} + V_{D_i} - V_{SUB}}{|V_p|}\right)\right]^2 \Bigg|_{V_{D_i}=V_{DS_{Sat}}} \tag{5.26}$$

Because large-width JMOS devices have the same JFET and MOSFET widths such that $W = W_J$, the above condition can be rearranged as

$$r_J = \frac{L_J}{g'_{max}} = \frac{|V_p|}{C_{ox}(V_{GS} - V_T)\langle v\rangle} \left[1 - \left(\frac{\phi_{bi} + V_{DS_{Sat}}(V_{GS}) - V_{SUB}}{|V_p|}\right)\right]^2 \tag{5.27}$$

where $V_{DS_{Sat}}(V_{GS})$ is the relationship in Eq. (5.19) for the MOSFET saturation voltage as a function of L_{eff} and gate bias, and r_J is the undepleted-channel JFET resistance normalized per unit width as defined in Eq. (5.7). The condition expressed in Eq. (5.27) determines, for the JFET parameters g'_{max}, L_J, and V_p, the values of $V_{GS} = f_s(L_{eff})$ for which the saturation of the short channel MOS and JFET occur simultaneously. In the design of an optimal JMOS, the JFET parameters should be chosen such that $V_T < f_s(L_{min}) < V_{DD}$. The larger $f_s(L_{min})$, the smaller the penalty for the current-drive capability of the minimum-size JMOS.

The dependence of r_J on the pinchoff voltage in Eqs. (5.19) and (5.27) is illustrated in Fig. 5.7 for three different L_{min}. The parameters for the scaled devices are listed in Table 5.3. Curves A, B, and C are for L_{min} = 0.5, 0.75, and 1.5 μm, respectively. The parameters g'_{max} and L_J are obtained from the V_p values determined from the following saturation current considerations. The set of curves labeled V_{GS} = 2 V indicates the $r_J(V_p)$ for which JFET pinchoff and MOS saturation

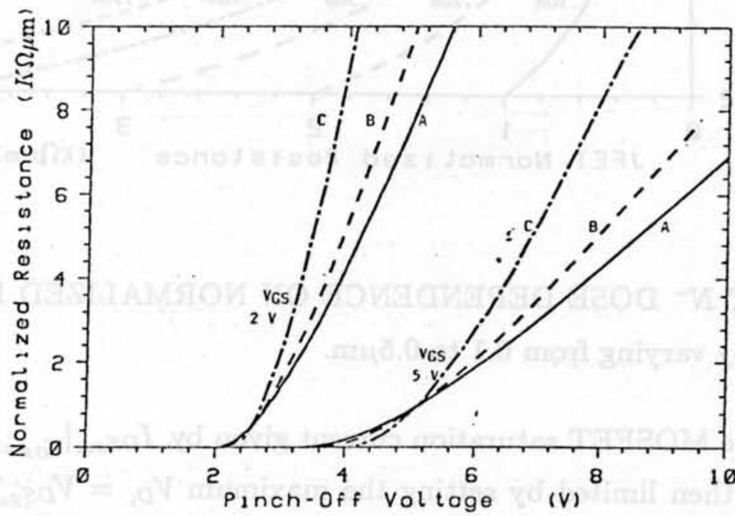

Figure 5.7: NORMALIZED RESISTANCE DEPENDENCE ON V_P IN A SATURATING JFET. $L_{min} = 0.5\mu$m (curves A), $L_{min} = 0.75\mu$m (curves B), $L_{min} = 1.5\mu$m (curves C).

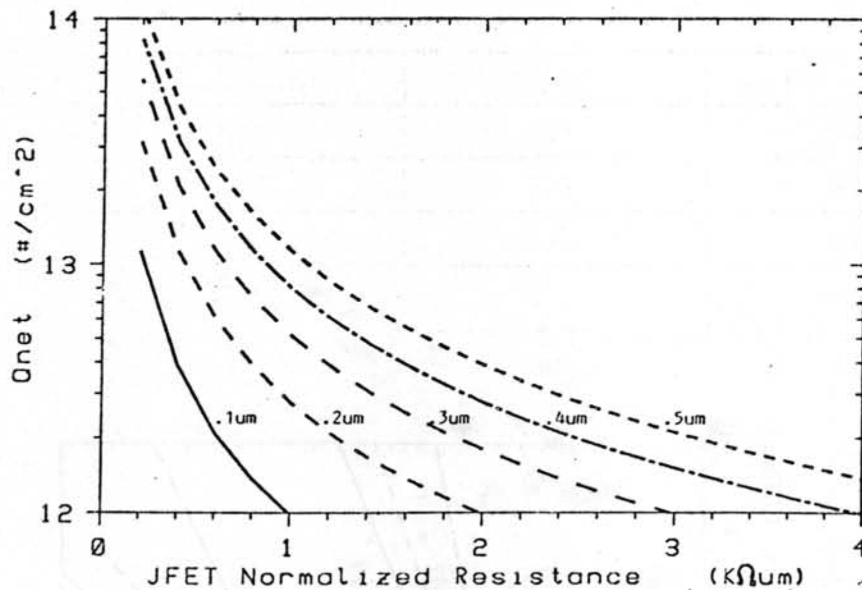

Figure 5.8: NET N^- DOSE DEPENDENCE ON NORMALIZED RESISTANCE. Curves are for L_J varying from 0.1 to 0.5μm.

both occur at the MOSFET saturation current given by $I_{DS_{Sat}}|_{V_{GS}=2\,V}$. The JMOS current drive is then limited by setting the maximum $V_{D_i} = V_{DS_{Sat}}$ at a 2 V gate bias. Although this design undermines the JMOS current capability, the effective V_{D_i} is low enough to reduce carrier heating in the drain. The set of curves labeled $V_{GS} = 5\,$V represents the designs that lead to a maximum $V_{D_i} = V_{DS_{Sat}}|_{V_{GS}=5\,V}$.

According to Eq. (5.7), there is a limited range of $r_J = L_J/(q\,\langle\mu\rangle\,Q_{net})$ in Fig. 5.7 that is practical to implement in VLSI JMOS. Assuming that the sidewall oxide lengths range from 0.2 to 0.5 L_{eff} (given that submicron polysilicon thickness is employed in conventional silicon-gate VLSI MOS technology), L_J will range from 0.1 to 0.5 μmfor micron-sized L_{min}. Figure (5.8) plots the required n^- doses as a function of r_J for different L_J. Linear region resistance and short channel effects prevent the use of light net dose (Q_{net}) and short-channel n^- regions. Unless extremely shallow highly doped n^- regions are used to implement low-dose JFETs, the n^- region is punched through and no JFET saturation can occur, as assumed

in the model.

The JMOS designer must select the degree of current limitation permitted in the device. The curves in Figs. 5.7 and 5.8 determine L_J and Q_{net}. The one-dimensional model for V_p and Q_{net}, however, does not predict the contribution of lateral n^- resistance; to minimize it, $x_{j_{p+}}$ must be shallow and the n^- lateral region needs to be adequately designed.

5.5.2 Linear Region ON-Resistance Considerations

The second criterion of performance for which the JMOSFET must be optimized is device ON-resistance. The values of r_J should be low enough to guarantee acceptable linear region characteristics. Optimization proceeds by setting a maximum ratio f_g for the MOSFET linear region output conductance g_{D_M} to the JFET g_{D_o}; that is, $f_g = g_{D_M}/g_{D_o}$. This implies that the linear region ON-resistance of the JMOS will be $100 f_g$ percent larger than that of the conventional device. Substituting Eq. (5.7) into Eq. (5.15),

$$f_g = \frac{g_{D_M}}{g_{D_o}} = \left(\frac{W/L_{eff}}{W_J/L_J}\right) \frac{\mu_{eff(V_{GS},V_{D_i})} C_{ox} \left(V_{GS} - V_T - \frac{V_{D_i}}{2}\right)}{g'_{max}\left(1 - \sqrt{\frac{V_{D_i} - V_{SUB} + \phi_{bi}}{|V_p|}}\right)} \tag{5.28}$$

The worst case (larger) f_g occurs at $V_{GS} \gg V_T$; in this mode and for a very low drain bias, the following approximations apply: $V_{D_i}(V_{GS}) \ll [\phi_{bi}, (V_{GS} - V_T)]$ and $\mu_{eff}(V_{GS}, V_{D_i}) \simeq \mu_o/(1 + \theta(V_{GS} - V_T))$. Taking $W = W_J$, Eq. (5.28) can then be rewritten for the minimum MOSFET effective channel length as

$$f_g = \left(\frac{L_J}{L_{min}}\right) \frac{\mu_o C_{ox}(V_{GS} - V_T)}{(1 + \theta(V_{GS} - V_T))\, q\, \langle\mu\rangle\, Q_{net}\left(1 - \sqrt{\frac{\phi_{bi} - V_{SUB}}{|V_p|}}\right)} \tag{5.29}$$

The worst-case f_g is the ratio of the low-field conductance of the minimum channel length MOSFET to the JFET low-field conductance.

Equations (5.27) and (5.29) can be used to determine the design parameters that satisfy the requirements on both the saturation current and ON-resistance degradation. By substituting Eq. (5.27) into Eq. (5.29), the conductance reduction

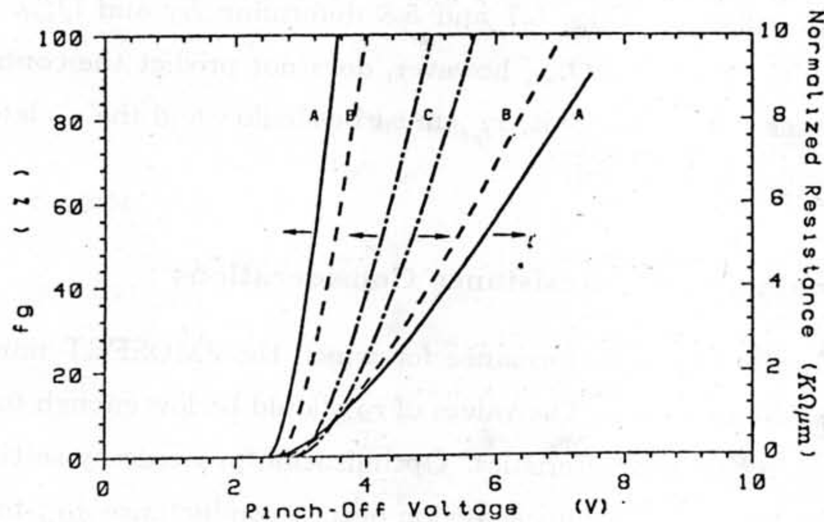

Figure 5.9: DEPENDENCE OF THE LINEAR CONDUCTANCE-REDUCTION FACTOR ON V_P. f_g is in percent. The corresponding r_J for the criterion in Eq. (5.27) at $V_{GS} = 3$ V is also plotted ($K\Omega\mu$m scale at the right).

factor for the minimum channel length JMOS is

$$f_g = \frac{\mu_o |V_p| \left[1 - \left(\frac{\phi_{bi} + V_{DS_{Sat}}(V_{GS}, L_{min}) - V_{SUB}}{|V_p|}\right)\right]^2}{L_{min} \langle v \rangle (1 + \theta(V_{GS} - V_T)) \left(1 - \sqrt{\frac{\phi_{bi} - V_{SUB}}{|V_p|}}\right)} \quad (5.30)$$

Figure 5.9 plots f_g vs the pinchoff voltage for the three L_{min} (A,B,C) listed in Table 5.3; the r_J that satisfies the saturation current criterion ($V_{D_i} = V_{DS_{Sat}}|_{V_{GS}=3V}$) in Eq. (5.27) is also plotted in Fig. 5.9. This criterion would lead to a JMOS design with as good a current drive as in the conventional devices operating at a 3 V supply voltage. Figure 5.9 demonstrates that, as the MOSFET parameters are scaled, some important practical constraints make it difficult to meet both the linear region criterion of, for example, a 20 percent increase in ON-resistance, and the saturation voltage criterion of limiting V_{D_i} to ensure reliability. First, the ON-resistance increase becomes more sensitive to the the pinchoff voltage (1 percent/10mV at

$L_{min} = 0.5\mu$m, vs 0.4 percent/10mV at $L_{min} = 1.5\mu$m) and, second, the JFET r_J must be severely reduced (150$\Omega\mu$m at $L_{min} = 0.5\mu$m, vs 1.1$k\Omega\mu$m at $L_{min} = 1.5\mu$m) to meet the 20 percent criterion. This series resistance requirement is very difficult to meet as JMOSFETs are scaled to submicron dimensions because of the practical limitations on grading the n^- profile; such a requirement translates into shorter L_J for the same Q_{net} or higher Q_{net} for the same L_J (Fig. 5.8). Considering the need for shallow junctions at shorter L_{min} and the optimal n^- dose that grades the drain junction fields, L_J should be reduced and Q_{net} increased simultaneously to meet the r_J required for JMOS scaling.

Obtaining r_J below 500 $\Omega\mu$m for $V_p < 5$ V requires highly doped medium-dose $> 10^{13}$ cm^{-2} n^- profiles and shallow $x_{j_{n^-}}$ (very steep profiles and, therefore, low S/D annealing temperatures are a necessity). Scaling the parasitic resistances is equally difficult for submicron LDDFETs. The self-aligned silicided or refractory-metal-covered S/D process is a solution to the scaling of n^+ series resistance that can be implemented in LDD and JMOS technologies using sidewall spacers [5.14]-[5.16]. The same need to reduce the n^- region length and junction depth and to increase n^- Q_{net} for series resistance scaling also applies to the submicron scaling of LDD technologies. Meeting the shallow junction requirements is easier, however, in submicron LDDFETs than in JMOS given the double-diffused nature of the JMOS.

5.6 Summary

The methodology developed to optimize of the JMOS devices revealed the shortcomings of scaling the JMOS to submicron L_{min}. Low-temperature retrograded shallow n^- profiles enhance performance and facilitate scaling. Two-dimensional process design is essential to guarantee adequate JMOS operation. The performance criteria for the design of the JFET profile and its associated low-field conductance, pinchoff voltage, and channel length are based on the current-drive capability of the minimum-sized JMOS and on low drain-bias conductance reduction. Reducing $V_{D'}$ results in less impact ionization under the MOSFET gate, and V_p and r_J are chosen such that the MOSFET effective drain bias is limited to $V_{DS_{Sat}}$ as determined

by the designer. Scaling the JFET parameters to a half-micron technology while maintaining its saturation properties and low series resistance is difficult. To minimize degradation of the linear region conductance when compared to conventional MOSFETs, a medium n^- sheet charge density is required; this, in turn, must be confined to a very thin ($< 0.1\mu$m) layer. Technological innovations in rapid thermal processing may be necessary to scale the JFET drain and MOSFET parameters at the same pace. Another significant consideration is two-dimensional profile optimization through process simulation. Improved two-dimensional process simulation models and tools are essential in the design of the JMOS because of the sensitivity of its electrical parameters to the impurity distributions in the drain end of the device.

Chapter 6

Conclusions and Recommendations

6.1 Conclusions

The drain region of VLSI MOSFETs should be engineered in such a way as to minimize the high field effects that result from the scaling of transistors under a constant supply voltage. Lightly doped drain (LDD) structures are necessary to reduce the harmful effects of intense drain fields. The reliability improvement in the LDD devices over conventional transistors is solely attributable to the reduction of these fields, which concomitantly leads to lower gate and substrate currents associated with hot carriers.

The major contributions of this research are summarized as follows.

- The JMOS transistor is a new lightly doped drain structure developed to overcome the limitations of conventional LDD devices with very low n^- drain doping density. It was designed to avoid the undesirable heating of carriers close to the gate oxide/silicon interface because damage to this interface leads to device degradation during its operation.

- The design of the JMOS was accomplished with the development of an equivalent circuit model that was simulated to demonstrate the ability of the JMOS to limit the effective drain voltage applied across the surface channel MOSFET. The ensuing reduction of drain fields was substantiated by two-dimensional simulation of submicron devices that demonstrated the reliability potential of the transistor. Both circuit and device simulations identified the principles of operation and the critical parameters of the proposed design.

- JMOS transistors were implemented with 2 μm NMOS technology. By varying the degrees of light doping, the trade-offs between high field effects and performance were identified. Reducing these field effects lowered the impact ionization substrate and gate injection currents but at the expense of limiting the current capability of the JMOS. The shortcomings of the structure in terms of series resistance and increased drain-to-substrate leakage were experimentally examined.

- The ability of the JMOS to sustain a 5 V supply with reduced fields is a property controlled by the device designer. The design of the drain JFET region was identified as critical to both the advantages and disadvantages of the structure when compared to conventional devices. The JFET structure parameters were optimized to observe the trade-off between the current-carrying capability and the attenuation of high field effects.

6.2 Recommendations

The following areas that could potentially enhance the understanding of JMOS operation were not addressed in this investigation.

- Two-dimensional models that would more closely describe the electrical characteristics of the drain JFET should be developed. As indicated by the simulation and experimental results, the short and two-dimensional distributions of the JFET channel are important in describing its action. A cylindrical plus a horizontal short-channel series JFET would be a possible lumped model for this work.

- The ac capacitance trade-offs of the JMOS should be investigated. Correct design of the drain can further minimize the Miller feedback capacitance and improve ac performance.

- The test of JMOS reliability under bias stresses that accelerate device aging by imposing stringent fields could further support the experimental evidence obtained from the gate and substrate characteristics that the JMOS indeed can reduce the high field effects to secure reliable submicron operation.

Additional experimental work on the implementation of LDD transistors could further extend the limits of constant voltage scaling and is described below.

- The implementation of a JFET with a shallower channel/substrate junction and higher doping densities would enhance the experimental results.

Achieving such densities would require the grading or elimination of the n^+-p^+ junction through highly two-dimensional process techniques. This structure should use shorter and lower temperature thermal cycles and would rely on two-dimensional implantation and diffusion effects to ensure the merging of the JFET and MOSFET channels. The results could lead to an even more suitable submicron device.

- An extremely lightly doped ($< 10^{15}\text{cm}^{-3}$) bulk-distributed drain has the potential of eliminating the problems associated with highly localized and peaked drain-induced fields. This approach is applied in power DMOS and LDMOS that require high drain-to-source isolation; a loss in circuit packing density could result. The buried-drain MOS transistor with a DMOS source has some of the positive aspects of this distributed-drain approach and should merit further investigation.

As the scaling of device dimensions continues, the need for accurate two-dimensional process models increases. The electrical characteristics of the JFET-MOSFET are sensitive to the lateral-diffusion profile in the region where the JFET and MOSFET channels merge. Because of this property, the JMOS could also be used as a test structure to experimentally ascertain the accuracy of two-dimensional diffusion, gate etching, and implantation process models.

Appendix A

MOSFET Model-Parameter Measurements

This appendix describes the MOSFET model parameters in this study and the procedure for extracting them from measured data. Because the goal was to obtain parameters suitable as input into a circuit simulator such as SPICE, the model chosen is the HPSPICE MOSFET. It consists of the classical MOS model to which several secondary effects (such as velocity saturation, mobility reduction, channel-length modulation, and short-channel threshold shift) are added.

A.1 Conventional MOSFET Model

In a conventional long channel MOSFET, the threshold voltage V_T is defined as

$$V_T = V_{T_O} + \gamma\left(\sqrt{|2\phi_f - V_{SUB}|} - \sqrt{2|\phi_f|}\right) \tag{A.1}$$

where

$$V_{T_O} = V_{FB} + 2\phi_f + \gamma\sqrt{2|\phi_f|} \tag{A.2}$$

$$\gamma = \pm\frac{\sqrt{2\epsilon_s q N_{SUB}}}{C_{ox}} \tag{A.3}$$

Here, V_{FB} is flatband voltage in the gate–oxide–silicon system, ϵ_s is the semiconductor dielectric constant, and $C_{ox} = \epsilon_{ox}/t_{ox}$ is the oxide capacitance per unit area. Most VLSI MOSFETs have threshold voltage adjustment ion implants in their channel region. Because substrate doping is depth-dependent, an effective substrate doping concentration N_{SUB} is used in the Eq. (A.3), where the ± denotes the n-channel (p-channel) MOSFETs. The Fermi potential in the bulk of the

semiconductor ϕ_f is referred to the bulk intrinsic Fermi potential as

$$\phi_f = -\frac{E_f - E_i}{q} \tag{A.4}$$

A.2 Mobility-Reduction Model

The MOSFET drain current [A.1] takes the form of

$$I_D = \frac{W_{eff}}{L_{eff}}\mu_{eff}C_{ox}\left[\left(V_{GS} - 2\phi_f - V_{FB} - \frac{V_{DS}}{2}\right)V_{DS} - \frac{2}{3}\gamma\left[(|V_{DS} + 2\phi_f|)^{3/2} - (2|\phi_f|)^{3/2}\right]\right] \tag{A.5}$$

where the source is assumed to be at ground potential, μ_{eff} is the effective inversion layer carrier mobility, and W_{eff} and L_{eff} are the effective channel width and length, respectively. The effective mobility is an average over the inversion layer that extends into the bulk from the oxide/semiconductor interface at $y = 0$,

$$\mu_{eff} = \frac{q\int_0^{\infty}\mu(y)n(y)dy}{|Q_m|} \tag{A.6}$$

where $\mu(y)$ and $n(y)$ are the mobility and density, respectively, of mobile carriers at a depth y from the interface, and $|Q_m|$ is the total absolute mobile charge per unit area in the inversion layer.

The mobility of carriers is a function of the transversal fields in the inversion layer because $E(y)|_{y=0}$ corresponds to a unique distribution of mobile carriers $n(y)$. The proximity to coulomb centers in the interface and the roughness of the interface play a role in reducing the effective mobility as obtained from device current measurements [A.2]. An empirical relationship [A.3] describes effective mobility reduction as a function of an effective transversal field in the inversion layer E_{eff} [A.4]

$$\mu'_{eff} = \mu_o\left(\frac{E_O}{E_{eff}}\right)^{C_1} \tag{A.7}$$

$$E_{eff} = \frac{1}{\epsilon_s}\left(\frac{Q_m}{2} + Q_B\right) \tag{A.8}$$

where Q_B is the bulk depleted charge, μ_o is the low field mobility, and E_O and C_1 are empirical constants that depend on the substrate doping. Typically, C_1 is on the order of 0.2–0.3 [A.2]. Under strong inversion $Q_B \ll Q_m$, and Eq. (A.8) can be

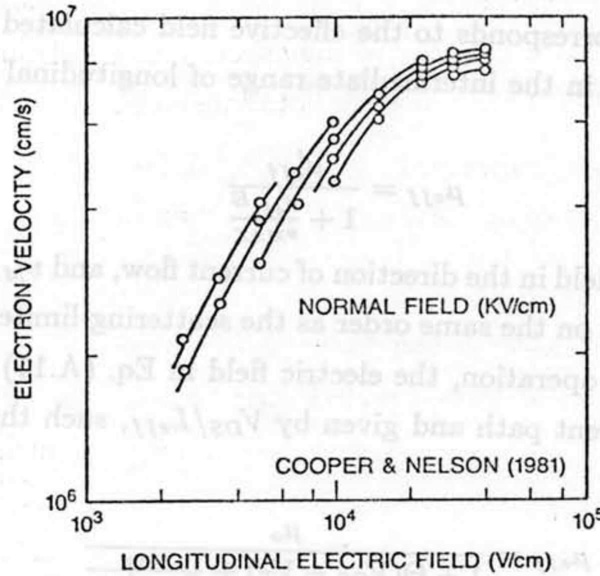

Figure A.1: Drift velocity as a function of longitudinal field for electrons on ⟨100⟩ silicon inversion layer at room temperature. Measured on MOS structures with $t_{ox} = 0.1\mu m$ [A.6].

approximated by

$$E_{eff} \simeq \frac{C_{ox}}{2\epsilon_s}(V_{GS} - V_T) \tag{A.9}$$

For circuit modeling purposes, it is more convenient to express the effective mobility reduction in terms of the gate electrode voltage. As a result, an empirical relationship is used by circuit simulators such as SPICE2 [A.5] to model surface mobility reduction caused by the transversal field as

$$\mu'_{eff} = \frac{\mu_o}{1 + \Theta(V_{GS} - V_T)} \tag{A.10}$$

where Θ is an empirical constant. The hyperbolic form of Eq.(A.10) has no physical meaning, but provides a reasonably simple and computationally fast approach to modeling the mobility reduction due to the gate-induced field which is transversal to carrier flow in the inversion layer.

The drift velocity of electrons in inversion layers increases sublinearly with longitudinal fields when their strength exceeds a few kV/cm. For fields larger than

the critical field E_{CRIT}, as shown in Fig. A.1 for n-channel devices, carrier velocity nearly saturates. The velocity-field relation in Fig. A.1 was measured by a time-of-flight technique for electrons in the silicon ⟨100⟩ inversion layers [A.6]. The normal field strength corresponds to the effective field calculated using Eq.(A.8). The mobility reduction in the intermediate range of longitudinal fields is modeled empirically [A.7] as

$$\mu_{eff} = \frac{\mu'_{eff}}{1 + \frac{\mu'_{eff} E}{v_{MAX}}} \tag{A.11}$$

where E is the electric field in the direction of current flow, and v_{MAX} is an empirical constant whose value is on the same order as the scattering-limited carrier velocity. In the triode region of operation, the electric field in Eq. (A.11) is assumed to be uniform along the current path and given by V_{DS}/L_{eff}, such that Eqs.A.10–A.11 can be rewritten as

$$\mu_{eff} = \frac{\mu_o}{1 + \Theta(V_{GS} - V_T) + \frac{V_{DS}}{E_{TRA} L_{eff}}} \tag{A.12}$$

where $E_{TRA} = v_{MAX}/\mu_o$ is an empirical constant. Eq. (A.12) is useful for device simulation because μ_{eff} is an explicit function of terminal voltages V_{GS} and V_{DS}. An alternative empirical formulation [A.3]

$$\mu_{eff} = \mu_o \left[\frac{\epsilon_s U_{CRIT}}{C_{ox}(V_{GS} - V_T - U_{TRA} V_{DS})} \right]^{U_{EXP}} \tag{A.13}$$

is also widely used by circuit simulators to model mobility reduction, The three empirical factors in this expression are U_{CRIT}, U_{TRA}, and U_{EXP}. In the parameter extraction procedure, Eq. (A.12) was used in which only two empirical factors appear.

A.3 Saturation Parameters

The model parameters that describe the saturation behavior of the transistors are E_{CRIT} and DE_{SAT}. In short channel transistors the drain current saturates at a drain voltage $V_{DS_{SAT}}$ for which the following equality holds:

$$\left. \frac{dI_D}{dV_{DS}} \right|_{V_{DS_{SAT}}} = \frac{I_D}{L_{eff} E_{CRIT}} \tag{A.14}$$

This yields the definition of E_{CRIT} which can then be extracted iteratively from the measured characteristics of short channel devices.

The drain current beyond the onset of saturation is given by

$$I_{D_{SAT}} = I_D(V_{DS_{SAT}})\left(1 + \frac{D_1}{L}\right) \quad \text{(A.15)}$$

where D_1 is nonzero if $V_{DS} > V_{DS_{SAT}}$ and zero otherwise. The parameter DE_{SAT} models the channel length modulation and the drain bias static induction that leads to the drain output conductance beyond saturation, by means of the expression

$$D_1 = \sqrt{\frac{V_{DS} - V_{DS_{SAT}}}{DE_{SAT}} + \left(\frac{E_{CRIT}}{2DE_{SAT}}\right)^2} - \frac{E_{CRIT}}{2DE_{SAT}} \quad \text{(A.16)}$$

A.4 Parameter Measurement and Extraction

The set of long channel parameters that is first extracted contains: the oxide thickness (t_{ox}), effective substrate doping (N_{SUB}), zero back gate bias threshold voltage V_{T_O}, low-field mobility (μ_o), and transversal-field mobility reduction parameter (Θ). The oxide thickness and the depletion edge doping concentration are measured over large area capacitors using the high frequency C–V technique. The test chips with capacitors and transistors of varying sizes enabled full parameter extraction.

The parameter extraction based on transistor measurements uses the oxide thickness from C–V measurements as an input parameter. First, the linear region characteristics $I_{DS} - V_{GS}$ of a large geometry MOSFET ($50/50\,\mu m$) are measured for various V_{SUB}. In a large-geometry device the effects of longitudinal drain fields, parasitic series resistances, and electrical channel length uncertainty are minimized. The four long channel parameters (N_{SUB}, V_{T_O}, μ_o, and Θ) were obtained by a simultaneous least-squares-fit optimization using the measured characteristics by the program TECAP2 [A.8].

The short channel parameters that model the threshold voltage fall off, the effective channel length, and the parasitic source and drain resistances are extracted by measuring similar linear region characteristics of short channel devices. Least squares fit to short channel device characteristics for a single channel length results in the extraction of L_{eff} and series source-drain resistances that are not as sound

Table A.1: SPICE MOSFET PARAMETERS.

Name	*Symbol*	*Value*	*Unit*
Low field mobility	μ_o	665	$cm^2V^{-1}sec^{-1}$
Oxide thickness	t_{ox}	393	Å
Transconductance factor	K_P	58.5	μAV^{-2}
Threshold voltage	V_{To}	0.32	V
Effective substrate doping	N_{SUB}	9.1×10^{15}	cm^{-3}
Body factor	γ	0.515	$V^{-1/2}$
$(L_{mask} - L_{eff})/2$	L_D	0.25	μm
Gate-field mobility factor	Θ (V_{NORM}^{-1})	0.061	V^{-1}
Longitudinal field mob. factor	E_{TRA}	7.3×10^4	$V\ cm^{-1}$
Critical field	E_{CRIT}	1.7×10^4	$V\ cm^{-1}$
Saturated drain conductance	DE_{SAT}	7.9×10^9	$V\ cm^{-2}$

as the values extracted for these parameters by the technique to be described in the next section. The saturation parameters are extracted last by using the $I_{DS} - V_{DS}$ characteristics of short channel transistors. From the least squares fit to these characteristics one optimizes simultaneously for the parameters E_{TRA}, E_{CRIT} and DE_{SAT}.

Table A.1 lists the n-channel MOSFET parameters extracted using the procedure explained. The transconductance factor, given by $K_P = \mu_o C_{ox}$, and the body factor (γ) defined in Eq. (A.3) are derived from the extracted parameters. The agreement between the measured and the simulated MOSFET I–V characteristics is illustrated in Fig. A.2.

A.5 Effective Channel Length and Series Resistance Extraction

An MOS transistor is represented in Fig. A.3 with the parasitic series source and drain resistances associated with the intrinsic device. For the linear regions bias, assuming that $V'_{DS} \ll V_T$, and $V'_{DS} \ll 2|\phi_f|$, the device current in Eq. (A.5)

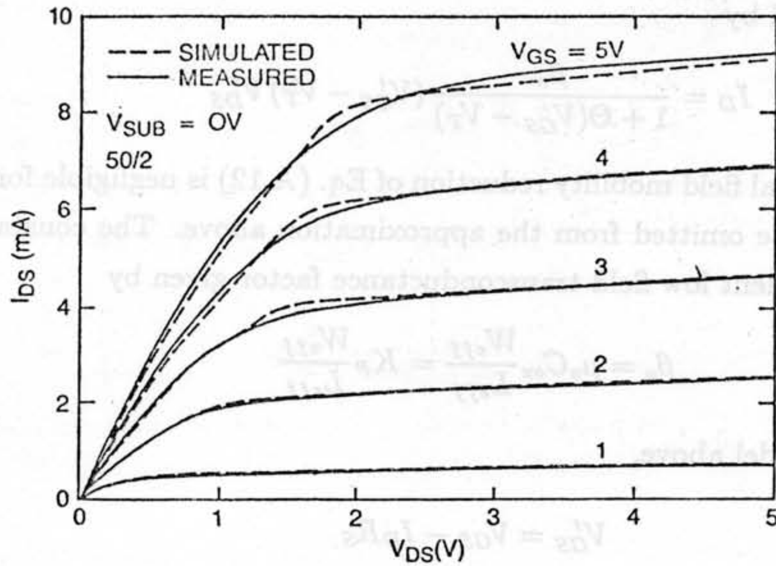

Figure A.2: Comparison of measured vs SPICE simulated MOSFET I–V characteristics for a conventional device. Measured model parameters used in the simulation are those of Table A.1.

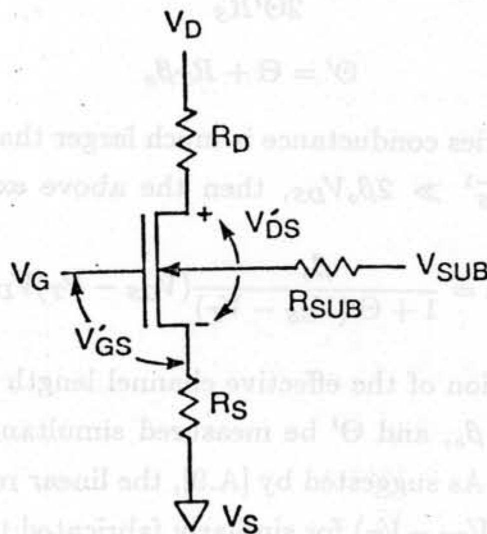

Figure A.3: Circuit model of the MOS transistor with series source-drain resistance.

can be approximated by

$$I_D = \frac{\beta_o}{1+\Theta(V'_{GS}-V_T)}(V'_{GS}-V_T)\,V'_{DS} \quad \text{(A.17)}$$

where the longitudinal field mobility reduction of Eq. (A.12) is negligible for $V'_{DS} \ll E_{TRA}L_{eff}$ and can be omitted from the approximation above. The constant β_o is the geometry dependent low field transconductance factor given by

$$\beta_o = \mu_o C_{ox}\frac{W_{eff}}{L_{eff}} = K_P\frac{W_{eff}}{L_{eff}} \quad \text{(A.18)}$$

From the circuit model above,

$$V'_{GS} = V_{GS} - I_D R_S \quad \text{(A.19)}$$

$$V'_{DS} = V_{DS} - I_D R_T \quad \text{(A.20)}$$

$$R_T = R_S + R_D \quad \text{(A.21)}$$

Substituting Eqs. A.19–A.21 into Eq. (A.17), and assuming that $(V_{GS}-V_T)R_T \gg V_{DS}R_S$, it results

$$I_D = \frac{1+\Theta'(V_{GS}-V_T) - \sqrt{[1+\Theta'(V_{GS}-V_T)]^2 - 4R_S\Theta'\beta_o(V_{GS}-V_T)V_{DS}}}{2\Theta' R_S} \quad \text{(A.22)}$$

$$\Theta' = \Theta + R_T\beta_o \quad \text{(A.23)}$$

If the parasitic source series conductance is much larger than the transistor channel transconductance, i.e $R_S^{-1} \gg 2\beta_o V_{DS}$, then the above expression for I_D can be simplified as

$$I_D = \frac{\beta_o}{1+\Theta'(V_{GS}-V_T)}(V_{GS}-V_T)V_{DS} \quad \text{(A.24)}$$

An adequate extraction of the effective channel length from linear region measurements requires that β_o, and Θ' be measured simultaneously for transistors of various channel lengths. As suggested by [A.9], the linear region plot of the relation $(V_{GS}-V_T)(V_{DS}/I_D)$ vs $(V_{GS}-V_T)$ for similarly fabricated transistors with identical geometry except for the drawn channel length, yields the values of β_o, and Θ'/β_o. As indicated by Eq. (A.24), the value of β_o^{-1} and of the latter are given by the intercept and the slope of the curves in Fig. A.4. The plot of the slope (Θ'/β_o) as a function

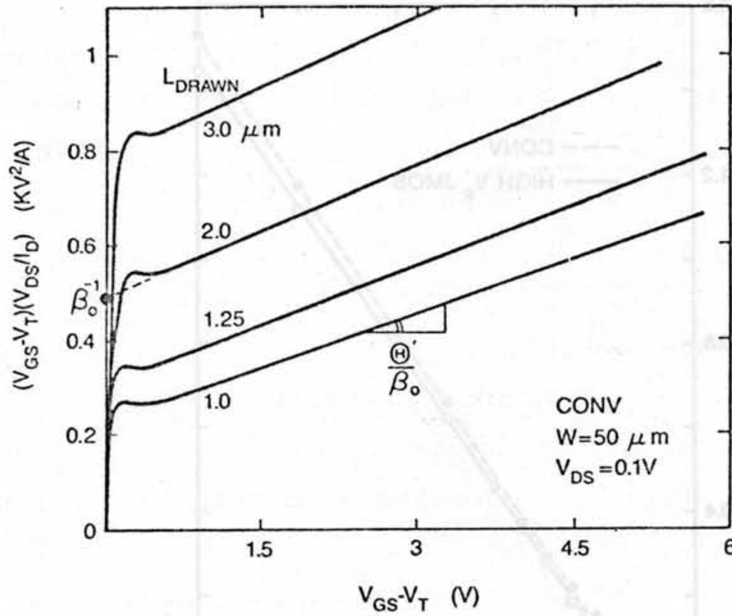

Figure A.4: Plot of the linear region $(V_{GS}-V_T)(V_{DS}/I_D)$ vs $(V_{GS}-V_T)$ for conventional n-channel transistors of various drawn channel lengths. Extraction of β_o and Θ' are indicated. V_{DS}= 0.1 V, $W_{DRAWN}=50\mu m$.

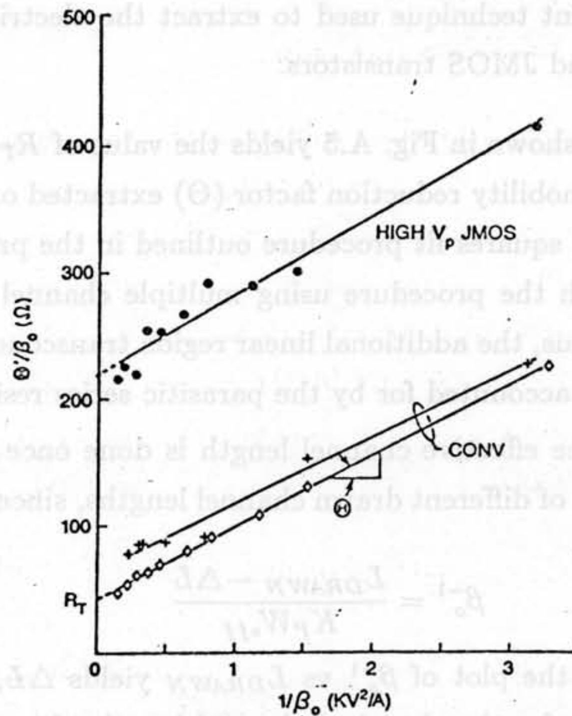

Figure A.5: Plot of Θ'/β_o vs β_o^{-1} to extract the value of Θ, R_T

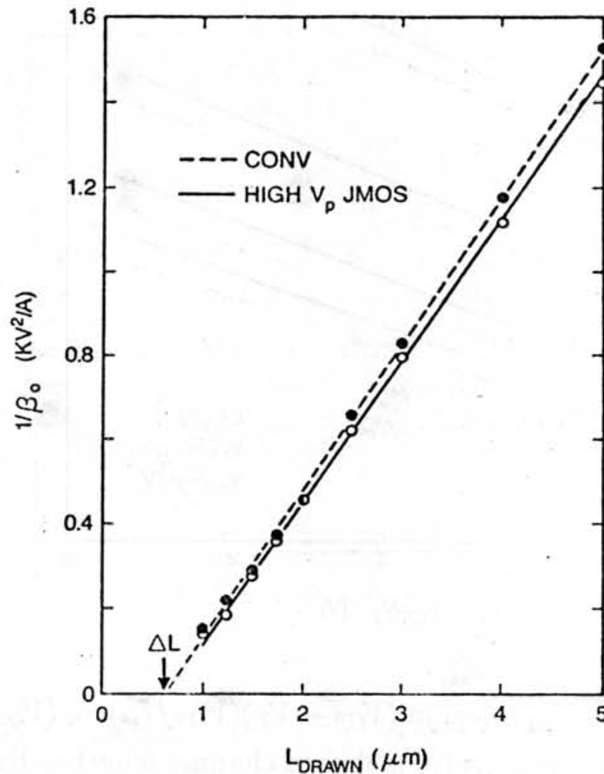

Figure A.6: Measurement technique used to extract the electrical channel length for both conventional and JMOS transistors.

of the intercept β_o^{-1}, as shown in Fig. A.5 yields the value of R_T and Θ. The value of the transversal field mobility reduction factor (Θ) extracted on a large geometry transistor with the least squares fit procedure outlined in the previous section and the value extracted with the procedure using multiple channel length transistors agreed within $\pm 4\%$. Thus, the additional linear region transconductance reduction for the device has to be accounted for by the parasitic series resistance.

The extraction of the effective channel length is done once the low field β_o is measured for transistors of different drawn channel lengths, since Eq. (A.18) can be rewritten as

$$\beta_o^{-1} = \frac{L_{DRAWN} - \Delta L}{K_P W_{eff}} \tag{A.25}$$

The x-axis intercept in the plot of β_o^{-1} vs L_{DRAWN} yields ΔL, which is then an average reduction factor for the electrical channel length of transistors fabricated side by side on the same chip. Fig. A.6 illustrates the extrapolation to ΔL for the case of both conventional and high V_p JMOS transistors built on the same

chip. The larger ΔL for the high V_p JMOSFETs is expected due to the larger junction depth for the n^- drain diffused layer. ΔL is assumed to be a channel length independent value for any given transistor design. This is a reasonable assumption provided that the transistors of multiple channel lengths used in the measurement are closely spaced to minimize unavoidable statistical variations across the wafer and from wafer to wafer. Thus, as the effective electrical channel length L_{eff} is determined from the measurement of the low field transconductance factor for various transistors, it is important to extract the true low field transconductance of the devices. This condition imposes the simultaneous extraction of the series resistance and gate-field mobility reduction factor for the L_{eff} measurement to be meaningful.

Appendix B

JFET–MOSFET Fabrication

Starting Material:

p-type, ⟨100⟩, 20 – 25 Ω-cm CZ Si, 75 mm diameter

1. Pad oxidation – 400 Å

   Dry oxidation, 1000°C/48 minutes.

2. Si_3N_4 deposition – 900 Å

   LPCVD deposition 790°C/27 minutes, 250 mTorr.

3. Si_3N_4 densification

   Anneal in O_2, 950°C/30 minutes.

4. Field photolithography

   Photoresist AZ1470J. Align and expose mask #1 with Canon projection aligner. Positive resist developer, 60 sec.

5. SiO_2 / Si_3N_4 etch

   50:1 H_2O:HF SiO_2 etch, 30 sec.

   Plasma etch Si_3N_4, Drytek 100 etcher, CF_4:O_2 500W, 7 min.

6. Channel stop implant

   Species: B^{11}

   Energy: 120 keV

   Dose: 1.5×10^{13} cm^{-2}

7. Field oxidation (LOCOS) – 7,600 Å

   Photoresist stripping. Standard cleaning.

   H_2O oxidation, 1000°C/200 minutes.

8. Nitride / Pad oxide stripping

Remove oxidized Si_3N_4, 6:1 BHF etch, 40 seconds. Hot DI water.

Si_3N_4 etch, H_3PO_4 at 155°C, 80 minutes.

Pad oxide strip, 6:1 BHF etch, 30 seconds.

9. Clean-up oxidation – 400 Å

    O_2–H_2O–O_2 cycle oxidation, 900°C/5 min.–12min.–5min.

10. Enhancement V_T adjustment implant

    Species: B^{11}

    Shallow V_T implant:

    Energy: 35 keV

    Dose: 5×10^{11} cm^{-2}

    Deep punchthrough supression implant:

    Energy: 180 keV

    Dose: 4×10^{11} cm^{-2}

11. Depletion photolithography

    Standard cleaning, no HF dip. PR coat, align and expose mask #2.

    PR developer, 60 sec. Descum in O_2 plasma, 500W, 2 min.

12. Depletion V_T adjustment implant

    Species: As^{75}

    Energy: 120 keV

    Dose: 2.6×10^{12} cm^{-2}

13. Clean-up oxide strip

    Resist strip. SiO_2 etch, 6:1 BHF, 30 sec.

14. Gate oxidation – 400 Å

    Dry oxidation, 1000°C/48 minutes.

    Oxide test. Gate oxide: 392 ± 4 Å. Field oxide: $5,800 \pm 40$ Å.

15. Buried contact photolithography

    PR coat. Align and expose mask #3.

    PR developer, 60 sec. Descum in O_2 plasma, 500W, 2 min.

16. Buried contact etch / backside oxide etch

    Oxide etch, 6:1 BHF, 70 sec.

17. Polysilicon deposition – 4,300 Å

    LPCVD deposition 620°C/68 minutes, 500 mTorr.

18. Polysilicon n^+ doping and masking oxidation

    $POCl_3$ source, 950°C/ 25 minutes.

    50:1 H_2O:HF, 30 sec. Dry oxidation cycle:

    N_2–O_2– N_2, 800°C, 5 min.–1 min.–2 min.

19. Polysilicon gate photolithography

    PR coat. Align and expose mask #4. Positive developer, 60 sec.

20. Polysilicon etch

    Masking oxide etch, 50:1 H_2O:HF, 30 sec.

    Descum in O_2 plasma, 500W, 90 sec.

    Poly plasma etch, C_2ClF_5:SF_6, 500W, 150 mTorr, 10% overetch.

21. LDD Phosphorous implant photolithography

    PR strip. Standard cleaning, no HF dip, 800°C N_2 singe.

    PR coat. Align and expose mask #5. Positive developer, 60 sec.

    Descum in O_2 plasma, 500W, 2 minutes.

22. n^- LDD implant

    Implant through 300 Å S/D oxide.

    Species: P^{31}

    Energy: 60 keV

    Dose: 2, 5, 7.5, 10 $\times 10^{13}$ cm^{-2} for JMOS runs.

    0.6, 1.2 $\times 10^{13}$ cm^{-2} for shallow LDD run.

23. n^- Phosphorous drive-in for JMOS runs

    PR strip. Standard cleaning, no HF dip.

    Argon anneal, 1050°C/60 minutes for JMOS runs.

24. p^+ JMOSFET Boron implant photolithography

    PR coat. Align and expose mask #6. Positive developer, 40 – 60 sec.

    Descum in O_2 plasma, 500W, 2 minutes.

25. p^+ JMOSFET Boron implant

    Species: $BF_2^{(49)}$

    Energy: 100 keV

    Dose: 0.6, 1.5, 2.2, 3 $\times 10^{14}$ cm^{-2}

26. n^+ conventional S/D Arsenic implant photolithography

    PR strip. Standard cleaning, no HF dip, 800°C N_2 singe.

PR coat. Align and expose mask #7. Positive developer, 40 – 60 sec.
Resist hardening, CF_4 plasma, 500W, 1 min. Resist bake at 150°C/30 min.
Descum in O_2 plasma, 500W, 2 minutes.

27. n^+ S/D implant

    Species: As^{75}
    Energy: 120 keV
    Dose: 1×10^{16} cm^{-2}

28. Photoresist removal

    O_2 plasma etch, 625W / H_2SO_4 etch cycles.

29. Sidewall oxide spacer deposition and densification – 8,200 Å

    Standard cleaning, no HF dip. LPCVD undoped SiO_2 deposition.
    at 450°C/54 minutes, 240 mTorr.
    SiO_2 densification in Argon, 900°C/30 minutes.

29. Spacer oxide etch

    Drytek plasma etcher, Ar:C_2F_6, 1 Torr.
    Silicon clean-up plasma etch, C_2ClF_5, 45 sec, 150 mTorr.

30. n^+ JMOS drain implant photolithography

    Standard cleaning, no HF dip, 800°C N_2 singe.
    PR coat. Align and expose mask #8. Mask large area JFET gates.
    Positive developer, 50 sec.
    Resist hardening, CF_4 plasma, 500W, 1 min. Resist bake at 150°C/30 min.
    Descum in O_2 plasma, 500W, 90 sec.

31. JMOS drain implant

    Species: As^{75}
    Energy: 120 keV
    Dose: 6×10^{15} cm^{-2}

32. Photoresist removal

    O_2 plasma etch, 625W / H_2SO_4 etch cycles.

33. Implant anneal / oxidation

    Standard cleaning, 15 sec. HF dip.
    900°C Argon anneal – 15 min., O_2 oxidation – 15 min.

34. Phosphorous glass deposition and densification – 6,200 Å

LPCVD SiO_2 deposition at 450°C, 290 mTorr.

500 Å SiO_2 / 5,700 Å SiO_2(7%P).

SiO_2 densification in Argon, 900°C/30 minutes.

35. Contact photolithography

    PR coat. Align and expose mask #9. Positive developer, 40 sec.

    Descum in O_2 plasma, 500W, 90 sec.

36. Contact etch

    Plasma etch, He:C_2F_6:CHF_3:O_2, 800 W, 10 Torr, 50 sec.

    Silicon clean-up plasma etch, C_2ClF_5, 45 sec, 150 mTorr.

    Resist bake at 120°C. Contact flash etch, 20:1 H_2O:HF, 30 sec.

37. Aluminum sputtering

    Standard clean. 50:1 HF dip.

    RF sputter etch, 2 min. Al(1% Si) sputtering.

38. Aluminum photolithography

    PR coat. Align and expose mask #10. Positive developer, 50 sec.

    Descum in O_2 plasma, 500W, 2 min.

39. Aluminum etch

    Wet etch at 40°Cuntil clear. Overetch $\simeq 2\mu m$.

    Plasma freckle removal, SF_6:C_2ClF_5, 30 sec.

    Backside oxide removal, 6:1 BHF etch.

40. Forming gas anneal and sinter

    PR strip and cleaning with PRS-1000 solution.

    Anneal in N_2:10% H_2, 400°C/45 minutes.

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