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Design of Wideband CMOS Building Block Circuits for Receivers from 0.5 up to 4 GHz

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Preface

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Abstract

This thesis has been focused on the design of wideband circuits for multi-band/multi-standard receivers. Three projects have been developed during this Ph.D. and are presented in this thesis: the required specifications of a wideband spectrum-sensing receiver, two versions of a 130 nm CMOS wideband low-noise variable gain amplifier, and a 40 nm CMOS wideband high-IF receiver.

The specifications of the spectrum-sensing receiver aim for the detection of three wideband signals WRAN, WiMax, and LTE. These are the principal wideband signals within the band from 50 MHz to 4 GHz, which has been selected because it was very crowded but with plenty of underused spaces. After the definition of the receiver specifications, the block-level specifications have also been calculated and verified through behavioral model simulations. The specifications have shown that a multi-standard receiver must cope with a large range of signal power, which motivated the design the low-noise variable gain amplifier (LNVGA).

The purpose of the LNVGA is to allow for the reception of both strong and weak signals by either reducing their signal power to values that do not compress the following blocks, like the mixer, or increasing it so that the noise figure is reduced, which increases the receiver sensitivity. The two fabricated LNVGAs achieve a gain tuning range up to 45 dB within a bandwidth of 3 GHz in addition to a NF as low as 3.4 dB. In contrast to other published VGAs, the proposed LNVGAs are the only ones that achieve a large gain tuning range in combination with a reasonably low NF. The large gain tuning range has been obtained thanks to the proposed low imbalance active balun. Both LNVGAs have been designed in 130 nm CMOS for a 1.2 V supply.

The final design is a 40 nm CMOS wideband high-IF receiver. Due to the evolution of CMOS technology, receivers with a higher IF and without external components are feasible in CMOS nodes below 65 nm. The main advantage of those high-IF receivers is their robustness to DC offsets, flicker noise, and even-order distortion. The two main contributions of this design are the LTNA and the modified bandpass switched-capacitor filter (SC-BPF). The LNTA uses a dual noise cancellation, which ensures a

low noise figure. Since both the mixer and the SC-BPF are passive, the LTNA needs an output impedance higher than the input impedance of the following blocks. Hence, a folded-cascode has been merged into the LNTA to increase its output impedance. The original SC-BPF has been modified by adding cross-connected transconductors at the in-phase (I) and quadrature (Q) inputs. These cross-connected transconductors not only boost but also allow for a variation of the Q-factor of the SC-BPF with a minimum increase of power consumption and design complexity. The highest voltage gain achieved by the receiver is 30 dB. While operating at the maximum gain, the receiver noise figure is 3.3 dB. The highest IIP3 is -2.5 dBm, and the IIP2 is as high as 35 dBm. The receiver and clock generation circuitry drain together 25 mA from a 0.9 V power supply. In comparison to the state-of-the-art, our receiver has the smallest area in addition to the reduced power consumption, and it targets the largest RF band.

Resumo

Projeto CMOS de circuitos banda larga para receptores de 0.5 à 4 GHz

O foco desta tese de doutorado é o projeto de circuitos integrados banda larga para receptores que atedem múltiplas bandas e padrões. Durante este doutorado, três projetos foram desenvolvidos e são apresentados nesta tese: a especificação de um receptor banda-larga para sensoriamento de espectro, duas versões do projeto de um amplificador de ganho variável e baixo ruído, fabricado em 130 nm CMOS, e o projeto de um receptor *high-IF* banda larga, fabricado em 40 nm CMOS.

As especificações do receptor de sensoriamento espectral visam a detecção de três sinais de banda larga: WRAN, WiMax e LTE. Estes são os principais sinais de banda larga dentro da banda de 50 MHz à 4 GHz. A band em questão, foi selecionada por estar, concomitantemente, superlotada e subutilizada. Após a definição das especificações do receptor, as especificações em nível de bloco também foram calculadas e verificadas através de simulações com modelos comportamentais dos circuitos. As especificações mostram que o receptor deve suportar sinais com diversos níveis de potência, o que motivou o projeto do amplificador de ganho variável de baixo ruído (LNVGA).

O objetivo do LNVGA é permitir a recepção de sinais fortes e fracos. Seja atenuando o sinal, de modo a evitar a sua compressão nos blocos subsequentes, como o mixer, ou amplificando-o, de modo a reduzir a figura de ruído do sistema, o que aumenta a sua sensibilidade. Os LNVGAs fabricados são capazes de ajustar o ganho em até 45 dB em uma banda de 3 GHz. Além disso, foi observada uma figura de ruído de até 3.4 dB. Em contraste com outros VGAs publicados, os LNVGAs propostos conseguem combinar grande capacidade de ajuste de ganho com uma figura de ruído satisfatoriamente baixa. Esta grande capacidade de se ajustar o ganho deve-se, parcialmente, ao *balun* ativo proposto neste projeto. Ambos os LNVGAs foram projetados em 130 nm CMOS com uma tensão de alimentação de 1.2 V.

O projeto final é um receptor *high-IF* banda larga em 40 nm CMOS. Devido à evolução da tecnologia CMOS, receptores *high-IF* sem componentes externos são viáveis em nós

abaixo de 65 nm. A principal vantagem destes receptores é a sua robustez, à *DC-offset*, ruído *flicker* e distorções de ordem par. As duas principais contribuições neste projeto são o transcondutor de baixo ruído (LTNA) e a modificação no filtro passa banda à capacitor chaveado (SC-BPF). O LNTA usa duplo cancelamento de ruído, garantindo uma baixa figura de ruído. Sendo o mixer e o SC-BPF passivos, a impedância de saída do LNTA deve ser maior que a impedância de entrada desses blocos. Deste modo, incorporou-se um *folded-cascode* ao LNTA para aumentar a sua impedância de saída. O SC-BPF original foi modificado adicionando-se um par cruzado de transcondutores as entradas em fase (I) e em quadratura (Q). Estes transcondutores permitem o aumento do valor do fator de qualidade (Q-factor) do SC-BPF e, até mesmo, o seu controle, isso com um aumento mínimo no consumo de energia e na complexidade do projeto. O maior ganho de tensão alcançado pelo receptor é de 30 dB. Operando com o ganho máximo, figura de ruído do receptor é de 3.3 dB. O IIP3 mais alto em 1 GHz é -2.5 dBm, e o IIP2 máximo é de 35 dBm. O receptor e o gerador de *clock* drenam 25 mA de uma fonte de 0.9 V. Em comparação com o estado da arte, o nosso receptor tem a menor área. Além disso, o consumo de energia é pequeno e buscamos operar numa banda mais ampla de entrada de RF.

Beknopte samenvatting

Dit proefschrift is gericht op het ontwerpen van breedbandige circuits voor multi-band/multi-standaard ontvangers. Drie projecten zijn ontwikkeld en worden beschreven in dit proefschrift: de vereiste specificaties van een breedbandige spectrum-detecterende ontvanger, twee versies van een 130 nm CMOS breedbandige lage-ruis versterker met variable versterking, en een 40 nm CMOS breedbandige hoog-IF ontvanger.

De specificaties van de spectrum-detecterende ontvanger zijn gericht op de detectie van drie breed-bandige signalen, namelijk WRAN, WiMax en LTE. Dit zijn de belangrijkste breedbandige signalen in de frequentieband van 50 MHz tot 4 GHz, een druk bezette band, maar met veel vrij beschikba-re ruimte. Na de definitie van de ontvanger specificaties, zijn de specificaties op blokniveau ook berekend en geverifieerd door gedragsmodel simulaties. De specificaties hebben aangetoond dat een multi-standaard ontvanger moet kunnen omgaan met een groot bereik in signaalvermogen, wat een motivatie is voor het ontwerp van de lage-ruis versterker met variabele versterking (LNVGA).

Het doel van de LNVGA is om de ontvangst van zowel sterke als zwakke signalen mogelijk te ma-ken, door ofwel signaalvermogen te verlagen tot waardes die niet tot compressie resulteren in de volgende blokken, zoals de mixer, of deze te verhogen zodat het ruisgetal wordt verminderd, wat een positief effect heeft op de gevoeligheid van de ontvanger. De twee gefabriceerde LNVGA's maken het mogelijk om de versterking aan te passen over een bereik van 45 dB, in een bandbreedte van 3 GHz, en met een ruisgetal van slechts 3,4 dB. In tegenstelling tot eerder gepubliceerde VGA's, zijn de voorgestelde LNVGA's de enige die een groot versterkingsbereik realiseren, in combinatie met een behoorlijk laag ruisgetal. Het grote versterkingsbereik is gerealiseerd dankzij de voorgestel-de actieve balun met lage onbalans. Beide LNVGA's zijn ontworpen in 130 nm CMOS voor een 1,2 V voedingsspanning.

Het laatste ontwerp is een 40 nm CMOS breedbandige hoog-IF ontvanger. Vanwege de schaling van CMOS technologieën, zijn ontvangers met een hoge IF en zonder externe componenten moge-lijk geworden voor CMOS technologieën onder 65 nm.

Het grote voordeel van deze hoog-IF ont-vangers is hun robuustheid ten opzichte van DC-verschuivingen, flikkerruis en even-orde vervor-ming. De twee belangrijkste bijdragen van dit ontwerp zijn de lage-ruis transimpedantie versterker (LNTA) en de aangepaste geschakelde-condensator banddoorlaat filter (SC-BPF). De LNTA maakt gebruik van een dubbele ruisonderdrukking, die zorgt voor een laag ruisgetal. Omdat zowel de mixer als de SC-BPF passief zijn, heeft de LNTA een uitgangsimpedantie nodig die hoger is dan de ingangsimpedantie van de volgende blokken. Vandaar dat een folded-cascode structuur gebruikt is in de LNTA om de uitgangsimpedantie te verhogen. De oorspronkelijke SC-BPF is aangepast door het toevoegen van kruisgekoppelde transconductors aan zowel de in-fase (I) als de kwadratuur-fase (Q) ingangen. Deze kruisgekoppelde transconductors verhogen niet alleen de Q-factor, maar maken ook een variatie mogelijk in de Q-factor van de SC-BPF met een minimale toename van het energieverbruik en complexiteit van het ontwerp. De grootste spanningsversterking van de ontvanger is 30 dB. Met deze maximale versterking is het ruisgetal van de ontvanger 3,3 dB. De hoogste IIP3 is 2,5 dBm en de IIP2 is 35 dBm. De ontvanger, inclusief klokgeneratie, verbruikt 25 mA van een 0,9 V voedingsspanning. In vergelijking met de state-of-the-art, heeft deze ontvanger de kleinste oppervlakte, een laag energieverbruik, en de grootste RF bandbreedte.

List of Abbreviations

Notation	Description
2G	Second generation mobile communication systems.
3G	Third generation mobile communication systems.
4G	Fourth generation mobile communication systems.
5G	Fifth generation mobile communication systems.
AC	Alternate current.
ADC	Analog-to-digital converter.
ATSC	Advanced television systems committee.
AWG	Arbitrary wave generator.
BER	Bit-error-rate.
BPF	Bandpass filter.
BR	Bit-rate.
CLK	Clock.
CMOS	Complementare metal oxide semiconductor.
CR	Cognitive Radio.
CS	Charge-sharing.
DAB	Digital audio broadcasting.
DC	Direct current.
DCS1800	Digital Cellular System at 1.8 GHz.
DMB	Digital multimedia broadcasting.
DSA	Dynamic spectrum access.
DSP	Digital signal processing.
DT	Discrete-time.
DUT	Dispositive under test.
DVB	Digital video broadcasting.

Notation	Description
FCC	American federal communications commission.
FFT	Fast fourier transform.
FPLL	Frequency-Phase locked loop.
FSV	Full-scale voltage.
GM-cells	Transconductor cells.
GPS	Global positioning system.
GSM850	Global System for Mobile communications at 850 MHz.
GSM900	Global System for Mobile communications at 900 MHz.
I	In-phase.
IF	Intermediate frequency.
IIP2	Input second-order intercept point.
IIP3	Input third-order intercept point.
IIR	Infinite impulse response.
IM2	Second-order intermodultion.
IM3	Third-order intermodulation.
IP1dB	Input 1 dB compression point.
IRR	Image rejection ratio.
LNA	Low-noise amplifier.
LNTA	Low-noise transconductance amplifier.
LNVGA	Low-noise variable-gain amplifier.
LO	Local oscillator.
LTE	Long-Term Evolution - 4G.
MI	Moderate inversion.
NEB	Noise equivalent bandwidth.
NF	Noise figure.
NMOS	N-channel MOSFET.
OFDM	Orthogonal frequency division multiplexing.
PAPR	Peak-to-average power ratio.
PCS1900	Personal communications service at 1.9 GHz.
PMOS	P-channel MOSFET.
PSG	Power signal generator.

Notation	Description
Q	Quadrature.
Q-factor	Quality-factor.
RF	Radio frequency.
RX	Receiver.
S11	The reflection coefficient of the input.
SAW	Surface acoustic wave.
SCC	Shared spectrum company.
SDR	Software defined radio.
SI	Strong inversion.
SNR	Signal-to-noise ratio.
SPI	Serial peripheral interface.
SS	Spectrum access.
TF	Transfer function.
TIA	Transimpedance amplifier.
UHF	Ultra high frequency radio for television broadcasting.
VDD	Voltage supply.
VGA	Variable-gain amplifier.
VVA	Variable-voltage attenuator.
WI	Weak inversion.
WiFi	WLAN - IEEE 802.11.
WiMax	Worldwide interoperability for microwave access - IEEE 802.16.
WLAN	Wireless local area network.
WPAN	Wireless personal area network.
WRAN	Wireless regional area network - IEEE 802.22.

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Chapter 1

Introduction

1.1 Motivation

The importance of wireless communication in our daily life has drastically increased over the last three decades thanks to the popularization of notebooks, tablets, and smartphones. The latter is, in fact, the main responsible for this wireless explosion. The number of cell phone subscriptions worldwide has risen by 133% over the last 10 years. In 2017, there were 7.7 billion subscriptions, whereas there were only 3.3 billion in 2007 [49]. In fact, there are already more subscriptions worldwide than people, with 1.03 subscription per person [49]. Moreover, 66.7% of the Earth population owns a cell phone, of those 54% owns a smartphone [40]. In addition to the number of users, the volume of data transferred is also rapidly increasing year by year. In order to attend this scenario of growing, new communication standards are emerging, and old standards are being expanded.

Conversely to an old cell phone that only connects with the base station, new wireless devices connect with many other devices, using a variety of wireless communication standards. For example, a modern smartphone supports the cellular (2G, 3G, 4G, etc.), WLAN (802.11a/b/g/n), WPAN (Bluetooth, Zigbee, etc.), broadcasting (DAB, DVB, DMB, etc.), and positioning (GPS) communication standards [44, 77]. Each of those standards is allocated within a band of the spectrum, which might differ from country to country. In addition to multiple bands, the wireless device must attend multiple specifications since each communication standard has an entirely different specification. Thus, the transceiver required for those applications must be not only portable but also multi-band and multi-standard.

The transceiver can be divided into three main parts: the receiver, the transmitter, and

the frequency synthesizer. The receiver and transmitter are responsible for receiving and transmitting the information, respectively, while the frequency synthesizer generates the clock frequencies needed within the radio transceiver for mixing with the incoming RF signal and also for mixing and converting to the ouput transmitter frequency RF band the outgoing baseband signal. The focus of this thesis are the blocks of the receiver; consequently, the discussion will be focused on the receiver hereafter.

1.2 Wideband receivers for multi-band and multi-standard applications

A receiver is usually composed of a low-noise amplifier (LNA), one or more RF mixers, filters for the band and channel selections, a baseband variable-gain amplifier (VGA), and the analog-to-digital converter (ADC). The LNA is the first block of the receiver chain; thus, it must provide the impedance match with the antenna and reduce the noise figure of the entire system. The mixer down-converts the income signal to low frequencies so that it can be processed by the ADC. Both the band and the channel are selected using either a lowpass or a bandpass filter. Those filters can be either passive or active. The baseband VGA controls the gain of the receiver so that the signal delivered to the ADC does not have a significant variation in amplitude, and stays within the dynamic range and full-scale range acceptable for the ADC. Finally, the ADC converts the analog signal to the digital domain.

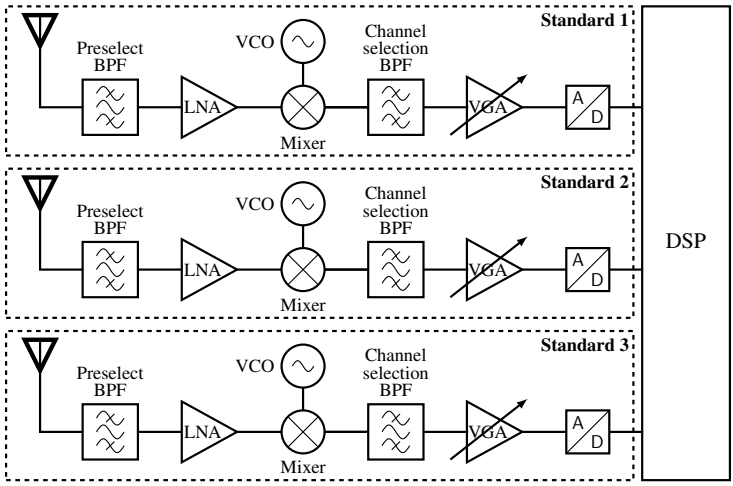


Figure 1.1: Multi-band/multi-standard receiver using multiple receivers [44, 77].

The most straightforward implementation of a multi-band/multi-standard receiver is one chip or, alternatively, one entire block in the receiver chip, per communication standard, like presented in figure 1.1. Since only the receiver block that is working is turned on, this approach can be very power efficient. Nevertheless, it requires multiple chips, or at least multiple blocks in a larger chip, which is not efficient from both the area and the design perspectives since each chip needs be designed individually. On top of that, every time a new communication standard is created the chip needs to be replaced.

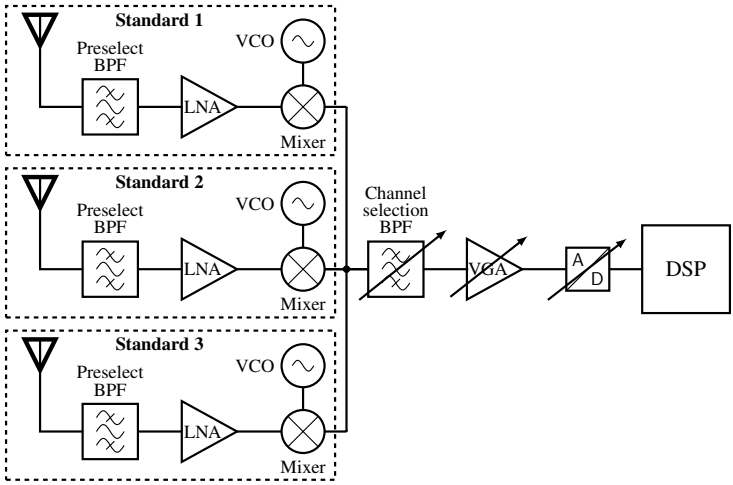


Figure 1.2: Multi-band/multi-standard receiver using multiple RF front-ends and sharing the baseband [44, 77].

Figure 1.2 shows a more efficient approach and the most common one [44]. It shares the baseband circuits, while the RF front-end circuits are replicated one per standard. In this case, since both the channel selection filter and the ADC must cope with all the communication standards, the blocks must be able to adjust their parameters to the communication standard in use. Although more complex than the first approach, this option reduces chip area, which reduces the overall cost, eventually. The inclusion of new communication standards or the modification of an old one still requires the replacement of the chip.

Another possible multi-band/multi-standard receiver is shown in figure 1.3, in which all the blocks are shared and can be adjusted to different communication standards. This block diagram is an example of software-defined radio (SDR). In order to share the RF front-end circuits, these circuits must be designed either with a tunable band or a wide band. The former changes its central frequency accordingly to the band in use, while the latter covers all the bands of interest. Although both approaches are possible, the

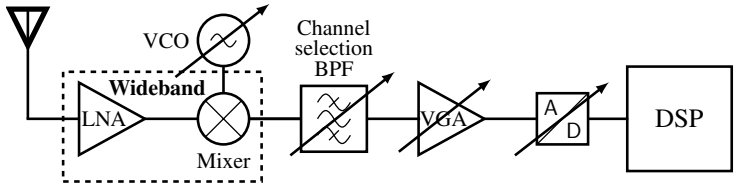


Figure 1.3: Multi-band/multi-standard receiver using a single receiver [44, 77].

research focus has been on SAW-less wideband receivers for SDR due to the pressure for cost reduction and universality of new wireless devices [65, 81, 61]. Currently, wideband RF techniques are the main direction for the design of multi-band/multi-standard receivers [61].

A SAW-less wideband receiver must have a low noise figure (NF), a high second and third order linearity, a high resilience to blockers, a wideband impedance match, and minimum external components, which poses a significant challenge to the RF circuits designers [61, 63, 15]. Indeed, blockers are the most significant threat to a SAW-less receiver since, without RF pre-filtering, a strong signal (e.g., 0 dBm) goes directly into the receiver desensitizing it, which deteriorates the receiver sensitivity. Also, the low supply voltage of new CMOS technologies aggravates the problem.

The wideband receivers can be divided into two groups: the ones with LNA [81, 71, 15, 93, 89, 63] and the ones without LNA (i.e., mixer first topology) [6, 73, 4, 60, 74, 58]. The mixer first receivers show a higher resilience to blockers than the LNA receivers. However, they are unable to achieve a low NF except for [73, 74, 58], which deliver a low NF but at the cost of a large area and high power consumption. On the other hand, the LNA receivers can achieve a very low NF with reasonable power consumption, but their 0 dBm blocker NF is 10 dB larger than that of the mixer first receivers [63].

So far, both approaches can achieve high performance but also have issues to solve. Even though it is not yet possible to surely state which is the best topology for wideband receivers, there are four techniques [61] presented in the previously cited works that will be probably part of them. Firstly, the noise canceling technique [17], which has been initially proposed to reduce the noise of LNAs and extrapolated to the receiver level in [73, 74]. This first technique has proven to be a sound technique to achieve a low NF within a wide band. Secondly, the N-path filtering [36], which was proposed in the 60's, has been successfully applied to design on-chip bandpass filters [96, 37, 71, 89, 64, 63]. Eventually, even high quality-factor (Q-factor) bandpass filters are achievable with N-path filtering [71]. Thirdly, the N-path passive mixer has been extensively used in previous designs. In fact, only [60] still uses an active mixer. Despite the lack of gain, the passive mixer under hard switching can have a low NF in addition to be an extremely linear circuit [5]. Finally, harmonic recombination has proven to be an

efficient way to reduce the intermodulation products. It must be applied in combination with the N-path mixing since it needs multiple paths with a different phase shift. Those paths are weighted and added in such way that the harmonics are canceled [81].

Due to the high importance of wideband blocks to those multi-band/multi-standard receivers, this thesis focuses on the design of such blocks. Although the projects developed in this thesis were done for two different CMOS technologies, and are not directly integrated all in the same silicon die for cost reasons. They are all aligned with multi-band/multi-standard applications.

1.3 Outline of this thesis

This thesis is structured as follows. Chapter 2 presents the first project, which aims at the specification of a wideband receiver for spectrum sensing of cognitive radio (CR). This work was part of the Cognitive Radio Project developed at the Federal University of Rio Grande do Sul (UFRGS), in which the purpose was the application of CR in a band wider than the one specified in the standard IEEE 802.22. Several masters and Ph.D. students were involved in this project, and this specification was used as a guideline in some of their designs [95, 23]. The CR design project at UFRGS was discontinued in late 2013, and silicon implementations for its modules were only in part finalized in 130nm CMOS, due to the complete absence of commercial interest (and financial support) for CR application. Nevertheless, this specification gives an overview of the challenges of RF wideband circuit design.

In the following chapters, the focus is moved to the circuit design of wideband blocks. In chapter 3, the design of two low-noise variable-gain amplifiers (LNVGA) in 130 nm CMOS are presented and discussed. The advantage of having a variable gain in the first stage of the receiver is to avoid signal compression. Whenever a strong signal arrives at the receiver, it can be attenuated, preventing the compression of the following blocks. This feature is particularly useful in a multi-standard application since there could be a considerable power variation between standards.

In chapter 4, the design of a discrete-time (DT) high-IF receiver in 40 nm CMOS is presented and discussed. This last design, encompassing an low-noise transconductance amplifier (LNTA), a mixer, and the band selection filtering, takes advantage of the CMOS technology evolution which allows for high-speed switches. Hence, the mixer and filters are designed with switched-capacitors circuit techniques, which enhance the performance of the passive mixer selected for the front-end and allow for the design of integrated charge-sharing (CS) bandpass filters (BPF), i.e., N-path filtering.

Finally, chapter 5 concludes this thesis, summarizes the main contributions, and proposes future work.

Chapter 2

A Spectrum-Sensing Receiver specification

2.1 Introduction

At the beginning of the 2000's, the spectrum scarcity became the central concern since the spectrum is a limited resource and the demand for wireless services were sharply rising [30, 24].

In 2002, the American Federal Communications Commission (FCC) made a limited measurement of spectrum use in certain USA urban areas, allowing for a partial view of the real spectrum usage [30]. During 2004 and 2005, the Shared Spectrum Company (SCC) did measurements of spectrum usage in several USA cities such as New York and Chicago [67, 68]. These measurements, which are presented in figure 2.1, show that the spectrum utilization was well below 100% of the sampled time. Those reports conclude that the problem is not only the congestion of the spectrum but its potentially poor usage too.

As a solution to that problem, the deployment of dynamic spectrum access (DSA) networks have been proposed, which opportunistically use the licensed spectrum without interfering with the licensed signals. This kind of system, however, is only feasible for radios that are aware of their surroundings and highly configurable such as the cognitive radio (CR) since it needs to change the operation parameters continuously [2].

The CR is a radio that can change the transmission and reception parameters based on the interaction with the environment in which it operates [21]. Hence, it must be able

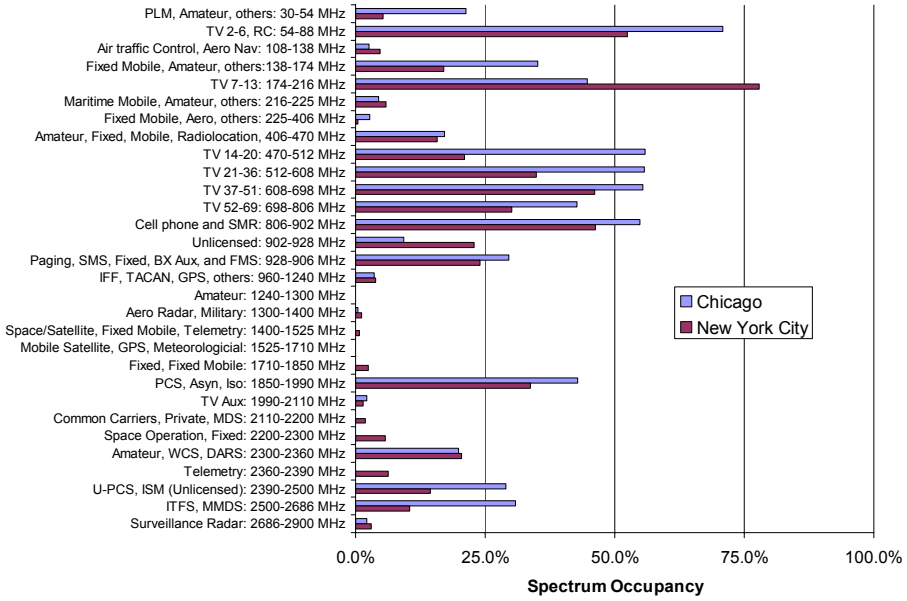


Figure 2.1: The spectrum occupation in New York and Chicago [67, 68].

to sense the spectrum information from its surrounding environment and to operate at several frequencies with different transmission standards [43, 87, 50, 2, 18].

The operation is divided into the spectrum sensing, analysis, and decision like is presented in figure 2.2a. First, the CR evaluates the spectrum. Second, it analyzes the data collected in the previous phase. Finally, it selects the operation parameters according to the spectral characteristics and user requirements.

The CR classifies the regions of the spectrum in either vacant or occupied. It is imperative that the CR operates only in the vacant regions. Thus, it updates this classification continuously. Also, this process must be fast and precise to avoid interference with other users. As soon as the primary user appears in the band in use by the CR, the CR must quickly tune itself to another spectrum region to avoid interference as shown in Fig 2.2b [43, 2].

The spectrum sensing (SS) receiver is a key block for the CR since it is responsible for the spectrum classification. The SS is called as digital when only the digital signal processing (DSP) does the channel classification. On the other hand, when the analog front-end partially or entirely does the classification, the SS is called analog.

The main difference between the SS and the primary receiver (i.e., the one used

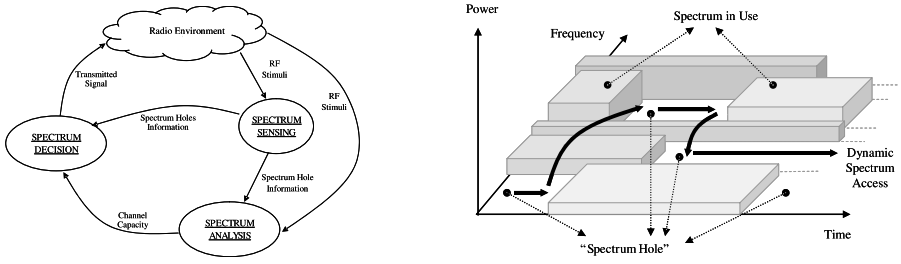


Figure 2.2: (a) The Cognitive cicle and (b) CR operation [2].

for actual communication) is their resilience to signal corruption. In contrast to the primary receiver, the SS receiver can still perform its detection task despite some signal corruption, so the requirements of noise and linearity are relaxed for the SS receiver. In fact, the acceptable signal-to-noise ratio (SNR) of the SS receiver is limited by the detection time and the coverage region, whereas the SNR of the primary receiver is limited by the bit-error-rate (BER).

2.2 The cognitive radio today

The cognitive radio (CR) drew a lot of attention during the last decade thanks to its exciting proposal of dynamically accessing the spectrum. In 2011, the first standard enabling CR deployment was published by IEEE. The IEEE 802.22 (WRAN) [47] has proposed the utilization of CR in the analog TV band to provide broadband wireless access in low population density areas, covering large regional distances (wider than typical cellular base-stations coverage), which are typically rural areas. However, this standard has never attracted the vital commercial interest and, eventually, the high-speed wireless communications standards for cell phones have reached those rural regions.

In late 2014, the WRAN working group initiated a project to broaden the spectrum sharing beyond TV bands [99]. In spite of that last effort, the research interest in circuits for CR faded. In the end, it was overshadowed by the research on SDR, which is similar to the CR but for the spectrum awareness. Although there is still some research related to the IEEE 802.22 and CR, the most recent publications are related to the MAC layer [42, 12].

Regarding spectrum sensing receivers, there are also few publications in the last 5 years. The most recent ones are [55, 52, 7].

2.3 The receiver specification

The specification of the SS receiver was part of the cognitive radio project at UFRGS, which aimed for the application of cognitive radio into a broader band than that of the IEEE 802.22. Until 2012, the cognitive radio application was limited to the analog TV bands. However, there was plenty of poorly used spectrum besides the TV band in which the CR could be explored [38].

Therefore, the RF band has been extended up to 3.8 GHz. With the extension of the RF band to the span of 50MHz to 3.8GHz, this radio would be able to cover the spectrum region with the best propagation conditions. Since the purpose is also a multi-standard receiver, three communication standards have been selected to be detected, WRAN (Wireless rural area network) [47], WiMax (IEEE 802.16) [46], and LTE [32]. We have considered other communication standards within this band as interferers. Among all the possible interferers, we have selected for the calculation the UHF wireless microphone [33], GSM850 [31], GSM900 [31], PCS1900 [31], DCS1800 [31], and WiFi [45] signals. Since those signal came all from portable devices, they ought to be most common interferers. Figure 2.3 shows a representation of the spectrum considered for the specification and also displays the maximum output power and RF bandwidth of the considered communication standards.

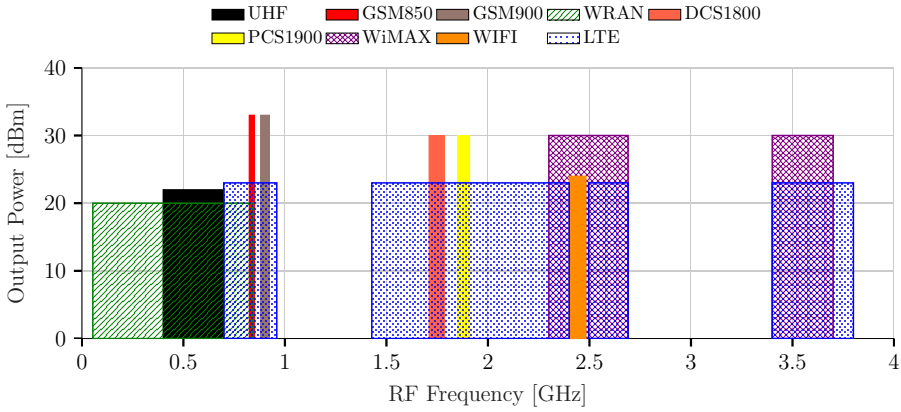


Figure 2.3: Maximum allowed output power and RF band of the communication standards considered in the specification [47, 46, 32, 33, 31, 45].

2.3.1 Frequency band

The frequency band of this SS receiver has to cover the standards WRAN, WiMax, and LTE, which are the signals to be detected. The WRAN band stretches from 54 to 842 MHz. In contrast, the WiMax and LTE bands are not composed of one single frequency band, several narrow frequency bands. The frequency bands that belong to the WiMax standard are located between 2.3 GHz and 11 GHz, while those of the LTE standard are located between 699 MHz and 3.8 GHz.

The spectrum sharing is a worthwhile feature within the crowded regions of the spectrum which is below 4 GHz. Although there are WiMax bands up to 11 GHz, it is not necessary to share the spectrum at frequencies above 4 GHz since this part of the spectrum is far from crowded. Moreover, the spectrum-sensing receiver needs to cover a wide band so that the possibility of finding a free frequency range for opportunistic CR operation is boosted. Thus, the design frequency band spans from 54 MHz up to 3.8 GHz.

2.3.2 Signal-to-noise ratio

The SNR is the comparison of the desired signal and the background noise that is given by [80]

$$SNR_{out} = \frac{E_b}{N_0} \cdot \frac{BR}{NEB}, \tag{2.1}$$

where E_b/N_0, BR, and NEB stand for the energy per information bit over noise power-spectral-density, the bit-rate in bps, and the noise-equivalent-bandwidth respectively. The ratio E_b/N_0 is proportional to the bit error rate (BER) and the type of signal modulation specified in the standard, the BR is close to the conversion rate of the analog-to-digital converter (ADC), and the NEB is equal to the channel bandwidth. Hence, improving the SNR also improves the BER. In contrast, when the receiver aims for the signal detection instead of the signal reception, the SNR is defined by the probabilities of detection and false alarm. The detection event is the correct classification of an occupied channel. Meanwhile, the false alarm event is the wrong classification of either a vacant or an occupied channel [51].

The relation of those probabilities and the SNR depends on the detection technique used by the SS receiver to classify the channels as vacant or occupied. The relationship between some detection methods and SNR have been presented in [47], and it is presented in table 2.1.

The detection methods are divided into two classes: the blind methods, which do not depend on specific signal features, and specific methods, which do rely on specific

signal features. The blind methods are the first three in table 2.1, whereas the others are specific techniques.

The blind methods of sensing are faster but less accurate than the specific ones. For example, the multi-resolution sensing method detects a signal in 0.1 ms, but it requires a -3 dB SNR. On the other hand, the FFT-based pilot detects a signal in 5 ms, but it does the detection with a -18 dB SNR. Since the methodologies of signal detection are not the focus of this work, we are just going to select the SNR values within table 2.1. Furthermore, the various sensing techniques are not going to be discussed here.

Table 2.1: SNR values and sensing time for different sensing techniques [47].

Sensing Techniques	Max. SNR [dB]	Min. Sensing time [ms]	Min. SNR [dB]	Max. Sensing time [ms]
Energy	-11	0.2	-18	5
Eigenvalue	-10.5	4	-15.8	32
Multi-resolution	-3.19	0.1	-24.47	16
Field-sync	-6	24.2	-12	24.2
Segment-sync	-7	4.06	-13	92.5
FFT-based pilot	-18	5	-24.5	50
Dual FPLL pilot	-12.42	50	-14.88	75
Spectral correlation	-7	0.333	-29	10
ATSC cyclostationary	-21	19.03	-31	19.03

2.3.3 Sensitivity

Sensitivity is the minimum signal power that a receiver detects with acceptable quality, which means the SNR needs to be sufficiently large so that the ADC correctly converts the analog signal.

Apart from the WRAN standard, the communication standards do not specify the sensitivity for spectrum-sensing since spectrum-sharing is not allowed. Therefore, this information is estimated based on the transmitted power, cell radius, and frequency band. The log-distance path loss model [79] gives a reasonable estimation of the received signal power. This model is estimated by

$$P_{RX} = P_{TX} - 20\log\left(\frac{4\pi f d_0}{c}\right) + n\,10\log\left(\frac{d_0}{d}\right), \tag{2.2}$$

where P_{RX}, P_{TX}, f, c, n, d_0, and d are the received signal power, the transmitted signal power, the frequency, the light speed, the path loss exponent, the reference distance, and the separation from the transmitter to the receiver respectively.

The minimum P_{RX} is equivalent to the receiver sensitivity. The value of n defines the environment where the transmission/reception takes place. For instance, n has values from 2.7 and 3.5 in urban areas, while n is 2 in free space. Table 2.2 shows the values of n for different environments. The transmitter was considered at the center of the cell. Hence, the separation of transmitter and receiver sets the coverage radius of the spectrum-sensing. Table 2.3 shows the minimum received signal power that has been calculated using 2.2 in addition to the information mentioned above.

Table 2.2: Path loss exponents for different environments [79].

Environment	n
Free space	2
Urban area cellular radio	$2.7 \sim 3.5$
Shadowed urban area cellular radio	$3 \sim 5$
In building line-of-sight	$1.6 \sim 1.8$
Obstructed in building	$4 \sim 6$
Obstructed in factories	$2 \sim 3$

Table 2.3: SS receiver minimum received signal for WRAN, WiMax and LTE detection.

	P_{TX} [dBm]	d [km]	n	f [GHz]	$P_{RX,min}$ [dBm]
WRAN	20 [47]	2	3	0.862	-110
WiMax	30 [46]	1.5	3	3.7	-109
LTE	23 [32]	1	3	3.8	-111

2.3.4 Noise Figure

The Noise Figure (NF) that is the representation of the noise factor (F) in dB quantifies the noise added by the circuit to the signal. F is given by

$$F = \frac{SNR_{in}}{SNR_{out}}, \tag{2.3}$$

where SNR_{in} and SNR_{out} are SNR at the input and output respectively. The relation between a receiver sensitivity and its NF is given by

$$P_{RX,min} = 10\log(kTB) + SNR_{out} + NF, \tag{2.4}$$

where $P_{RX,min}$ is the receiver sensitivity, k is the Boltzmann constant, T is the absolute temperature, and B is the channel bandwidth in Hz.

The eq. (2.4) shows that as the SNR increases either a lower NF is needed or the coverage area (i.e. the distance of the RX to the transmitter) has to be reduced. On the other hand, the reduction of the SNR slows down the detection since the signal is buried in noise. The first alternative forces the designer to reduce the system linearity to improve the NF, whereas the second one may cause harmful interference to the primary users since the detection will not be fast enough. Therefore, the minimum SNR is -20 dB that relaxes the NF requirement.

The WRAN standard proposes a 50 MHz channel for the spectrum sensing operation. Thus, this value has been used in calculations further in this section on SS.

The NF required for each one of the wireless system signals has been calculated using eq. (2.4) and the considerations mentioned above. The receiver NFs are 6.9 dB, 7.8 dB, and 6 dB for the standards WRAN, WiMax, and LTE respectively. These values are replaced in the Friis equation,

$$F = 1 + (F_1 - 1) + \frac{(F_2 - 1)}{A_{p1}} + \cdots + \frac{(F_m - 1)}{A_{p1} \ldots A_{p(m-1)}}, \tag{2.5}$$

where F_n is the noise factor for each stage and A_{Pn} is their respective available power gain, so the NF specification for each block of the circuit is calculated.

2.3.5 Linearity

The circuit linearity is defined by the interferers present inside the band and by the power of the received signal. The interferers may harm the incoming signal due to intermodulation, cross modulation, and desensitization. Meanwhile, the power of the received signal may create gain compression or desensitization.

There are three most common methods to evaluate the system linearity: the 1 dB input compression point (IP1dB), the input third-order intercept point (IIP3), and the input second-order intercept point (IIP2).

The IP1dB is the input power at which the gain drops by 1 dB, and it detects gain compression and desensitization. Indeed, both gain compression and desensitization saturate the receiver, but their causes are different. The former is the consequence of a strong incoming signal, while the latter is the result of a strong blocker at frequencies close to that of the incoming desired signal.

The gain compression is a major problem whenever the modulation scheme contains information in the amplitude since this information will be distorted when the receiver is saturated. The desensitization, on the other hand, is an issue regardless of the modulation scheme. Even with a small input signal, the blocker saturates the receiver

that reduces the gain. Consequently, the SNR at the receiver output is lowered, which becomes a critical issue for the receiver.

Since the receiver is a nonlinear system, any two signals that are applied to the system create components at frequencies that are not harmonics of those input frequencies. These components are the intermodulation (IM) products. Whenever one of these IM products falls onto the reception channel, it corrupts the incoming signal.

The consequence of IM in the reception is evaluated with the intercept point, which is the point in which the intermodulation (IM) product is equal to the fundamental tone. In the case of the second-order IM product (IM2) and third-order IM product (IM3), those points are named IIP2 and IIP3 respectively.

The selected signals, WRAN, WiMax, and LTE, use orthogonal frequency division multiplexing (OFDM), which is a popular scheme for wideband communication. Due to the subcarriers interaction, the OFDM shows a significant amplitude variation. Thus, the calculation of IP1dB needs to take into account the signal peak-to-average power ratio (PAPR). The PAPR of signals with a large number of subcarriers is [26]

$$PAPR \leq 2\ln(N), \tag{2.6}$$

where N is the number of subcarriers. Therefore, IP1dB is

$$IP1dB = P_{RX,max} + PAPR_{[dB]}, \tag{2.7}$$

where $P_{RX,max}$ is the maximum signal power in dBm that the receiver can detect. Table 2.4 shows the calculated IP1dB for the receiver.

Table 2.4: WRAN, WiMax, and LTE IP1dB for a spectrum-sensing receiver.

	N	PAPR (dB)	$P_{RX,max}$ (dBm)	IP1dB (dBm)
WRAN	2048	11.8	-41.8 [14]	-29.7
WiMax	256	10.44	-30 [46]	-19.5
LTE	1200	11.8	-25 [32]	-13.2

Due to the extended bandwidth of the receiver this thesis is focusing on, the interferers enter into the system without any filtering. Thus, the IM products created by those interferers can severely harm the incoming signal. The IIP2 and IIP3 are calculated by

$$IIP2 = 2P_{int} - IM2 \tag{2.8}$$

and

$$IIP3 = \frac{3P_{int} - IM3}{2} \tag{2.9}$$

respectively, where P_{int} is the interferer power at the receiver input. The IM2 and IM3 have been set to the receiver total integrated noise [80],

$$IM3 = IM2 = 10\log(kTB) + NF. \tag{2.10}$$

The power of each interferer has been estimated using (2.2). Like in section 2.3.3, the n is set to 3. The separation interferer-receiver has been set to 15 meters for all interferers apart from WRAN interferer, which has been set to 30 meters. The calculated IIP3 and IIP2 are presented in table 2.5 and table 2.6 respectively.

Table 2.5: Estimated SS Receiver IIP3 requirements due to IM interference in dBm.

	WRAN	WiMax	LTE	UHF	GSM850	GSM900	WiFi
WRAN	-1.1	-22.5	-17.5	-14.7	-4.2	-5.7	-38
WiMax	-1.6	-22.9	-17.8	-15	-4.63	-6.2	-38.8
LTE	-0.6	-21.9	-16.9	-14.1	-3.7	-5.2	-23.2

Table 2.6: Estimated SS Receiver IIP2 requirements due to IM interference in dBm.

	WRAN	WiMax	LTE	UHF	GSM850	GSM900	WiFi
WRAN	28.5	0	6.7	10.5	24.4	22.4	-20.7
Wimax	27.6	-0.8	5.8	9.55	23.5	21.5	-21.6
LTE	29.6	1.1	7.8	11.5	25.5	23.4	-0.5

The most demanding values of IP1dB, IIP2, and IIP3 for the 3 standards considered are -13.2, 29.6, and -0.6 dBm respectively. The IIP3 is the most severe linearity requirement since the system is wideband. Hence, there are a lot of pairs of interferers that can generate IM products that fall onto the channel.

The intercept point (IIPn) of each block of the receiver has been calculated with the cascade equation

$$\frac{1}{IIPn^2} \approx \frac{1}{IIPn_1^2} + \frac{A_{p1}^2}{IIPn_2^2} + \cdots + \frac{A_{p1}^2 \ldots A_{p(m-1)}^2}{IIPn_m^2}. \tag{2.11}$$

Also, the IP1dB of each block has been calculated with the same equation but replacing IIPn for the IP1dB.

2.3.6 Gain

The receiver gain has been calculated so that the signal amplitude at the output of the receiver is within the ADC full-scale voltage (FSV). A reasonable FSV is 1 V peak-to-peak, which is equivalent to 4 dBm in a 50 Ω system (i.e., 50 Ω at both ends) [80]. The gain needs to accommodate for the variation of the input power. Thus, we calculate both the maximum and minimum gain required for the wideband receiver. These results are presented in Tab 2.7. We are considering this receiver a 50 Ω system, so the receiver power and voltage gain are the same, which simplifies the calculation. In fact, only the input impedance of the LNA must always match the 50 Ω impedance of the antenna (or signal generator). The definition of the VGA output impedance depends on the input impedance of the ADC. The ADC input impedance, at low frequencies, is a resistance, which must ideally be either infinite large for a voltage input or zero for a current input [66]. Hence, the output impedance of the VGA must be selected to maximize either voltage or current transfer. At high frequencies, the input impedance of the ADC is dominated by a capacitive component, which is usually a switched-capacitor, which samples the input [66]. The main difference appears at very high frequencies, in which the input of the ADC must match the output of the VGA [66].

Table 2.7: Maximum and minimum receiver power gain (A_p).

	$P_{RX,min}$ [dBm]	$P_{RX,max}$ [dBm]	$A_{p,min}$ [dB]	$A_{p,max}$ [dB]
WRAN	-110	-41.8	45.8	114
Wimax	-109	-30	33.9	113
LTE	-111	-25	28.9	115

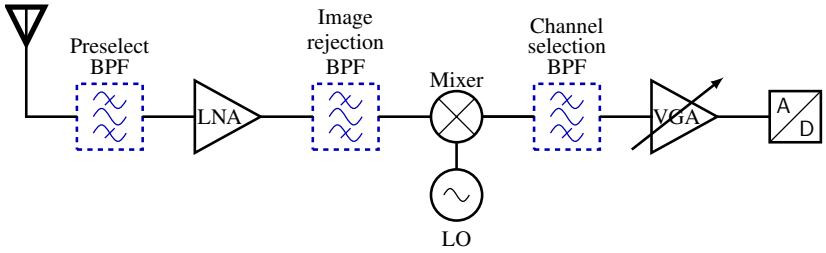
2.4 Receiver architectures

The three possible architectures for the receiver are superheterodyne, low-IF, and zero-IF. The main difference between these architectures is the position of the intermediate frequency (IF). Additionally, other differences arise as consequence of the IF position.

The superheterodyne receiver that is shown in figure 2.4 uses an LO frequency different than the RF frequency, so it has a nonzero IF. Also, the position of the IF is fixed so that the receiver does not need a channel-selection filter with a variable central frequency, which simplifies the design of the filter.

The problem of the superheterodyne receiver is the image. Due to the nonzero IF, the RF frequency is translated to the same IF whether it is above or below the LO frequency as shown in figure 2.5. This effect is called the image problem, and it is a

Figure 2.4: Superheterodyne receiver chain.



huge issue to the receiver since an interferer that falls onto the image position will be down-converted onto the IF, corrupting the incoming signal. Therefore, a filter with a proper image rejection is mandatory for the superheterodyne receiver.

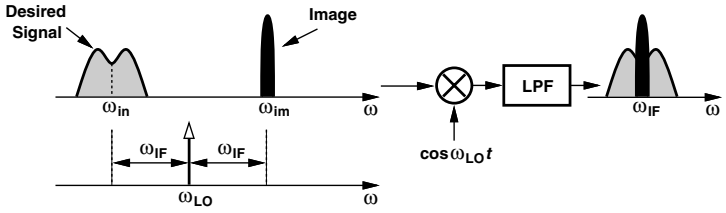


Figure 2.5: The image problem [80].

The image rejection filter, typically, appears between the LNA and the mixer so that the gain of the LNA reduces the filter contribution to the NF. Moreover, since the distance between the image and RF frequency is twice the value of the IF, a large attenuation of the image is achieved by selecting a sufficiently high IF. However, the premise of the superheterodyne receiver is to perform the channel selection at a low IF so that a channel-selection filter with high Q is feasible. Hence, there is a trade-off between image rejection and channel selection in the superheterodyne receiver. This trade-off is solved by using the dual down-conversion as shown in Fig 2.6, in which a second mixer is used to translate the first IF to a second IF, which is lower than the first one. Usually, this second IF is zero to avoid the creation of a second image.

Although the solutions presented above solve the image problem and the channel selection, the filters used in those solutions are off-chip, which is a significant disadvantage in comparison to the architectures that do not need off-chip components such as low-IF and zero-IF.

The zero-IF topology that is shown in figure 2.7 down-converts the signal directly to its baseband. Because the image frequency problem is absent in this topology, the

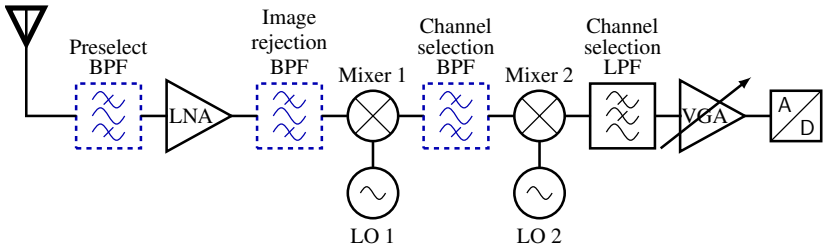


Figure 2.6: Dual IF Superheterodyne receiver chain.

receiver design is greatly simplified, and the off-chip image rejection filter is not needed anymore. Additionally, it performs the channel selection with a low-pass filter which can be done on-chip using either an active or passive filter topology. In comparison to the superheterodyne, the zero-IF architecture has less mixing spurs. Thanks to those advantages, the zero-IF architecture is considered superior to the superheterodyne [80].

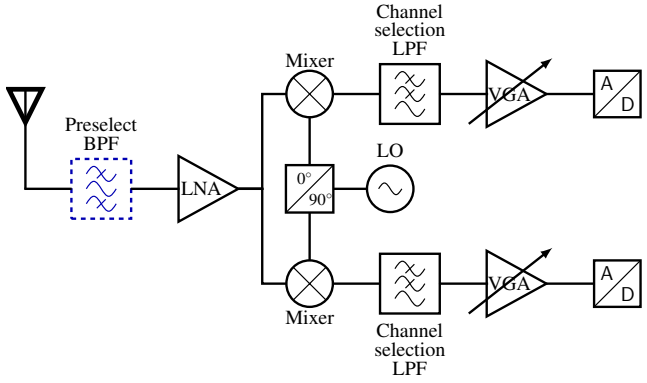


Figure 2.7: Zero-IF receiver chain.

The zero-IF receiver also has problems such as LO leakage, DC offsets, even-order distortion, I/Q mismatch, and flicker noise, which can significantly constrain the receiver performance.

The zero-IF receiver emits part of its LO power from the antenna. The LO couples to the antenna through the parasitic capacitances of LNA and mixer and the substrate due to the LO on-chip inductors. Although LO leakage occurs in superheterodyne receivers, it is not an issue since the LO frequencies are outside the operation band. Another consequence of the LO leakage is the DC offset. The portion of the LO signal coupled to the input is down-converted together with the input signal that creates a strong DC component as shown in figure 2.8a. Thus, the baseband circuits must include DC offset

cancellation, for the DC component can saturate them. The I/Q mismatch is another issue that plagues the zero-IF receiver. Although the superheterodyne also suffers from I/Q mismatch, the mismatch is larger at the zero-IF receiver due to the higher frequency of the LO. This mismatch is fixed by using calibration at the clock generation.

The two main problems for the zero-IF receiver are the even-order distortion and flicker noise that are shown in figure 2.8c and figure 2.8b respectively. The former is created either by two blockers or by the envelope. When those two blockers pass through the LNA, they are going to experience a nonlinear amplification that creates low-frequency components such as $f_1 - f_2$, $2 \times (f_1 - f_2)$, and $3 \times (f_1 - f_2)$, i.e., intermodulation products. Asymmetries in the mixer allow for such components to appear into the baseband without frequency translation that corrupts the down-converted signal, that is called mixer feedthrough. Additionally, if the blockers are closely spaced, the intermodulation component may fall onto the channel. Moreover, the even order distortion can demodulate the envelope either of the signal or a strong blocker. Due to the mixer feedthrough, those components will also appear at the baseband and corrupt the signal. Consequently, the IIP2 is a major concern for the zero-IF receiver.

Flicker noise is another significant issue for the operation of the zero-IF receiver since it is proportional to $1/f$, and the IF is around zero. Not only is the signal corrupted by the flicker noise but also the mixers can generate more flicker noise. Although the corner frequency of the flicker noise is reduced by raising the gain of the LNA, it is still difficult to use zero-IF receivers for standards with narrow channel bandwidth.

Despite being a good way to eliminate the image, the zero-IF architecture still has issues such as the even order distortion, DC offset, and flicker noise which might harm the receiver performance. Another method to eliminate the image without filtering is using either the Hartley or the Weaver architecture. Indeed, these architectures are very similar. First, they use a quadrature mixer, which performs Hilbert's transform, to separate the signal and its image. After that, another Hilbert's transform is applied either in the in-phase (I) path or in the quadrature (Q) path. By adding the result, the image is entirely canceled. The difference between the Hartley and the Weaver architectures is that the former uses an RC-CR network to perform the second Hilbert's transform, whereas the latter uses a second quadrature mixer to do it. Therefore, the Weaver architecture is more robust to mismatch.

The low-IF receivers are an evolution from the zero-IF. Instead of placing the LO frequency at the center of the channel, like in the zero-IF receiver, the LO frequency is placed at the edge of the channel in the low-IF receiver. Therefore, the edge of the channel is at 0 Hz instead of the center. Because the signal carries little information near the channel edge, it suffers less corruption from flicker noise. Moreover, the DC offsets can be removed using on-chip high-pass filters. Those filters are feasible at low-IF receiver due to the nonzero IF.

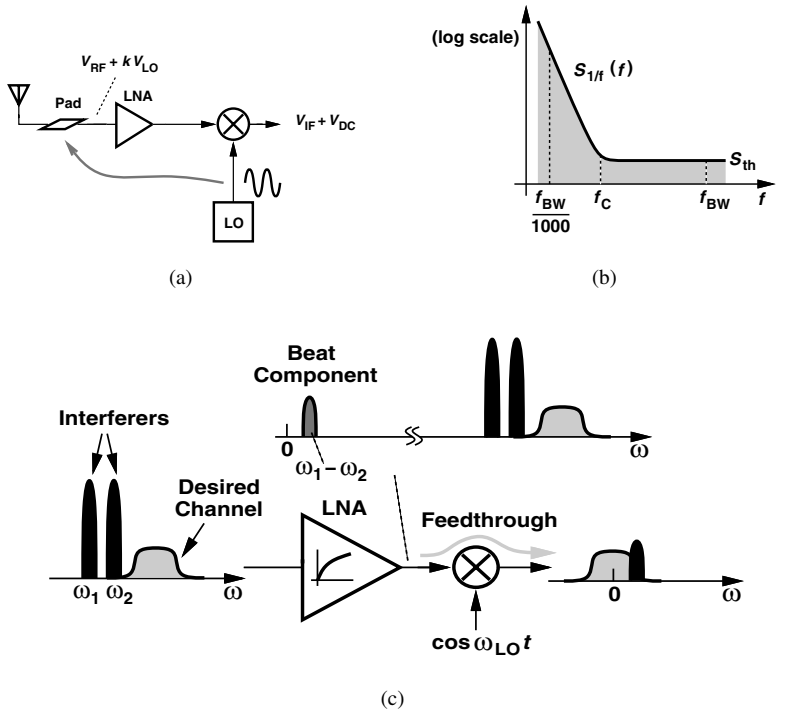


Figure 2.8: (a) DC offset, (b) spectrum of flicker noise, and (c) the effect of even-order distortion components [80].

Unlike the zero-IF receiver, the low-IF has the image issue. Since the image falls in the adjacent channel, it cannot be eliminated with on-chip filters. Thus, the image is rejected similarly to the Weaver topology but for the second Hilbert's transform which is implemented in the digital domain. Indeed, the down-conversion and channel selection are equal on both the zero-IF and low-IF receivers, yet the ADC of the low-IF receiver needs to support a bandwidth twice that of the zero-IF, which then results in an increase in the ADC power consumption.

In a nutshell, the superheterodyne receiver is not the most common choice for receiver due to the need for external filters to perform image filtering and channel selection. The zero-IF receivers are a possible choice for applications with a wide channel because the portion of information located around 0 Hz that is going to be corrupted is small. Despite the image issue, the low-IF receivers are the best choice for narrow channel application because the flicker noise corrupts only the edge of the channel.

2.5 This specification and the state-of-art of spectrum sensing receivers

The specification of the spectrum-sensing (SS) receiver needs to allow for the detection of signals from the standards WRAN, WiMax, and LTE. Therefore, each parameter of the specification presented in table 2.8 is the worst case of those three standards.

Table 2.8: Spectrum-sensing receiver specification.

Sensitivity [dBm]	NF [dB]	IIP3 [dBm]	IIP2 [dBm]	IP1dB [dBm]	Gain [dB]
-111	6	-0.6	29.5	-13.2	$28.9 \sim 115$

Since the receiver specified above has never been realized in silicon, it is impossible to establish a comparison with the state-of-art SS receivers. However, by verifying if the SS receivers published in the last ten years achieve this specification or not, it is possible to see how challenging it would be to achieve such performance. Table 2.9 summarizes this.

The first challenge is the RF bandwidth since keeping the performance over a wide band is a complex task. The receivers of [59, 52] achieve high frequencies, above 3 GHz, but they do not cover the low frequencies. On the other hand, the receivers of [3, 55, 7] cover the low frequencies, but [3, 7] are unable to work above 1.5 GHz, and [55] is unable to work above 2.5 GHz.

The majority of the published SS receivers are unable to achieve a sensitivity below - 110 dBm. In fact, only the receivers in [3, 85] comply to this requirement. The circuits using analog detection methods [78, 52, 7] hardly achieve sensitivity values better than -80 dBm. Hence, the utilization of digital detection methods is advisable since those methods use sophisticated algorithmics that identifies the signal even if it is buried in noise.

In conclusion, the design of such wideband receiver is a very challenging task. The receiver in [3] is the one with performance closest to our requirements, but it is unable to cover the CR operation, with the quoted performance, at frequencies higher than 1.5 GHz. A possible solution is to split the band into smaller parts, like in [15].

Table 2.9: Performance of state-of-art SS receivers.

	Sensitivity [dBm]	NF [dB]	IIP3 [dBm]	IIP2 [dBm]	IP1dB [dBm]	RF Band [GHz]
[78]	-74	N/A	N/A	N/A	N/A	0.6-0.614
[3]	-130* ✔	4-17 ✔	17-24 ✔	N/A	-7✔	0.05-1.5
[85]	-113* ✔	11	2 ✔	N/A	N/A	0.7-2.6
[59]	-100	N/A	-38	N/A	N/A	0.6-3.4
[55]	-83	5-8 ✔	-11	38 ✔	N/A	0.03-2.4
[52]	-40	N/A	N/A	N/A	N/A	0.25-3.25
[7]	-83	N/A	13.4 ✔	N/A	0.2✔	0.05-1.25

* Calculated from the data presented, considering a SNR of -20 dBm.
✔ It attends the proposed specification.

2.6 Budget of the SS receiver specification

After the definition of the receiver specification, the budget of each block is calculated in such way that the specifications of these blocks are well balanced.

First, the receiver architecture is selected. Since a 50 MHz channel is chosen for this application, the receiver can use either the zero-IF or the low-IF architecture. The superheterodyne architecture has been discarded due to the need for external components. Therefore, this receiver will be composed by LNA, mixer, and VGA as shown in figure 2.7 and the main topic of discussion are the LNA and mixer.

The receiver is designed to detect signals from -111 dBm up to -25 dBm, so it must have a variable gain that accommodates these signal powers. In addition to providing the gain variation, the baseband VGA deliveries the major part of the receiver gain. As a result, the gain of the LNA and mixer are minimized, avoiding the signal compression in the following blocks. This gain distribution allows the receiver for a high linearity.

The mixer can be either passive or active. The passive mixer has the advantage of being high-linear but without gain. Conversely, linearity may be an issue for the active mixer unless some harmonic cancellation is used, but a gain moderately high and NF reasonably low are feasible. Thus, the selection of the mixer is a critical decision in the receiver design.

Indeed, if the passive mixer is selected, it is necessary either to place a transconductor between the LNA and mixer to drive the latter or to convert the LNA into a LNTA that incorporates the transconductor function and drives the passive mixer. The first solution jeopardizes the receiver linearity unless the transconductor is extremely linear since the LNA amplifies the signal that arrives at the input of the transconductor. The second solution gives a better linearity than the first one due to the removal of the intermediate stage. Additionally, LNTAs can achieve an IIP3 up to 20 dBm as was reported in [69]. The NF, however, is an issue because neither the LNTA nor the passive mixer has a very low NF. For example, the high-linear LNTA reported in [69] has a 6 dB NF.

In both solutions, the passive mixer limits the NF of the receiver. The NF of the passive mixer can be enhanced by reducing the length or increasing the width of the transistors so that it lowers the on-resistance of the switches. Thus, the passive mixer may be a good option for newer CMOS technologies such as 65, 40, or 28 nm. However, since this design will be done in 130 nm CMOS, which is a mature technology, the passive mixer hardly achieves a low NF.

The active mixer seems to be a better design choice than the passive. First, it has a lower NF and a higher gain than those of the passive mixer. Second, it is preceded by a simple LNA, which can use noise-canceling topologies that are already prone to wideband applications such as this receiver. Although those LNAs are not as linear

as the LNTA, they still achieve an IIP3 around 0 dBm in addition to an NF below 3 dB [17, 76, 84, 13, 103, 54]. Finally, the active mixer can achieve a reasonable high linearity by using harmonic canceling techniques. The active mixers reported in [72, 92, 16] reached IIP3 and IIP2 above 10 dBm and 80 dBm respectively. Therefore, the budget of the specification has been done considering an LNA followed by an active mixer.

The specification of noise and linearity of the blocks are calculated with 2.5 and 2.11 respectively. Replacing the data of table 2.10 into these equations returns an NF, IIP3, IIP2, and IP1dB of 4.9 dB, -0.5 dBm, 30 dBm, and -12.5 dBm respectively. These results achieve the specification of the receiver.

Linearity is the most restrictive figure, in particular for the LNA and mixer. Although the linearity requirements of the VGA appear to be extremely severe, they are easier to achieve than those of the LNA and mixer because the channel selection filter before the VGA that attenuates the interferers. On the other hand, LNA and mixer need to withstand unattenuated interferers. Thus, the gain and NF requirements of those blocks are relaxed so that they can achieve their linearity requirements.

Table 2.10: Budget of the specification.

	NF [dB]	IIP3 [dBm]	IIP2 [dBm]	IP1dB [dBm]	A_p [dB]
LNA	3.5	4	35	-12	12
Mixer	10	14	60	12	8
VGA	15	30	60	20	$10 \sim 97$

After a preliminary budgeting, the SS receiver has been simulated using behavioral models. In contrast to the cascade equation, the output and input impedances can be specified in these simulations which give a more precise estimation for the budget. The results of voltage, NF, IP1dB, and IIP3 are presented in figure 2.9. The IIP2 was not simulated because the mixed signal Verilog models in the Cadence environment do not have this parameter. Despite the addition of the impedances, the simulated results are similar to the calculated ones.

2.7 Conclusion of the chapter

In this chapter, the specification of a wideband receiver for SS has been developed as part of the UFRGS Cognitive Radio Project. The CR was a topic of interest in the 2000's, but the interest has faded over the following decade due to the lack of commercial applications and the growing interest in SDR.

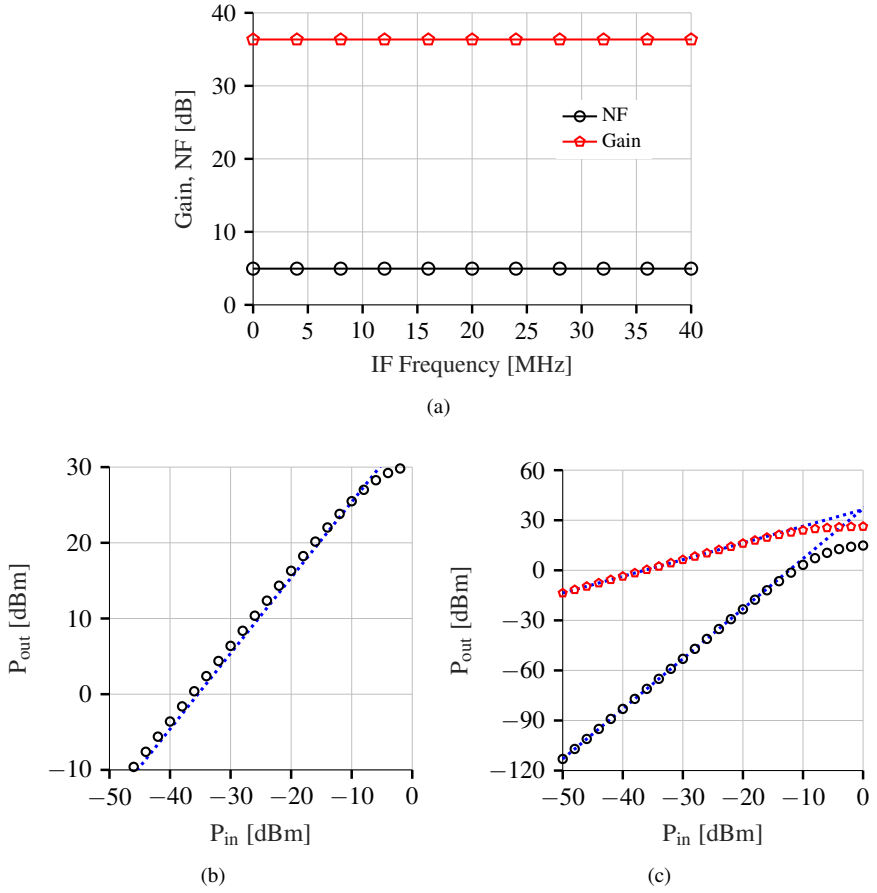


Figure 2.9: Behavioral simulation results of (a) voltage gain and NF, (b) IP1dB, and (c) IIP3.

The top-level and the block-level specifications were discussed in this chapter, but the specification has never been fully realized in silicon because the project was discontinued in 2013. Therefore, in order to evaluate the feasibility of this specification, we have checked which of the SS receivers published in the last ten years reached some of the specifications derived by the author. Due to the wide RF band, none of the SS receivers achieved the requirements. One way to overcome this limitation is to split the receiver in two, one for the sub-1 GHz band and another one for the upper-1 GHz band.

In a nutshell, the implementation of an SS receiver with such wideband is not worthwhile because it is extremely complicated to keep the performance in such wideband and it lacks commercial application. Despite the lack of implementation, this

study offered an overview of the challenges in the design of multi-band/multi-standard receivers. For instance, the intent of designing wideband RF circuits remains in the following projects, but taking into consideration more restricted - and not so wide as 50MHz to 4 GHz - RF band.

Chapter 3

A Wideband Low Noise Variable Gain Amplifier in 130 nm CMOS

3.1 Introduction

The second project of this thesis addresses the design of a wideband low-noise variable-gain amplifiers (LNVGA) in 130 nm CMOS, which is a daunting challenge given the issues already discussed in the previous chapter.

Exploiting a wide range of bands in the same receiver, as required in multi-band/multi-standard radios, demands a flexible and programmable RF front-end [1]. In particular, the gain is a requirement that demands a lot of flexibility. For instance, the hypothetical multi-standard receiver discussed in chapter 2 requests a gain tuning range of 87 dB. In cases like that, where a broad gain tuning range is required, it is better to share the gain control between the blocks of the receiver rather than concentrate it on the baseband amplifier. Either the LNA or the mixer could perform this task, but the LNA is the best option because it is the first block in the receiver chain. Hence, by controlling its gain, the compression of the following blocks of the receivers could be avoided. Although variable-gain amplifiers (VGA) are a well-known solution for that purpose, they are rarely used at RF frequencies due to the difficulty of achieving a flat gain response up to GHz frequencies [83].

There are three possible methodologies to control the gain on the VGA: by tuning resistive elements, by tuning the bias voltage of one transistor, or by adding two signals

with a 180 degrees phase shift (phase cancellation). The resistive elements of the first methodology are usually replaced by transistors, which are biased in the triode mode of operation. And, the gain is controlled by changing the voltage at the gate of those transistors. This approach is applied in [98], and it achieves a significant gain control range (up to 60 dB gain variation). However, the transistors in triode are extremely noisy; thus, the noise figure of the circuit becomes prohibitively high. Moreover, the huge gain control range is achieved due to the utilization of multiple stages, that takes its toll on linearity. The second methodology, on the other hand, can achieve a low noise figure, as shown in [102, 27], yet these circuits are unable to get a large gain control range. The third methodology has been proposed in [82]. In addition to the large gain tuning range, this technique achieves an IIP3 above 0 dBm. However, in spite of these good features, the phase cancellation technique, as presented in [82], is unable to amplify the signal, so it suffers from a high noise figure which is undesirable in a receiver.

The above-mentioned VGAs achieve either a low-noise figure or a large gain tuning range. On the contrary, our low noise variable gain amplifier (LNVGA) achieves both of them. The LNVGA is composed of two-stages. The first one uses noise cancellation, achieving a low noise figure within a wide bandwidth. And the second one uses phase cancellation by which a large gain tuning range is achieved in a single stage. Moreover, the proposed balun achieves a small imbalance, which is crucial to the performance of the second stage.

This chapter is organized as follows. In section 3.2 the state-of-art RF VGAs are presented. Section 3.3 describes the characteristics of the proposed and designed circuit. The simulation results are discussed in sections 3.4 and 3.5. Section 3.6 shows the measurements of the fabricated circuit. Finally, Section 3.7 summarizes the chapter's contribution.

3.2 Previous wideband VGAs

The three most common methods to control gain in amplifiers are to employ variable resistive elements, to change the transistors bias voltages, which change their operating points, and to add two 180° out-of-phase signals, i.e. phase cancellation. Each one of these techniques has its advantages and drawbacks.

A 3-stage distributed amplifier is presented in [102]. In addition to a wide band, this type of topology provides a good input and output matching. The gain variation is added to this topology by changing the bias of the cascode transistors (M2, M4, and M6), which are presented in figure 3.1. When the bias of the cascode is reduced, the transistors M1, M3, and M5 change their operation point from saturation to triode which changes their transconductance. Therefore, the gain changes.

Although this VGA achieves a 7 GHz band and consumes only 9 mW, it achieves a small gain tuning range of 18 dB. The minimum transconductance of M1, M3, and M5 set the bottom gain. Meanwhile, the number of stages sets the upper gain. Thus, the gain tuning range can only be enhanced by increasing the number of stages. However, this kind of circuit uses too many inductors that increase the circuit area. The VGA of [102] occupies an area of 1.16 mm^2 due to the requirement of integrating eight inductors of few nH each.

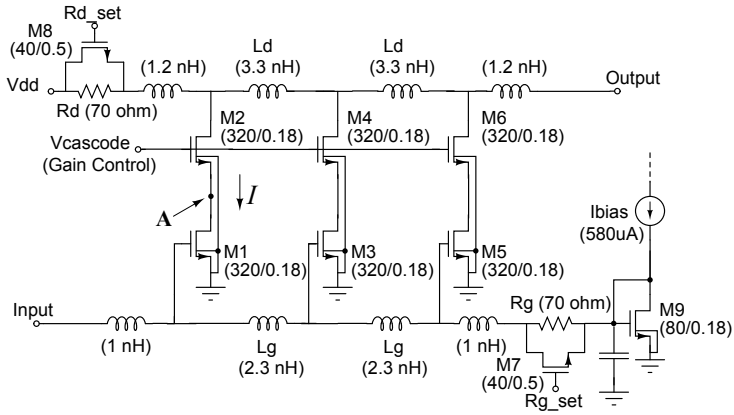


Figure 3.1: 3-stage distributed VGA proposed in [102].

The phase cancellation technique was proposed in [82]. First, the circuit in figure 3.2 splits the incoming signal into two 180° out-of-phase signals. Then, these signals pass through two identical triode transistors (M1 and M2) that attenuate them. Finally, the signals are added at the load resistance. The gain is controlled by changing the bias of M2 that changes their resistance, while the bias of M1 is kept fixed. When the bias of M1 and M2 are equal, the gain is minimum since the equally attenuated signals cancel each other. On the other hand, when the bias of M2 is 0, the gain is maximum since only the signal that passes through M1 arrives at the output.

This approach achieves a gain control range around 28 dB, but the NF seems to be high due to the transistors in triode. The maximum gain is limited by the attenuation of M1, and the minimum gain is restricted by the mismatch between M1 and M2 in addition to the imbalance of the active balun. Thus, the maximum can only be improved by replacing M1 and M2 for another circuit that gives a higher gain. The minimum, on the other hand, cannot be further improved. Indeed, the minimum gain reported in [82] is the lowest reported so far. In addition to the large gain control range, this VGA is extremely compact. Since the circuit is inductorless, it occupies an area of only 0.05 mm^2. However, it consumes 18 mW of power that is two times more than the VGA reported in [102]. Additionally, this VGA is unable of amplification, so its noise

figure is inherently high. Therefore, this VGA is useless on a receiver unless preceded by an LNA.

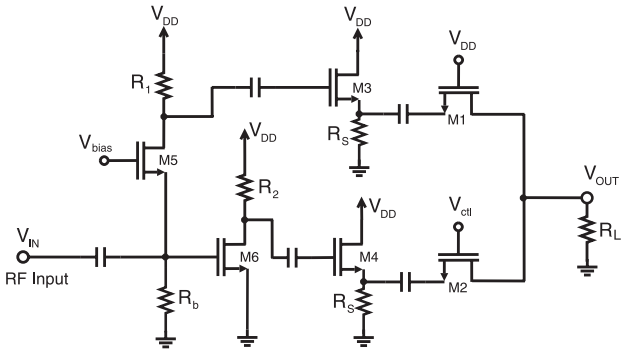


Figure 3.2: VGA proposed in [82] that uses phase cancellation.

The VGA presented in [98] targets baseband application for a 60 GHz receiver. It uses a chain of four Cherry-Hooper amplifiers that are equal but for their input capacitance which is reduced by a factor of two at each stage to enhance the bandwidth. In addition, the DC-offset cancellation network further enhances the circuit bandwidth. The VGA achieves a 2.2 GHz bandwidth without using inductors, resulting in a circuit area of 0.0135 mm^2.

The Cherry-Hooper amplifiers were modified by replacing their resistive shunt-feedback for two MOST, M3 and M4, biased in triode, as shown in 3.3. These MOSTs work as variable resistors and their gate voltage controls their resistance value. Since each one of the amplifiers has variable gain, the four stages combined provides the largest reported gain tunning range, 60 dB. Furthermore, [98] presents the lowest reported power consumption, 2.5 mW.

Despite the good features described above, the VGA presented in [98] has a noise figure above 17 dB due to the transistors in triode. In addition, the multistage approach takes its toll on linearity. The compression point is as high as -55 dBm. Therefore, the circuit reported in [98] is only suitable for baseband applications.

Another VGA in which the gain is controlled by the bias of one transistor is presented in [27]. This circuit employs noise-canceling which reduces the overall NF to a minimum of 3.2 dB. Since noise-canceling LNAs are already prone to be wideband, this VGA covers a band from 1 GHz up to 5 GHz without the need of inductors. As shown in figure 3.4, the gain is controlled by changing the bias of M4.

Although this VGA has reported the lowest NF in comparison to the others, it has a small gain tuning range of 16 dB. Additionally, it has a high power consumption of

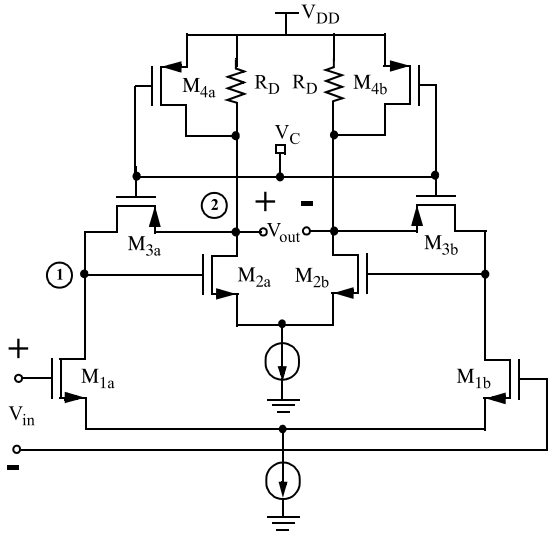


Figure 3.3: Cherry-Hooper VGA proposed in [98].

19 mW. In comparison to the VGA in [82], this VGA reports a much smaller gain, but with the same power consumption. Moreover, the NF degrades, reaching a maximum of 9 dB, as the gain reduces. On the bright side, this VGA occupies an area of only 0.0675 mm^2 due to its avoidance of integrated inductors.

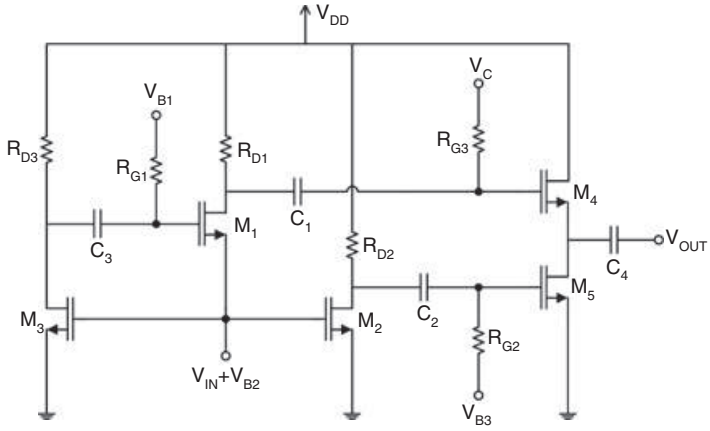


Figure 3.4: VGA proposed in [27].

In a nutshell, when the gain is controlled by changing the bias point of one or more transistors, the best NF results are achieved. However, those circuits did not produce a large gain control range. In contrast, when the gain is controlled by a transistor biased in triode, a considerable large gain tuning range is achieved, but it costs a high NF. The phase cancellation technique also allows for a reasonable large gain tuning range, but the high NF remains an issue to be solved.

The most recent published low-noise variable-gain amplifiers target the 5G bands [29, 94]. The LNVGA presented in [29] achieves a gain tuning range of 8 dB (18-26 dB) and 3.3-4.3 dB NF across 26-33 GHz frequency range. Meanwhile, the LNVGA presented in [94] covers the 5G bands from 68 to 96 GHz, acomplishing a 6.4 dB NF and 11 dB (29.6-18 dB) gain tuning range. The design of LNVGAs remains an interesting research topic, but the target band has shifted to higher frequencies, which changes completely the design constraints and the RF circuits design approaches to be used. This thesis has no focus on the 5G bands of modern interest, as it is motivated for SDR at microwave range, hence those LNVGAs at above 26GHz or above 60 GHz will not be discussed here.

3.3 Design of the proposed LNVGA

Two stages compose the LNVGA, as shown in figure 3.5a. The low noise amplifier (LNA) is the first stage that aims to provide a low noise figure (NF), an average voltage gain (A_v) and the input matching to a 50Ω signal source. The variable-voltage attenuator (VVA), the second stage, controls the gain and limits the LNVGA linearity. By controlling the gain, the LNVGA can increase the sensitivity when receiving a weak signal, whereas it avoids the signal compression when the received signal is too strong. Thus, the dynamic range of the LNVGA is enhanced.

The LNA uses a noise-cancelling topology [17, 57] that provides a low noise figure and input matching in a wide band. Since the noise-cancelling requires a secondary path to cancel the noise, the power consumption is higher than conventional LNAs. The utilization of g_m − boosting [91, 27] at M1 mitigates this drawback, for M1 is allowed for a lower transconductance.

The operation of the transistors in weak inversion greatly reduces the power consumption of the circuit. However, due to the size of the transistors in WI, the circuit bandwidth is reduced. This compromise between bandwidth and power consumption can be broken by using inductors or distributed amplifiers although the former increases the circuit area and the latter degrades linearity. Thus, the LNVGA uses two inductors and transistors in moderate inversion (MI), for the best compromise between power consumption and bandwidth. Bias the transistors in MI also offers other two advantages, low noise [35] and good linearity [90].

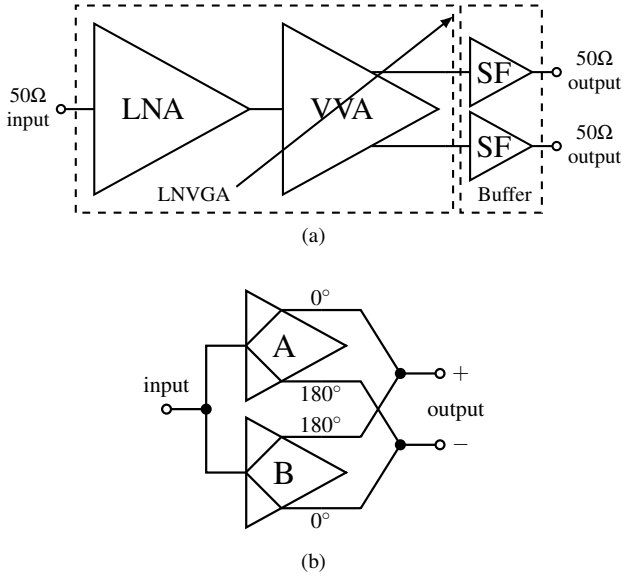


Figure 3.5: (a) Block diagram of the VGA circuit and the measurement buffer. (b) VVA composed by two baluns.

Figures 3.6 and 3.7 show those two inductors. The L_{S2} improves the high-frequency input matching that is damaged by the capacitances of M2A. Meanwhile, L_{D2} extends the bandwidth of the LNA, which is limited by the input capacitance of the VVA.

The noise-cancelling cancels both the noise and the nonlinear terms of the transistor [17]. Since M1 and M3 are in the cancellation loop, their contribution to noise and nonlinearity is reduced. Hence, the noise and nonlinearity of M2A and M2B are predominant. After some investigation, we conclude that M2A limits the noise figure, while M2B bottlenecks linearity.

Two active baluns compose the VVA, as shown in figure 3.5b. Their output terminals are cross-connected, so the out-of-phase signals are added at the output node, which implements the phase cancellation [82]. The LNVGA obtains the maximum gain when the balun A is off, and the balun B is on. Meanwhile, by fully turning on both baluns, the gain of the LNVGA is minimized since the signals are canceled at the output node.

The LNVGA is single-to-differential owing to the need of out-of-phase signals to implement the phase cancellation and to easily integrate with a differential mixer. The VVA uses a common-source transistor at the input, so its input impedance is much higher than the output impedance of the LNA, which maximizes the voltage gain.

The phase cancellation strongly relies on the signal imbalance of the balun. Ideally, the

signal at the output of the balun has the same magnitude, and their phases are shifted 180°. Any deviation from this ideal situation is called imbalance. Since the signal will be fully canceled at the output only if the imbalance is satisfactorily small, it is mandatory to minimize the imbalance.

A well known active balun is the differential pair in which one of the inputs is AC grounded. Ideally, the RF signal goes through both differential branches with the same magnitude, but out-of-phase. However, the balance of the differential output is limited by the finite parasitic conductance of the tail transistors (M8 and M9) and the capacitance of the differential pair, mainly C_{gd}. The solution is to increase the transconductance from the differential pair and the channel length of the tail transistors, yet the output balance remains limited. Hence, a cross-connected pair of transistors (M5 and M7) have been added to the differential pair in order to reduce the output imbalance, which is shown in figures 3.6 and 3.7. Consequently, the gain tuning range of the LNVGA is enhanced.

Finally, two LNVGAs have been designed and prototyped. The first and the second design are shown in Fig 3.6 and Fig 3.7 respectively. The principal difference between them is that the LNVGA I uses an active inductor on the VVA to extend its bandwidth [100, 101]. However, since these active inductors increase the LNVGA noise figure, we remove them on the LNVGA II.

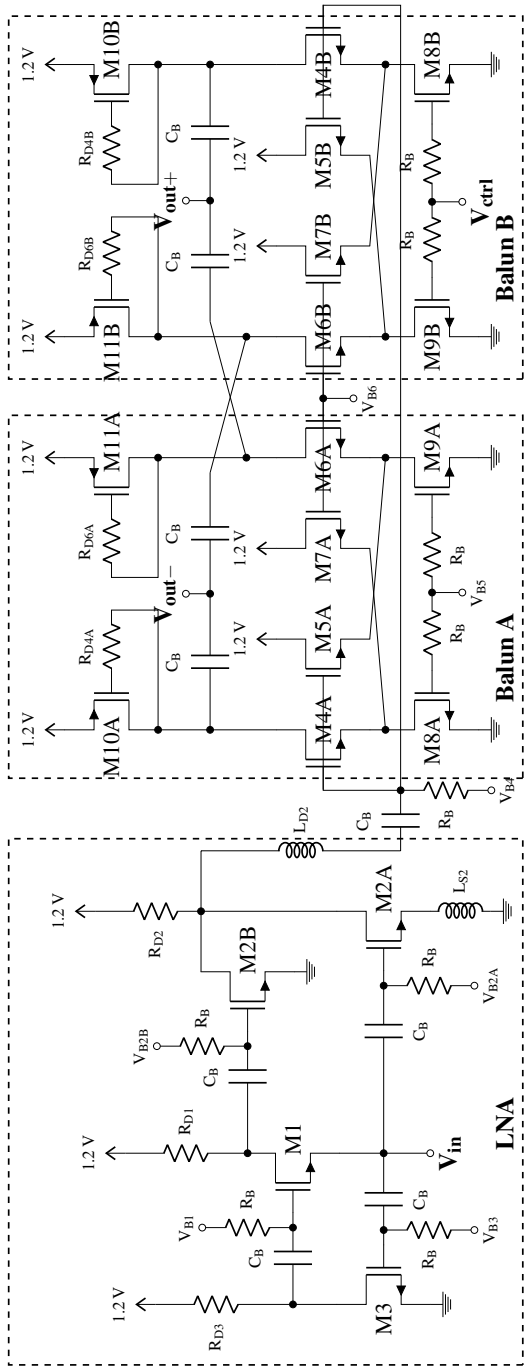


Figure 3.6: The schematics of the LNVGA I.

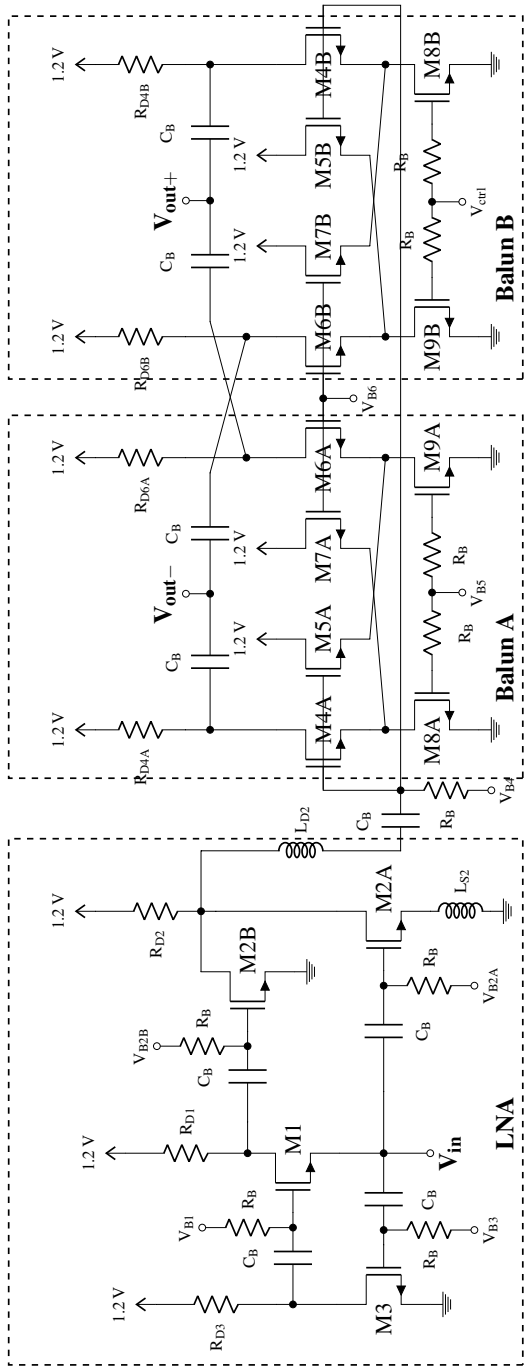


Figure 3.7: The schematics of the LNVGA II.

3.3.1 Input Matching

The input impedance of the LNVGA is chiefly defined by the transconductance of M1 and the loop gain through M3. At low frequencies

$$Z_{in,LNVGA} \approx \frac{1}{g_{m1}\left(1+g_{m3}R_{D3}\right)}, \tag{3.1}$$

where g_{m1} is the transconductance of M1 and g_{m3} is the transconductance of M3. That impedance must match to the 50Ω source impedance (R_S).

However, since M2A has been biased in MI which increases the size of the transistor, the parasitic capacitances become meaningful and worsen the input matching at high frequencies. The input impedance high-frequency equation is approximated by

$$Z_{in,LNVGA}(s) \approx \left(\frac{g_{ds1}R_{D1}+1}{G_{m1}+g_{ds1}}\right)\frac{C_{gs2A}L_{S2}s^2+L_{s2}g_{m2A}s+1}{C_{gs2A}L_{S2}s^2+\left[g_{m2A}L_{S2}+\left(\frac{g_{ds1}R_{D1}+1}{G_{m1}+g_{ds1}}\right)C_{gs2A}\right]s+1}, \tag{3.2}$$

where $G_{m1} = g_{m1}\left(1+g_{m3}R_{D3}\right)$, g_{ds1} is the drain-source conductance of M1, and C_{gs2A} is the gate-source capacitance of M2A.

Fig 3.8 shows the evaluation of the input impedance and input reflection coefficient (S11) based on (3.2). The inductor connected to the source of M2A solves the input mismatch at high frequencies. An S11 below -10 dB is achieved by using a 1 nH inductor. In addition to enhancing the S11, L_{S2} degenerates the source of M2A that reduces the gain, while it improves linearity. Since the minimization of the noise of M2A is the priority, it is not possible to use inductors larger than 500 pH. Moreover, this value of inductance is reachable with a minimum area inductor, $100x100\mu m^2$. Hence, L_{S2} has been set to 460 pH which gives a good compromise between the features presented above.

3.3.2 Noise Figure

The noise analysis has been separately done for the LNA and VVA. After that, the overall NF is calculated with the Friis equation. Hereafter, the notation of noise factor (F) will be used. This notation is related to NF by $NF = 10\log_{10}F$.

Because the LNVGA is a two stage circuit, the first stage chiefly defines the noise figure (NF), and the noise contribution of the following stages are mitigated by the gain of the first one. By using the Friis equation, the noise factor of the LNVGA is

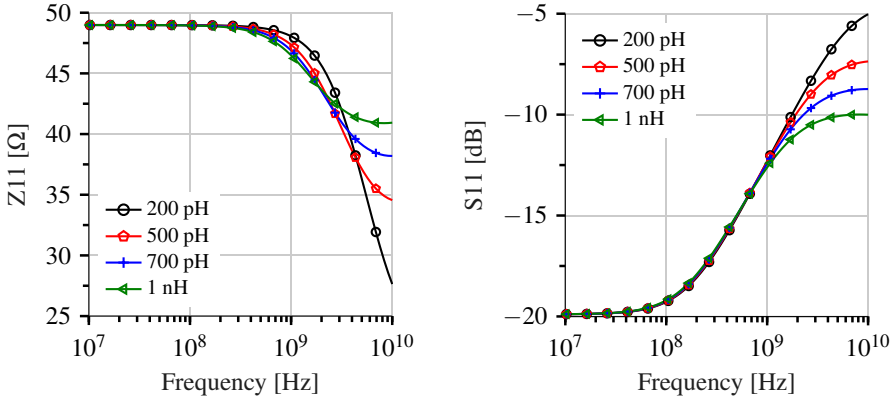


Figure 3.8: The calculated (a) input impedance and (b) S11 of the LNVGA.

calculated as

$$F_{LNVGA} = F_{LNA} + \frac{F_{VVA} - 1}{\left(\frac{R_{in,LNA}}{R_{in,LNA} + R_S}\right)^2 A_{V,LNA}^2 \frac{R_S}{R_{out,LNA}}}, \tag{3.3}$$

where $R_{in,LNA}$ is the LNA input resistance, $A_{V,LNA}$ is the LNA voltage gain, and $R_{out,LNA}$ is the LNA output resistance. Thus, we will focus on the noise contribution of the LNA.

The noise factor of the LNA is approximated as the sum of the noise factor of each component of the LNA,

$$F_{LNA} \approx 1 + \sum_j \frac{\overline{V_{n,j|out}^2}}{\overline{V_{n,R_S|out}^2}} = 1 + \sum_j F_j, \tag{3.4}$$

where j are the circuit components that add noise to the system, i.e., M1, M2A, M2B, M3, R_{D1}, R_{D2}, R_{D3}.

The noise of M1, M3, and R_{D3} are completely cancelled if

$$\frac{g_{m2A}}{g_{m2B}} = \frac{R_{D1}}{R_S} \tag{3.5}$$

as shown by

$$F_{M1} = \frac{\left(\frac{\gamma}{\alpha}\right) g_{m1} R_S R_{D1}^2 \left(\frac{g_{m2A}}{R_{D1}} - \frac{g_{m2B}}{R_S}\right)^2}{(g_{m2A} + G_{m1} g_{m2B} R_{D1})^2}, \tag{3.6}$$

$$F_{M3} = \frac{\left(\frac{\gamma}{\alpha}\right) g_{m3} R_S g_{m1}^2 R_{D1}^2 R_{D3}^2 \left(\frac{g_{m2A}}{R_{D1}} - \frac{g_{m2B}}{R_S}\right)^2}{(g_{m2A} + G_{m1} g_{m2B} R_{D1})^2}, \tag{3.7}$$

and

$$F_{R_{D3}} = \frac{R_S R_{D3} g_{m1}^2 R_{D1}^2 \left(\frac{g_{m2A}}{R_{D1}} - \frac{g_{m2B}}{R_S}\right)^2}{(g_{m2A} + G_{m1} g_{m2B} R_{D1})^2}, \tag{3.8}$$

where γ and α are the noise parameters and R_S is the source resistance which must be equal to $1/G_{m1}$.

Consequently, the noise factor of the LNA is reduced to

$$F_{LNA} = 1 + \left(\frac{\gamma}{\alpha}\right)\left(\frac{1}{g_{m2A} R_S} + \frac{g_{m2B}}{g_{m2A}^2 R_S}\right) + \left(\frac{g_{m2B}}{g_{m2A}}\right)^2 \frac{R_{D1}}{R_S} + \frac{1}{g_{m2A}^2 R_S R_{D2}}. \tag{3.9}$$

Additionally, the noise of M2B is reduced by the gain of $G_{m1} R_{D1}$ and the noise of the resistors are small. Therefore, M2A becomes the main noise contributor of the LNA.

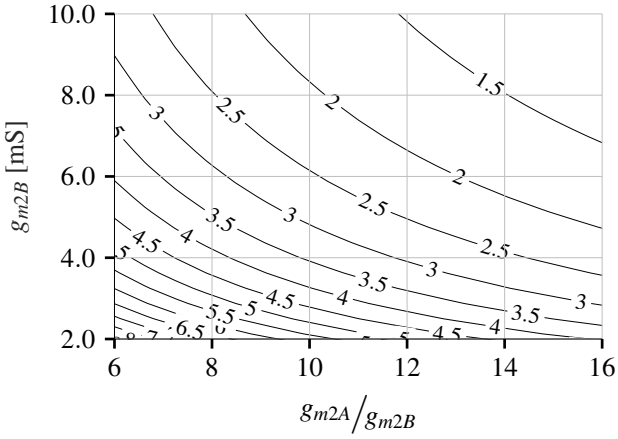


Figure 3.9: LNA NF calculated for different values of g_{m2A}/g_{m2B}, at $\gamma = 4/3$ [53], $\alpha = 0.8$ [53].

The noise cancellation happens whenever the condition (3.5) is followed. However, the noise factor of M2A and M2B change for different g_{m2A}/g_{m2B}. Figure 3.9 presents the calculated results for the NF, where g_{m2A} and g_{m2B} are the design variables.

The values of g_{m2A} and g_{m2B} must be correctly set in such way that minimizes the NF and does not harm other design figures. For example, the size of M2A will damage the S11 at high frequency as previously discussed. Moreover, a large M2B will shift the pole at $1/R_{D1}C_{gs2B}$ to low frequencies due to the increase of C_{gs2B}. The transconductance g_{m2B} also moves to low frequencies the pole mentioned above since g_{m2B} needs to be proportional to R_{D1} to keep the noise cancellation condition. Additionally, since every signal was amplified by M1 before reaching M2B, g_{m2B} may reduce the LNA linearity. Finally, we chose $g_{m2A}/g_{m2B} = 14$ and $g_{m2B} = 5\ mS$. This combination gives a noise figure around 2 dB and M2B is harmless to linearity due to the small g_{m2B}.

Even though the gain of the LNA reduces the noise contribution of the VVA, the latter remains a high noise contributor. The noise factor of the first and second VVAs when the Balun B is turned off is given by

$$F_{VVA1} = 1 + \left(\frac{\gamma}{\alpha}\right)\left(\frac{1}{2R_S g_{m4}} + \frac{1}{2R_S g_{m5}} + \frac{g_{m8}}{2R_S g_{m5}^2} + \frac{g_{m11}(g_{m4}+g_{m5})^2}{2R_S g_{m4}^2 g_{m5}^2}\right) + \frac{R_{D4} g_{m11}^2 (g_{m4}+g_{m5})^2}{2R_S g_{m4}^2 g_{m5}^2} \tag{3.10}$$

and

$$F_{VVA2} = 1 + \left(\frac{\gamma}{\alpha}\right)\left(\frac{1}{2R_S g_{m4}} + \frac{1}{2R_S g_{m5}} + \frac{g_{m8}}{2R_S g_{m5}^2}\right) + \frac{(g_{m4}+g_{m5})^2}{2R_S R_{D4} g_{m4}^2 g_{m5}^2}, \tag{3.11}$$

respectively. These equations have been simplified thanks to the circuit symmetricity. Hence, M4 = M6, M5 = M7, M8 = M9, and $R_{D4} = R_{D6}$. The active inductor not only adds another term to the noise equation but also increase the noise contribution of R_{D4} and R_{D6}. Hence, the NF of the LNVGA I is expected to be much larger that of the LNVGA II.

The previous statement is verified by replacing (3.10) and (3.11) in (3.3). Thus, the impact of each VVA on the LNVGA NF is quantitatively evaluated. Figure 3.10 and figure 3.3.2 show these results. By removing the active inductor, the NF of the LNVGA considerably improves. For example, the NF at the point where both g_{m4} and g_{m5} are 35 mS is 1.2 dB lower in the LNVGA II in comparison to the LNVGA I.

The LNVGA1 has been designed for an NF around 4.5 dB, whereas the LNVGA II has been designed for an NF below 3 dB. The LNVGA II NF can be reduced to values close to 2 dB, but the linearity reduction makes the NF improvement of little worth to the overall receiver performance.

When the Balun B is turned on, the overall NF will increase since more noise sources are included into the circuit and it works as an attenuator.

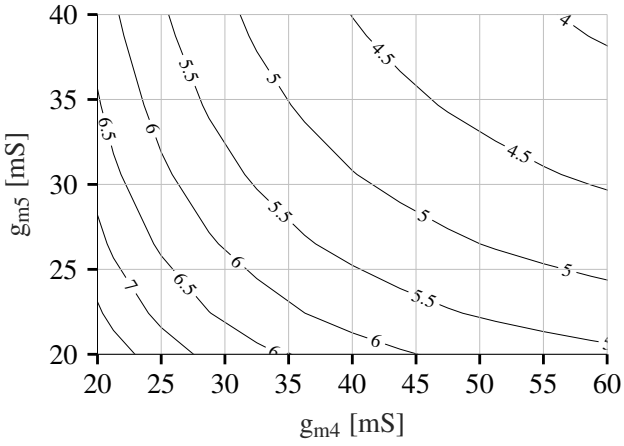


Figure 3.10: LNVGA NF calculated for the LNVGA I.

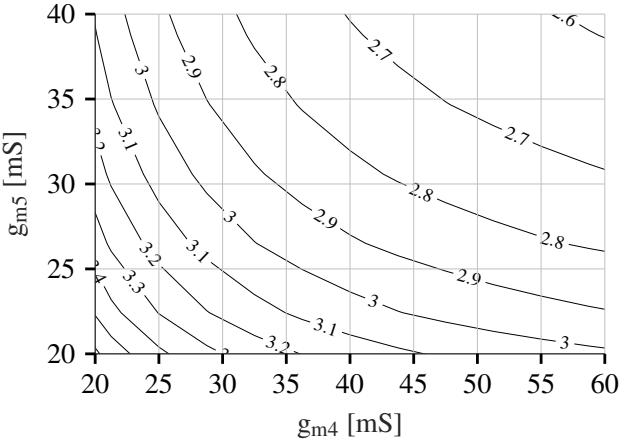


Figure 3.11: LNVGA NF calculated for the LNVGA II.

3.3.3 Voltage Gain

As it has been done in the NF analysis, the gain of the LNA and the VVA will be separately discussed. The interface between the LNA and the VVA is chosen for the maximum voltage gain, i.e. voltage matching. Hence, $R_{out,LNA} \ll R_{in,VVA}$. The transfer function of each circuit is calculated by applying KCL on the schematics of figure 3.6 and figure 3.7.

The LNA transfer function is given by

$$H_{LNA}(s) \approx -\frac{g_{m2A}R_{dout}\left(C_{gs1}C_{gs2b}R_{D1}R_{D3}s^2+(C_{gs1}R_{D3}+C_{gs2b}R_{D1})s+2\right)}{(C_{gs1}R_{D3}s+1)(C_{gs2B}R_{D1}s+1)(C_LL_{D2}s^2+C_LR_{dout}s+1)}, \quad (3.12)$$

where C_L is the input capacitance of the VVA, and R_{dout} is the parallel association of R_{D2}, g_{ds2A}, and g_{ds2B}. The circuit is considered under input matching and noise-canceling condition.

Setting the dominant pole, the inductor L_{D2} is crucial for achieving a large bandwidth and a flat gain. Although the two other poles are not dominant, they must be carefully placed so that they do not take the dominant pole position and reduce the circuit bandwidth. It is important to keep those secondary poles at frequencies much higher than that of the dominant pole. Hence, the best option is to minimize the capacitances C_{gs1} and C_{gs2B}.

The VVA is composed by two identical baluns that are presented in figures 3.6 and 3.7. The Balun A has a fixed gain, whereas the Balun B has a variable gain that is controlled by the voltage V_{ctrl}. When V_{ctrl} is 0 V, the Balun is turned off and the gain is maximum. By increasing V_{ctrl} the gain of the VVA drops, the gain is minimum when V_{ctrl} equals V_{b5}.

The transfer function of the VVA in figure 3.6 when the Balun B is turned off is given by

$$H_{VVA1}(s) \approx -\frac{\frac{g_{m4}(g_s+2g_{m5})}{g_s+g_{m4}+g_{m5}}(R_{D4}C_{gs10}s+1)\left(\frac{2C_{gs5}+C_S}{g_s+2g_{m5}}s+1\right)}{\left(\frac{R_{D4}C_{gs10}s+1}{C_{gs10}s-g_{m10}}C_Ls+1\right)(C_{gs10}s-g_{m10})\left(\frac{C_{gs4}+C_{gs5}+C_S}{g_s+g_{m4}+g_{m5}}s+1\right)}, \quad (3.13)$$

where g_s and C_S are the parasitic conductance and capacitance respectively that are associated with M8 and M9. As previously told, the active inductor creates both a zero and a pole, which has been used to extend the bandwidth of the circuit. However, the output impedance of the VVA is smaller with this active inductor that reduces the gain of the VVA.

The transfer function of the VVA figure 3.7 with the Balun B turned off is given by

$$H_{VVA2}(s) \approx -\frac{\frac{g_{m4}R_{D4}(g_s+2g_{m5})}{g_s+g_{m4}+g_{m5}}\left(\frac{2C_{gs5}+C_S}{g_s+2g_{m5}}s+1\right)}{(R_{D4}C_Ls+1)\left(\frac{C_{gs4}+C_{gs5}+C_S}{g_s+g_{m4}+g_{m5}}s+1\right)}. \quad (3.14)$$

Apart from the output impedance, the transfer functions of both VVAs are similar. Due to the higher output impedance that increases the maximum gain, the second VVA achieves a larger gain tuning range than the first the VVA.

The proposed active balun uses the transistors M5 and M7 to reduce the output imbalance, yet this technique only tackles the imbalance due to the parasitic components of the tail transistors (M8 and M9). The imbalance caused by C_{gd4} is neglected because it only harms the circuit at frequencies outside our interest band. Moreover, since the load of the VVA does not affect the output imbalance, a generic load Y_L is considered for the imbalance analysis.

The transfer function of the positive branch of the balun needs to be equal to that of the negative branch so that the output will be balanced, i.e. the imbalance will be zero. The balun transfer functions of negative and positive branches are

$$H_{balun,n} \approx -\frac{g_{m4}(g_s+g_{m5})\left(\dfrac{C_{gs5}+C_S}{g_s+g_{m5}}s+1\right)}{Y_L(g_s+g_{m4}+g_{m5})\left(\dfrac{C_{gs4}+C_{gs5}+C_S}{g_s+g_{m4}+g_{m5}}s+1\right)} \tag{3.15}$$

and

$$H_{balun,p} \approx \frac{g_{m4}g_{m5}\left(\dfrac{C_{gs5}}{g_{m5}}s+1\right)}{Y_L(g_s+g_{m4}+g_{m5})\left(\dfrac{C_{gs4}+C_{gs5}+C_S}{g_s+g_{m4}+g_{m5}}s+1\right)}, \tag{3.16}$$

respectively.

The magnitude imbalance happens because $g_{m4}(g_{m5}+g_s) \neq g_{m4}g_{m5}$, so the magnitude imbalance is reduced if $g_{m5} \gg g_s$. Since M5 and M7 do not have a resistor connected to their drains, they can have a higher current without falling into the triode region, so the g_m of M5 and M7 will be larger than those of M4 and M6 and much larger than g_s. Hence, the magnitude imbalance is reduced.

The phase imbalance happens because $\frac{C_{gs5}+C_S}{g_{m5}+g_s} \neq \frac{C_{gs5}}{g_{m5}}$. Hence, the phase imbalance will be reduced if both $g_{m5} \gg g_s$ and $C_{gs5} \gg C_S$. First, instead of using one transistor at the tail, the proposed active balun uses two (M8 and M9), that reduces C_S by 50%. Additionally, M8 and M9 have been biased in strong inversion (SI), which further reduces the size of the transistors and also their capacitances.

3.3.4 Linearity

The MOSFET current can be represented by a power series on v_{gs}:

$$i_{ds} = g_1 v_{gs} + g_2 v_{gs}^2 + g_3 v_{gs}^3 + \cdots, \tag{3.17}$$

where g_1 is the transconductance (g_m), $g_2 = \frac{1}{2!}\frac{\partial^2 I_{DS}}{\partial V_{GS}^2}$, and $g_3 = \frac{1}{3!}\frac{\partial^3 I_{DS}}{\partial V_{GS}^3}$. The second order nonlinearities and the third order nonlinearities are represented by the second and the third element of the series respectively.

Figure 3.12 shows the simulated g_3 of the NMOS transistor. Due to the small g_3, it is common to bias the transistors in SI whenever high linearity is needed. However, this choice leads to a high power consumption. Moreover, there are some bias points in MI that have values of g_3 smaller than that in SI. Indeed, the values of g_3 are smaller within $15 \geq {}^{g_m}/_{I_D} \geq 20$ than their values in SI. There is even a bias point where $g_3 = 0$. By biasing the transistors close to this bias point, the IIP3 will be enhanced [90] in addition to reducing the power consumption. The third order distortion term can also be canceled by using two transistors biased in such way that their g_3 have an opposite polarity. Both techniques have been used in the design of the LNVGAs.

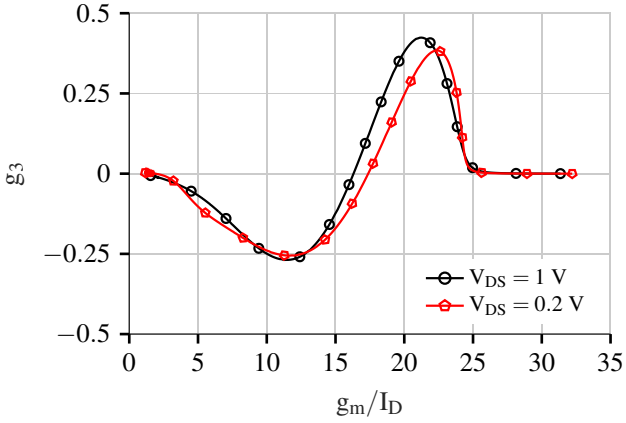


Figure 3.12: Simulated g_3 for a single NMOS transistor with L=120 nm.

Table 3.1 and table 3.2 show the bias points of the first and LNVGA II respectively. In the LNVGA I, the transistors M2A and M2B have been biased close to WI, whereas the same transistors in the LNVGA II have been biased in such way that their g_3 have an opposite polarity. In both prototypes the pair M4-M5 have been biased so that their g_3 cancel each other. The transistors M1 and M3 are not a concern in both LNVGAS since their nonlinear terms are canceled in the same way as the noise. As a result, the IIP3 of the LNVGA II is better than that of the LNVGA I despite its higher gain.

Table 3.1: LNVGA I transistors parameters.

	g_m/I_D	W (μm)	L (μm)
M1	15.82	35	0.12
M2A	18.52	400	0.12
M2B	18.73	10	0.12
M3	16.84	15	0.12
M4, M6	16.34	84.98	0.12
M5, M7	14.24	84.98	0.12
M8, M9	4.2	30	0.18
M10, M11	15.54	300	0.12

Table 3.2: LNVGA II transistors parameters.

	g_m/I_D	W (μm)	L (μm)
M1	13.2	20	0.12
M2A	16.9	360	0.18
M2B	17.86	30	0.13
M3	13.05	22	0.12
M4, M6	15.86	85	0.12
M5, M7	14.41	120	0.12
M8, M9	3.46	30	0.18

3.3.5 Measurement Buffer

The LNVGA has been designed to drive a capacitive load, which emulates the input of an active mixer, whereas every measurement equipment has a 50 Ω impedance. Thus, a highly linear source-follower buffer has been added to the LNVGA to provide the impedance matching with the measurement setup.

Since the buffer needs to have minimum effect on the circuit performance, thick-oxide 3.3 V transistors were used so that it achieves a high linearity. The linearity of the LNVGA, therefore, is unaffected by the buffer. However, the buffer still reduces the gain and increases the noise of the LNVGA. These issues are circumvented by de-embedding their effects from the measured results. Since the de-embedment methodology is well explained in [54], it will not be further discussed here.

In addition to reducing the power consumption, the class AB buffer (figure 3.13c) has superior linearity. For this reason, this buffer was used in the LNVGA I. However, the input capacitance of the PMOS transistor is considerably large which reduces the

bandwidth of the VVA. Hence, the buffer with an active load (figure 3.13b) was used in the LVNGA II. Although the buffer with an active load is not as linear as the class AB one, it is linear enough to avoid signal compression.

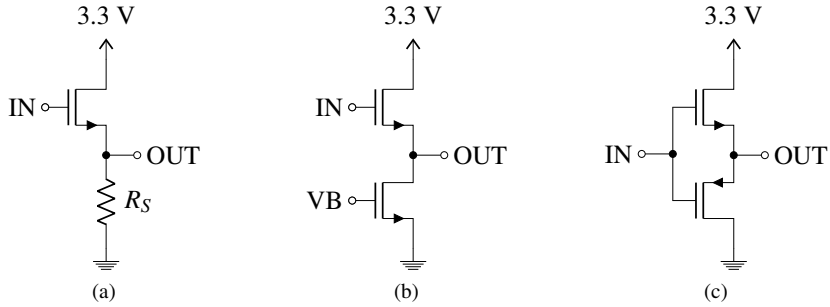


Figure 3.13: The measurement buffers using (a) source followers with a passive load, (b) source follower with an active load, and (c) class AB source followers.

3.4 Simulation Results

Even though both LNVGAs have similar topologies, the design options in each one of them are different. Those differences are apparent in the results. Figure 3.14 and figure 3.15 compares the S11, the NF, and the voltage gain of the circuits.

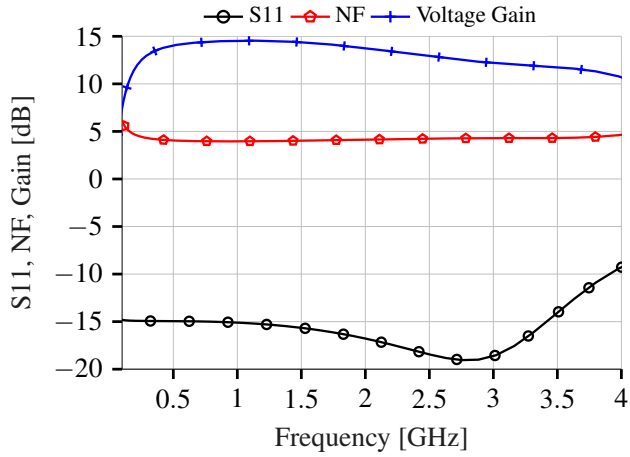


Figure 3.14: S11, NF, and Voltage Gain post-layout simulation results of the LNVGA I.

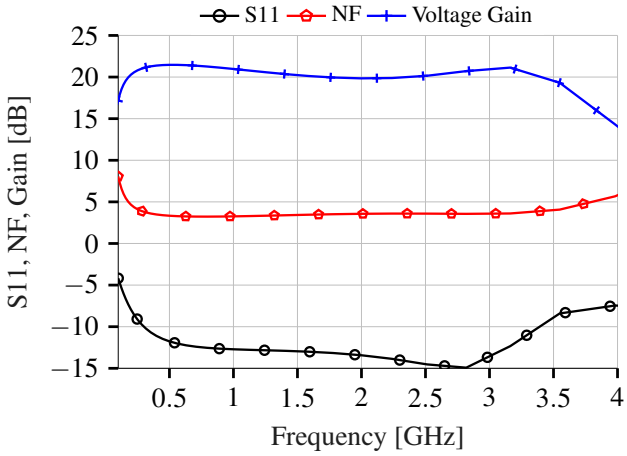


Figure 3.15: S11, NF, and Voltage Gain post-layout simulation results of the LNVGA II.

The reason for the better S11 presented by LNVGA I is the external biasing of the input. The LNVGA I uses an external bias-T to bias the input node, whereas the LNVGA II uses an on-chip resistor. Although the resistor is designed to be as large as possible, it still affects the input matching.

The difference in the NF and gain is a consequence of the VVA load. The active inductors of the LNVGA I not only reduce the gain but also increases the NF. By removing those active inductors, both the gain and NF are enhanced. Furthermore, due to a miscalculation of the inductor L_{d2}, the bandwidth improvement produced by the active inductor was useless. Hence, the LNVGA II achieves even a better bandwidth than that obtained by the LNVGA I.

Another figure to be taken into consideration is output balance. As previously told, the load of the LNVGA has a minor impact on the output balance, and the results shown in figure 3.16 confirms that statement. Both the magnitude and phase differences are almost the same regardless of the VVA load.

In addition to the best NF of the two LNVGAs, the LNVGA II has the largest gain control range. Although both LNVGAs have a similar minimum of -30 dB, the LNVGA II has a maximum gain more than 5 dB higher than that of the LNVGA I. Hence, it has the largest gain control range of the two LNVGAs. Figures 3.17 and 3.17 show the gain sweeping of the LNVGAs.

The linearity of the LNVGAs are presented in figures 3.19 and 3.20 at 1 GHz, which is the point of highest gain. Due to the two stage approach, neither the LNVGA I nor the second one achieves a very high IIP3. Even though the LNVGA II achieves a peak of

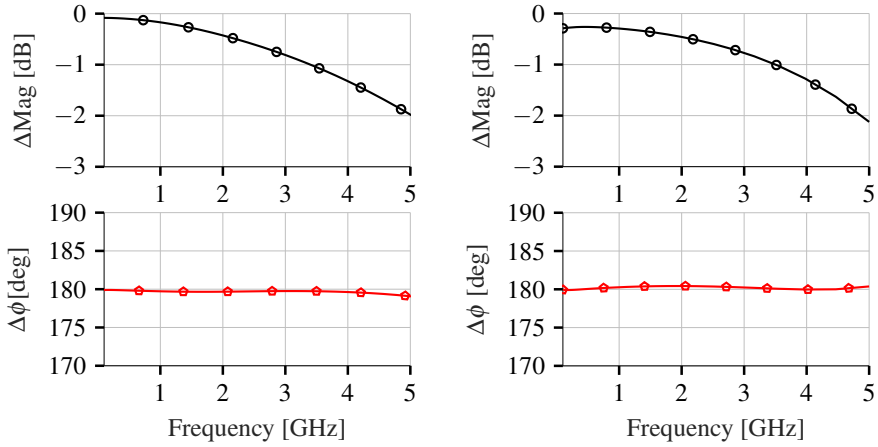


Figure 3.16: Magnitude and phase imbalance post-layout simulation results of the (a) LNVGA I and (b) LNVGA II.

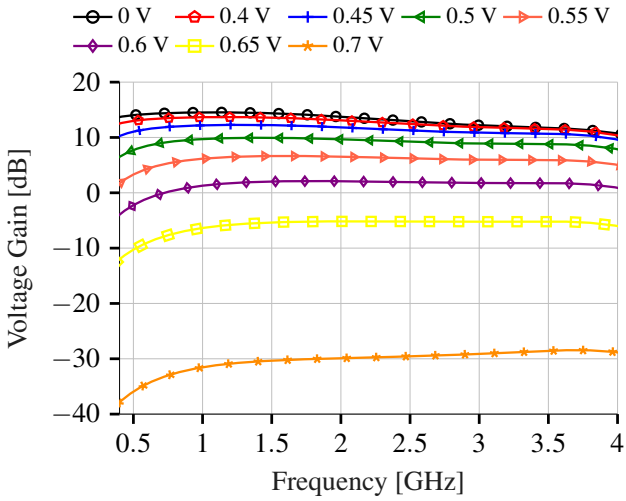


Figure 3.17: Voltage gain post-layout simulation results of the LNVGA I, where each curve uses a different V_{CTRL}.

-5 dBm, the other points are around -11 dBm.

The simulated performance of both LNVGAs are presented in table 3.3. The LNVGA II

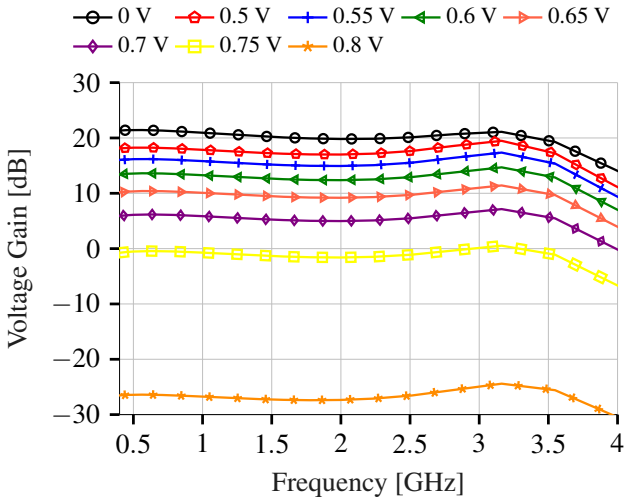


Figure 3.18: Voltage gain post-layout simulation results of the LNVGA II, where each curve uses a different V_{CTRL}.

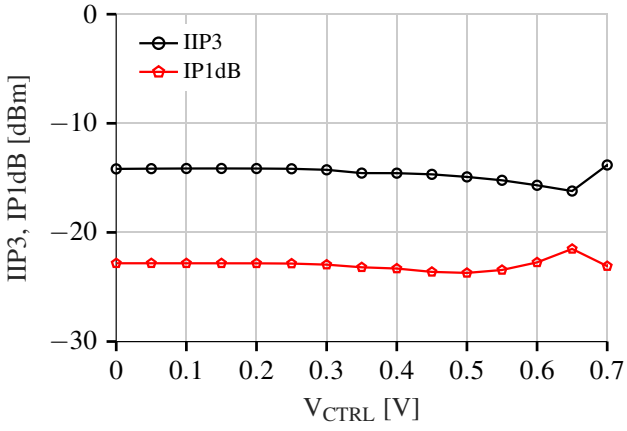


Figure 3.19: IP1dB and IIP3 post-layout simulation results of the LNVGA I at 1 GHz, using different values of V_{CTRL}.

beats the first one not only in NF but also in gain tuning range. The LNVGA I, on the other hand, beats the second one in power consumption. The IIP3 of them are similar, but for a peak of -5 dBm achieved by the LNVGA II.

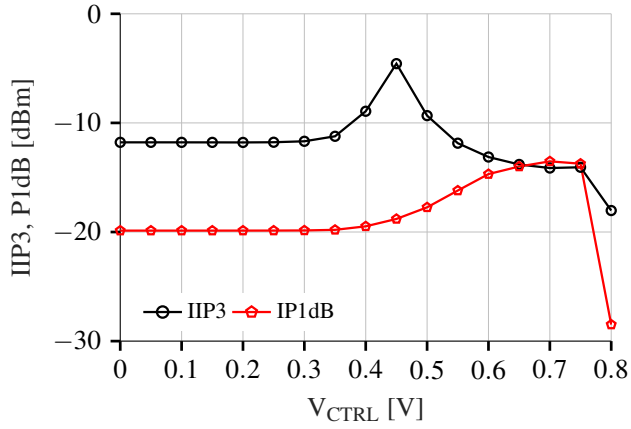


Figure 3.20: IP1dB and IIP3 post-layout simulation results of the LNVGA II at 1 GHz, using different values of V_{CTRL}.

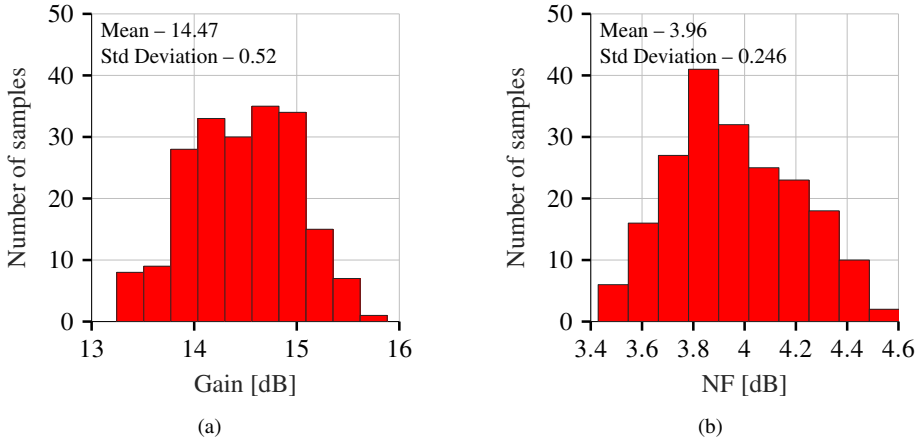
Table 3.3: Simulation results of the LNVGAs.

REF.	Gain [dB]	Min. NF [dB]	IIP3 [dBm]	BW [GHz]	Power [mW]
LNVGA I	-30∼14.8	3.9	-14	0.1-3.5	15.6
LNVGA II	-27∼21.5	3.3	-11.2	0.1-3.5	19

3.5 Monte Carlo simulation results

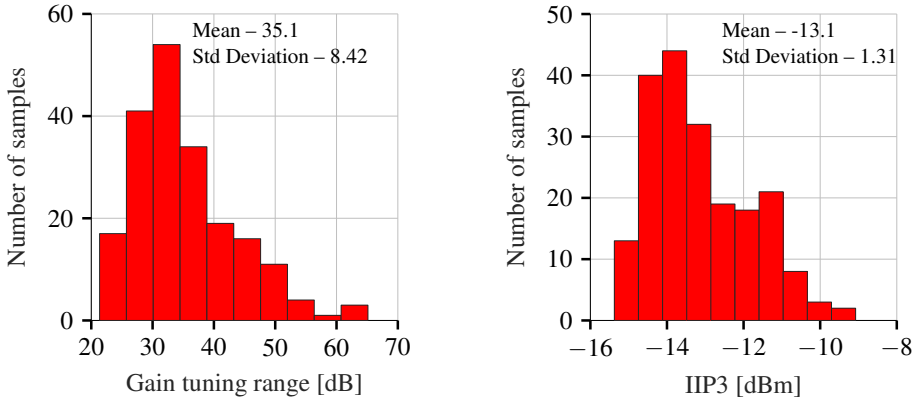
The Monte Carlo results for process variation of the LNVGA I are presented in the figures 3.21a, 3.21b, 3.22a, 3.22b, and 3.23, while the same simulation results for the LNVGA II are presented in figures 3.24a, 3.24b, 3.25a, 3.25b, and 3.26. As it was expected, the spread presented by both circuits are very similar. The voltage gain, NF, and S11 of both circuits show a deviation from the mean below 1 dB. Meanwhile, the IIP3 results of both LNVGAs present a deviation from the mean slightly above 1 dB. Additionally, those mean values are very close to the typical results shown in table 3.3.

The main difference observed between those circuits was the spread of the gain tuning range. While the LNVGA I deviates 8.42 dB, the LNVGA II deviates only 0.58 dB from the mean value of gain tuning range. This difference is probably caused by the active inductor used in the LNVGA I. The LNVGA II uses simple resistors instead of the active inductors, which are less sensitive to process variation.



(a) (b)

Figure 3.21: Post-layout Monte Carlo (process variation) simulation results of the LNVGA I for 200 samples: (a) Voltage gain and (b) noise figure.



(a) (b)

Figure 3.22: Post-layout Monte Carlo (process variation) simulation results of the LNVGA I for 200 samples: (a) Gain tuning range and (b) third-order intercept point.

3.6 Measurement Results

The first (figure 3.27) and the second (figure 3.28) LNVGA were fabricated in 130 nm CMOS. However, since these LNVGAs were separately fabricated, they were tested in different places and with a different test-setup. The LNVGA I was tested using probes for the RF and DC pads, whereas the LNVGA II was tested using probes to the RF

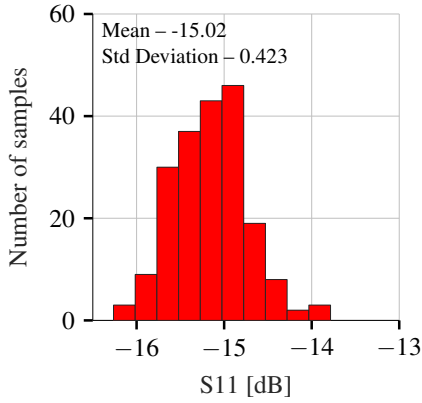


Figure 3.23: Post-layout Monte Carlo (process variation) simulation results of the LNVGA I for 200 samples: Input match.

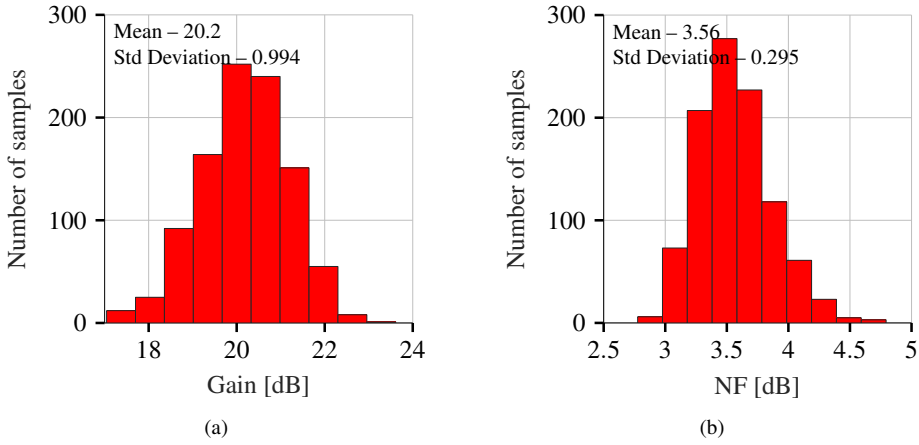


Figure 3.24: Post-layout Monte Carlo (process variation) simulation results of the LNVGA II for 1000 samples: (a) Voltage gain and (b) noise figure.

pads but bondwrires to the DC pads, which were connected to a PCB. Consequently, the latter has the performance affected by those bondwires as we are going to discuss further on this section.

Three samples of the LNVGA I have been tested, achieving similar performance. Meanwhile, only one sample of the LNVGA II has been tested due to technical problems during the chip assembling on the PCB. Since this is an academic work, we do not have the time and the resources to test a large number of samples.

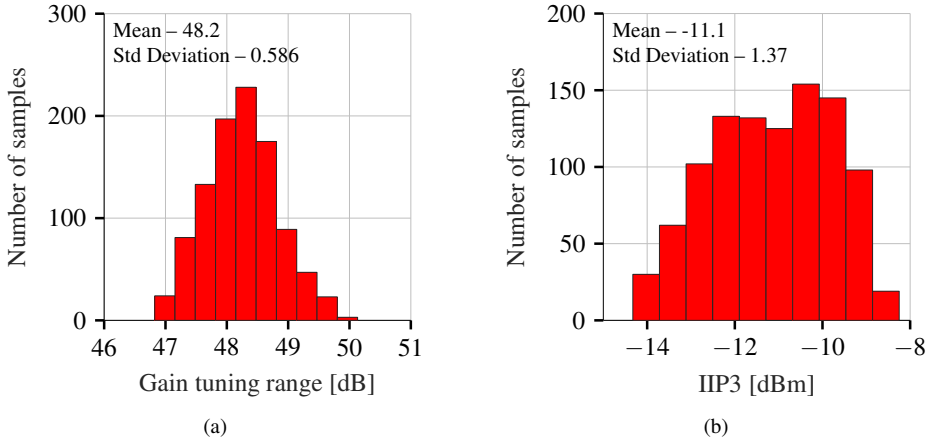


Figure 3.25: Post-layout Monte Carlo (process variation) simulation results of the LNVGA II for 1000 samples: (a) Gain tuning range and (b) third-order intercept point.

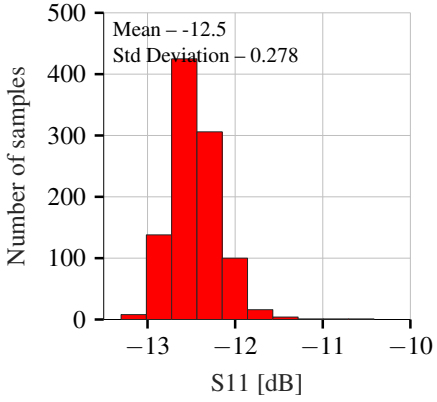


Figure 3.26: Post-layout Monte Carlo (process variation) simulation results of the LNVGA II for 1000 samples: Input match.

The power consumption of the LNVGA I is 15.6 mW at maximum gain and 23 mW at minimum gain when the two baluns are turned on. The power consumption of the LNVGA II is slightly higher than that of the first one because of the different bias choice in some transistors. It consumes 19 mW when the gain is maximum and 27 mW when the gain is minimum.

The active area of both the first and LNVGA II are approximately the same since the components are similar. However, the floorplan of the LNVGA II is more compact

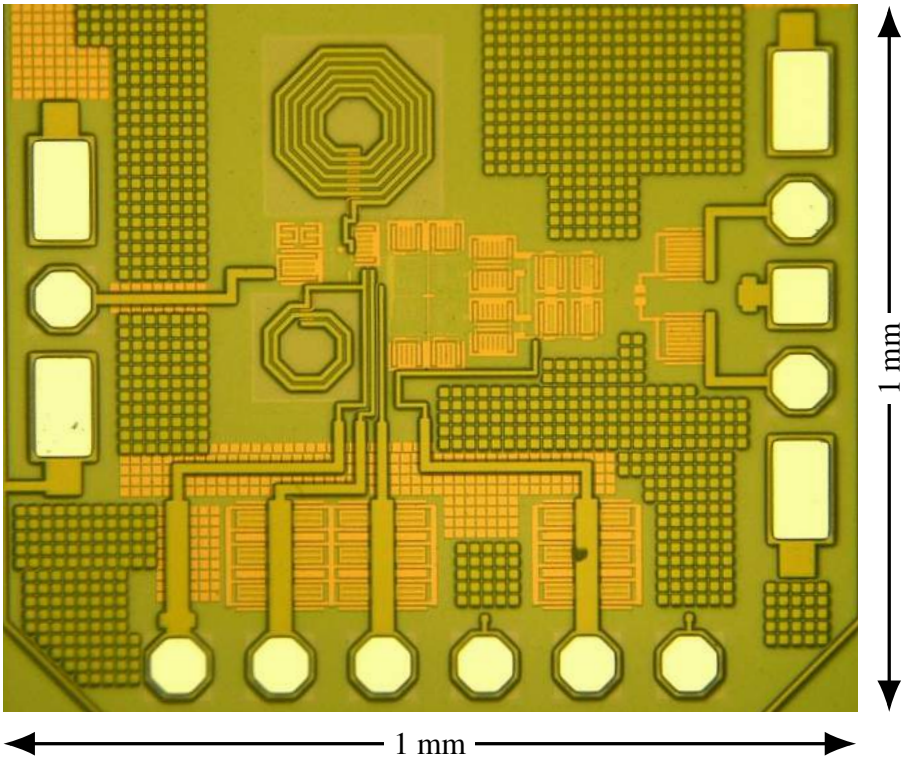


Figure 3.27: Chip photograph of the LNVGA I.

than that of the first one, so the second chip has an area 60% smaller than the area of the LNVGA I.

Table 3.4: LNVGA results in comparison with prior works.

REF.	Gain [dB]	Min. NF [dB]	IIP3 [dBm]	BW [GHz]	Power [mW]	Area [mm^2]	CMOS Process
[102]	-10∼8	4.2	1.8	0.03-7	9	1.16	180nm
[82]	-30∼-2.6	3	N/A	1-3.5	18	0.05	180nm
[98]	-10∼50	17	-45.4∼-3.4†	0.01-2.2	2.5	0.01	90nm
[27]	-5∼11	3.2	-4.5∼0	1-5	19	0.067	180nm
LNVGA I	-25∼10	4.9	-10	0.4-3.3	15.6	0.15	130nm
LNVGA II	-25∼20	3.4	N/M	0.2-3.3	19	0.15	130nm

†Calculated from IP1dB

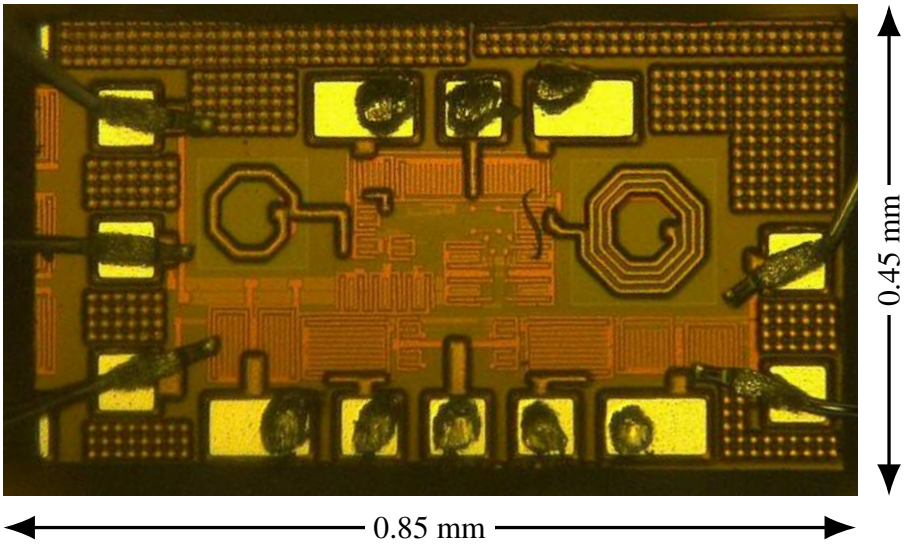


Figure 3.28: Chip photograph of the LNVGA II.

Figure 3.29 shows the gain tuning range of the LNVGA I. It achieves a maximum gain of 10 dB and a minimum gain of -25 dB. The circuit has been tested from 0.4 to 4 GHz, and the 3 dB cutoff frequency is 3.3 GHz at the maximum gain. Although the circuit has been designed to achieve minimum gain when $V_{CTRL} = 0.7$ V, it only achieves the minimum gain when $V_{CTRL} = 0.75$ V due to the voltage drop across this path.

The gain tuning range of the LNVGA II between 0.2 and 4 GHz is presented in figure 3.30. The circuit has a maximum gain of 20 dB at $V_{CTRL} = 0$ V and a minimum gain of -25 dB at $V_{CTRL} = 0.8$ V. In contrast to the LNVGA I, the LNVGA II does not have a flat gain response at low gain levels due to the length of the GND bondwire (≈ 4 mm) and insufficient DC coupling capacitors at the GND. Despite these issues, the LNVGA II achieves a wide band, for the 3 dB cutoff frequency is 3.3 GHz at the maximum gain. Even though the LNVGAs are similar, the gain tuning range of the first is 35 dB, whereas the second has a gain tuning range of 45 dB. Hence, the removal of the active inductor proves to be the right choice.

The measurement of the input reflection coefficient (S11), shown in figures 3.31 and 3.32, demonstrate that, regardless of the gain, the input of both LNVGAs remain matched to 50 Ω within the entire band. The GND bondwire that harms the gain flatness of the LNVGA II also affects the S11 as is noticeable in figure 3.32, yet the S11 remains below -10 dB.

In contrast to the S11, the NF changes a lot with the gain. Figures 3.33b and 3.34b

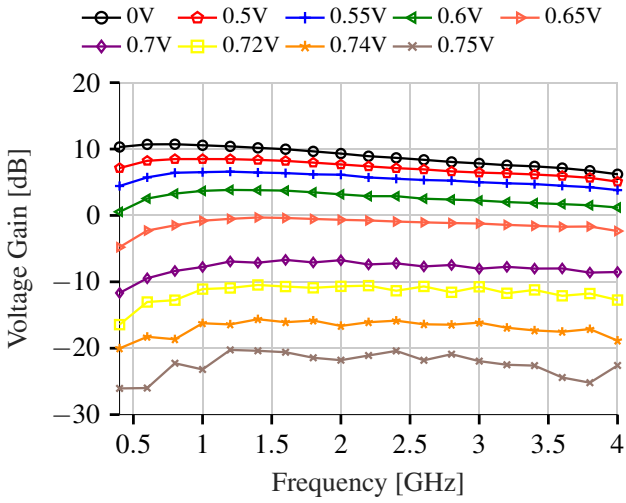


Figure 3.29: Voltage gain variation with V_{CTRL} across the entire band of the LNVGA I.

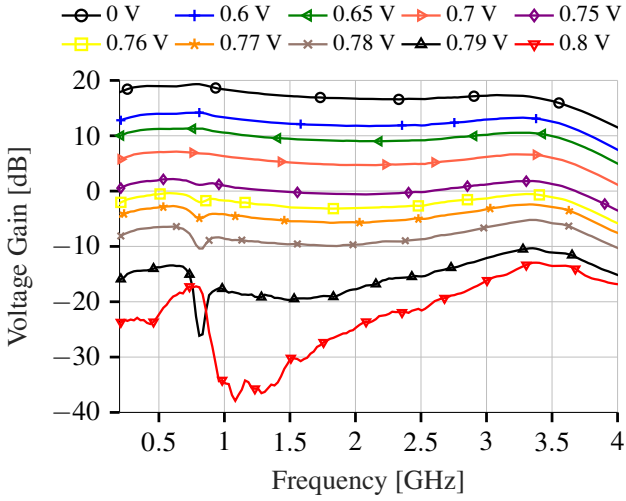


Figure 3.30: Voltage gain variation with V_{CTRL} across the entire band of the LNVGA II.

show that the NF sharply rises as the gain falls at both LNVGAs. Meanwhile, the gain variation with the control voltage is presented in figures 3.33a and 3.34a. Although the LNA reduces the LNVGA NF, it cannot hold the NF low after the LNVGA gain falls below zero. Hence, the NF sharply rises after this point due to the massive noise

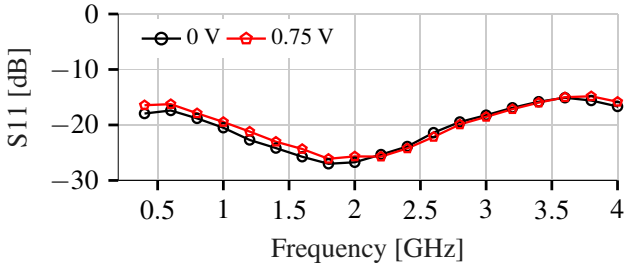


Figure 3.31: S11 results at maximum gain and minimum gain of the LNVGA I.

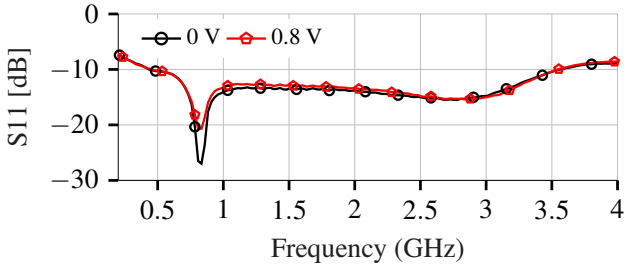


Figure 3.32: S11 results at maximum gain and minimum gain of the LNVGA II.

contribution of the VVA. Nevertheless, the high NF at the minimum gain is not a problem since the purpose of the minimum gain mode is to receive strong signals without compression. The LNVGA II has a minimum NF of 3.4 dB, while the LNVGA I has a minimum NF of 4.9 dB. In comparison to the simulated results, the LNVGA II has similar performance, whereas the LNVGA I has the measured NF 1 dB above the simulated NF. The LNVGA I presented a higher NF than that simulated because the gain falls 5 dB in comparison to simulation.

Figure 3.35 show the input third-order intercept point (IIP3) and the input compression point (IP1dB), respectively. They were measured at different V_{ctrl} values and remains almost constant across the whole band. The input second order intercept point (IIP2) is presented in figure 3.36. The maximum IIP2 is achieved when V_{ctrl} is 0.7 V (+40 dBm), as shows figure 3.36b. At other values of control voltage, the IIP2 remains around +10 dBm (figure 3.36a).

Unfortunately, we were unable to test linearity of the LNVGA II.

A comparison with prior works is shown in table 3.4. In addition to the second largest gain tuning range, our LNVGAs presented very low NF. Even though greater gain

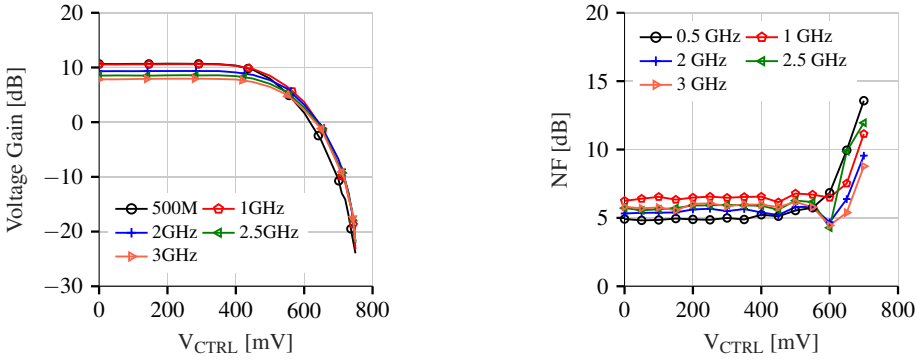


Figure 3.33: The variation of the (a) voltage gain and (c) NF of the LNVGA I.

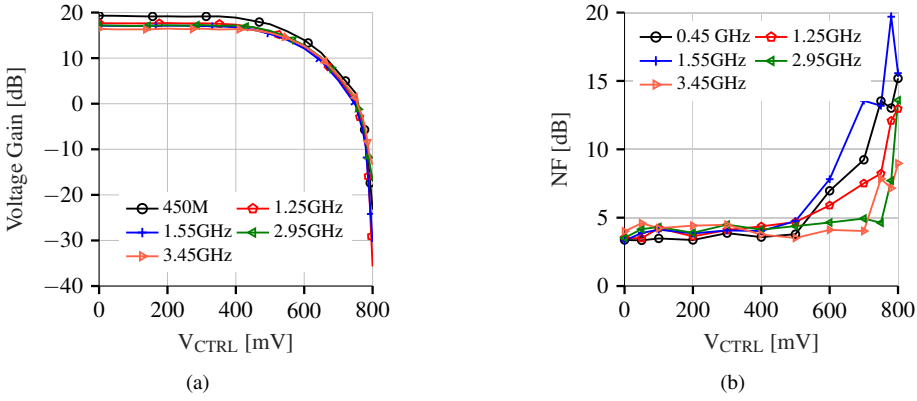


Figure 3.34: The variation of the (a) voltage gain and (b) NF of the LNVGA II.

tuning range is given in [98], this circuit has not only a prohibitively high NF but also a low IIP3. The circuits shown in [102] and in [27] achieve an NF similar to our LNVGAs, but their gain tuning range is much smaller than the gain tuning range of the LNVGAs presented in this chapter. Indeed, the LNVGAs presented here are the only ones that achieved at the same time a large gain tuning range and a low NF.

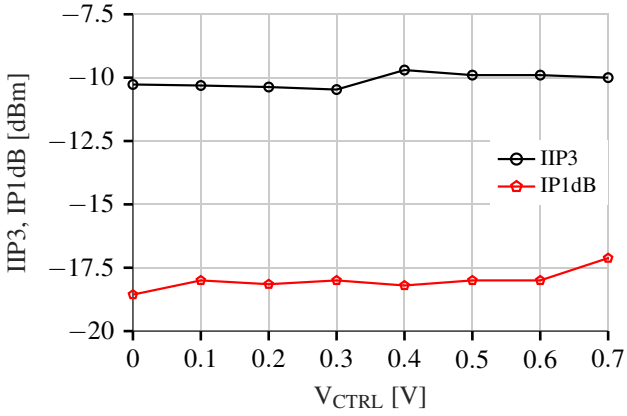


Figure 3.35: The IIP3 and IP1dB variation within the gain levels of the LNVGA I.

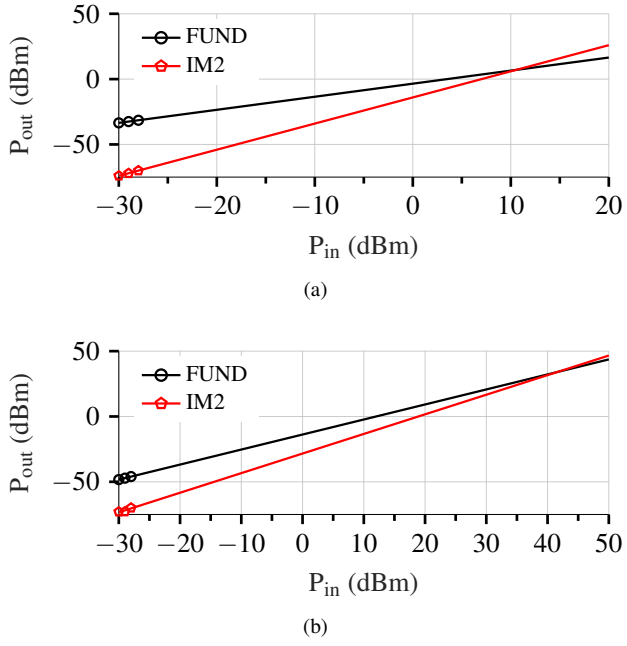


Figure 3.36: The (a) maximum and (b) minimum IIP2 results of the LNVGA I.

3.7 Conclusion of the chapter

Multi-standard receivers must comply with a large range of signal powers, as shown in the hypothetical receiver discussed in chapter 2. In spite of concentrating the gain tuning range on the baseband VGA, it is a wiser choice to share this burden with other blocks in the receiver, and the LNA is the best candidate for that. Therefore, two LNVGAs were presented in this chapter.

The LNVGAs have been designed and fabricated in 130 nm CMOS, and they achieved not only a low noise figure but also a large gain tuning range within a wide band, whereas the circuits previously reported have failed to improve both features simultaneously. The large gain tuning range was enabled by the low-imbalance active balun proposed here. The LNVGA I and LNVGA II achieve a gain tuning range of 35 dB and 45 dB respectively. The LNVGA I achieves a 4.9 dB NF, while the LNVGA II achieves a 3.4 dB NF. On both LNVGAs, the NF rises with the gain reduction, which is not an issue since the attenuation is used only with a strong input signal. The power consumption at maximum gain of the LNVGA I is 15.6 mW and the LNVGA II is 19 mW from a 1.2 V supply. However, the power consumption rises with the gain reduction due to the power consumption of the second active balun.

The technique used on both LNVGAs to control the gain can produce a considerable large gain variation in only one stage, which is useful for multi-standard receivers. However, it cannot be used to reduce performance to save power. Moreover, although the LNVGA successfully avoids the compression of the following stages, it could not prevent its compression. Additionally, the two-stage approach used on the LNVGA design aggravates that mather. Therefore, the LNVGAs herein developed, fabricated, and measured would then become the linearity bottleneck of the receiver.

Chapter 4

Wideband High-IF Receiver Using a Modified Charge-Sharing Bandpass Filter to Boost Q-factor in 40 nm CMOS

4.1 Introduction

The third project of this thesis is a wideband high-IF receiver in 40 nm CMOS, using a modified CS bandpass filter.

The CMOS scaling brings both advantages and challenges in the design of multi-band/multi-standard receivers. Conversely to the design presented in chapter 3, the circuits designed in smaller CMOS nodes, like 40 nm, can achieve a wide bandwidth without using bulky inductors or power-hungry distributed amplifiers. Also, the speed of the transistors increases with scaling, so mixers and high-sampling rate filters can be implemented using switched-capacitors. On the other hand, the supply voltage has been reduced below 1 V, and the transistor has a low intrinsic gain.

Customarily, multi-band/multi-standard radios adopt either zero-IF or low-IF receiver architectures since they offer less or no concerns about image rejection. In such architectures, the channel selection is easily performed on-chip by a lowpass filter (LPF)

after the mixer [80] that also adjusts the channel bandwidth. Despite these interesting characteristics, the zero-IF and low-IF topologies are constrained by $1/f$ noise, second-order nonlinearity, and DC-offset, as previously discussed in chapter 2. To optimize their performance, such receivers overcome these constraints by extensively using calibration [15, 93, 74]. On the other hand, superheterodyne receivers are not affected by these common issues due to their high IF [71, 41, 62], but they traditionally require external filters for image rejection and channel selection. Thus, they have drawn less interest for many years.

However, thanks to CMOS scaling, a new light has been shed on the design of multi-band/multi-standard receivers. The N-path filter proposed in [71], which is an evolution of the original concept [96, 36], solves the superheterodyne external filter problem by implementing a bandpass filter (BPF) using a passive switched-capacitor (SC) topology. The low-Q filter is translated to the radio frequency (RF) input by the mixer, solving the requirement for large external filters. Following the introduction of this new approach, other passive SC-BPFs have been reported [25, 89, 64, 63, 56, 34]. Because of their implementation only with switches and capacitors, those filters are more friendly to process scaling since CMOS trends from one generation to another more advanced tend to reduce the resistance of the switches. In fact, their performance should improve in smaller CMOS nodes, and the scalability can be increased by using MOS capacitors.

Switched-capacitors BPFs allow for the design of fully integrated receivers with a high-IF [71, 88, 64, 63, 56, 34], avoiding the shortcomings presented previously. Like the superheterodyne architecture, the high-IF works with IFs of tens or even hundreds of megahertz. The image and blockers are filtered along the receiver chain by BPFs in the RF-domain, as shown in [71], and in the IF-domain, as shown in [71, 64, 63, 56, 34].

This chapter presents a wideband high-IF receiver, using CS-BPFs to attenuate the image and out-of-band interferers. The receiver operates from 0.5 GHz to 4 GHz, and two main architecture innovations are introduced here. First, the low-noise transconductance amplifier (LNTA) implements a utilization of a folded-cascode structure, which increases the output impedance of the LNTA. Since the following stage is a current mixer, it is mandatory for the LNTA to have a high output impedance. Second, a CS-BPF, in which the Q-factor is boosted by cross-connected transconductors at the input, is presented and discussed. Moreover, since the mixer performs a single-to-differential conversion, the LNTA is single-ended, and there is no need for a chunky transformer at the input. This results in a receiver showing high performance in a wide band, low power consumption, and small area.

This chapter is organized as follows. In section 4.2 the most relevant high-IF receiver are briefly presented. Section 4.3 discusses the receiver architecture. The circuits that compose the receiver are presented in sections 4.4 - 4.8. The sections 4.9 and 4.10 show the measurement setup and results respectively. Finally, section 4.11 summarizes the main achievements of this receiver design work.

4.2 Overview of the state-of-the-art

In this section the most important high-IF receivers that have been published since 2011 are briefly presented. The high-IF receivers are an evolution of the traditional superheterodyne receivers which require external filters. Filters designed with SC are the pre-condition to design those receivers due to their easy integration.

The receiver proposed in [71] is presented in figure 4.1. This receiver was the first fully integrated receiver with a high IF. The utilization of three M/N-phase filters to select the channel and to attenuate blockers is the condition for the full integration of this receiver. The M/N-phase filter, where M is the number of inputs and N the number of clock phases, is an evolution of the N-path filter [96, 36] where the principal difference is the complex transfer function of the former. Consequently, in addition to the blockers, the M/N-phase filter attenuates the signal image.

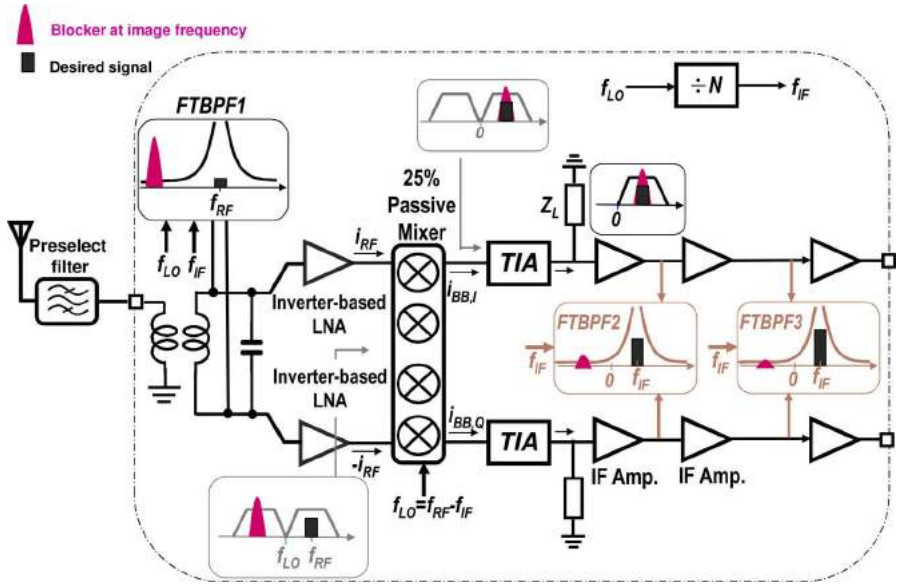


Figure 4.1: High-IF receiver proposed in [71].

The first stage of this receiver is the on-chip balun that converts the incoming signal to a differential signal. After the signal conversion, the first M/N-phase filter selects the desired signal, while attenuating blockers within its stopband, which includes the signal image since this filter is complex. Hence, this first filter prevents that out-of-band blockers compress the LNA composed by self-biased inverters. After that, the signal is down-converted using a 25% passive mixer loaded by a transimpedance amplifier

(TIA). This TIA has a particular bandpass transfer function centered at f_{IF} both at its input and its output. The following circuits are IF amplifiers, which are self-biased inverters like the LNA, and two more M/N-phase filters centered at f_{IF}.

The first M/N-phase filter is a 16-phase filter (4/16-phase BPF), whereas both the second and third filters are 8-phase filters (4/8-phase BPF). Moreover, since the 4/16-phase BPF needs to be centered at f_{RF} to attenuate blockers before the LNA, a passive mixer upconverts its transfer function to f_{RF}. The clock frequency precisely controls the center frequency of theses filters; thus, they are very flexible. The main advantage of these filters is their high Q, which offers an image attenuation as high as 10 dB. However, M/N-phase filter creates replicas at $(4k+1)f_{IF}$, where k is an integer, which might be an issue for the receiver. Moreover, some of those replicas fold on top of the main signal at f_{IF}, which can harm the signal further. In the 4/16-phase BPF, the major folding components are located at $+17f_{IF}$ and $-15f_{IF}$, in which the folding gain is about 23 dB lower than the gain at f_{IF}. In the 4/8-phase BPF, the folding components are located at $-7f_{IF}$ and $+9f_{IF}$; moreover, the folding gain is respectively -17 dB and -19 dB lower than the gain at f_{IF}. Those replicas are the principal liability to the M/N-phase BPF because they compromise the blocker rejection.

The combination of pre-select filter and on-chip filters efficiently attenuate the blockers. A blocker located at $f_{RF}-8f_{IF}$ is attenuated by 70 dB. However, the blocker rejection takes its toll on NF since the 4/16-phase BPF must be enabled. Although the 4/16-phase BPF is a low noise circuit, it still increases the noise figure of the receiver by almost 3 dB. Hence, it must be disabled whenever a better noise figure is needed. The receiver NF is 6 dB when the 4/16-phase BPF enabled, and it is 2.8 dB when this filter is disabled.

Even though the receiver proposed in [71] efficiently removes the out-of-band blockers, the replicas created by the BPF remains a problem. Moreover, the BPF placed at the input of the LNA to filter those out-of-band blockers degrades the NF of the receiver.

The problem with the replicas is solved in [88], in which a charge-sharing (CS) BPF with neither replicas nor folding frequencies within $-f_S/2$ to $f_S/2$ is presented, where f_S is the sampling frequency of the filter. The authors have implemented a receiver based on this CS-BPF, which is shown in figure 4.2. In combination with a current passive mixer, the CS-BPF creates an anti-aliasing filter, canceling the replicas. Although the receiver presented in [88] includes the baseband, we are not going to discuss it here since baseband circuits are not part of the scope of this thesis.

The CS-BPF shares the charges between the in-phase (I) and the quadrature (Q) path, using the rotating and history capacitors, C_R and C_H respectively. In each phase C_R removes a charge proportional to $C_R/(C_H+C_R)$ from each C_H and then delivers it to the next C_H. The CS-BPF works with a f_S four times higher than the LO frequency so that there is no signal aliasing near the RF central frequency.

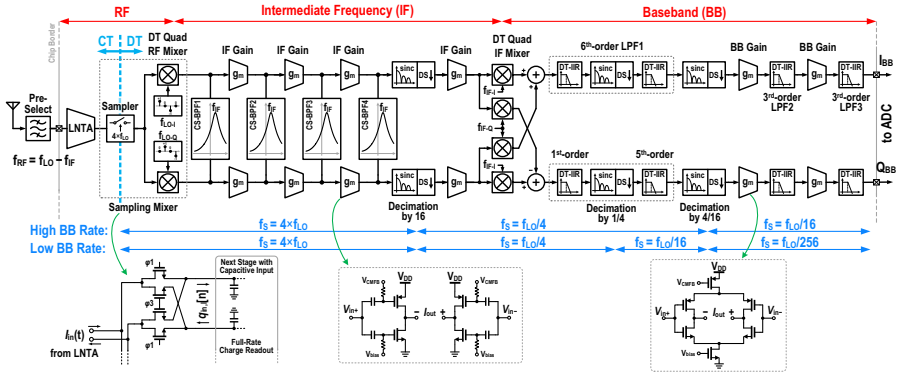


Figure 4.2: High-IF receiver proposed in [88].

In contrast to the M/N-phase BPF, the CS-BPF has a low Q-factor. Thus, four BPFs are cascaded to increase the image and out-of-band blocker attenuation in [88]. Even though the CS-BPF is extremely linear, the transconductor that precedes each CS-BPF is not. Hence, those transconductors become the receiver linearity bottleneck. Due to low linearity of the IF transconductors, the IIP3 of the receiver is only -7 dB.

Another interesting circuit of this receiver is the LNTA. It provides a NF below 2 dB and an IIP3 of 0 dBm. However, it uses a supply voltage of 2 V at the first stage of the LNTA which increases the power consumption. The LNTA alone consumes 14 mW.

Based on the CS-BPF reported in [88], two other receivers had been reported. In [63] a receiver was reported targeting the GSM and PCS bands, while in [56] the target is the Bluetooth band. Both receivers have used variations of the CS-BPF within their designs.

The receiver of [63] is shown in figure 4.3. In comparison to the receiver in [88], the first improvement is in the CMOS technology. The receiver reported in [63] was designed in a smaller node than the previous one, which is a huge advantage to the design of SC based circuits like the CS-BPF. Moreover, it presents an LNTA more linear and less power hungry than that presented in [88].

In addition to the LNTA, the CS-BPF was also improved. Instead of four inputs and four phases like the previous reported BPF, this BPF has eight inputs and sixteen phases so that a much higher Q-factor. We are also going to use the notation M/N-phase to the CS-BPF [63]. Hence, the CS-BPF presented in [88] is the 4/4-phase and in [63] is the 8/16-phase.

Having eight input instead of four, the 8/16-phase CS-BPF achieves a higher Q-factor than the 4/4-phase CS-BPF. In addition, the 8/16-phase CS-BPF has an additional

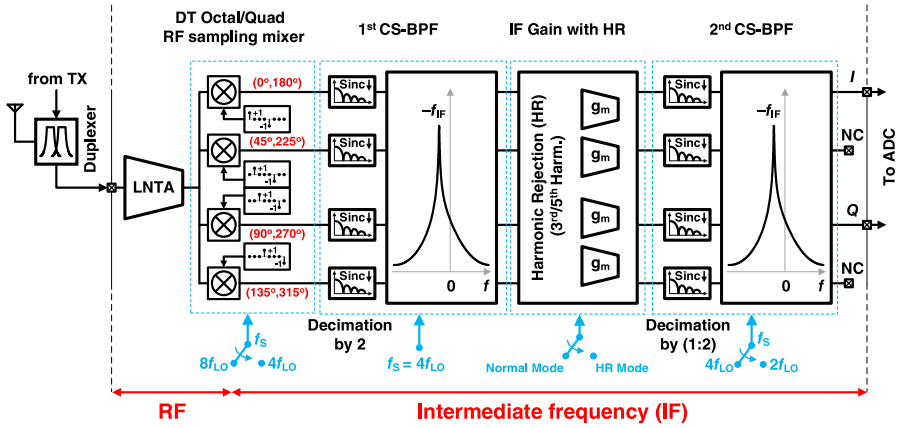


Figure 4.3: High-IF receiver proposed in [63].

IIR LPF that increases the order of the CS-BPF. Consequently, the Q-factor is further increased. By cascading two 8/16-phase CS-BPF, the receiver achieves an image attenuation of 65 dB. It also attenuates the out-of-band blockers, improving the out-of-band IIP3. Besides, because of the eight inputs, a harmonic rejection stage could be implemented after the mixer, which further improves the IIP3.

Thanks to the design techniques mentioned earlier, the receiver in [63] achieves an NF below 3 dB and an IIP3 between 2 and 14 dBm. However, it ends up increasing the power consumption and the area due to the number of switches within the BPFs. Whereas the 4/4-phase CS-BPF has only sixteen switches, the 8/16-phase CS-BPS has 256 switches. Thus, despite the supply voltage of 0.9 V, this receiver shows a power consumption similar to the receivers reported in [71, 88] that have used a larger supply voltage.

The receiver of [56] is shown in figure 4.4. Even though [56] targets an entirely different application than the receiver reported in this chapter, two interesting ideas must be highlighted. The passive mixer does the single-ended to differential conversion. Hence, there is no need for an on-chip balun [71] or a differential input [63] which may be incompatible with the antenna. Furthermore, the receiver in [56] heavily decimates the signal after the first filtering stage which reduces the power consumed by the following filtering stages. Although the reduction of the sampling frequency of the BPF increases the NF, the impact on the receiver NF will be minimum if the BPF is the third or fourth stage in the receiver's chain. Therefore, the power consumption of the receiver can be reduced with a small impact on the NF.

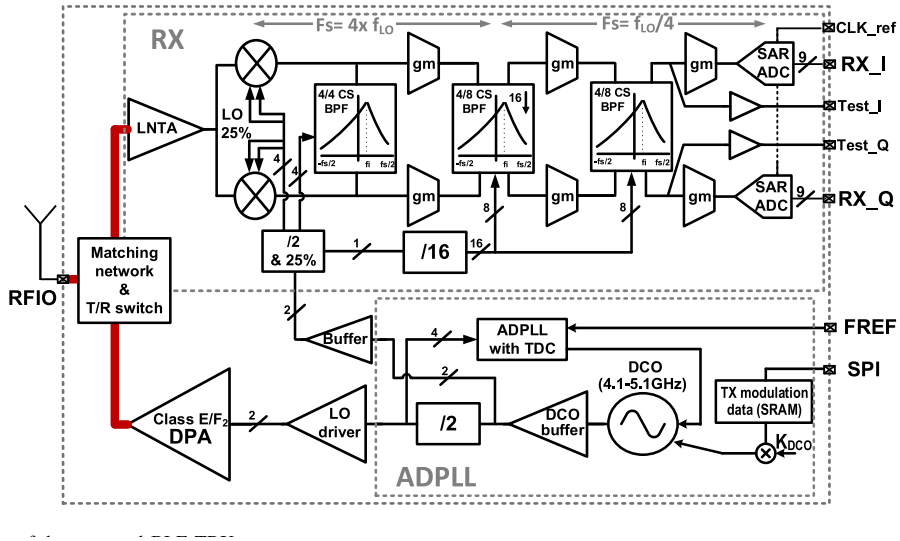


Figure 4.4: High-IF receiver proposed in [56].

4.3 High-IF receiver architecture

The receiver chain using a high-IF architecture with quadrature down-conversion is presented in figure 4.5. This topology has been selected because of its low noise and high-linearity. Despite the passive blocks such as the mixer and the BPFs, the noise remains low thanks to the high performance LNTA. Moreover, the first BPF shapes the input impedance of the mixer and attenuates the interferers.

As the first block in the receiver chain, the LNTA has the primary task of mitigating the noise contribution from the whole receiver chain. In addition, since the following block is a current mode mixer, the LNTA must work as a transconductor, having a large output impedance which maximizes the AC current delivered to the mixer [70]. The LNTA has also an additional linearity burden; since the following mixers and filters are passive, i.e. highly linear but gain-less and noisy, the LNTA must have a higher gain, which reduces its linearity. Moreover, the supply voltage is 0.9 V which further limits the linearity. Consequently, the LNTA becomes the linearity bottleneck of the receiver.

In [71] the LNTA is a self-biased inverter-based transconductor. Also, a large on-chip transformer to convert the input from single-ended to differential has been used, which gives an extra 10 dB of voltage gain. Recently published LNTAs [88, 63] use noise canceling techniques to improve noise figure. In [88] a two-stage LNTA is presented: the first stage is a high-linear low-noise amplifier since it works with a

supply voltage higher than the nominal (2 V), and the second stage does the voltage to current conversion. In [63] the LNTA has only one stage which reduces the power consumption, but requires a cascode at the output to create a high output impedance which limits the LNTA linearity due to the 0.9 V supply voltage. Both circuits create the input match using a common-gate transistor with their sources biased with external inductors. This work uses a fully integrated single-ended LNTA, without the need for external inductors or a chunky transformer. The choice for a single-ended topology is further discussed in section 4.4.

One of the most interesting features of the passive mixer is its transparency [5]. Combining the mixer with a BPF, the impedance seen at the input of the mixer is shaped by the BPF transfer function (TF). Therefore, interferers that eventually arrive at the input have lower gain than the main signal, increasing the linearity of the LNTA and, consequently, of the receiver. Moreover, the passive mixer creates an anti-aliasing filter when working as a sampler [70] an it performs the single-ended to differential conversion easily, without requiring additional circuitry.

The SC filters operate in the discrete-time (DT) domain. Their advantages over the continuous-time (CT) filters were extensively discussed in [71, 64]. Overall, DT filters, such as the N-path filters [71, 37, 25] and the charge-sharing (CS) filters [64, 63, 34, 56], are passive filters based on SC, being more linear and less power hungry than CT filters. Although the N-path filter has a higher Q-factor than the CS filter, its transfer function has several replicas, while the CS filter transfer function has only one peak between $-f_s/2$ and $f_s/2$. These replicas can reduce the blocker rejection or fold blockers on top of the main signal. Hence, CS filters were chosen for this design. Since the CS BPF has a low Q-factor [64], the receiver needs two filter stages to attenuate the image and the out-of-band interferers. The first filter is a first order BPF which operates at the same sampling frequency (f_s) as the mixer to properly cancel the aliasing. The second BPF, on the other hand, does not need to use the same f_s as the mixer since the aliasing requirement was already met. Hence, the clock of the second BPF is reduced which decimates the input signal. In addition, the Q-factor of this BPF is enhanced by increasing the order of the filter and by a circuit modification as explained further ahead.

The GM-cells are an intermediate stage between the first and second filtering stages. These transconductors are needed to drive the passive second filtering stage like the LNTA drives the passive mixer. Being the fourth block in the chain, the GM-cells main restriction is linearity. Moreover, the receiver requires two non-overlaping clocks, two 25% duty-cycle clocks and one 12.5% duty-cycle clock, with two different circuits to generate them. Finally, the output buffers are simple source-followers that isolate the circuit and provide a 50 Ω output match to the measurement equipment.

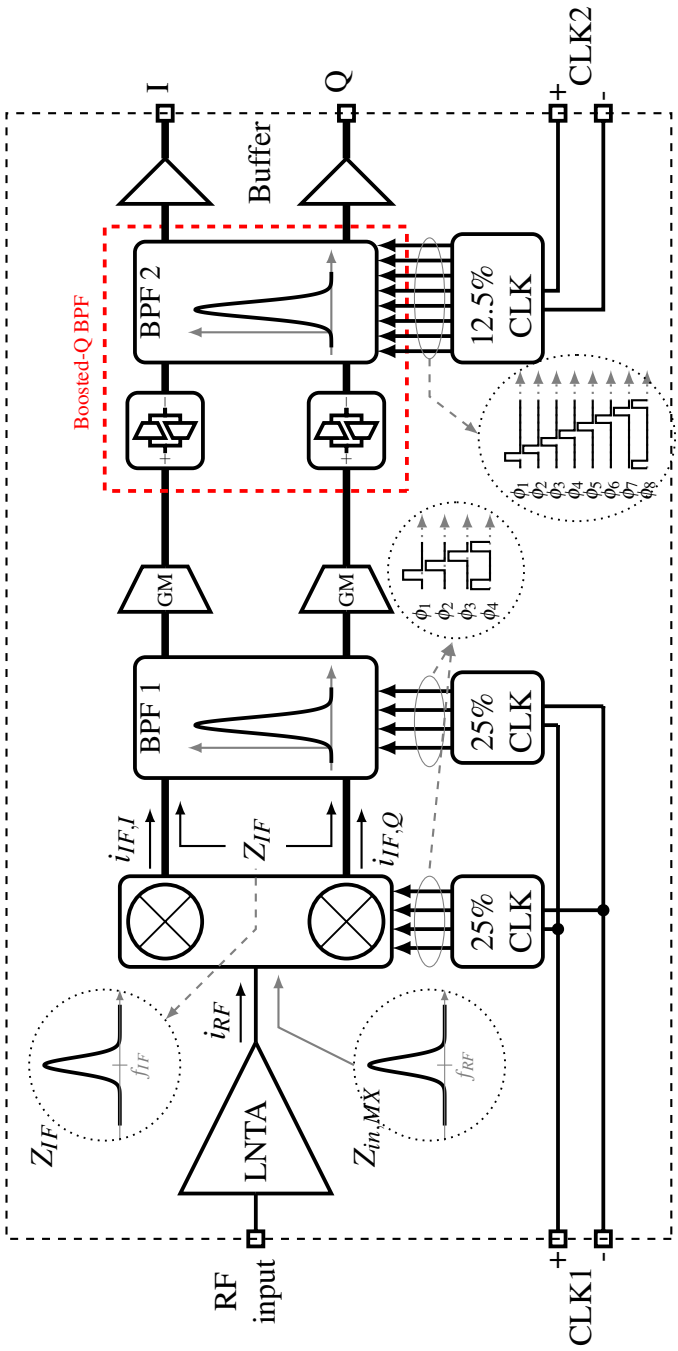


Figure 4.5: The proposed receiver chain together with the clock generation.

4.4 LNTA

The output impedance is one of the most important non-idealities of transconductors since it limits the AC current delivered to the load and the effective V-to-I conversion (GM). Therefore, the output impedance ($Z_{out,LNTA}$) of the LNTA (figure 4.6) has to be higher than the input impedance of the passive mixer ($Z_{in,MX}$). The higher $Z_{out,LNTA}/Z_{in,MX}$ ratio, the better GM implementation.

The LNTA has two cascodes and one folded-cascode which ensure a high output impedance. The cascodes also improve the load isolation, so the input match and noise canceling are immune to any load variation. The use of long channel transistors for M2 and M3 would also increase the output impedance without the need for cascodes, but it would harm the input match at frequencies higher than 1 GHz since C_{gs} increases proportionally to the gate length.

The folded-cascode that is created by connecting M6 to the source of M5 is the best solution for the connection between M6 and the output. Although M6 can be directly connected to the output, it would reduce the output impedance.

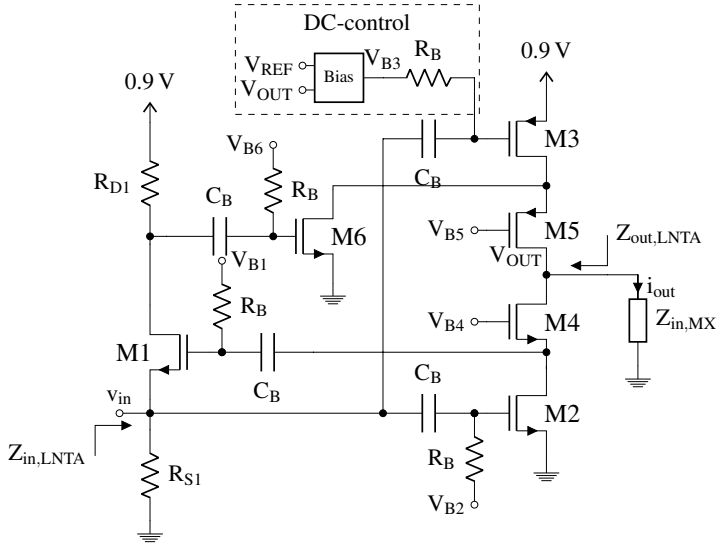


Figure 4.6: The proposed LNTA topology.

The 50 Ω input match is provided by M1. Since its transconductance (g_{m1}) is boosted by the local feedback through M2, the LNTA input impedance is $Z_{in,LNTA} \approx 1/g_{m1}(g_{m2}/g_{m4}+1)$, where g_{m2} and g_{m4} are the transconductances of M2 and M4, respectively. However, since the intrinsic gain (g_m/g_{ds}) for a minimum length transistor in this technology

is about 5 V/V, g_{ds1} cannot be neglected, and $C_{gs2,3}$ are also not negligible at high frequencies. The input impedance including those effects is given by

$$Z_{in,LNTA} = \frac{1}{\dfrac{g_{m1}(g_{m2}/g_{m4}+1)}{1+g_{ds1}R_{D1}} + \dfrac{g_{ds1}}{1+g_{ds1}R_{D1}} + s\,(C_{gs2}+C_{gs3})}, \tag{4.1}$$

considering $R_{S1} \gg 50\ \Omega$. Usually, $Z_{in,LNTA}$ is designed to be slightly higher than 50 Ω to compensate for the parasitic impedances that appear in parallel with $Z_{in,LNTA}$ and reduce its value.

The noise canceling technique cancels only the noise of the transistor responsible for the input matching [17, 13, 19], which is M1 in this design. Hence, the noise generated by the auxiliary amplifier, which is initially M2 in this design, remains a full contributor to the overall noise figure, and it needs to be reduced by traditional means, like increasing the g_m.

In order to further reduce noise figure, the noise of M2 is fed back to the input and amplified through a second auxiliary amplifier. Thus, the noise of M2 is partially canceled as explained further. The local feedback is created by connecting the drain of M2 to the gate of M1 [97, 28], which also boosts the g_m of M1. The second auxiliary amplifier is created by using current-reuse [86], which saves power. Hence, M3 is added to the circuit. As a result, this LNTA topology completely cancels the noise of M1 and partially cancels the noise of M2, which are the major noise sources of the circuit.

The noise factor contribution of all components of the LNTA are represented by

$$F_{M1} \approx \gamma g_{m1} R_S \left[\frac{g_{m2}+g_{m3}-g_{m6}G_{m1}R_{D1}}{g_{m2}+g_{m3}+g_{m6}G_{m1}R_{D1}}\right]^2, \tag{4.2}$$

$$F_{M2} \approx \gamma g_{m2} R_S \left[\frac{g_{m1}\left(1+G_{m1}+G_{m1}R_{D1}g_{m6}-\dfrac{g_{m3}}{g_{m4}}\right)}{g_{m2}+g_{m3}+g_{m6}G_{m1}R_{D1}}\right]^2, \tag{4.3}$$

$$F_{M3} \approx \gamma g_{m3} R_S \left[\frac{2G_{m1}}{g_{m2}+g_{m3}+g_{m6}G_{m1}R_{D1}}\right]^2, \tag{4.4}$$

$$F_{M4} \approx \gamma g_{m4} R_S \left[\left(\frac{g_{m1}}{g_{m4}}\right)\frac{g_{m2}+g_{m3}-g_{m6}G_{m1}R_{D1}}{g_{m2}+g_{m3}+g_{m6}G_{m1}R_{D1}}\right]^2, \tag{4.5}$$

$$F_{M6} \approx \gamma g_{m6} R_S \left[\frac{2G_{m1}}{g_{m2}+g_{m3}+g_{m6}G_{m1}R_{D1}}\right]^2, \tag{4.6}$$

$$F_{R_{D1}} \approx \frac{R_S}{R_{D1}} \left[\frac{2g_{m6}G_{m1}R_{D1}}{g_{m2}+g_{m3}+g_{m6}G_{m1}R_{D1}} \right], \tag{4.7}$$

$$F_{R_{S1}} \approx \frac{R_S}{R_{S1}}. \tag{4.8}$$

Where G_{m1} is $g_{m1}(g_{m2}/g_{m4}+1)$ and R_s is the signal source resistance, which should be equal to $Z_{in,LNTA}$. Also, these equations consider the circuit input matched to 50Ω. Consequently, the noise factor of the LNTA is given by

$$F_{LNTA} \approx 1 + \sum_j F_j, \tag{4.9}$$

where j are the circuit components that add noise to the system. After the noise cancellation, M3 and R_{D1} are the dominant noise sources of the LNTA since the noise contribution of M6 is reduced by the gain $g_{m1}R_{D1}$ and the noise contribution of M4 and M5 are small.

It can be deduced from (4.2) that the noise contribution of M1 is zero if

$$g_{m2}+g_{m3} = g_{m6}G_{m1}R_{D1} \tag{4.10}$$

and from (4.3) that the noise contribution of M2 is zero if

$$1+G_{m1}+G_{m1}R_{D1}g_{m6} = \frac{g_{m3}}{g_{m4}}. \tag{4.11}$$

However, these conditions cannot be achieved simultaneously. The best choice, therefore, is to fully cancel the noise of M1 since it is the primary noise source and only cancel the noise of M2 partially. After the noise cancellation, M3 and R_{D1} are the dominant noise sources of the LNTA. The noise contribution of M6 is reduced by the gain $g_{m1}R_{D1}$ and can thus be neglected.

The proposed single-ended topology has two advantages over its differential counterpart: a lower power consumption and a larger GM while keeping the noise canceling condition. The single-ended topology needs R_{D1} and M6 to invert the polarity of both signal and noise. This additional stage increases the degree of freedom of the design since it decouples the values of g_{m2}, g_{m3}, and G_{m1}. In the differential version of this LNTA, the noise cancellation condition would be $g_{m2}+g_{m3}=G_{m1}$ since neither M6 nor R_{D1} are present. Hence, the values for g_{m2} and g_{m3} would be limited by G_{m1}. The single-ended version, on the other hand, does not have this limitation. Not being limited by G_{m1}, g_{m2} and g_{m3} can be set to much higher values which further reduce their noise and increase the transconductance.

In the single-ended topology of this LNTA, the main problem is the linearity since both M6 and the cascode transistors (M4 and M5) impose limits. The former increases the signal distortion because M1 and R_{D1} have already amplified the signal. The latter

reduces the linearity due to the four stacked transistors within a supply voltage of 0.9 V. Furthermore, the small V_{DS} across those stacked transistors increases the value of their distortion terms. In particular, the distortion of M4 and M5 cannot be neglected [20].

Therefore, the gain of M6 is kept below one to minimize distortion. The g_m/I_D of M1 and M2 have been selected in such a way that their third-order distortion terms cancel each other. The former is biased in strong inversion, and the latter in moderate inversion [84]. Additionally, M4 and M5 are biased like in [20] to achieve an optimal trade off between linearity and noise.

The DC voltage at the output node is kept constant by the DC-control block. In spite of any variation on the V_{DS} of the cascode, the DC output voltage remains constant at $VDD/2$, which maintains these transistors in the selected operation point.

Table 4.1 summarizes the sizing of the transistors. The resistors and capacitors of bias, R_B and C_B, are 10 kΩ and 4 pF respectively. The resistor R_{S1} is 1 kΩ so that $R_{S1} \gg 50$ Ω, while R_{D1} is 500 Ω. Also, figure 4.7 and figure 4.8 show post-layout simulation results. The LNTA was simulated using a 50 Ω load that corresponds to the minimum input impedance of the mixer. The simulated NF is below 2.3 dB within the entire band, and it has a minimum value of 1.8 dB. The gain varies from 17 to 13.5 dB at 0.2 and 4 GHz respectively. Also, the input reflection coefficient (S11) remains below -10 dB over the entire band considered. Due to parasitic capacitances, the output impedance of the LNTA reduces at higher frequencies. Consequently, the ratio $Z_{out,LNTA}/Z_{in,MX}$ is reduced, which increases the difficulty to drive the mixer and compromises the overall receiver gain.

Figure 4.9, Fig 4.10, and Fig 4.11 show the results of corners simulation. Temperature variation has a minimum effect on the LNTA. Process variation, on the other hand, reduces the gain down to 12 dB, while it raises the NF up to 3 dB.

Table 4.1: LNTA sizing parameters.

	M1	M2	M3	M4	M5	M6
g_m/I_D [S/A]	17.9	8.4	9.3	12.9	14.6	12
L [nm]	45	60	60	80	80	40
I_D [mA]	0.4	5.2	6.2	5.2	5.2	1

4.5 First filtering stage

The combination of a passive mixer and a charge-sharing (CS) SC filter is beneficial since the mixer, if properly designed, cancels the aliasing created by the SC architecture.

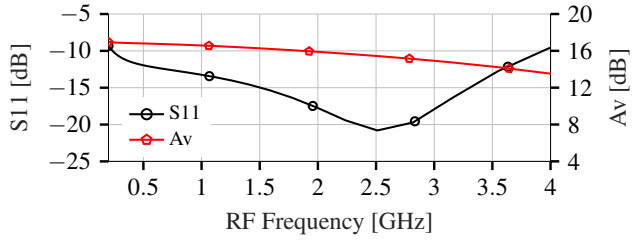


Figure 4.7: The voltage gain and input reflection coefficient simulation results.

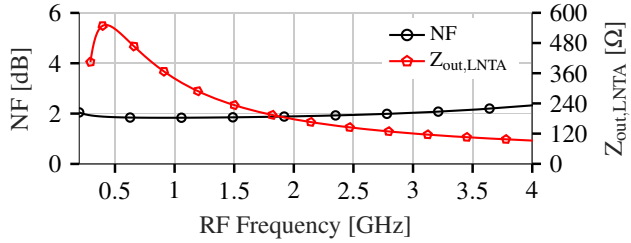


Figure 4.8: The output impedance and noise figure simulation results.

However, the aliasing cancellation happens only if the peaks from the BPF filter are aligned with the nulls from the mixer. Thus, their f_s have to be equal or $f_{s,BPF} = \frac{f_{s,MX}}{2n}$ for $n \in \mathbb{N}^*$, i.e. using clock decimation for the BPF. The decimation is avoided here since it would increase the noise figure due to noise folding. As a result, the first BPF works at a high f_s, the same as the mixer, narrowing down the topology of choice to the 1st order BPF with 4 phases (BPF 4/4) [64], which works well at high frequencies.

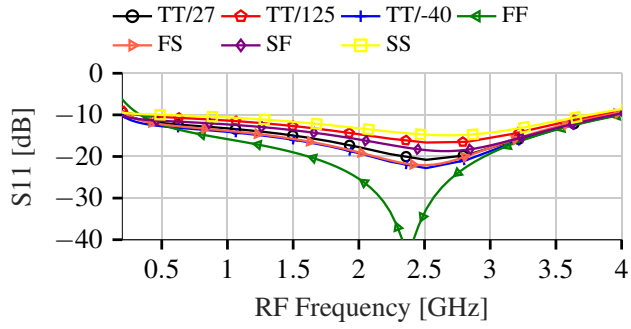


Figure 4.9: LNTA post-layout results of S11.

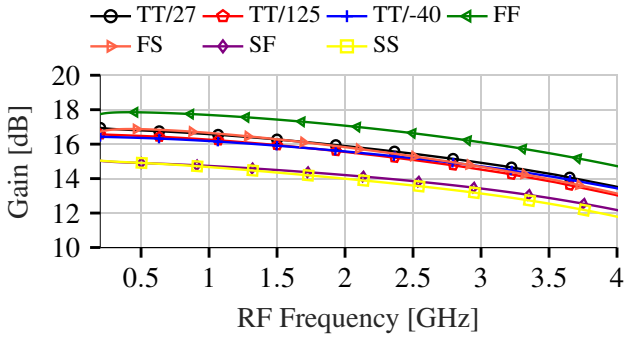


Figure 4.10: LNTA post-layout results of voltage gain.

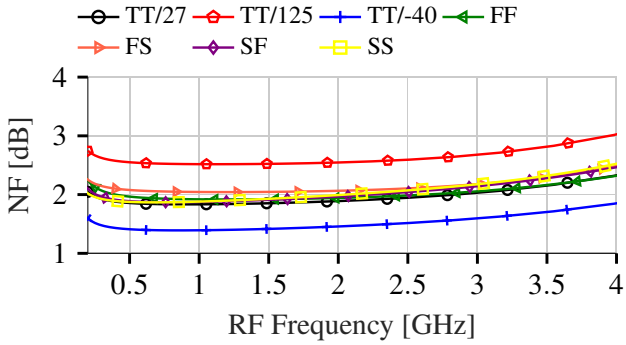


Figure 4.11: LNTA post-layout results of NF.

Since the mixer has to match the number of phases of the BPF, this design uses a 4-phase passive mixer. Also, this 25 %-duty-cycle non-overlapping clock drives the mixer, preventing I-Q crosstalk [70]. In addition, the mixer sampling frequency is four times the LO frequency.

4.5.1 Mixer

The anti-aliasing filter is created only if the mixer, which is presented in Fig 4.15, works as a sampler when its transfer function is a *sinc* function [70],

$$H(f) = \frac{sin(\pi f T_s)}{\pi f T_s}, \tag{4.12}$$

where T_s is the sampling period and f the frequency in Hz. Figure 4.12 shows the TF of the anti-aliasing filter (dotted black line). When combined with the BPF TF, the only remaining peak is at the central frequency of the BPF while all the DT replicas are attenuated.

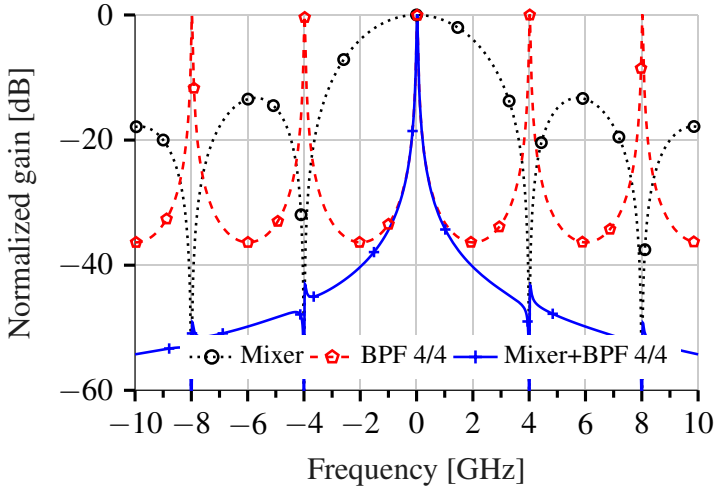


Figure 4.12: Transfer Function of the mixer and BPF when $f_s = 4GHz$.

A consequence of the mixer transparency is the up-conversion of the baseband impedance, in this case an IF impedance. Thus, its input impedance is a function not only of the resistance of the switches, but also of the IF impedance, which is a BPF filter in this design. According to [5], the input impedance of a passive mixer is also affected by the harmonics of the clock driving its switches. A resistor in parallel with the IF impedance adds this effect to the electrical model as can be seen in figure 4.13a. Moreover, the resistance of only one switch has to be taken into consideration since the switches are not closed at the same time due to the non-overlapping clocks.

Figure 4.13a shows the electrical model proposed in [5], where R_{sw} is the resistance of the switches, R_{sh} models the effect of the clock harmonics on the input impedance, Z_{IF} represents the IF impedance, i.e. the BPF 4/4 input impedance, and ζ is the impedance up-conversion constant. Hence, the input impedance of the passive mixer is [5]

$$Z_{in,MX} = R_{sw} + R_{sh} || \zeta Z_{IF}, \tag{4.13}$$

where $\zeta \approx 0.203$ and $R_{sh} \approx 4.3(R_{out,LNTA} + R_{sw})$ [5]; $R_{out,LNTA}$ is the real part of the output impedance of the LNTA. Eq. (4.13) shows that Z_{IF} and R_{sh} have a considerable effect on the input impedance of the mixer. Based on (4.13), the input impedance of the mixer can be predicted as shown in figure 4.13b. Since the input impedance of

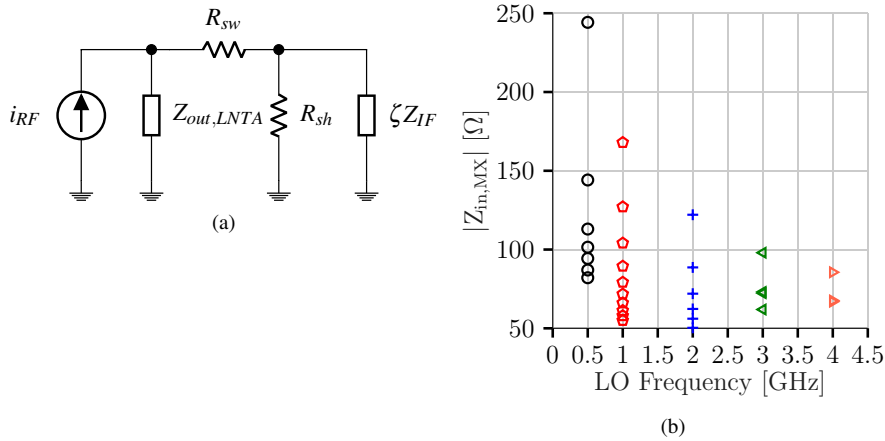


Figure 4.13: (a) The passive mixer electrical model [5]. (b) The variation of the input impedance of the mixer with the LO frequency.

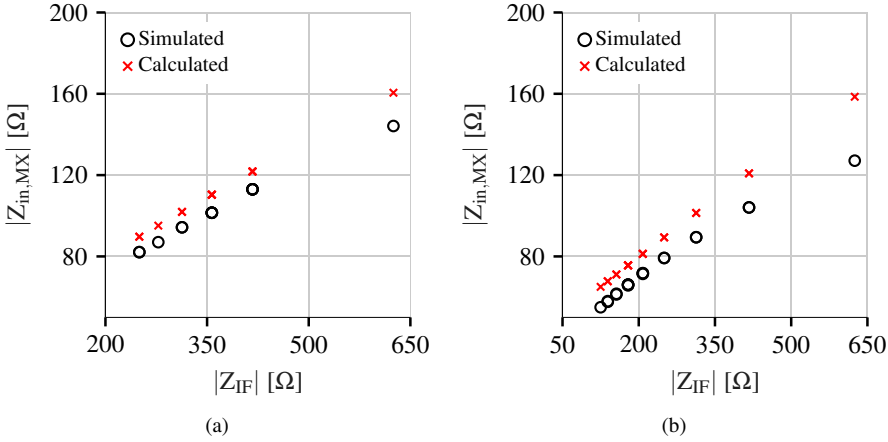


Figure 4.14: The comparison of the calculated and simulated input impedance of the mixer at (a) 500 MHz and (b) 1 GHz.

the BPF 4/4 decreases with the LO frequency increase, the input impedance of the mixer also drops, thereby reducing the overall gain. The gain drop can be compensated by changing the value of the capacitor C_R, which controls the input impedance of the BPF 4/4 and enable a flat gain response. The values predicted with (4.13) are reasonably accurate as observed in figure 4.14a and figure 4.14b.

The mixer and BPF 4/4 will properly work as long as $|Z_{out,LNTA}| \gg |Z_{in,MX}|$, so that the

$Z_{in,MX}$ is dominant. As discussed in [70], the gain and the null depth of the mixer are reduced if the previous condition is not fulfilled. Henceforth, the aliasing cancellation, which is generated by these nulls, will be limited.

There are two main reasons to reduce as much as possible $Z_{in,MX}$: it increases the bandwidth of the LNTA, and $Z_{in,MX}$ has to accommodate for any reduction on $Z_{out,LNTA}$ that happens at high frequencies due to parasitic capacitances. Otherwise, the mixer and the BPF 4/4 will not work as planned at these frequencies. Nevertheless, $Z_{in,MX}$ ends up being limited by the CMOS technology since it is directly dependent on the resistance of the mixer and BPF 4/4 switches.

The noise factor of the mixer and the BPF 4/4 can also be calculated from the model in figure 4.13a and is given by

$$F_{MX\&BPF} = 1 + \frac{\overline{v_{n,sw}^2}}{\overline{v_{n,R_{out,LNTA}}^2}} + \frac{\overline{v_{n,sh}^2}}{\overline{v_{n,R_{out,LNTA}}^2}} \left(\frac{R_{out,LNTA} + R_{sw}}{R_{sh}} \right)^2 + \frac{\overline{v_{n,IF}^2}}{\overline{v_{n,R_{out,LNTA}}^2}} \left(\frac{R_{out,LNTA} + R_{sw}}{\zeta Z_{IF}} \right)^2, \tag{4.14}$$

which is simplified to

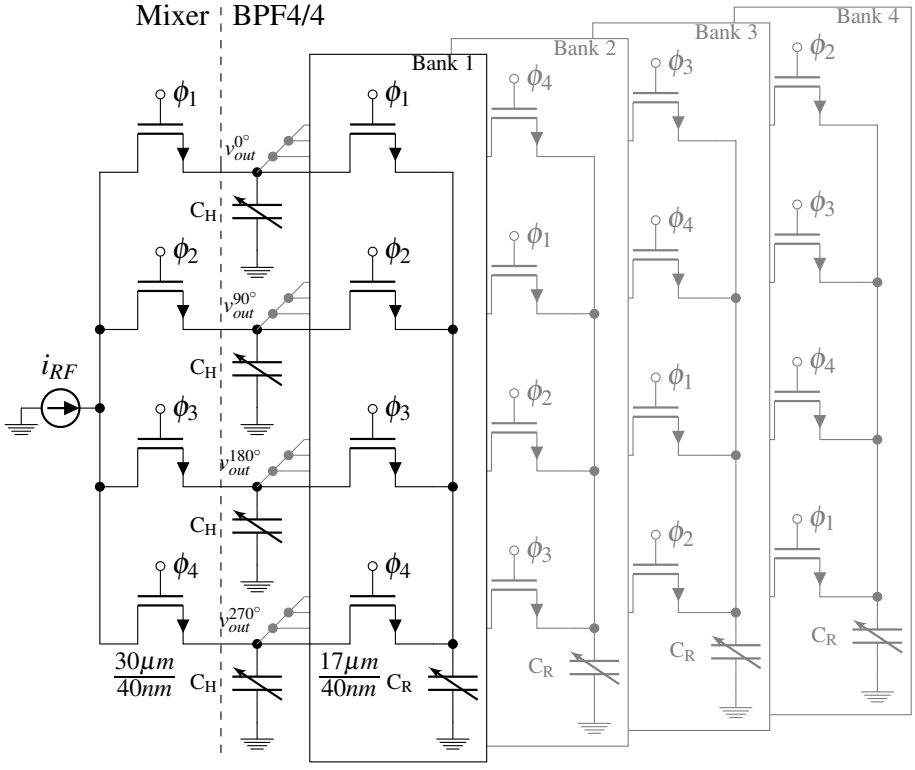
$$F_{MX\&BPF} \approx 1 + \frac{\overline{v_{n,sw}^2}}{\overline{v_{n,R_{out,LNTA}}^2}} + \frac{\overline{v_{n,sh}^2}}{\overline{v_{n,R_{out,LNTA}}^2}} \left(\frac{1}{4.3} \right)^2 + \frac{\overline{v_{n,IF}^2}}{\overline{v_{n,R_{out,LNTA}}^2}} \left(\frac{R_{out,LNTA}}{\zeta Z_{IF}} \right)^2, \tag{4.15}$$

where $\overline{v_{n,sw}^2}$ is the noise voltage of the mixer switches, $\overline{v_{n,sh}^2}$ is the noise voltage of R_{sh}, and $\overline{v_{n,IF}^2}$ is the up-converted noise from the IF stage, i.e. $\zeta \overline{v_{n,BPF4/4}^2}$. Eq. (4.15) shows the BPF 4/4 as the main contributor to this noise factor. Since increasing ζZ_{IF} affects the input impedance of the mixer, the noise factor can only be effectively reduced by reducing $\overline{v_{n,IF}^2}$. In [5] the analysis has been done considering the interface with a 50 Ω antenna, which is not the case in this design. Thus the model has to be adjusted to the LNTA interface. For simplicity, hereafter, only the real part of the output impedance of the LNTA will be considered.

4.5.2 First-order Bandpass Filter

The main advantage of the BPF 4/4 is its high-frequency operation; and, its main disadvantage is the low Q-factor (ideally 0.5). The low Q-factor of the BPF 4/4 limits

Figure 4.15: Schematic of the passive mixer and the BPF 4/4.



linearity improvement on the LNTA. Figure 4.15 shows the BPF 4/4, where C_H is the history capacitor, that stores the charge until sampling and C_R is the rotating capacitor, that shares the charges with other branches. The time-domain output voltage of each branch are

$$v_{out}^{0^\circ}[n] = a\,v_{out}^{0^\circ}[n-1] + (1-a)\,v_{out}^{270^\circ}[n-1] + k\,q_{in}^{0^\circ}[n], \tag{4.16}$$

$$v_{out}^{90^\circ}[n] = a\,v_{out}^{90^\circ}[n-1] + (1-a)\,v_{out}^{0^\circ}[n-1] + k\,q_{in}^{90^\circ}[n], \tag{4.17}$$

$$v_{out}^{180^\circ}[n] = a\,v_{out}^{180^\circ}[n-1] + (1-a)\,v_{out}^{90^\circ}[n-1] + k\,q_{in}^{180^\circ}[n], \tag{4.18}$$

$$v_{out}^{270^\circ}[n] = a\,v_{out}^{270^\circ}[n-1] + (1-a)\,v_{out}^{180^\circ}[n-1] + k\,q_{in}^{270^\circ}[n], \tag{4.19}$$

where the $a = {}^{C_H}/_{(C_H+C_R)}$ and $k = {}^{1}/_{(C_H+C_R)}$. Applying the Z-transform on (4.16) - (4.19) The complex Z-domain transfer function of the BPF 4/4 is [64]

$$H_{4/4}(z) = \frac{v_{out}}{q_{in}} = \frac{k}{(1-az^{-1}) - j(1-a)z^{-1}}. \tag{4.20}$$

The central frequency of the filter is

$$f_{IF} = \frac{f_s}{2\pi} arctan\left(\frac{C_R}{C_H}\right). \tag{4.21}$$

Moreover, since the $f_s \gg f_{IF}$, (4.20) can be converted to the S-domain using the bi-linear transformation, $z = {}^{(2+sT_s)}/_{(2-sT_s)}$, when $sT_s < 2$; thus

$$H_{4/4}(s) = \frac{v_{out}}{I_{in}} = \frac{R_{eq}}{1 - j\,(1 - R_{eq}C_H\omega)}, \tag{4.22}$$

where $R_{eq} = {}^{1}/_{(f_sC_R)}$ is the discrete-time equivalent resistance of C_R. Moreover, $Z_{IF}(s) = H_{4/4}(s)$ since the input and output nodes are the same; therefore, $Z_{IF} = R_{eq}$ at the BPF central frequency. The dashed red line on figure 4.12 shows the BPF 4/4 transfer function.

In sampled systems not only the noise generated directly by the switches has to be taken into consideration but also the wideband noise folded back into IF when sampled. The noise produced by a SC is divided into two parts: the direct noise and the sample-and-hold noise. The former is equal to the noise generated by the switch and appears directly across the capacitor during the ON-phase, in which the switch is closed and modeled by a resistance (R_{sw}). During the OFF-phase this noise is zero. The latter corresponds to the last value of the direct noise which remains stored across the capacitor during the OFF-phase, in which the switch is open [39]. If $f_s \gg f_{IF}$ the two-sided direct noise density is [39]

$$S^d(f) \approx 2mkTR_{sw} \tag{4.23}$$

and the two-sided sample-and-hold noise density is [39]

$$S^{s/h}(f) \approx \frac{(1-m)^2kT}{f_sC_R}, \tag{4.24}$$

where m is the duty-cycle, k is the Boltzmann constant, and T is temperature. Since the sample-and-hold noise dominates the noise of the SC at low frequencies, reducing R_{sw} has minimum impact on the overall thermal noise; on the other hand, increasing C_R reduces the dominant sample-and-hold noise [39]. Moreover, since $R_{eq} = {}^{1}/_{f_sC_R}$, reducing R_{eq} reduces the overall noise produced by the BPF.

Since the selection of C_H and C_R controls the input resistance and central frequency of the filter, their capacitances must be variable to make the BPF flexible. Therefore, two banks of capacitors, controlled by 8-bits, compose C_H and C_R; the former sweeps from 6 pF to 60 pF, and the latter sweeps from 200 fF to 2 pF. Moreover, since the BPF 4/4 needs large C_H capacitances to achieve a low R_{eq}, C_H is differential to improve its capacitance per area.

The post-layout simulation results of the LNTA and first filtering stage are presented in figure 4.16a and figure 4.16b. Since the input impedance of the mixer is higher at 500 MHz, the gain at this frequency is about 5 dB higher than that at the other frequencies. The input impedance of the mixer naturally falls as the frequency increases thanks to the reduction of the input impedance of the BPF 4/4. Although this variation has been mitigated by designing the mixer with a very small R_{sw}, it is still necessary to re-program the bank of capacitors to keep the gain steady. Consequently, the gain variation is small from 1 to 4 GHz. Since the output impedance of the LNTA is higher at frequencies below 1 GHz, it is possible to have a higher gain at those frequencies by increasing the input impedance of the mixer. The same cannot be done at frequencies above 1 GHz because the output impedance of the LNTA might not be high enough to drive the mixer. Despite this gain variation, the NF only varies 0.5 dB from 500 MHz to 4 GHz, as shown in figure 4.16b. The Q-factor of the BPF 4/4 also reduces as the frequency increases, but it remains higher than 0.4.

The flexibility of the filter is shown in figure 4.17. By controlling the value of the capacitors C_H and C_R, the central frequency of the filter is modified which allows for the same filter to be used with different standards.

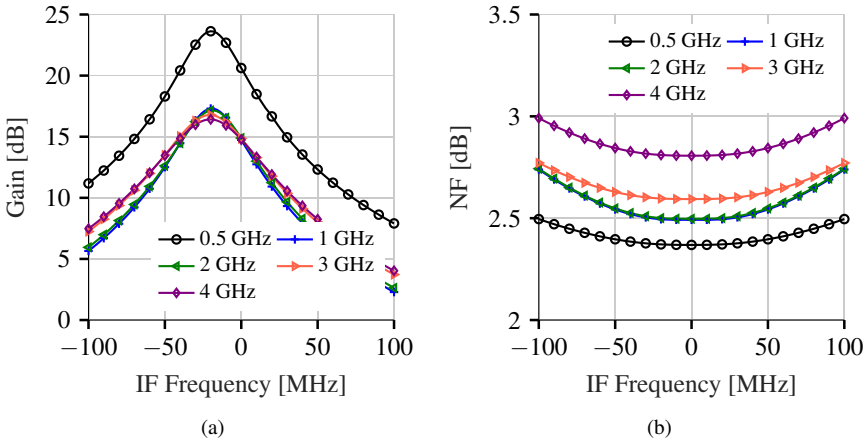


Figure 4.16: (a) Voltage gain and (b) noise figure post-layout simulation results of combined LNTA, mixer and first filtering stage.

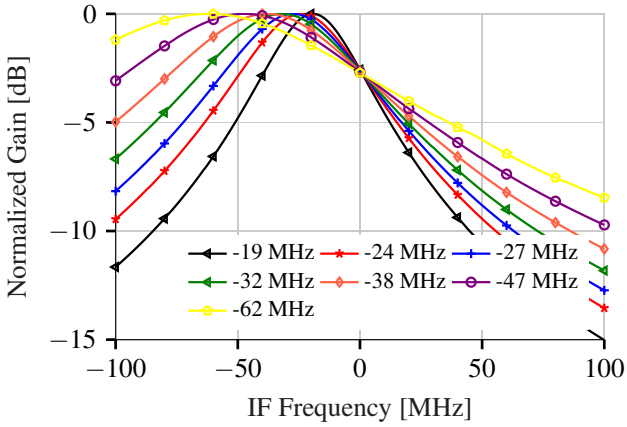


Figure 4.17: Normalized transfer function sweeping the central frequency, which is shown at the legend.

4.6 Second filtering stage

The second filtering stage is composed by IF transconductors (GM-cells) driving a passive DT BPF. Since the noise contribution from these cells are mitigated by LNTA gain, this filter can work at a lower sampling frequency than the previous filtering stages. Consequently, a second-order filter with a Q-factor higher than one can be adopted here. Additionally, a cross-connection between positive and negative nodes in the direct (I) and quadrature (Q) input of the filter boosts the Q-factor with a minimum increment on power consumption and complexity of the filter.

4.6.1 GM-Cells

The GM-cell converts the output voltage from the previous stage to the current input required for the DT filter. Moreover, since the mixer and the BPF are passive, LNTA and GM-cells are the only sources of gain in the receiver.

As shown in figure 4.5, the GM-cells are in the fourth stage of the chain; thus, noise is not a primary concern since the LNTA mitigates their noise contribution. On the other hand, the 0.9 V supply headroom limits its linearity.

Figure 4.18 shows the schematic of the GM-cells are based on CMOS inverters which is a topology more suited to supply voltage reduction constraints [75]. The common-mode feedback (CMFB) sets the output common mode. Besides, by biasing the PMOS

and NMOS devices so that their transconductances are the same improves the IIP2 and IIP3 [104, 48]. The post-layout simulation predicts 10 dBm IIP3. Eventually, the IIP3 can be further enhanced with thick-oxide transistors, which support a supply voltage up to 2.5 V; however, that design option has not been used since it would significantly increase power consumption. The stability analysis of the CMFB loop shows a phase margin of 70°, which guarantees that the GM-cell is stable.

The output impedance of the GM-cell has to be at least three times the input impedance of the next BPF. To achieve this requirement, long-channel transistors are used in this design. Moreover, a common-mode feedback keeps the output node properly biased at $^{VDD}/_{2}$.

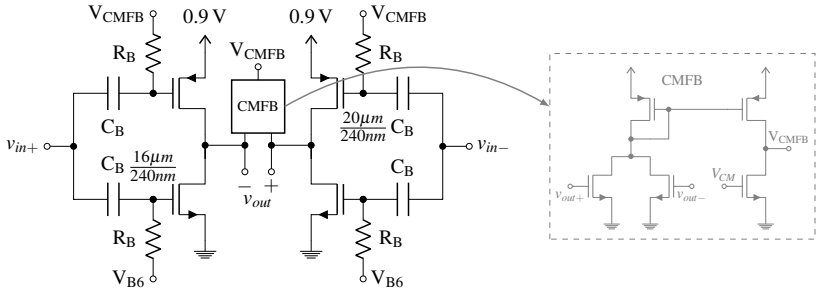


Figure 4.18: The GM-cell.

4.6.2 Modified Second-order Bandpass filter

The second filtering stage is a second-order bandpass filter (BPF 4/8) [34] with cross-connections at I and Q inputs, as shown in figure 4.19. A similar circuit modification was implemented in a N-path filter, establishing a feedback loop in [25]. The cross-connection modification to the BPF 4/8 adopted here enhances its Q-factor, increases the image attenuation, and improves the filtering of out-of-band blockers. Nevertheless, the cross-connection maintain I and Q independent, hence not affecting quadrature which is mainly a consequence of clock generation as observed in [56].

The BPF 4/8 is a derivation from the BPF 4/4 by cascading an additional infinite impulse response (IIR) LPF and increasing its order. The transfer function in the z-domain is given by (4.25) [34].

$$H(z) = \frac{k(1-a)z^{-1}}{(1-az^{-1})^2 - j(1-a)^2 z^{-2}} \tag{4.25}$$

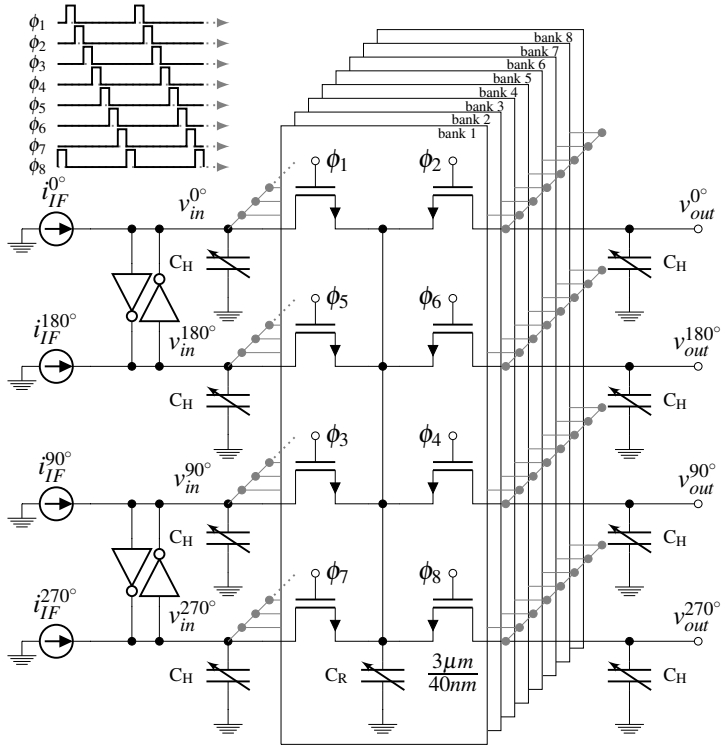


Figure 4.19: The BPF 4/8 modified circuit with implemented cross-connected transconductors.

Moreover, as presented in [89, 63], the BPF order can be further increased by adding more LPFs to it. Increasing the order of the filter improves the Q-factor; thus, improving image attenuation and out-of-band IIP3, as shown in figure 4.20. On the other hand, it implicates a higher number of switches and clock phases, hardly operating at high sampling frequencies since the switches have to be proportionally faster.

The image attenuation improves 6 dB from the BPF 4/4 to the BPF 4/8, a further increment of the BPF order adds less than 3 dB per order (figure 4.20). This behavior is a consequence of the loss of symmetry at the BPF as its order increases. The higher order also increases substantially the number of switches and capacitors, increasing area and power consumption. Since the number of switches is $n_{sw} = (ord)^2 2^4$, where *ord* is the order of the filter, the number of C_H and C_R are increased by 4 each time the order is increasead by 1. Moreover, the increase in the number of switches also increases the number of dividers and buffers to drive them, and the overall system power consumption. Based on the number of switches, the increase in power consumption

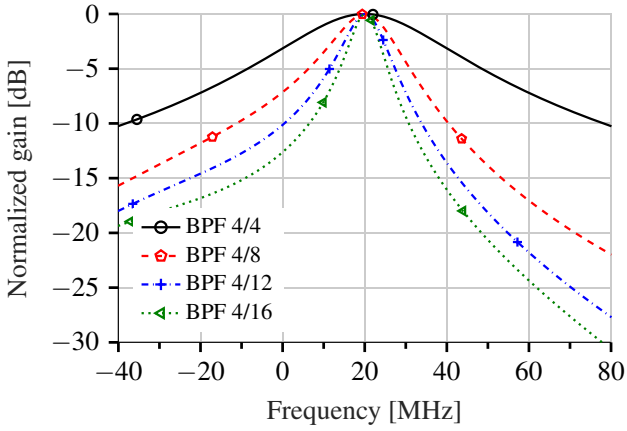


Figure 4.20: Transfer function of the BPF 4/4, 4/8, 4/12, 4/16.

can be estimated. If the only difference between the filters is the order, a first order BPF will consume four times less power than a second order BPF and sixteen times less power than a fourth order BPF. Consequently, increasing the BPF order beyond two which corresponds to BPF 4/8 is hardly worth the cost in complexity and power consumption.

By adding the cross-connected transconductors, as proposed in figure 4.19, it is possible to increase the Q-factor with minimum impact in power consumption and area. Based on figure 4.19, the discrete time output voltages at $T = nT_s$ can be found as:

$$v_{out}^{0^\circ}[n] = a v_{out}^{0^\circ}[n-1] + (1-a) v_{in}^{0^\circ}[n-1], \tag{4.26}$$

$$v_{in}^{0^\circ}[n] = a v_{in}^{0^\circ}[n-1] + (1-a) v_{out}^{270^\circ}[n-1] + k q_{in}^{0^\circ}[n] + (1-a)\beta v_{in}^{180^\circ}[n], \tag{4.27}$$

$$v_{out}^{90^\circ}[n] = a v_{out}^{90^\circ}[n-1] + (1-a) v_{in}^{90^\circ}[n-1], \tag{4.28}$$

$$v_{in}^{90^\circ}[n] = a v_{in}^{90^\circ}[n-1] + (1-a) v_{out}^{0^\circ}[n-1] + k q_{in}^{90^\circ}[n] + (1-a)\beta v_{in}^{270^\circ}[n], \tag{4.29}$$

$$v_{out}^{180^\circ}[n] = a v_{out}^{180^\circ}[n-1] + (1-a) v_{in}^{180^\circ}[n-1], \tag{4.30}$$

$$v_{in}^{180^\circ}[n] = a v_{in}^{180^\circ}[n-1] + (1-a) v_{out}^{90^\circ}[n-1] + k q_{in}^{180^\circ}[n] + (1-a)\beta v_{in}^{0^\circ}[n], \tag{4.31}$$

$$v_{out}^{270^\circ}[n] = a v_{out}^{270^\circ}[n-1] + (1-a) v_{in}^{270^\circ}[n-1], \tag{4.32}$$

$$v_{in}^{270^\circ}[n] = a v_{in}^{270^\circ}[n-1] + (1-a) v_{out}^{180^\circ}[n-1] + k q_{in}^{270^\circ}[n] + (1-a)\beta v_{in}^{90^\circ}[n]. \tag{4.33}$$

By converting the equations (4.26) - (4.33) to the z-domain, the transfer function for the BPF 4/8 is derived as

$$H(z) = \frac{k(1-a)z^{-1}}{(1-az^{-1})^2 + (1-az^{-1})(1-a)\beta - j(1-a)^2 z^{-2}}. \tag{4.34}$$

The new term $(1-az^{-1})(1-a)\beta$ is created by the cross-connection, where β is the cross-connection gain - i.e., the gain of each transconductors at the input of the BPF. Therefore, β can be calculated by $\beta = -G_m R_{eq}$, where G_m is the transconductance of the inverters at the input of the BPF 4/8 shown on figure 4.19 and R_{eq} is the switched-capacitor equivalent resistance of the BPF 4/8 (without the cross-connection), which equals its input impedance at the central frequency.

The stability of the new TF can be studied from the poles movement in the z-plane as β is varied. Figure 4.21 presents a zoomed plot of the pole-zero map when β is varied between 0, which corresponds to BPF 4/8 without cross-connection, and -0.5. The two complex poles observed in the figure are not conjugates since the transfer function implements a complex filter. Also, when $\beta = -0.5$, one of the poles is on the unit circle and the transfer function gets unstable.

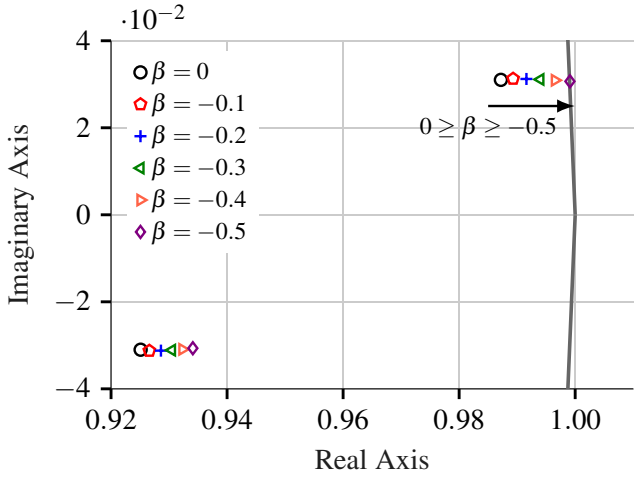


Figure 4.21: Pole-zero mapping of the modified BPF 4/8 TF.

Figure 4.22 shows the plotted transfer function of the BPF 4/8 with the circuit modification. The best Q-factor would be obtained when $\beta = -0.5$ with an image attenuation as high as 36 dB. Unfortunately, β must be higher than -0.5 for stability.

Central frequency of the BPF is

$$f_{IF} \approx \frac{f_s}{2\pi} arctan\left(\frac{(1-a)sin(\pi/4)}{a+(1-a)cos(\pi/4)}\right), \tag{4.35}$$

as long as $\beta > -0.5$.

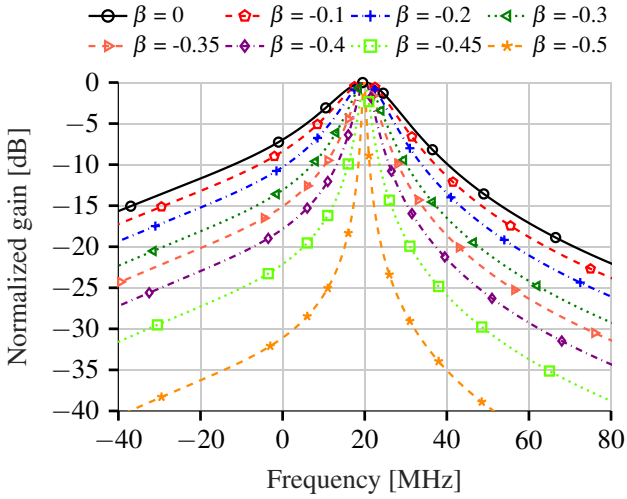


Figure 4.22: Transfer function of the modified BPF 4/8, where β is the cross-connection gain.

The sampling frequency versus noise trade-off discussed in Section 4.5.2 is still valid. Another metric that has a trade-off with the sampling frequency is the Q-factor. If the sampling frequency is too high the switches might not open and close completely; thus, the BPF loses selectivity. In this sense, to improve the noise figure the BPF 4/8 has to sacrifice some selectivity.

The post-layout simulation shows that if the sampling frequency is 4 GHz, the BPF 4/8 loses about 3 dB in image attenuation due to a reduced selectivity. Thus, the circuit modification on the BPF 4/8 was used to compensate for that loss with $|\beta| = 0.2$. In the end, the image attenuation is about 11 dB, and the noise figure of the GM-cells plus the BPF 4/8 with cross-connected transconductors is around 15 dB. Figure 4.23a and figure 4.23b compare the post-layout results of gain and noise of the BPF 4/8 and its improved version with $|\beta| = 0.2$. Also, the post-layout voltage gain of the second filtering stage is 12.8 dB with a total voltage gain of 36.4 dB and 29.8 dB at 500 MHz and 1 GHz respectively for the complete receiver. Like the BPF 4/4, the central frequency of the modified BPF 4/8 is also controlled by the capacitors C_H and C_R, as shown in figure 4.24.

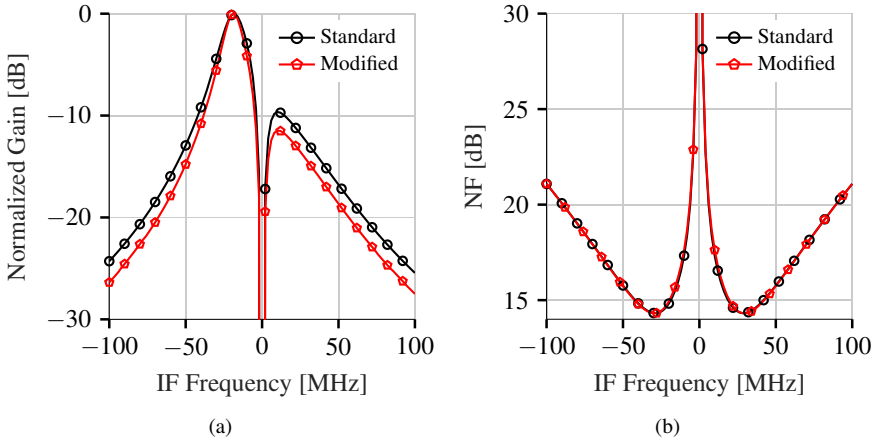


Figure 4.23: (a) Normalized gain and (b) Noise figure of the standard and modified BPF 4/8 with $|\beta| = 0.2$.

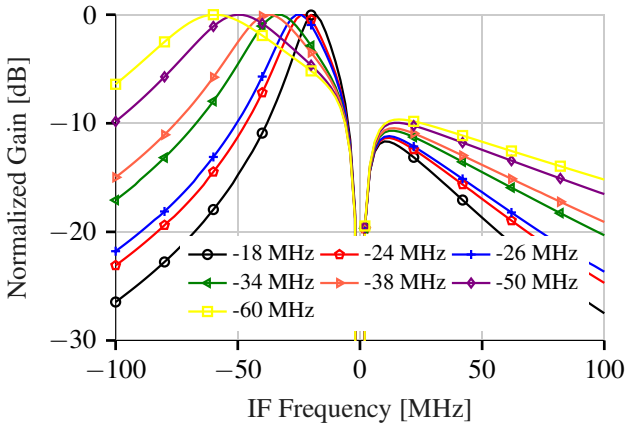


Figure 4.24: Normalized transfer function of the modified BPF 4/8 sweeping the central frequency, which is shown at the legend.

4.7 Image rejection ratio

The CS-BPF filters are known for their high image rejection ration (IRR) [63, 34], and the modification with the transconductors does not affect the IRR results. The post-layout simulation of the entire receiver achieved an IRR of -60 dB, as shown in figure 4.25, and the Monte Carlo simulation for process variation shows that the

deviation from the mean is only 3.3 dB for 200 samples (figure 4.26). Since the performance of the filters strongly relies on the ratios between the capacitors C_H and C_R, mismatch is not a concern for the CS-BPF [63].

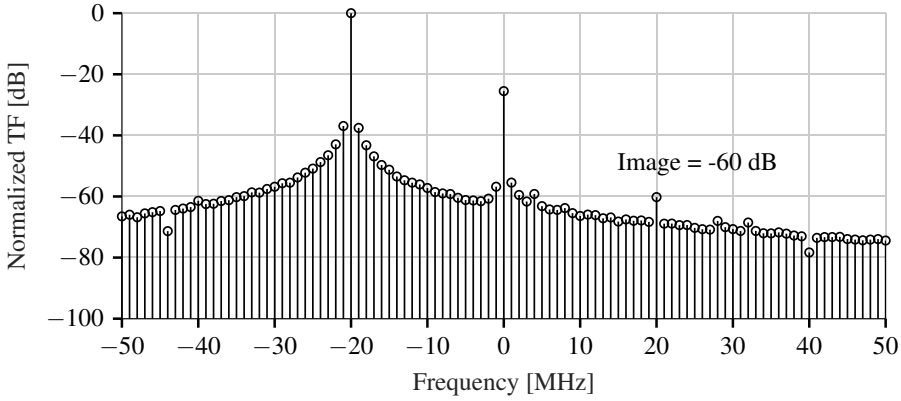


Figure 4.25: Normalized transfer function.

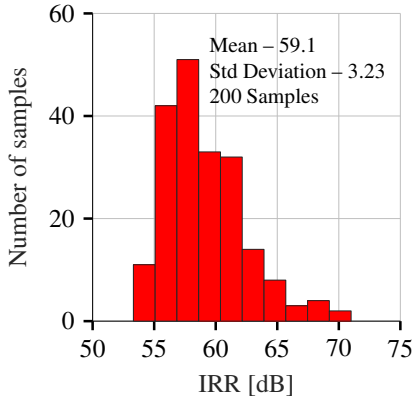


Figure 4.26: IRR Monte Carlo (process variation) simulation results of the receiver.

4.8 Clock Generation

The receiver requires two non-overlaping clocks: one with 25% duty-cycle, that drives the mixer and the BPF 4/4, and the other with 12.5% duty-cycle, which drives the

BPF 4/8. These clocks are generated on-chip based on a pure sinusoidal signal, which is generated off-chip.

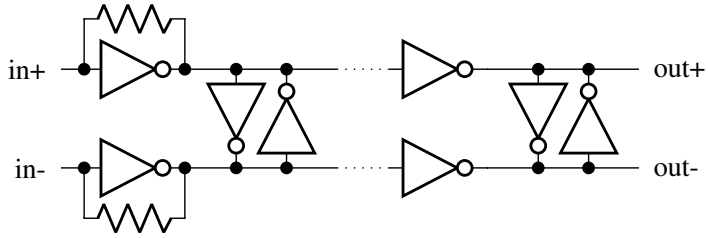


Figure 4.27: The delay line, which converts the input sinusoidal wave to a square wave.

First, a delay line (figure 4.27) [77] converts the sinusoidal input signal into a rail-to-rail square wave with 50% duty-cycle. This delay line not only creates the square wave but also alignes the two phases of the input clock. Moreover, the delay line needs a 100 Ω resistor in parallel with its input, providing the impedance match with the external signal generator.

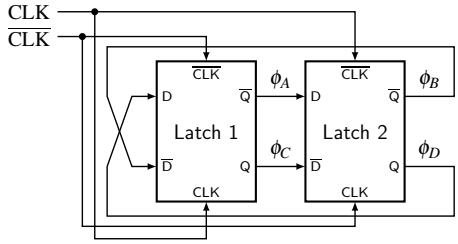


Figure 4.28: The Frequency divider-by-2.

Then, two synchronous frequency dividers create the multiphase clock. The divide-by-2 (figure 4.28) creates the 4-phase clock, and the divider-by-4 creates the 8-phase clock. Both dividers use a chain of latches that are connected back-to-back. The divide-by-2 needs two latches, whereas the divide-by-4 needs four latches. The output of the dividers, which have a 50% duty-cycle, are combined with logical circuits likewise the circuit in figure 4.29, creating the non-overlaping clock with 25% duty-cycle and 12.5% duty-cycle.

figure 4.30a shows the latches designed with tristate inverters, and figure 4.30b shows tristate inverter topology. Since a transmission gate is used for enabling this tristate, the charge and discharge of the load are faster than other tristate inverters topologies [77].

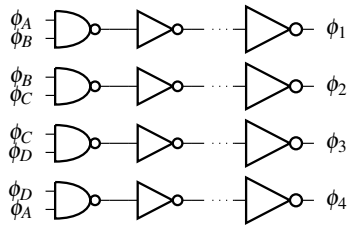


Figure 4.29: The logic circuit that creates the 25% non-overlaping clock.

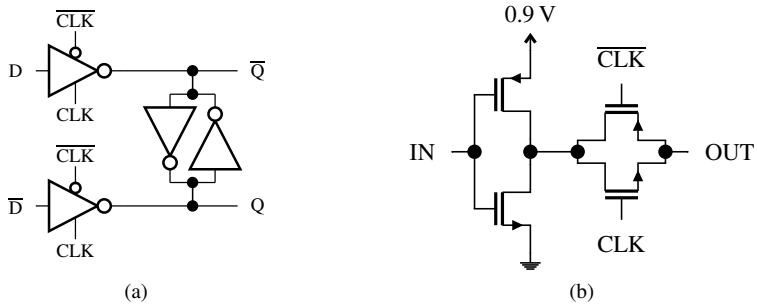


Figure 4.30: (a) The latch and (b) the tristate inverter with a transmission gate.

4.9 Receiver Measurement Setup

In order to fully test the circuit, four measurement setups are used. These setups are presented in figures 4.31, 4.32, 4.33, and 4.34.

The DUT (dispositive under test) needs two clock signals, one per filtering stage, which are generated by an Arbitrary Waveform Generator (AWG) or an analog signal generator (PSG). The former has been used for frequencies below 3 GHz, and the latter has been used for frequencies above 3 GHz. The waveform generated by either the AWG or the PSG is pure sinusoidal because pure sinusoidal signals are easy to generate and to transmit to the chip. Moreover, the clock aligner creates the square wave on-chip in addition to fix an eventual mismatch between the input clock phases. The AWG can produce differential signals, whereas the PSG only produces single-ended signals. Hence, an external balun is needed when using the PSG.

An Arduino controls the bank of capacitors of the two BPFs using a Serial Peripheral Interface (SPI) bus. The Arduino sends two signals (clock and data input) to the DUT, and it receives back the data output (output of the on-chip shift-register) to check if the data has arrived correctly to the DUT.

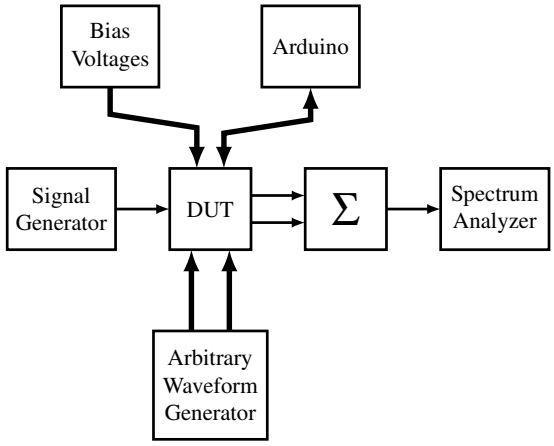


Figure 4.31: Gain measurement setup.

The I and Q outputs are differential, whereas every measurement equipment is single-ended. Hence, these output signals are combined by an external balun.

The test-setup for gain is presented in figure 4.31. The Vector Signal Generator (SMBV) creates the input signal, while the Spectrum Analyzer (FSW) observes the output signal. The clocks frequencies are kept constant so that the LO frequency is constant. The input frequency, on the other hand, is swept from $f_{RF} - 100$ MHz to $f_{RF} + 100$ MHz so that the transfer function of the receiver can be observed in the FSW. After that, the frequency of the first clock (CLK1 in figure 4.5) is increased in such way that the frequency of LO changes with a 500 MHz step. This procedure has been repeated until the entire band from 500 MHz to 4 GHz is covered. The frequency of the second clock (CLK2 in figure 4.5), on the other hand, is kept constant at 500 MHz.

The test-setup for NF requires an FSW with the option for NF measurement and a noise source. Previously to the measurement, the test-setup must be calibrated. Hence, the noise is observed without the DUT. After that, the pieces of equipment are connected like in figure 4.32, and the NF is measured for frequencies around the central frequency of the receiver. Like in the previous test-setup, the input and LO frequencies are changed after each measurement so that the entire band is covered. Furthermore, the average parameter must be carefully set for this measurement since the noise has a random characteristic. An average of few points will give a fast but imprecise measurement. On the other hand, an average of several points will be extremely precise, but the measurement will take an enormous amount of time. Thus, this test-setup uses an average of sixteen points that offers a good compromise between precision and test-time.

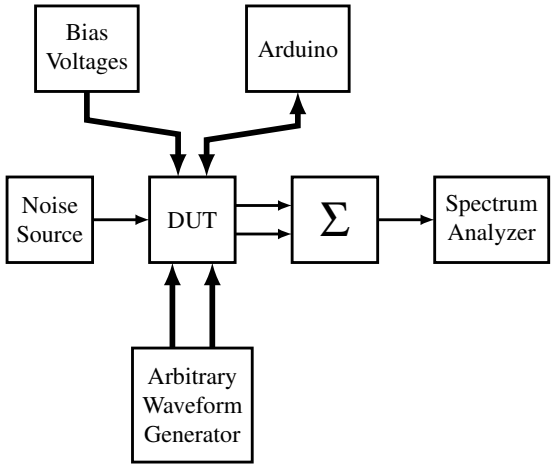


Figure 4.32: Noise figure measurement setup.

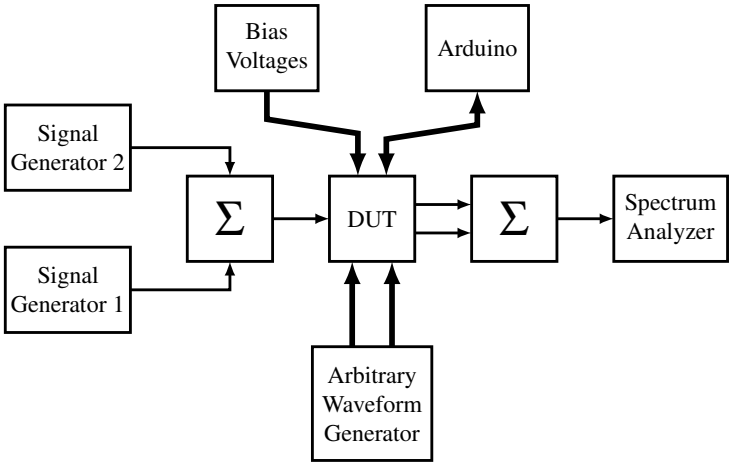


Figure 4.33: IIP3/IIP2 measurement setup.

Being a two-tone test, the test-setup for IIP2 and IIP3 requires a pair of SMBVs to generate each one of the tones like shown in figure 4.33. A hybrid combines these signals before feeding them to the DUT. The intermodulation products and the main signals are observed in the FSW.

The input reflection coefficient (S11) has been tested as shown in figure 4.34. The input of the DUT is connected to a Network Analyzer which sweeps the frequency and

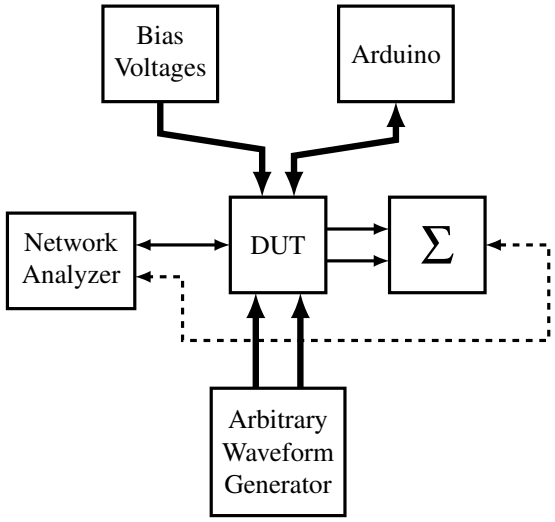


Figure 4.34: S-parameters measurement setup.

verifies the s-parameters. Although this test-setup evaluates all s-parameters, only S11 has been tested in the presented design since the other ones, such as S21, S22, and S12, are meaningless to our design.

The measurements were done with a chip-on-board assembly, which is shown in figure 4.35. The high-frequency signals are routed on PCB using grounded coplanar waveguides to preserve signal integrity.

4.10 Receiver Measurement Results

The entire chip, as shown in figure 4.36, occupies an area of 1300 x 900 μm^2 with a highlighted core area of only 630 x 218 μm^2. Most of the die area around the core is occupied by power supply decoupling capacitors. We were able to test completely two samples, and to partially test four samples.

The floorplan was designed to reduce the length of the clock routing lines, especially in the CS-BPF 4/4 which must have a low input impedance. Also, the I and Q paths need to be symmetrical to minimize the I-Q mismatch. Therefore, the mixer and the four phase clock generator are merged into the CS-BPF 4/4, as shown in figure 4.36, being placed on the central region of the layout with the I path at the top and the Q path at the bottom. This approach reduces the input resistance and the capacitance of the clock routing lines, besides keeping the design symmetrical. In the CS-BPF 4/8 layout, the

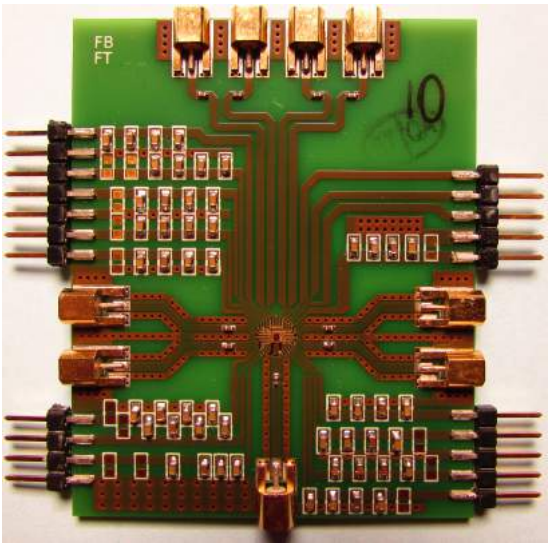


Figure 4.35: Measurement PCB.

primary concern is the symmetry of the clock traces, so that the phase shift between the lines remains the same.

The receiver power consumption varies from 22.5 mW to 33.41 mW, as the programmed LO frequency is raised from 0.5 to 4 GHz. The analog blocks, mainly the LNTA and the GM-cells, consume around 11.7 mW, reasonably constant with the LO frequency. The power consumption of the clock generation, on the other hand, varies with the clock frequency, from 10.8 mW @500 MHz to 21.71 mW @4 GHz. These blocks include the clock aligner, frequency dividers, and the buffers that drive the mixer and the BPFs. Figure 4.37 shows the power budget variation for eight different LO frequencies. The power increase is dominated by the Mixer and CS-BPF 4/4 clock generation.

The LNTA provides a wideband input match; the S11 is around -10 dB from 200 MHz to 4.5 GHz. Figure 4.38 shows S11 results from four samples. In comparison with simulation, the results are slightly different at high frequencies due to the length of the bondwire, which cannot be precisely controlled in the assembling process.

Figure 4.39 presents the receiver voltage gain measured for the I path. The recombination of the I and Q path adds 6 dB to these. For the gain measurements, the RF input and LO frequencies were swept to cover the range of IF frequencies shown in figure 4.39, and an external balun was used to combine the differential outputs. A maximum voltage gain of 30 dB is achieved at 500 MHz LO frequency. Due to the presence of parasitic capacitances, as the frequency increases the gain drops to 17 dB at

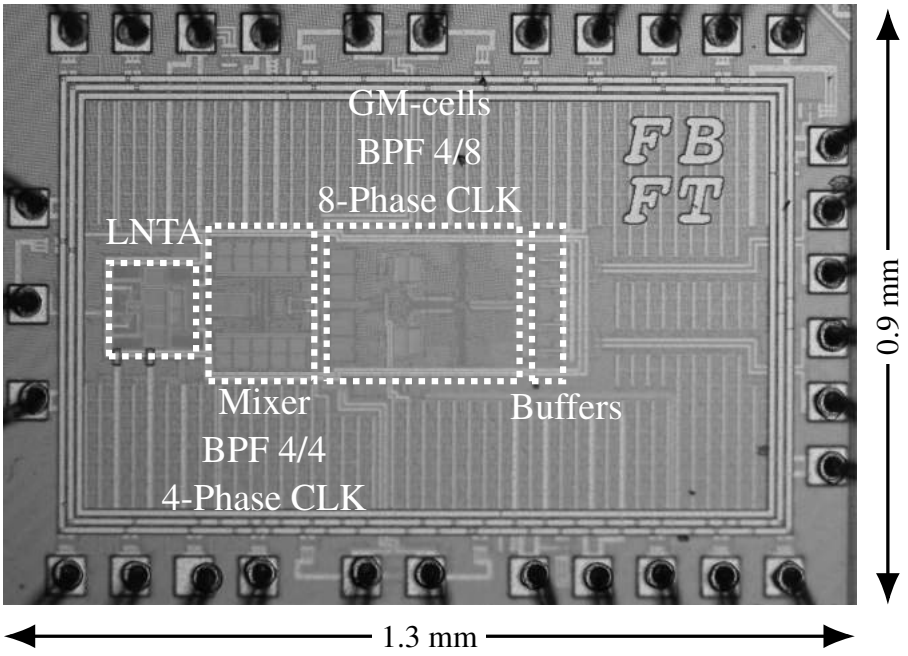


Figure 4.36: Chip photograph.

4 GHz LO frequency (figure 4.40). Figure 4.39 also shows that the image attenuation is 16 dB at the highest gain and 17 dB at the lowest gain.

The receiver gain reduced 5 dB from simulation to measurements at low frequencies (figure 4.41), and this gain drop increases with frequency causing NF degradation. According to our simulations and lab experiments, the mixer is the probable culprit for this gain drop. This matter will be further discussed on appendix A. In frequencies below 1 GHz, it is possible to re-program the capacitor banks of the first filter to achieve a higher mixer input impedance, increasing the gain and reducing the overall NF. However, the same strategy cannot be employed much above 1 GHz because the output impedance of the LNTA is reduced at higher RF input frequencies.

Figure 4.42 shows the measured NF for different LO frequencies. These measurements were performed by sweeping the input frequency with a span of 20 MHz at a fixed LO. The minimum NF is 3.3 dB. However, since the gain reduces at LO frequencies above 1 GHz, the NF increases, reaching a maximum of 8 dB at the central frequency (-21 MHz).

The NF was also measured under the presence of strong blockers positioned at 30 MHz

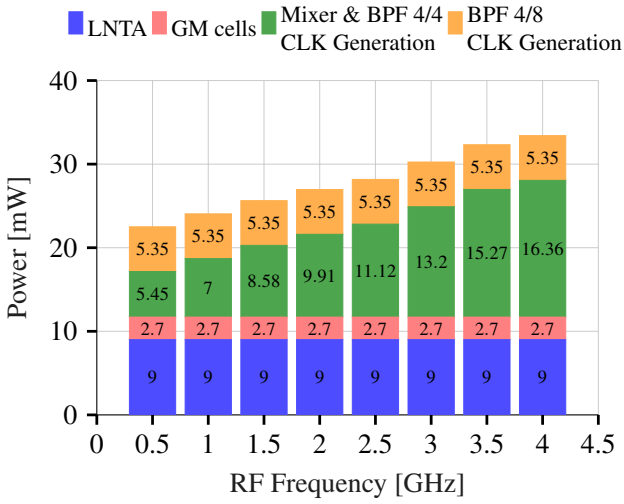


Figure 4.37: Power budget.

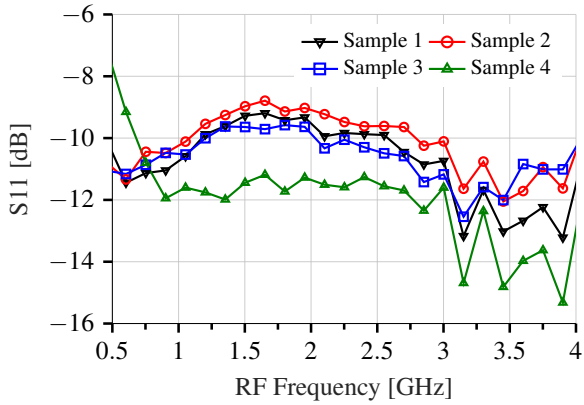


Figure 4.38: S11 measurement results from four samples.

and 80 MHz away from the central frequency. The presence of a 0 dBm blocker on those positions raises the NF to 20 dB due to LNTA compression. The resilience to strong blockers is a limitation of this LNTA due to the cascode and the transistor M6. The utilization of thick-oxide transistors with a supply higher than 0.9 V at the cascode would solve the compression point problem [15], but it would harm the input match at high-frequencies due to the large input capacitance of these transistors. A high-Q BPF before the LNTA like proposed in [71] would be another possibility. However, it

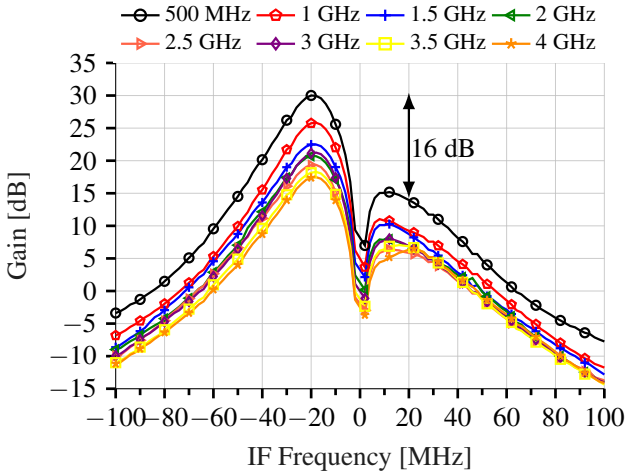


Figure 4.39: Gain measured at the I path at different RF frequencies, the legend shows the LO frequency in which the measurement has been performed.

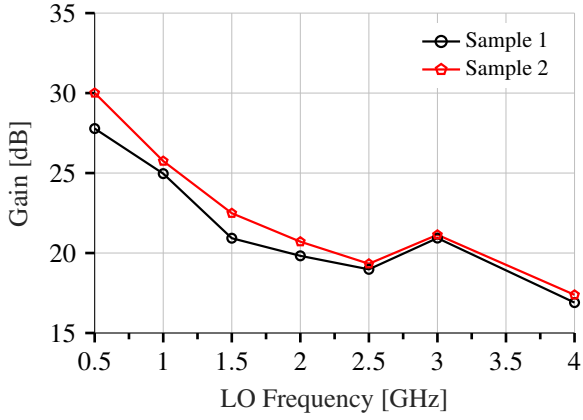


Figure 4.40: Gain measurement results at the central frequency while the LO frequency is swept from 0.5 to 4 GHz.

would increase the overall NF of the receiver.

The IIP3 and IIP2 results, presented in figure 4.43 and in figure 4.44, respectively are chiefly determined by the LNTA since the interferers are not yet filtered at this point. After the LNTA, the first and second BPF will attenuate those interferers, improving both the IIP3 and IIP2. Since the gain of the LNTA changes with frequency, it is

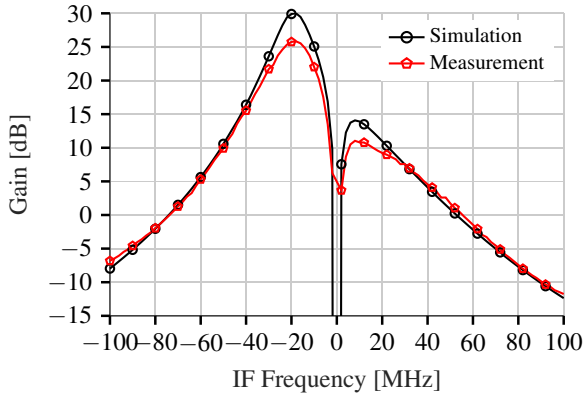


Figure 4.41: Gain simulation results versus measurement results.

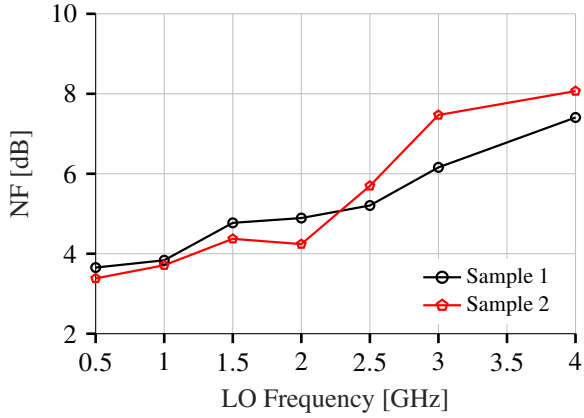


Figure 4.42: Noise Figure measurement results at the central frequency while the LO frequency is swept from 0.5 to 4 GHz.

also expected that both IIP3 and IIP2 change as well. Although the modulated input impedance of the mixer provides some attenuation of the intereferers, it is not large enough to produce a meaningful improvement as the interferers are moved further away from the central frequency.

The measurements performed at 500 MHz show an IIP3 about 5 dBm lower than that at 1 GHz, whereas the IIP3 at 2 GHz is about 5 dBm higher than that at 1 GHz, presented in figure 4.43b. Similarly, the IIP2 values also rise with the frequency. Thus, the highest values are achieved at 2 GHz. The IIP3 can be improved by harmonic cancellation

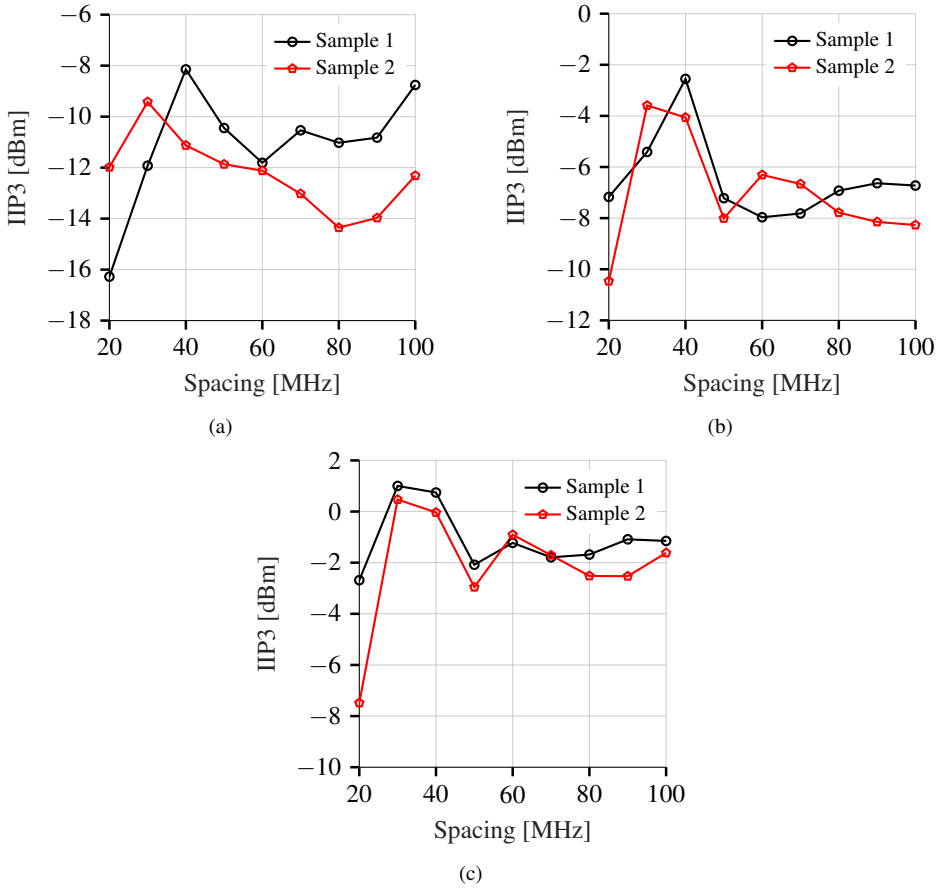


Figure 4.43: The IIP3 measurement results at (a) 500 MHz, (b) 1 GHz, and (c) 2 GHz.

using phase shifted paths [81]. However, mixer and filter would have to operate with at least 8 phases, increasing not only the complexity, but also the power consumption of the clock generation.

Unlike the low-/zero-IF receivers, the products of second-order intermodulation (IM2) generated by closed spaced tones are not an issue for the HIF receiver since these IM2 products are down-converted to frequencies far away from the central frequency. Nevertheless, the IIP2 is still limited by the single-ended topology of the LNTA. If a very high IIP2 is required, the LNTA topology proposed here can be easily converted either to fully differential or to single-ended-to-differential topology, which are both able to achieve IIP2 values as high as 40 dBm.

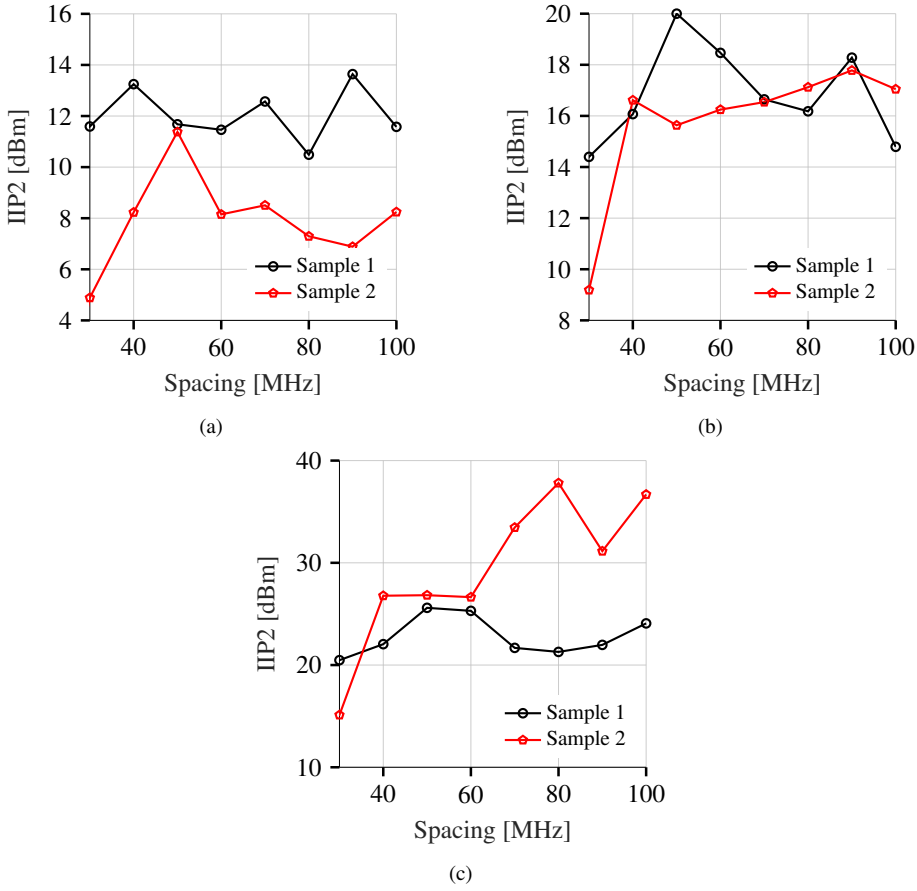


Figure 4.44: The IIP2 measurement results at (a) 500 MHz, (b) 1 GHz, and (c) 2 GHz.

Table 4.2 compares the presented high-IF receiver with similar state-of-the-art publications. The main difference between this design and the previous ones is the modified BPF. The cross-connection at input of the BPF improves the Q-factor with a minimum increase in power and area consumption. Hence, this receiver achieves the smallest area and a very low power consumption. Moreover, since the Q-factor is now function of β, it can be tuned, which increases the receiver flexibility. This design presents smaller area and lower power consumption than [63] which is implemented in a more advanced CMOS technology. In comparison with [71] and [88] a similar IIP3 was achieved, despite the higher supply voltage used in these designs.

Table 4.2: Receiver performance summary and comparison with other HIF receivers.

	[71]	[88]	[63]	This work
CMOS node [nm]	65	65	28	40
Gain [dB]	55	82 †	$29 \sim 35$	$17 \sim 30$
Operating RF [GHz]	$1.8 \sim 2.2$	$1.8 \sim 2.5$	$0.5 \sim 2.5$	$0.5 \sim 4$
OB-IIP3 [dBm]	-	-	$2 \sim 14$	-
IB-IIP3 [dBm]	$-8.3 \sim -6.3$	-7	-	$-10 \sim -2.5$
S11 [dB]	< -10	< -10	< -10	< -10
NF [dB]	2.8	$3.2 \sim 4.5$	$2.1 \sim 2.6$	$3.3 \sim 8$
0 dBm Blocker NF [dB]	N/A	N/A	14	19
Power [mW]	39	$55 \sim 65$	$22 \sim 40$	$22.5 \sim 33.41$
Harmonic rejection	No	No	Yes	No
Supply [V]	1.2/2.5	1.2/2	0.9	0.9
Area [mm^2]	0.76	1.1	0.52	0.137

†including the analog baseband.

4.11 Conclusion of the chapter

CMOS scaling enables new receiver architectures thanks to the implementation of mixer and filters using switched-capacitors. In fact, those implementations are already common in most of the recently published wideband receivers, as discussed in chapter 1. Hence, a receiver using a high-IF architecture, in which both mixer and bandpass filters have been implemented with switched-capacitors, have been presented in this chapter.

The receiver has been designed in 40 nm CMOS. The design is based on an entirely integrated single-ended inductorless LNTA, which uses a dual noise-cancellation and a new strategy to increase the output impedance with a folded-cascode. Since the LNTA is single-ended, the mixer does the single-to-differential conversion, which removes the need for a transformer at the input of the receiver. However, it also limits the IIP2 of the circuit. After that, two filtering stages have been implemented. The first filtering stage uses a first order CS-BPF, while the second filtering stage uses a second order modified CS-BPF, which has the selectivity enhanced by the using of cross-connected transconductors at the filter input. This modification boosts the Q-factor without increasing the complexity or power consumption of the filter, and it also can be used to control the Q-factor, increasing or decreasing the filter selectivity.

Overall, the receiver achieves a small area compared to the state-of-art and good power consumption up to 4 GHz. The measurement results have shown a 3.3 dB NF and -10 dBm IIP3 at the maximum gain, which is 30 dB. However, due to a mismatch

between the LO phases, the receiver could not keep the performance up to 4 GHz. The gain and NF at 4 GHz have degraded to 17 dB and 8 dB respectively. The power consumption is 22.5 mW at 0.5 GHz and 33.41 mW at 4 GHz.

Chapter 5

Conclusions and Future Work

5.1 General conclusions

This thesis has focused on the design of wideband circuits for receivers, which was motivated in chapter 1. In fact, three projects were developed during the author's Ph.D. program. Firstly, the specification of a spectrum-sensing receiver. Secondly, the design and test of two wideband low-noise variable-gain amplifiers in 130 nm CMOS. Finally, the design and test of a wideband receiver in 40 nm CMOS that uses charge-sharing filters.

Chapter 2 dealt with the specification of a hypothetical spectrum-sensing receiver that aims for the detection of the wideband standards WRAN, WiMax, and LTE. These are the principal wideband standards within the band 50 MHz to 4 GHz. In addition to the receiver specification, the receiver topology and the block-level specification has also been discussed. The latter has been verified through behavioral model simulation. The results of this work have been published in ICECS'13 [8]. Even though this SS receiver has never been implemented in silicon, it gave us insight in the challenges faced by a multi-band/multi-standard receiver.

Chapter 3 presented the design and measurement results of two 130 nm CMOS wideband low-noise variable gain amplifiers (LNVGA). These LNVGAs allow for the reception of either a strong or a weak signal. Whenever a strong signal is received, the LNVGA reduces the signal power to values that do not compress the following blocks such as the mixer. Moreover, the LNVGAs can achieve a sufficiently low NF, which allows for the reception of weak signals. The LNVGAs are shown a gain tuning range up to 45 dB, within a bandwidth of 3 GHz, in addition to an NF as little as 3.4 dB. In contrast to other published VGAs, these LNVGAs were the only ones that

achieve a substantial gain tuning range combined with a low NF. The significant gain tuning range has been achieved thanks to the proposed low imbalance active balun. The results of this work have been published in SBCCI'15 [10] and AICSP'17 [11]. Since multi-standards receivers need to cope with a vast range of signal powers, the ability of control the gain at the first stage of the receiver is very useful. Not only it avoids the compression of the following circuits, but also it absorbs part of the gain tuning range required in those receivers. For example, the hypothetical receiver of chapter 2 needs a 97 dB gain tuning range, which is a demanding requirement for the baseband VGA. By using the LNVGA, the required gain tuning range of the baseband VGA would be reduced, reducing the design complexity.

Chapter 4 dealt with the design and measured results of a 40 nm CMOS wideband high-IF receiver using a modified charge-sharing bandpass filter to boost the Q-factor. Since this last design has been done in an advanced CMOS node, it enables the receiver for a high IF due to the on-chip implementation of discrete-time bandpass filters. The high-IF receiver architecture is more robust to even-order distortion, DC-offset and flicker noise than the zero-IF and low-IF architectures. This receiver was not designed to support a particular communication standard. The first design goal is to cover a wide band, up to 4 GHz, facing the difficult challenges of such widened band. Also, we have aimed to explore in its design and fabrication the improvements in the LNTA and the charge-sharing complex filter architecture. Our receiver achieves an NF of 3.3 dB with a voltage gain of 30 dB, and the IIP3 ranges from -10 up to -2.5 dBm at 1 GHz. However, due to a mismatch between the LO phases, the receiver could not keep the performance up to 4 GHz. Also, it occupies a tiny area, merely 0.137 mm^2, which is the smallest one reported. The power consumption is likewise small, varying from 22.5 up to 33.41 mW. The results of this work have been published in TCASI'18 [9]. In comparison to the LNVGA design, since a more advanced technology has been used in this last design, we were able to extend the RF bandwidth despite the removal of the inductors.

5.2 The achivements of the thesis

The main contributions of this thesis are summarized in the following bullets:

- The LNVGA achieving a considerable large gain tuning range thanks to the low imbalance active balun proposed.
- The LNTA was improved using a second noise cancellation path, which canceled the noise of the second largest noise contributor. Also, the interconnection between the match stage and the output stage has been made through a folded-cascode, which raises the output impedance.

- The second discrete-time BPF in the 40 nm design has been modified by using cross-connected inverters at its input. This modification allows for the enhancement of the Q-factor with a small increment in the power consumption. Eventually, it is possible to achieve a performance equivalent to a 4/16 filter, but with the power and simplicity of a 4/8, hence with about 16 times fewer switches and also with less power. Although it is not implemented in the reported design, the Q-factor of the BPF can be tuned by changing the gain of the cross-connected inverters.

5.3 Future work

There are some possibilities of future works based on this thesis. The power consumption of the LNVGA is considerably high. In particular, when the two active baluns are turned on. Also, the IIP3 is low. Thus, there are two possible works related to the LNVGA.

- The simplification of the gain variation stage so that the power consumption is reduced. The replacement of the active baluns for less power hungry circuits is a possible way to reduce the power consumption. For example, a single transistor in which one output is taken at the drain while the other one is taken at the source does the single-ended to differential conversion.
- Design the gain variation stage in such way that it also works as the mixer. The removal of a stage between LNA and mixer increases the IIP3. Moreover, if the active balun is replaced by a passive mixer, it will also reduce the power consumption.

The main problem of the high-IF receiver is the compression point, so it suffers from desensitization in the presence of a stronger blocker. Due to the cascode at the LNTA and the 0.9 V supply voltage, the compression point is not high enough. Consequently, some improvements can still be implemented in the receiver.

- The utilization of stacked thin-oxide transistors at LNTA and a large supply voltage to improve the compression point. A straightforward way to increase the compression point is increasing the supply voltage of the LNTA. However, since thin-oxide transistors cannot support this large voltage supply, thick-oxide transistors are normally used. Although it solves the compression point issue, it harms the input impedance of the LNTA due to the large input capacitance of thick-oxide transistors. Another option is to stack thin-oxide transistors so that supply voltage higher than 0.9 V is allowed, like in line drivers [22].

- The design of a mixer-first high-IF receiver. Removing the LNTA is another way to improve the receiver compression point [74]. The mixer-first receiver is not only highly linear but also resilient to blockers. Additionally, it is low-noise if noise cancellation is implemented in the receiver chain. So far, those receivers have been only implemented using zero/low-IF topologies. A mixer-first high-IF receiver would merge the advantages of both topologies.
- The possibility of using the modified CS-BPF to control the Q-factor has been proposed and simulated herein, but this solution was not implemented in silicon. This is a proposal for future follow-on works.

Appendix A

Considerations regarding the gain reduction in the high-IF receiver

After the layout, the expected gain of the first (LNTA+Mixer+CS-BPF 4/4) and second (GM+CS-BPF 4/8) stages are 17 dB and 12.8 dB respectively, as shown in the figure A.1. Thus, the total expected gain was 29.8 dB at 1 GHz, yet the measurement results showed a gain of 25 dB at the same frequency.

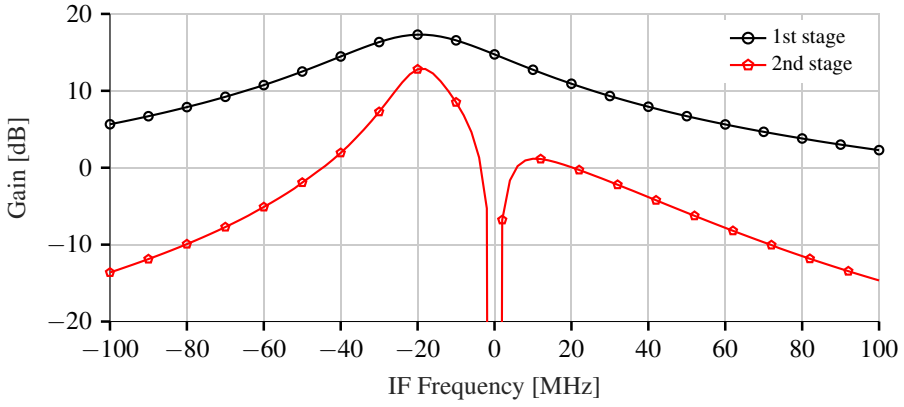


Figure A.1: Post-layout simulation results of the first and second stages.

Considering that the NF has also been hindered, the gain drop must have happened within the first stage. Based on that hypotheses, we have verified for possible problems in the LNTA, mixer, and CS-BPF 4/4. After some investigation, the mismatch between the clock phases of mixer and CS-BPF 4/4 seems to the source of the issue.

Therefore, we have explored two possibilities: In figures A.2a, A.2b, A.3a, A.3b, A.4a, and A.4b either one or two clock phases are shifted by the delta-time shown in the figures. In figure A.5 the excursion of the mixer clock is reduced from 0.9 V down to 0.5 V. In all simulations, the clock is 1 GHz.

Although the reduction of the clock amplitude reduces the gain (figure A.5), the gain drop is just 2 dB even with a large clock amplitude drop (a 0.5 V clock excursion). In figures A.2a, A.3a, and A.4a only the clock phase of the mixer is varied, and the gain drop is around 2 dB in the worst case. On the other hand, when the clock phases of both the mixer and the CS-BPF 4/4 are mismatched in phase, a gain drop as large as 6 dB is observed. Indeed, the figure A.4b seems to present a good match to the measurement results. The voltage gain suffers a considerable drop, while the Q-factor of the filter suffers minimum variation, as we have seen in our measurements. Hence, we believe that clock phase mismatching is the cause of the gain drop in the receiver.

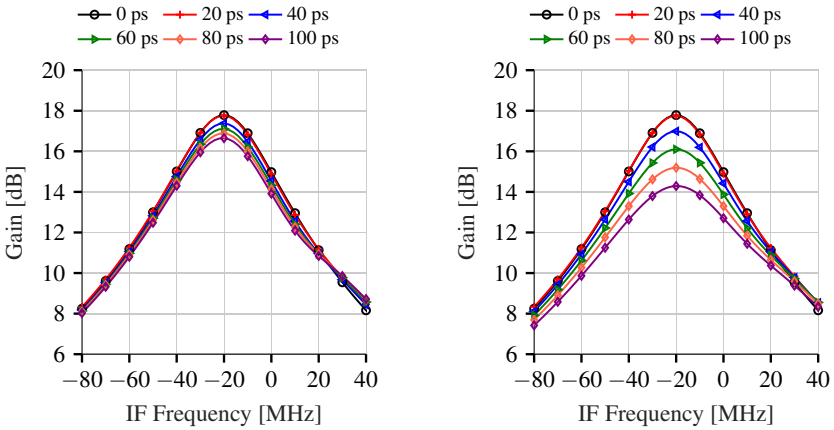


Figure A.2: The gain drop when (a) the clock phase ϕ_1 of the mixer is shifted forward, and (b) the clock phase ϕ_1 of both the mixer and CS-BPF 4/4 are shifted forward.

The mismatch between the clock phases could be caused by unaccounted parasitic capacitances in the clock routing, process and mismatch variation within the clock generation circuitry, or even both. Even though the source of the problem is not apparent, the solution is straightforward. To compensate for any mismatch between the

clock phases, a bank of capacitors should be added to the frequency divider outputs and used to calibrate the clock for the correct phase shift.

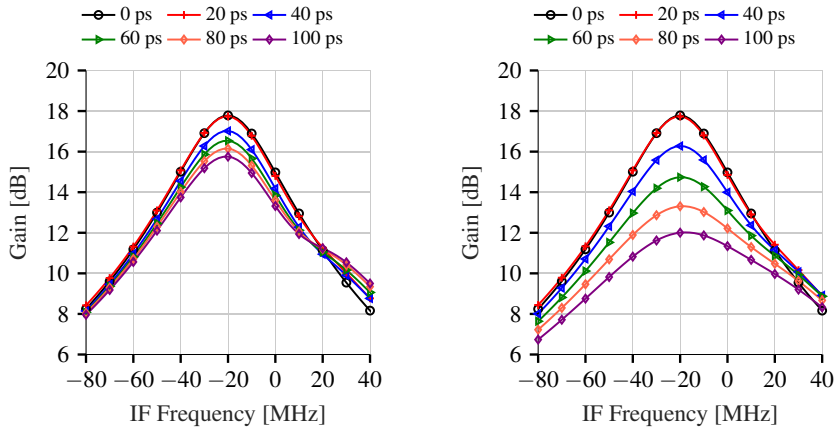


Figure A.3: The gain drop when (a) the clock phases ϕ_1 and ϕ_3 of the mixer are shifted forward, and (b) the clock phase ϕ_1 and ϕ_3 of both the mixer and CS-BPF 4/4 are shifted forward.

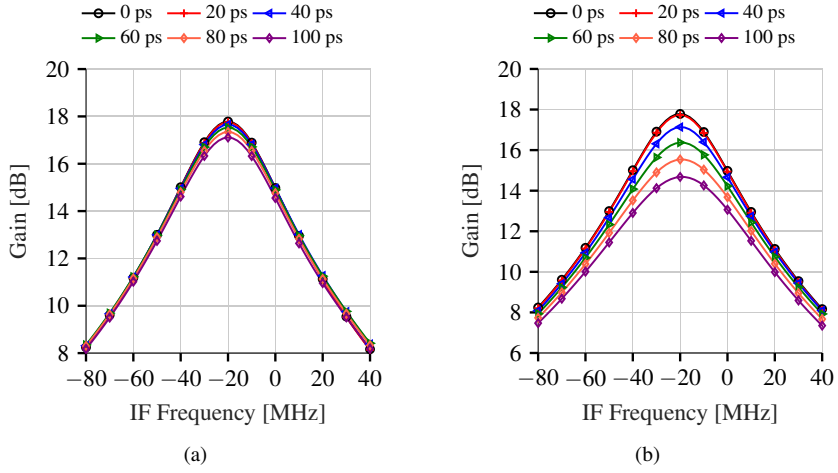


Figure A.4: The gain drop when (a) the clock phases ϕ_1 and ϕ_2 of the mixer are shifted forward, and (b) the clock phase ϕ_1 and ϕ_2 of both the mixer and CS-BPF 4/4 are shifted forward.

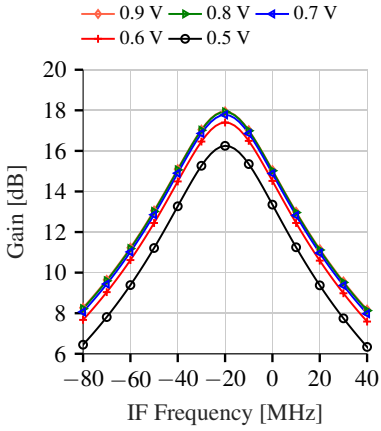


Figure A.5: The gain drop when the clock amplitude is reduced.

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