EDA tools to Improve Neuromorphic NoCs Design

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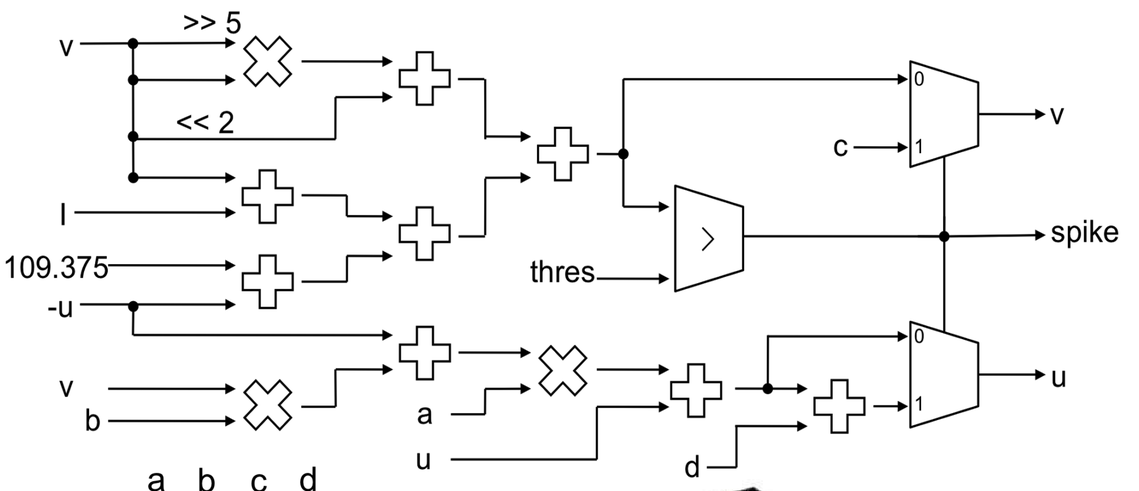
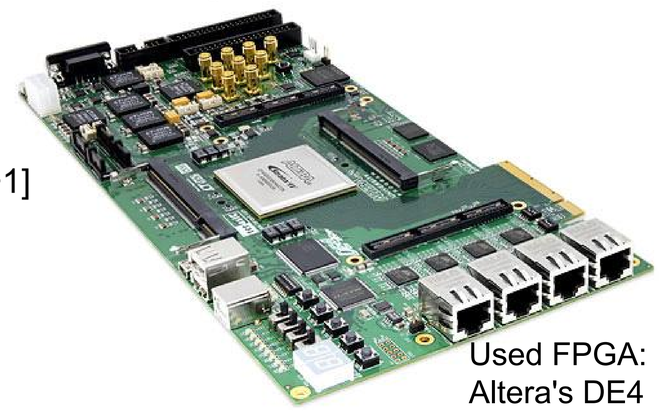
Bioinspired and Biomimetic Circuits are new and promising research topics. To be implemented in hardware they need to provide adaptive and reconfigurable connections and, at the same time, be highly scalable. Network-on-Chip (NoCs) seem to fill all these requirements, but the EDA tools to design and implement such NoCs need improvements.

Implemented Neuron [1]



Neuron Entity



Used FPGA: Altera's DE4

High time precision
8 ns Latency

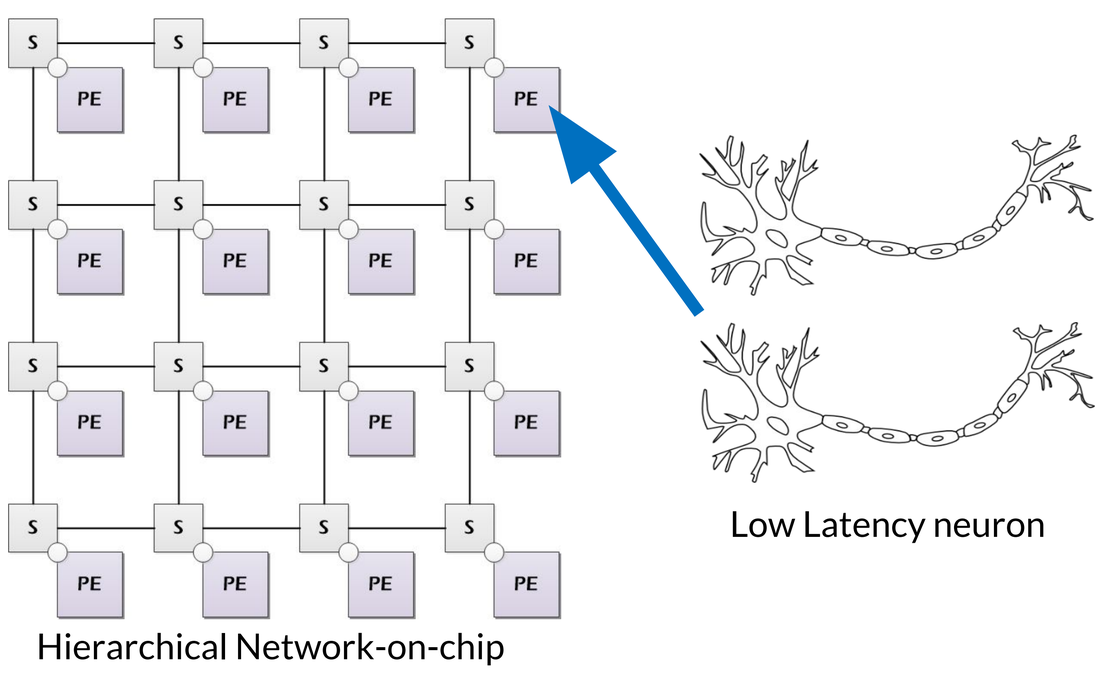
100 MHz clock
147 ALUTS per neuron

Current Large Scale Neural Networks

Project	Neurons	Synapses	Topology	Bio Real-time/ Spike rate
EMBRACE[2]	400 per tile	-	Hybrid (star-mesh)	yes/ 174kHz
SpiNNaker[3]	20 million	20 billion	Triangular lattice (folded into a toroid)	yes
TrueNorth[4]	1 million	256 million per chip	Mesh	yes
Neurogrid[5]	983,040	8 billion	Star	yes
BrainScaleS[6]	196,608 per wafer	114,688 per wafer	Hierarchical Buses (2D Torus wafer)	yes/ (10^5) xbio

[1] Bandeira, V. V., Costa, V. L., Bontorin, G., Reis, R. A. L., "Low Latency Izhikevich Neuron Model on FPGA", IESS 2016.
[2] J. Harkin, F. Morgan, L. McDaid, S. Hall, B. McGinley, and S. Cawley, "A reconfigurable and biologically inspired paradigm for computation using network-on-chip and spiking neural networks," Int. J. Reconfig. Comput., Jan. 2009.
[3] "The spinnaker project website," http://apt.cs.manchester.ac.uk/projects/SpiNNaker/, accessed November, 2015.
[4] F. Akopyan, J. Sawada, A. Cassidy, R. Alvarez-Icaza, J. Arthur, P. Merolla, N. Imam, Y. Nakamura, P. Datta, G.-J. Nam, B. Taba, M. Beakes, B. Brezzo, J. Kuang, R. Manohar, W. Risk, B. Jackson, and D. Modha, "Truenorth: Design and tool flow of a 65 mw 1 million neuron programmable neurosynaptic chip," Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on, vol. 34, no. 10, pp. 1537–1557, Oct 2015.
[5] "Brains in silicon website," https://web.stanford.edu/group/brainsinsilicon, accessed November, 2015.
[6] "The brainscales project website," http://brainscales.kip.uniheidelberg.de/, accessed November, 2015.

Our NoC Prototype



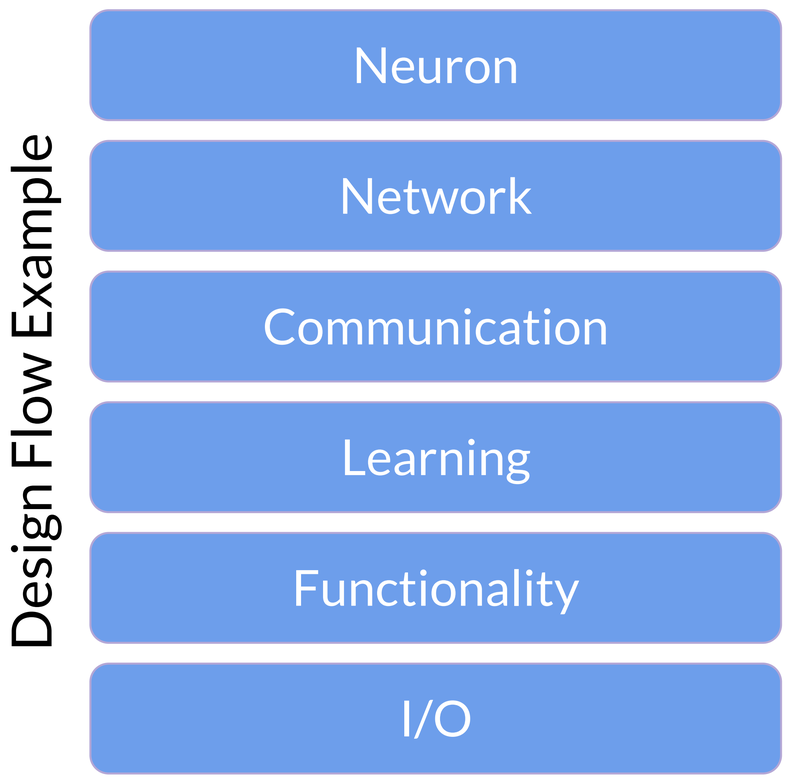
Hierarchical Network-on-chip

Low Latency neuron

We chose a hierarchical NoC, as they scale easily, and can also provide the integration of different neural networks.

Future with EDA

As a future work, we will develop an EDA tool for the design and implementation of Neuromorphic circuits and NoCs.



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