UNIVERSIDADE FEDERAL DO RIO GRANDE DO SUL
PROGRAMA DE PÓS-GRADUAÇÃO EM MICROELETRÔNICA - PGMICRO

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Analysis, Design and Implementation of Analog/RF Blocks Suitable for a Multi-Band Analog Interface for CMOS SOCs

Thesis presented in partial fulfillment of the requirements for the degree of Doctor in Microelectronics

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Porto Alegre, January 2008.

CIP – CATALOGAÇÃO NA PUBLICAÇÃO

Paixão Cortes, Fernando da Rocha

Analysis, Design and Implementation of Analog/RF Blocks Suitable for a Multi-Band Analog Interface for CMOS SOCs / Fernando da Rocha Paixão Cortes – Porto Alegre: Programa de Pós-Graduação em Microeletrônica, 2008.

148 f.:il.

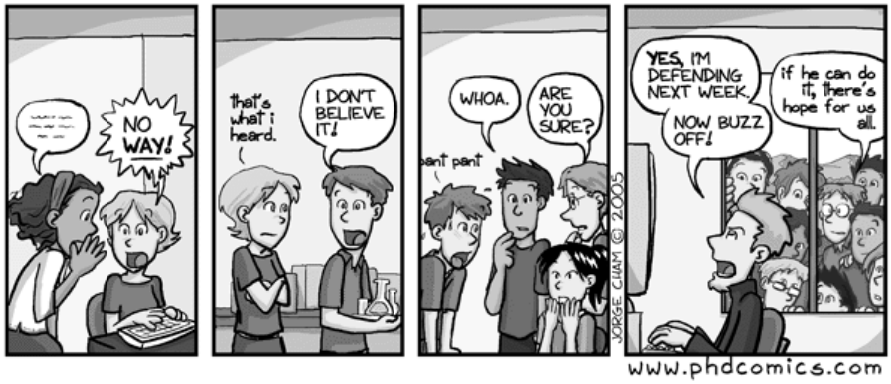
Tese (doutorado) – Universidade Federal do Rio Grande do Sul. Programa de Pós-Graduação em Microeletrônica. Porto Alegre, BR – RS, 2008. Orientador: Sergio Bampi.

1. Projeto analógico/RF CMOS. 2. Sistema RF 3. Células analógicas 4. Implementação física. I. Bampi, Sergio II. Título.

TO MY FAMILY

Mom, Dad and Sis

Scully the Dog and Bruna the Bird



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LIST OF ABBREVIATIONS AND ACRONYMS

ADC	Analog to Digital Converter
BJT	Bipolar Junction Transistor
CMOS	Complementary Metal Oxide Semiconductor
CT	Continuous Time
DAC	Digital to Analog Converter
DC	Direct Current
FAC	Fixed Analog Cell
FPGA	Field Programmable Gate Array
HF	High Frequency
IC	Integrated Circuit
IF	Intermediate Frequency
IIP3	Input Third-Order Intercept Point
IM	Intermodulation
LNA	Low Noise Amplifier
LO	Local Oscillator
NF	Noise Figure
OIP3	Output Third-Order Intercept Point
OTA	Operational Transconductance Amplifier
OPAMP	Operational Amplifier
Q	Quality Factor
RF	Radio Frequency
SOC	System-On-a-Chip
VGA	Variable Gain Amplifier
ΣΔ	Sigma-Delta

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ABSTRACT

The development of IC technologies coupled with the demand for more digital signal processing integrated in a single chip has created an increasing need for design of mixed-signal systems in CMOS technology. Previously, a general analog interface architecture targeted to mixed-signal systems on-chip applications was developed and implemented, which is composed by a fixed analog cell (FAC), that translates the input signal to a processing frequency, and a digital block, that processes the signal. The focus of this thesis is to analyze, design and implement analog/RF building blocks suitable for this system. First, a set of system specifications is developed and verified through system level simulations for the FAC system, aiming the signal processing of three target applications: FM, video and digital cellular frequency bands. Then, a fully CMOS integrated dual-conversion heterodyne front-end architecture with 2 active mixers and a variable-gain amplifier is presented, enumerating and proposing solutions for the design challenges and methodology. The stand-alone building blocks and the front-end system are designed and implemented in IBM 0.18μm CMOS process, presenting simulations and experimental data from an actual physical prototype.

Keywords: Mixed-Signal, CMOS Analog/RF Design**,** Frequency Translation**,** Mixer, Gilbert Cell, High Frequency, Variable Gain Amplifier.

Análise, Projeto e Implementação de Blocos Analógicos/RF Aplicados a uma Interface Analógica Multi-banda para Sistemas-em-Chip (SOCs) em CMOS

RESUMO

O desenvolvimento de tecnologias de integração para circuitos integrados junto com a demanda de cada vez mais processamento digital de sinais, como em sistemas de telecomunicações e aplicações SOC, resultaram na crescente necessidade de circuitos mistos em tecnologia CMOS integrados em um único chip. Em um trabalho anterior, a arquitetura de uma interface analógica para ser usada em aplicações SOC mistas foi desenvolvida e implementada. Basicamente esta interface é composta por uma célula analógica fixa (*fixed analog cell* – FAC), que translada o sinal de entrada para uma freqüência de processamento fixa, e por um bloco digital que processa este sinal. Primeiramente, as especificações de sistema foram determinadas considerando o processamento de sinais de três bandas de freqüência diferentes: FM, vídeo e celular, seguido por simulações de alto-nível do sistema da FAC. Então, uma arquitetura heteródina integrada CMOS para o *front-end* que integrará a FAC, composto por 2 *mixers* ativos e um amplificador de ganho variável, foi apresentada, enumerando-se e propondo-se soluções para os desafios de projeto e metodologia. Os blocos analógicos/RF, juntamente com o *front-end*, foram projetados e implementados em tecnologia *CMOS IBM 0.18μm*, apresentando-se simulações e medidas de um protótipo físico.

Palavras Chave: Sinais mistos, Projeto CMOS Analógico/RF, Translação em Freqüência**,** *Mixer*, Célula de Gilbert, Alta Freqüência, Amplificador de Ganho Variável.

1 INTRODUCTION

The development of ultra-scaled integrated circuits (IC) technologies coupled with the demand for more digital signal processing integrated in a single chip, like wireless communication systems and system-on-a-chip (SOC) applications, has resulted in an increasing need for design of mixed-signal systems in CMOS technology. Most of these systems require analog blocks, such as amplifiers, filters, mixers, oscillators, digital-to-analog converters (DAC), analog-to-digital converters (ADC), and other radio frequency (RF) blocks. In this context, the ever increasing effort to reduce IC costs and improve performance advises the use of mixed-signal design techniques compatible with implementation of analog blocks in a deep sub-micron CMOS technology.

In a previous work, a general analog signal interface architecture targeted to mixed-signal SOC applications was developed and implemented. This interface utilizes the concept of frequency translation (mixing) of the input signal followed by its conversion to the digital domain using sigma-delta ($\Sigma\Delta$) modulation. Basically this interface is composed by a fairly fixed analog cell (FAC), which translates the input signal to a processing frequency, and a digital block that processes the signal. The FAC is fixed at structural and functional level, providing appropriate bandwidth, noise, and frequency coverage for a target application set. A high level performance model prediction and a discrete prototype of this system have been developed and tested in (FABRIS, 2005). The modeled and experimental results have shown a good matching, demonstrating the interface use potentialities in a variety of applications classes for analog signal processing.

Thus, there is an open research opportunity for the integration of the FAC system in a single chip, achieving all the benefits from integration. The natural place to look for an architecture integrated solution for this system should be among RF receivers basic building blocks, where the mixers are the core of these systems.

The focus of this thesis is to analyze, design and implement analog/RF building blocks suitable for the FAC system. First, a set of system specifications is developed and verified through system level simulations for the FAC system, aiming the signal processing of the three target applications: audio (FM), video (VHF/UHF) and digital cellular (GSM/CDMA) frequency bands. Then, a fully CMOS integrated dual-conversion heterodyne front-end architecture, with 2 active mixers and a variable-gain amplifier, is presented, enumerating and proposing solutions for the design challenges and methodology.

This thesis is organized as follows. Chapter 2 discusses the general analog signal interface to be employed in mixed-signal SOC applications (FABRIS, 2005), reviewing the basic concepts and presenting the mixed-signal interface. Chapter 3 discusses the FAC integration issues, analyzing the system specifications and presenting a dual-conversion heterodyne architecture as best solution. In Chapter 4, we briefly discuss an early low-frequency implementation of the baseband blocks of the FAC system, presenting some experimental data. The RF section of the FAC, the IF front-end stage, is addressed in detail in Chapter 5, where it architecture and system design issues are discussed. Chapter 6 reviews and discusses the most significant characteristics and topologies of the front-end building blocks, detailing the blocks architectures. Chapter 7 addresses the complete design from the building blocks to the whole front-end, where electrical simulations results are included. In Chapter 8, experimental results from a test chip prototype with the discussed analog/RF building blocks are presented. Finally, in Chapter 9, we present our conclusions.

2 THE ANALOG MIXED-SIGNAL INTERFACE

System-on-chip (SOC) applications are growing rapidly nowadays, creating the necessity of design tools that increase the degree of design automation and allow faster prototyping and production. Such applications deal with low and high frequency signals and linear/non-linear signal processing functions. Many SOC applications require a mixed-signal (analog and digital circuits) design approach, demanding a wide range of specific analog or mixed-signal blocks, such as amplifiers, analog-to-digital converters, filters and mixers. Thus, the incorporation of some degree of analog programmability in this type of system is indispensable.

However, analog design automation still did not reach a reasonable degree of performance and integration. Looking at the specification of analog blocks, one finds constraints like noise, stability, frequency response, linearity, power consumption and others. These parameters are directly dependent on the target technology (transistor sizing, layout), which makes the reuse and automation task more difficult.

In the research work developed by (FABRIS, 2005), a general analog mixed-signal interface to be employed in mixed-signal SOC applications was proposed and modeled. This approach utilizes the concept of frequency translation (mixing) of the input signal followed by its conversion to the ΣΔ domain.

This chapter will present and briefly analyze the basic concepts and architecture of this proposed interface. First, an overview of the main concepts and terminology used in RF systems is presented. Then, the mentioned analog mixed-signal interface concept is discussed, presenting the interface system architecture suitable for SOC applications. Finally, the proposed system architecture is described in more detail, showing the modeling and discrete implementation developed in (FABRIS, 2005), with results from a discrete prototype.

2.1 Basic concepts in RF systems

Considering the wide scope of this work, involving analysis and design of low-frequency and RF circuits and systems, it is necessary to define and enumerate its main concepts that originate from the theory of signal and systems.

This section gives a briefly overview of the main basic concepts and terminology used in this area based in (LEE, 1998) (RAZAVI, 1998) (SANCHEZ, 2004), emphasizing the effects of linearity and noise.

2.1.1 The frequency translation concept

The concept of frequency translation is a well know mechanism used in communications systems. By multiplying two signals in the time domain, the resultant output spectrum is at the sum and difference frequencies of the input (LEE, 1998) (RAZAVI, 1998).

To illustrate this frequency translation, let us consider the signals described in equations 2.1 and 2.2.

$$x(t) = A_{RF} \cdot \sin(\omega_{RF} \cdot t) \tag{2.1}$$

$$y(t) = A_{LO} \cdot \sin(\omega_{LO} \cdot t) \tag{2.2}$$

The multiplication of these two signals will be

$$z(t) = \frac{A_{RF} \cdot A_{LO}}{2} \cdot (\cos(\omega_{RF} - \omega_{LO}) - \cos(\omega_{RF} + \omega_{LO})) \tag{2.3}$$

and from Fourier theory we have

$$Z(\omega) = \frac{A_{RF} \cdot A_{LO}}{2} \cdot \pi \cdot (\delta(\omega - (\omega_{RF} - \omega_{LO})) + \delta(\omega + (\omega_{RF} - \omega_{LO})) - \delta(\omega - (\omega_{RF} + \omega_{LO})) - \delta(\omega + (\omega_{RF} - \omega_{LO}))) \tag{2.4}$$

Figure 2.1 illustrates this process in frequency domain. The input signal f_{RF} is relocated to different positions in the resultant spectrum. These two new positions are at the intermediate frequencies at $f_{RF} + f_{LO}$ and $f_{RF} - f_{LO}$. Setting the low frequency component $f_{RF} - f_{LO}$ as the intermediate frequency (IF) to be acquired and processed, the local oscillator (LO) frequency can be determined to bring the input signal to the fixed processing band ($f_{LO} = f_{RF} + f_{IF}$). In order to separate the desired output to be processed, a pass band filter with its central frequency set to this intermediate frequency (IF) is usually used.

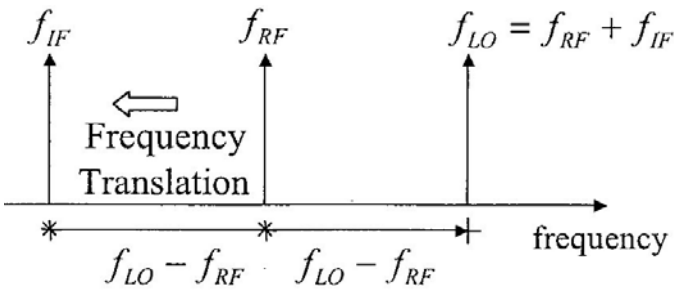


Figure 2.1: Frequency translation process.

In communication systems, the transmitted/received signals are usually a high frequency carrier modulated by the original signal through the frequency translation process previously described. In this context, it is common practice to define two types of signals: the *baseband* signal, defined one whose spectrum is nonzero in the vicinity of $\omega = 0$ and negligible elsewhere, and the *passband* (or RF) signal, defined as one

whose spectrum in nonzero in a band around a carrier frequency ω_c and negligible outside this band.

2.1.2 Linearity

A system is considered linear if its output can be expressed as a linear combination (or superposition) of responses to individual inputs (RAZAVI, 1998). However, practically any real system has a limit where the output has a sublinear dependence on the input. Such systems are considered nonlinear systems. We now enumerate the main nonlinearities effects considered in analog and RF circuits.

2.1.2.1 Distortion

If a signal is applied to a nonlinear system, the output generally exhibits frequency components that are multiples of the input frequency. To understand this, let's assume a nonlinear system described by the following equation

$$y(t) = b0 + b1 \cdot x(t) + b2 \cdot x^2(t) + b3 \cdot x^3(t) \tag{2.5}$$

Assuming $x(t) = A \cdot \cos(\omega \cdot t)$, from equation 2.5 and trigonometric identities we have

$$\begin{aligned} y(t) &= \left(b0 + \frac{b2 \cdot A^2}{2} \right) + \left(b1 \cdot A + \frac{3 \cdot b3 \cdot A^3}{4} \right) \cdot \cos(\omega \cdot t) \\ &+ \left(\frac{b2 \cdot A^2}{2} \right) \cdot \cos(2\omega \cdot t) + \left(\frac{b3 \cdot A^3}{4} \right) \cdot \cos(3\omega \cdot t) \end{aligned} \tag{2.6}$$

The term with the input frequency is called the fundamental and the higher-order terms the harmonics.

Harmonic distortion factors (HD_i) provide a measure for the distortion introduced by each harmonic for a given input signal level (using a single tone at a given frequency). HD_i is defined as the ratio of the output signal levels of the i^{th} harmonic to the fundamental.

From equation 2.6, assuming $b1 \cdot A >> \frac{3 \cdot b3 \cdot A^3}{4}$, the second harmonic distortion (HD_2), the third harmonic distortion (HD_3) and the total harmonic distortion (THD) are defined as

$$HD_2 = \frac{b2 \cdot A}{2 \cdot b1} \tag{2.7}$$

$$HD_3 = \frac{b3 \cdot A^2}{4 \cdot b1} \tag{2.8}$$

$$THD = \sqrt{HD_2{}^2 + HD_3{}^2 + HD_2{}^2 + \cdots} \tag{2.9}$$

For fully differential systems, ideally even harmonics will vanish and only odd harmonics remain. However, in real systems, mismatches corrupt the symmetry yielding finite even-order harmonics.

2.1.2.2 1dB compression point

The small-signal gain of a circuit is usually obtained with that assumption that the harmonics are negligible. However, as the signal amplitude increases, the gain begins to vary. This effect is called the 1dB compression point.

The 1dB compression point is defined as the point where the fundamental gain deviates from the ideal small signal gain by 1 dB, as shown in Figure 2.2.

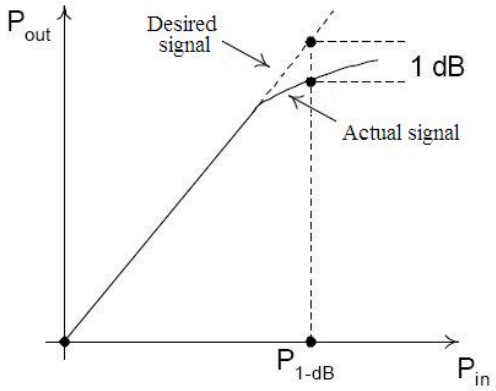


Figure 2.2: Definition of the 1dB compression point.

From the previous definition and from equation 2.6, we have

$$20\log\left(b1\cdot A_{1-dB}+\frac{3\cdot b3\cdot A_{-1dB}{}^{3}}{4}\right)=20\log\left(b1\cdot A_{1-dB}\right)-1 \tag{2.10}$$

$$A_{1-dB}=\sqrt{0.145\cdot\frac{b1}{b3}} \tag{2.11}$$

2.1.2.3 Intermodulation

When two signals with different frequencies are applied to a nonlinear system, the output exhibits some components that are not harmonics of the input frequencies. This phenomenon is called intermodulation (IM) and it arises from undesired mixing process due to nonlinearities present in the circuit.

To understand this, let's assume the same nonlinear system described by equation 2.5, and assume $x(t)=A\cdot\cos(\omega_1\cdot t)+A\cdot\cos(\omega_2\cdot t)$. Thus, from trigonometric identities we have

$$y(t) = \left(b0 + b2 \cdot A^2\right) + \left(b1 \cdot A + \frac{9 \cdot b3 \cdot A^3}{4}\right) \cdot \cos(\omega_1 \cdot t) + \left(b1 \cdot A + \frac{9 \cdot b3 \cdot A^3}{4}\right) \cdot \cos(\omega_2 \cdot t) +$$
$$\left(\frac{b2 \cdot A^2}{2}\right) \cdot \cos(2\omega_1 \cdot t) + \left(\frac{b2 \cdot A^2}{2}\right) \cdot \cos(2\omega_2 \cdot t) + \left(b2 \cdot A^2\right) \cdot \cos((\omega_1 + \omega_2) \cdot t) +$$
$$\left(b2 \cdot A^2\right) \cdot \cos((\omega_1 - \omega_2) \cdot t) + \left(\frac{3 \cdot b3 \cdot A^3}{4}\right) \cdot \cos((2\omega_1 - \omega_2) \cdot t) + \left(\frac{3 \cdot b3 \cdot A^3}{4}\right) \cdot \cos((2\omega_2 - \omega_1) \cdot t) + \quad (2.12)$$
$$\left(\frac{3 \cdot b3 \cdot A^3}{4}\right) \cdot \cos((2\omega_1 + \omega_2) \cdot t) + \left(\frac{3 \cdot b3 \cdot A^3}{4}\right) \cdot \cos((2\omega_2 + \omega_1) \cdot t) +$$
$$\left(\frac{b3 \cdot A^3}{4}\right) \cdot \cos(3\omega_1 \cdot t) + \left(\frac{b3 \cdot A^3}{4}\right) \cdot \cos(3\omega_2 \cdot t)$$

The corruption of signals due to the third-order intermodulation of two nearby interferes is very common and critical mostly in RF systems, so that a performance metric has been defined to characterize this behavior. The third-order intercept point (*IIP3*) is defined as the point that the input signal power generates a third-order intermodulation product with the same power of the fundamental component, as shown in Figure 2.3. If a weak signal accompanied by strong interferers experiences a third-order nonlinearity, then one of the IM products falls in the band or interest, corrupting the desired signal.

From the previous definition and from equation 2.12, assuming $b1 \cdot A >> \frac{9 \cdot b3 \cdot A^3}{4}$, we have

$$(b1 \cdot A_{IIP3}) = \left(\frac{3 \cdot b3 \cdot {A_{IIP3}}^3}{4}\right) \Rightarrow {A_{IIP3}}^2 = \frac{4}{3}\frac{|b1|}{|b3|} \quad (2.13)$$

Where the input amplitude $IP3$ is $A_{IIP3} = \left[\frac{4}{3}\frac{|b1|}{|b3|}\right]^{1/2}$ and the output amplitude $IP3$ is $b1 \cdot A_{IIP3}$.

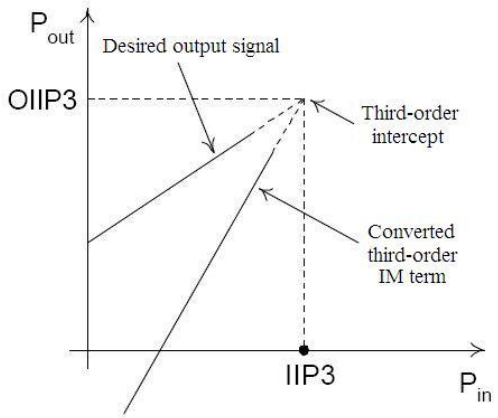


Figure 2.3: Definition of the third-order intercept point.

In a two-tone test, the input third-order intercept point can be considered as half the difference between the magnitudes of the fundamentals and the IM3 products at the output plus the corresponding input level (Figure 2.4a). The geometric interpretation of this relationship is shown in Figure 2.4b. This approach provides an estimation of $IIP3$, where the actual value must be obtained from the extrapolated intersection of the two curves shown in Figure 2.3.

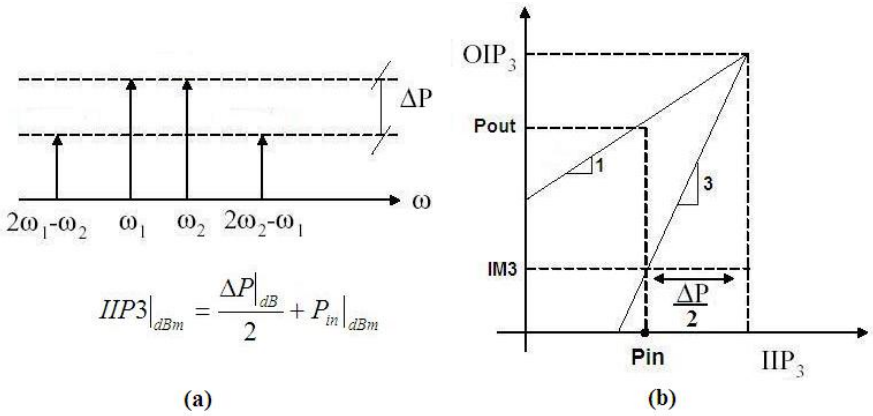


Figure 2.4: (a) Calculation of IIP3 without extrapolation, (b) graphical interpretation.

In general, the higher the third-order intercept point, the more linear the system. Additionally, it is common to abbreviate the third-order intercept point as $IP3$, or $IIP3$ and $OIP3$, the input and output third-order intercept point, respectively.

2.1.2.4 Cascade nonlinear stages

Since in RF systems, signals are processed by cascade stages, it is important to know how the nonlinearity of each stage contributes to the overall system. In particular, it is desirable to calculate an overall input third intercept point in terms of the $IP3$ and gain of the individual stages.

Let's consider *n* nonlinear stages in cascade as shown in Figure 2.5. The overall third intercept point A_{IIP3} will be given by

$$\frac{1}{A_{IIP3}{}^2} = \frac{1}{A_{IIP3,1}{}^2} + \frac{G1^2}{A_{IIP3,2}{}^2} + \frac{G1^2 \cdot G2^2}{A_{IIP3,3}{}^2} + \cdots \tag{2.14}$$

where $A_{IIP3,n}$ is the IIP3 of the nth stage, and Gn is the gain of the nth stage.

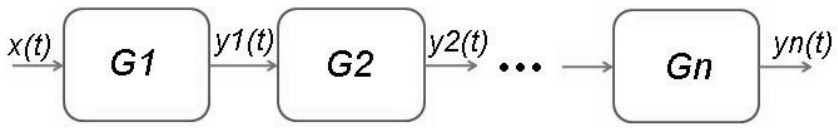


Figure 2.5: Cascade nonlinear stages.

2.1.3 Noise

Noise can be defined as any random interference unrelated to the signal of interest. The main noise sources in circuits are the thermal noise (generated by resistors and transistors), flicker noise ($1/f$ noise) and shot noise (LEE, 1998). We now define the performance metric used to characterize the noise behavior in analog and RF real systems.

2.1.3.1 Input-referred noise

Let's consider the noise two-port driven circuit showed in Figure 2.6, where $N_{out} = A^2 \cdot N_o + N_{ckt}$ is the output noise density, N_o is the noise from the input resistance, and N_{ckt} is the circuit generated noise density, and A the circuit gain.

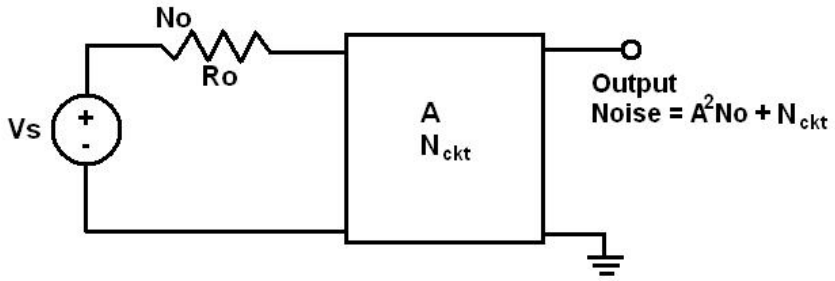


Figure 2.6: Noise performance in a real circuit.

The input-referred noise density is defined as

$$N_{inp,ref} = \frac{N_{out}}{A^2} = N_o + \frac{N_{ckt}}{A^2} \tag{2.15}$$

2.1.3.2 Noise figure

From the previous analysis, the noise factor (F), that measures the amount of noise produced by a RF device relative the ambient thermal noise at its input, can be defined as the ratio:

$$F = \frac{N_{out}}{N_{in}} = \frac{N_{out}}{A^2 \cdot N_o} = \frac{A^2 \cdot N_o + N_{ckt}}{A^2 \cdot N_o} = 1 + \frac{N_{ckt}}{A^2 \cdot N_o} \tag{2.16}$$

The noise figure (NF) is often defined as the noise factor in units of dB, where

$$NF = 10 \cdot \log F \tag{2.17}$$

The noise figure of a circuit can be also defined as the signal-to-noise ratio (SNR) at the input port divided by the SNR at the output port. Thus, we can rewrite F as

$$F = \left(\frac{S_i / N_o}{S_o / N_{out}} \right) = \frac{SNR_i}{SNR_o} \tag{2.18}$$

where S_i and S_o are the input and output signal power, respectively. In other words, the NF can be considered as the measure of how much the SNR degrades as the signal pass through a system.

2.1.3.3 Noise figure of cascade stages

For cascade stages, the overall noise figure can be obtained in terms of the NF and gain of each stage.

Let's consider *n* noisy stages in cascade as shown in Figure 2.7, where *Nin, N1, ... Nout* are the noise at the input, output stage 1, … and output, respectively.

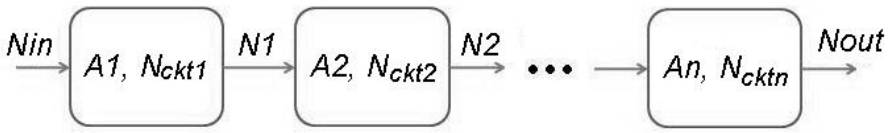


Figure 2.7: Cascade noisy stages.

Thus, from equation 2.14 the input referred noise due to *N1, N2,... Nn* becomes

$$N_{inp,ref} = \frac{N_{out}}{A1^2 \cdot A2^2 \cdots An^2} \tag{2.19}$$

Then, from equation 2.15 the overall noise factor can be expressed as

$$F_{total} = F1 + \frac{F2-1}{A1^2} + \frac{F3-1}{A1^2 \cdot A2^2} + \cdots + \frac{Fn-1}{A1^2 \cdot A2^2 \cdots An^2} \tag{2.20}$$

2.1.4 Sensitivity

The sensitivity of a system (RF receiver) is defined as the minimal signal level that the system can detect with acceptable output signal-to-noise ratio, i.e., the minimal input signal that a system (receiver) can detect.

From equation 2.17 and assuming that the overall signal power is distributed across the system bandwidth (*BW*), the sensitivity (S_{mim}) can be defined as the minimum

signal power applied to the receiver input terminals that yields the required output *SNR*. Thus, we have

$$S_{mim} = (N_{in})_{dBm} + (NF)_{dB} + (10\log BW)_{dB} + (SNR_o)_{dB} \quad (2.21)$$

where N_{in} is the input noise density produced on the source resistor feeding the system (for instance, the input resistor of an input signal generator used for testing or the equivalent resistance from the antenna in a receiver - $(N_{in})_{dBm} = -174dBm$).

The sum of the first three terms in equation 2.21 is the total integrated noise of the system and is usually called the *noise floor* of the system.

2.1.5 Dynamic range

Dynamic range (DR) is generally defined as the ratio between the maximum input level that a circuit can tolerate and the circuit's minimum input level that provides a reasonable signal quality. This definition is usually quantified differently, depending on the application (RAZAVI, 1998).

In analog circuits such as amplifiers and analog-to-digital converters the dynamic range is defined as the ratio of the full-scale input level (typical input level beyond which a hard saturation occurs) to the input level which the SNR is one.

In RF design, the dynamic range is quantified by the spurious-free dynamic range (SFDR). The SFDR is the difference, in dB, between the maximum input level for which the third-order IM products do not exceed the noise floor and the sensitivity of the system, as illustrated in Figure 2.8.

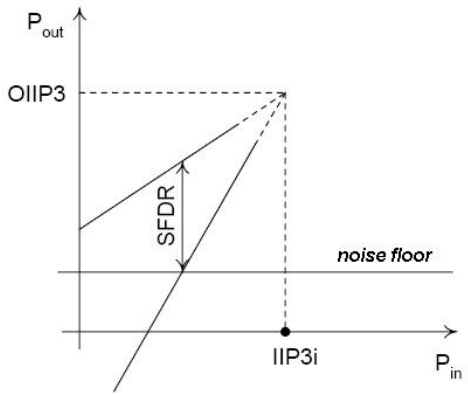


Figure 2.8: SFDR definition.

2.2 The interface system overview

Considering that for most applications the input signal is band limited, relocating the input signal to a fixed frequency band and processing this translated spectrum using a high performance mixed-signal section can be a good alternative to process an analog signal. Hence, the frequency translation concept can be used to acquire a signal at an intermediate frequency (IF), and then the signal can be processed entirely in the digital domain. Thus, this mixed-signal interface should deliver the following characteristics:

- performance almost constant from DC to high frequencies (HF) for band limited signals;
- capability of realization of a wide variety of linear and non-linear applications;
- compatibility with digital control and programmability;
- CMOS technology compatible.

Figure 2.9 shows the block diagram of the approach developed in (FABRIS, 2005). The input signal is translated to the processing frequency (f_P) through a mixer block. The mixed signal then passes through a pass band filter in order to select the desired component. The select spectrum is sampled and digitized by and analog-to-digital converter (ADC). This sample data is then processed by a configurable digital system and converter back to analog domain using a digital-to-analog converter (DAC). The digital configurable block demodulates the signal and processes it in the base band. Finally, the processed output signal is sent out by an output block composed by a DAC and a reconstruction filter.

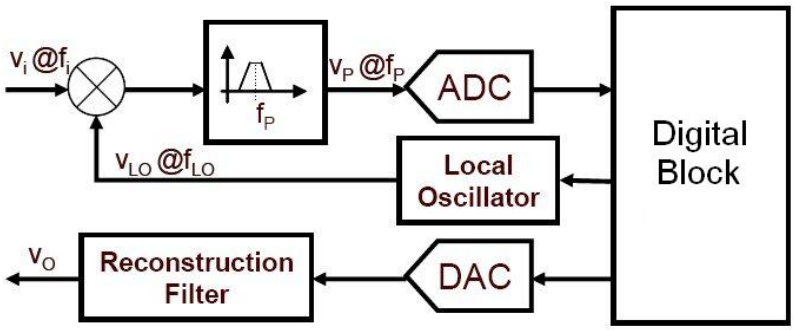


Figure 2.9: Block diagram of the mixed-signal interface structure (FABRIS, 2005).

Whenever the input signal is translated to f_P, this approach permits the use of an ADC with lower sampling rate than would be required to direct digitize a HF input signal. Another advantage of the use of the mixer in the front of the front-end is to enable the manipulation of band limited signals located in a wide frequency range, covering from DC to high frequencies.

2.3 The interface architecture

Considering this approach, an architecture suitable for this interface was developed and analyzed. Figure 2.10 shows the basic structure of the mixed-signal interface architecture: a *fixed analog cell* (FAC), composed by an input mixer, variable gain amplifier (VGA), and a continuous time (CT) *Nth* order band-pass ΣΔ modulator, and a digital reconfigurable block. The signals for controlling the mixer and the DAC are generated by the digital reconfigurable block. The desired output signal is sent back to the analog form by a 1bit DAC and a reconstruction filter.

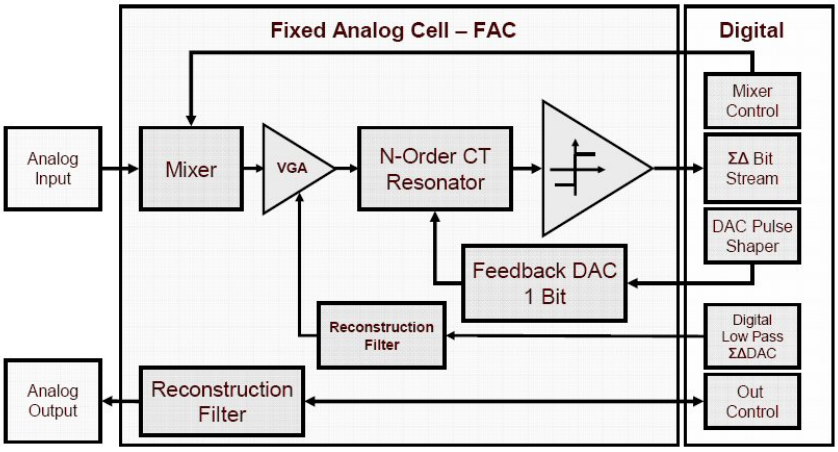


Figure 2.10: General mixed-signal interface architecture (FABRIS, 2005).

The primary purpose of this interface is simply to convert an input signal into a digital form and process it in the digital domain, where the input frequency and the signal bandwidth are allowed to vary from application to application. The interface can be used in applications like a multi-band analog-to-digital converter, channel adders, analog multipliers and RF receivers (considering that it comes from a previous stage with an antenna and LNA).

As the FAC is fixed at the structural and functional levels, it design can be optimized to provide appropriated bandwidth, noise and frequency coverage for a target set of applications. By using the intermediate frequency f_P to acquire the signal, problems like 1/f or flicker noise and DC offsets are attenuated.

The single channel solution presented in Figure 2.10 can be extended for the multi-channel case by replicating the FAC according to the number of desired analog signal inputs. Figure 2.11 shows the architecture of a multi-channel solution, using a set of identical FACs as building blocks.

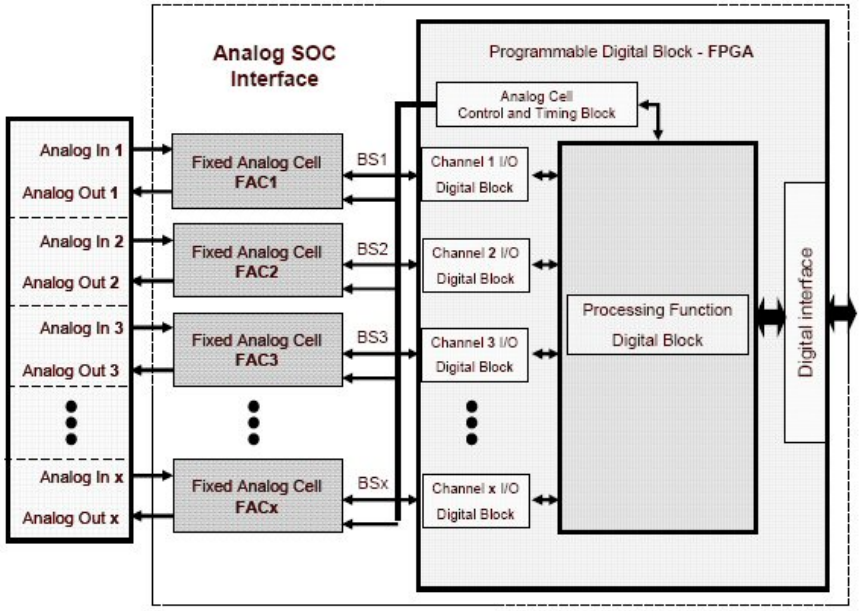


Figure 2.11: Multi-channel mixed-signal interface architecture (FABRIS, 2005).

2.4 Results from a discrete board implementation

A high level performance prediction and a discrete prototype for the FAC were developed in (FABRIS, 2005). The discrete prototype comprises a FAC and a digital structure based on a Field Programmable Gate Array (FPGA). The mixer block was implemented in a passive topology using a CMOS switches, and the continuous band-pass ΣΔ modulator in an active RC topology. Although discrete, the overall principle is certainly valid for VLSI implementations.

A series of test procedures were conducted to evaluate the performance of the system. The FPGA board used in the discrete prototype has an internal clock of 32.786 MHz limits the maximum mixer control frequency to half of its clock. The overall performance test was done applying a full scale single tone at the interface input and the corresponding bit-stream was acquired for each testing frequency. Table 2.1 summarizes the overall performance of the prototyped FAC.

Table 2.1: Summary of the overall performance of the discrete prototyped FAC.

Parameter	*Measurement*
Frequency coverage	DC to 17.4 MHz
Signal bandwidth	60 KHz
Processing frequency - f_P	1.042 MHz
Linearity - IMD3 / IIP3	60 dBFS / 15 dBFS
SDFR (Modulators's OSR = 32)	69 dBFS

The prototype was also analyzed to implement some reconfigure analog signal acquisition and processing functions, demonstrating the potential of the interface as a general reconfigurable platform. Applications like a multi-band analog-to-digital converter, an *N* channel adder and a two-channel analog multiplier were implemented and analyzed using the interface discrete prototype (FABRIS, 2003).

2.5 Discussion

This chapter discussed the development of general analog signal interface to be employed in mixed-signal SOC applications, proposed, modeled and implemented in (FABRIS, 2005). This approach utilizes the concept of frequency translation of the input signal followed by its conversion to the ΣΔ domain.

First, we addressed the main concepts and defined the terminology used in such systems originated from the theory of signal and systems. Then, we briefly described proposed system architecture, showing the design and construction of a prototype that validates the proposed architecture. The prototype was implemented in a discrete board,

achieving a frequency coverage from DC to 17MHz, limited by the discrete components and FPGA board.

Thus, there is an opportunity research for investigation towards the integration of the whole system in a single a chip, achieving all the benefits from integration. More specific, the investigation of the best architecture for the FAC integration, considering a wider frequency coverage (from FM to cellular frequency bands), and the CMOS implementation of the FAC's building blocks.

3 THE FIXED ANALOG CELL INTEGRATION

We now discuss the Fixed Analog Cell (FAC) as a part of the mentioned mixed-signal interface system, aiming its CMOS integration.

In (FABRIS, 2005), the application mapping capability of this interface was validated, implementing some reconfigurable analog signal acquisition and processing functions, such as an analog-to-digital converter and an analog multiplier. However, the performance results were limited to a small frequency range with high power consumption due to the low frequency discrete prototype used. Thus, the next step is to integrate the whole FAC in a chip, achieving the expected benefits from integration.

In this chapter, we discuss the FAC integration. First, we present an architecture for the FAC suitable for CMOS integration, based on receivers architectures used in communication systems. Following we analyze three frequency bands (FM, video and digital cellular frequency bands) as our target applications for the integrated FAC. Finally, we present our initial system specifications for the FAC in order to work with the target applications.

3.1 FAC architecture

Figure 3.1 shows the block diagram of the proposed architecture of the complete mixed-signal system, aiming its integration. The FAC is composed by a variable gain front-end stage, a continuous-time bandpass ΣΔ modulator, a frequency synthesizer, and a reconstruction filter. It is easy to note that the FAC architecture is based on heterodyne receivers used in wireless communication systems (RAZAVI, 1998).

The complete system is described as follows. The input signal enters the variable gain front-end stage, which translates this signal to the processing frequency, providing gain control to adjust it dynamic range. The selected signal is sampled by the continuous-time bandpass ΣΔ Modulator and then processed by the digital block. The frequency synthesizer block generates the LO signals that enters the front-end stage (and it can be controlled by the digital block). The desired output signal is sent back to the analog form by the reconstruction filter.

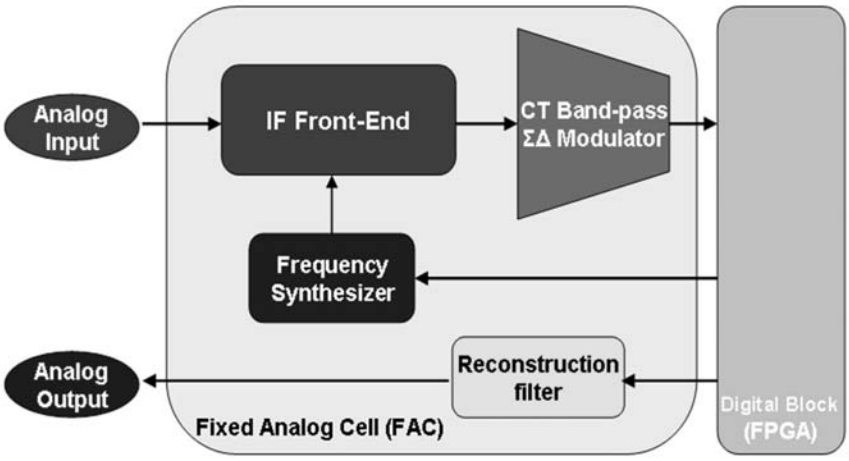


Figure 3.1: Block diagram of the architecture of the complete mixed-signal system, aiming the FAC integration.

Each building block architecture and specification is critical to the system performance, which is direct dependent of the type of signals that the system is going to deal with. Thus, the next step must be the definition of the target application, in order to specify the FAC performance requirements.

3.2 Application mapping

The primary purpose of the FAC is to convert an input analog signal into a digital form, where the input frequency and the signal bandwidth are allowed to vary from application to application. We intend to process input signals of three specific bands: FM, video (VHF/UHF) and digital cellular (CDMA/GSM) frequency bands. Table 3.1 summarizes the application mapping for different target frequency bands that we intend to work with.

Table 3.1: Application mapping for different target frequency bands

Application	*Frequency Band*
FM radio receivers	88 – 174 MHz (FM)
VHF/UHF TV tuners	48 – 860 MHz
Digital Cellular receivers	869 – 894 MHz (CDMA) 935 – 960 MHz (GSM)

We now discuss each frequency band, aiming in how these signals are processed. Several receiver architectures with ADC are reviewed, considering general system

specifications (input level, sensitivity, modulation format, carrier frequency, and signal bandwidth) and its applications.

3.2.1 AM/FM radio receivers

The aim for high integrated wireless communication devices has resulted in a digitalization trend in radio receiver technology, including car radio applications (VAN DER ZWAN, 2000) (VAN ENGELEN, 1999) (VOGT, 1996).

Figure 3.2 shows a typical architecture of an AM/FM broadcast radio receiver using digital audio signal processing. The receiver consists of a low-noise amplifier (LNA) followed by a mixer. The mixer converts the signal to the IF frequency (usually of 10.7 MHz). For FM signals (88 – 174 MHz), the mixer performs a down-conversion; in case of AM signals (540 – 1630 kHz), the mixer performs an up-conversion. A bandpass filter is used for channel selection for both AM and FM signals. The filter is followed by an automatic gain control (AGC) amplifier, which feeds the signal to the ADC (usually an ΣΔ ADC). Additional filtering, final channel selection, and demodulation of the signal are done by a digital signal processing (DSP) block. Finally, the demodulated signal passes to a DAC and made audible by a power amplifier (PA) followed by a loudspeaker.

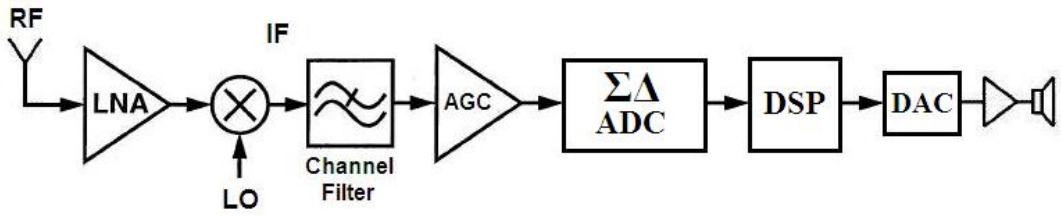


Figure 3.2: A typical digital IF radio receiver.

In these solutions, the analog-to-digital (A/D) conversion takes place at a fixed IF of 10.7 MHz, both for AM and FM signals. An FM channel filter, usually about 200 kHz wide, is required to protect the AGC and the ADC from strong interfering signals (its specifications can be relaxed, since final channel filtering takes place in the digital domain). For AM signals, only 9 kHz wide filters are used, where no selectivity is provided in front of the ADC (about twenty AM channels will pass through the 200 kHz FM channel filter). The AM channel selection can be done completely in the digital domain.

The key element in this system is the IF ADC, where continuous-time bandpass ΣΔ modulation is preferred used (VAN DER ZWAN, 2000) (VAN ENGELEN, 1999). The requirements for the ΣΔ modulator are determined by its input signal characteristics. For AM and FM broadcast radio receiver, a dynamic range of 65 and 90 dB, respectively, is desirable. The ΣΔ modulator should achieve this dynamic range at low input signals levels to alleviate the AGC requirements. In AM/FM receivers, usually a resolution of 10 bits in 11 MHz bandwidth may be sufficient to achieve the noise specifications.

Table 3.2 shows an overview of the requirements of a typical AM/FM receiver based in digital radio applications, aiming general system specifications (input level, sensitivity, carrier frequency, signal bandwidth) and building blocks specifications.

Table 3.2: Overview of requirements of a typical AM/FM digital IF radio receiver.

Frequency band	*Channel Bandwidth*	*Sensitivity*	*IF*	*Image rejection*	*ΣΔ A/D*			
					Resolution	*Sampling frequency*	*SNR*	*Dynamic range*
AM 540 – 1630 KHz	9 KHz	1μVrms	10.7MHz	80 dB	10 - 16 bits	30 – 80 MHz	80dB	65 dB
FM 88 – 174 MHz	200 KHz							90 dB

3.2.2 VHF/UHF TV tuners

Nowadays there are several analog/digital TV standards throughout the world. The standard terrestrial and cable TV band (North America) covers a wide frequency range from 48 to 860 MHz, with a 6 MHz channel bandwidth.

The broadband TV tuner design involves some challenging technical issues, such as harmonic mixing, image, dynamic range, and linearity. Traditionally, superhererodyne TV turners have been implemented, as shown in Figure 3.3a, where the TV signals are down-converted to a 36/44 MHz IF. Tunable RF resonant tanks are used to suppress the higher bands channels to be mixed down and filter out the image channel. In addition to that, external surface acoustic wave (SAW) filters are also needed to suppress the mixing and image components. However, this type of architecture is very difficult to integrate on a chip.

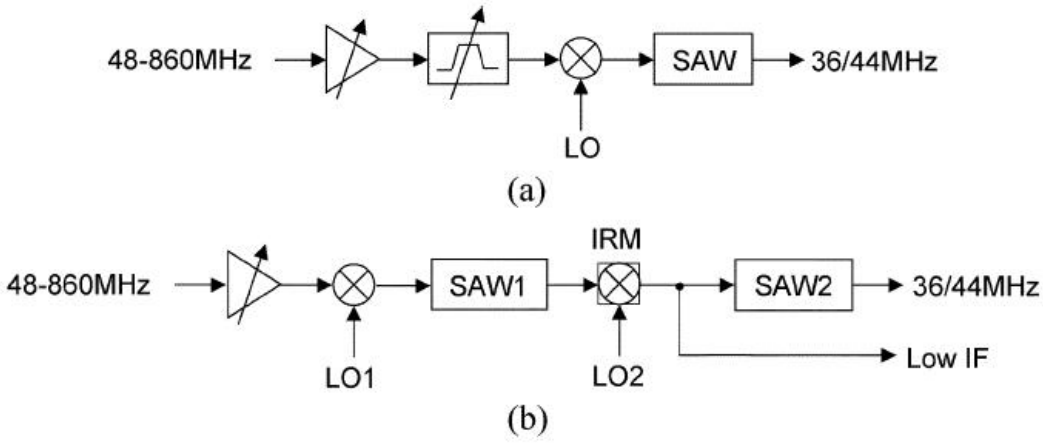


Figure 3.3: (a) Conventional TV tuner. (b) Integrated TV tuner using a dual-conversion system.

Solutions using an up/down dual-conversion system were proposed (CONNEL, 2002) (VAN SINDEREM, 2003), as shown in Figure 3.3b. The reason for the up-conversion (usually 1GHz) is to keep the harmonics of the local carrier out of the TV

band, avoiding the harmonic mixing. An external SAW filter is still needed to suppress both harmonic mixing and image components at the fixed first IF rather than at the RF. The signal is then down-converted to the lower IF of 36/44 MHz for standard TV demodulation. In order to achieve a desired image rejection of 60dB, an image rejection mixer must be used as the second mixer. The need of external SAW filter limits the level of integration and power consumption in these approaches.

In a recent fully integrated TV tuner implementation (HENG, 2005), a low-IF turner with digital image rejection was proposed. In this system, harmonic mixing is suppressed through the up/down dual-conversion architecture with an on-chip LC tuning tank. A low second IF of 1.75 MHz is chosen to receive the analog TV channels. The down-converted low-IF in phase and quadrature (I/Q) signals are digitized after being filtered by an analog complex antialiasing filter. The channel select filtering and image cancellation are performed by the digital part. This approach offers a simple generic solution for image rejection applicable to low or zero-IF RF systems. The system requires an 11-bit ADC, made of five pipelined stages of a standard 3-bit multiplying DAC (MDAC).

Table 3.3 shows an overview of the requirements of VHF/UHF TV tuners, based on video application, aiming general system specifications (input level, sensitivity, carrier frequency, signal bandwidth) and building blocks specifications.

Table 3.3: Overview of requirements of a typical VHF/UHF TV tuner.

Frequency Band	*Bandwidth*	*Sensitivity*	*IF*	*Image rejection*	*SNR*	*A/D resolution*
48 – 860 MHz	812 MHz (6 MHz of channel spacing, 130 channels)	170μVrms	36/48 MHz	60 dB	40dB	11 bits

3.2.3 Digital cellular receivers

Cellular standards such as Global System for Mobile Communications (GSM) and Code-division Multiple Access (CDMA) are widely used in wireless communication products (RAPPAPORT, 2002). The standards, being different in many aspects, such as modulation and channel bandwidth, place differing requirements on the system, which calls for highly flexible implementations. This flexibility comes naturally to digital signal processing (DSP) where different functionalities are often implemented in the digital world.

Figure 3.4 shows a typical superheterodyne architecture of a digital cellular receiver. The superheterodyne receiver architecture employs two stages of down-conversion (dual-IF), improving the trade-off between sensitivity and selectivity in the architecture. In these solutions, like in (BREMS, 2000) (SCHEIRER, 2001), the desired signal is converted to a first IF (10-300MHz), followed by filtering, and then converted again to

a second IF (1-4MHz), with a combination of a mixer and a continuous-time bandpass ΣΔ ADC (SCHEIRER, 2002), to be processed by a DSP block.

Others solutions, like in (GUO, 2002), uses a single high-IF architecture for digital such receivers. In these types of solutions, the signal is down-converted, filtered and amplified only once (with an IF in the range of 70-300MHz), which saves power and area and helps reduce the noise contributions, followed by the ΣΔ ADC stage.

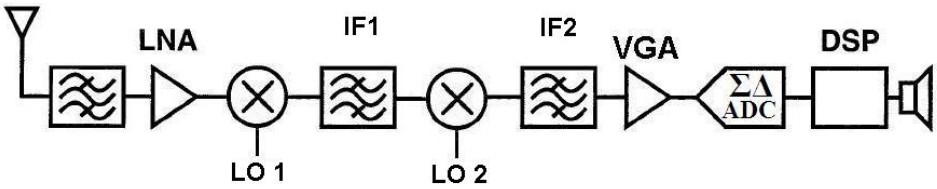


Figure 3.4: A typical superheterodyne architecture of a cellular receiver.

Considering the diversity of wireless communication standards, solutions of the integration of multimode receiver architectures for digital cellular systems were also developed. In such systems, the ADC must adapt to the required signal bandwidth in each mode. The ADC architecture is usually based on ΣΔ modulators, combining continuous-time and switched-capacitor stages (SALO, 2003) (VAN VELDHOVEN, 2003).

Table 3.4 shows an overview of the requirements of a typical digital cellular receiver for CDMA/GSM standards, based on digital cellular applications, aiming general system specifications (input level, sensitivity, carrier frequency, signal bandwidth) and building blocks specifications.

Table 3.4: Overview of requirements of a typical digital cellular receiver.

Frequency Band	*Bandwidth*	*Sensitivity*	*NF*	*Image rejection*	*IF*	*ΣΔ A/D*			
						Topology	*Resolution*	*SNR*	*Dynamic range*
869 – 894 MHz (CDMA)	25 MHz (1.25MHz of channel spacing, 20 channels)	- 102 dBm	10dB	80 dB	70-300 MHz (IF1) 4MHz - DC (IF2)	IF BPΣΔ modulator	7 - 10 bits	40 dB	100 dB
935 – 960 MHz (GSM)	25MHz (200KHz of channel spacing, 124 channels)					BPΣΔ with a integrated mixer			

3.3 FAC system specification

Based on the general system specifications of each target application reviewed in the previous sections, we now can set the initial specifications for the receiver path (front-end + ΣΔ modulator) of the FAC. Table 3.5 shows an overview of the initial requirements of the receiver path of the FAC.

Table 3.5: FAC's receiver path initial specifications.

Frequency band		48MHz – 960MHz
Signal bandwidth		200kHz (FM, GSM) 1.25MHz (CDMA) 6 MHz (VHF/UHF)
Sensitivity		< 1μVrms
NF		< 15 dB
Linearity (IIP3)		> -30 dBm
Front-end gain range		0 to 80 dB
ΣΔ A/D	Topology	Multi-mode bandpass (continuous-time/switched-capacitor)
	Dynamic range	90 dB (200mVpp input)

Considering the wide range of input signals and a variable signal bandwidth that enters the FAC, the use of a superheterodyne front-end and a multimode ΣΔ modulator is straightforward.

3.4 Discussion

This chapter discussed the CMOS integration of the FAC, based on heterodyne receivers architectures used in wireless communication systems.

In this context, we analyzed three frequency bands (FM, video and digital cellular frequency bands) as our target application, focusing on the receiver architectures and how the signals are processed for each application. Several receiver architectures with ADC were reviewed, considering it general system specifications. Finally, we presented our initial set of system specifications for the FAC, aiming the signal processing of the three target applications previous analyzed.

Thus, the next step must be analysis of the best architecture for the building blocks that composes the FAC. First, Chapter 4 will present some experimental results

obtained from an early low-frequency implementation of a bandpass filter and comparator aiming a continuous-time ΣΔ modulator suitable for the FAC developed on the author's Master dissertation. Finally, from chapter 5 until the end of this thesis, we propose, analyze and implement the building blocks of the RF section of the FAC system.

4 BASEBAND BLOCK DESIGN AND EXPERIMENTAL RESULTS

In the author's Master dissertation (CORTES, 2003), several analog blocks were designed and implemented in 0.35μm CMOS technology. These blocks were analyzed using different design methodologies: a conventional design methodology, based on the modeling where a current equation is obtained considering that the transistor is in the saturation region, and a design methodology based on the g_m/I_D characteristic (SILVEIRA, 1996), that allows a unified synthesis methodology in all regions of operation of the transistor. More specific, three analog building blocks were analyzed, designed and implemented aiming the baseband section of the FAC, i.e., the continuous-time ΣΔ modulator stage: an operational transconductance amplifier (OTA), a bandpass continuous-time filter and a switched analog comparator.

This work is considered as a first analysis of the FAC building blocks integration, aiming CMOS low frequency analog blocks design, analyzing and demonstrating the g_m/I_D design method (which will be use in the design of RF blocks of the FAC in this work). The analog building blocks were prototyped in a test chip fabricated in AMS 0.35μm CMOS technology.

This chapter will present the experimental results obtained from this early low-frequency implementation of the baseband FAC's building blocks. First, we briefly review the implemented building blocks architectures and design using the g_m/I_D method. Following a quick overview of the prototyped test chip on which the blocks were fabricated is presented. Finally, we present the experimental results obtained from the test chip prototype, validating the design method.

4.1 Low frequency analog blocks design using the gm/ID method

Most methods for analytical synthesis of analog circuits suppose that the MOS transistors are either in strong inversion or weak inversion. The design methodology based on the g_m/I_D transistor characteristics, proposed in (SILVEIRA, 1996), allows a unified synthesis methodology which is valid in all regions of operation the MOS transistors. In this method, we consider the relationship between the ratio of the transconductance gain g_m over the DC drain current I_D, and the normalized drain current $I_D/(W/L)$ as a fundamental design relationship to be explored over the entire design space.

Considering that the g_m/I_D ratio and the normalized current $I_D/(W/L)$ are independent of the transistor sizes, the relationship between them represents a unique characteristic for all transistors of the same type (NMOS and PMOS) in a specific technology. This "universal" quality of the g_m/I_D vs. $I_D/(W/L)$ curve can be exploited during the design phase, when the transistors aspect ratios (W/L) are unknown. Once the value of the g_m/I_D ratio is chosen, i.e., the device operation region is determined, the W/L of the transistor can be determined in the curve.

Figure 4.1 shows the g_m/I_D versus $I_D/(W/L)$ curves (NMOS and PMOS) obtained through measurements and electrical simulations for the AMS0.35µm CMOS technology (CORTES, 2003). For the blocks design, the simulated g_m/I_D curve was considered, since the experimental data was not available at that time.

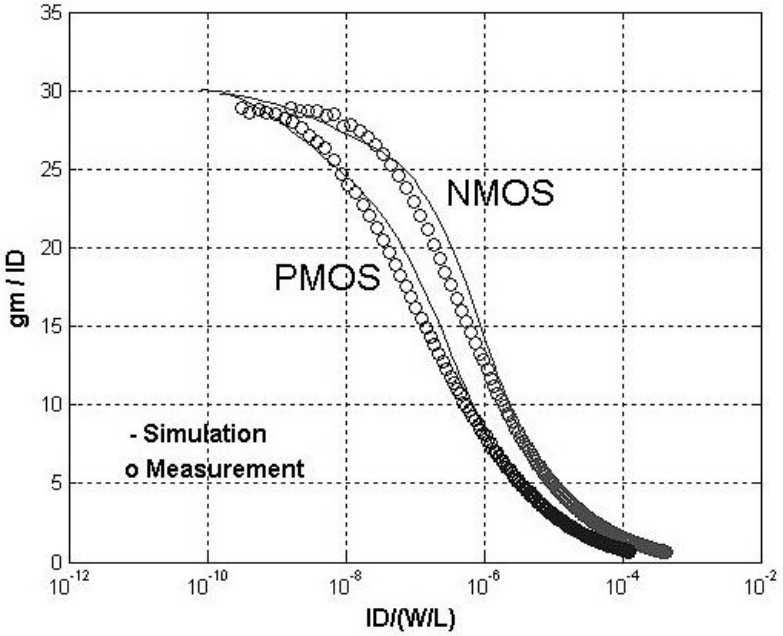


Figure 4.1: Simulated and measured g_m/I_D curves for NMOS and PMOS transistors in CMOS 0.35µm technology.

For each analog block the designer has to deal with a fixed power (or current) budget. Then, with the drain current desired – normally at a maximum level set by power or bandwidth constraints – and the operation region of the transistors is chosen, the W/L ratio of each transistor can be found using this curve (CORTES, 2003) (SILVEIRA, 1996).

In the next subsections, we briefly review the architectures and design using the g_m/I_D method of each building block, considering a 5MHz 1-bit second-order bandpass ΣΔ modulator implementation with a simple set of system requirements for the FAC (CORTES, 2003).

4.1.1 Bandpass *Gm-C* filter

Continuous-time transconductance-C (*Gm-C*) filters have been widely used for several applications such as digital video, RF/IF filters, and continuous-time ΣΔ

modulators (SCHAUMANN, 2005). The basic building block of a Gm-C filter is an integrator: basically a transconductor and a capacitor. The transconductors employed in these filters must be linear over the expected signal swing; hence the design of the transconductor is critical. Although high-frequency filters are the main aim of this topology, Gm-C filters can be used for integrated filters at low frequencies.

Figure 4.2 shows the filter's chosen architecture: a fully-differential continuous-time *Gm-C* band-pass filter with a *biquad* circuit topology. This topology was selected to provide a simple structure that demonstrates the capabilities of the technology and the filter design methodology. The filter was implemented using the 3 identical OTA as the transconductors. The 4 capacitors were fixed at *2pF* (*2C*), and laid out as a double-poly capacitor (in this way, the non-linear gate capacitance effects will not interfere in the amplifier performance). All transconductors operate with one common bias generating circuit, which improves the matching between the filter's stages over the tuning range.

The filter center frequency *Fc* was designed for 5MHz, with a quality factor *Q* of about 50, considering a load *C= 1pF* (CORTES, 2006-a).

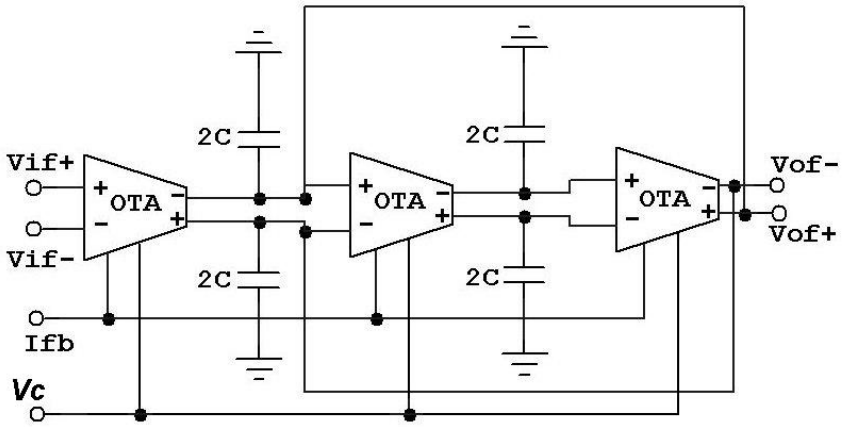


Figure 4.2: Gm-C band-pass biquad filter topology.

Figure 4.3 shows the operational transconductance amplifier (OTA) used in the filter implementation. Again, a simple structure was selected that demonstrated the capabilities of the technology and the transconductor design methodology. Because of the fully differential circuit, a common-mode feedback circuit (CMFB) is needed to set the DC output level of the OTA. A simple circuit is used that amplifies the common-mode signal while rejecting the differential signal. The source degeneration technique (SÁNCHEZ-SINENCIO, 2000) was used for the transconductor linearization. The OTA input transconductance gain can be tuned by a tunable resistor, implemented by the NMOS transistor M3 operating in the triode region and controlled by the voltage *Vc*.

The transconductors were designed using the g_m/I_D method, considering the filter's specifications. For each transistor, the g_m/I_D factor is chosen, and then the normalized current $I_D/(W/L)$ is determined for each transistor from the g_m/I_D *vs.* $I_D/(W/L)$ curve for the target technology. Then, with the drain current value found, the *W/L* of each transistor can be obtained. The complete design procedure is described in detail in (CORTES, 2003).

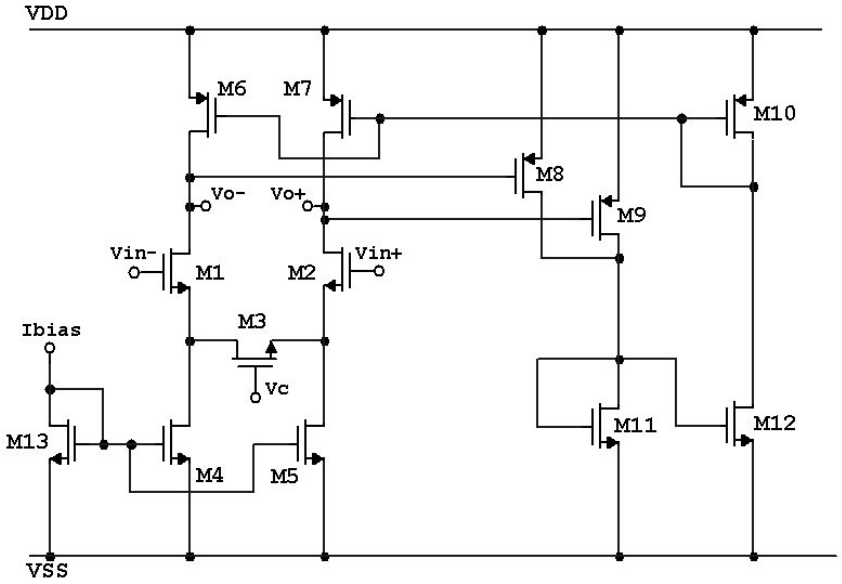


Figure 4.3: OTA used for the filter implementation.

4.1.2 Track-and-latch comparator

The comparator executes two important tasks in 1-bit ΣΔ modulators: comparison and binary quantization adjusting the modulator output to a digital logic level. The track-and-latch comparator topology (CHOI, 2001), shown in Figure 4.4, is composed by an NMOS input differential pair M1-M2, inverters M3-M8 and M4-M9 in positive feedback configuration, pre-charge transistors M6-M7, and by the current source controlled (*phi1*) M5. It has the advantage of low stand-by dissipation, since it shuts down current consumption after the clocked comparison.

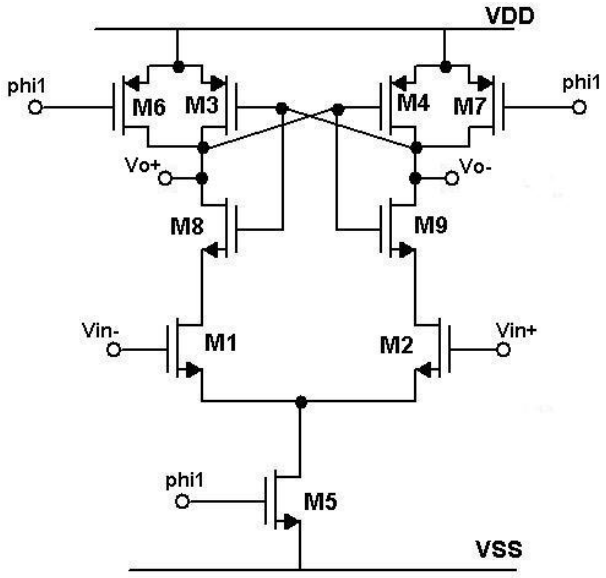


Figure 4.4: CMOS Track-and-latch switched analog comparator.

The input signals must be stable during the comparison semi-cycle *phi1* (clock). At the rising edge of the clock *phi1*, the pre-charge transistors are "open" and the differential pair is activated, initiating the comparison. In the pre-charge phase (inactive semi-cycle), the current of M5 (I_{tail}) is turned off and the input drivers are reset. The outputs *Vo+* and *Vo-* are pre-charged to V_{DD}. The speed of this type of comparator is strongly dependent on the I_{tail} current, that is, speed is directly proportional to the current in M5.

The comparator design must meet the following specifications (CORTES, 2006-b): 50mV sensitivity, 5MHz operating frequency, $C_L = 100fF$. The g_m/I_D method was used, where the design optimizes both the speed and the power consumption, as long as reasonable sensitivity and gain are achieved. Once the design operating frequency is reached, the power consumption is set by the current I_{tail}. While the design does not meet the specifications, it is iteratively improved by changing the size of the differential pair M1-M2, until the desired performance is achieved. The complete design procedure is detailed described in (CORTES, 2003).

4.2 System chip

A test chip with several analog blocks and test vehicles, including the designed Gm-C filter and comparator, was fabricated in AMS 0.35µm CMOS technology. The total chip area including pads is 4.55 mm². The die microphotography of the chip is shown in Figure 4.5. Details about the chip components and areas of the blocks are in Table 4.1.

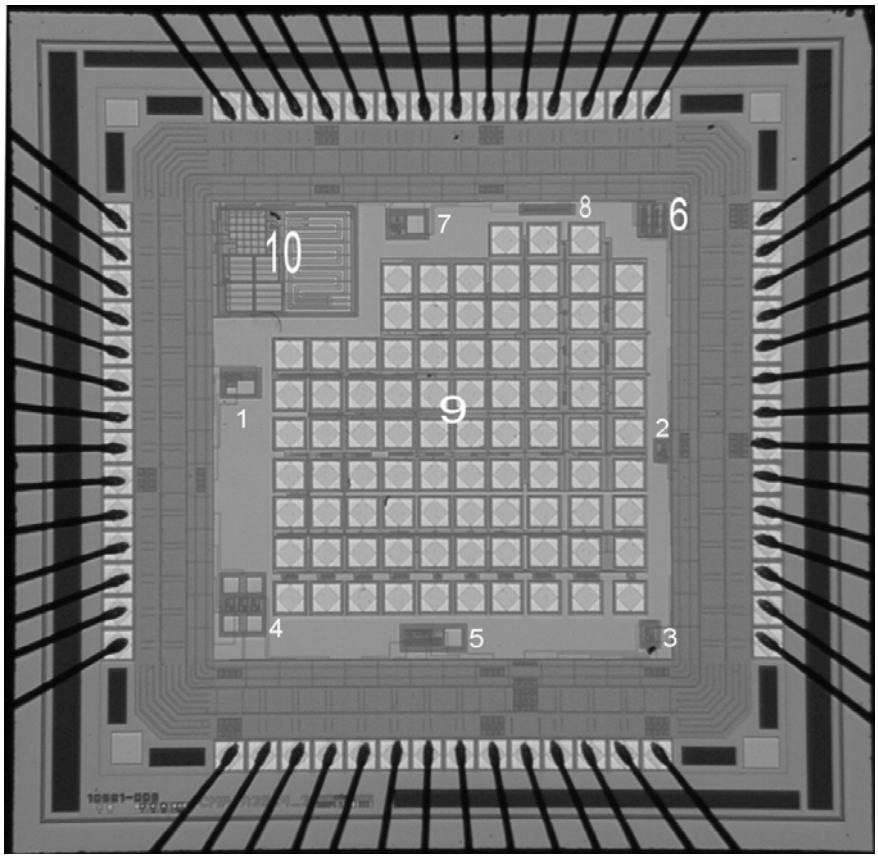


Figure 4.5: AMS 0.35µm test Chip die microphotography.

Table 4.1: AMS 0.35µm test chip components overview.

	Block	*Area (µm²)*
1	Miller OTA - Ver. 1	83 x 119
2	Comparator – Ver. 1	41 x 70
3	Filter's OTA	56 x 82
4	Gm-C bandpass filter	90x70
5	Miller OTA - Ver.2	77 x 198
6	Comparator – Ver. 2	93 x 108
7	Miller OTA - Ver.3	90 x 125
8	Ring oscillator	29 x 165
9	Test structures	1,100 x 1,150
10	Band-gap ref.	350 x 400
Total Area		2,134 x 2,134 mm²

The chip was tested in a 10cm x 13cm printed circuit board (PCB), where each target block output was connected to a buffer stage (external discrete components). Figure 4.6 shows the simplified block diagram, including the configurations for the OTA, bandpass filter and comparator blocks, of the testing boarding. The photograph of the actual PCB is showed in Figure 4.7.

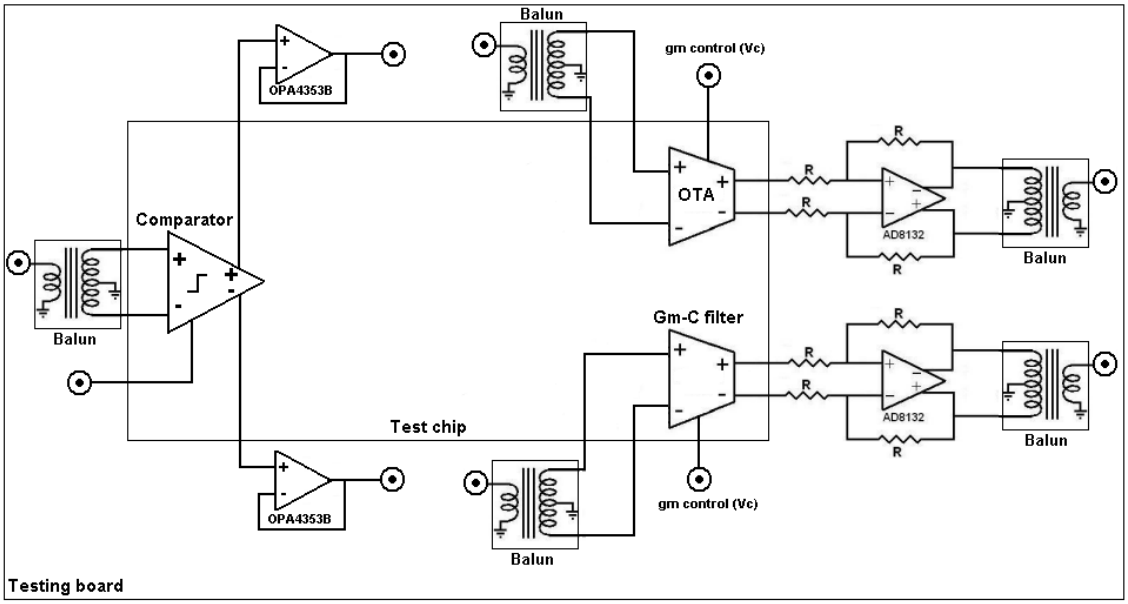


Figure 4.6: Simplified block diagram of the testing board.

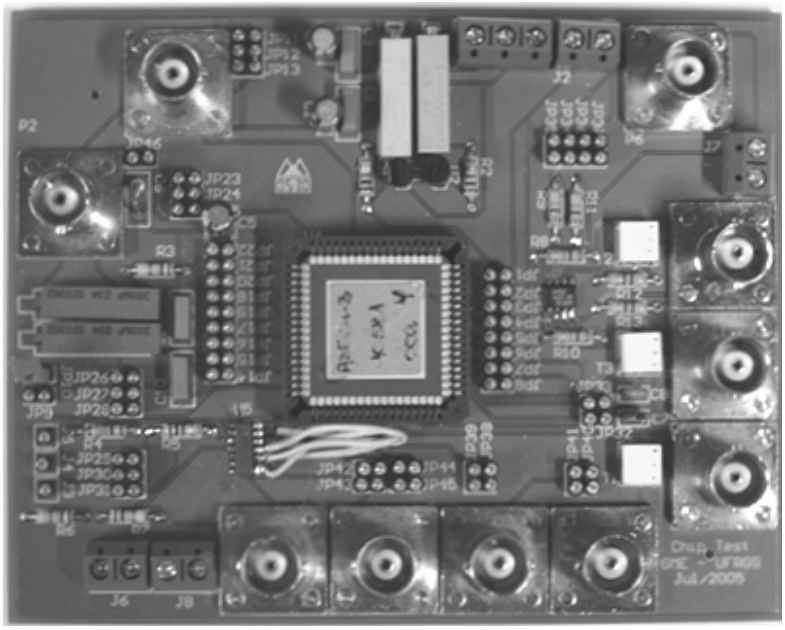


Figure 4.7: Test board with discrete components for the test chip.

4.3 Experimental results

We now present the performance measurements of each analog block obtained from the testing board described in the previous section (Figure 4.5).

The input signals were generated by Agilent 33250A Waveform Generator and the DC bias by Agilent E3630A DC Power Supply. The output signals were measured using the Tektronix 2420 Oscilloscope 500MS/s. The cable/board load was estimated in *20pF*.

All the results reported herein are an average of measurements on 5 encapsulated samples.

4.3.1 OTA

The operational transconductance amplifier (OTA) used in the filter implementation was tested connecting its output to an off chip buffer stage (AD8132 amplifier). From this test configuration (showed in Figure 4.6), an input sinusoidal signal of $f = 1MHz$ and A= $400mVpp$ is applied to the OTA, with a current bias of 25µA. The output signal is then obtained from the buffer stage output. The OTA transconductance gain was controlled by the voltage *Vc*, from 0.1 – 1V.

Figure 4.8 shows the measured frequency response of the maximum achievable transconductance gain (*gm*) of the OTA (for a fixed voltage bias - *Vc=1V*). Table 4.2 summarizes the measured performance of the OTA.

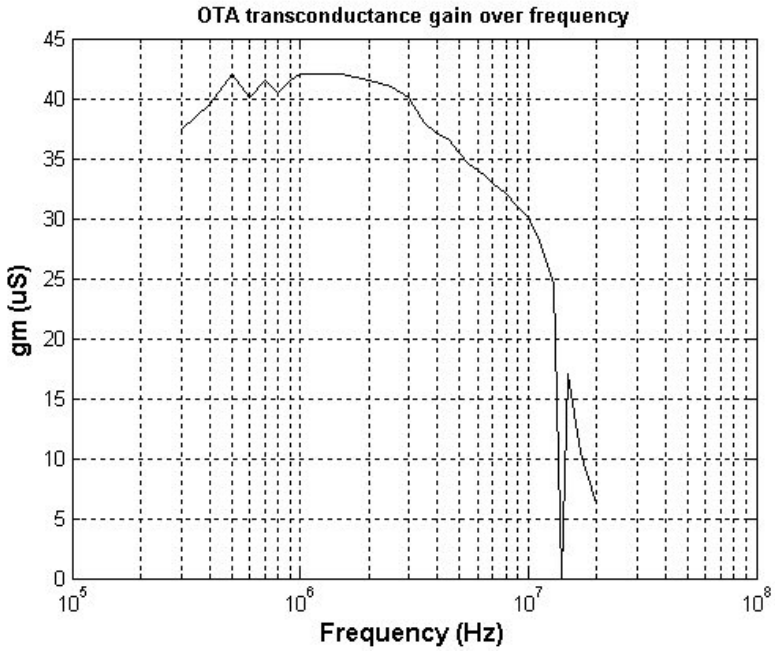


Figure 4.8: Measured frequency response of the maximum achievable *gm* of the OTA - *Vc=1V*.

Table 4.2: Summary of the measured performance of the OTA.

VC = 0.1V			*VC = 0.5V*			*VC = 1V*		
Vout(Vpp)	gm(µS)	IDD(µA)	Vout(Vpp)	gm(µS)	IDD(µA)	Vout(Vpp)	gm(µS)	IDD(µA)
112.4m	28.1	121.48	142.4m	35.6	121.48	158m	39.5	121.48

4.3.2 Bandpass *Gm-C* filter

The same test configuration described above was used in the filter test. An input sinusoidal signal of amplitude of A= $400mVpp$ is applied to the filter's input, varying its frequency, with a current bias of 30µA. The output signal is then measured in output of the buffer stage. The center frequency *Fc* of the filter can be adjusted according the value of the bias voltage *Vc*.

The measurements results show a frequency range of operation from 4.24 MHz to 4.9MHz while the quality factor ***Q*** is about 25. Figure 4.9 shows the measured results of the frequency response of the filter, under 3 different bias conditions for *Vc*.

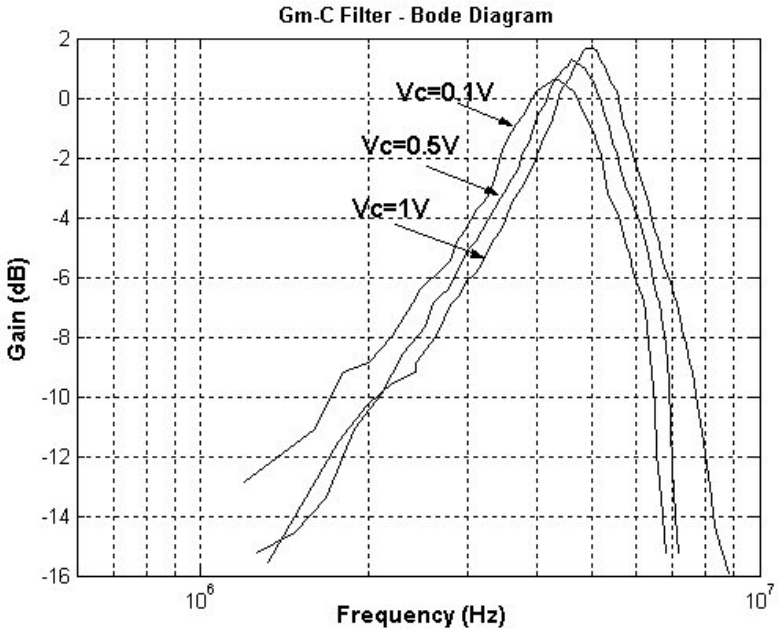


Figure 4.9: Measured frequency response of the filter, tuned by *Vc*.

Table 4.3 shows an overview of the measured filter performance. There is significant decreasing in the filter's quality factor performance in the experimental results (a ***Q*** of about 100 was estimated by simulation). This is due to the larger variation of the transistor's output conductance for short channel devices in the prototyped samples, where the filter's quality factor is inversely proportional to the output conductance parameter ($Q = gm/3Go$). Also, the output load (from the test setup) variations can contribute to decrease the circuit performance.

Table 4.3: Summary of measured performance of the filter.

Fc (MHz) (Vc = 0.1 - 1V)	4.2-4.9
Q	25
Output Swing (V)	-0.45/+0.6
Current consumption (μA)	263

4.3.3 Track-and-latch comparator

In the comparator test configuration, each output was connected to a buffer stage (AD8132 amplifier), with unit gain configuration. An input sinusoidal signal of $f = 100kHz$ and a square clock signal (*phi1*) of $f = 5MHz$ were applied to the comparator.

Figure 4.10 shows the measured performance of the comparator. At the rising edge of *phi1*, the pre-charge transistors are open and the differential pair is activated, initiating the comparison. In the pre-charge phase, the pre-charge transistors are off, and the input drivers are reset. The outputs *Vo+* and *Vo-* are pre-charged to V_{DD}. The

sensitivity of the comparator can also be measured: the input signal amplitude is decreased until the comparison is achieved.

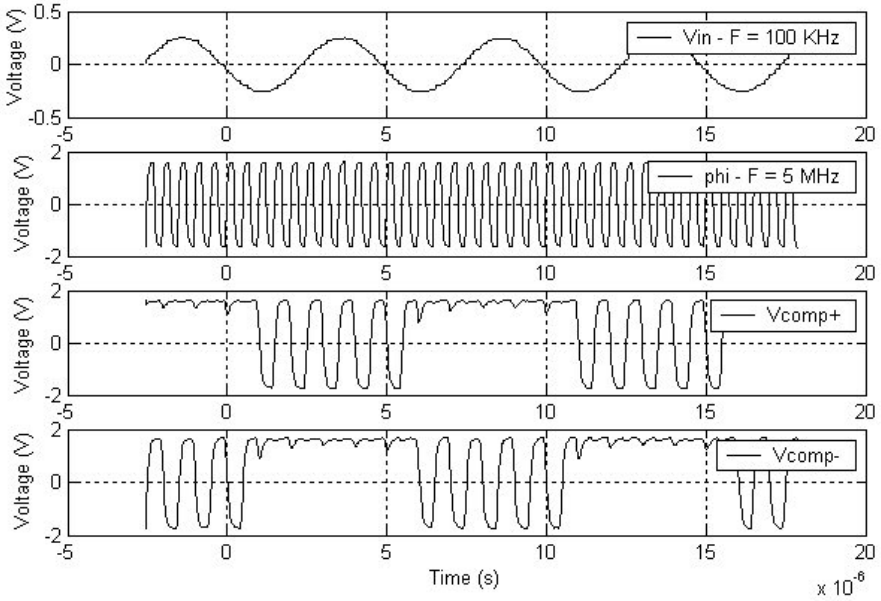


Figure 4.10: Measured performance of the comparator: Fin=100 kHz and phi1=5MHz.

Figure 4.11 shows the measured plot of the current of M5 (I_{tail}), where the standby current in the *phi1* inactive semi-cycle is very low (about 40µA), which minimizes power consumption.

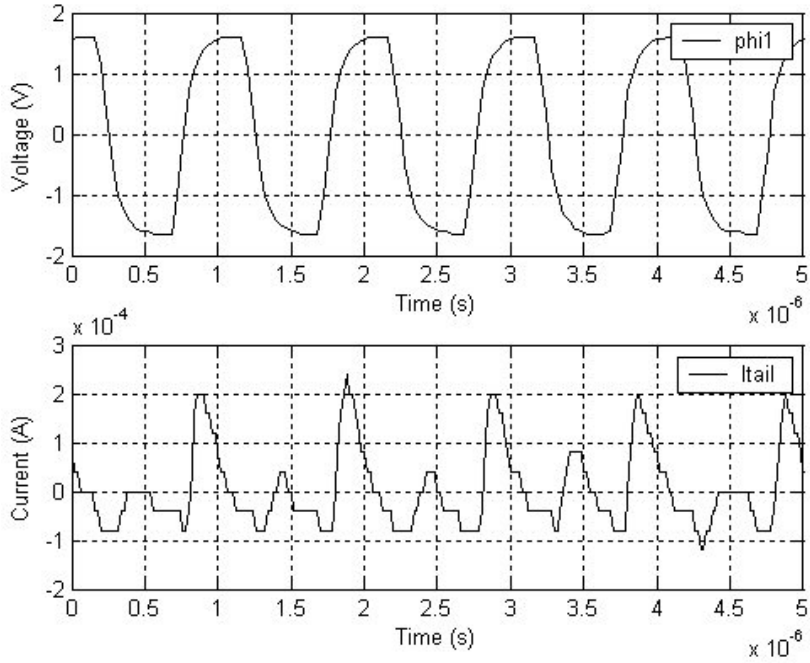


Figure 4.11: Measured switched tail current of the comparator – Fin=100 kHz and phi1=1MHz.

The complete characterization of the comparator is shown in Table 4.4. The design shows good performance in comparison to the given specifications, except for larger differential input sensibility, due to the dependency of the comparator maximum frequency on the current that feeds the differential pair (I_{tail}) (CORTES, 2003).

Table 4.4: Summary of the measured performance of the comparator.

Delay td_{hl} *(ns)* (phi1 *50m*$V_p \rightarrow V_{o+}$)	80
$f_{máx}$ (MHz)	18
Sensibility ΔV_{in}(V_p) @ 5MHz	184m
I_{tail} (μA)	288

4.4 Discussion

In this chapter, we presented the experimental results obtained from an early low-frequency implementation of analog blocks aiming a continuous-time ΣΔ modulator suitable for the baseband section of the FAC, developed on the author's Master dissertation (CORTES, 2003): an operational transconductance amplifier (OTA), a bandpass Gm-C filter and switched analog comparator. A quick overview of the test chip, fabricated in 0.35μm CMOS technology, was presented, including the testing configuration of each block realized in a discrete testing board.

The measurements results demonstrate the capability of the g_m/I_D design method, which will be use in the following design of the analog blocks that composes the RF section of the FAC (IF front-end).

5 RF BLOCK DESIGN – THE IF FRONT-END

We now discuss the RF section of the FAC, the front-end stage. It translates the input signal to the processing frequency, providing a gain control to adjust the input signal dynamic range. This stage is critical to the system performance.

In this chapter, we discuss heterodyne and homodyne receivers architectures, looking for the best front-end architecture choice suitable for the FAC integration. Following the determination of the front-end architecture, we discuss the main system level design issues, determining the optimal specifications for the system and for each building block. Finally, the front-end overall system performance is verified by system level simulations.

5.1 Front-end architecture

In the next subsections, we discuss the main receivers architectures used in wireless applications (LEE, 1998) (RAZAVI, 1998-a) (RAZAVI, 1998-b), looking for the best choice suitable for our application.

5.1.1 Heterodyne architectures

In heterodyne architectures (also called Low-IF architectures), the signal band is down-converted to a lower frequency (called intermediate frequency – IF), as illustrated in Figure 5.1. The translation is carried out by a mixer, followed by a filtering and amplification. Because of its typically high noise, the mixer stage is usually preceded by a low-noise amplifier.

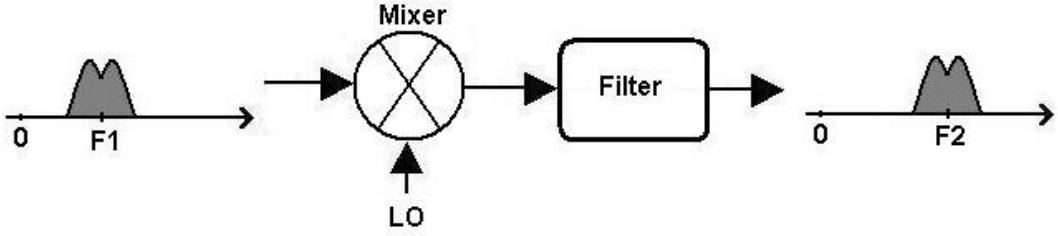


Figure 5.1: Simple heterodyne down-conversion.

The primary motivation for choosing this type of architecture is that such a frequency lowering makes it easier to realize high-quality IF filters and to obtain the requisite gain. However, it also entails several performance drawbacks, which are discussed as follows.

5.1.1.1 The image problem

Perhaps the most significant problem of this topology is the "image frequency". In order to understand this effect, let us consider that the signal of interest has an image (also called interferer) and a simple analog multiplier does not preserve the polarity of the difference between its input frequencies. Thus, in a heterodyne architecture, the bands both above and below the LO frequency are translated to the same intermediate frequency, as illustrated in Figure 5.2. If the received band of interest is centered around $F1\ \left(=F_{LO}-F_{IF}\right)$, then the image is around $2F_{LO}-F1\ \left(=F_{LO}+F_{IF}\right)$ and vice versa.

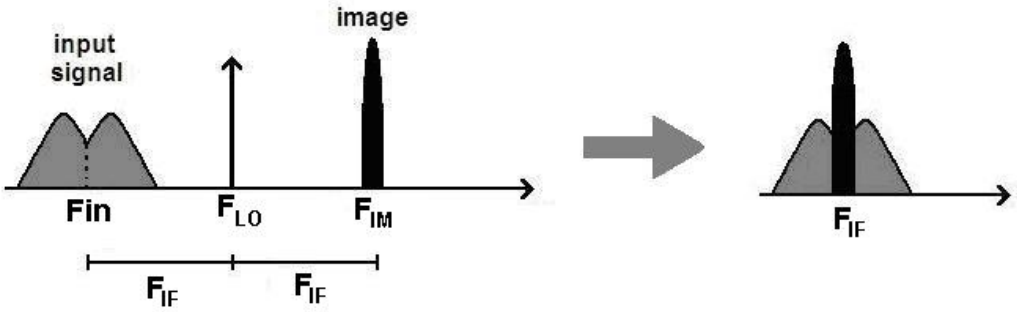


Figure 5.2: Image problem in heterodyne architectures.

This effect is very important, mostly when the image power is much higher than the main input signal, requiring a proper "image rejection" in the system.

The most common approach to suppressing the image is the use of an image rejection filter before the mixer (RAZAVI, 1998-b). This issue leads to some trade-offs between the amount of image noise, the spacing between the signal band and the image and the loss of the filter. This type of filter is usually realized as a passive, external component.

5.1.1.2 The half-IF problem

Another interesting effect in heterodyne receivers is the "half-IF" problem (RAZAVI, 1998-a), illustrated in Figure 5.3. Considering that in addition to the desired signal at *Fin*, an interferer at $\left(Fin+F_{LO}\right)/2$, i.e., half of the IF from the desired band toward the LO frequency, is also received. If in the receiver path, the interferer experiences second-order distortions and the LO contains a significant second harmonic, then the output will exhibit a component at $\left|\left(Fin+F_{LO}\right)-2F_{LO}\right|=F_{IF}$. If the interferer is translated to $\left(Fin-F_{LO}\right)/2=F_{IF}/2$ and a second-order distortion undergoes at the baseband, its second harmonic can also fall into the output band of interest. This phenomenon is also called harmonic mixing.

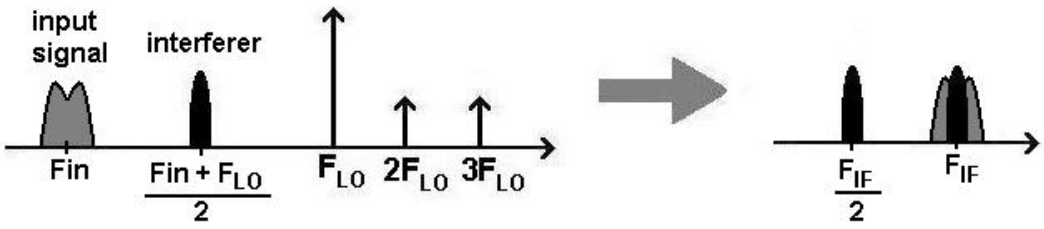


Figure 5.3: The half-IF problem in heterodyne architectures.

In order to suppress this phenomenon, second-order distortion in the input paths (RF and IF) must be minimized, and a 50% LO duty cycle must be maintained (RAZAVI, 1998-a). It may also be necessary an image-reject filter that achieves sufficient attenuation at interferer frequency.

5.1.2 Dual-IF heterodyne architectures

In order to resolve the image and half-IF issues, the concept of heterodyning can be extended to multiple down-conversions, each followed by filtering and amplification. Showed in Figure 5.4, this technique performs partial channel selection at progressively lower frequencies, relaxing the *Q* required of each filter. Most of today's RF receivers employ two stages of down-conversion, hence the name "dual-IF". However, in the second down-conversion the image problem is still critical, and since more cascade elements are present in the receiver path, the noise is also critical.

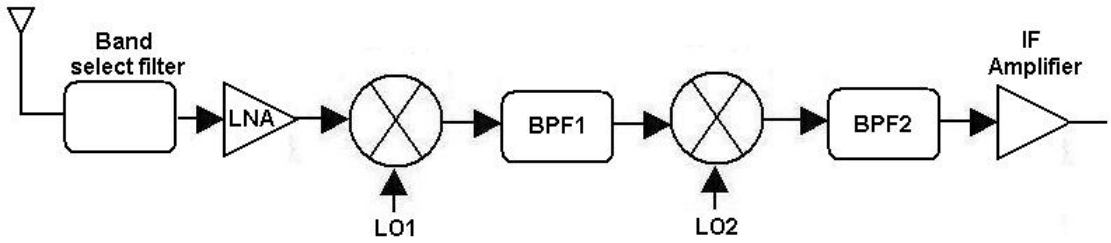


Figure 5.4: Dual-IF heterodyne receiver.

Another solution is to combine both down-conversion and up-conversion in the receiver path (LEE, 1998). In a dual-conversion superheterodyne receiver, a first mixer produces a high IF to take care of the image rejection issue, while a second mixer produces a low IF to take care of the channel selection problem. Some receivers employ a third IF to provide even greater flexibility in the tradeoff.

Despite the complexity and the need of a large numbers of external components, heterodyne architectures are still viewed as the most reliable reception technique nowadays.

5.1.3 Homodyne architectures

In homodyne architectures, the signal of interest is simply translated to the baseband in the first down-conversion. Also called “direct-conversion”, or “zero-IF” architecture, it entails several different issues from heterodyne topologies. A simple homodyne architecture is shown in Figure 5.5, where the LO frequency is equal to the input carrier frequency.

The simplicity of the homodyne architecture offers two important advantages over its heterodyne counterpart. Fist, the problem of image is solved, since $IF = 0$. As a result, no image filter is required. Second, the IF filter and subsequent stages are replaced by low-pass filters and baseband amplifiers that are more suitable for monolithic integration.

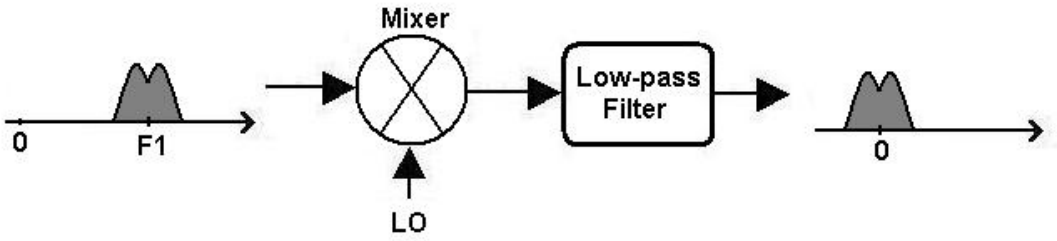


Figure 5.5: Simple homodyne architecture.

Despite the advantages named above, direct translation of the spectrum to zero frequency entails a number of issues that do not exist (or are not as serious) in heterodyne topologies The main problems are channel selection (rejection of out-of-band interferers by active low-pass filter is more difficult), DC offsets (offset voltages can corrupt the signal and saturate the following stages), I/Q mismatch, LO leakage, even-order distortion and flicker noise interferences (RAZAVI, 1998-a).

5.1.4 Proposed front-end architecture suitable for the FAC

Since we intend to work with a wide range of frequencies (FM, video and cellular frequency bands), down-converting the signal to an IF inside the input frequency band without proper pre-filtering will inevitably result in the image and half-IF problems described in Section 5.1. This filtering is usually made by bulky tunable RF resonant tanks, as in conventional superheterodyne TV tuners (VAN SINDEREN, 2003), that not only suppress higher band channels to be mixed down by the harmonics of the LO but also filter out the image channel. However, this superheterodyne architecture is not amenable to monolithic integration, since tunable RF bandpass filters with high Q are difficult to integrate on a chip.

In order to circumvent this problem, an up/down dual-conversion system can be considered, as in (CONNEL, 2002) (HENG, 2005). This architecture does not require tunable RF filters. The reason for the up-conversion for a higher first IF outside the input frequency band is to avoid both image and half-IF components. The signal is then down-converted to a lower IF for channel selection and demodulation. A passband filter

is still required to suppress image components at the fixed IF rather than at the RF, that are usually external components limiting the level of integration.

Considering the previous analysis, we now propose a dual-conversion heterodyne architecture for the variable-gain front-end required for the FAC system. The primary purpose of this front-end is simply to convert an input signal to a processing frequency, where the input signal and bandwidth are allowed to vary from the 3 previous discussed applications.

The complete dual-conversion architecture, showed in Figure 5.6, is described as follows. The input signal enters an up-conversion mixer, which translates this signal to the first IF outside the input frequency band. A simple on-chip LC tank is then applied to the signal, suppressing harmonic mixing and image components. A down-conversion mixer translates the signal to a second low IF and a variable gain amplifier (VGA), provides gain adjustment. The selected signal is ready to be sampled by the ΣΔ modulator stage, and then processed by the digital block in the full mixed-signal interface, where channel selection and image cancellation can be made.

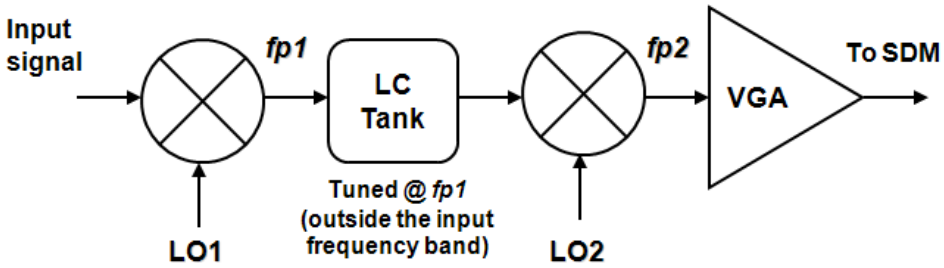


Figure 5.6: Proposed heterodyne architecture to be used in the FAC system.

At least two frequency synthesizer blocks should be implemented in the FAC, since it is necessary two LO signals capable of translating the input signal to both intermediate frequencies.

5.2 System design issues

In the following subsections, the main system design issues in the chosen front-end architecture are discussed. The goal here is to determine the optimal specifications for the system.

5.2.1 Processing frequencies

Regarding the choice of the most appropriated processing frequencies *fp1* and *fp2* (following the nomenclature used in the interface system described in Chapter 2, the intermediate frequency is referred as processing frequency), we now briefly discuss some tradeoffs.

Considering the wide range of input signals that enters the front-end, the first *fp* must be chosen to be out of the input frequency band. In order to avoid any signal interference between the input and translated signals, *fp1* must be distant at least half of

the larger signal bandwidth from the highest input signal frequency. If we consider that the highest input signal frequency is 960MHz and half of the larger signal bandwidth is 406MHz (half of the VHF/UHF TV tuner band), we conclude that at least *fp1* should be 1.366GHz. Thus, *fp1* is chosen to be 1.4GHz. Figure 5.7 illustrate this issue.

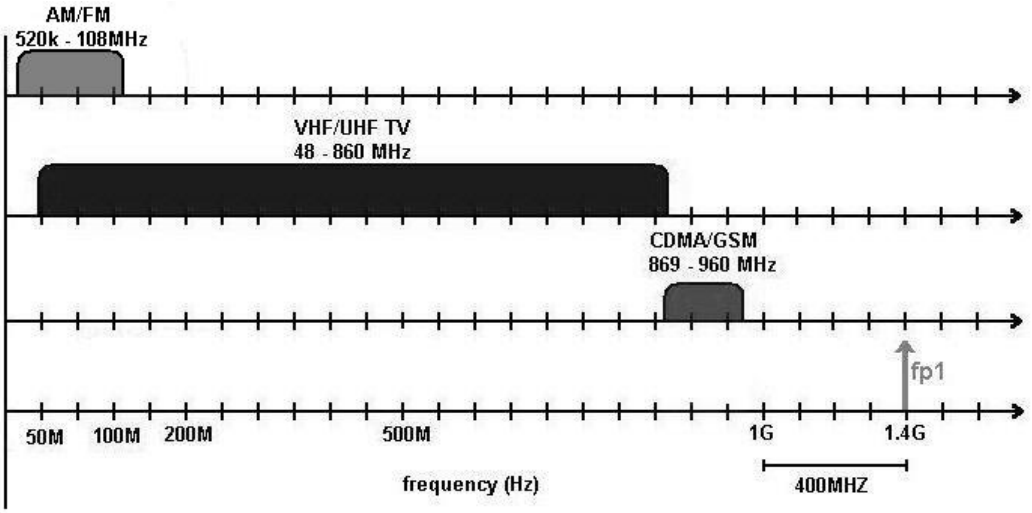


Figure 5.7: Choice of the first processing frequency.

The second *fp* is chosen to be 40 MHz (as in TV tuners and low-IF digital cellular receivers), based on the analysis made in Chapter 3. The VGA and CT band-pass ΣΔ modulator stages can be easily implemented at this operating frequency.

5.2.2 Sensitivity, linearity and noise

The key specifications of any receiver architecture are the sensitivity, linearity (IIP3) and noise (NF) specifications. These parameters were derived from the receiver specification analysis of each target application discussed in Chapter 3. Therefore, the required sensitivity is 1μVpp (-80dBm), NF is 15dB and IIP3 is -20dBm.

5.2.3 LO phase noise

Ideally, the output of the LO is a single tone signal in the required frequency. However, due to the thermal and *1/f* noise of the transistors used in the VCO circuitry, amplitude and phase noise components appear at the LO output. Amplitude noise is not critical because of the hard switching of the mixer transistors. Phase noise, in the other hand, is very critical in low-IF and direct conversion receiver architectures, mostly in the presence of strong interferers. The carrier is spread in frequency by the phase noise modulation, which results in a frequency component that is proportional to the LO phase noise. This effect is similar to the half-IF problem described in Section 5.1, where the LO harmonics can be replaced by the LO spreading produced by the phase noise.

However, considering our target dual-conversion heterodyne architecture, the phase noise issue is not critical in the first up-conversion stage, since these effects don't occur due to the fact that the carrier is outside the input frequency band. From the analysis of

phase noise specification of each target application, the LO phase noise requirement was set to -110dBc/Hz, which is easily achievable.

5.2.4 VGA dynamic range

The dynamic range of the VGA is determined by the input signal power level range and the required signal level at the ADC input. Assuming that the minimum (sensitivity) and the maximum signal levels are -80dBm to 0dBm, respectively, to cover this 80dB variation, the overall gain of the front-end must be adjusted that, for all signals levels, the signal at CT band-pass ΣΔ modulator stage input is within the allowable signal level (200mVpp). In order to have some margin in sensitivity and maximum signal levels specifications and the mixer gain variations, a 0-70dB VGA is specified.

5.2.5 Final system specifications

Based on the application mapping analysis of Chapter 3 and the system design issues described above, we now can obtain the initial specifications for the target dual-conversion heterodyne front-end architecture. Table 5.1 shows an overview of the requirements of this architecture.

Table 5.1: IF Front-end system specifications.

Frequency band	48MHz – 960MHz
Sensitivity	> 1μVpp
fp1	1.4 GHz
LC tank	tuned @ 1.4GHz
fp2	40 MHz
NF	< 15 dB
IIP3	> -25 dBm
LO phase noise	-110dBc/Hz
VGA gain range	0 - 70 dB

5.3 Determination of the front-end building blocks specifications

From the front-end system specifications, the specifications of the individual building blocks can be obtained. Conversion from system to blocks specifications is an interactive process, where first we start with an initial distribution, and then the overall system specifications are calculated to see if the system specifications are met. A *Matlab* code was developed to calculate the system parameters from the blocks specifications.

5.3.1 Gain distribution

The first step is to obtain the characteristics of the front-end system is to determine its gain distribution. Considering our target front-end architecture, composed by 2 mixers, the LC tank and the VGA, it is straightforward that a large fraction of the gain is given by the VGA.

According to typical values, both mixer gains are chosen to be 5dB. Therefore, in order to have some margin with the signal levels (a small attenuation can occur due to the LC tank), the VGA gain is specified to vary in the range of 0-70dB.

5.3.2 NF distribution

Considering the gain distribution in the previous subsection, we now can distribute the NF among the front-end blocks. The overall system NF is then calculated using the following equation of cascade stages:

$$System\_NF = 10 \cdot \log\left(10^{NF1/10} + \frac{10^{NF2/10}-1}{10^{A1/10}} + \frac{10^{NF3/10}-1}{10^{(A1+A2)/10}}\right)[dB] \qquad (5.1)$$

where *NFi* and *Ai* are the NF and gain of the ith stage, where the up-conversion mixer is the first stage. Equation 5.1 indicates that the noise contributed by each stage decreases as the gain of the preceding stages increases, implying that the first few stages are the most critical. According to typical values, the NF values are chosen to be 10dB, 12dB and 20dB, respectively for each stage.

5.3.3 IIP3 distribution

The same analysis can be used to distribute the IIP3 among the front-end blocks. The overall system IIP3 is then calculated using the following equation of cascade stages:

$$System\_IIP3 = 10 \cdot \log\left(\frac{1}{\sqrt{\frac{1}{\left(10^{IIP3_1/10}\right)^2} + \frac{\left(10^{A1/10}\right)^2}{\left(10^{IIP3_2/10}\right)^2} + \frac{\left(10^{A1/10+A2/10}\right)^2}{\left(10^{IIP3_3/10}\right)^2}}}\right)[dBm] \qquad (5.2)$$

where *IIP3i* and *Ai* are the IIP3 and gain of the ith stage. According to typical values, the IIP3 values are chosen to be 1dBm, -2dBm and -20dBm, respectively for each stage.

5.3.4 Building blocks and system specifications overview

From this initial distribution, now the overall system specifications can be calculated to see if the system specifications are met. Table 5.2 lists the contributions of each building block and the overall system specifications for this distribution.

Table 5.2: Front-end gain, NF and IIP3 distributions.

	Up-conversion mixer	*Down-conversion mixer*	*VGA*	*System*
Gain (dB)	5	5	70	80
NF (dB)	11	12	20	15
IIP3 (dBm)	1	-2	-20	-30

5.4 System design verification

Once all the block specifications are determined, the next step is to verify the front-end overall system performance. This is done by system level simulations that are performed using the *Agilent ADS* tool. *Agilent ADS* has an Analog/RF simulation environment that computes the response of a circuit to a particular stimulus by formulating a system of circuit equations and then solving them numerically (ADS, 2005). Each building block is emulated with a behavioral system model from a system component library provided by this tool.

Harmonic balance simulation was performed using *Agilent ADS*, providing a frequency-domain analysis of the system. It calculates the magnitude and phase of voltages or currents in a potentially nonlinear circuit with one or multiple input frequencies (ADS Manual, 2004). Figure 5.8 shows the basic simulation setup for the front-end simulations using *Agilent ADS*, and it is shown here as an example.

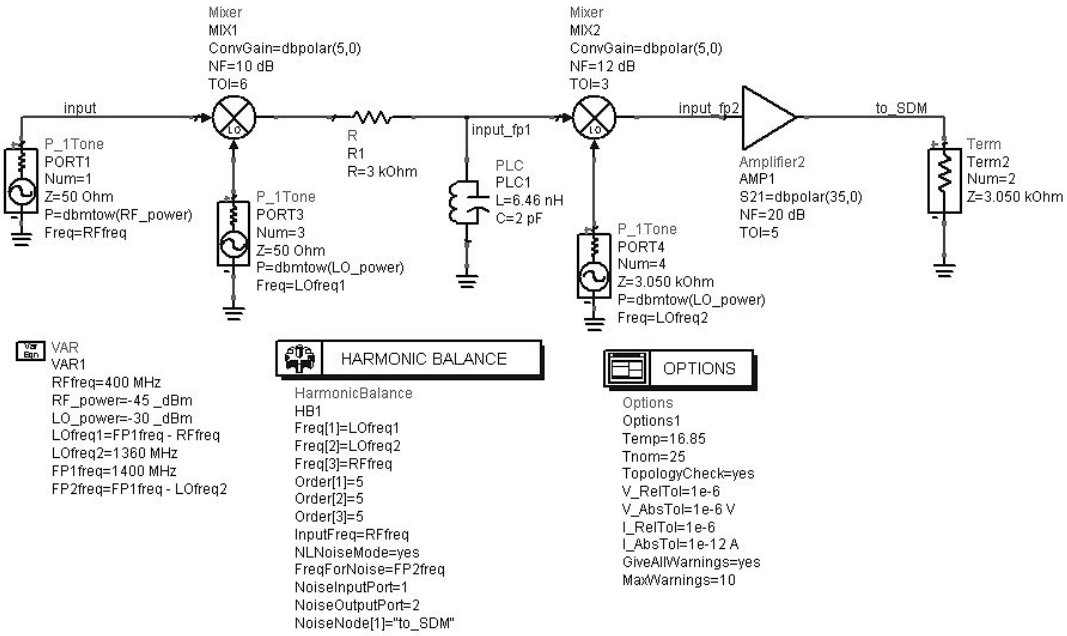


Figure 5.8: Front-end simulation setup in *Agilent ADS*.

The RF, LO1, LO2 frequencies as well the RF and LO power are all defined as variables, making it easier to change values and to rerun simulations if necessary. The quality factor (*Q)* of the LC tank was set to 50 in order to provide a reasonable suppression in the system.

In the next subsections, several simulations are made in order to verify the front-end system performance and main specifications.

5.4.1 Overall performance

The frequency-domain simulations, shown in Figures 5.9, 5.10 and 5.11, illustrate the overall performance of the entire system for the 3 previous discussed signal bands. In all simulations, an input signal of -45dBm (a) is applied to the front-end. The signal is up-converted to an *fp1* of 1.4GHz (b), where a LC tank tuned at this frequency suppresses undesired signals. The signal is then down-converted to an *fp2* of 40MHz (c) and its gain is adjusted such that the signal level at the output is around 0dBm (d). The gain of the system was set to 45dB.

As mentioned before, this result signal will be the input of the CT band-pass ΣΔ modulator stage in the FAC system.

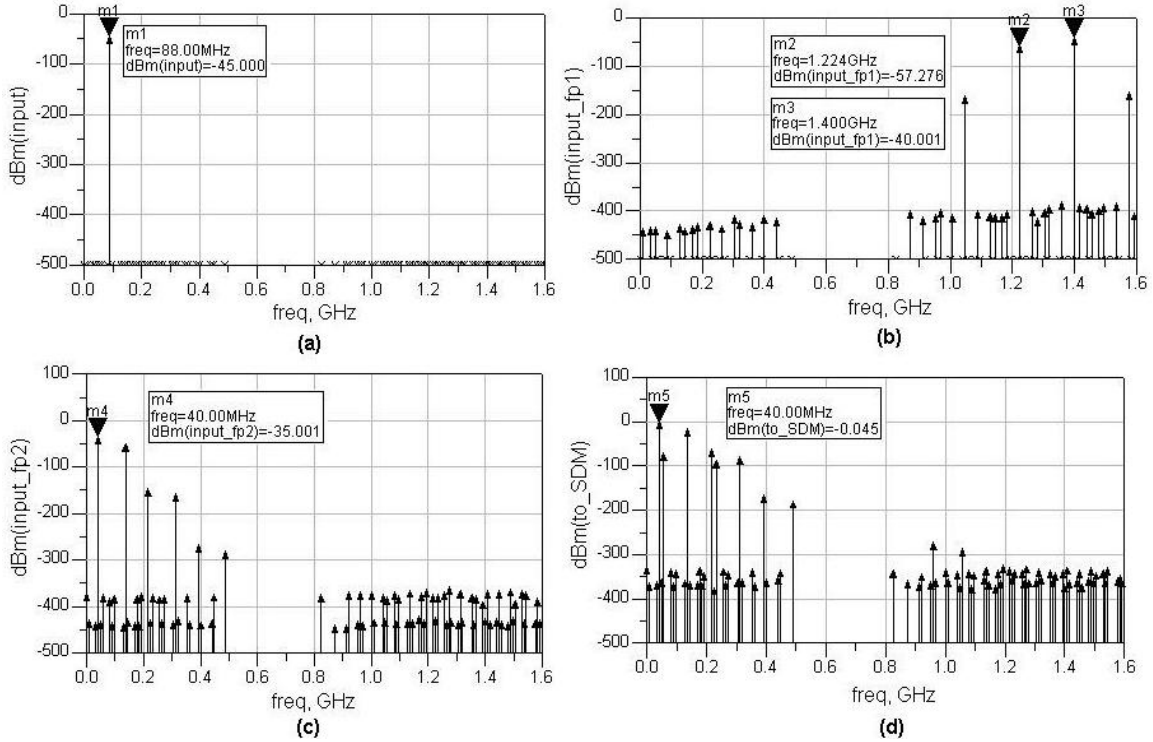


Figure 5.9: Spectrum (in dBm) of the system's overall performance applying a -45dBm input at 88MHz (FM band).

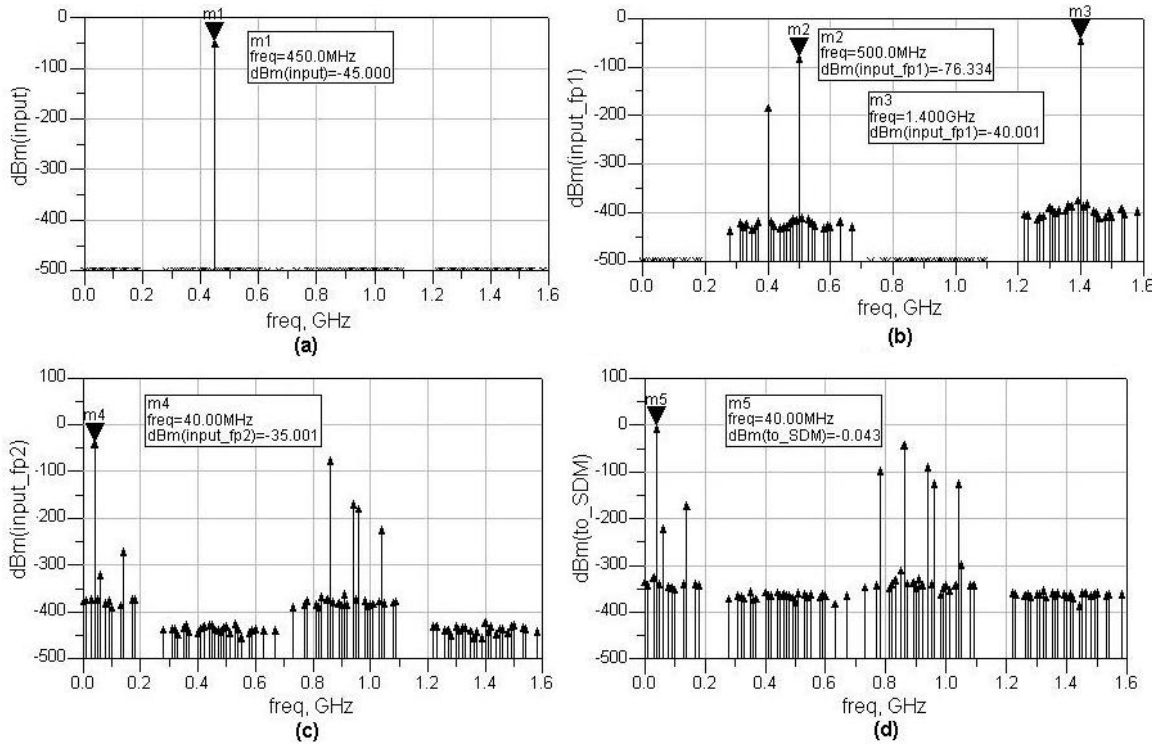


Figure 5.10: Spectrum (in dBm) of the system's overall performance applying a -45dBm input at 450MHz (TV tuner band).

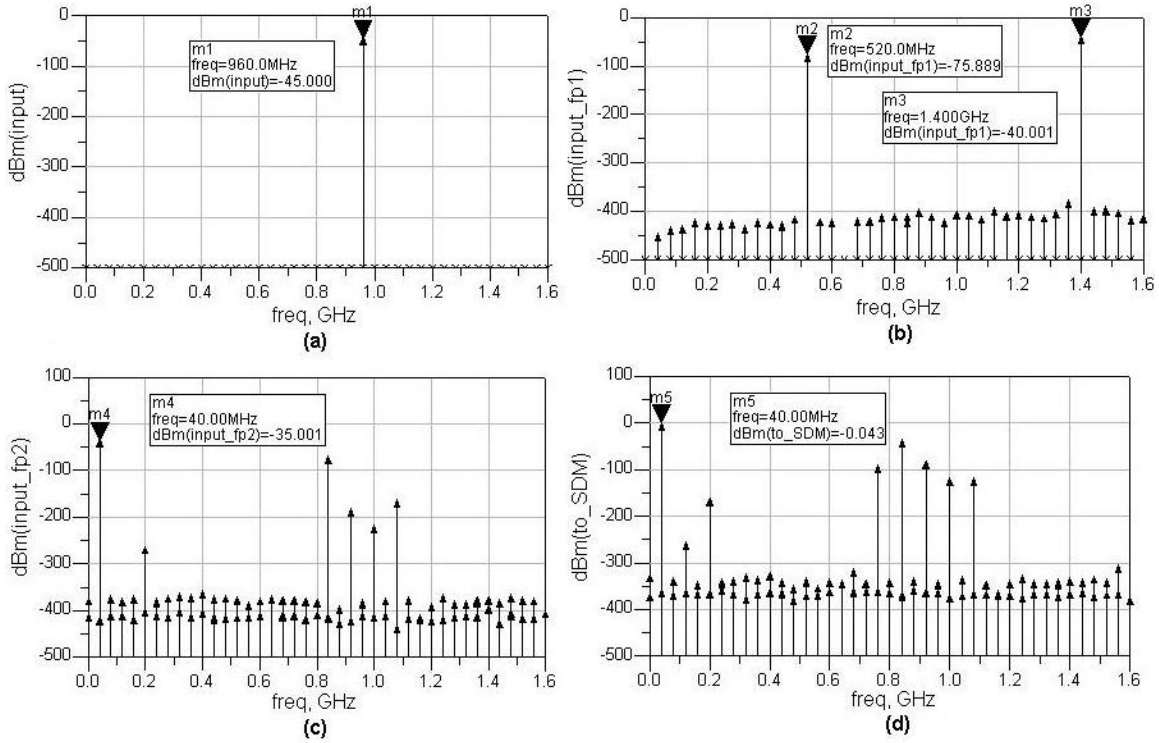


Figure 5.11: Spectrum (in dBm) of the system's overall performance applying a -45dBm input at 960MHz (Cellular band).

5.4.2 Gain and noise simulations

The same basic simulation setup of Figure 5.8 is used to obtain the conversion gain and noise figure at a single frequency. The conversion gain is calculated on the schematic, so this parameter could be optimized.

An input signal of -45dBm at 400MHz is applied to the front-end input (Figure 5.12a), resulting in an output signal around 0dBm at 40MHz (Figure 5.12b). Figure 5.12c shows the values obtained from the simulation. Thus, the conversion gain is 45dB and the noise figure is 17.72dB.

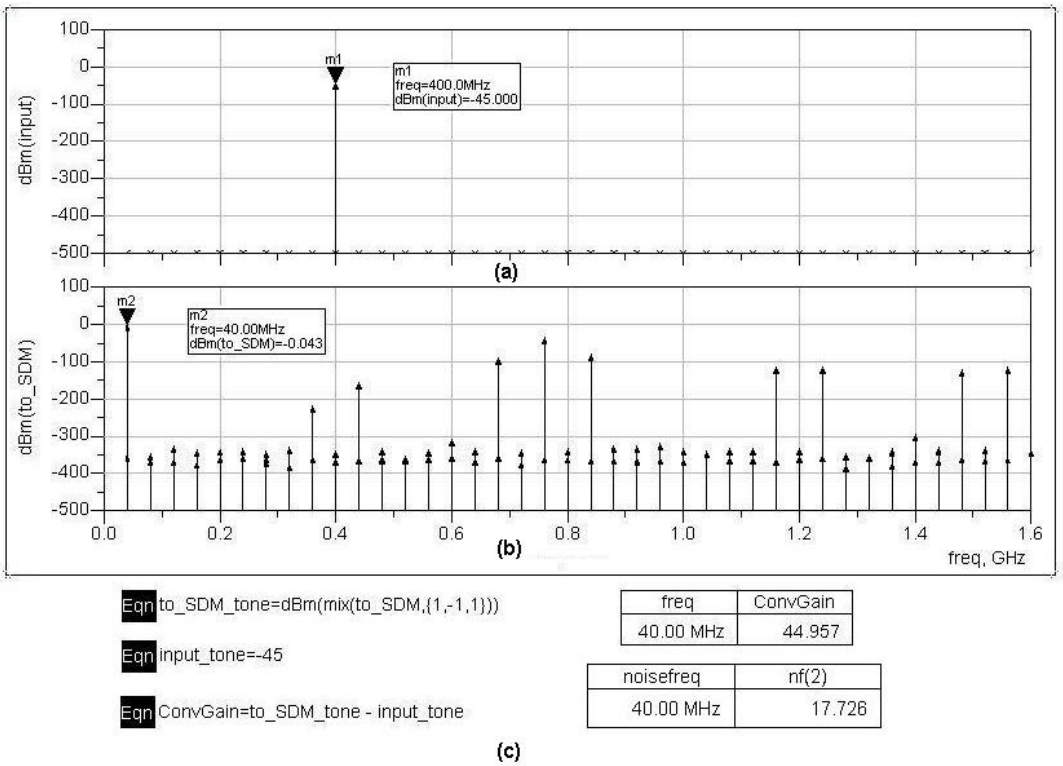


Figure 5.12: Front-end's input (a) and output (b) spectrum, conversion gain and noise figure (c) results at 40MHz.

5.4.3 Intermodulation test

The two-tone intermodulation test is used to characterize the system linearity. The simulation setup is similar to the one in Figure 5.8, except now two equal tones at 390MHz and 410MHz are applied at the input port (as the two-tone intermodulation test described in Chapter 2). Nonlinearities in the system will generate third-order intermodulation distortion, and the input-referred third-order intercept point (IIP3) is a measure of how much distortion is generated.

Figure 5.13 shows the output spectrum with intermodulation distortion products near the the 40MHz frequency. The output-referred third-order intercept point (OIP3) is then calculated, using the display marker readouts, as half the difference between the magnitudes of the fundamentals and the IM3 products at the output plus the corresponding input level. The IIP3 is just the OIP3 minus the conversion gain. The IIP3 also is calculated using a built-in function, *ip3_in*, showing the same results.

Thus, the OIP3 is 17.55dBm and the IIP3 is -27.44dBm.

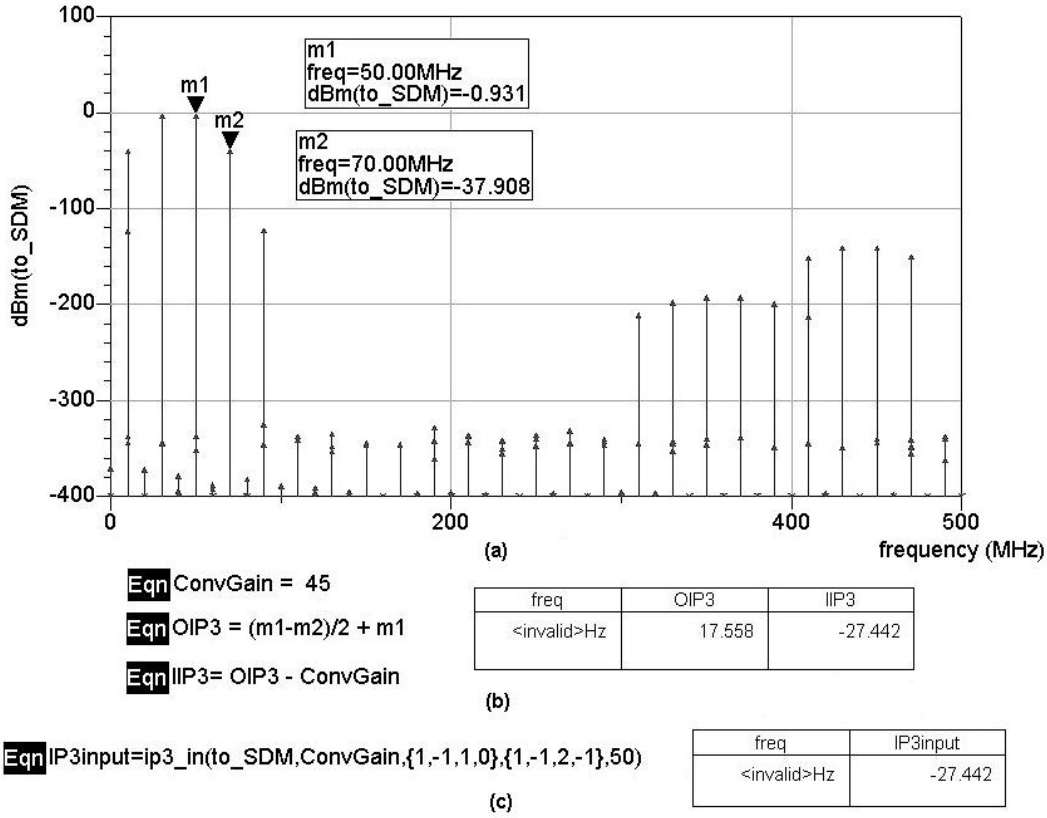


Figure 5.13: Two-tone intermodulation simulation results: (a) output spectrum, (b) OIP3 and IIP3 calculations based on simple geometry, (c) IIP3 calculation using a built-in *Agilent ADS* function.

5.4.4 Adjacent channel test

In these simulations, in addition to the desired input signal, another signal is applied to the front-end at a specified adjacent frequency. These simulations are used to emulate the image and half-IF affects previous described in section 5.1. Each simulation test is described as follows.

5.4.4.1 Image problem

In order to emulate this effect, both a desired signal at 400MHz and an image signal at 480MHz are applied to the front-end's input. In a heterodyne single-IF down-conversion architecture, for an intermediate frequency of 40MHz and a LO signal of 440MHz, both the desired and image signals would be translated to the same frequency of 40MHz.

Figure 5.14 illustrate the overall performance of the entire system for this test. Both input signals of -45dBm at 400MHz and 480MHz are applied to the front-end (Figure 5.14a). At the system output, the signals are then down-converted around 40MHz (Figure 5.14b) and its gain is adjusted such that the signal level at the output is around 0dBm.

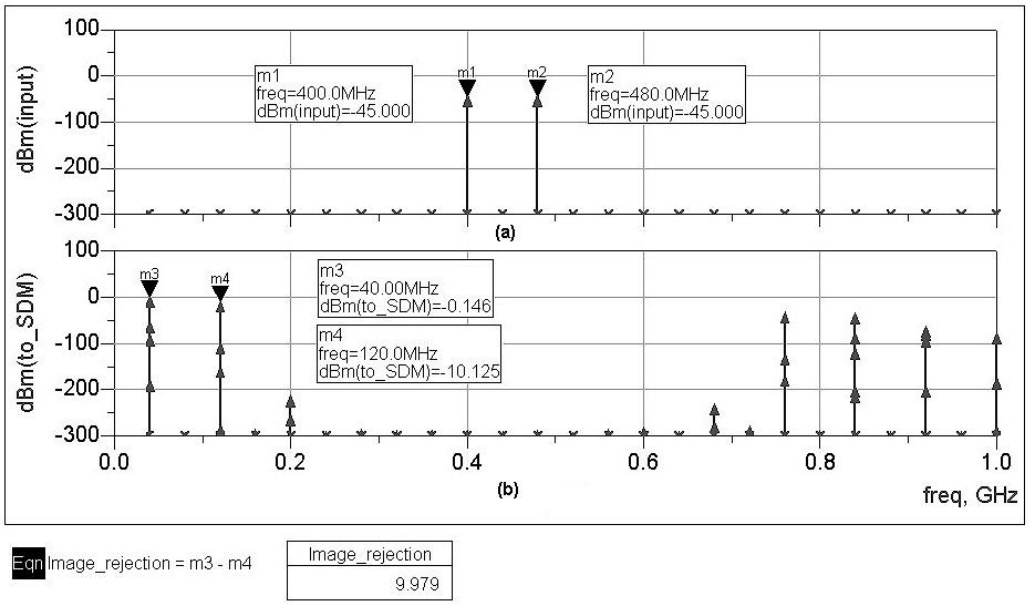


Figure 5.14: Image problem simulation.

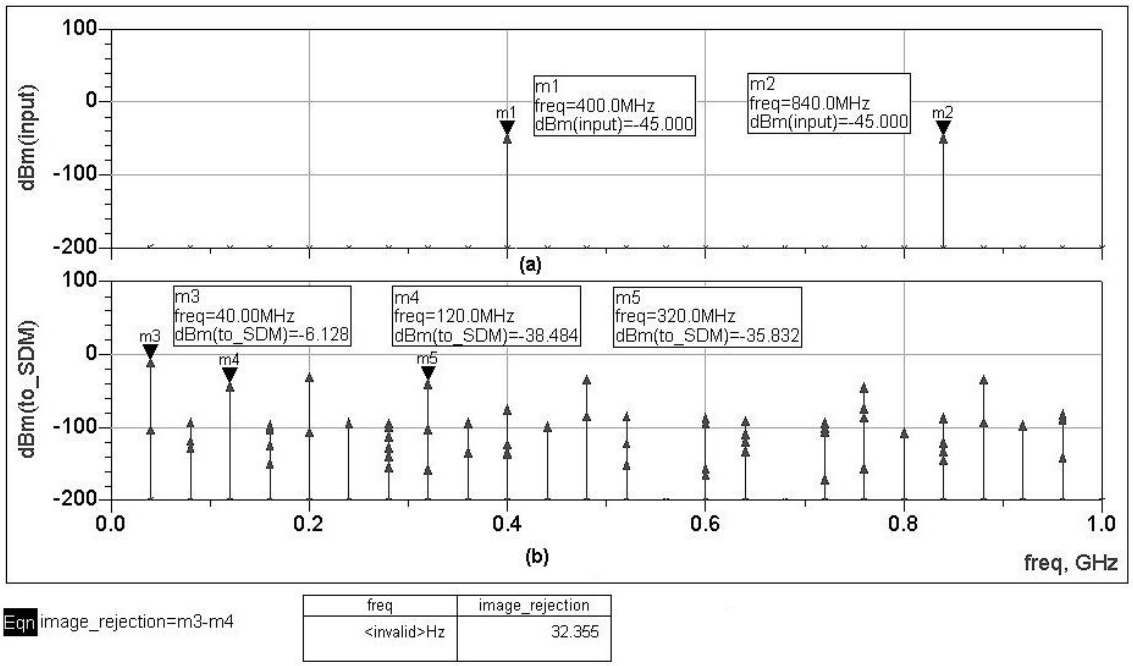
From the final output signal showed in Figure 5.14b, it can be notice that while the desired input signal is translated to 40MHz (*fp1)*, the image signal is translated to 120 MHz, eliminating the image problem. The system provides an image rejection of 9.9dB.

5.4.4.2 Interferer and LO harmonics

We now consider that in addition to the desired signal at *Fin*, an interferer at $(Fin + F_{LO})$ is applied to the front-end. If the LO contains a significant second harmonic, then the output will exhibit a component at $|(Fin + F_{LO}) - 2F_{LO}| = F_{IF}$, i.e., both the desired and interferer signals would be translated to the same intermediate frequency.

In order to emulate this effect, both a desired signal at 400MHz and an interferer signal at 840MHz are applied to the front-end's input. In a heterodyne single-IF down-conversion architecture, for an intermediate frequency at 40MHz and a LO signal at 440MHz, and considering a LO second harmonic component at 880MHz, both the desired and interferer signals would be translated to 40MHz.

Figure 5.15 illustrate the overall performance of the entire system for this test. Both input signals of -80dBm at 400MHz and 840MHz are applied to the front-end (Figure 5.15a). Both LO input signals, including both second harmonics components, are also applied to the front-end. At the system output, the signals are then down-converted around 40MHz (Figure 5.15b) and its gain is adjusted such that the signal level at the output is around 0dBm.



Eqn image_rejection=m3-m4

freq	image_rejection
<invalid>Hz	32.355

Figure 5.15: Interferer and LO harmonics effects simulation.

From the output signal showed in Figure 5.15b, it can be notice that while the desired input signal is translated to 40MHz (*fp2)*, the interferer signals are translated to 120MHz and 320MHz due to the mixing with both LO harmonics. The system provides an image rejection of 32.2dB.

5.5 Discussion

This chapter discussed the RF section of the FAC, more specific, the integration of the IF front-end stage, which is critical to the system performance.

In this context, we analyzed heterodyne and homodyne receiver architectures, looking for the best front-end architecture choice suitable for our application: a dual-conversion heterodyne architecture, composed by two mixers, a LC tank and a variable gain amplifier (VGA). We then discussed the main system level design issues, determining the optimal specifications for the system and for each building block of the front-end. Finally, the front-end overall system performance was verified by system simulations using the *Agilent ADS* tool, proving the architecture choice.

Thus, the next step must be analysis of the best CMOS architecture for the building blocks that composes front-end: mixer and VGA.

6 ANALYSIS OF THE FRONT-END BULDING BLOCKS

In this chapter, we review and discuss the most significant characteristics and topologies of the building blocks that composes the chosen dual-conversion superheterodyne front-end: the mixer and VGA blocks.

Finally, the chosen architecture for each building block of the front-end is presented, aiming the best performance in our target application.

6.1 Mixers

Mixers play an important role in communications systems. A mixer is used to translate an incoming RF signal to a higher/lower frequency, called intermediate frequency (IF), in order to transmit/receive a signal (LEE, 1998) (SANCHEZ, 2004).

A mixer block has two different inputs, called the RF port and the LO port. The RF port senses the signal to be translated (down-conversion or up-conversion) and the LO port senses the periodic waveform generated by the local oscillator. This can be seen in the simple representation of Figure 6.1.

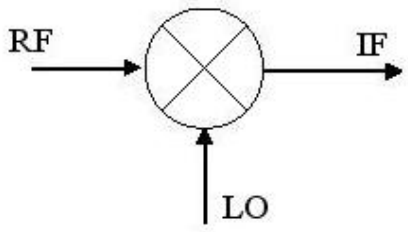


Figure 6.1: Mixer block representation.

Since linear, time-invariant systems cannot produce outputs with spectral components not present at the input, mixers must be either nonlinear or time-varying elements in order to provide frequency translation. Virtually any nonlinear element can be used as a mixer.

6.1.1 Mixer fundamentals

At the core of all mixers is the multiplication of two signals in the time domain. The fundamental of multiplication can be understood from the examination of the following trigonometric identity:

$$\left(A_1 \cdot \cos\omega_1 t\right) \cdot \left(A_2 \cdot \cos\omega_2 t\right) = \frac{A_1 \cdot A_2}{2}\left[\cos(\omega_1 - \omega_2)t + \cos(\omega_1 + \omega_2)t\right] \tag{6.1}$$

The multiplication results in output signals at the sum and difference of the frequencies of the input signal, whose amplitudes are proportional to the product of the input signals amplitudes. For down-conversion mixers, the component $\omega_1 + \omega_2$ is filtered out, and for up-conversion mixers the component $\omega_1 - \omega_2$ is filtered out.

Having revised the fundamental role of multiplication, the most significant characteristics of mixer are briefly discussed in the next subsections.

6.1.1.1 Conversion gain

One important characteristic of mixer is the *conversion gain* (or loss). It is defined as the ratio of the desired IF output to the value of the RF input. For the multiplier described in equation 6.1, the conversion gain is the IF output ($\left(A_1 \cdot A_2\right)/2$) divided by A_1. Therefore, the conversion gain in this case is $A_2/2$, or half of the LO amplitude. The conversion gain may be measured as voltage or power gain.

6.1.1.2 Noise figure

Noise figure is simply defined as the signal-to-noise ratio (SNR) at the input (RF) port divided by the SNR at the output (IF) port.

It is important to mention that in a typical mixer, there are two input frequencies that will generate a given output IF: the desired RF signal, and the image signal. These two signals are often referred as *sidebands*. The existence of this image frequency can complicate the noise figure computations because the noise originating in both the desired and image frequencies becomes IF noise, even though there is no desired signal at the image frequency. When the desired signal exists at only one frequency, the measured noise figure is called single-sideband noise figure (Figure 6.2a); in rare cases, when both the RF and image signals contain useful information, the measured noise figure is called double-sideband (Figure 6.2b).

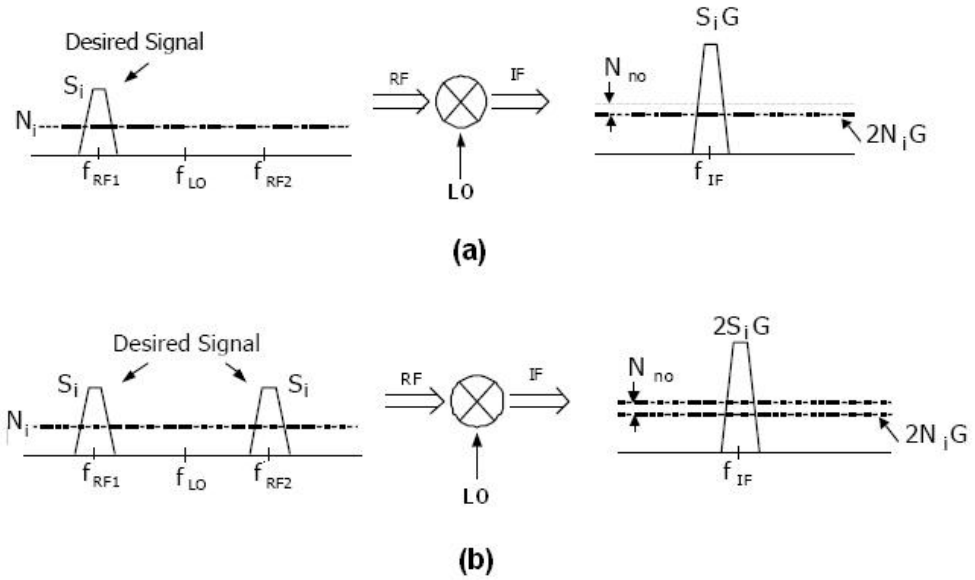


Figure 6.2: Input signals and noise computations for (a) single-sideband – SSB and (b) double-sideband – DSB signals.

6.1.1.3 Linearity

As amplifiers, real mixers are nonlinear systems. The linearity of mixers is characterized by the 1dB compression point (P_{1dB}) and the third-order intercept point ($IIP3$), both parameters previously described in Chapter 2.

The two-tone intermodulation test is usually used to characterize mixer linearity: it mimics the real world scenario in which both the desired signal and a potential interferer feed a mixer input. Thus, the output of the mixer will contain frequency-translated versions of third-order IM components whose frequency are at $2\omega_1 \pm \omega_2$ and $2\omega_2 \pm \omega_1$.

6.1.1.4 Isolation

Another parameter of great practical importance is the isolation. It informs about the leakage of either the LO signal to input and output ports. Thus, it is desirable to minimize interaction among the IF, RF and LO ports. For instance, any LO feedthrough to the output can cause problems at subsequent stages.

The required isolation levels depend on the environment in which the mixer will be used. If the isolation provided by the mixer is inadequate, the preceding or following blocks may be modified to fix the problem (LEE, 1998) (SANCHEZ, 2004).

6.1.2 Mixer topologies

As mentioned before, mixers use multiplication to achieve frequency translation. Multiplication can be implemented either directly, using a multiplier circuit, or indirectly, using a nonlinear circuit.

Nonlinear circuits provide multiplication due to the multiplications they provide incidentally, usually due to second-order nonlinearities (LEE, 1998). Precisely due to this incidental multiplication, these nonlinearities usually generate undesired spectral components, in addition to isolation problems.

Mixers based directly on multiplication generally exhibit superior performance because they ideally generate only the desired intermodulation product and provide a high degree of isolation among all three signals. These types of mixers can be classified as single-balanced and double-balanced mixers.

A single-balanced mixer converts the incoming input signal voltage into current and then performs a multiplication in current domain, exhibiting less input-referred noise for a given power dissipation, however it is more susceptible to noise in the LO signal. In double-balanced mixers, the same V-I converter principle is used, but now two single-balanced circuits are combined to produce the multiplication, providing better port-to-port isolation. For both topologies the output can be sensed as either a differential or single-ended signal.

Considering that the scope of this work is the system integration in CMOS technology, we now revise and discuss some passive and active mixer CMOS architectures.

6.1.2.1 Passive mixers

Passive mixers have some attractive properties, such as low power consumption and superior linearity compared to active mixers. Considering that CMOS technology offers excellent switches, multiplier-based mixers using switching can be easily implemented in this technology.

A simple differential single-balanced passive mixer is shown in Figure 6.3a. The two MOS switches are driven by complementary phases of the LO. If the swing of the LO is large so that the gate-to-source overdrive is large enough, the channel on-resistance is almost independent of the RF voltage, implementing a linear mixer (in case of low voltage applications, where LO swing is small, the linearity is degraded).

The same idea is used to implement a differential double-balanced passive mixer, shown in Figure 6.3b. In each LO phase only two switches are "on" in opposite branches, creating a balanced output. The voltage conversion gain of both basic implementations is $2/\pi$ (around -4dB).

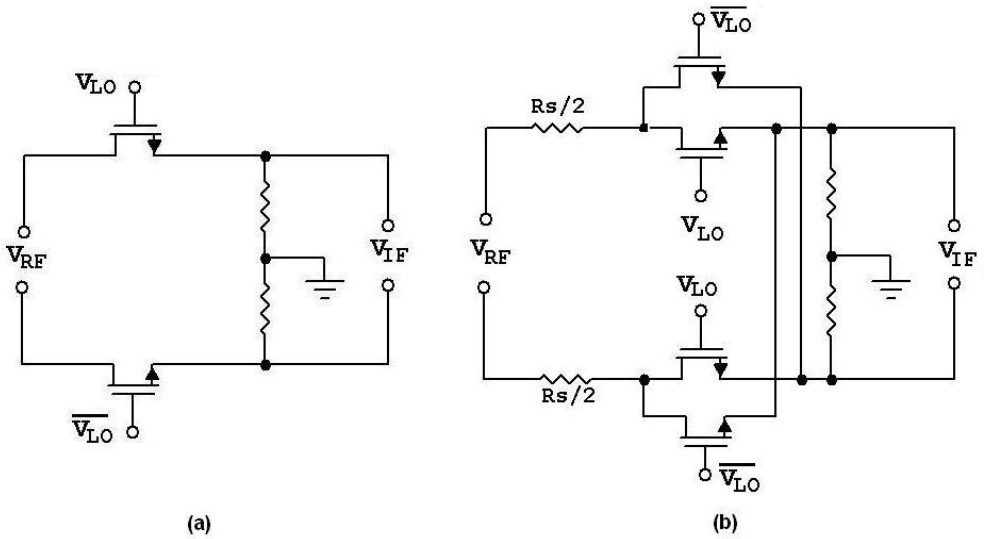


Figure 6.3: Passive CMOS differential mixer: (a) single-balanced, (b) double-balanced.

These topologies suffer from a number of severe drawbacks. First, the conversion gain is less than one, which can increase the noise of the stage following the mixer when referred to the RF input. For sinusoidal LO signals, the gain is even lower because the switches are simultaneously "on" for a considerable time. Second, both NF and IP3 are strongly dependent on the LO input, since the resistance switches in the "on" state must be kept low and constant to optimize both parameters. This leads to large transistors, increasing the parasitic capacitances, which has impact on power consumption, frequency coverage and noise injection (LEE, 1998).

Considering the case of CMOS mixers, where the load is typically capacitive, the modified topology, showed in Figure 6.4, provides better performance. The input network consists of an L-match in cascade with a parallel tank, providing an impedance transformation that boosts the input RF signal voltage to help reduce the voltage conversion loss. The parallel tank filters out the out-of-band noise and unwanted tones.

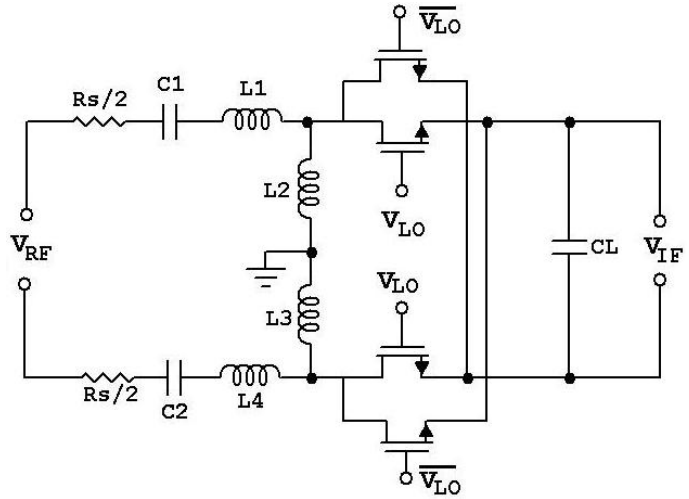


Figure 6.4: Low-noise, narrowband double-balanced CMOS passive mixer.

There are various reports of CMOS passives mixer implementations (RAZAVI, 1998) (SANCHEZ, 2004), with the same basic core described here, showing excellent results in linearity, noise figure and power consumption. However, one of the major problems of this topology is that the conversion gain, linearity performance and noise figure are strongly dependent on the power supply, process and temperature variations.

6.1.2.2 Active Mixers

Active mixes, in contrast to passive mixers, provide gain and reduce the noise contributed by subsequent stages. The basic principle of this implementation can be illustrated by the simple unbalanced mixer shown in Figure 6.5, where the RF signal is converted to a current signal using a transconductance. This current is switched to the IF port via a switch-wave signal. The output IF current is switching between I_{RF} and zero at the LO frequency. Therefore, it can be expressed, assuming 50% duty cycle, as

$$I_{IF} = \left(I_{Bias} + gm \cdot v_{RF}\right) \cdot \left(0.5 + \frac{2}{\pi} \cdot \cos \omega_{LO} t + \frac{2}{3\pi} \cdot \cos 3\omega_{LO} t + \frac{2}{5\pi} \cdot \cos 5\omega_{LO} t + \ldots\right) \quad (6.2)$$

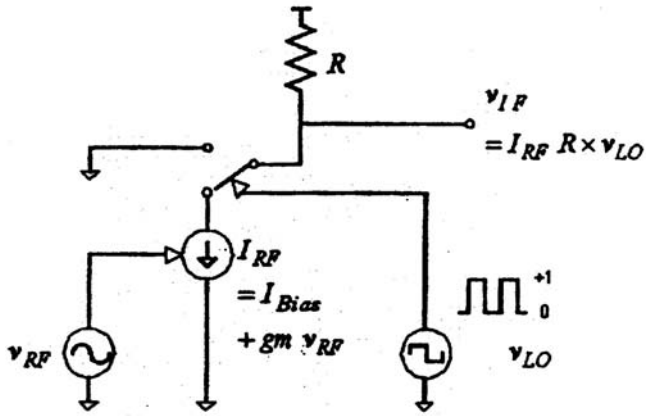


Figure 6.5: Low-noise, narrowband double-balanced CMOS passive mixer.

Assuming that $v_{RF} = V_{RF} \cos \omega_{RF} t$, the current at the output becomes

$$I_{IF} = \frac{I_{Bias}}{2} \cdot \left(1 + \frac{4}{\pi} \cdot \cos\omega_{LO} t + \frac{4}{3\pi} \cdot \cos 3\omega_{LO} t + \frac{4}{5\pi} \cdot \cos 5\omega_{LO} t + \ldots\right) + \frac{gm}{2} \cdot V_{RF} \cos\omega_{RF} t$$

$$+ gm \cdot V_{RF} \left[\begin{array}{l} \frac{1}{\pi}\cos(\omega_{LO} - \omega_{RF})t + \frac{1}{\pi}\cos(\omega_{LO} + \omega_{RF})t + \frac{1}{3\pi}\cos(3\omega_{LO} - \omega_{RF})t \\ + \frac{1}{3\pi}\cos(3\omega_{LO} + \omega_{RF})t + \frac{1}{5\pi}\cos(5\omega_{LO} - \omega_{RF})t + \frac{1}{5\pi}\cos(5\omega_{LO} + \omega_{RF})t + \ldots \end{array}\right] \quad (6.3)$$

The output thus consists of sum and difference components, including components at DC and harmonics of the LO mixing with the RF input signal. The conversion transconductance gain is $Gc = gm / \pi$.

The same basic principle can be applied in the implementation of active single-balanced and double-balanced mixers. In single-balanced implementations (Figure 6.6a), the IF current is switching between $\pm I_{RF}$ at the LO frequency, so the average is zero, which doubles the amplitude of the spectral components of the square wave.

This implementation can be improved with the use of two balanced circuits to implement a double-balanced mixer, as shown in Figure 6.6b. The current at the IF port switches between $\pm gm \cdot v_{RF}$. This configuration cancels out the DC component (since it flows through both load resistors at all times) and the spectral components at $n \cdot \omega_{LO}$, reducing the feedthrough between the input ports. The conversion transconductance gain is equal to $Gc = 2gm / \pi$.

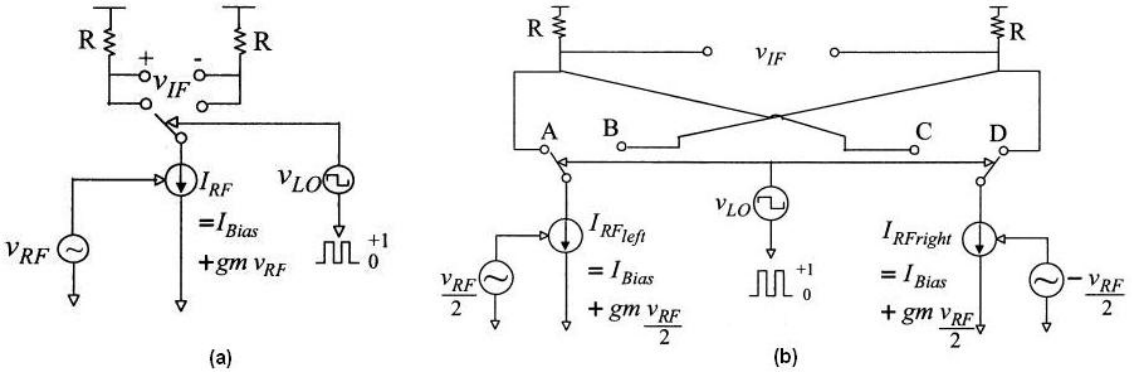


Figure 6.6: Active mixers: (a) single-balanced, (b) double-balanced.

The most straightforward way to implement a single-balanced mixer in CMOS process is to use a current-mode stage (differential-pairs), as showed in Figure 6.7. As we have seen before, the conversion transconductance and, hence, the conversion gain, depends on the device transcondutance of the MOS transistor used to convert the RF voltage signal to a current signal. The double-balanced version takes the form of a Gilbert Cell, and will be discussed in the next section.

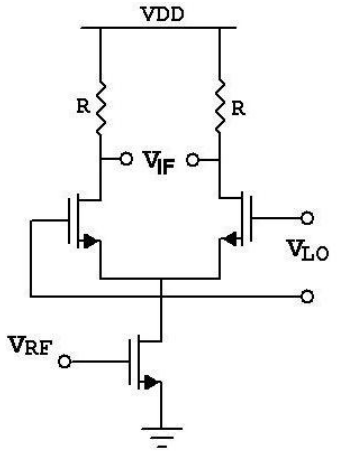


Figure 6.7: CMOS active single-balanced mixer.

Most of the design effort in this type of implementation is spent attempting better ways to improve the linearity and noise of the basic V-I conversion stage.

6.1.3 The Gilbert Cell based mixer

The double-balanced mixer based on the Gilbert Cell topology (GILBERT, 1968) proves to be the most useful multiplier topology to be used as mixers nowadays. It demonstrates excellent performance as both up-converter and down-converter, broadband properties, and it is suitable for integrated circuit applications (SULLIVAN, 1997) (LEE, 1998) (DARABI, 2001) (HARVEY, 2001).

The operation of the Gilbert Cell can be viewed as the operation of the transconductor blocks shown in Figure 6.8. The basic idea is to have $Gm1$ that is a

function of $Gm2$ and the operation of the transconductor internally produces the multiplication component. Using the differential nature, the undesired components can be eliminated.

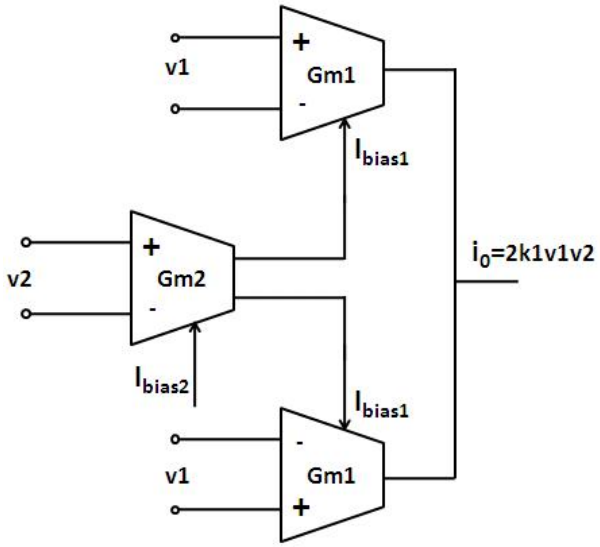


Figure 6.8: Block diagram for multiplication – Gilbert Cell based topology.

6.1.3.1 Basic topology

Figure 6.9 shows the CMOS implementation of the Gilbert Cell, where two single-balance circuits combine to produce a double-balanced mixer. The input differential pair (M1/M2) is connected to V_{RF} and the overall operation of the two cross-coupled cascode differential pairs depends on the output current due to the V_{RF} and being a function of the V_{LO}. The upper cross-coupled transistors are connected antiparallel so that the LO components sum up to cancel each other. The produced IF component will not be cancelled but doubled at the output.

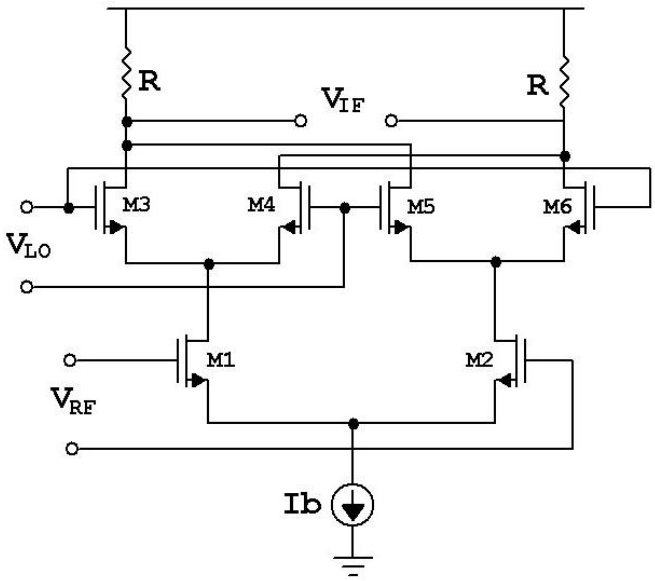


Figure 6.9: Double-balanced Gilbert Cell mixer.

In a Gilbert Cell multiplier, the idea is to have a linear gain by using the input port of one differential pair as the control and the others as the input pairs connected in opposite polarities or vice versa. Since the small signal current flowing on the input differential pair in a Gilbert Cell is the function of the cross-coupled differential pairs, we obtain a multiplication component of the two inputs.

Thus, we can design the LO differential pairs to act like switches. Their operation can be viewed as a square pulse for:

$$V_{LO}(t) > \left|V_{LOthrehold}\right| \tag{6.4}$$

From this assumption, an approximation can be done by assuming the operation of V_{LO} as a square signal, as shown in Figure 6.10.

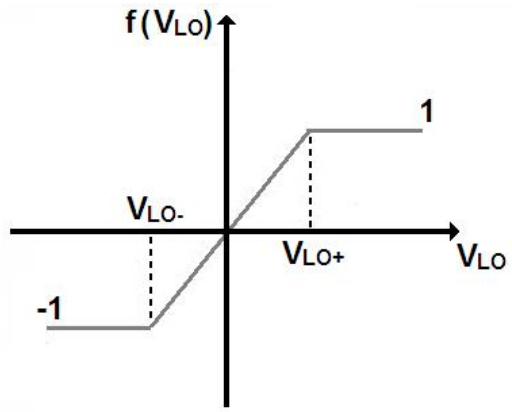


Figure 6.10: V_{LO} behavior as a square function.

Therefore, we can write the output current of the mixer to be

$$I_{IF}(t) = V_{RF}(t) \cdot K \cdot f\left(V_{LO}(t)\right) \tag{6.5}$$

The conversion gain of the Gilbert Cell can be analyzed in two stages, for the case where $V_{LO}(t) > \left|V_{LOthreshold}\right|$ and the LO transistors operate as switches and the case where LO transistors are both *on* and in the linear region of their operating function.

It is assumed that the transition phase of the switch is very small, which is reasonable in the case of hard switching in the LO. When the LO transistors act like switches we have:

$$\begin{aligned} I_{IF}(t) &= gm \cdot A_{RF} \cdot \cos(\omega_{RF} t) \cdot \left[\frac{4}{\pi} \cdot \sum_{n=1,3,5\ldots}^{\infty} \sin(n \cdot \omega_o t)\right] = \\ & gm \cdot A_{RF} \cdot \cos(\omega_{RF} t) \cdot \left[\frac{4}{\pi} \cdot \sin \omega_o t + \frac{4}{3\pi} \cdot \sin 3\omega_o t + \frac{4}{5\pi} \cdot \sin 5\omega_o t + \ldots\right] \end{aligned} \tag{6.6}$$

If we take the multiplication of LO and RF components into consideration and assume that unwanted terms are eliminated (filtered) by a following stage, we will have

$$K = \frac{2 \cdot gm \cdot A_{IF}}{\pi} \tag{6.7}$$

The conversion gain will then be:

$$G_C = \frac{2 \cdot gm}{\pi} \tag{6.8}$$

The noise figure of this topology will be mainly dominated by the input RF transistors. The worst case for the noise figure will be when the LO transistors are in their linear region where they both conduct current. In this particular case the switching noise will be added to the overall noise and degrade it. Thus, the best option is to have the switching as fast as possible so that these transistors are either on or off. Then, since LO transistors are in cascade configuration, we can consider the overall noise to be dominated by RF transistors only (LEE, 1998).

Another point in the analysis of noise figure is that the output current is reflected to input as input voltage noise when it is divided by gain. Then, for small conversion gain, the transistors noise has larger effect, which is not desirable. Thus, we find that all the noisy components including the resistive load have a significant noise contribution at the RF input port. Then, for a better NF performance we would like to keep the LO switching as fast as possible and also the conversion gain large. Finally, the 3 dB loss due to neglecting the effect of single sideband signal will be there, which is unalterable.

The *IIP3* of the system will be affected mainly by the linearity of the RF transconductor if the switches are designed well. The LO drive of the switches should be optimized such that it is high to keep the switching accurate and also it should not be too high to prevent the parasitic capacitances and their degradation on high frequency operation. To improve the linearity of the RF transconductor, source degeneration can be used.

6.1.4 Linearization techniques

Since in our application the input signal varies in amplitude and frequency in a wide range, the linearity of the mixers stages (mainly the first up-conversion stage) must be optimized.

In current-mode mixers, the linearity is controlled primary by the quality of the transconductance, thus, is straightforward the use of linearization techniques used in transconductance amplifiers (RAZAVI, 2002).

We now revise the main linearization techniques used in Gilbert Cell based mixers reported in the literature (LEE, 1998) (SANCHEZ, 2000) (SANCHEZ, 2004).

6.1.4.1 Source degeneration

The simplest linearization method is called source degeneration, by means of a linear resistor. This method reduces the signal swing applied between the gate and the source of the transistor, making the input/output characteristic more linear.

An input differential pair can be degenerated as shown in Figures 6.11a and 6.11b. From the expression of the output current related to the input voltage, and neglecting the body effect, the overall transconductance gain of the stage can be approximated as follows:

$$G_m = \frac{gm}{1 + gm \cdot R} \tag{6.9}$$

which for large $gm \cdot R$ approaches $1/R$, an input independent value.

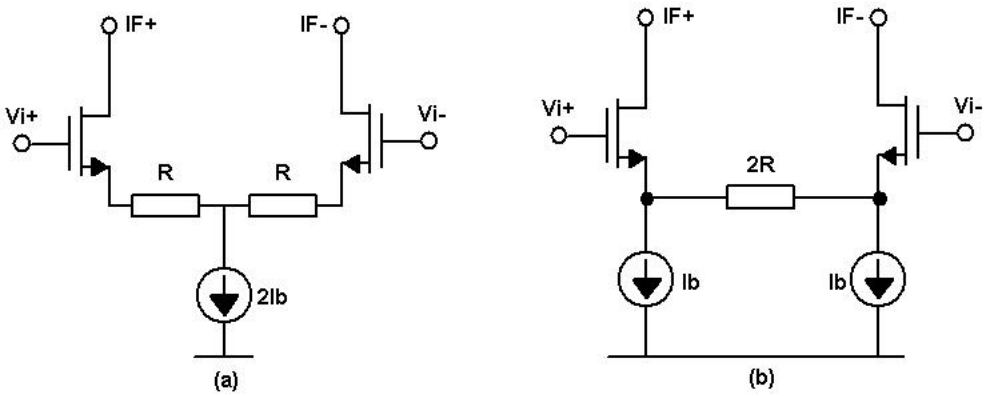


Figure 6.11: Source degeneration applied to a differential pair.

Although both topologies realize the same transconductance, they have different properties. In the topology of Figure 6.11a, the current bias flows through both resistors, thereby reducing the common-mode swing of the input signals, which is particularly critical to low voltage applications. On the other hand, the topology of Figure 6.11b does not involve this issue but it suffers from a higher noise (and offset voltage) because the noises of each current sink.

Resistive degeneration requires high-quality resistors, which are usually difficult to implement in CMOS technology. As shown in Figure 6.12a, the resistor can be replaced by a MOS transistor operating in the linear region controlled by a bias voltage. Figure 6.12b illustrates the use of two MOS transistors operating in the linear region, where the circuit remains relatively linear if one degeneration device goes into saturation.

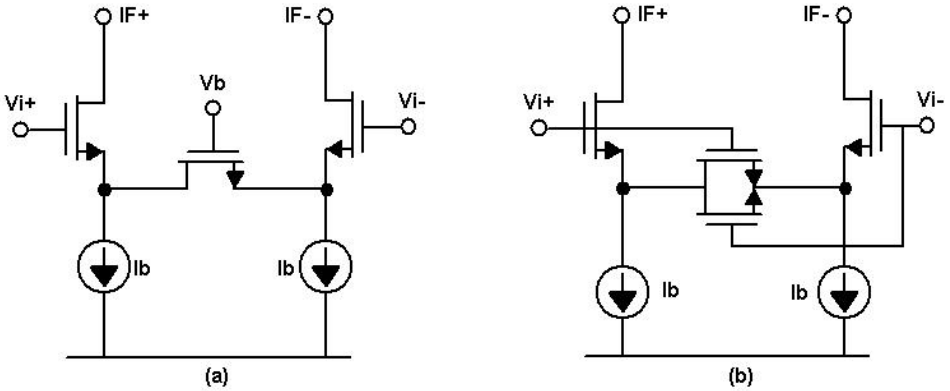


Figure 6.12: Differential pair degenerated by (a) a MOS transistor operating in linear region; (b) two MOS transistors operation in the linear region.

In some cases, inductive degeneration is preferred over resistive degeneration due to better inductance properties, such as the absence of thermal noise and DC voltage drop (LEE, 1998).

6.1.4.2 The multi-tanh technique

This technique was first introduced by (GILBERT, 1998), where a class of linear transcondutance cells characterized by the use of parallel or series connected sets of bipolar differential pairs were analyzed and implemented. The name "multi-tanh" derives the fact that the transfer characteristic of a bipolar differential pair is a hyperbolic tangent. Bipolar multi-tanh cells has been used as a linearization method in amplifiers, mixers, continuous-time tunable filters, voltage controlled oscillators (VCOs), and miscellaneous nonlinear applications (GILBERT, 1998) (LEE, 1998).

The extension to MOS implementations operating in the weak inversion is straightforward. The voltage capacity of a transconductance cell (basically a simple MOS differential pair) is extended by using at least two, in general *N*, differential pairs operating in parallel. A deliberate input offset voltage is applied to the input of each pair, which splits the individual transconductance functions along the input voltage axis. This allows the cell to handle larger voltage swings at its input, while the overall transconductance is more linear, providing a low distortion function. Since each pair is responsible for only a fraction of the total linear range, it can be designed to provide a larger transconductance.

There are several ways in which the necessary offset voltage can be introduced. For low-order cells (N=2 doublet and N=3 triplet, as shown in Figure 6.13) it can be generated simply by using mismatched transistor aspect ratios (while this mismatched may be achieved by scaling either width or length of the input pair, in practice both transistors have identical gate lengths to improve device matching). For large values of *N*, in bipolar technology, the offset may be introduced using bias currents operating on chains of resistors (GILBERT, 1998).

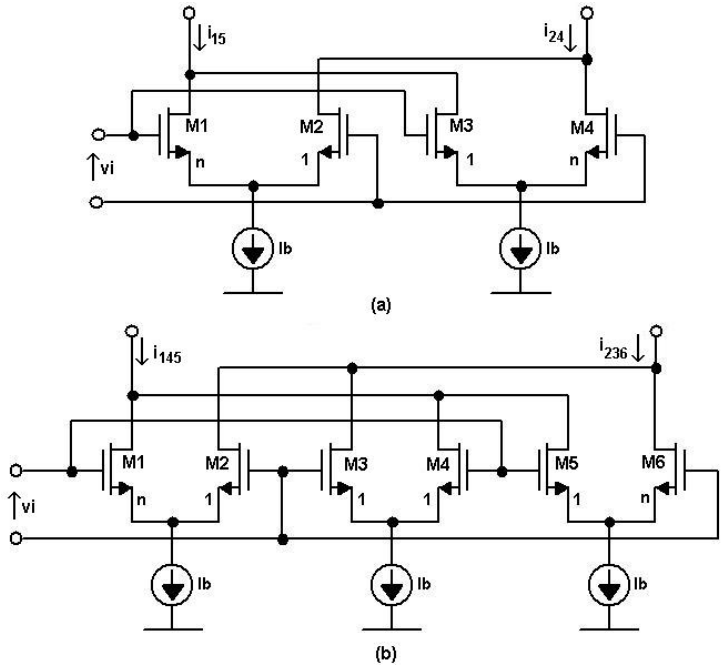


Figure 6.13: Basic MOS multi-tanh cell: (a) doublet; (b) triplet.

There are a few reported papers that directly use the square-law properties of MOS transistors for similar purpose. In (RYAN, 2004) and (WANG, 1990), linear input transconductors are realize, where the offset voltage is generated by a proper bias network that provides decibel-linear control and temperature stabilization of the circuit gain over a wide dynamic range. Mixers implementations using this technique are usually implemented in bipolar technology, as in (CARRARA, 2005) (SCHERIER, 2002) and (WANG, 1991).

6.1.4.3 Additional techniques

Depending on the application, additional ways to extend linearity in active mixers are used, usually attempting to find better ways of providing the V-I conversion (LEE, 1998).

In low-voltage applications, the DC current source can be replaced by a parallel LC tank in order to create a zero-headroom AC current source, providing rejection of whatever common-mode component at the resonant frequency. In such cases, inductive degeneration is preferred over resistive degeneration, due to the absence of thermal noise and DC voltage drop. Another technique used to improve the linearity in active mixers is the use some kind of feedback or feedfoward in the input transconductor stage of the mixer, cancelling the errors that distortion represents (LEE, 1998).

6.1.5 Multi-band Gilbert Cell mixer implementations

The natural place to look for an architecture solution for the mixer stages should be among receivers systems that target different cellular standards, the so-called multi-mode receivers, where RF input signal varies in amplitude, frequency and bandwidth. In this context, the Gilbert Cell topology proves to be the multiplier topology mostly used in such applications, where its input stage is optimized for best linearity performance, since the input signal varies in amplitude and frequency in a wide range.

In (ADISENO, 2002), (HENG, 2005) and (SCHEIRER, 2002), a variation of the multi-tanh linearization technique is used in order to linearize the input transconductor stage. An additional bias network circuitry provides some gain control and temperature stabilization of the circuit gain over a wide dynamic range.

In (ROSSI, 2005) and (RYYNÄNEN, 2001), an addition stage is implemented using a current boosting stage in the output load. The boosting enables the utilization of higher mixer conversion gain by allowing the resistive loading in the mixer output. The load is implemented as MOS transistors pairs between the mixer output terminals, which can provide an adjustable conversion gain.

Mostly of these topologies are implemented in BiCMOS technology with some additional stage or off-chip component, for high linearity performance, providing a low range of gain control with reasonable noise performance. Table 6.1 summarizes the main published multi-band Gilbert Cell mixer topologies.

Table 6.1: Review on Multi-band Gilbert Cell mixer implementations

Author	Technology	*Topology & features*	Operating frequencies *(Hz)*		*Gain (dB)*	IIP3 *(dBm)*	*Application*
			Input (RF)	*Output (IF)*			
(ADISENO, 2002)	RF Si-bipolar process	Voltage controlled linear input differential pair Bias offset technique	800M - 2.4G	5M	20 (LNA+ mixer)	-3 (LNA+ mixer)	Multi-band multi-standard low-IF receiver
(HENG, 2005)	0.25µm CMOS process	I/Q mixer with input devices biased with a large V_{GS} for high linearity	48M - 860M	1G / 1.75M	-15 to 25 (LNA+ mixer)	+8 (LNA+ mixer)	TV tuner
(ROSSI, 2005)	0.25µm SiGe BiCMOS process	Variable gain Gilbert cell with inductive degeneration and load boosting	5 - 6G	12M	-2.5 to 8.5	+17	Variable gain front-end (LNA+mixer) for multi-standard applications (WLAN)
(RYYNÄNEN, 2001)	0.35µm BiCMOS process	Gilbert cell with current boosting	880M - 1.98G	300M / 400M	4 -15	+8	WCDMA/GSM receiver
(SCHREIER, 2002)	0.35µm BiCMOS process	Gilbert cell with bipolar input multi-tanh V-I converter and an off-chip LC tank	10-300M	1-4MHz	15 (LNA+ mixer)	-1 (Backend)	Backend (LNA, Mixer and ΣΔ Modulator) of a dual-conversion receiver for FM and GSM

6.2 Variable gain amplifiers

Variable gain amplifiers (VGA) are widely used in telecommunication systems. They play the important role of stabilizing the amplitude of signal of interest under various conditions, providing constant-amplitude signal to the baseband section of a receiver.

There are two basic ways to realize VGAs depending on whether the control signal is digital or analog (SANCHEZ-SINENCIO, 2004). The digitally controlled VGAs (Figure 6.14a) use a series of resistors or switched capacitors techniques in order to control the gain, which can lead to discontinuous signal phases in the output since the gain varies as a discrete function of the control signal (a larger number of control bits are necessary to avoid this problem).

On the other hand, VGAs controlled by analog signals typically adopt variable transconductance or variable loads (of resistance stages) for gain variation, as shown in Figure 6.14b. In these topologies, the gain can be controlled continuously, however obtaining a wide range of gain variation as a function of the control voltage is a big issue, especially in CMOS technology.

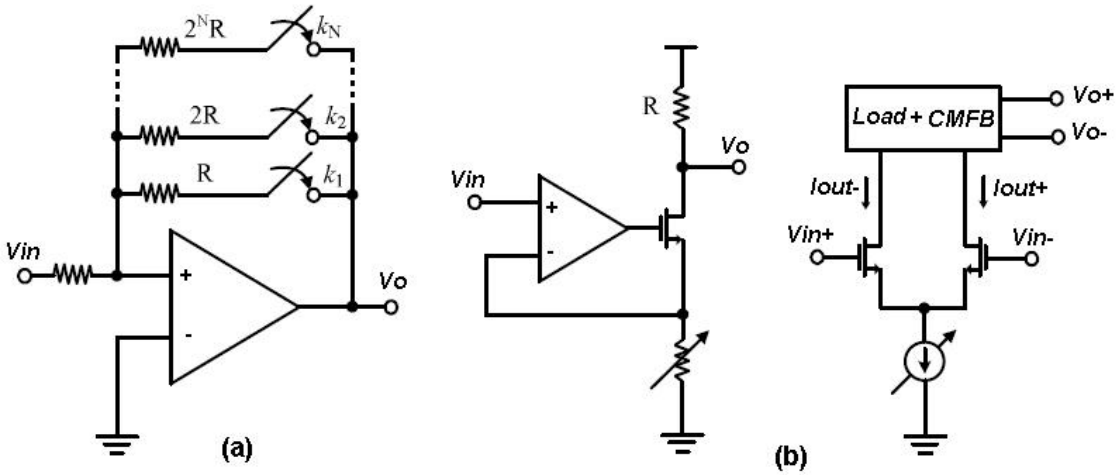


Figure 6.14: Basic realization of VGAs: (a) digital-controlled and (b) analog-controlled.

6.2.1 VGA fundamentals

Considering the fundamental role of the VGA block in receivers systems, the most significant characteristics and features of this block are briefly discussed in the next subsections.

6.2.1.1 Gain and bandwidth

Usually the basic stage of a VGA is a simple differential amplifier where the gain is directly proportional and the -3dB bandwidth is inversely proportional to its output resistance, leading to a tradeoff between the maximum gain that can be achieved and the speed of the amplifier. Cascode structures and diode connected loads are generally used in these implementations in order to increase the gain maintaining reasonable bandwidth and power consumption.

Considering CMOS topologies, variations in the gain of a VGA can be obtained by either varying the transconductance of the MOS transistor operating in saturation or by varying the output loads (RAZAVI, 2002). Thus, to cover a wide dynamic range (typical in wireless communication receivers) CMOS-based VGAs require at least 3 or 4 gain-varying stages.

6.2.1.2 Common mode feedback (CMFB)

In high gain differential amplifiers with active current source loads, the output common mode (CM) level is quite sensitive to device properties and mismatches and it cannot be stabilized by means of a differential feedback (RAZAVI, 2002). Thus, to avoid this problem and fix the CM voltage to a certain value that maximizes the output voltage swing (ensuring that all transistors are saturated), a common mode feedback (CMFB) circuitry is used.

This circuit, with a high loop gain, introduces negative feedback and adjusts the output DC level to a specific value without regard of the changes in the input CM voltage. It also decreases the variation of the output DC voltage with temperature, supply and process.

6.2.1.3 Noise and linearity

In communications systems, noise and linearity of amplifiers are normally measured by evaluating the noise figure (NF) and the third-order intercept point (IIP3), respectively.

The noise figure is simply defined as the signal-to-noise ratio (SNR) at the input divided by the SNR at the output. The two-tone intermodulation test is usually used to characterize the amplifier linearity. Since the IIP3 varies regarding the gain of the amplifier, the output-referred third-order intercept point (OIP3) is usually used as linearity metric.

6.2.1.4 Offset cancellation

In order to prevent the VGA from being saturated due its high gain and high offset voltage, the use of an offset cancellation circuitry is indispensable. Offset cancellation techniques usually uses sampling circuits and memory components in order to sample, store and cancel the offset voltage (RAZAVI, 2002).

6.2.1.5 Automatic gain control (AGC)

In receiver systems, the VGA is usually employed in a feedback loop to implement an automatic gain control (AGC) amplifier. The AGC amplifier is a circuit that automatically controls its gain in response to the amplitude of the input signal, leading to a constant signal amplitude in the output. The gain as an exponential function of control range (which is not easily obtained in CMOS process) is desirable for minimizing the settling time of AGC loops.

6.2.2 Review on CMOS-based VGA implementations

We now review some CMOS-based VGA architecture solutions, considering receivers systems in GSM and CDMA standards. In such applications, the amplitude of the receiver and transmitter signals varies greatly. For this reason, the transceiver requires about 80dB of dynamic gain variation and splits into RF and IF/baseband stages. In a typical receiver, most of the gain variation is assigned to the baseband stage. Table 6.2 summarizes the main published CMOS-based VGA implementations in the literature, targeting different applications.

Table 6.2: Review on VGA implementations for receivers.

Author	*Technology*	*Topology & features*	*Number of stages*	*Operation frequency (MHz)*	*Gain range (dB)*	*Power consumption (mW)*	*Application*
(DUONG, 2006)	0.18µm CMOS process	Input source-coupled pair with diode-connected load and a bias circuit for temperature-independent gain	2 (plus control stage)	32 - 1050	68 to 95	6.5 (1.8V supply)	CDMA receiver
(GUO, 2000)	0.5µm CMOS process	Input differential pair with cross-coupled control transistors and offset cancellation circuitry	3	70	0 to 70	15 (2.5V supply)	GSM receiver
(ORSATTI, 2000)	0.25µm CMOS process	Differential amplifier with CMFB	3	71	10 to 90	12 (2.5V supply)	IF-Baseband strip (VGA+Mixer +IF Filter) for a GSM receiver
(XIAO, 2007)	0.18µm CMOS process	Variable *Gm* topology with gain-independent input impedance matching	5	470 - 870	-17 to 16	22 (1.8V supply)	DTV Tuner
(YMAJI, 2002)	0.25µm CMOS process	Variable *Gm* input amplifier and a transimpedance buffer	4	30 - 210	-35 to 55	27.5 (2.5V supply)	CDMA receiver

In (GUO, 2000) and (ORSATTI, 2000), two different intermediate frequencies VGA implementations were developed, aiming a low-IF GSM receiver. Both implementations use 3 stages of a differential amplifier with CMFB and offset circuits. The gain control is achieved by varying the transconductance and output loads.

In (DUONG, 2006) and (YMAJI, 2002), in order to achieve a wide linear-in-dB control range and a wider bandwidth (necessary in CDMA applications), the transistors of the differential amplifier stages are biased in a subthreshold exponential region. An additional temperature independent bias circuitry is used to control the gain.

In (XIAO, 2007), a high dynamic range RF (470 – 870MHz) VGA implementation suitable for mobile digital television (DTV) tuners was developed. The architecture is based in a variable-G_m configuration with a pre-attenuation stage ensuring both low noise and robust input matching. In order to achieve a high gain and bandwidth (with a 1dB resolution) a control block based on a master-slave technique is implemented.

6.3 The front-end building blocks topologies

Considering the previous analysis, the chosen CMOS-based topologies for each building block stage of the front-end are now presented, aiming its best performance for our target application.

6.3.1 The up-conversion mixer stage

The up-conversion mixer must translate the input signal to the first processing frequency *fp1* outside the input frequency band. A double-balanced CMOS Gilbert Cell based topology with multi-tanh V-I converter and a LC tank as output load was chosen, as showed in Figure 6.15.

Since the input signal varies in amplitude and frequency in a wide range, a very linear input stage is realized using the multi-tanh technique. The LC tank load tuned at the output frequency (*fp1)* optimizes the noise figure and provides some suppression of the harmonic mixing and image components of the system path.

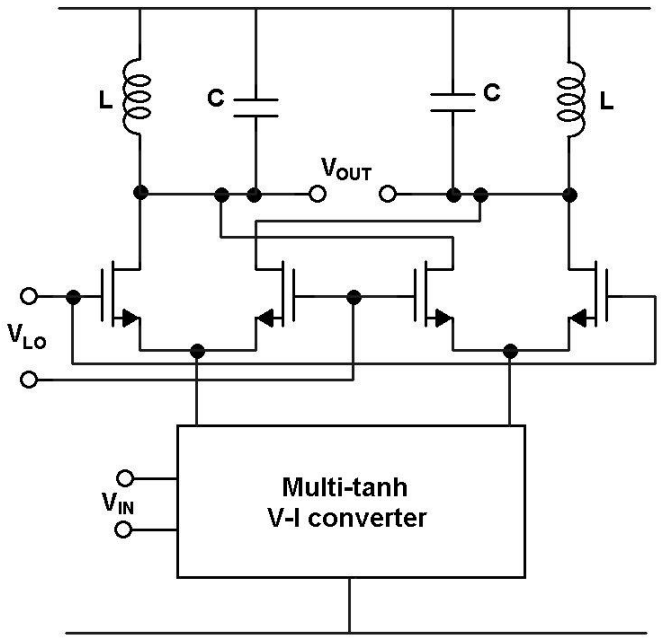


Figure 6.15: Up-conversion mixer topology to be implemented.

6.3.2 The down-conversion mixer stage

The down-conversion mixer must translate the signal from the first processing frequency *fp1* to the second processing frequency *fp2*.

Figure 6.16 shows the chosen down-conversion mixer architecture: a simple double-balanced CMOS Gilbert Cell based topology with resistive load. The input now is at a fixed frequency (*fp1)* tuned and filtered by LC tank load of the previous stage, relaxing the linearity and noise requirements for this stage.

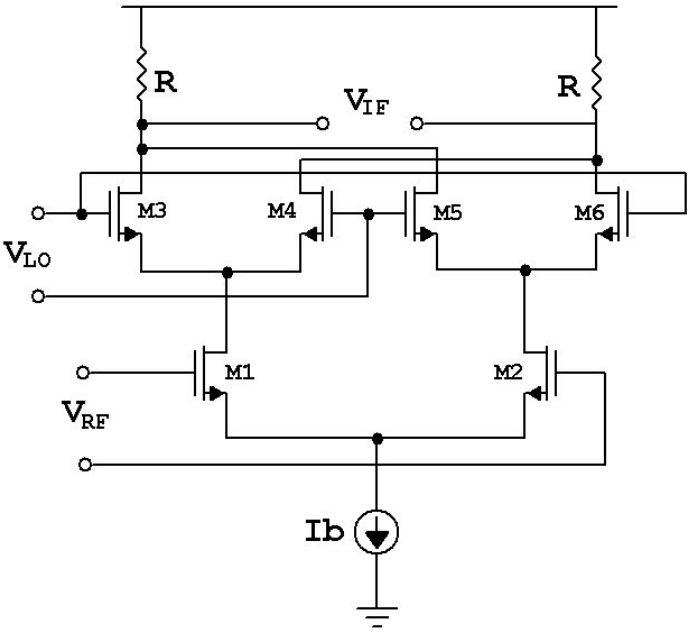


Figure 6.16: Down-conversion mixer topology to be implemented.

6.3.3 The VGA stage

Considering that our application requires a gain variation range of about 70dB, a 3-stage VGA was chosen be used, with about 26dB/stage, as illustrated in Figure 6.17.

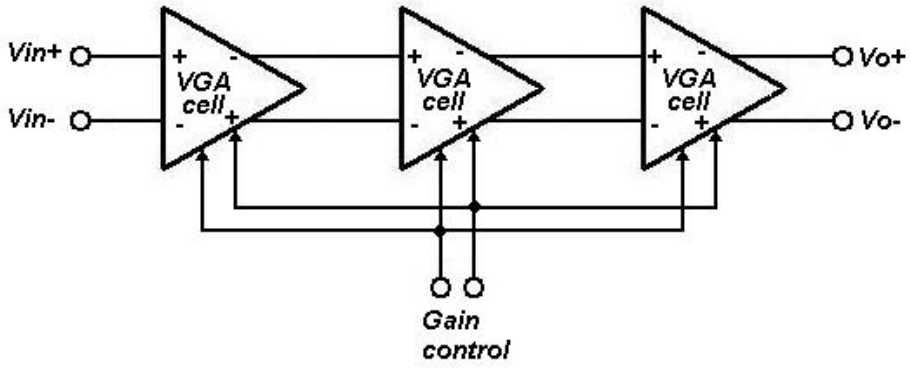


Figure 6.17: Block diagram of the 3-stage VGA.

Figure 6.8 shows the VGA basic cell architecture, based on (GUO, 2000) (GUO, 2002). It comprises a NMOS input differential pair (M1-M2) with four cross-coupled transistors in cascade to control the gain (M3-M4-M5-M6), two PMOS transistors as active load (M7-M8), and a common mode feedback circuitry (M9-M10). Vc and Vr are used to control the gain. When the cross is turned off, Vr= 0.6V and Vc=0.1V, the gain is maximum. When Vr=Vc=0.6V, the cross coupling is maximum and the gain is about 0dB.

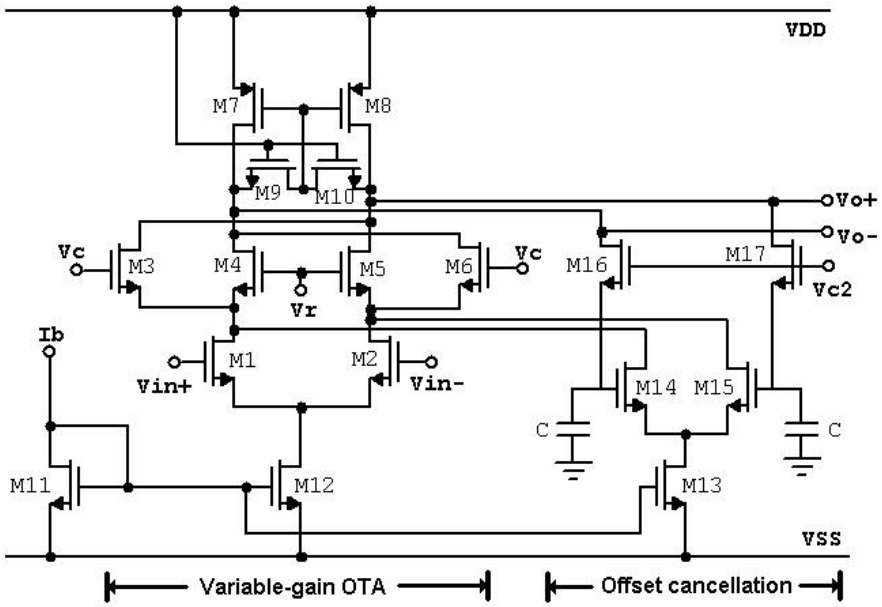


Figure 6.18: VGA basic cell with offset cancellation proposed in (GUO, 2000).

In order to prevent the VGA from being saturated due its high gain and high input offset voltage, an offset cancellation circuitry is employed. It consists of a negative feedback with a lowpass filter. M16 and M17 are working in linear region as two resistors. These resistors together with the two capacitors form the lowpass filters that block the input signal in the feedback path in order to guarantee that the gain is not affected. M14 and M15 are used to convert the voltage feedback signal to current, which is added to the input signal.

Compared to other recent CMOS VGAs implementations, in which the gain variation is obtained by varying either the source degeneration transistors or the bias current, this simple topology consumes less power and area, using a continuous-time automatic offset cancellation technique.

6.4 Discussion

This chapter addressed the analysis of the building blocks that composes the target dual-conversion superheterodyne front-end block of the FAC, aiming CMOS-based topologies.

In this context, we analyzed and discussed the most significant characteristics and topologies of each the building block: the mixer and VGA blocks. The main published implementations of each building block were also briefly described.

Finally, the chosen CMOS-based topologies for the three building blocks of the front-end were presented, aiming the best performance for our target application. Each circuit will be analyzed and designed in the next chapter.

7 FRONT-END BUILDING BLOCKS DESIGN, IMPLEMENTATION AND SIMULATION

In this chapter, the implementation of the discussed building blocks, from the mixers to the VGA, including the complete front-end will be presented. Each block was design using the g_m/I_D method, and implemented in IBM 0.18µm CMOS technology.

7.1 The g_m/I_D method applied to analog/RF circuit design

In Chapter 4, we presented the experimental results obtained from a low-frequency implementation of several analog blocks using the g_m/I_D method (SILVEIRA, 1996), aiming the baseband section of the FAC, demonstrating the capability of this design method. Thus, the use in the design of the analog blocks that composes the RF section of the FAC (IF front-end) is straightforward.

In this method, the relationship between the ratio of the transconductance over DC drain current and the normalized drain current $I_D/(W/L)$ is considered as a fundamental design tool to be explore in the design space. Once the value of the g_m/I_D ratio is chosen to fit the operation region of the device (strong, moderate and week inversion), the W/L of the transistor can be determined in the curve.

7.1.1 The g_m/I_D curves

The first step is to obtain the g_m/I_D curves to be used as a design tool for the target technology (IBM 0.18µm CMOS process). Since the experimental data is not available yet, the simulated data (using *Spectre* simulator and the foundry-supplied typical BSIM3v3 model parameters) will be considered.

Figure 7.1 shows the g_m/I_D versus $I_D/(W/L)$ fundamental curves obtained through electrical simulations for the IBM 0.18µm CMOS process. First, the I_D vs. V_{GS} DC curves were obtained using both NMOS and PMOS transistors of $W/L=1$ (W=1µm, L=1µm), where $V_D=V_G= 0$ *to* $1.8V$ and $V_S=V_B= 0V$. From equation 7.1, the g_m/I_D vs. $I_D/(W/L)$ curve can be obtained.

$$\frac{gm}{ID} = \frac{1}{ID} \times \frac{\partial ID}{\partial VG} = \frac{\partial \ln ID}{\partial VG} \tag{7.1}$$

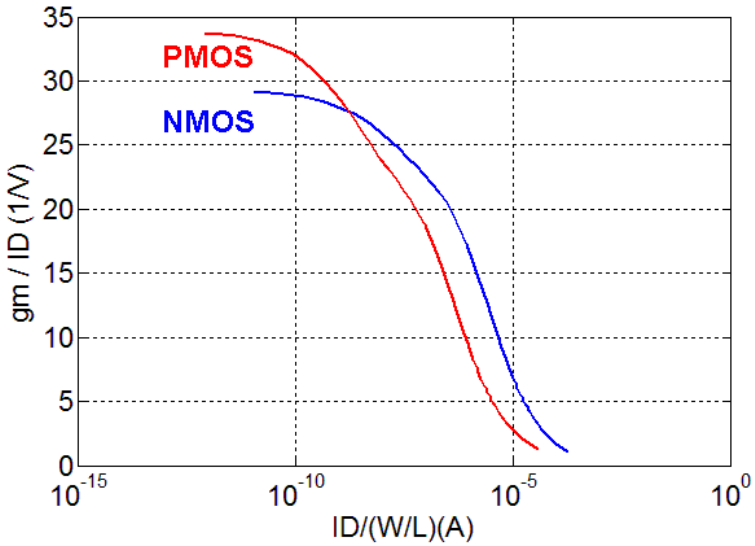


Figure 7.1: Simulated g_m/I_D versus $I_D/(W/L)$ plots for NMOS and PMOS transistors for IBM 0.18µm CMOS process.

In addition to the fundamental g_m/I_D curve, two additional curves were obtained in order to help in the design. The g_m/I_D vs. V_{GS} curve, showed in Figure 7.2, is obtained directly from the procedure described above. This curve can be used in the design of mixers when external bias voltages are needed in order to bias the differential pairs.

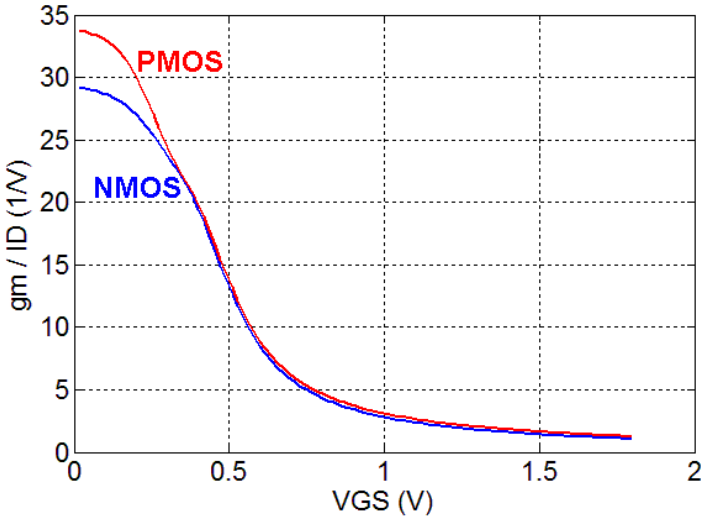


Figure 7.2: Simulated g_m/I_D *vs.* V_{GS} plots for NMOS and PMOS transistors for IBM 0.18µm CMOS process.

For the second additional curve, we consider another important characteristic related with the g_m/I_D parameter: the relationship between g_m/I_D vs. VA (the Early Voltage parameter). This relationship is considered as a fundamental device technology relation that determines the minimum allowable transistor lengths.

Figure 7.3 shows the g_m/I_D vs. *VA* curves obtained through electrical simulations for the IBM 0.18µm CMOS process. The values of g_m/I_D and *VA* were obtained directly from the DC operating point calculations using the *Spectre* simulator and BSIM3v3 model. The curves were obtained using both NMOS and PMOS transistors of W=1µm and different lengths (L = 0.18, 0.6, 1, 2.5, 5µm), where $V_D=V_G=0$ *to* $1.8V$ and $V_S=V_B=0V$.

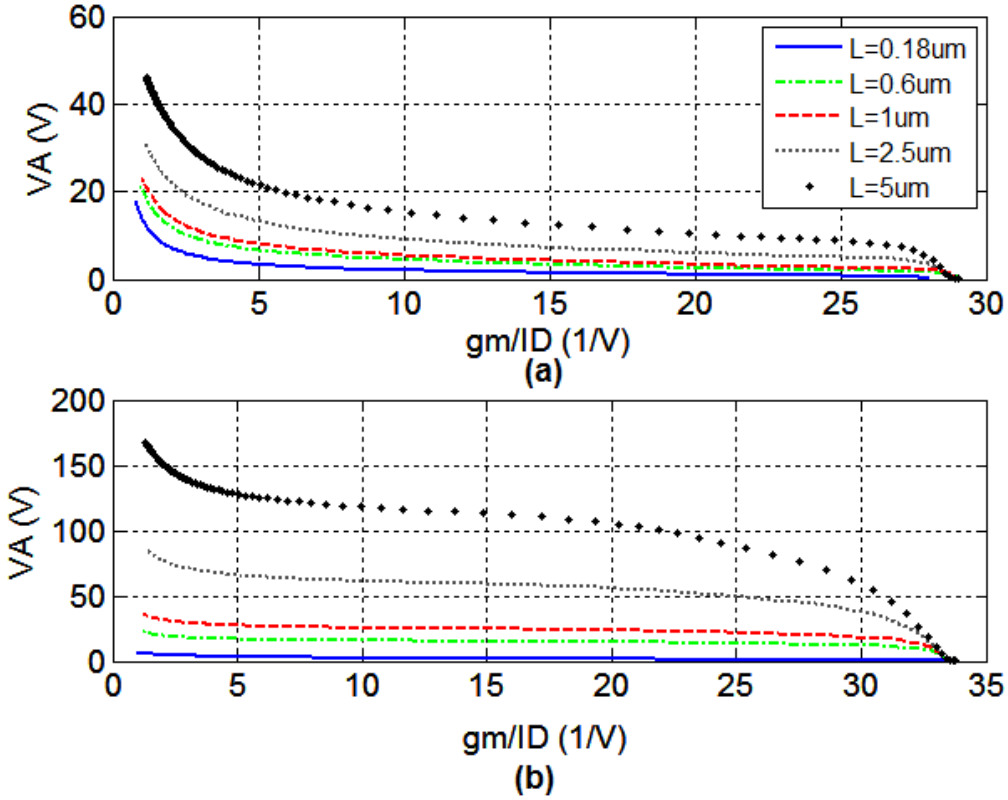


Figure 7.3: Simulated g_m/I_D *vs.* VA plots for (a) NMOS and (b) PMOS transistors for IBM 0.18µm CMOS process.

7.1.2 Design methodology

The design methodology discussed here is based in (SILVEIRA, 1996) (CORTES, 2003), and it is focused on the particularity of our target analog/RF building blocks. The three previous obtained curves are the main design tools, each a characteristic curve that depends only on the technology. The proposed design methodology is presented in the scheme of Figure 7.4.

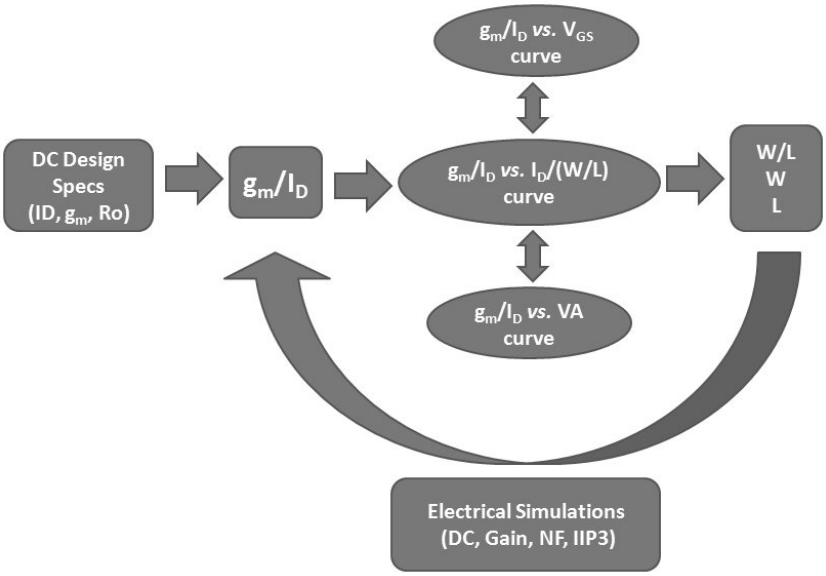


Figure 7.4: Design methodology.

Given a DC specification (bias current, transconductance gain, etc.) the g_m/I_D factor is chosen for each transistor (the operation region of the device is determined). Using the transistors characteristics curves of Figures 7.1, 7.2 and 7.3, the dimensions (W/L), bias voltages and lengths can be determined. From this point, several electrical simulations are executed and then the design parameters can be readjusted until the desired performance can be achieved.

Depending on the circuit topology, different design performance parameters can be considered in the design process. There are several factors that can reflect the performance of our target circuits, such as gain, linearity, noise and power consumption. Adjusting circuitry in order to optimize a particular performance parameter may unintentionally degrade the performance of other parameters. Thus, it is important to monitor all the performance parameters in the design process through electrical simulations.

In the following sections, the design of each building block, followed by its layout implementation and post-layout simulations, will be described in detail.

7.2 Up-conversion mixer design

The up-conversion mixer stage must translate the input signal to the first processing frequency *fp1* outside the input frequency band. Figure 7.5 shows the complete schematic of the double-balanced CMOS Gilbert Cell based topology with multi-tanh V-I converter and a LC tank output load, as discussed in Chapter 6.

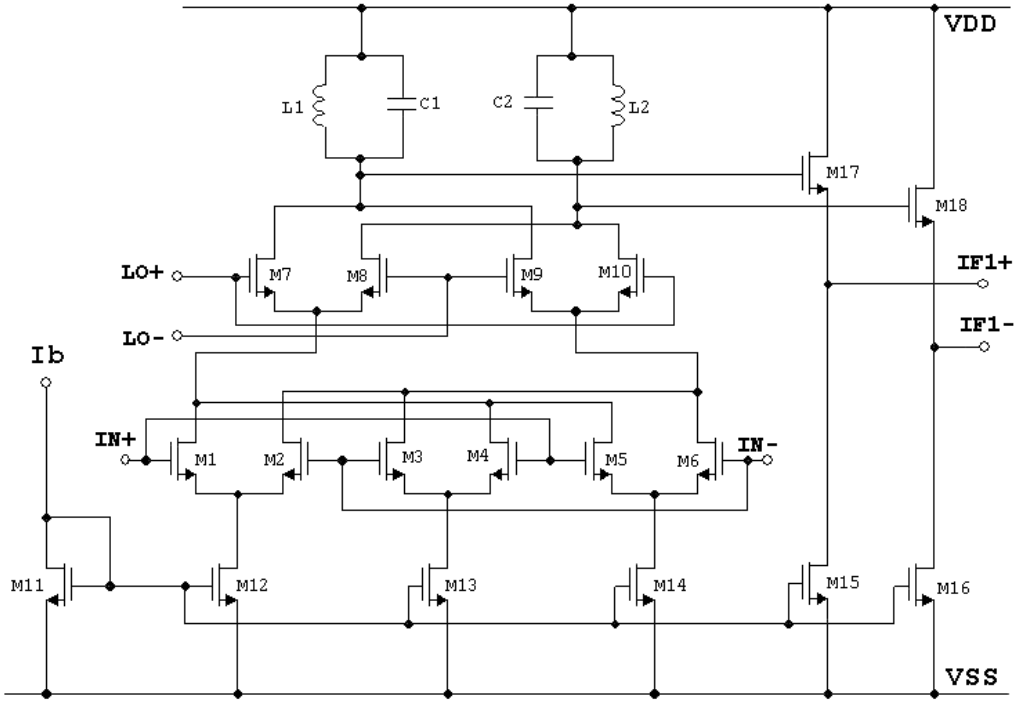


Figure 7.5: Up-conversion mixer complete schematic.

7.2.1 Design procedure

The up-conversion mixer was analyzed and designed in IBM 0.18µm CMOS process using the g_m/I_D design method. It must provide a 5dB gain, 10dB noise figure, and 1dBm IIP3, under different input frequencies (according to the system level analysis described in Chapter 5).

For the initial design, the double-balanced CMOS Gilbert Cell topology was considered. The design procedure is based in (SILVER, 1997) (SANCHEZ, 2004), using the g_m/I_D method previous described. The complete design procedure is demonstrated as follows.

7.2.1.1 Current mirror stage

Considering signal level and power specifications, the bias current in was set to *4mA*.

The current mirror transistors should operate in strong inversion in order to guarantee good matching and noise properties. Thus, the g_m/I_D ratio was initially set to 8, and from the g_m/I_D *vs.* $I_D/(W/L)$ curve we have $(W/L)=596$.

7.2.1.2 LO stage

In the LO stage, for proper switching, the *Vgs* of the LO differential pairs need to be just slight larger then *Vt* and the width need to be large. Thus, V_{GS} was chosen to be *0.7V*, and from the g_m/I_D *vs.* V_{GS} curve we can determine the operation region the transistors: $g_m/I_D=6$. From the g_m/I_D *vs.* $I_D/(W/L)$ curve we have $(W/L)=74$.

7.2.1.3 Input stage

Assuming a simple differential pair at the input stage with a resistive load, the conversion gain is proportional do the transconductance of the input differential pairs as shown in equation 7.2.

$$CG = \frac{2}{\pi} \times (gm \times RL) \tag{7.2}$$

With the *CG* goal set at 5 dB and assuming RL=500Ω, we can calculate *gm* :

$$3.16 = \frac{2}{\pi} \times (gm \times 500) \leftrightarrow gm = 9.92mS \tag{7.3}$$

By knowing the required transconductance (*gm*), the g_m/I_D is set to 5 and the sizes of the input differential pairs can be determined by using the g_m/I_D *vs.* $I_D/(W/L)$ curve. Thus, we have *(W/L)=113.*

In order to improve linearity without decreasing the gain, the multi-tanh linearization technique was used. First, the simple differential pair (Figure 7.6a) was replaced by two differential pairs operating in parallel (Figure 7.6b) using mismatched transistor aspect ratios (*n=6*). Finally, the desired linearity and gain tradeoff was obtained by replacing the simple differential pair by three differential pairs operating in parallel (Figure 7.6c) using mismatched transistor aspect ratios (*n=9*).

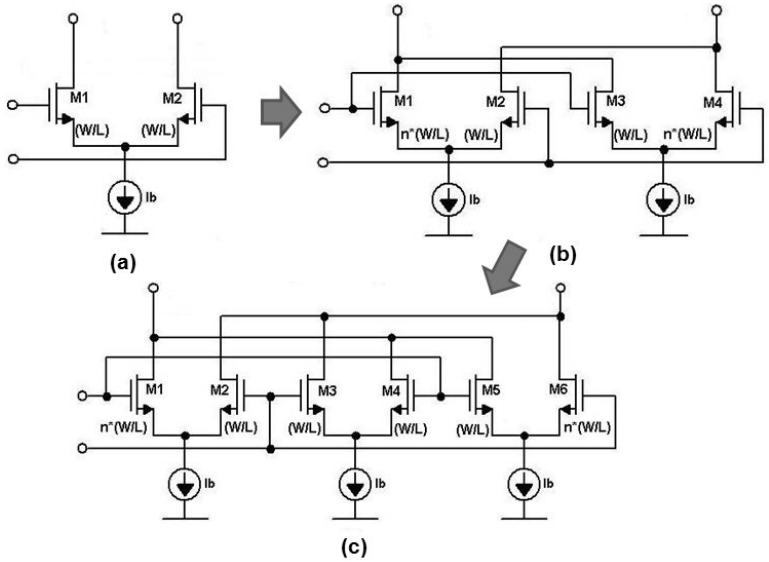


Figure 7.6: (a) Simple differential pair cell, (b) multi-tanh doublet cell, (c) multi-tanh triplet cell.

7.2.1.4 LC tank load

The up-conversion mixer has a broadband input and a fixed output at 1.4GHz. It only needs to provide gain over a narrow frequency range centered at 1.4GHz.

A LC tank tuned at *fp1* (1.4GHz*)* is used in the load, providing larger output swings, and some image and noise suppression. From equation 7.4 (and assuming a *Q* of about 8 at 1.4GHz), we obtained *C=1.42pF* and *L=9.1nH*.

$$\omega_0 = \frac{1}{\sqrt{LC}} \tag{7.4}$$

Considering the available component library of the IBM 0.18µm process design kit, the inductor was implemented as a single layer spiral inductor (L=7.218n), and the capacitor as a metal-insulator-metal (MIM) capacitor (C=898.63fF).

7.2.1.5 Buffer stage

Considering a *5pF* load at the output, a buffer stage was added in the output for convenience of measurements (in order to drive instrumentation with 50Ω inputs).

A NMOS source follower topology (RAZAVI, 2002) was chosen due to its low input capacitance and flat gain response over a wide range of frequencies. Assuming that the output resistance of this stage is $1/gm_1$ (neglecting the body effect), we have

$$R_{out} = \frac{1}{gm} = 50\Omega \rightarrow gm = 20mS \tag{7.5}$$

For high bandwidth and low input capacitance, the signal transistors (*M17/M18*) were sized to operate in strong inversion with $g_m/I_D=10$, dictating a bias current of approximately *10mA* and a *(W/L)=192* (from the g_m/I_D *vs.* $I_D/(W/L)$ curve).

Considering a 50 Ω and *5pF* load at the output, the simulated gain of the buffer is roughly -6dB up to 10GHz, which is enough for this case.

7.2.1.6 Design modifications – final design

Considering this previous analysis, several modifications and adjustments were made to the initial design after running electrical simulations. The following changes were incorporated to the design:

- The LO switching transistors were resized, considering a $g_m/I_D=9$, to achieve improved NF and conversion gain. These transistors significantly improved the overall performance;
- The transistors were implemented as "multifinger" transistors, reducing both the S/D junction area and gate resistance;
- All transistors lengths were set to minimum ($L=0.2\mu m$), in order to minimize thermal noise.

Table 7.1 shows all the components values for the final version of the up-conversion mixer design.

Table 7.1: Up-conversion mixer component summary.

Component Name	*Value*	g_m/I_D
M1,M6 (W/L)	n*30*(2.5µm/0.2µm)	17
M2,M3,M4,M5 (W/L)	30*(2.5µm/0.2µm)	10
M7, M8, M9, M10 (W/L)	28*(2.5µm/0.2µm)	9.5
M11, M12, M13, M14 (W/L)	40*(6µm/0.2µm)	12
M15, M16 (W/L)	100*(12µm/0.2µm)	11.3
M17, M18 (W/L)	10*(52µm/0.2µm)	7
N	9	-
C1, C2	898.63fF (MIM HK cap – 20 x 22 μm^2)	-
L1, L2	7.218nH (ML ind - x=400µm, w=5µm, s=4µm, n=3)	-

7.2.2 Layout implementation

The circuit layout design was completed using *Cadence Virtuoso Design Editor Environment* in IBM 0.18µm CMOS process with 6 metal layers.

In order to prevent the effect of gradients resulting mismatches due to process variations, the input differential pairs were implemented using a common-centroid configuration. The switching transistors were interdigitated, minimizing interface between the pair during on/off switching.

The on-chip LC tank was implemented using automatic layout generation from the available component library of the IBM 0.18µm process design kit. The inductor was implemented as a single layer ML (last metal) spiral inductor with a M1 groundplane. Considering typical inductor modeling (BURGHARTZ, 1998) (NIKNEJAD, 1998) (MOHAN, 1999), a spiral inductor with x=400µm (diameter), w=5µm (turn width), s=4µm (turn spacing) and n=3 (number of turns) was chosen (L=7.218n, *Q* of about 8 at 1.4GHz). The capacitor was implemented as a single HiK-dielectric MIM (metal-insulator-metal) capacitor (C=898.63fF, considering the parasitic capacitances of the buffer stage).

In order to eliminate the nonlinearity effects due to the body effect, in the source follower buffer stage, a triple well (isolated NMOS) transistor (available at the component library of the IBM 0.18µm process design kit) was used, allowing the transistor bulk to be tied to the source.

All mixer components are symmetric with respect to other components in the same stage, i.e., switching LO transistors, input differential pairs, current mirrors and LC tank loads. The architecture is fully differential and laid out as symmetrically as possible to minimize the mismatch in the signal paths. The physical spaces in components were carefully chosen to be small enough to reduce parasitics and area, and at the same time far enough apart to minimize coupling and contamination of the RF signals. Figure 7.7 illustrates the complete up-conversion mixer layout design, with a total area of $0.71mm^2$.

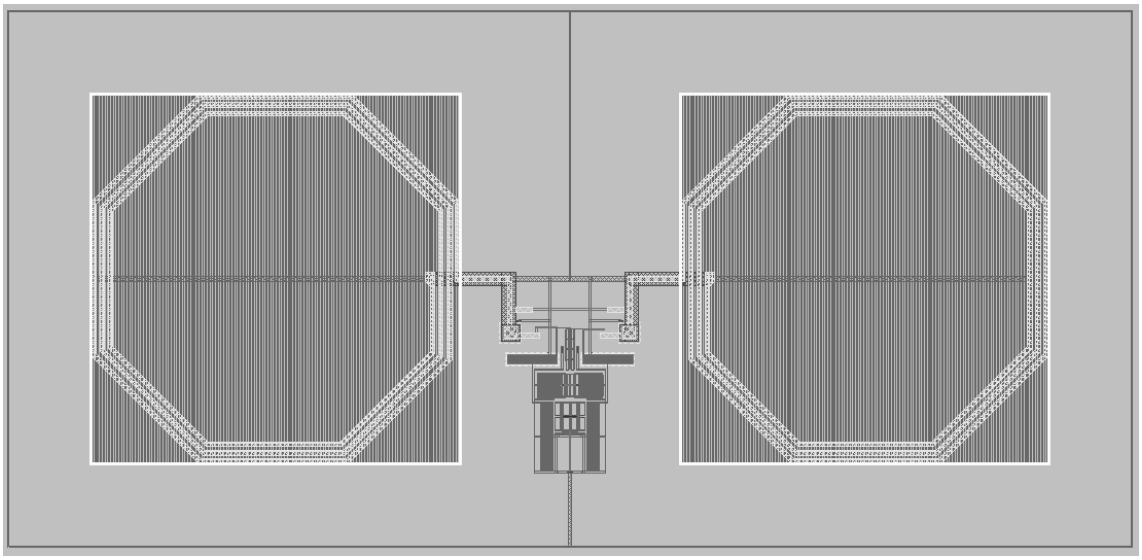


Figure 7.7: Up-conversion mixer final layout.

7.2.3 Simulation results

The circuit performance was verified through electrical simulations using the *Spectre* simulator tool and the BSIM3v3 foundry supplied model. The simulation setup used to simulate the mixer is shown in Figure 7.8.

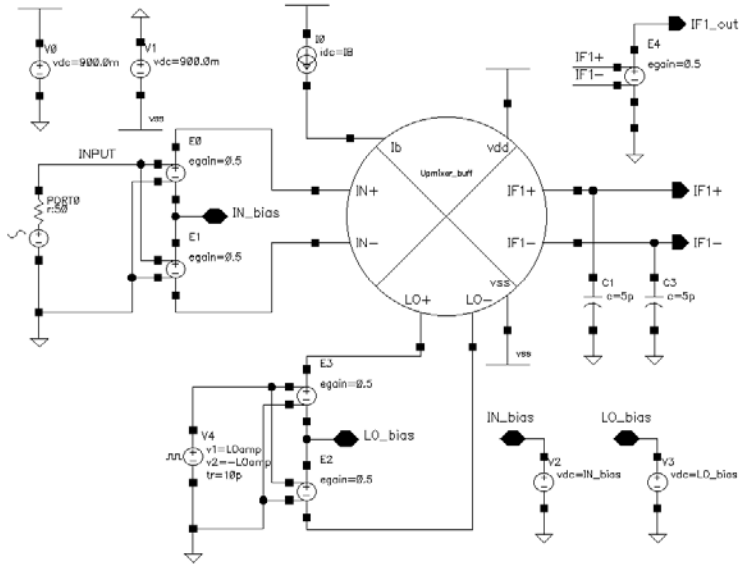


Figure 7.8: Up-conversion mixer simulation testbench.

In the following subsections, the main simulated curves which characterize the performance of the mixer (schematic version) are presented, considering an input signal of -30dBm at 450MHz and a square LO signal of 950MHz and 200mVpp of amplitude. Square LO signals (hard switching) are usually preferred over the sinusoidal LO signals (Soft switching), since the LO differential pair transistors act as hard switches, and the noise contribution of these transistors can be analyzed during these two stages:

- when both the LO transistors are ON, they behave as a normal differential pair and have a huge contribution to noise;
- when one of the transistors is ON, and the other OFF, the ON transistor behaves as a cascode transistor to the input RF transistor. Cascode transistors are known to have minimal noise contribution.

7.2.3.1 Transient analysis

The transient analysis displays the AC signal in the time domain. A sinusoidal input signal of 450MHz of frequency, and amplitude of 31.6mVp (-30 dBm) was applied on the input. Figure 7.9 shows the transient and frequency (FFT) curves, respectively of the input and output signals.

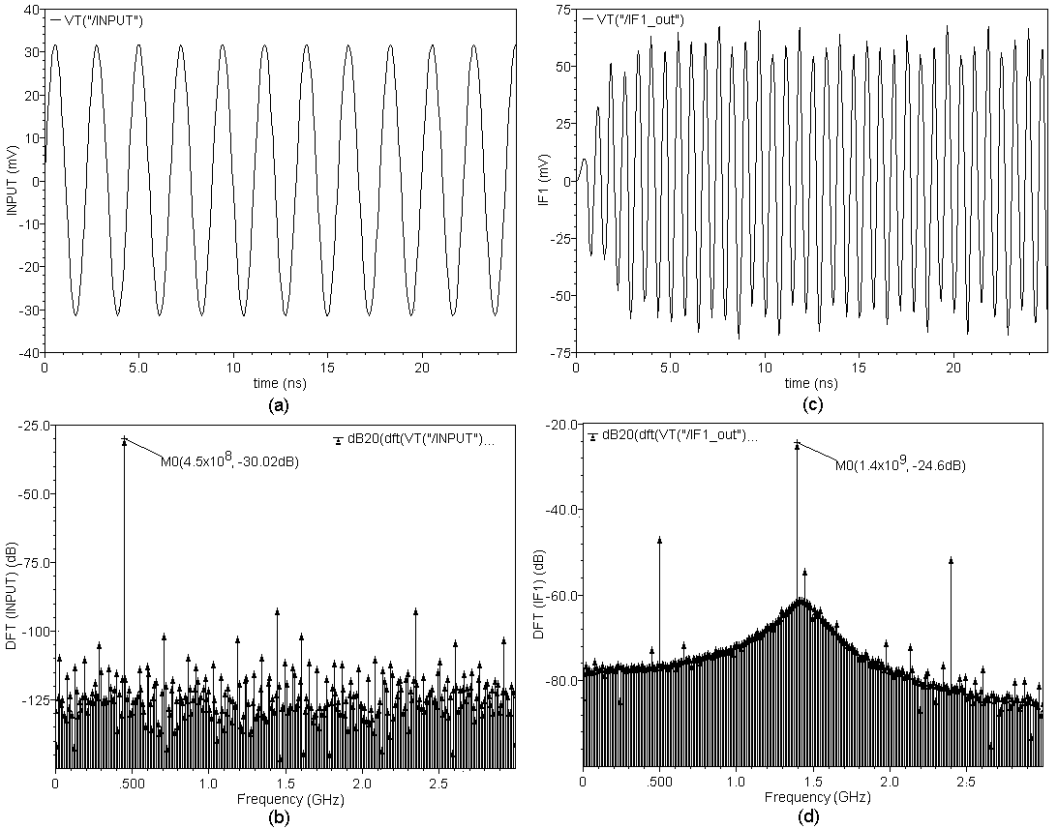


Figure 7.9: Up-conversion mixer transient analysis: input (a) and output (b) signals curves in time domain; input (c) and output (d) signals curves in frequency domain.

7.2.3.2 PSS analysis

The periodic steady-state (PSS) analysis is employed to characterize the conversion gain (CG) of the mixer. The voltages at the output and input ports in dB20 are given in Figure 7.10.

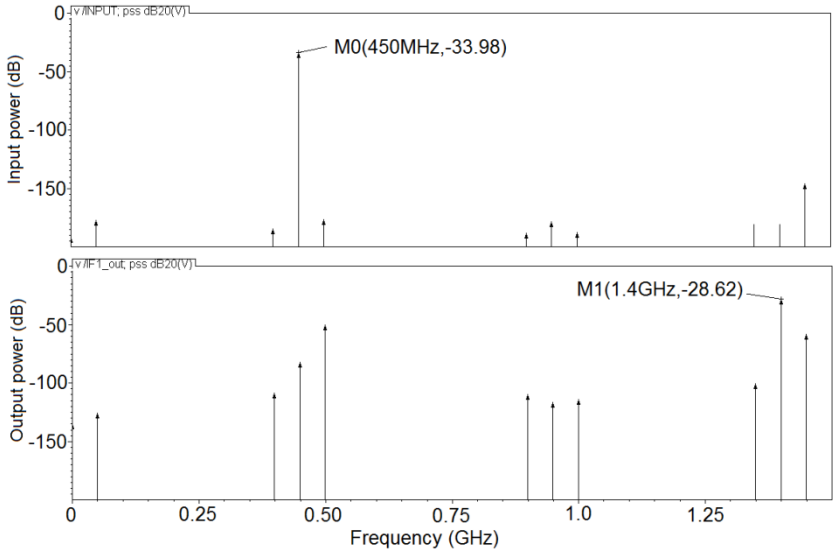


Figure 7.10: Up-conversion mixer PSS simulation results.

It can be observe that the input port, there are signal tones at 450 MHz and 1.4 GHz (this tone is due the feed through from the LO port). Thus, the conversion gain is

$$CG = -28.62 — (-33.98) = 5.36dB \tag{7.6}$$

A swept periodic steady-state analysis is employed to characterize the effect of the variation of both input and LO power signals in the performance of the mixer. Thus, the conversion gain vs. input power plot was obtained and is given in Figure 7.11. The conversion gain vs. LO amplitude plot is given in Figure 7.12.

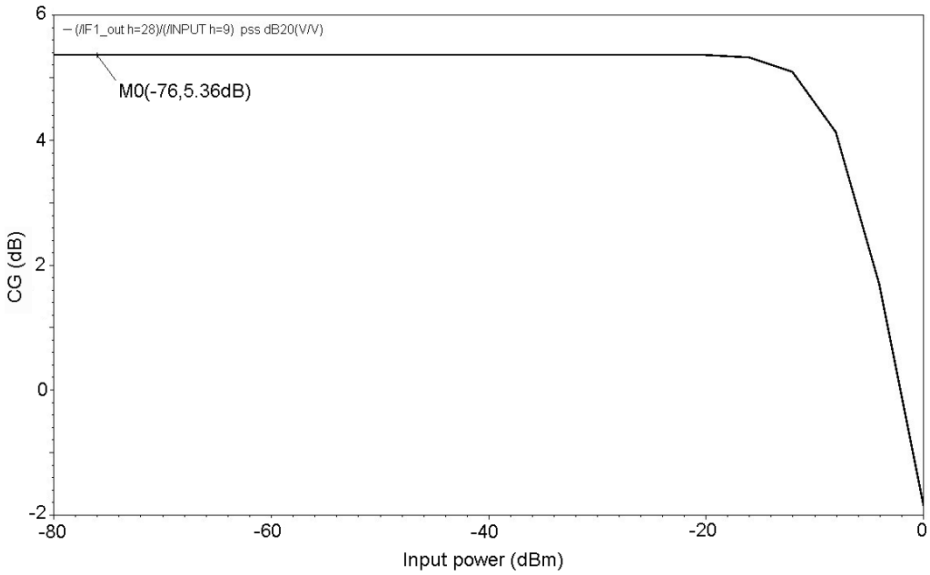


Figure 7.11: Conversion Gain vs. Input Power simulation results – up-conversion mixer.

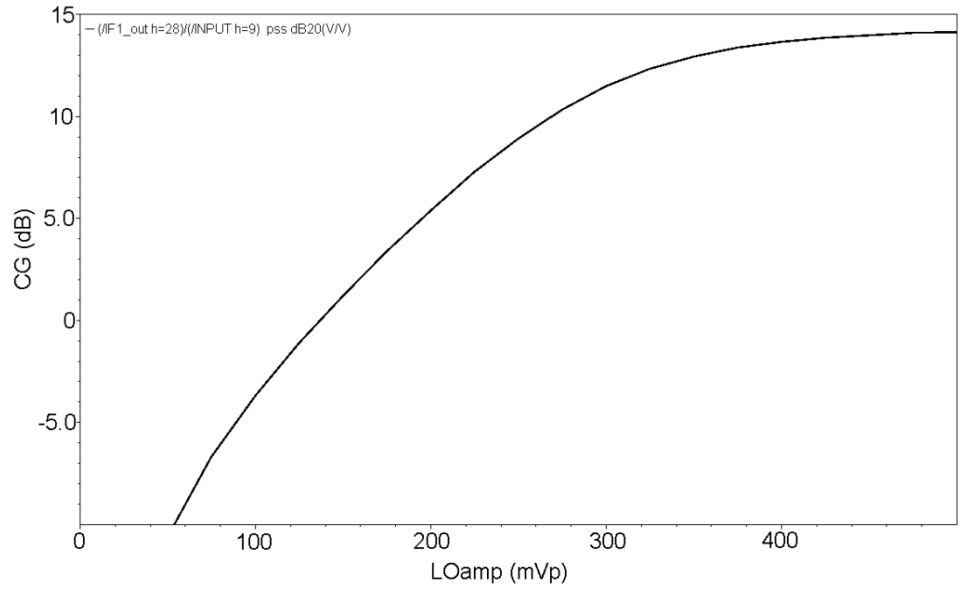


Figure 7.12: Conversion Gain vs. LO Power simulation results – up-conversion mixer.

7.2.3.3 Linearity analysis

For the IIP3 simulation, two equal tones at *FIN+2MHz* and *FIN-2MHz* are given at the input port, as the two-tone intermodulation test method (RAZAVI, 1998).

Figure 7.13 shows the overall IIP3 curve sweeping the input power of an input signal of 450MHz. It is reasonable to estimate the IIP3 using 1.402 GHz as the up converted fundamental and 1.394 GHz as the up converted IM3. It was further observed that the IIP3 obtained from the PSS simulations, was the same, with a fixed input power of -20 dBm.

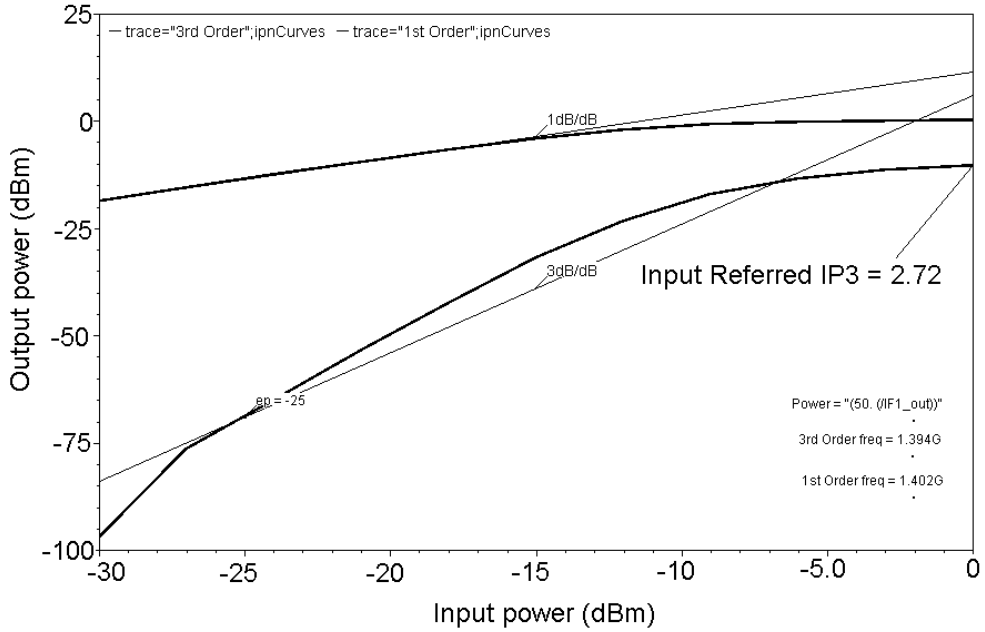


Figure 7.13: IIP3 simulation – up-conversion mixer.

7.2.3.4 Noise analysis

The noise figure (NF) of the mixer was obtained by using the *pnoise* option in the PSS simulations (Figure 7.14). For the mixer, the noise figure is usually related to the output noise at the IF port referred back to the input RF port.

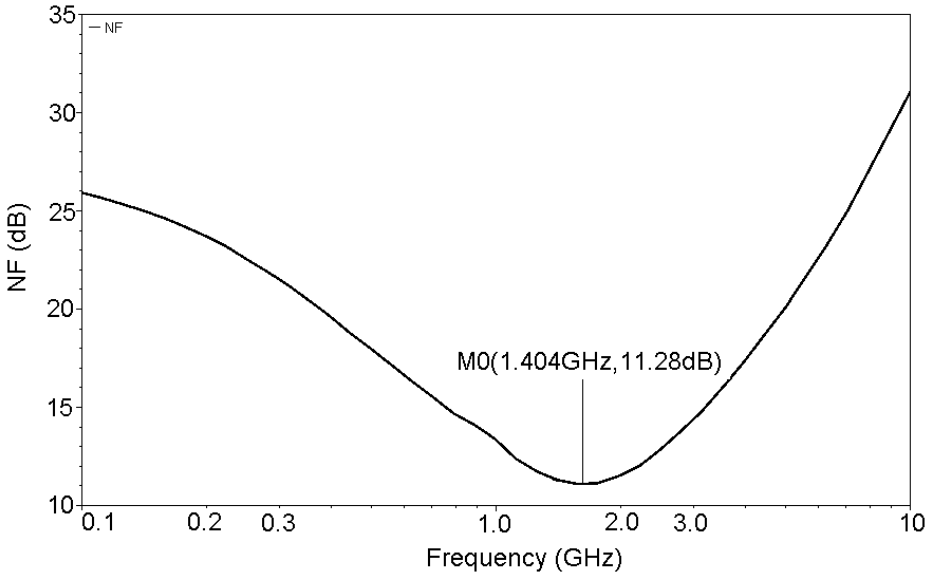


Figure 7.14: Noise figure simulation results – up-conversion mixer.

7.2.3.5 Performance summary

Table 7.2 summarizes the mixer simulation performance for both schematic and extracted versions of the design, under different input and LO frequencies. A 4.7bB conversion gain, 12dB noise figure, and 1.5dBm IIP3 are obtained under different input frequencies. The mixer core consumes about 10mA at a power supply of 1.8V (the output buffer consumes about 22mA). Considering these performance parameters, the mixer is appropriate to be used in our target system.

Table 7.2: Up-conversion mixer simulation performance summary.

		Schematic					*Extracted*			
FIN (Hz)	*LO (Hz)*	*IF1 (Hz)*	*CG (dB)*	*NF(dB) @1.4GHz*	*IIP3 (dBm)*	*Power cons. (mW)*	*CG (dB)*	*NF(dB) @1.4GHz*	*IIP3 (dBm)*	*Power cons. (mW)*
48M	1.352G		5.4		2		4.8		1.2	
108M	1.292G		5.3		2.8		4.8		1.2	
270M	1.130G		5.4		3	71.3	4.5		1.4	60.7
450M	950M	1.4G	5.3	11.2	3	(23.3 – mixer,	4.6	12.8	1.5	(18 – mixer,
600M	800M		5.4		3	48.03 – buffer)	4.5		1.4	42.7 – buffer)
869M	531M		5.4		2.4		4.5		1.5	
960M	440M		5.3		2.8		4.4		1.4	

7.3 Down-conversion mixer design

As shown in Figure 7.15, the down-conversion mixer stage is implemented in a simple double-balanced CMOS Gilbert Cell based topology. The input differential pair is degenerated by means of a two resistors.

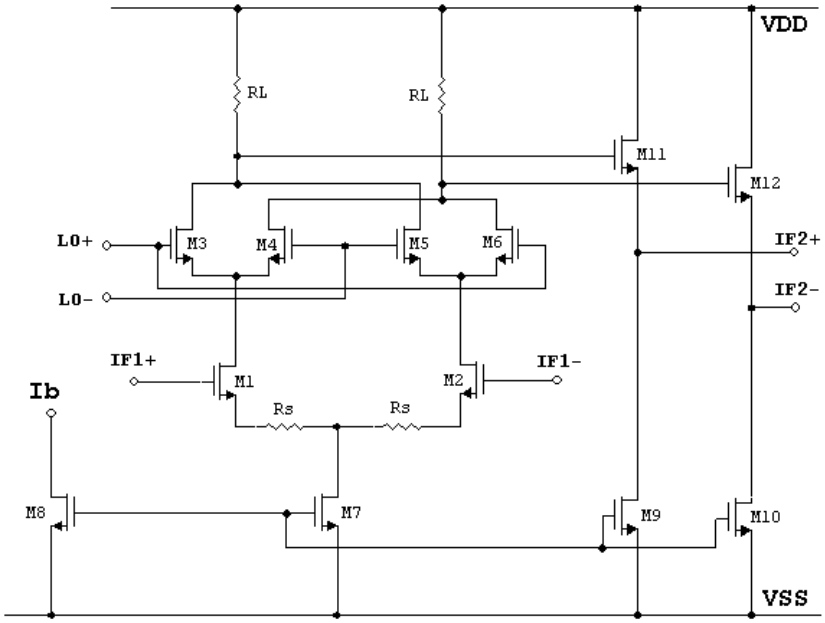


Figure 7.15: Down-conversion mixer complete schematic.

7.3.1 Design procedure

This stage was analyzed and designed in IBM 0.18µm CMOS process using the g_m/I_D design method. It must provide a 5dB gain, 12dB noise figure, and -3dBm IIP3, under an input frequency of 1.4GHz and a LO frequency of 1.36GHz.

The complete design procedure is demonstrated as follows.

7.3.1.1 Current mirror stage

Considering signal level and power specifications, the bias current in was set to *2mA*.

The current mirror transistors should operate in strong inversion in order to guarantee good matching and noise properties. Thus, the g_m/I_D ratio was set to 12, and from the g_m/I_D *vs.* $I_D/(W/L)$ curve we have *(W/L)=847.*

7.3.1.2 LO stage

In the LO stage, for proper switching, the *Vgs* of the LO differential pairs need to be just slight larger then *Vt* and the width need to be large. Thus, V_{GS} was chosen to be *0.6V*, and from the g_m/I_D *vs.* V_{GS} curve we can determine the operation region the transistors: $g_m/I_D=8$. From the g_m/I_D *vs.* $I_D/(W/L)$ curve, we have *(W/L)=150.*

7.3.1.3 Input stage

Assuming a simple differential pair at the input stage with a resistive load, the conversion gain is proportional do the transconductance of the input differential pairs as shown in equation 7.7.

$$CG = \frac{2}{\pi} \times (gm \times RL) \tag{7.7}$$

With the *CG* goal set at 5 dB and assuming RL=500Ω, we can calculate *gm* :

$$3.16 = \frac{2}{\pi} \times (gm \times 500) \leftrightarrow gm = 9.92mS \tag{7.8}$$

By knowing the required transconductance (*gm*) and the current bias, the g_m/I_D is set to 10 and the sizes of the input differential pairs can be determined by using the g_m/I_D *vs.* $I_D/(W/L)$ curve. Thus, we have *(W/L)=218*.

Source degeneration resistors were added in the input differential pair, improving linearity at the cost of increased NF (HAN, 1998).

7.3.1.4 Buffer stage

Considering a *5pF* load at the output, a NMOS source follower buffer stage was added in the output for convenience of measurements (in order to drive instrumentation with 50Ω inputs).

The signal transistors (*M11/M12*) were sized to operate in strong inversion with $g_m/I_D=10$, dictating a bias current of approximately *4mA* and a *(W/L)=260* (from the g_m/I_D *vs.* $I_D/(W/L)$ curve). When driving 50Ω and *5pF* load at the output, the simulated gain of the buffer is roughly -4dB up to 1GHz, which is enough for this case.

7.3.1.5 Design modifications – final design

Considering this previous analysis, some modifications and adjustments were made to the initial design after running electrical simulations. The following changes were incorporated to the design:

- The LO switching transistors were resized, considering a $g_m/I_D=9$, to achieve improved NF and conversion gain. These transistors significantly improved the overall performance;
- The source degeneration and load resistors were adjusted, considering the target linearity and gain requirements;
- The transistors were implemented as "multifinger" transistors, reducing both the S/D junction area and gate resistance.

Table 7.3 shows all the components values for the final version of the down-conversion mixer design.

Table 7.3: Down-conversion mixer component summary.

Component Name	*Value*	g_m/I_D
M1,M2 (W/L)	(32*11µm/0.2µm)	10
M3, M4, M5, M6 (W/L)	(24*7.5µm/0.2 µm)	13
M7, M8 (W/L)	(10*65 µm /1 µm)	9
M9, M10 (W/L)	(20*65 µm /1 µm)	12
M11, M12 (W/L)	(10*52 µm /0.2 µm)	11
RL	708.24 Ω (opnd res – w=0.85µm, l=8µm)	-
Rs	38.29 Ω (opnd res – w=3.5µm, l=1.5µm)	-

7.3.2 Layout implementation

The circuit layout design was completed using *Cadence Virtuoso Design Editor Environment* in IBM 0.18µm CMOS process with 6 metal layers.

The input differential pairs were implemented using a common-centroid configuration. The switching transistors were interdigitated, minimizing interface between the pair during on/off switching. The resistors (Rs and RL) were implemented as an N^+ diffusion resistor, considering the available component library of the IBM 0.18µm process design kit. In the source follower buffer stage, a triple well (isolated NMOS) transistor was used, allowing the transistor bulk to be tied to the source.

All mixer components are symmetric with respect to other components in the same stage, i.e., switching LO transistors, input differential pairs, current mirrors and resistor loads. The architecture is fully differential and laid out as symmetrically as possible to minimize the mismatch in the signal paths. Figure 7.16 shows the complete mixer layout, with a total area of 20,733µm^2.

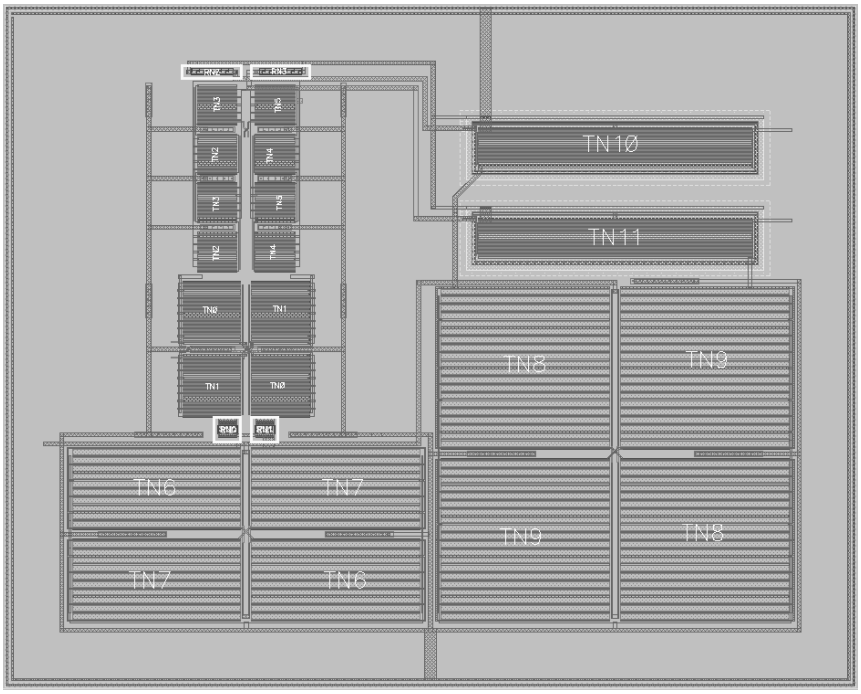


Figure 7.16: Down-conversion mixer final layout.

7.3.3 Simulation results

The circuit performance was verified through electrical simulations using the *Spectre* simulator tool and the BSIM3v3 foundry supplied model. The simulation setup used to simulate the mixer is shown in Figure 7.17.

In the following subsections, the main simulated curves which characterize the performance of the mixer (schematic version) are presented, considering an input signal of -30dBm at 1.4GHz and a square LO signal of 1.36GHz and 200mVpp of amplitude.

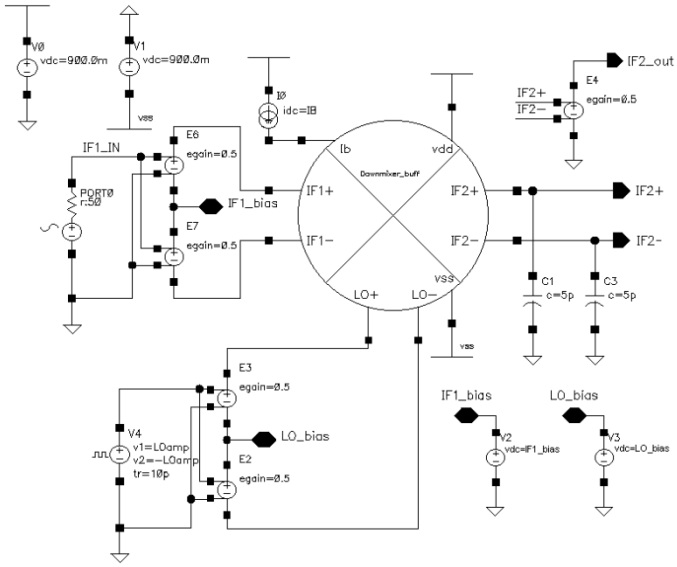


Figure 7.17: Down-conversion mixer simulation testbench.

7.3.3.1 Transient analysis

The transient analysis displays the AC signal in the time domain. A sinusoidal input signal of 1.4GHz of frequency, and amplitude of 31.6mVp (-30dBm) was applied on the input. Figure 7.18 show the transient and frequency (FFT) curves, respectively of the input and output signals.

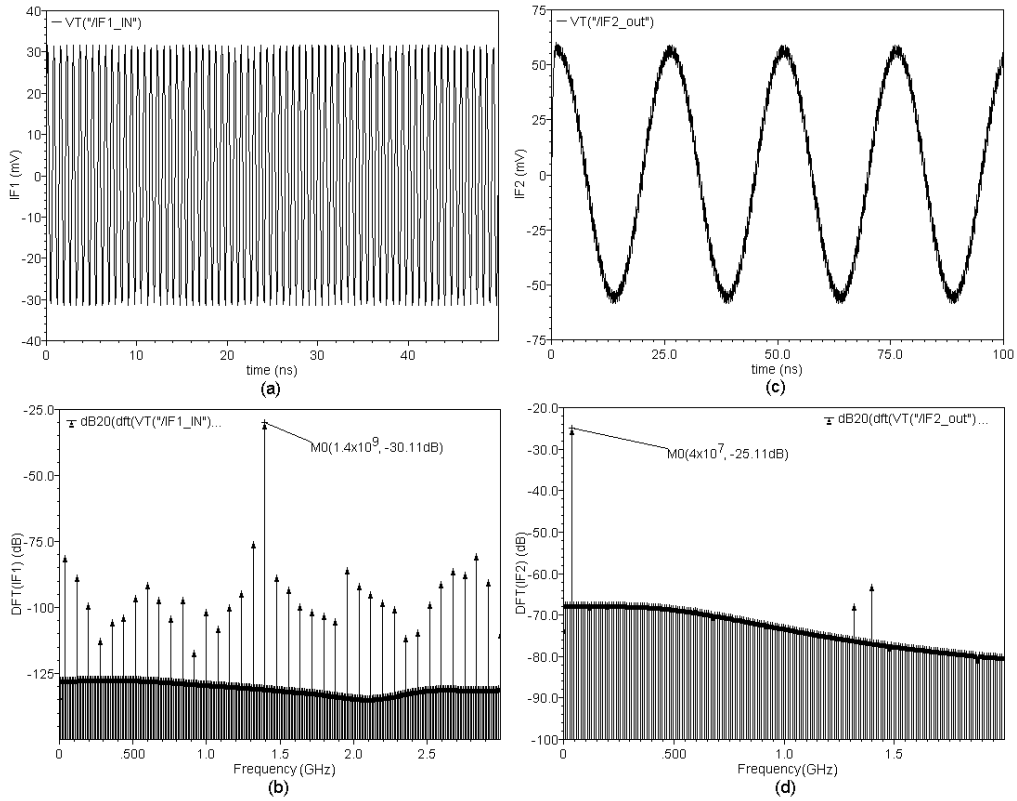


Figure 7.18: Down-conversion mixer transient analysis: input (a) and output (b) signals curves in time domain; input (c) and output (d) signals curves in frequency domain.

7.3.3.2 PSS analysis

The periodic steady-state analysis is employed to characterize the conversion gain of the mixer. The voltages at the output and input ports in dB20 are given in Figure 7.19.

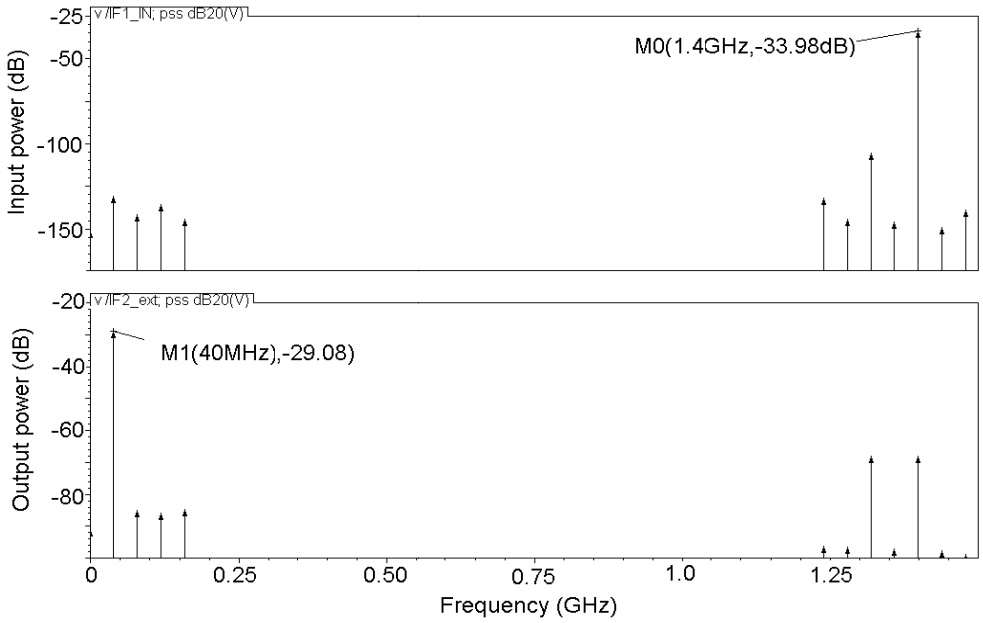


Figure 7.19: Down-conversion mixer PSS simulation results.

It can be observe that the input port, there are signal tones at 450 MHz and 1.4 GHz (this tone is due the feed through from the LO port). Thus, the conversion gain is

(7.9)

A swept periodic steady-state analysis is employed to characterize the effect of the variation of both input and LO power signals in the performance of the down-conversion mixer. Thus, the conversion gain vs. input power plot was obtained and is given in Figure 7.20. The conversion gain vs. LO amplitude plot is given in Figure 7.21.

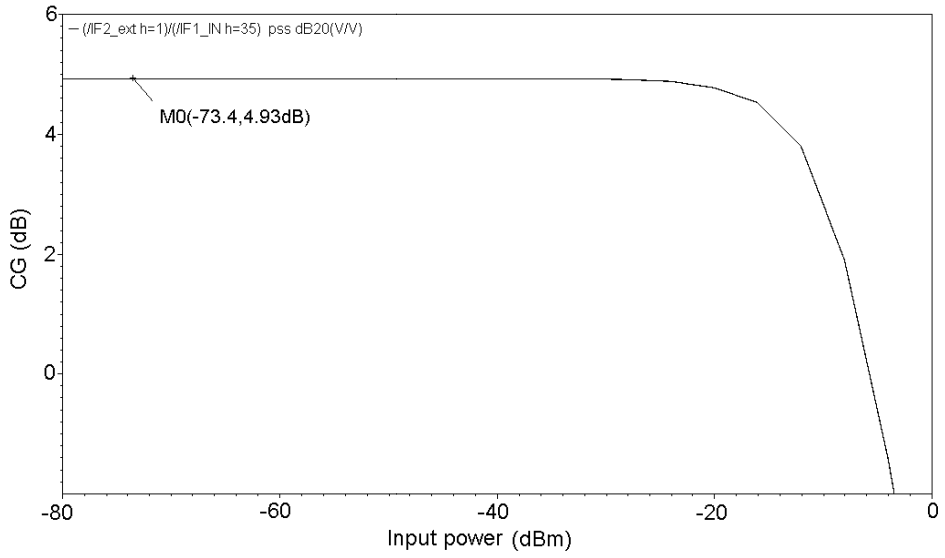


Figure 7.20: Conversion Gain vs. Input Power simulation results – down-conversion mixer.

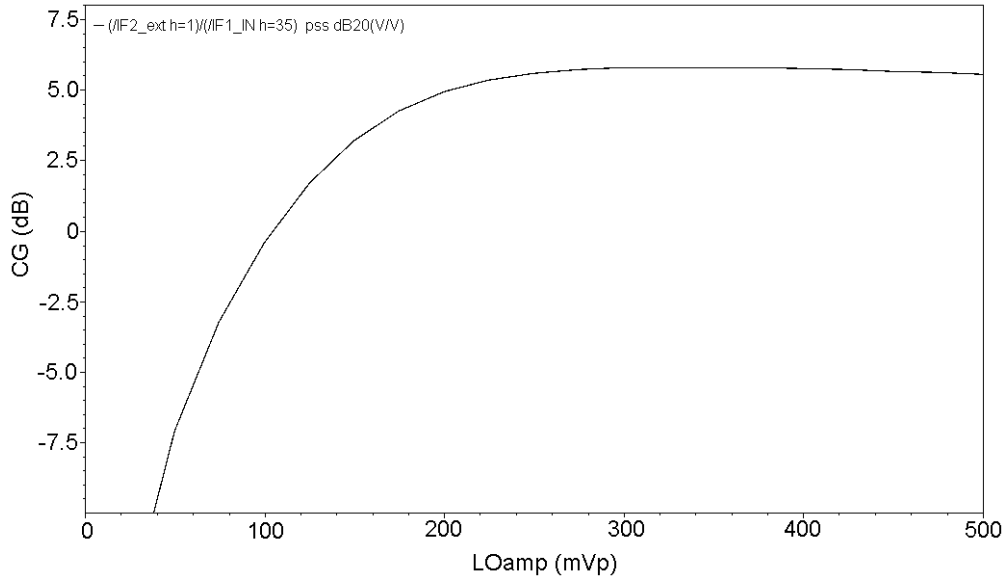


Figure 7.21: Conversion Gain vs. LO Power simulation results – down-conversion mixer.

7.3.3.3 Linearity analysis

For the IIP3 simulation, two equal tones at *IF1+50MHz* and *IF1-50MHz* are given at the input port (RAZAVI, 1998). Figure 7.22 shows the overall IIP3 curve sweeping the input power of the input two tones. It is reasonable to estimate the IIP3 using 10MHz as the down-converted fundamental and 190MHz as the down-converted IM3. It was further observed that the IIP3 obtained from the PSS simulations, was the same, with a fixed input power of -20dBm.

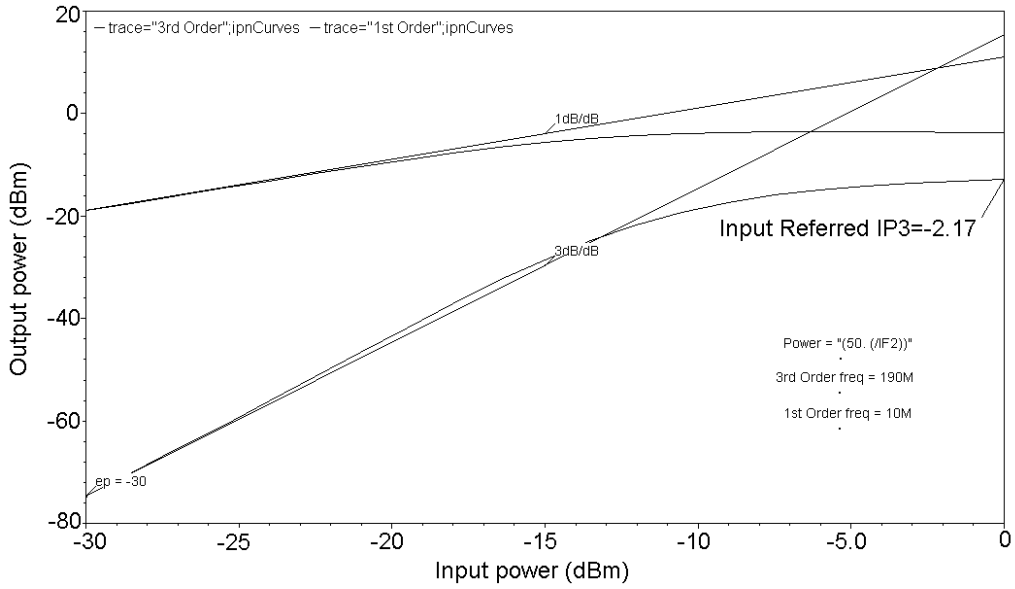


Figure 7.22: IIP3 simulation - downconversion mixer.

7.3.3.4 Noise analysis

The noise figure (NF) of the mixer was obtained by using the *pnoise* option in the PSS simulations (Figure 7.23). The noise figure is related to the output noise at the IF port referred back to the input RF port.

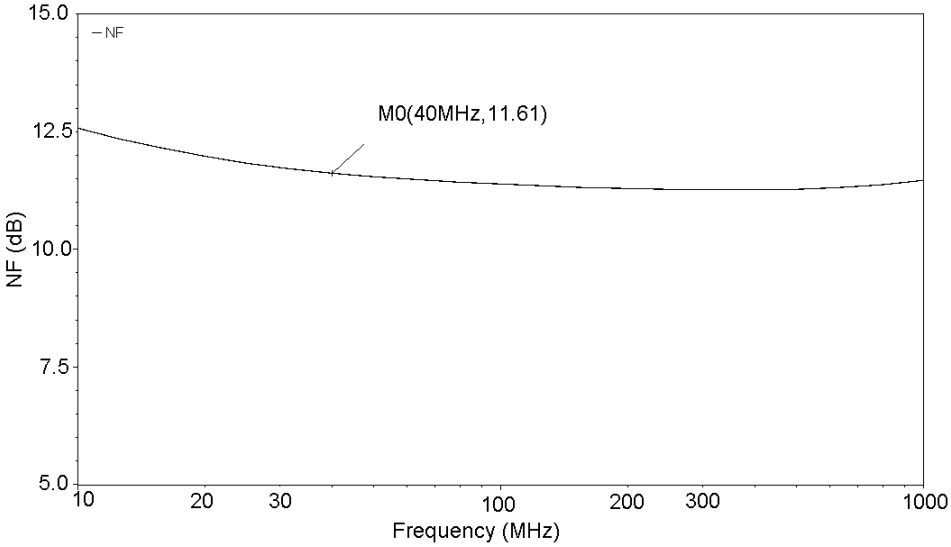


Figure 7.23: Noise figure simulation results – down-conversion mixer.

7.3.3.5 Performance summary

Table 7.4 summarizes the mixer simulation performance for both schematic and extracted versions of the design, under a fixed input and LO frequencies. A 4.7bB conversion gain, 12dB noise figure, and -2.5dBm IIP3 are obtained. The mixer core consumes 5mA at a power supply of 1.8V (the output buffer consumes about 5mA). Considering these performance parameters, the mixer is appropriate to be used in our target system.

Table 7.4: Down-conversion mixer simulation performance summary.

	Schematic	*Extracted*
IF1 (Hz)	1.4G	
LO (Hz)	1.36G	
IF2 (Hz)	40M	
CG (dB)	5	4.7
NF (dB) @40MHz	11.6	11.88
IIP3 (dBm)	-2.2	-2.5
Power cons. (mW)	20.5 (10.1 – mixer, 10.4 – buffer)	18 (9 – mixer, 9 – buffer)

7.4 Variable gain amplifier design

The 40MHz variable gain amplifier (VGA) is constructed with three operational transconductance amplifiers (OTA) in cascade so more than 70dB of gain variation can be achieved. Figure 7.24 shows the block diagram of the overall 3-stage VGA, where a buffer stage is added for the convenience of measurements.

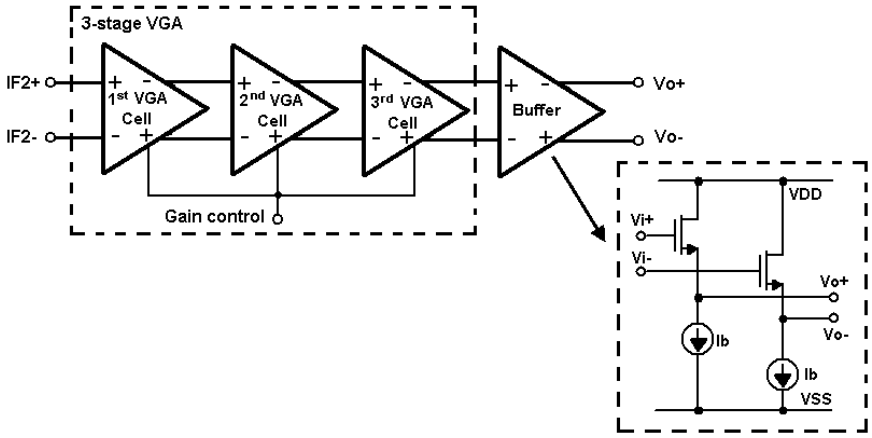


Figure 7.24: Complete block diagram of the 3-stage VGA.

The OTA, showed in Figure 7.25, is composed by a differential pair with common mode feedback and four cross-coupled control transistors. *Vc* and *Vr* are used to control the cross coupling between the two differential ends, controlling the gain. To prevent this cell from being saturated due to its high gain and input offset voltage, an offset cancellation circuitry is used.

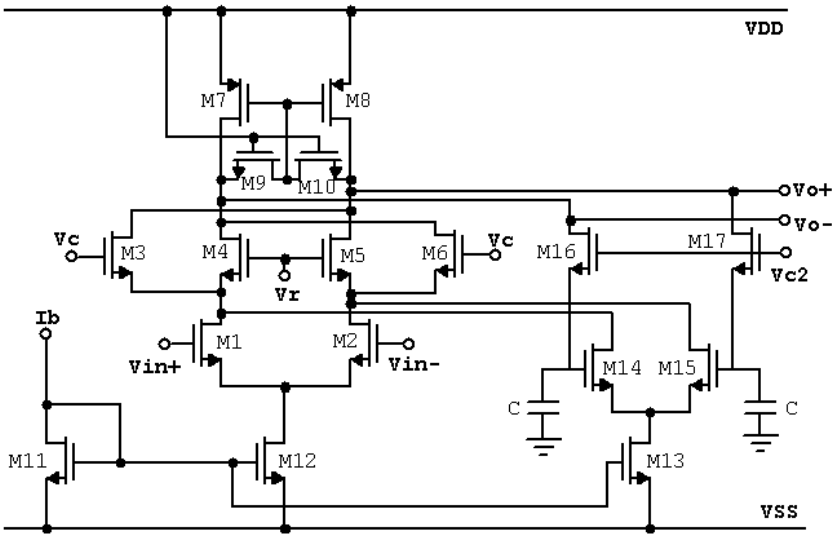


Figure 7.25: Circuit schematic of the OTA.

7.4.1 Design procedure

The 3-stage VGA was analyzed and designed in IBM 0.18µm CMOS process using the g_m/I_D design method. It must provide a 70bB gain range, 20dB NF, and 5dBm OIP3, with minimum power dissipation. The gain at 40MHz for each OTA stage is specified to be 23dB. The complete design procedure of the OTA is described as follows.

7.4.1.1 Small-signal analysis

As shown in Figure 7.25, the OTA is composed by amplifier stage and an offset cancelation stage with a negative feedback. The resulting small-signal model is illustrated in Figure 7.26a.

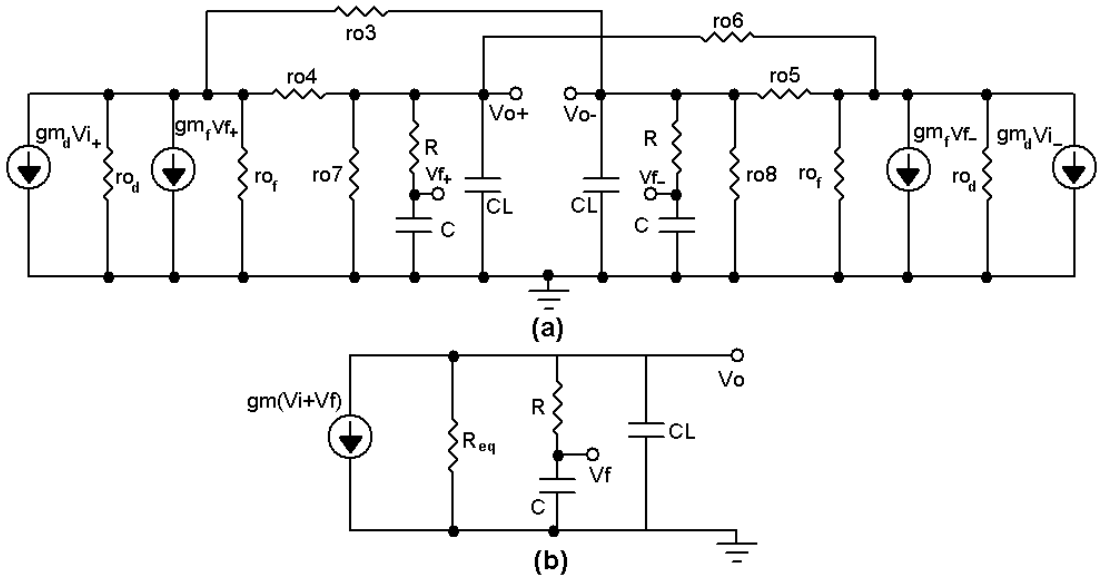


Figure 7.26: Small-signal model for the OTA.

Assuming that $gm_d = gm_f$, Req as the equivalent resistance of the variable gain stage, and the lowpass filter in the offset cancelation stage is formed by resistors R (M16/M17) together with the capacitors C, the small-signal model can be simplified as illustrated in Figure 7.26b.

Thus, the overall transfer function can be found as

$$H(s) = \frac{gm \cdot Req}{(1 + gm \cdot Req)} \cdot \frac{1 + (R \cdot C) \cdot s}{\left(\frac{Req \cdot CL \cdot R \cdot C}{1 + gm \cdot Req}\right) s^2 + \left(\frac{Req \cdot CL + Req \cdot C + R \cdot C}{1 + gm \cdot Req}\right) s + 1} \tag{7.10}$$

where

$$\omega_o = \sqrt{(1 + gm \cdot Req) \cdot \omega_{-3db,VG} \cdot \omega_{-3db,f}} \tag{7.11}$$

and

$$\omega_{-3db,VG} = \frac{1}{Req \cdot CL} \quad , \quad \omega_{-3db,f} = \frac{1}{R \cdot C} \tag{7.12}$$

$\omega_{-3db,VG}$and $\omega_{-3db,f}$ are the -3dB frequencies of the amplifier and feedback stages, respectively. The OTA can be considered as a two-pole system with a center frequency at ω_o, which can be set to 40MHz by properly designing $\omega_{-3db,f}$.

7.4.1.2 Block design using the g_m/I_D method

The g_m/I_D design method was applied to the synthesis of OTA. The complete design procedure is demonstrated as follows:

- Considering signal level and power specifications, the bias current in each stage was set to 500µA;
- The g_m/I_D ratio of the input differential pair and the cross-coupled transistors were set to 8 and 4, respectively, in order to achieve the maximum gain requirement of 24dB at 40MHz;
- The current mirror and the load transistors should operate in strong inversion to guarantee good matching and noise properties. Thus, g_m/I_D ratio was set to 8;
- For the CMFB circuitry, in order to guarantee stable bias conditions, the transistors must operate in the linear region (strong inversion - g_m/I_D ratio of 3);
- In order to obtain a tradeoff among power, area, noise and output offset, the g_m/I_D ratio of the negative feedback transistors was set to be the same as the input differential pair, where the DC gain is about 0dB. The lowpass filter cutoff frequency was set to be around 40MHz;
- The transistors lengths L are determined by a trade-off between area and DC gain requirement (due to the dependence of the Early voltage on the transistor length).

The designed values for the transistors sizes and circuit components are shown in Table 7.5.

Table 7.5: OTA component summary.

Component Name	*Value*	g_m/I_D
M1, M2 (W/L)	12*(2µm/0.6µm)	8
M3, M4, M5, M6 (W/L)	8*(5µm /1µm)	4
M7, M8 (W/L)	32*(12µm /1µm)	8
M9, M10 (W/L)	(0.22µm /8µm)	-
M11, M12, M13 (W/L)	10*(27µm /1µm)	8
M14, M15 (W/L)	12*(2µm /0.6µm)	3
M16, M17 (W/L)	(1.5µm /2µm)	3
C	500fF (MIM HK cap – 16 x 15.5 μm^2)	-

7.4.2 Layout implementation

The circuit layout design was completed using *Cadence Virtuoso Design Editor Environment* in IBM 0.18µm CMOS process with 6 metal layers. Each OTA cell was laid out in cascade, resulting in the 3-stage VGA final layout showed in Figure 7.27.

The input differential pairs and current mirrors were implemented using a common-centroid configuration. The capacitors were implemented as a single HiK-dielectric MIM (metal-insulator-metal) capacitors (C=500fF), considering the available component library of the IBM 0.18µm process design kit. In the buffer stage, a triple well source follower buffer transistor was used, allowing the transistor bulk to be tied to the source.

The architecture is fully differential and layout as symmetrically as possible to minimize the mismatch in the signal paths. The total area of the implemented circuit is 34,840µm^2.

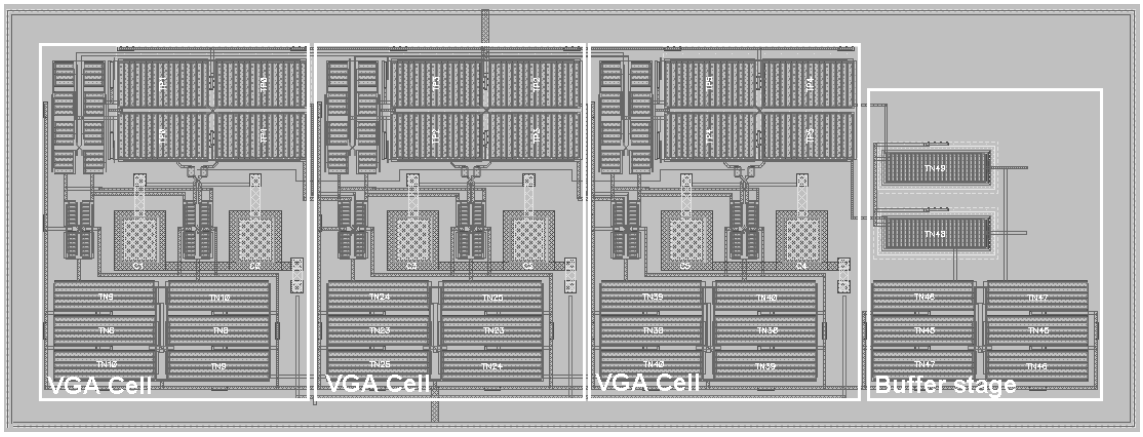


Figure 7.27: 3-stage VGA final layout.

7.4.3 Simulation results

The circuit performance was verified through electrical simulations using the *Spectre* simulator tool and the BSIM3v3 foundry supplied model. The simulation setup used to simulate the VGA is shown in Figure 7.28.

In the following subsections, the main simulated curves which characterize the performance of the VGA (schematic version) are presented, considering an input sinusoidal signal at 40MHz, where *Vc* and *Vr* are used to control the gain.

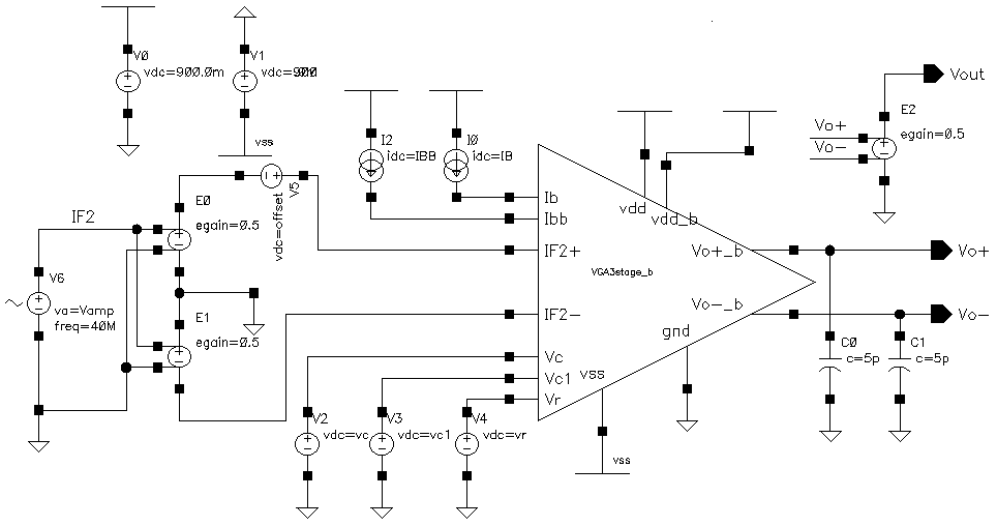


Figure 7.28: VGA simulation testbench.

7.4.3.1 AC analysis

The simulated frequency response of the VGA with maximum gain (Vr=0.6V, Vc=0.2V) is shown in Figure 7.29. The maximum gain is 77dB at 41.7MHz. It demonstrates that with the offset cancellation circuitry, the VGA is two-pole system with a center frequency at 40MHz.

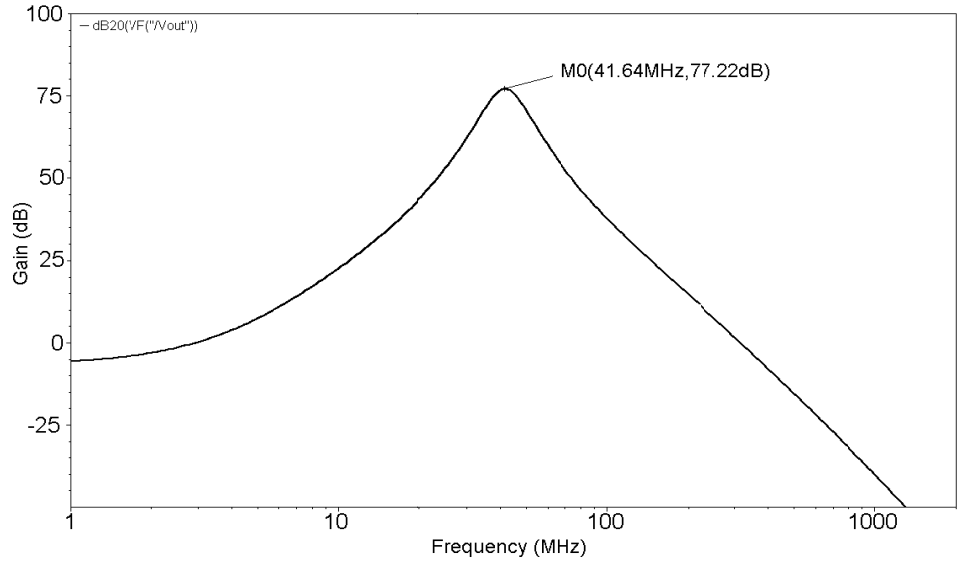


Figure 7.29: VGA frequency response – Vr=0.6V, Vc=0.2V.

The simulation of gain control range of the VGA at 40MHz is shown on Figure 7.30. As the control voltage (Vc) decreases, the gain increases. The maximum gain is 77dB, varying continuously from 0dB to 70dB, corresponding to a control voltage range from 0.2V to 0.55V (Vr=0.6V).

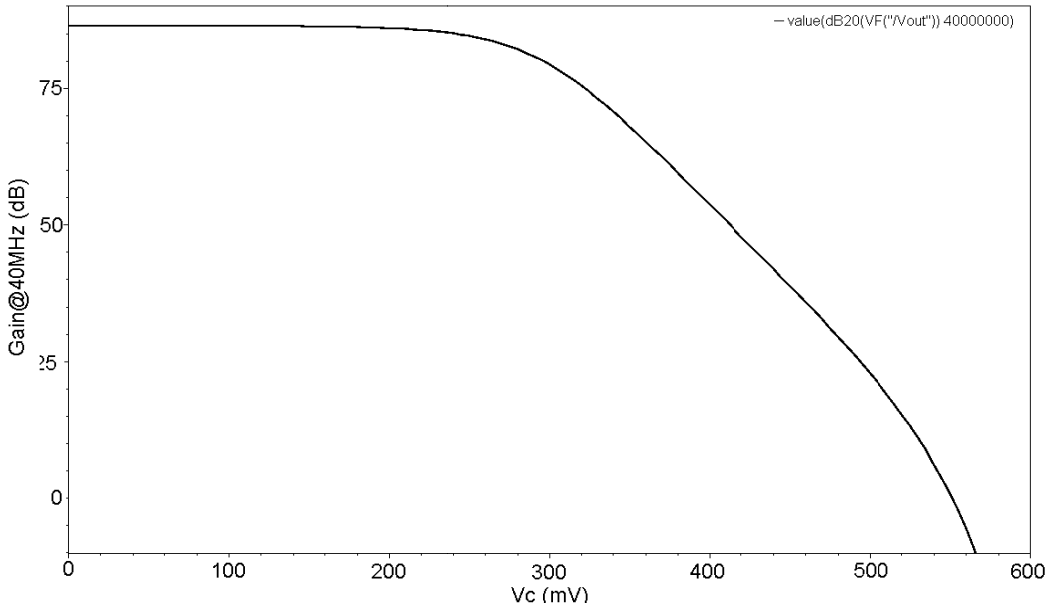


Figure 7.30: Gain control range of the VGA at 40MHz – Vr=0.6V.

Figure 7.31 shows the gain of the VGA as a function of the input offset voltage. With the offset cancellation circuitry, the VGA is insensitive to the input offset voltage. From this simulation, the maximum tolerable offset voltage of the VGA, defined as the input offset voltage that causes a 1dB decrease in the gain, can be obtained, which is 33mV.

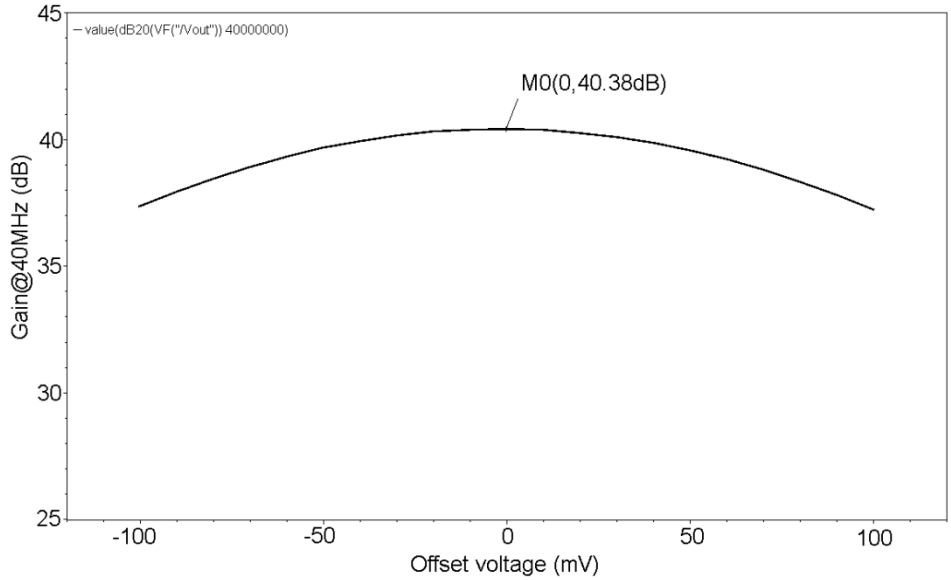


Figure 7.31: Gain variation due to the input offset voltage of the VGA at 40MHz – Vr=0.6V, Vc=0.4V.

7.4.3.2 Linearity analysis

In order to obtain a linearity simulation of the VGA, a two-tone test was performed using two input signals at 39.5MHz and 40.5MHz. As shown in Figure 7.32, the OIP3 of the VGA is about 5dBm. The VGA achieves a noise figure (NF) of 20dB.

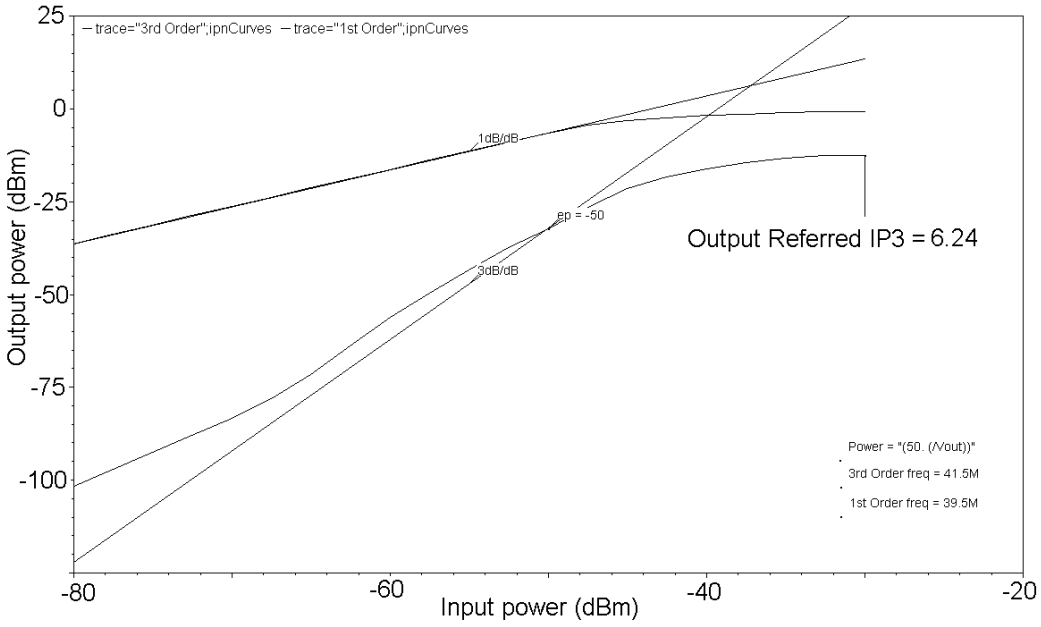


Figure 7.32: OIP3 of the VGA at 40MHz – Vr=0.6V, Vc=0.4V.

7.4.3.3 Noise analysis

The noise figure of the VGA was obtained by using the *pnoise* option in the PSS simulations (Figure 7.33). The noise figure is related to the output noise at the output referred back to the input.

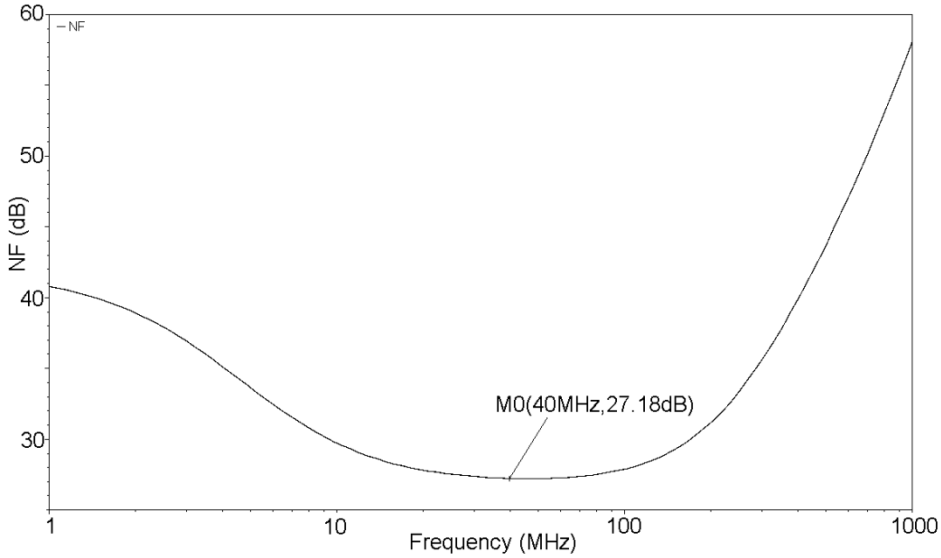


Figure 7.33: NF of the VGA– Vr=0.6V, Vc=0.4V.

7.4.3.4 Transient analysis

In order to obtain the transient response of the VGA, a sinusoidal input signal of 40MHz of frequency, and amplitude of 5.65mVp (-35 dBm) was applied on the input, with the gain set to be 35dB (Vc=0.44V). Figure 7.34 show the transient curves, of the input and output signals, respectively.

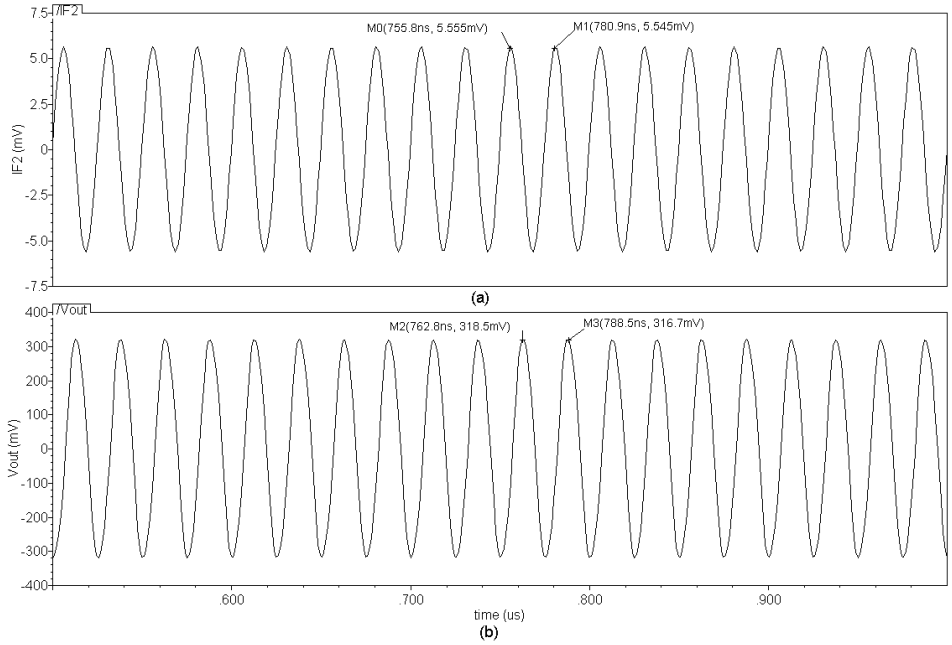


Figure 7.34: VGA transient analysis, 35dB gain: input (a) and output (b) curves.

7.4.3.5 Performance summary

Table 7.6 summarizes the 3-stage VGA simulation performance for both schematic and extracted versions of the design. Results shows that the VGA has a continuous gain control range of 70dB, NF of 20dB, OIP3 of 5dBm, consuming 8mW from a 1.8V supply.

Table 7.6: 3-stage VGA simulation performance summary.

Design metrics	*Schematic*	*Extracted*
Gain control range (dB)	0 - 78	0 - 75
NF (dB)	27	26.2
OIP3 (dBm)	6.2	6.7
Offset cancellation (mV)	57	60
Output Swing (mVpp) (@35dB gain)	700	600
Power cons. (mW)	18.8 (8.2-VGA, 10.6-buffer)	18.6 (8-VGA, 10.6-buffer)

7.5 Front-end design

Considering the previous analysis of each building block, the entire dual-conversion heterodyne front-end architecture was designed.

Figure 7.35 shows the complete block diagram of the front-end circuitry. The overall system is constructed with three building blocks in cascade, where an extra AC-coupled stage is placed between both mixers in order to properly bias the down-conversion mixer stage. A buffer stage is also added for the convenience of measurements.

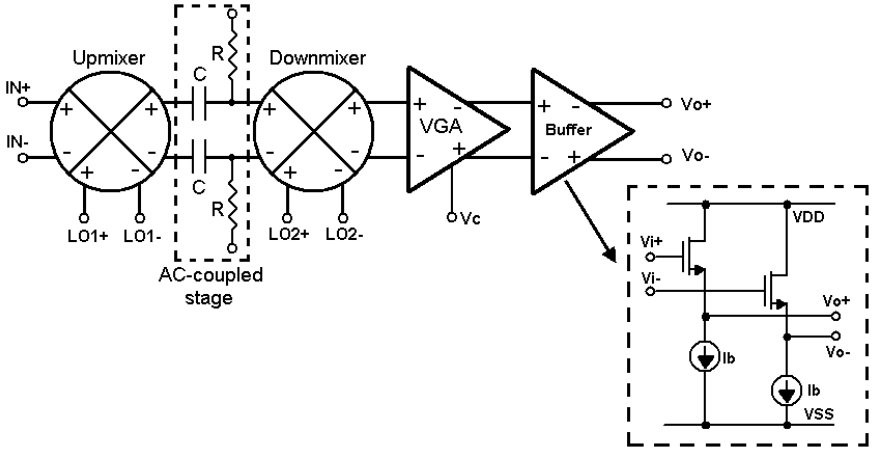


Figure 7.35: Block diagram of the RF front-end.

7.5.1 Circuit implementation

All circuits were designed and implemented as stand-alone building blocks (as previously discussed) and as a part of the entire front-end, in IBM 0.18µm CMOS process with 6 metal layers.

All the building blocks were laid out to be fully differential and laid out as symmetrically as possible to minimize the mismatch in the signal paths. The physical spaces in the inductors and the building blocks were carefully chosen to be small enough to reduce parasitics and area, and at the same time far enough apart to minimize coupling and contamination of the RF signals. Figure 7.36 shows the layout of the whole front-end, with a total area of 0.77mm^2.

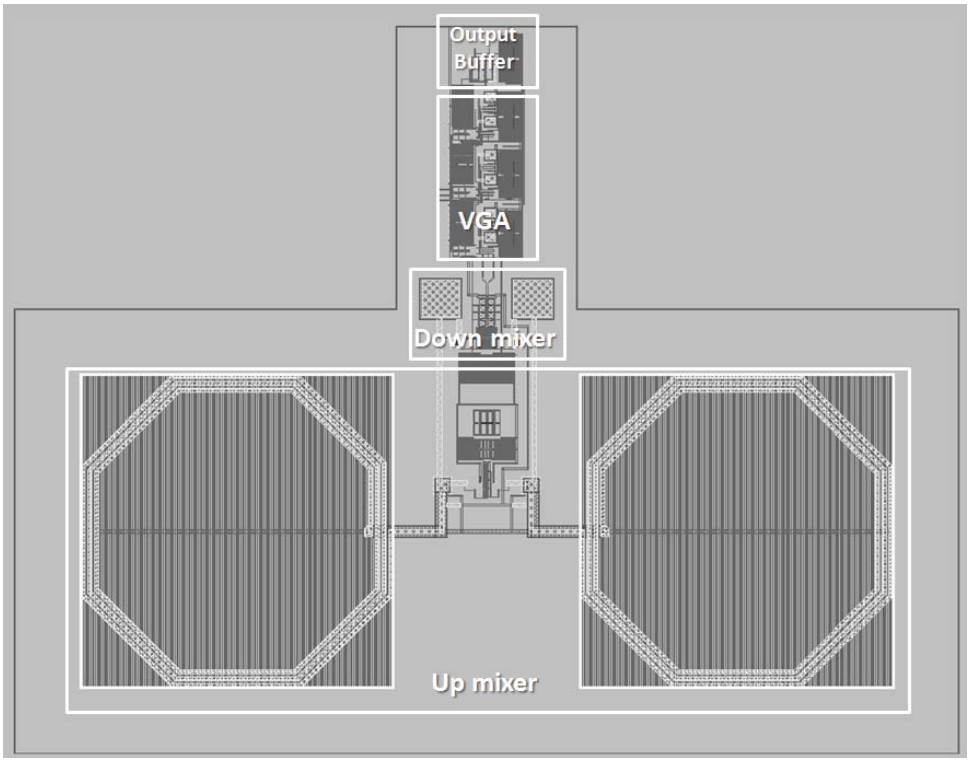


Figure 7.36: Layout of the RF front-end.

7.5.2 Simulation results

The circuit performance was verified through electrical simulations using the *Spectre* simulator tool and the BSIM3v3 foundry supplied model. The simulation setup used to simulate the front-end is shown in Figure 7.37.

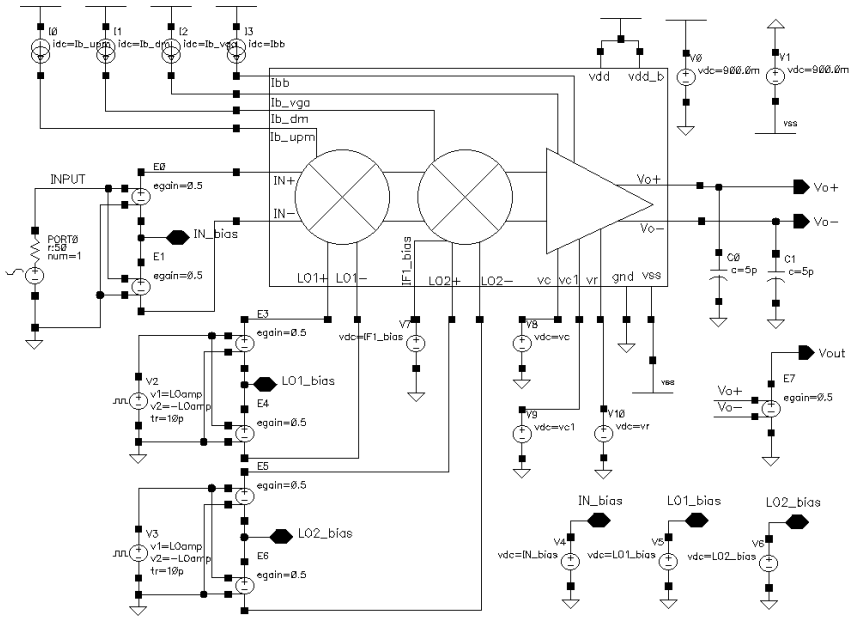


Figure 7.37: Front-end simulation testbench.

In the following subsections, the main simulated curves which characterize the performance of the front-end (schematic version) are presented. A sinusoidal signal of -40dBm at 450MHz is applied to the input, while two square signals of 200mVpp of amplitude are applied at different frequencies (950MHz and 1.36GH for LO1 and LO2, respectively). The gain in the VGA stage is set in order to provide a 200mVpp signal at 40MHz in the output of the system (35dB gain).

7.5.2.1 PSS analysis

The periodic steady-state analysis is employed to characterize the conversion gain of the system. The voltages at the output and input ports in dB20 are given in Figure 7.38.

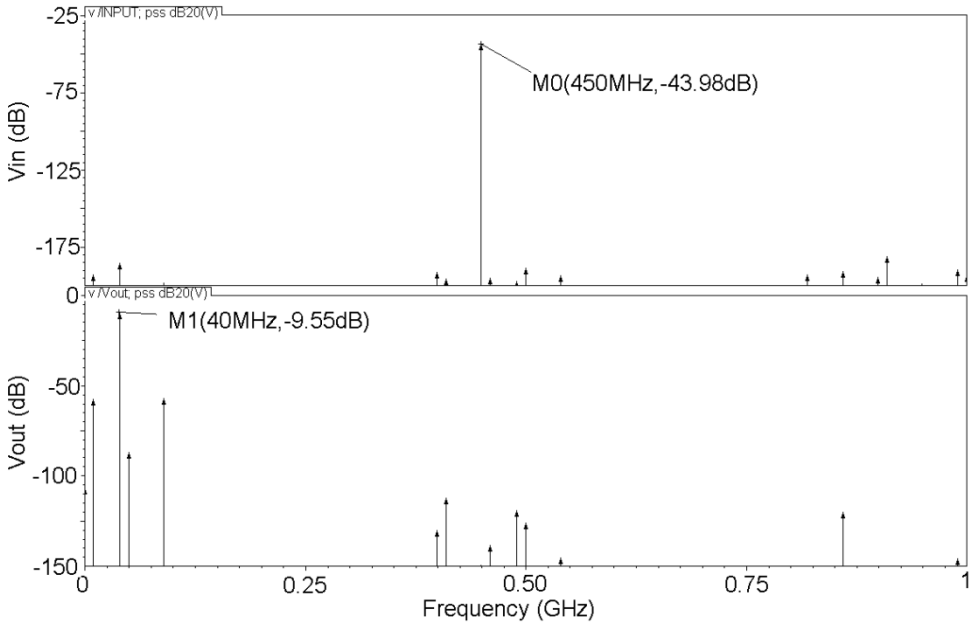


Figure 7.38: Front-end PSS simulation results.

Thus, the conversion gain is

$$CG = -9.545 - (-43.98) = 34.435dB \tag{7.13}$$

7.5.2.2 Linearity analysis

For the IIP3 simulation, two equal tones at (*450+10)MHz* and (*450-10*)*MHz* are given at the input port, as the two-tone intermodulation test method previously discussed.

Figure 7.39 shows the overall IIP3 curve sweeping the input power of an input signal of 450MHz. It is reasonable to estimate the IIP3 using 30MHz as the output fundamental and 70MHz as the output IM3. It was further observed that the IIP3 obtained from the PSS simulations, was the same, with a fixed input power of -20dBm.

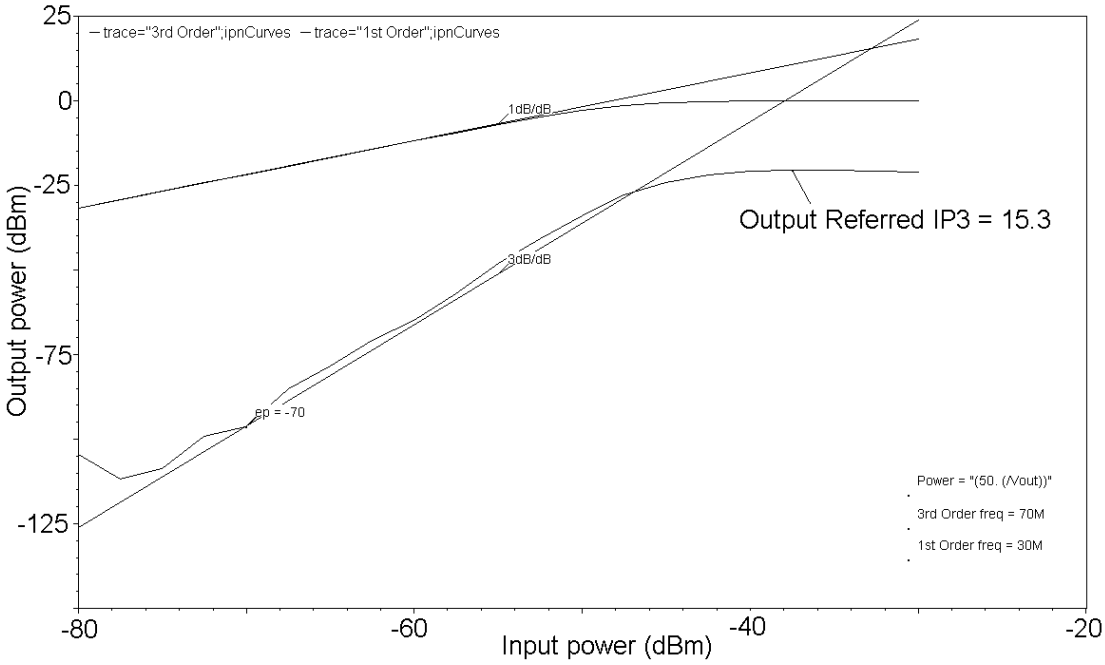


Figure 7.39: IIP3 intercept point front-end simulation.

7.5.2.3 Transients analysis

The transient simulation of the whole front-end is shown in Figure 7.40. A signal at 450MHz and a signal level of -40dBm is applied at the input and VGA gain is set to 35dB in order to provide a 200mVpp signal at 40MHz in the output of the system.

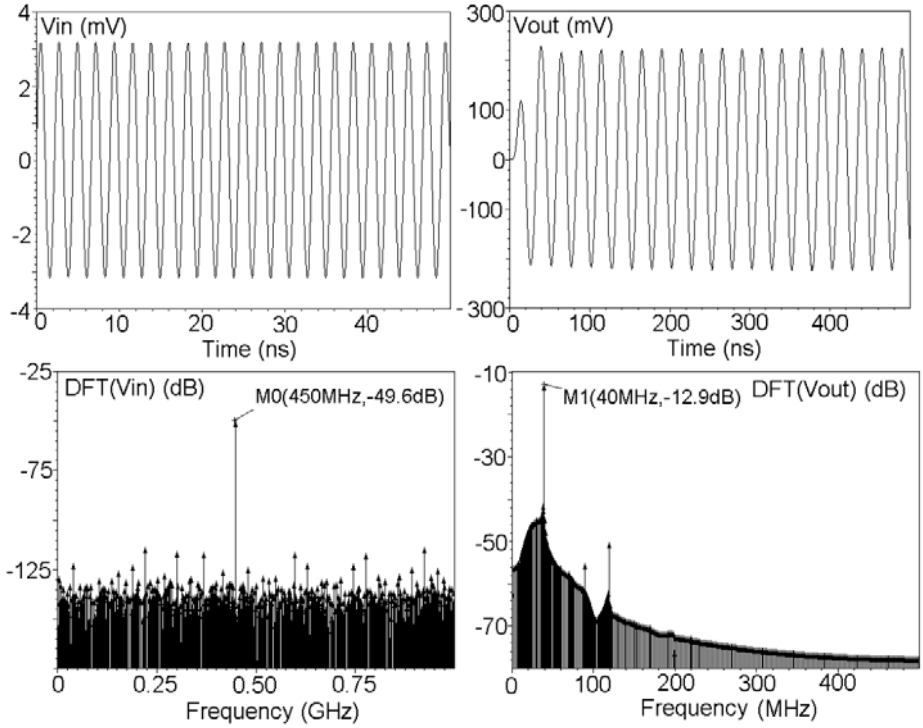


Figure 7.40: Transient simulation of the front-end (input signal of -40dBm at 450MHz): (a) input signal, (b) FFT of the input signal, (c) output signal, (d) output spectrum.

From this simulation the sensitivity and the output voltage swing can also be obtained. The sensitivity of the system, defined as the minimum input signal level which the system can detect at the output, is 50µVpp. The output voltage swing was obtained at a fixed input signal of 100µVpp of amplitude, where the VGA gain is adjusted (high gain mode) until the output signal saturates. The maximum output swing of the system was simulated to be 650mVpp.

7.5.2.4 Performance summary

Table 7.7 summarizes the front-end simulation performance for both schematic and extracted versions of the design, under different input and LO frequencies.

Table 7.7: RF Front-end simulation performance summary.

Design metrics	*Schematic*	*Extracted*
Frequency range (MHz)	48 - 960	
Gain control range (dB)	0 - 75	0 - 70
Sensitivity (µVpp)	20	80
IIP3 (dBm)	-28	-29
Output Swing (mVpp) (@35dB gain)	700	650
Power cons. (mW)	44.6 (7.16 - buffer)	38.22 (7.2 - buffer)

Results show that the whole front-end system achieves an overall sensitivity of -70dBm, an IIP3 of -28dBm, sensitivity of -78dBm, and a power consumption of 40mW, with the input frequency varying from 48MHz to 960MHz.

7.6 Discussion

This chapter discussed the design of the target RF front-end system, with 2 active mixers and a variable-gain block, suitable for the mixed-signal analog interface. The system was designed using the specifications related to three different target applications previsouly discussed.

The building blocks and the front-end were designed in IBM 0.18µm CMOS process without any off-chip components. Post-layout simulation results shows that the whole front-end system achieves an overall sensitivity of -70dBm, an IIP3 of -28dBm, and a NF of 25dB, with a power consumption of 40mW, with the input frequency varying from 48MHz to 960MHz.

Considering these simulated performance parameters, the system is appropriate to be used in our target system. Each building block together with the entire front-end system was prototyped in a chip. The measurements will be presented and analyzed in the next chapter.

8 RF BUILDING BLOCKS CHIP: EXPERIMENTAL RESULTS

In this chapter, the implementation of the discussed building blocks (mixers, VGA, and the complete front-end) in a single chip will be discussed. Each block will be characterized by experimental measurements.

8.1 System chip

The system chip, with all the discussed analog/RF blocks and some test scructures, was fabricated in IBM 0.18µm CMOS process through MPW MOSIS. The chip was prototyped in a 64-pin QFN package, with a total area (including pads) of 6.8mm^2. The die micrograph of the chip is shown in Figure 8.1. Details about the areas of each block are in Table 8.1.

Table 8.1: System chip area breakdown.

Block	*Area (mm^2)*
Up mixer	0.71
Down mixer	0.021
VGA	0.035
Front-end	0.77
VCO	0.022
Ring oscillator	0.0073
Test structures	1.248
Pad ring	1.76
Unused space	2.226
Total area	6.8

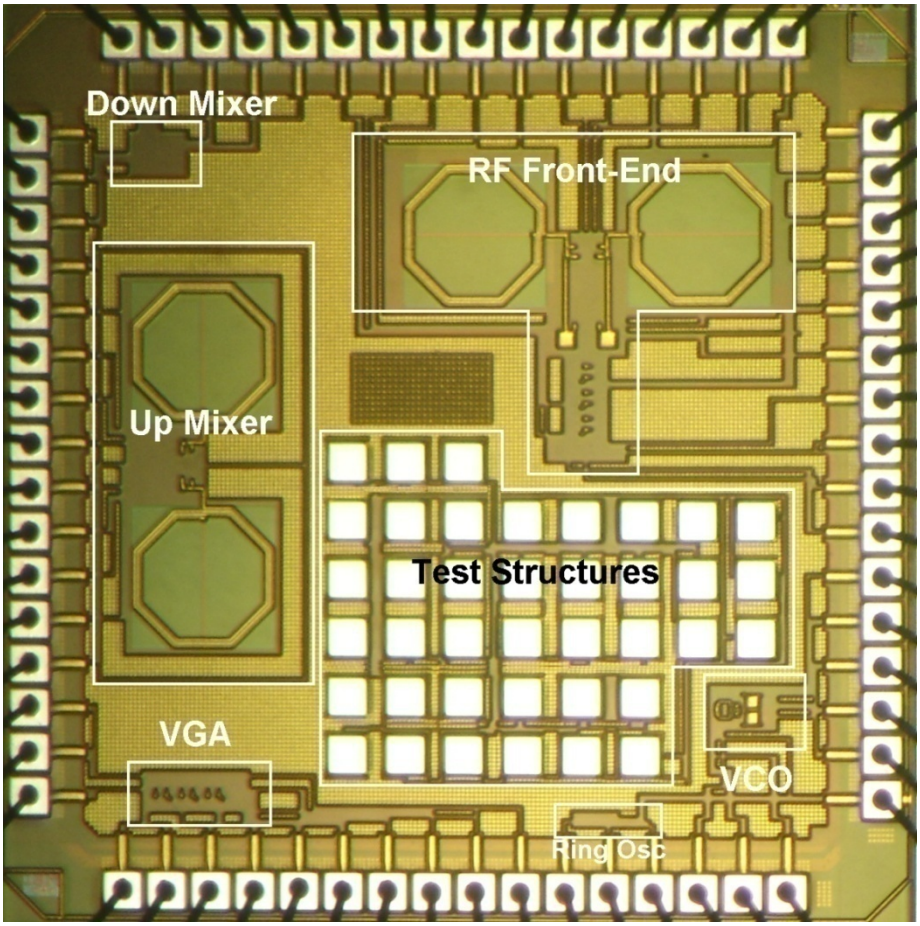


Figure 8.1: System chip die micrograph.

8.2 PCB for testing

The chip was tested in a 190mm x 99mm double-face printed circuit board (PCB). The PCB uses FR-4 material with thickness of 0.8mm, in order to have reasonable tracks widths for inpedance matching at 1.4GHz. In order to create controlled impedance transmission lines on the PCB, the Microstrip technique was used. Photograph of the actual PCB is depicted in Figure 8.2.

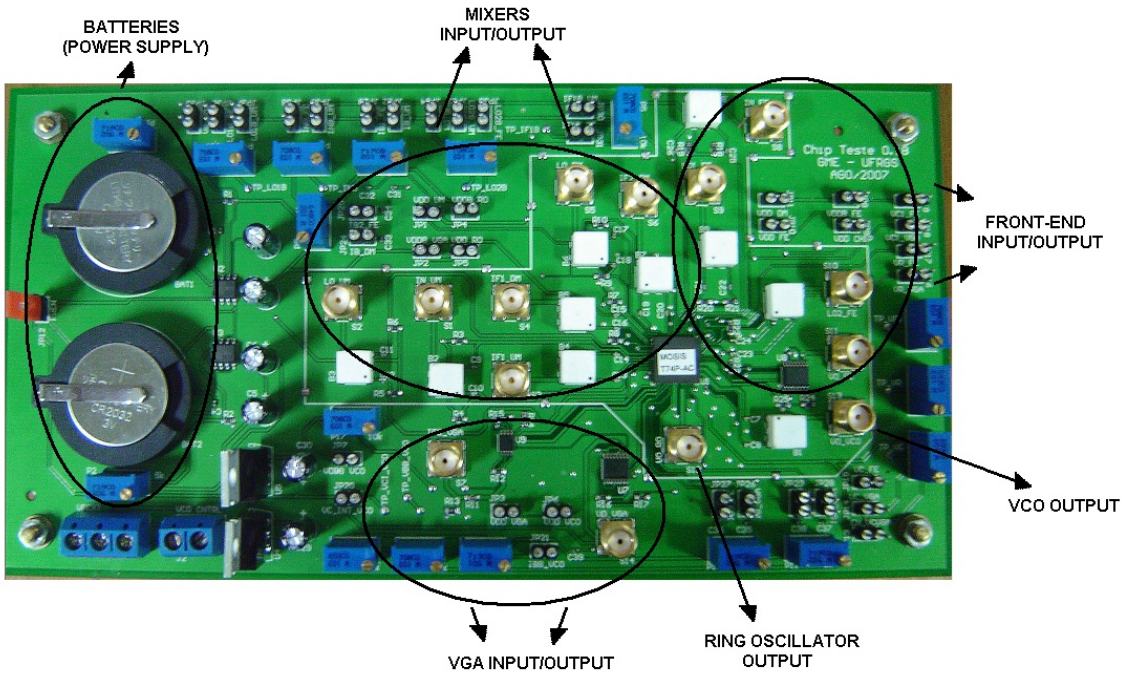


Figure 8.2: Photograph of the PCB for testing.

8.3 Experimental results

We now present the performance measurements of the discussed blocks obtained from the testing board previously described. All the results reported herein are an average of measurements on 3 encapsulated samples, each directly soldered in 3 different PCBs.

The input signals were generated by the Agilent E4438C ESG Vector Signal Generator and the Rohde & Schwarz SM300 Signal Generator (maximum input power of -26dBm). The output signals were measured using the Rohde & Schwarz FS300 Spectrum Analyzer.

8.3.1 Technology characterization

The first step is to characterize the design CMOS process. Here, we concentrate in two parameters: the g_m/I_D curve and the gate delay.

8.3.1.1 The g_m/I_D curve

Figure 8.3 shows the g_m/I_D versus $I_D/(W/L)$ fundamental curves obtained through experimental data for the IBM 0.18µm CMOS process. Through non-encapsulated die samples, the I_D vs. V_{GS} DC curves were obtained for both NMOS and PMOS transistors of $W/L=1$ (W=1µm, L=1µm), where $V_D=V_G= 0$ *to* $1.8V$ and $V_S=V_B= 0V$. From equation 7.1, the g_m/I_D vs. $I_D/(W/L)$ curve is obtained.

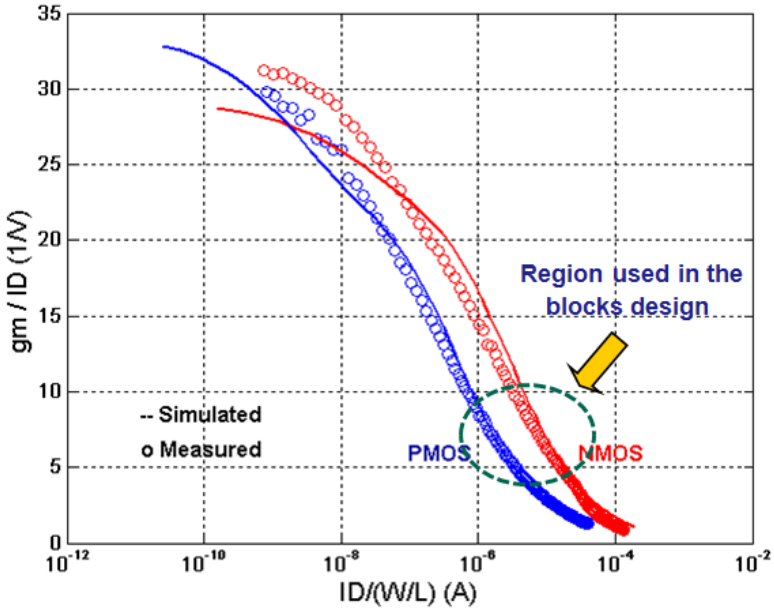


Figure 8.3: Simulated and measured g_m/I_D versus $I_D/(W/L)$ curves for NMOS and PMOS transistors in IBM 0.18µm CMOS process.

8.3.1.2 Ring oscillator

In order to verify the typical gate delay for inverters in this process, a ring oscillator was characterized. A 19-stage ring oscillator circuit was implemented. It was verified through experimental data that at a typical power supply voltage (± 0.9V) the oscillation frequency is 710MHz, resulting in an average gate delay of *37.9ps*. Figure 8.4 shows the measured output spectrum of this block at a typical power supply voltage. Figure 8.5 shows the oscillation frequency and average gate delay dependencies on the power supply voltage.

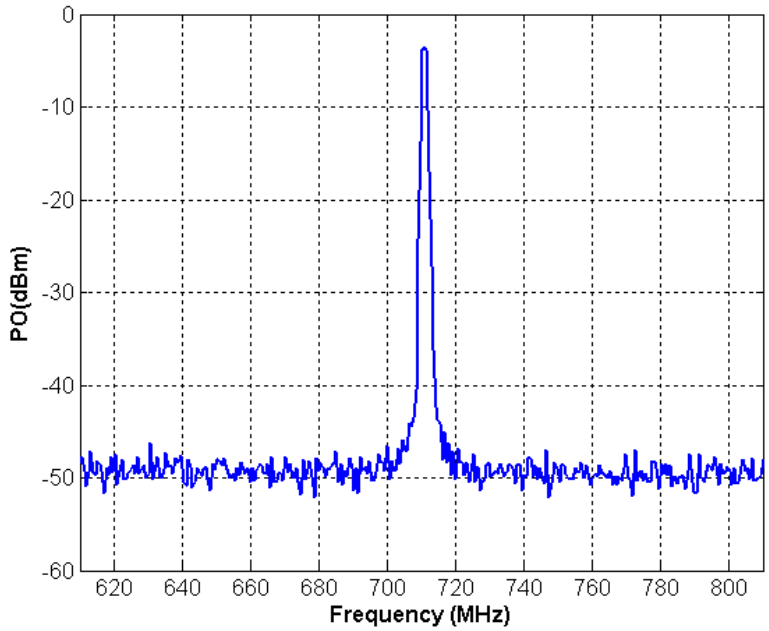


Figure 8.4: Ring oscillator output spectrum at a typical power supply voltage (± 0.9V).

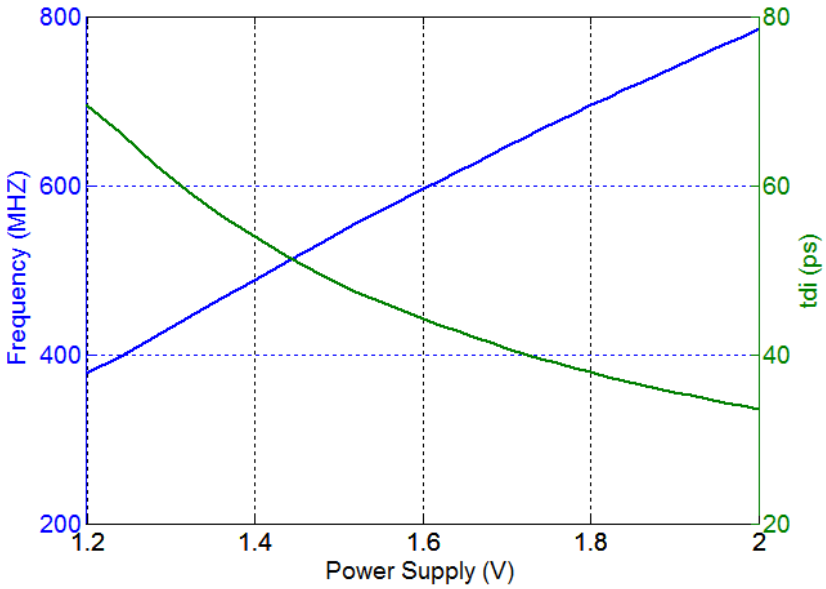


Figure 8.5: Ring oscillator measured oscillation frequency and average gate delay vs. power supply.

8.3.2 Mixers

The testing setup of the designed mixers is illustrated in Figure 8.6. Due to limitations in the test equipments, only functional measures could be performed.

Both sinusoidal input signals (IN and LO) are generated by the Vector Signal Generators previously described. A power of -30dBm is applied to the input, while a power of -10dBm is applied to the LO. The frequency of each output is adjusted according the mixer configuration.

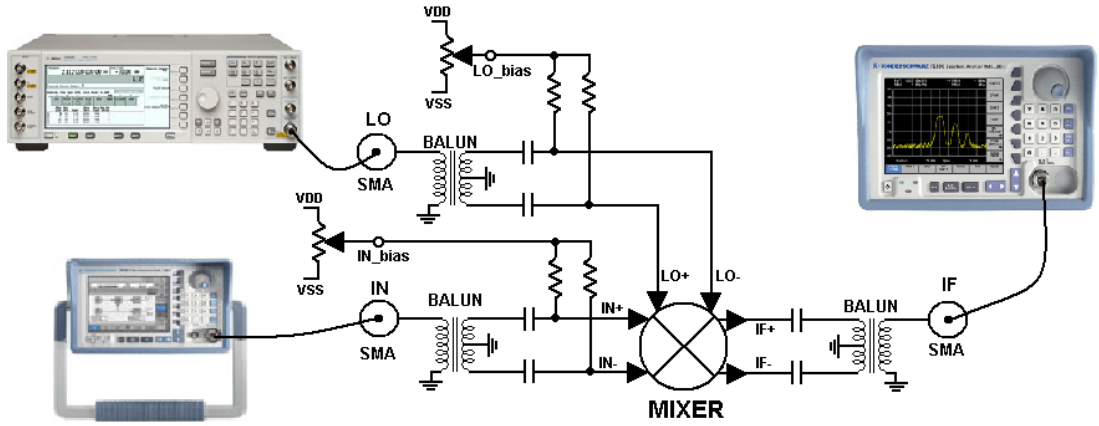


Figure 8.6: Mixers test setup.

8.3.2.1 Up-conversion mixer

Figure 8.7 shows the output spectrum of the up-conversion mixer in typical condition, i.e., where an input signal of 450MHz and a LO signal of 950MHz are applied to the block, resulting in an output signal at 1.4GHz.

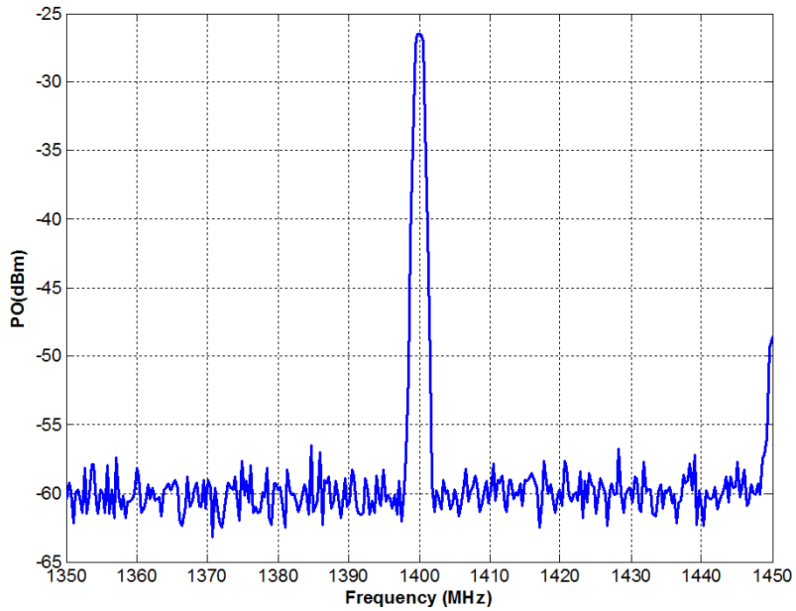


Figure 8.7: Measured output spectrum of the up-conversion mixer – typical condition

To examine the up-conversion mixer LO power requirement, conversion gain was measured at 1.4GHz while sweeping the LO power (Figure 8.8). A peak conversion gain of about 4dB is achieved with -5dBm LO power. Reducing the LO power below -5dBm results in a considerable reduction of the conversion gain.

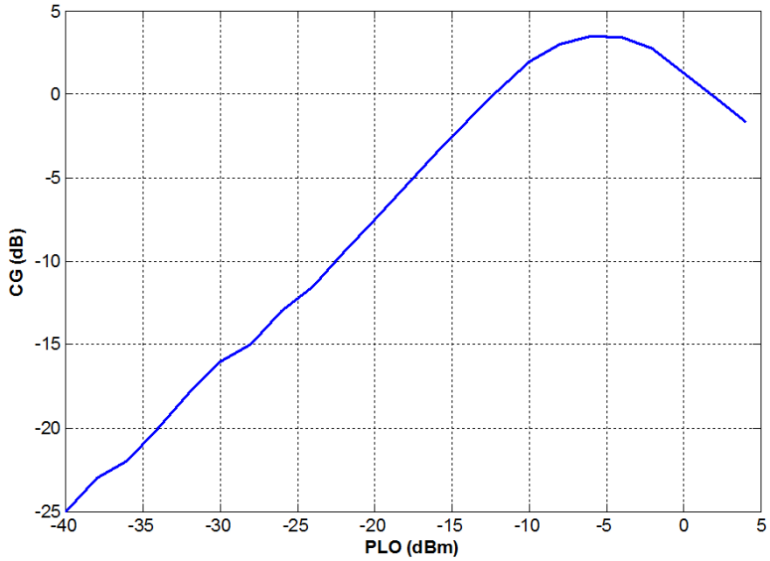


Figure 8.8: Measured CG vs. LO power of the up-conversion mixer – typical condition.

In order to examine the LC tank load variation of the mixer, conversion gain was measured while the input frequency was adjusted in order to obtain the maximum conversion gain, for the 3 different samples available. Figure 8.9 shows the results obtained, where for each sample there is a different peak conversion gain, i.e., a different tuned frequency of the LC tank load.

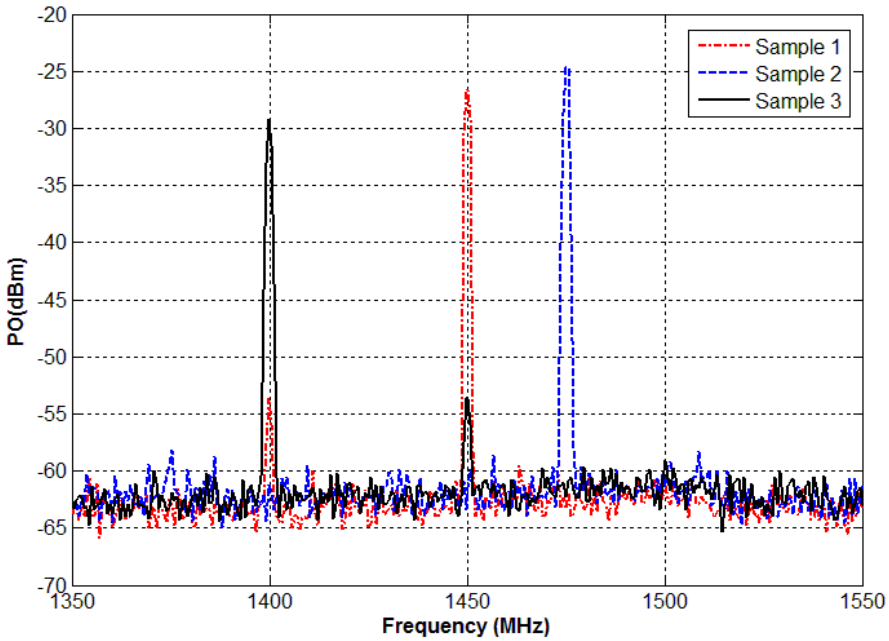


Figure 8.9: Measured output spectrum of the up-conversion mixer from 3 different samples – LC tank load variation.

The up-conversion mixer was also measured over a variety of input and LO frequencies. A 4dB conversion gain is obtained under the different target input frequencies. The DC power consumption of the mixer circuitry (core + buffer) was 17.2mA, at a power supply of ± 0.9V.

Table 8.2 summarizes the obtained measured performance of the up-conversion mixer, comparing with the previous obtained post-layout simulation, under different input and LO frequencies.

Table 8.2: Up-conversion mixer performance under different input frequencies – INpower=-30dBm.

			Post-layout simulation		**Measurement**	
FIN (Hz)	*LO (Hz)*	*IF1 (Hz)*	*CG (dB)* *LOpower=-10dBm* *IB=4mA* CL=5pF	Power cons. (mW)	***CG (dB)*** ***LOpower=-5dBm*** ***IB=3mA*** ***PCB load***	**Power cons. (mW)**
48M	1.352G		4		**3.8**	
108M	1.292G		4		**4**	
270M	1.130G		4		**3.9**	
450M	950M	1.4G	4.7	60.7	**4**	**31**
600M	800M		4		**4**	
869M	531M		4.3		**3.8**	
960M	440M		4.4		**4.4**	

8.3.2.2 Down-conversion mixer

Figure 8.10 shows the output spectrum of the down-conversion mixer in typical condition, i.e., where an input signal of 1.4GHz and a LO signal of 1.36GHz are applied to the block, resulting in a down-converted output signal at 40MHz. A 4dB conversion gain is achieved, while the mixer circuitry (core + buffer) consumes 8.1mA at a power supply of 1.8V.

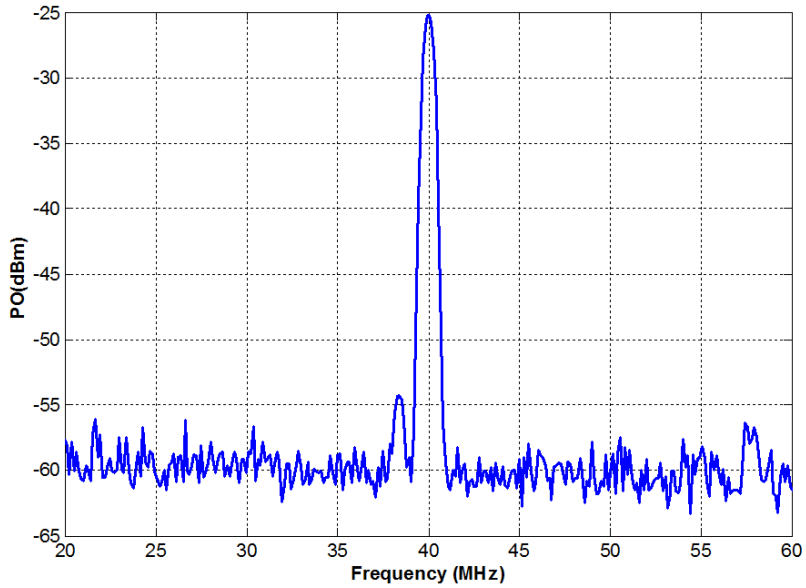


Figure 8.10: Measured output spectrum of the down-conversion mixer – typical condition

In order to examine the down-conversion mixer's LO power requirement, conversion gain was measured at 40MHz while sweeping the LO power (Figure 8.11). A peak conversion gain of about 5.2dB is achieved with +6dBm LO power. Reducing LO power below +2dBm results in a considerable reduction of the conversion gain.

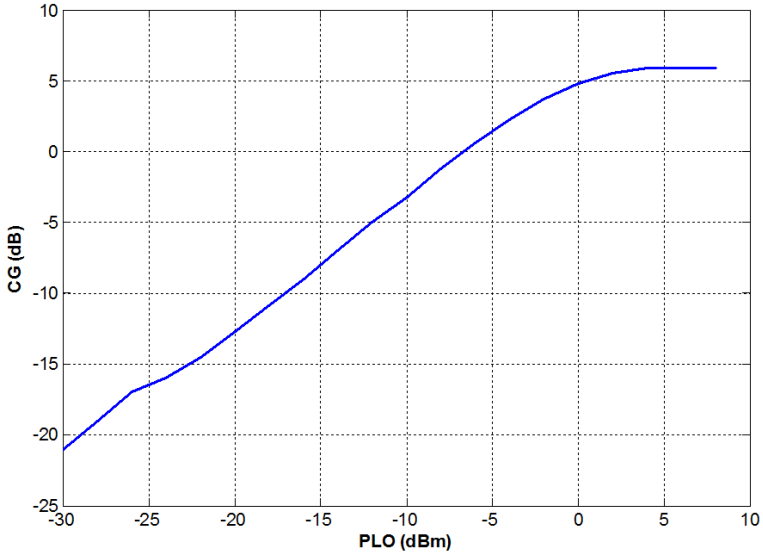


Figure 8.11: Measured CG vs. LO Power of the down-conversion mixer – typical condition.

Table 8.3 summarizes the obtained measured performance of the down-conversion mixer, comparing with the previous obtained post-layout simulations.

Table 8.3: Down-conversion mixer performance – INpower=-30dBm.

			Post-layout simulation		**Measurement**	
FIN (Hz)	*LO (Hz)*	*IF1 (Hz)*	*CG (dB) LOpower=-10dBm CL=5pF IB=3mA*	Power cons. (mW)	***CG (dB) LOpower=0dBm PCB load IB=3mA***	**Power cons. (mW)**
48M	1.352G	1.4G	4.7	18	**5**	**15**

8.3.3 VGA

Testing setup of the 3-stage VGA is illustrated in Figure 8.12. Additional commercial integrated circuits were implemented together in the PCB in order to test this block. Due to problems in the PCB soldering, only one encapsulated sample could be measured.

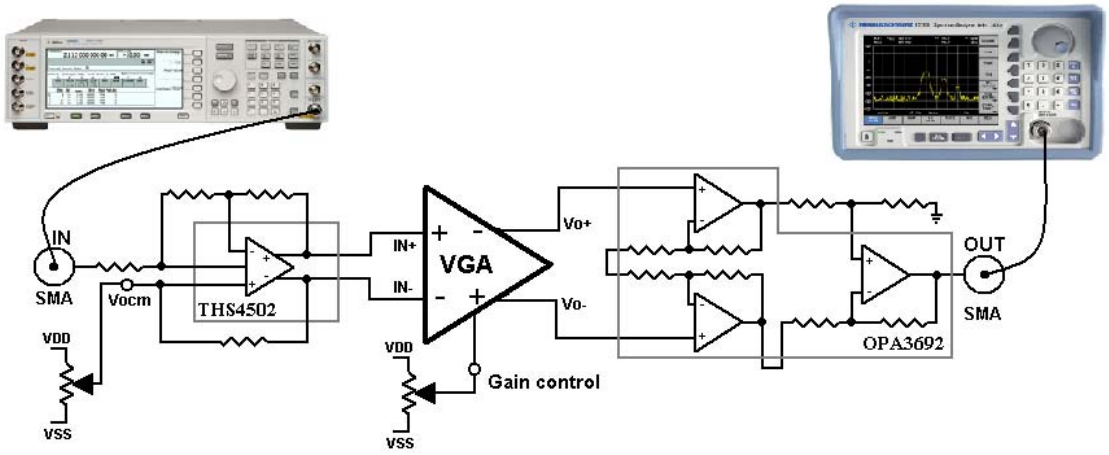


Figure 8.12: VGA test setup.

The measured frequency response of the VGA is shown in Figure 8.13. The gain at 40MHz is 70dB, and the maximum gain is about 72dB at 38MHz. The input signal generator was set to -80dBm in order to avoid saturation.

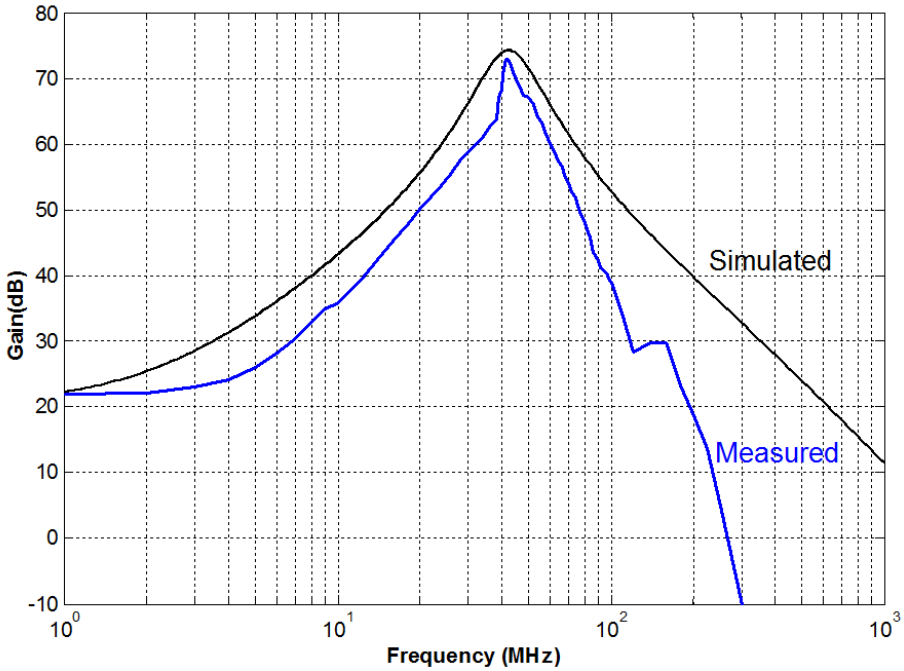


Figure 8.13: Measured and simulated frequency response of the VGA.

Measurement of the gain control range of the VGA at 40MHz is shown in Figure 8.14. As the control voltage decreases, the gain of the VGA increases. The maximum measured gain is about 70dB. The gain varies continuously from 0 to 70dB, corresponding to a control voltage (*Vc*) from 0.4V to 0.7V. Further decrease of the control voltage completely turns off the cross-coupling transistors, and the gain becomes constant.

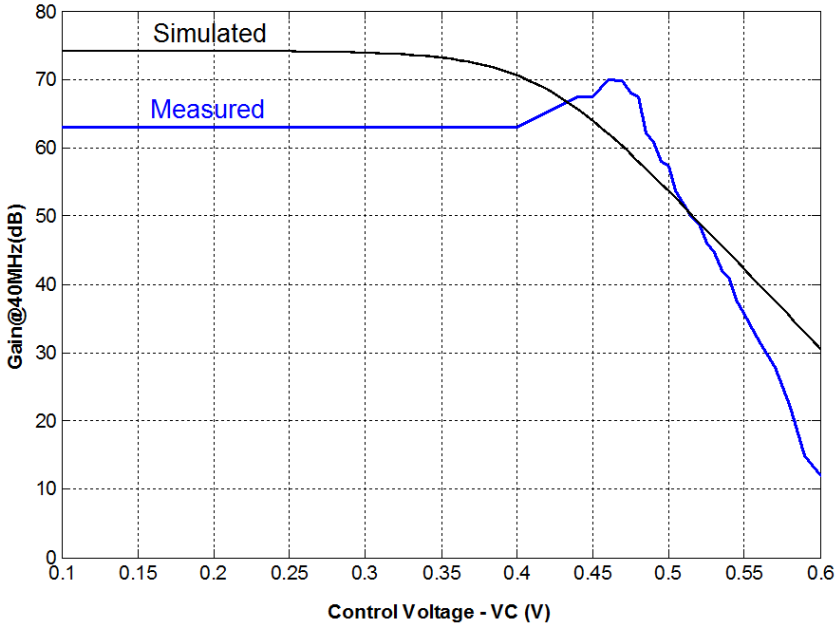


Figure 8.14: Measured and simulated gain control range of the VGA at 40MHz.

Figure 8.15 shows the VGA gain as a function of the input offset voltage, with a 35dB gain. With offset cancellation, the circuit is quite insensitive to the input offset voltage. The maximum tolerable offset voltage of the VGA, defined as the offset voltage in which the gain decreases by 1dB, is measured to be 50mV.

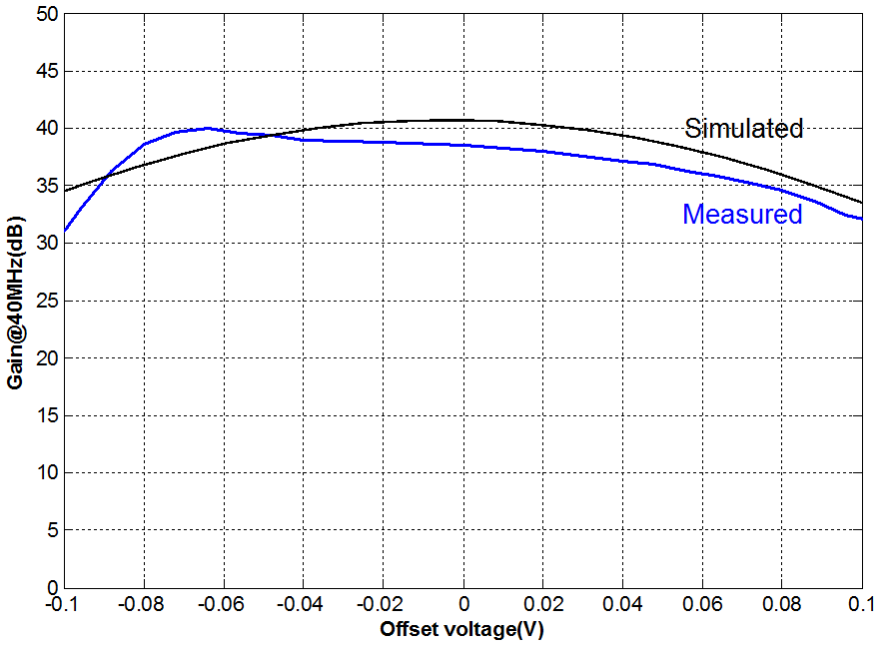


Figure 8.15: Measured and simulated gain variation due to the input offset voltage of the VGA at 40MHz.

Table 8.4 summarizes the 3-stage VGA measured performance, comparing with the previous obtained post-layout simulations. Results shows that the VGA has a continuous gain control range of 70dB, quite insensitive to the offset voltage, consuming 2.75mA (without buffer) from a 1.8V supply.

Table 8.4: VGA measured performance summary.

	Post-layout Simulation *IB=1.5mA* *CL=5pF*	***Measurement*** ***IB=1.5mA*** ***PCB load***
Gain control range (dB)	0 - 75	**0 - 72**
Offset cancellation (mV)	60	**50**
Output Swing (mVpp) (@35dB gain)	600 (0dBm)	**600** **(0dBm)**
Total power cons. (mW) (including buffer)	18.6	**15.21**

8.4 Discussion

This chapter discussed the testing of the discussed building blocks in a single chip in IBM 0.18µm CMOS process. An overview of the test chip was presented, including the testing configuration of the blocks performed in a printed circuit board.

First, the target design CMOS process was characterized. The g_m/I_D versus $I_D/(W/L)$ curves were obtained from non-encapsulated die samples, while a 19-stage ring oscillator was measured in the designed PCB. It was verified that at a typical power supply voltage (± 0.9V) the oscillation frequency is 710MHz, resulting in an average gate delay of *37.9ps*.

The designed front-end building blocks were tested. The up-conversion mixer demonstrates a gain around 4dB under different input frequencies at an output frequency of 1.4GHz, where its LC tank load is tuned. The down-conversion mixer achieves a conversion gain of 4dB at 40MHz with reasonable power consumption. The 40MHz 3-stage VGA achieved a continuous tuning range of 70dB for the gain, which is quite insensitive to the input offset voltage.

Due to limitations in the test equipments, only simple functional measurements could be performed. The linearity measurement could not be performed, since the two-tone test requires two signal generators and a power combiner (EMIRA, 2003), equipments that are not available in our laboratory. The noise figure measurement could not be performed either, since the measurement using the gain method (TUTORIALSWEB, 2007) requires a spectrum analyzer with a very good resolution bandwidth and noise floor of the order of -130dBm (the spectrum analyzer available provides a noise floor of the order of -80dBm). The whole front-end system could not be tested, since it requires at least 3 signal generators.

The measurement results for these blocks demonstrate the validation of the design of the analog blocks that composes the RF section of the FAC. Comparing to the previous obtained post-layout simulations, the results matched. In all blocks measurements, the power consumption is smaller compared to the estimation from electrical simulations.

In the case of the mixers measurements, the input signals power (IN and LO) had to be adjusted in order to obtain a reasonable conversion gain, given the signal losses from the circuitry test setup (baluns and RC bias circuits). However, in the up-conversion mixer, a peak conversion gain of about 4dB was achieved with almost the half of the power consumption obtained through electrical simulations (bias current of *4mA*), considering a bias current of *3mA*.

9 CONCLUSIONS

This thesis has examined in detail a number of issues related to the design, implementation and integration of analog/RF building blocks suitable for a general analog interface architecture targeted to systems on-chip applications (FABRIS, 2005), which is composed by a fixed analog cell (FAC) and a digital block.

In this context, three frequency bands (FM, video and digital cellular frequency bands) were analyzed and considered as our target application. Several recently reported RF receiver architectures with ADC were reviewed, considering its general system specifications. Thus, an initial set of system specifications was developed for the FAC system.

A CMOS integrated dual-conversion heterodyne front-end architecture, with 2 active mixers and a variable-gain block, suitable for the FAC architecture, was implemented, enumerating and proposing solutions for the design challenges and methodology. The main system design issues in the chosen architecture were discussed, where the final system specifications were derived and the front-end overall system performance was verified through system level simulations.

At the building block level, 2 active mixers and a 3-stage variable gain amplifier (VGA) has been designed and implemented using the g_m/I_D design method. The up-conversion mixer is implemented as double-balanced CMOS Gilbert Cell based topology with a linear input V-I converter and a LC tank load (since in our application the input signal varies in amplitude and frequency over a wide range, the linearity of this stage is optimized using a multi-tanh input triplet input stage). The down-conversion mixer was implemented as a simple double-balanced CMOS Gilbert Cell based topology, where the input differential pair is degenerated by means of two resistors. The 40MHz VGA was constructed with three operational transconductance amplifiers (OTA) in cascade, each of which has a variable gain from 0 to 20dB, where an offset cancellation circuitry is used to prevent this cell from being saturated due to its high gain and input offset voltage. The building blocks and the front-end system were designed and implemented in IBM 0.18μm CMOS process without resorting to any off-chip components.

Each building block and the entire front-end were simulated using the *Spectre* simulator and the foundry-provided BSIM3v3 electrical model parameters, in Cadence environment. The up-conversion mixer achieves a conversion gain of 5dB, a third input intercept point (IIP3) of 1.5dBm and an noise figure (NF) of 12dB for different input frequencies, where the multi-tahn triplet input cell and the integrated LC tank load

garanties the linearity of the circuit with reasonable gain and noise at the output frequency of 1.4GHz. The down-conversion mixer, achieves a gain of 5dB, while the degenerated input differential pair provides an IIP3 of -2dBm. The VGA has a continuous gain control range of 70dB, NF of 20dB, OIP3 of 5dBm, consuming 8mW from a 1.8V supply. The whole fron-end system achieves an overall sensitivity of about -70dBm, and IIP3 of -25dBm, and a NF of 25dB, with a power consumption of 55mW, with the input frequency varying from 48MHz to 960MHz.

A system chip, with all the discussed analog/RF blocks and some test scructures, was fabricated in IBM 0.18µm CMOS process through MPW MOSIS. The chip was prototyped in a 64-pin QFN package, with a total area of 6.8mm^2. The chip was tested in a double-face printed circuit board (PCB). First, the target design CMOS process was characterized. The g_m/I_D vs. $I_D/(W/L)$ curves were obtained from non-encapsulated die samples, while a 19-stage ring oscillator was measured in the designed PCB. It was verified that at a typical power supply voltage of 1.8V the oscillation frequency is 710MHz, resulting in an average gate delay of *37.9ps*.

The designed building blocks were tested. The up-conversion mixer demonstrates a gain around 4dB under different input frequencies at an output frequency of 1.4GHz, where the LC tank load is tuned. The down-conversion mixer achieves a conversion gain of 4dB at 40MHz with reasonable power consumption. The 40MHz VGA achieved a continuous tuning range of 70dB for the gain, and is quite insensitive to the offset voltage. The measurements results for these blocks validates of the design of the analog blocks that composes the RF section of the FAC. However, due to limitations in the test equipments, several performance measurements could not be performed, such as linearity and noise figure measurements. The whole front-end system could not be tested either, since it requires at least three RF signal generators.

In summary, the contribution highlights of this thesis are:

- Redefinition of the system specifications for the FAC system, focusing in 3 frequency bands applications: FM, video and digital cellular receivers;
- Complete specification and design of a fully integrated CMOS dual-conversion heterodyne front-end architecture suitable for the FAC system;
- Application of the g_m/I_D design method in CMOS mixers and high frequency amplifiers;
- Multi-band Gilbert Cell based up-conversion mixer with a linear input stage;
- 0-70dB variable gain amplifier with offset cancellation circuitry;
- Development of a RF system from system specifications to an actual physical prototype in a deep-submicron CMOS technology followed by measurements in a prototype SMT (surface mounted technology) board.

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APPENDIX A SUMMARY IN PORTUGUESE (RESUMO DA TESE)

Análise, Projeto e Implementação de Blocos Analógicos/RF Aplicados a uma Interface Analógica Multi-Banda para Sistemas-em-Chip (SOCs) em CMOS

1 Introdução

O desenvolvimento de novas tecnologias de integração *ultra-scale* para circuitos integrados (IC) junto com a demanda de cada vez mais processamento digital de sinais, como em sistemas de telecomunicações e aplicações SOC (*system-on-chip*), resultaram na crescente necessidade de circuitos mistos (analógico e digitais) em tecnologia CMOS integrados em um único chip. Grande parte destes sistemas necessita de blocos analógicos, como amplificadores, filtros, mixers (misturadores), osciladores, conversores analógico-digitais (ADC) e outros blocos de radio-freqüência (RF). Neste contexto, o crescente esforço para se aumentar o desempenho destes sistemas vem especialmente do uso de técnicas de projeto misto (*mixed-signal*) compatíveis com a implementação de blocos analógicos em tecnologias CMOS de última geração.

Em um trabalho anterior, a arquitetura de uma interface analógica para ser usada em aplicações SOC mistas foi desenvolvida e implementada. Esta interface utiliza o conceito de translação em freqüência do sinal de entrada analógico seguido por sua conversão para o domínio digital utilizando modulação sigma-delta (ΣΔ). Basicamente esta interface é composta por uma célula analógica fixa (*fixed analog cell* – FAC), que translada o sinal de entrada para uma freqüência de processamento fixa, e por um bloco digital que processa este sinal. A FAC é fixa em níveis estrutural e funcional, fornecendo largura de banda, ruído e cobertura de freqüência apropriados de acordo com a aplicação alvo. Um modelo de alto nível da interface junto com um protótipo discreto do mesmo foram desenvolvidos e testados em (FABRIS, 2005). Os resultados obtidos através do modelo e os resultados experimentais demonstram a potencialidade do uso desta interface numa variedade de aplicações.

Portanto, há uma oportunidade de pesquisa para a integração desta interface em um único chip, buscando todos os benefícios que esta integração possibilita. O lugar natural para a busca da solução para uma arquitetura completa para este sistema deve ser entre arquiteturas de receptores RF e de seus respectivos blocos construtivos, onde *mixers* são partes principais destes sistemas.

O foco desta tese é analisar, projetar e implementar blocos analógicos/RF para serem usados nesta inteface, mais especificamente na FAC. Primeiramente, as especificações de sistema foram determinadas considerando o processamento de sinais de três bandas de freqüência diferentes: áudio (FM), vídeo (VHF/UHF) e celular (GSM/CDMA), seguido por simulações de alto-nível do sistema da FAC. Então, uma arquitetura heteródina integrada CMOS para o *front-end* que integrará a FAC, composto por 2 *mixers* ativos e um amplificador de ganho variável, foi apresentada, enumerando-se e propondo-se soluções para os desafios de projeto e metodologia.

2 A interface analógica multi-banda para SOCs em CMOS

Como na maioria das aplicações o sinal de entrada é limitado por sua banda de freqüência, o processo de realocação do sinal de entrada para uma freqüência fixa e o processamento deste usando um bloco de alta performance misto pode ser uma boa alternativa para o processamento de um sinal analógico. Portanto, o conceito de translação em freqüência pode ser usado para se adquirir um sinal em uma freqüência intermediária (IF), e posteriormente processar este mesmo sinal no domínio digital.

Desta forma, uma arquitetura com a finalidade de ser usada nesta interface foi proposta, desenvolvida e analisada em (FABRIS, 2005). A Figura 1 (Figure 3.1) mostra a estrutura básica desta arquitetura proposta: a célula analógica fixa (*fixed analog cell* – FAC), que translada o sinal de entrada para uma freqüência de processamento fixa, e um bloco digital reconfigurável, que processa este sinal. O objetivo principal desta interface é simplesmente converter um sinal analógico em um sinal digital e processá-lo no domínio digital, onde a freqüência e a largura de banda do sinal de interesse variam dependendo da aplicação. Esta interface pode ser usada em várias aplicações, como conversores A/D multi-banda, filtros, multiplicadores analógicos e receptores RF.

A FAC é fixa tanto em níveis estrutural como funcional. Seu projeto pode ser otimizado para disponibilizar uma largura de banda apropriada, ruído e cobertura de freqüência para uma determinada aplicação alvo. A FAC é composta por um estágio *front-end*, um modulador ΣΔ passa-band contínuo no tempo, um sintetizador de freqüência e um filtro reconstrutor.

3 Projeto de blocos RF – O *front-end* IF

Este trabalho trata da implementação do estágio *front-end* da FAC, considerando uma grande cobertura de freqüência e implementação CMOS dos blocos que compõem este sistema. A finalidade deste estágio é converter um sinal de entrada analógico para uma freqüência de processamento fixa, onde a freqüência e a largura de banda do sinal de entrada variam. Para este trabalho foram escolhidas 3 aplicações alvo diferentes com os sinais de entrada nas seguintes bandas: áudio (FM), vídeo (VHF/UHF) e celular (GSM/CDMA).

Portanto, uma arquitetura heteródina de conversão dupla foi escolhida para o estágio *front-end*. A arquitetura completa, mostrada na Figura 2 (Figure 5.6), é descrita a seguir. O sinal de entrada entra no bloco *up-conversion mixer*, que converte este sinal para a primeira freqüência de processamento de 1.4GHz, que está fora da banda de freqüência de entrada. O sinal então passa por um simples tanque LC, fornecendo ao sistema uma supressão inicial de componentes de imagem e harmônicas. Posteriormente, o bloco *down-conversion mixer* converte o sinal para a segunda freqüência de processamento de 40MHz e finalmente o bloco do amplificador de ganho variável (VGA) fornece o ajuste de ganho do sistema. O sinal selecionado está agora pronto para ser amostrado pelo bloco modulador ΣΔ, e então processado pelo bloco digital da interface completa, onde a seleção de canais e cancelamento de imagem podem ser feitas. Cada bloco que compõe o *front-end*, será brevemente analisado a seguir.

A Figura 3 (Figure 7.5) mostra o esquemático do bloco *up-conversion mixer,* uma topologia baseada em uma Célula de Gilbert CMOS com um estágio de entrada conversor V-I e um tanque LC como carga. Como os sinais de entrada podem ter uma grande variação em amplitude e freqüência, a linearidade deste bloco deve ser otimizada. Isso é feito com a substituição do par diferencial de entrada por 3 pares pares diferenciais operando em paralelo (técnica *multi-tanh*).

Como mostrado na Figura 4 (Figure 7.15), o bloco *down-conversion mixer* é implementado numa topologia simples baseada em uma Célula de Gilbert CMOS. A fim de melhorar desempenho em linearidade, o par diferencial de entrada é degenerado por 2 resistores. O sinal de entrada está em uma frequência fixa (1.4GHz) sintonizado e

filtrado pelo tanque LC do estágio anterior, portanto, performance de ruído e linearidade são relaxadas.

O amplificador de ganho variável (VGA), operando na freqüência de 40MHz, é construído com 3 amplificadores operacionais em cascata, cada um deles com um ganho variável de 0 a 26dB, como é mostrado na Figura 5 (Figure 7.25). O estágio amplificador é composto por um par diferencial com realimentação de modo-comum (*CMFB*) e 4 transistores cruzados (*cross-coupled*) de controle, usados para o controle do ganho. A fim de se evitar que esta célula sature devido a tensão de *offset* de entrada em função de seu alto ganho, um circuito de cancelamento de *offset* é adicionado.

4 Projeto implementação, simulação e medidas experimentais dos blocos

Todos os circuitos foram projetados e implementados nesta tese separadamente e como parte o sistema *front-end* completo, no processo *CMOS IBM 0.18µm* com 6 níveis de metal (alimentação de ±0.9V). Todos os blocos foram projetados usando a metodologia $g_m/I_{D,}$ onde o projeto é ajustado a fim de se otimizar a performance especificada. Considerando um carga de saída de 5pF, um estágio buffer (estágio seguidor de fonte NMOS) foi adicionado a saída de cada bloco para conveniência de medidas.

Os *layouts* dos blocos foram feitos usando a ferramenta *Cadence Virtuoso Design Editor*, onde foram implementados em configuração diferencial e simétricos a fim de se minimizar o descasamento do caminho dos sinais. O tanque LC integrado foi implementado considerando a biblioteca de componentes do kit de design do processo *CMOS IBM 0.18µm*. Os indutores integrados, usados no estágio *up-conversion mixer*, foram implementados utilizando uma única camada de metal (ML – última camada de metal) em forma espiral (L=7.218nH, *Q* de aproximadamente 8 em 1.4GHz). A Figura 6 (Figure 7.36) mostra o *layout* o sistema *front-end* completo, com uma área total de $0.77mm^2$.

Cada bloco, incluindo o sistema *front-end* completo, foi caracterizado por simulações elétricas usando o simulador *Spectre*, e o modelo elétrico BSIM3v3 em ambiente *Cadence.* As tabelas 1, 2, 3 e 4 (Table 7.2, Table 7.4, Table 7.6, Table 7.7) mostram os resultados de simulação da performance de cada bloco mencionado.

Um chip teste, com todos os blocos analógicos/RF e estruturas de teste, foi fabricado em tecnologia *CMOS IBM 0.18µm*, pelo programa *MPW MOSIS*. O chip foi prototipado em um encapsulamento QFN de 64 pinos, com uma área total (incluindo os pads) de $6.8mm^2$. Todos os blocos foram caracterizados através de medidas experimentais, onde uma placa de circuito impresso foi projetada e implementada para este fim. As tabelas 5, 6, e 7 (Table 8.2, Table 8.3, Table 8.4) mostram os resultados de medidas da performance destes blocos.

5 Conclusões

Esta tese examinou em detalhe várias questões relacionadas ao projeto, implementação e integração de blocos analógicos/RF a serem usados em uma interface analógica para aplicações SOC, que é composta por uma célula analógica fixa (FAC) e um bloco digital.

Primeiramente, três bandas de freqüência foram consideradas e analisadas (FM, vídeo, e celular) como a aplicação alvo, onde várias arquiteturas de receptores RF com ADC foram analisadas considerando suas especificações de sistema. A partir desta análise, as especificações de sistema da interface completa foram determinadas.

Um bloco *front-end*, com uma arquitetura de conversão dupla heteródina, com 2 *mixer* ativos e um bloco de ganho variável, que compõe a FAC, foi implementado, enumerando e propondo soluções para os desafios de projeto e metodologia. As principais especificações de sistema para a arquitetura proposta foram discutidas, onde as suas especificações de sistema finais foram verificadas através de simulações a nível de sistema.

No nível de blocos, 2 *mixer* ativos e um amplificador de ganho variável foram projetados e implementados utilizando o metodologia de projeto g_m/I_D. Cada bloco, juntamente com o *front-end* completo, foram integrados em tecnologia *CMOS IBM 0.18μm* sem nenhum componente fora do chip. Todos os blocos foram caracterizados por simulações elétricas. O *up-conversion mixer* fornece 5dB de ganho de conversão, IIP3 de 1.5dBm e um NF de 12dB, para as diferentes freqüências do sinal de entrada (onde o seu estágio de entrada *multi-tahn triplet* garante performance em linearidade com ganho e ruído razoáveis em 1.4GHz). O *down-conversion mixer* fornece 5dB de ganho de conversão, enquanto o par diferencial degenerado fornece um IIP3 de -2dBm. Já o VGA tem um controle de ganho contínuo de 0 a 70dB, NF de 20dB, OIP3 de 5dBm, consumindo 8mW. O *front-end* completo fornece uma sensibilidade de -70dBm, IIP3 de -25dBm e NF de 25dB, com um consumo total de 55mW, onde a freqüência e amplitude do sinal de entrada variam (48MHz a 960MHz).

Os blocos analógicos/RF e algumas estruturas de teste foram prototipados em um chip neste processo, com uma área total de 6.8mm^2, e testados em uma placa de circuito impresso. Primeiramente, o processo CMOS foi caracterizado, onde as curvas g_m/I_D vs. $I_D/(W/L)$ foram obtidas através de medidas DC de amostras não-encapsuladas. Um oscilador em anel de 19 estágios também foi caracterizado, resultando em uma freqüência de oscilação típica de 710MHz (atraso médio por estágio de 37.9ns).

Os blocos analógicos/RF também foram testados. O *up-conversion mixer* fornece um ganho de conversão de 4dB para diferentes freqüências de entrada, resultando em um sinal de 1.4GHz, onde o tanque LC está sintonizado. O down-conversion *mixer* fornece um ganho de conversão de 4dB em 40MHz com consumo de potência razoável. Uma variação de ganho de 0 a 70dB foi medida para o VGA, onde sua performance é insensível a *offsets* de entrada até 50mV. Por causa de limitações nos equipamentos de testes, a caracterização completa dos blocos (inclusive a performance do *front-end* completo, onde são necessários 3 geradores de sinais RF) não pode ser feita.

Em resumo, as principais contribuições desta tese são:

- Redefinição das especificações de sistema da FAC, considerando sua aplicação em 3 bandas de sinais específicas: FM, vídeo e celulares;

- Especificação e projeto do bloco *front-end*, em uma arquitetura CMOS de conversão dupla heteródina, a ser usado na FAC;
- Aplicação da metodologia de projeto g_m/I_D no projeto dos módulos CMOS mixer e amplificador;
- *Up-conversion mixer* multi-banda baseado um uma Célula de Gilbert com um estágio de entrada linear;
- VGA com uma variação de ganho de 0 a 70dB com um estágio de cancelamento de *offset*;
- Desenvolvimento e projeto de um sistema RF de suas especificações de sistema até ao seu protótipo físico integrado em uma tecnologia *deep-submicron* CMOS, seguido por medidas experimentais de um protótipo SMT.