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Design of CMOS Active Downconversion Mixers for Gigahertz Multi-Band and Multiple-Standard Operation

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“Legere est omnis scientiae fundamentum”
”To read is the foundation of all knowledge”

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ABSTRACT

The linearity and noise requirements in multi-band multi-standard applications make the design of RF CMOS mixers a very challenging task. In this dissertation two down-conversion mixers based on the Gilbert-cell topology are proposed. Linearity and noise were the principal figures of merit for the proposed mixers. For linearity improvement, post distortion harmonic cancellation (PDHC) was employed. And, for noise reduction, dynamic current injection combined with an LC filter tuned at the LO frequency and thermal-noise cancellation were used.

A Volterra series analysis of the transconductance stage is reported to show the effectiveness of the post-distortion harmonic cancellation technique. The added linearization circuitry does not increase the size of the mixer, nor does it degrade conversion gain, noise figure, or power consumption.

Electrical simulations were performed on extracted layout level from the first topology and schematic level from the second topology. Using an IBM 0.13 μm CMOS process improvements on IIP_3 and IIP_2 in comparison to the conventional Gilbert-cell mixer are demonstrated.

For the first topology, we achieved a conversion gain of 10.2 dB with a NF of 12 dB for the designed mixer working at 2 GHz, with a low-IF of 500 kHz and an IIP_2 and IIP_3 of 55 dBm and 10.9 dBm, respectively, while consuming only 5.3 mW from a 1.2 V supply.

For the second topology, we achieved a conversion gain range of [13.8 ~11] dB, an input reflection coefficient (S_{11}) of [-18 ~-9.5] dB and a NF of [8.5 ~11] dB in the frequency range of 1 to 6 GHz. For the linearity specs, an IIP_3 of 0 dBm was achieved for the whole frequency range, while consuming 19.3 mW from a 1.2 V supply, making the second topology well suited for multi-band and multi-standard operation.

Keywords: CMOS, Direct Conversion, Multi-Band Receivers, Gilbert-cell Mixer, Post-Distortion Harmonic Cancellation, Volterra series, Distortion Analysis, RF, Radio frequency, Receiver front-end.

Um Misturador Ativo CMOS para Conversão a Baixas Frequências com Operacão Multi-Banda e Multi-Protocolo

RESUMO

Os requisitos de linearidade e ruído em aplicações multi-banda e multi-protocolo fazem que o projeto de misturadores RF seja uma tarefa muito desafiadora. Nesta dissertação dois misturadores com base na topologia célula de Gilbert são propostas. Linearidade e ruído foram as principais figuras de mérito consideradas para o misturadores propostos. Para aumento linearidade, foi utilizada uma técnica de cancelamento de harmônicas pós-distorção (PDHC). E, para redução de ruído, foi utilizado um circuito de redução dinâmica de corrente combinada com um filtro LC sintonizado na frequência do LO e cancelamento de ruído térmico.

A análise por séries Volterra do estágio transcondutância do misturador proposto é reportada para mostrar a eficácia da técnica de cancelamento de harmônicos com pós-distorção. O circuito de linearização adicionado não aumenta o tamanho do misturador, nem degrada ganho de conversão, figura de ruído, ou consumo de potência.

Simulações elétricas foram realizadas em nível de pós-layout para a primeira topologia e nível esquemático para a segunda topologia, usando processo CMOS de 0.13 μm da IBM. As melhorias em IIP_2 e IIP_3 são apresentadas em comparação com o misturador do tipo célula de Gilbert convencional.

Para a primeira topologia, foi obtido um ganho de conversão de 10.2 dB com uma NF de 12 dB para o misturador projetado funcionando a 2 GHz, com uma frequência intermediária de 500 kHz. E um IIP_2 e IIP_3 de 55 dBm e 10.9 dBm, respectivamente, consumindo apenas 5.3 mW de uma fonte de 1.2 V.

Para a segunda topologia, foram obtidos um ganho de conversão de [13.8 ~11] dB, um coeficiente de reflexão na entrada (S_{11}) de [-18 ~-9.5] dB e um NF de [8.5 ~11] dB no intervalo de 1 a 6 GHz. Para as especificações de linearidade, um valor médio de IIP_3 de 0 dBm foi alcançado para toda a faixa de frequência, consumindo 19.3 mW a partir de uma fonte de 1.2 V. Especificações adequadas para operação multi-banda e multi-protocolo.

Palavras-chave: CMOS, Conversão Direta, Receptores Multi-Banda, Misturador com Topologia Célula de Gilbert, Cancelamento Harmônico com Pós-Distorção, Séries de Volterra, Análise de Distorção, RF, Radiofrequência, Receptor front-end, Projeto de Circuitos Integrados, Relação Transcondutância-Corrente .

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LIST OF ABBREVIATIONS AND ACRONYMS

GSM	Global System for Mobile Communications
LAN	Local Area Network
CDMA	Code Division Multiple Access
GMSK	Gaussian Minimum-Shift Keying
LNA	Low Noise Amplifier
Balun	Balanced-Unbalanced
SDR	Software Defined Radio
RF	Radio Frequency
IF	Intermediate Frequency
HD_2	Second-order Harmonic Dirtortion
HD_3	Third-order Harmonic Distortion
IM_2	Second-order Intermodulation
IM_3	Third-order Intermodulation
$IP1dB$	Input referred 1dB Compression Point
IIP_2	Input referred Second-order Interception Point
IIP_3	Input referred Third-order Interception Point
OIP_2	Output referred Second-order Interception Point
OIP_3	Output referred Third-order Interception Point
AIP_2	Amplitude of the Input referred Second-order Interception Point
AIP_3	Amplitude of the Input referred Third-order Interception Point
IIV_3	Input referred Third-order Voltage Point
SNR	Signal-to-Noise-Ratio
CNR	Carrier-to-Noise-Ratio
DR	Dynamic Range
SFRDR	Spurious-Free Dynamic Range
MDS	Minimum Detectable Signal

dB	decibel
dBm	decibel-miliwatts
LO	Local Oscillator
LPF	Low Pass Filter
Q	Quality Factor
F	Noise Factor
NF	Noise Figure
CG	Conversion Gain
BER	Bit-error-rate
DC	Direct Current
AC	Alternate Current
MHz	MegaHertz
GHz	GigaHertz
BW	BandWidth
WBLNA	Wide Band Low Noise Amplifier
ESD	ElectroStatic Discharge
CS	Common-Source
CG	Common-Gate
CD	Common-Drain
I/O	Input-Output
FET	Field Effect Transistor
MOSFET	Metal-oxide-semiconductor Field Effect Transistor
CMOS	Complementary metal-oxide-semiconductor
PMOS	P-channel MOSFET
NMOS	N-channel MOSFET
NFET	N-channel FET
PFET	P-channel FET
PCB	Printed-Circuit Board
KCL	Kirchoff's Current Law
PDK	Process Design Kit
IEEE	Institute of Electrical and Electronics Engineers
IBM	International Business Machines Corporation
ICC	IBM Customer Connect
MIM	Metal-Insulator-Metal

DRC	Design Rules Check
LVS	Layout-vs-Schematic
VCO	Voltage-Controlled Oscillator
Amp	Amplifier
EMI	Electro-Magnetic Interference
SD	Skin Depth
DUT	Device Under Test
MEMS	Micro Electro Mechanical Systems
SAW	Surface Acoustic Wave
PCB	Printed Circuit Board
VGA	Variable Gain Amplifier
A/D	Analog/Digital Converter
LSB	Least Significant Bit
R_X	Receiver
CMRR	Common Mode Rejection Ratio
NLTI	Non-Linear Time Invariant
ACM	Advance Compact Model
DS	Derivative Superposition
MGTR	Multiple Gated Transistor
PDHC	Post Distortion Harmonic Cancellation
CMFB	Common Mode Feedback
VNA	Vector Network Analyzer
ENR	Excess Noise Ratio

CONTENTS

1 INTRODUCTION

1.1 CMOS Technology and Wireless Systems

Until the late 1980s, radios were implemented using discrete components such as transistors, capacitors, and inductors. The transistors used in these radios were manufactured using expensive process technologies that were optimized for high- frequency applications ABIDI (1999). As sales of wireless communication handsets have risen, the wireless transceiver market has become increasingly attractive to electronics hardware vendors. This has led to a highly competitive consumer market space, with tremendous pressures in the industry for lowest-cost solutions.

In the early 1990s, the adoption of standards such as GSM, and advances in digital signal processing increased the demand for digital circuits in radio systems. CMOS has been the technology of choice for implementing digital signal processors, since CMOS devices consume less power than competing technologies. This has spurred research efforts to reduce the cost of CMOS transistors and implementations. Given sufficient production volume, the cost of a CMOS chip decreases as the size of a unit transistor decreases, because the same functionality can be provided in a smaller silicon die area. In 1965, Gordon Moore predicted that the number of transistors that could be put in a given space would double approximately every two years MOORE (1998). His prediction has proved true: transistor unit size has decreased exponentially for decades RABAEY; A.CHANDRAKASAN; NIKOLIC (2002).

As CMOS transistor size shrinks, device parasitic capacitances also become smaller, and the transistor becomes faster GRAY et al. (2001). Eventually, CMOS transistors become sufficiently fast to be used in radio frequency integrated circuit implementations. From that point, CMOS provides the highest analog-digital on-chip integration and yields the lowest-cost solutions for implementing wireless transceivers. For these reasons, much research on CMOS wireless transceivers has been published, describing increasing levels of digital and analog integration RUDELL et al. (1997), ERDOGAN et al. (2005), MEHTA et al. (2005). Although competing technologies exist, the cost benefits of mixed-signal CMOS technology make it the process of choice for transceivers used in high-volume applications.

1.2 Need for Multi-Standard Receivers

The limited available frequency spectrums have become overcrowded as wireless network deployments have proliferated. This crowding has stimulated research efforts to increase spectral efficiency through better modulation schemes or advanced system-level techniques (e.g., power control in CDMA systems). In the last 20 years, several new

standards have been proposed and implemented; Table 1.1 shows the wireless standards currently in use CHEN; POOBUAPHEUN; NIKNEJAD (2006). From the table, it is clear that each standard specifies its own frequency band, modulation scheme, signal power, and data rates. The differences in the defined standards translate into different requirements for receiver front-ends – when a new standard is created, a new receiver front-end must be designed, which is time-consuming. One approach to reducing the system design time is to optimize an existing receiver front-end for a different application. However, this methodology results in inferior performance.

Table 1.1: Comparison of wireless standards (table from CHEN; POOBUAPHEUN; NIKNEJAD (2006))

Range	Long		Medium	Short	
System	GSM/DCS	UMTS	(Wi-Fi) 802.11a	Bluetooth	DECT
Frequency	0.9/1.8 GHz	2 GHz	5 GHz	2.4 GHz	1.9 GHz
Channel spacing	200 kHz	5 MHz	20 MHz	1 MHz	1.728 MHz
Access	TDMA	CDMA	CSMA/CA	CDMA	TDMA
Modulation	GMSK	QPSK	BPSK/QPSK/QAM	GFSK	GFSK
Bit rate	270 k/s	3.84 M/s	5.5~54 M/s	1 M/s	1.152 M/s
Rx sensitivty	-100 dBm	-117 dBm	-65 dBm	-70 dBm	-83 dBm
Signal S/N+I	9 dB	5.2 dB	28 dB	21 dB	10.3 dB
Rx NF	9 dB	9 dB	7.5 dB	23 dB	18 dB
Rx IIP_3	-18 dBm	-4 dBm	- 20 dBm	-15 dBm	-22 dBm
Phase noise	-141 dBc@3M	-150 dBc@135M	-102 dBc@1M	-105 dBc@1M	-99 dBc@2.2M

Over the past decade, consumer electronics manufacturers have tried to integrate many features in a single hand-held device (e.g., multi-band multi-standards compatibility). This has given rise to a need for receivers that are compatible with as many standards and frequency bands as possible. Most current multi-band receivers rely on multiple receiver front-ends to process signals at different bands MANKU et al. (2004). The major drawback of this approach is that each front-end must be individually optimized, resulting in longer design and simulation times, due to the number of circuit blocks, and interface complexity. In addition, this approach can require very large front-end silicon die areas, especially if inductors are used in each receiving path. Finally, this type of implementation is highly standard-specific; thus, a major redesign would likely be required if the same topology were used for different standards – when, for example, there is an immediate need for a front-end that is compatible with the system, but with different requirements from previous front-ends.

1.3 Research Contributions

In this thesis, we contribute mainly to the development of low-distortion and low-noise active downconverter mixers that comply with multi-band multi-standard operation.

- A new method to improve the linearity performance of the transconductance stage of a Gilbert-cell mixer is proposed using the post-distortion harmonic cancellation technique. Utilizing the Volterra series method, the linearity performance is analyzed.
- Two topologies of downconversion Gilbert-cell mixer type are proposed in this

work. The first employs the post-distortion harmonic cancellation to improve linearity. The second topology combines thermal noise cancellation and post-distortion cancellation for the transconductance stage. The resulting downconversion mixers will be part of a low-noise and high linearity front-end circuit.

- A constraint-based design methodology for the mixers is proposed, so that optimization of individual specs or a trade-off between key specs can be achieved using this methodology.

1.4 Thesis Organization

The thesis is organized as follows:
Chapter 2 provides a review on wireless receivers for multi-band multi-standard operation, beginning with receivers architecture, performance characterization and, finally, discussing the effects of distortion in wireless receivers.

Chapter 3 reviews the Gilbert-cell mixer, performance characterization and improvements. It presents a full Volterra analysis of the linearity performance of the Gilbert-cell mixer, and a concise literature review of previous works on active mixers for multi-band receivers. Two topologies of downconversion Gilbert-cell mixer type are proposed. The linearity performance using Volterra series and the noise contribution of the first topology are described.

Chapter 4 presents a constraint-based design methodology for a Gilbert-cell mixer. The key specs are characterized as function of the drain current efficiency ($\frac{g_m}{I_D}$) and circuit parameters. Using this methodology the proposed mixers are designed and evaluated through simulations. Finally, an assessment of the designed mixers is made with respect to the state of the art.

Chapter 5 discusses the test chip configuration for measurements.

Chapter 6 concludes presents the conclusion of the thesis and directions for future works.

2 WIRELESS RECEIVERS

2.1 Introduction

This chapter covers two important receiver concepts: selectivity and sensitivity. These parameters are the most comprehensive figures of merit in receiver performance and are influenced by many sub-figures of merit, such as noise performance of the individual building blocks, linearity, gain distribution, and image rejection ratio. The relationships between these sub-figures of merit and selectivity and sensitivity are discussed in sections 2.2, 2.3, and 2.4.

Section 2.5 offers a review of basic receiver architectures characterized by various frequency planning methodologies, including super-heterodyne, zero-IF (direct conversion), and low-IF receivers. Comparisons between several receiver architectures for multi-band receivers are given in section 2.6, along with a discussion on the requirements and estimated performance of a broadband front-end.

2.2 Sensitivity

Sensitivity is defined as the minimum signal level at the receiver input such that there is a sufficient signal-to-noise ratio (SNR) at the receiver output for a given application. It can be specified in units of dBm (decibels relative to one milliwatt), along with reference impedance (50 Ω for most systems), and is typically measured in an interference-free environment. Usually, the input of the receiver is matched to a certain source impedance, simplified as the real impedance $R_{in} = R_s$, as shown in Fig. 2.1.

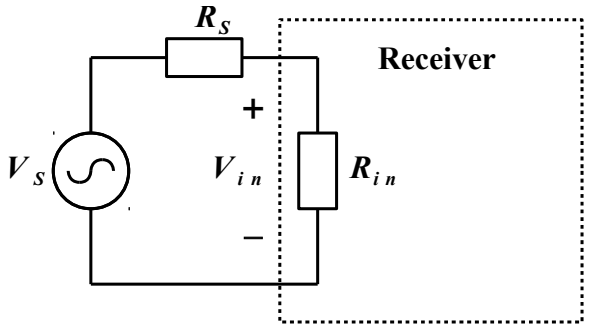


Figure 2.1: Impedance matching in a receiver

2.2.1 Noise Figure Definitions

The overall sensitivity is directly related to the noise figure of the receiver, which is impacted by noise from individual blocks in the receiver as well as the gain distribution of the receiver chain. The noise figure is defined as a ratio between the SNR at the input and the SNR at the output of the circuit:

$$F \equiv \frac{SNR_{in}}{SNR_{out}} \tag{2.1}$$

$$NF \equiv 10\log(F)\,(dB) \tag{2.2}$$

where F is noise factor and NF is the noise figure of the system. Noise figure is calculated in reference to the specified source impedance and the temperature (T). In standard communication systems, the typical values are $R_s = 50\ \Omega$ and $T = 293\,K$. For a circuit building block such as an amplifier, the total noise figure can be calculated in terms of added output noise and the gain of the system. An amplifier with power gain G, input signal power P_{in}, and input noise power N_{in} will have the output signal power GP_{in} and the output noise power $GN_{in} + N_{add}$. The noise figure of the amplifier can then be calculated using the definitions in Eq. 2.1.

$$F = \frac{\frac{P_{in}}{N_{in}}}{\frac{GP_{in}}{GN_{in}+N_{add}}} \tag{2.3}$$

$$F = 1 + \frac{N_{add}}{GN_{in}} = 1 + \frac{N_{add,in}}{N_{in}} \tag{2.4}$$

where $N_{add,in}$ is the input-referred added noise from the amplifier, defined as $N_{add,in} = N_{add}/G$.

2.2.2 Noise Figure Calculations for Cascaded Blocks

The previous section discussed the definition of the noise figure for a single circuit block. However, for a receiver, we need to calculate the noise figure of cascaded circuit blocks in order to determine the overall system sensitivity. The cascaded noise figure depends strongly on the noise figures of individual blocks, as well as the gain distribution of the receiver chain. If two blocks are cascaded with each other, as shown in Fig. 2.2, and the impedance matching is done properly (input and output are matched), the total output noise is then given by:

$$P_{noise,out} = F_1 P_{noise,in} G_1 G_2 + (F_2 - 1) P_{noise,in} G_2 \tag{2.5}$$

G_1 and G_2 are the power gains for each block in the given matching condition. F_1 and F_2 are the noise figures for each block. The output SNR of the cascaded blocks is then given by:

$$SNR_{out} = \frac{S_{out}}{P_{noise,out}} = \frac{S_{in} G_1 G_2}{F_1 P_{noise,in} G_1 G_2 + (F_2 - 1) P_{noise,in} G_2} = SNR_{in} \left(\frac{1}{F_1 + \frac{F_2 - 1}{G_1}} \right) \tag{2.6}$$

Finally, the total cascaded noise figure can be calculated as:

$$F = \frac{SNR_{in}}{SNR_{out}} = F_1 + \frac{(F_2 - 1)}{G_1} \tag{2.7}$$

From Eq. 2.7, the overall noise figure depends on the noise figures of both stages and on the gain of the first stage. If G_1 is large, noise from the later stage will have less effect on the overall noise figure. As a result, the first block in the receiver must exhibit low noise and must have at least moderate gain. An amplifier with those characteristics is usually called a low-noise amplifier, (LNA).

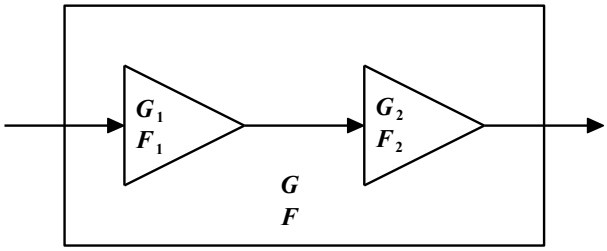


Figure 2.2: Cascaded blocks

2.2.3 Relationship between Noise Figure and Sensitivity

Direct relationship exists between the noise figure of the amplifier and the sensitivity of the receiver. Sensitivity can be calculated in terms of noise floor and the required SNR at the input. Since the required SNR at the output of the receiver is set by top-level specifications such as modulation techniques and bit-error-rate (BER), it is usually fixed for a given application. These numbers determine carrier-to-noise ratio (CNR), which is the ratio between the carrier power and the integrated noise power in the frequency band. Once the CNR is known, the required receiver input SNR can be calculated as:

$$SNR_{in}(dB) = CNR_{out}(dB) + NF(dB) \tag{2.8}$$

Finally, the expression for the sensitivity is given by:

$$Sensitivity(dBm) = SNR_{in}(dB) + NoiseFloor(dBm) + 10log(BW)(dB) \tag{2.9}$$

where BW is the bandwidth of the communication channel.

2.3 Selectivity

In the last section, we discussed receiver performance, measured by sensitivity to the desired signal. We did not consider interference from other undesired signals. Receiver selectivity is a performance measure of the ability to separate the desired signal from these unwanted interfering signals. It usually becomes important in the near-far situation where the desired signal is weak and there is a strong adjacent- band/channel interfering signal at the receiver input.

There is no clear quantitative measure of selectivity, especially at the circuit level. It is usually specified in the physical layer, such as in blocking masks, which can be used

to obtain the filtering, nonlinearity, and phase noise requirements in the circuit. The other test related to selectivity of the receiver is the third-order intermodulation or two-tone test. In this case, a pair of undesired signals is applied to the receiver in such a way that their third-order intermodulation will line up in the same band as the desired signal. We will discuss these specifications and tests in detail in the next sections.

2.3.1 Blocking Performance

Blocking performance is usually specified with a desired signal being applied to the receiver at a specified power level above the required sensitivity. Simultaneously, an additional signal, called a blocker (sometimes called a jammer) is applied to the receiver at a defined power level and offset from the carrier. Under these conditions, the receiver must maintain the required bit error rate (BER) in the presence of the blocking signal.

A strong blocker can degrade receiver performance in several ways. First, it can cause gain compression, as well as degradation of the noise figure of the receiver. This directly reduces the sensitivity of the receiver for the desired signal MEYER; WONG (1995). The second problem comes from the nonlinearity of the system. When the large blocker goes through second-order nonlinearity in the receiver chain, it can mix with itself down to a very low frequency and so create problems, especially in direct-conversion or low-IF receivers. A detailed analysis of nonlinearity will be given in the next section. Finally, the strong blocker can mix with the local oscillator sidebands resulting from its phase noise, a process known as reciprocal mixing. The mixed signal can be in the same frequency band as the desired signal, effectively decreasing the signal-to-noise ratio. More details about the reciprocal mixing can be found in RUDELL (2000).

An example of the blocking definition is shown in figure 2.3 for the GSM 900 standard ETSI (1996). The blocking test is performed by applying a Gaussian Minimum-Shift Keying (GMSK) modulated signal at 3 dB above the required sensitivity, along with the single-tone blocker at the input of the receiver. The blockers are located at increments of 200 kHz away from the desired signal, with the amplitudes shown in Fig. 2.3. To pass the test, the receiver must maintain the bit-error–rate within a defined limit.

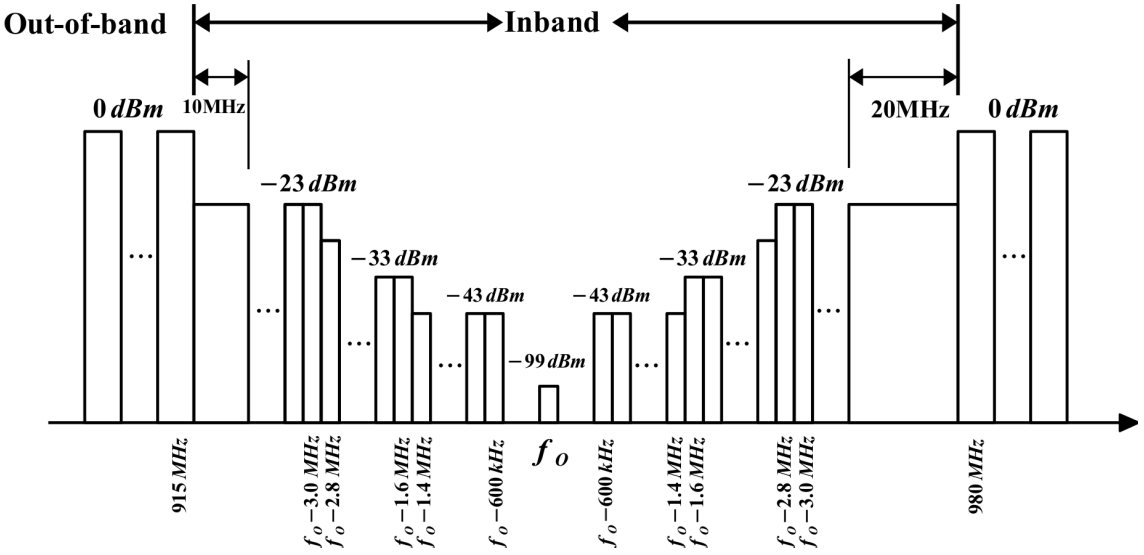


Figure 2.3: GSM 900 blocking definition

There are two types of blockers: in-band and out-of-band. Usually, the band- selecting filter in front of the receiver will filter out the out-of-band blockers. As a result, those

blockers will be highly attenuated before arriving at the real receiver input. However, this is not the case for in-band blockers, where all the signals are in the passband of the filter.

2.3.2 Second-order Nonlinearity

Second-order nonlinearity in the receiver blocks causes many problems, especially in direct-conversion or low-IF receivers. This can be understood by examining an expression that relates the input and output signals of the block. First, assuming we have a relationship given by:

$$S_{out}(t) = \alpha_1 S_{in}(t) + \alpha_2 S_{in}^2(t) + \alpha_3 S_{in}^3(t) + \ldots \tag{2.10}$$

where $S_{in}(t)$ is the input signal and $S_{out}(t)$ is the output signal. If the input signal (the blocker) is a sine wave, we then have:

$$S_i(t) = A_{rf} cos(\omega_b t) \tag{2.11}$$

where ω_b is the frequency of the blocker. Applying Eq. 2.11 into Eq. 2.10,

$$S_{out}(t) = \underbrace{\frac{\alpha_2 A_{rf}^2}{2}}_{DC} + \underbrace{\left(\alpha_1 A_{rf} + \frac{3\alpha_3 A_{rf}^3}{4}\right) cos(\omega_b t)}_{Fundamental} + \underbrace{\frac{\alpha_2 A_{rf}^2}{2} cos(2\omega_b t)}_{2^{nd}\,harmonic} + \underbrace{\frac{\alpha_3 A_{rf}^3}{4} cos(3\omega_b t)}_{3^{rd}\,harmonic} \tag{2.12}$$

There are two components of Eq. 2.12 created by the second-order nonlinearity, one located at DC and the other at the frequency of $2\omega_b$. The DC component can superimpose onto the baseband signal at DC and degrade the receiver performance. This becomes problematic in direct conversion receivers with the presence of a strong blocking signal.

Defining second-order harmonic distortion and second-order intermodulation as in MEYER (2004), the expressions for HD_2 and IM_2 are given by:

$$HD_2 = \frac{Amplitude\,of\,2^{nd} - order - term}{Amplitude\,of\,fundamental} = \frac{\frac{\alpha_2}{2} A_{rf}^2}{\alpha_1 A_{rf}} = \frac{1}{2}\frac{\alpha_2}{\alpha_1} A_{rf} \tag{2.13}$$

$$IM_2 \cong HD_2 + 6dB = 2HD_2 \tag{2.14}$$

Since IM_2 increases linearly with input signal level, there will be a point where the extrapolated IM_2 is equal to the extrapolated first-order output signal (Fig. 2.4). The amplitude (in voltage) of the input interferer at the second-order intercept point, AIP_2, is defined by the relation

$$20log(\alpha_1 A_{IP2}) = 20log(\alpha_2 A_{IP2}) \tag{2.15}$$

From equation 2.15 we can solve for AIP_2:

$$AIP_2 = \frac{\alpha_1}{\alpha_2} \tag{2.16}$$

For a 50 Ω load, we define the input second-order intercept point (IIP_2) as $IIP_2 = A_{IP2}^2/50\Omega$. ($IIP_3$ is hence interpreted as the power level of the input interferer for a 50 Ω load at the second-order intercept point). Notice that IIP_2 can be interpreted in terms

of absolute value or decibels. One useful equation that relates IIP_2 to IM_2, expressed in decibels, is the following JOHNS; MARTIN (1997):

$$IIP_2|_{dBm} = P_{in}|_{dBm} - IM_2|_{dB} \tag{2.17}$$

Here P_{in} is the power level of the input interferer and is typically defined for a 50 Ω load. Both IIP_2 and P_{in} have been expressed in dBm, whereas IM_2 is expressed in dB.

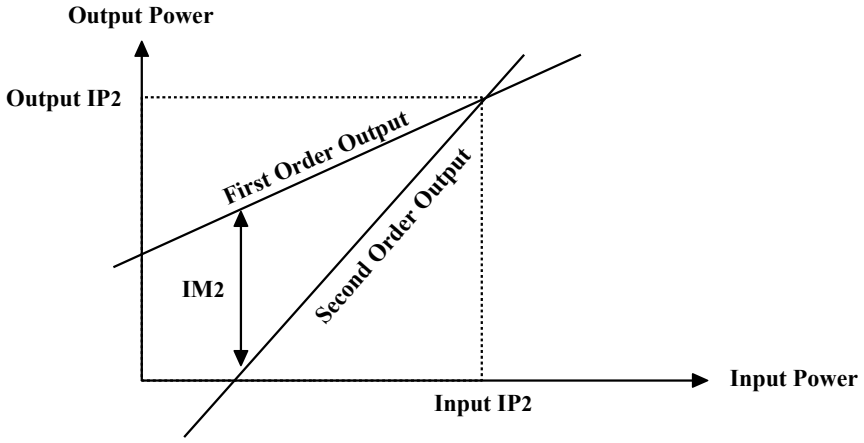


Figure 2.4: IM_2 plot and IIP_2 intercept point

2.3.3 Third-order Nonlinearity

Another important type of nonlinearity in receiver systems is third-order nonlinearity. Problems associated with third-order nonlinearity arise from two out-of- channel signals passing though the nonlinear blocks. We begin applying the definition of third-order harmonic distortion on the Eq. 2.12 and assuming $\alpha_1 A_{rf} \gg \left(3\alpha_3 A_{rf}^3\right)/4$, the expression for HD_3 is given by:

$$HD_3 = \frac{Amplitude\,of\,3^{rd} - order - term}{Amplitude\,of\,fundamental} = \frac{\frac{\alpha_3}{4}A_{rf}^3}{\alpha_1 A_{rf}} = \frac{1}{4}\frac{\alpha_3}{\alpha_1}A_{rf}^2 \tag{2.18}$$

Intermodulation arises when more than one tone is present at the input. A common method for analyzing this distortion is the "two-tone" test. Assuming that these two signals are sinusoidal, we can write them in combination as an input signal:

$$S_i(t) = A_1 cos(\omega_1 t) + A_2 cos(\omega_2 t) \tag{2.19}$$

After $S_i(t)$ passes through the third-order nonlinearity term in Eq. 2.12, several unwanted frequencies are generated. After simplification, we get:

$$\begin{aligned}\alpha_3 S_i^3 = {} & \frac{\alpha_3 A_1^3}{4}(cos(3\omega_1 t) + 3cos(\omega_1 t)) + \frac{\alpha_3 A_2^3}{4}(cos(3\omega_2 t) + 3cos(\omega_2 t)) + \\ & \frac{3}{4}\alpha_1 A_1 A_2^2 [2cos(\omega_1 t) + cos((2\omega_2 - \omega_1)t) + cos((2\omega_2 + \omega_1)t)] + \\ & \frac{3}{4}\alpha_1 A_1^2 A_2 [2cos(\omega_2 t) + cos((2\omega_1 - \omega_2)t) + cos((2\omega_1 + \omega_2)t)]\end{aligned} \tag{2.20}$$

The graphical presentation of Eq. 2.20 is shown in Fig. 2.5. There are linear terms (ω_1, ω_2), third-order harmonics ($3\omega_1$ and $3\omega_2$), and third-order intermodulation terms ($2\omega_2 - \omega_1$, $2\omega_2 + \omega_1$, $2\omega_1 - \omega_2$ and $2\omega_1 + \omega_2$).

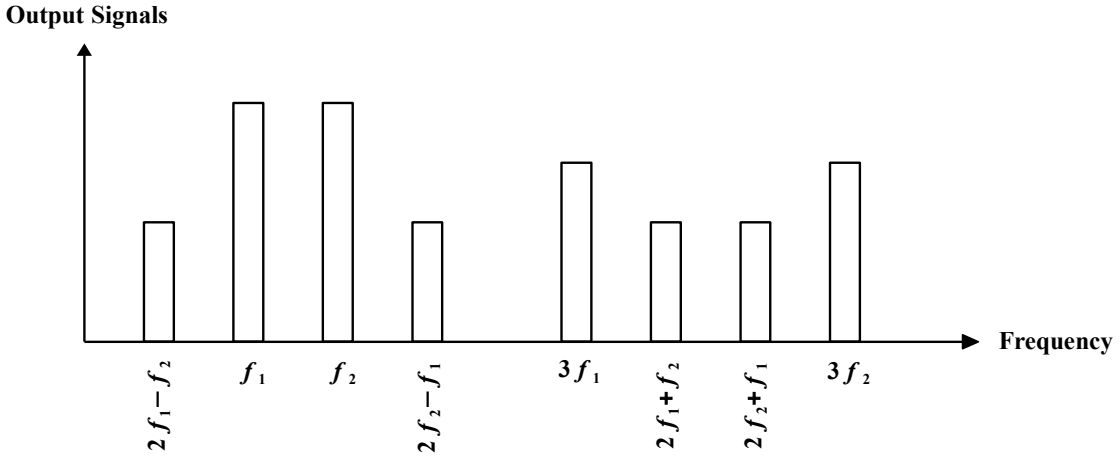


Figure 2.5: Third–order products in frequency domain

To quantify this distortion we first define the third-order intermodulation distortion, IM_3, as the ratio of the amplitude of the third-order intermodulation product to the amplitude of the fundamental output component. In order to quantify IM_3, let us simplify by assuming $A = A_1 = A_2$.

$$IM_3 = \frac{Amplitude\,of\,3^{rd} - order - intermod}{Amplitude\,of\,fundamental} = \frac{\frac{3\alpha_3}{4}A^3}{\alpha_1 A} = \frac{3}{4}\frac{\alpha_3}{\alpha_1}A^2 \tag{2.21}$$

Comparing Eq. 2.18 to Eq. 2.21, it is seen that

$$IM_3 = 3HD_3 \tag{2.22}$$

If the two-tones are placed adjacent to each other, some of the IM_3 products will lie just next to ω_1 and ω_2. If the desired channel is located at either $2\omega_2 - \omega_1$ or $2\omega_1 - \omega_2$, it will experience interference due to these components. This is often the most troubling case for receiver applications where there might be alternate channel users present very close in frequency to the receiver's desired channel.

Fig. 2.6 shows the logarithmic plot between the output and input signals assuming the same power of the two-tones. The third-order intermodulation grows with the input power at three times the rate at which the linear components increase. The third-order intercept point (IP_3) is defined as the intersection of the two lines.

The horizontal coordinate of this point is called the input IP_3 (IIP_3), and the vertical coordinate is called the output IP_3 (OIP_3). We can see that the amplitude (in voltage) of the input interferer at the third-order intercept point, A_{IP3} is defined by the relation

$$20log(\alpha_1 A_{IP3}) = 20log(\frac{3}{4}\alpha_3 A_{IP3}^3) \tag{2.23}$$

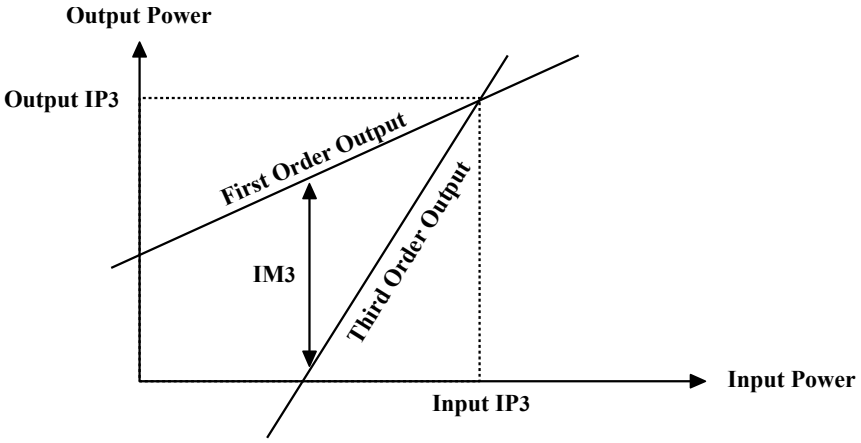


Figure 2.6: Third-order intercept points

From Eq. 2.23 we can solve for A_{IP3}:

$$AIP_3 = \sqrt{\frac{4}{3}\left|\frac{a_1}{a_3}\right|} \tag{2.24}$$

For a 50 Ω load, we define the input third-order intercept point (IIP_3) as $IIP_3 = A_{IP3}^2/50\Omega$. ($IIP_3$ is hence interpreted as the power level of the input interferer for a 50 Ω load at the third-order intercept point). Notice that IIP_3 can be interpreted in terms of absolute value or decibels. One useful equation that relates IIP_3 to IM_3, expressed in decibels, is the following JOHNS; MARTIN (1997):

$$IIP_3|_{dBm} = P_{in}|_{dBm} - \frac{IM_3|_{dB}}{2} \tag{2.25}$$

Here P_{in} is the power level of the input interferer and is typically defined for a 50 Ω load. Both IIP_3 and P_{in} have been expressed in dBm, whereas IM_3 is expressed in dB.

For cascaded nonlinear stages such as the one in Fig. 2.2, the overall IIP_3 is affected by the nonlinearity of each block and gain distribution. As shown in RAZAVI (1998), the overall IIP_3 is given (neglecting second-order interaction) by:

$$\frac{1}{IIP_{3,overall}^2} \approx \frac{1}{IIP_{3,1}^2} + \frac{G_1^2}{IIP_{3,2}^2} + \frac{G_1^2 G_2^2}{IIP_{3,3}^2} + \ldots \frac{G_{k-2}^2 G_{k-1}^2}{IIP_{3,k}^2} \tag{2.26}$$

where $IIP_{3,k}$ and G_k are the voltage IIP_3 and voltage gain for the block k. If one block dominates the overall third-order nonlinearity of the system, the IIP_3 can be estimated as BEHZAD (1995):

$$IIP_{3,overall} \approx min\left[IIP_{3,1}, \left(\frac{IIP_{3,2}}{G_1}\right), \left(\frac{IIP_{3,3}}{G_1 G_2}\right), \ldots\right] \tag{2.27}$$

2.4 Receiver Dynamic Range

The dynamic Range (DR) of a receiver is defined as the ratio of the maximum input level that the circuit can tolerate, to the minimum input level that is still detectable. The quantitative definitions differ from application to application. In analog circuits such as A/D converters, it can be defined as a ratio between the “full-scale” (FS) input level and

the input level for which SNR=1. In RF receivers, however, it is very hard to define FS input level. The commonly used method is to define the upper limit of the input power as the maximum two-tone input level at which the produced output IM_3 is still below the noise floor. Such a definition is called the "spurious-free dynamic range" (SFDR) RAZAVI (1998).

By rewriting Eq. 2.25, we have:

$$P_{in}|_{dBm} = \frac{2\,IIP_3|_{dBm} + IM_3|_{dB}}{2} \tag{2.28}$$

The integrated noise floor over the bandwidth (N_{in}) at the input of a receiver is given by:

$$N_{in}(dBm) = NoiseFloor\,(dBm) + 10log(BW)\,(dB) \tag{2.29}$$

The *input referred* integrated noise floor at the *output* of the receiver is then given by:

$$N_{out,in}(dBm) = N_{in}(dBm) + NF(dB) \tag{2.30}$$

The input referred third-order intermodulation product must be equal or less than $N_{out,in}$. This gives us:

$$P_{in,max} = \frac{2IIP_3 + N_{out,in}}{2} \tag{2.31}$$

Since the lower bound of the input power is the sensitivity or minimum detectable signal (MDS) of the receiver, the spurious-free dynamic range is:

$$DR = P_{in,max} - Sensitivity \tag{2.32}$$

2.5 Receiver Architecture Reviews

The previous sections presented the basic requirements of receiver functionalities and figures of merit. We now move our focus to methods for designing receiver systems that meet both selectivity and sensitivity requirements. This section will review the two most popular receiver architectures, heterodyne receivers and homodyne receivers. The contents of this section follow the reviews in LIMKETKAI (1999).

2.5.1 Heterodyne Receiver

The heterodyne architecture has been used in wireless receivers for almost a century and provides superior sensitivity and selectivity compared to other architectures LEE (1998). The basic block diagram of the receiver is shown in Fig. 2.7. Immediately after the antenna, there is an RF bandpass filter, used to filter out-of-band signals, followed by a low-noise amplifier (LNA), an image-reject filter, an RF mixer, a channel select filter, an IF mixer, and finally a low-pass filter and baseband processor.

The main concept of this architecture is that the frequency translation process is divided into two steps. The first is the transition of a signal from radio-frequency (RF) to the intermediate frequency (IF). The second is the frequency translation from IF to baseband. The channel filtering takes place at the IF frequency by a bandpass filter with fixed center frequency at the IF. This means that the channel selection takes place at the first mixing process by selecting the local oscillator (LO) frequency, such that the RF signal

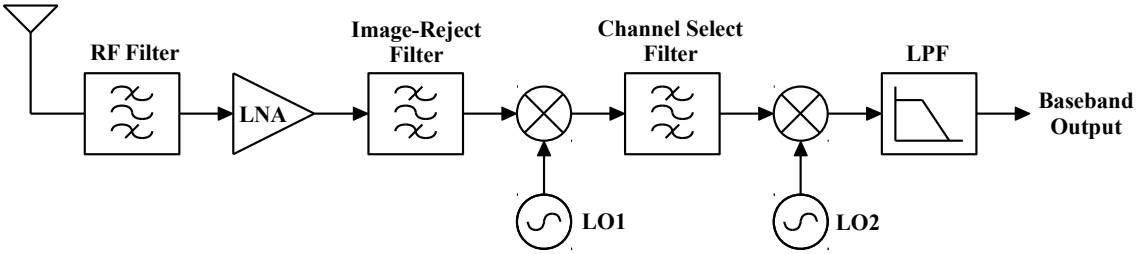


Figure 2.7: Heterodyne receiver architecture

is shifted down by different amounts to locate the desired channel at the fixed IF. Performing channel filtering at the fixed IF frequency greatly relaxes the requirements on the channel-select filter. Channel filtering at the RF frequency would require a tunable RF filter with prohibitively high quality factor (Q).

The RF bandpass filter is a fixed-frequency filter that attenuates out-of-band signals. The low-noise amplifier then provides primary gain for the receiver front-end. As shown in section 2.2, this first block in the receiver chain (besides the bandpass filter) has significant impact on the overall noise in the system. Thus, the main objective of the LNA design is to provide large gain with minimal noise. The other constraint in the LNA design is that its input impedance must match the output impedance of the RF filter, which is usually 50 Ω.

Since the same frequency components at IF frequencies can be created by RF signals on both sides of the LO, an undesired image signal will be superimposed on the desired signal after the first mixing (Fig. 2.8). This image signal can be comparable in magnitude to the desired signal, and may obscure all the information if not treated properly. In this case, an image reject filter is used before the first mixing to attenuate the image of the desired RF signal.

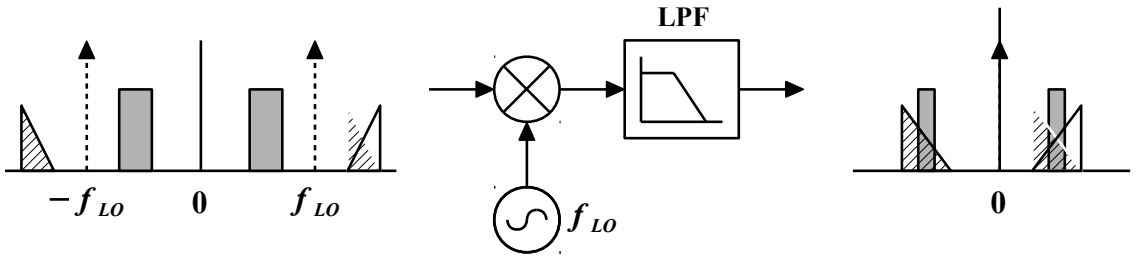


Figure 2.8: Image problem

Although the RF bandpass filter suppresses the image signal to some extent, it will be amplified by the LNA before mixing. This is why the image-reject filter is placed immediately before the mixer. This filter also suppresses noise in the image band.

The heterodyne architecture provides superior selectivity performance due to the benefits from including the IF stage. However, it requires many functional blocks in the system, and many of the blocks are very hard to integrate on-chip. For example, the image-reject and channel-select filters are difficult to implement on-chip due to the relatively low quality factor (Q) of the on-chip inductors. The need for additional off- chip components results in higher passive component costs, chip pin count, and extra board areas.

2.5.2 Homodyne Receiver

For a homodyne receiver (Fig 2.9), the RF signal is downconverted directly to DC (or near-DC) by matching the LO frequency to the center frequency of the RF passband. In the direct-conversion case, where the signal at RF is converted to baseband directly, the signal is placed on both sides of the LO frequency, as shown in Fig. 2.10. If complex modulation is used, which is more bandwidth-efficient, there will be garbling due to negative frequency components going to positive frequencies and vice versa, and an image-rejection mechanism will still be required. However, since the image is the mirror of the signal itself, the power level of the image is the same as the level of the desired signal. As a result, the image-rejection requirements can be relaxed and could be achieved with simple image-reject mixer architectures. In addition, since the channel filtering is now done at baseband, it is possible to implement it as a high- order on-chip low-pass filter.

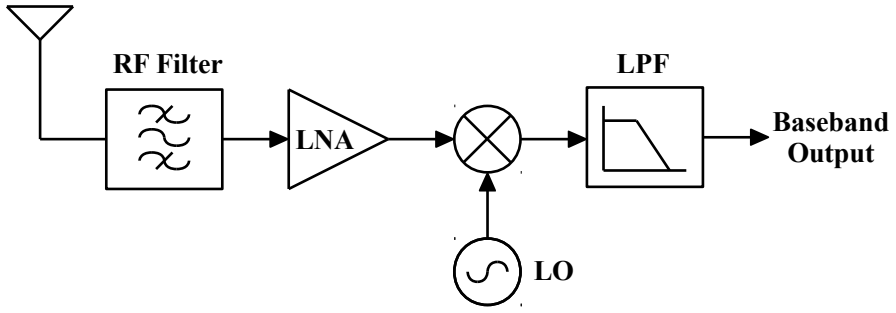


Figure 2.9: Homodyne Receiver

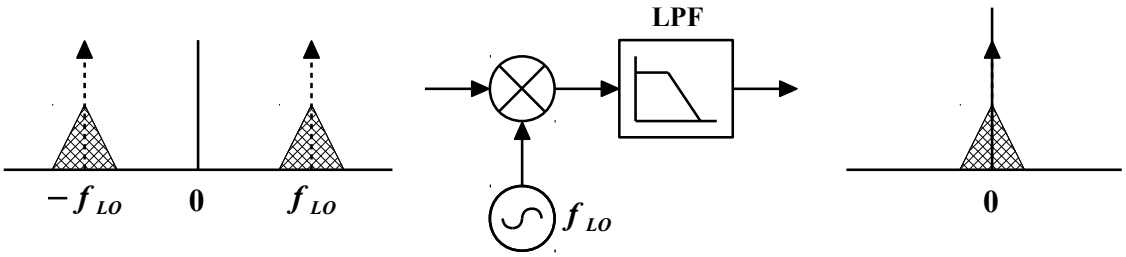


Figure 2.10: Direct-conversion frequency plan

Direct-conversion systems, however, do have some serious problems not present in heterodyne systems. Because the signal is now mixed directly to DC, any DC offset in the receiver path can corrupt the desired signal or saturate the signal path. The unwanted DC offsets can be removed by placing an AC coupling capacitor at the mixer output. However, this may adversely impact the bit-error-rate, since the signal energy at DC will be removed as well. In high-bandwidth systems such as wireless LANs, the use of an on-chip AC coupling capacitor might be acceptable without significant penalties YEE et al. (2000). However, in a system with narrower channel bandwidths, the AC coupling capacitors, if used, are of such a size such that they must be placed off-chip HULL; CHU; LEONG THAM (1996). Techniques used to reduce the DC content of the signal through coding or redefinition of the baseband signal can be used to alleviate this problem. Another approach to removing the offset is to use the training signal to estimate the existing DC offset. Based on this estimation, the offset can be removed or omitted from the mixer

output CAVERS; LIAO (1993). However, this method does not address dynamic DC offset or $1/f$ noise problems.

An alternative technique for addressing the DC offset problem in the direct- conversion receiver is the use of low-IF architecture STEYAERT et al. (1998). In this case, the RF signal is down-converted to a very low IF, instead of baseband. In this case, the DC offset problem is relaxed, since the power at DC can be removed by using an on-chip AC coupling capacitor without significantly affecting the desired signal. However, the image becomes a larger problem; in this case, the image power is set by the blocking profile and usually grows stronger as the frequency moves away from the carrier. To minimize the image rejection requirement, the IF frequency is usually not more than one or two channels away from the DC, where the blocker levels are still relatively low. All of the image rejection must be performed with a Weaver-like structure or polyphase filter (see next section) and this strongly depends on the matching between the I and Q paths of the receiver. The other drawback of this architecture is that it requires higher bandwidth baseband blocks because the signal is now moved to a higher frequency.

2.5.3 Image-Reject Mixers and Complex Filters

Several systems have been proposed to solve image problems in receivers without using an off-chip image-reject filter. These systems are called image-reject architectures. The most common are Hartley and Weaver image-reject mixers, these are reviewed in this section. More complete descriptions and analysis of these architectures can be found in RAZAVI (1998), MARTIN (2004).

2.5.3.1 Hartley Architecture

The Hartley architecture is shown in Fig. 2.11. Note that the 90° phase-shifter is a Hilbert transformer with the transfer function:

$$H(j\omega) = -jsgn(w) \tag{2.33}$$

The multiplication of the RF signal with the 90° phase-shifted LO followed by the 90° degree phase-shift inverts the signal on one side of the LO, thus distinguishing the signal from the image. Adding this to the signal that is downconverted with non- phase-shifted LO leads to image-rejection. A disadvantage of this architecture is the need for a wideband phase-shifter that provides 90° phase shifts for the entire signal bandwidth.

2.5.3.2 Weaver Architecture

Unlike the Hartley architecture, the Weaver architecture uses two additional mixers placed after the low-pass filters to perform the phase-shifting instead of using a wideband phase shifter. The RF signal is first downconverted to an intermediate frequency, then downconverted once again to the "final" IF. After the first down conversion, one path is multiplied by the sine wave, which is simply the phase-shifted cosine wave, equivalently downconverting the signal to the output frequency and phase- shifting it by 90° at the same time. The other path, which is multiplied by the cosine wave, is downconverted without the phase shift. As in the Hartley architecture, summing these two paths results in image rejection.

An advantage of using the Weaver architecture is that the wideband phase shifter is no longer needed. Although the 90° phase shifters for the LO quadrature signals are still needed, they are narrowband and easier to design.

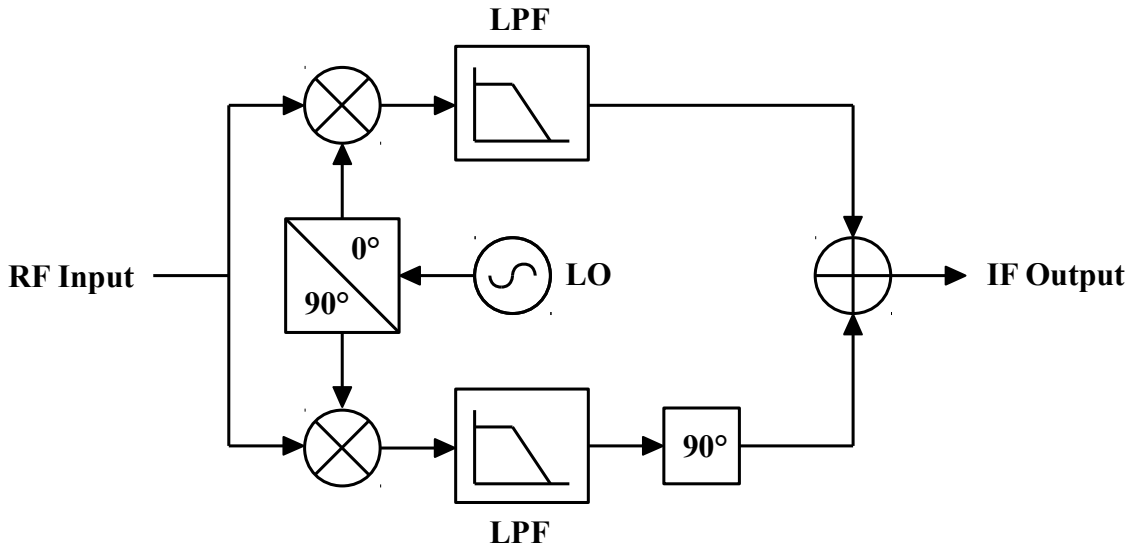


Figure 2.11: Hartley Architecture

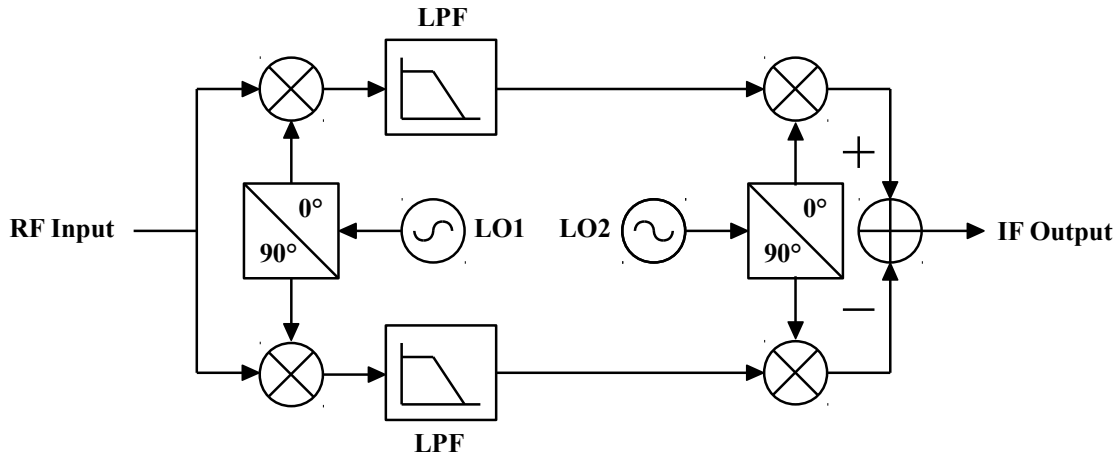


Figure 2.12: Weaver Architecture

2.5.3.3 Complex Filters

Besides image-reject mixers, complex filters are important and widely used in receiver designs, especially in low-IF architectures RUDELL et al. (1997), CROLS; STEYAERT (1998). Complex filters use cross-coupling between the real and imaginary signal paths in order to realize filters with transfer functions that do not have the conjugate symmetry (in the frequency domain) of real filters. This implies that their transfer functions have complex coefficients. The filters can be realized using basic operations, i.e., addition, multiplication, and delay operations for discrete-time digital filters, or the integrator operator for continuous-time analog filters. More information on complex mixers is given in MARTIN (2004).

2.6 Multi-Band Receivers Using Broadband Front-End

A recent trend in the electronics industry has been to integrate many features, including multi-band multi-standards compatibility, in a single handheld device. This has

created a need for receivers that are compatible with as many standards as possible. In this section, we will focus on preliminary architectures and issues in designing universal radio front-ends. We will begin by discussing the challenges in designing a broadband receiver. An important issue is that most existing receiver topologies are designed for a fixed single band, or only a few bands ZARGARI et al. (2004), ERDOGAN et al. (2005). Next, we will investigate the possible implementations for a universal radio receiver using architectures modified from those presented earlier in this chapter. We will compare topologies in terms of their suitability for integration and multi-band capabilities. Finally, we will give a performance estimation of a broadband receiver based on the selected topology.

2.6.1 Possible Front-end Implementations

Unlike conventional narrow-band receivers, universal receiver front-ends must be able to detect and process signals at different frequency bands. Since the operations are still narrow-band, one way to implement the receiver is to use a high-Q tunable RF bandpass filter for frequency band selection, in conjunction with a broadband LNA and mixer, as shown in Fig. 2.13. The RF filter is required in order to attenuate any out-of- band jammers and relax the front-end linearity requirements. For example, the out-of- band jammers could be as high as 0 dBm for the GSM standard, as shown in Fig. 2.3.

Such a high-Q tunable RF bandpass filter is difficult if not impossible to implement on a silicon substrate (such as CMOS IC) using current technology RAZAVI (1998). However, RF MEMS technology has shown promising results NGUYEN (2004) and could become a commercially available option in the future.

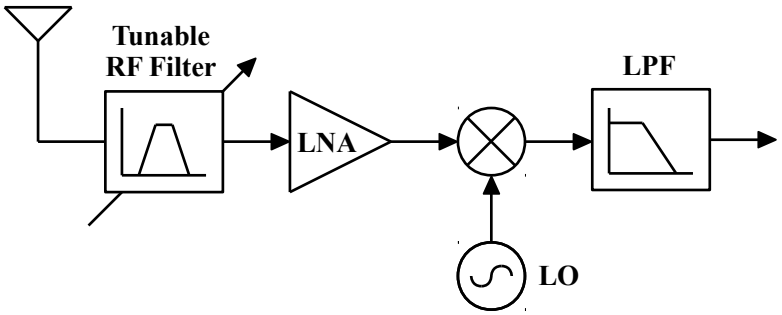


Figure 2.13: A multi-band multi-mode receiver utilizing a tunable RF bandpass filter

The need for a RF tunable filter can be avoided by implementing the “effective” tunable RF filter with several high-Q RF bandpass filters placed in parallel, each covering a frequency band for the intended application. Switches are needed to select which frequency band to use at a given time, as shown in Fig. 2.14. Although this method is acceptable for implementing a few narrow frequency bands, it would become impractical for generic universal radio or configurable radio, where the receiver must be able to operate in any band in the required frequency range. Moreover, these switches need to have low loss and high linearity at high frequency, both of which are not achievable by CMOS devices.

One straightforward solution for the problem of having too many RF bandpass filters is to not to perform any filtering at all. This leaves the broadband receiver with no bandpass filters in the front-ends, as shown in Fig. 2.15. Because there is no bandpass filtering, any large interfering signals can saturate the signal path or create intermodulation products that overtake the desired signal. For standards with stringent out-of-band

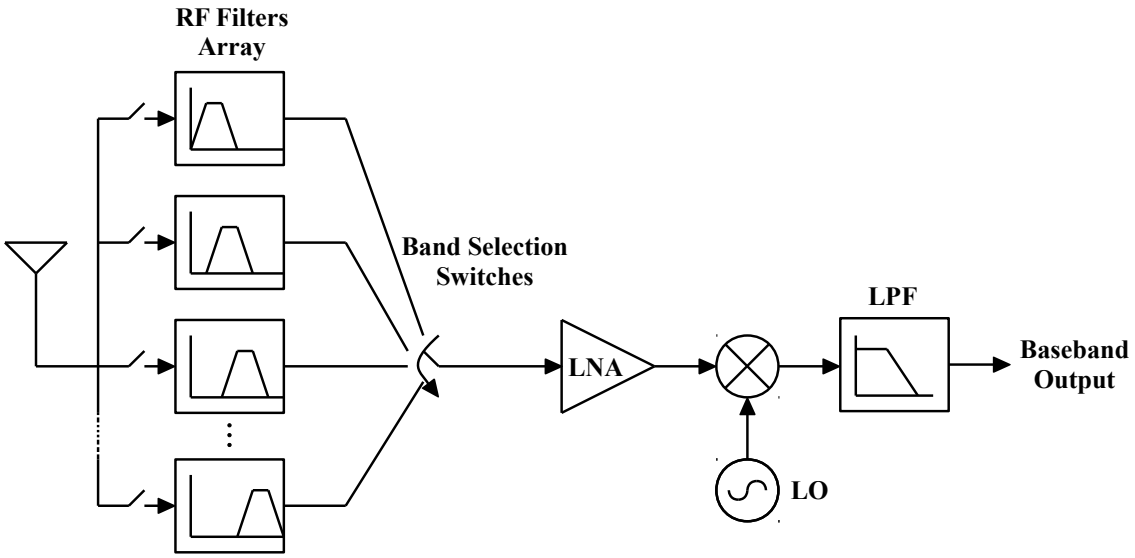


Figure 2.14: A receiver using multiple RF filters and switches

jammer requirements (GSM, for example), having no out-of-band attenuation requires an extremely linear receiver front-end, which is very difficult, if not impossible, to implement in modern CMOS technologies. For some standards such as wireless LANs, there is no out-of-band blocking requirement for the standard, and the front-end linearity specifications can be relaxed. However, a high-linearity front-end is still desirable in this case due to possible jamming situations in real-world applications.

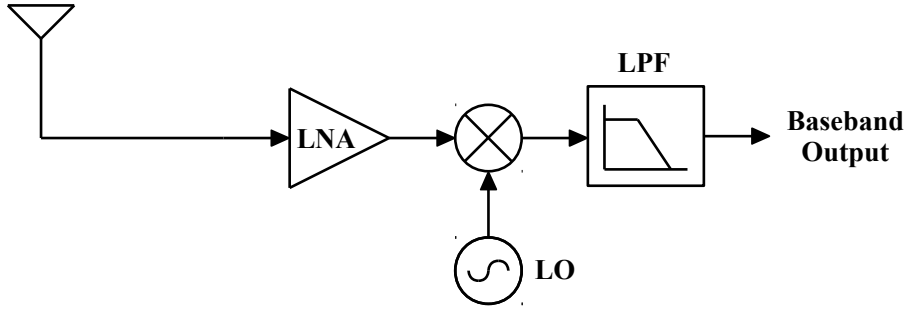


Figure 2.15: A broadband receiver with no RF bandpass filtering

Active research has been done on implementing a receiver that can tolerate large out-of-band jammers without using filters. For example, an active filtering technique has been proposed for removing an out-of band blocker without using an extra SAW filter in DARABI (2007). The circuit employs a feed-forward filter path, and the high-Q characteristic of the filter is realized by using a translinear loop.

If the receiver is broadband, there will be problems with harmonic distortion and harmonic mixing, as well as intermodulation distortion problems that also exist in narrowband receiver front-ends. For example, if the intended receiving frequency can be anywhere from 0.5 MHz to 5 GHz, a strong signal at 0.8 GHz will create a third- order harmonic distortion at 2.4 GHz and will interrupt any desired signals at that frequency. Likewise, if the desired signal and LO are at 0.8 GHz (narrow channel bandwidth), a strong signal at 2.4 GHz will mix with LO harmonics locating at $3f_{LO}$ and may corrupt the desired signal. Moreover, signals at 0.9 GHz and 2.4 GHz could mix and create an

IM_2 that corrupts any desired signals at 1.5 GHz. The problems of harmonic mixing and wideband harmonic distortion could be alleviated by:

1. Using harmonic reject mixers that suppress harmonic mixing at near-LO harmonics such as at $3f_{LO}$ at $5f_{LO}$. An example of such a mixer can be found in WELDON et al. (2001) and has been used in BAGHERI et al. (2006).
2. Employing differential circuits in the RF front-end paths to suppress even- order harmonics or intermodulation.
3. Limiting the ratio between the highest and lowest frequency of the intended receiving signals to less than two by using a band-pass filter. In this case, harmonic distortions of an incoming signal will fall out-of-band and will not interfere with the intended receiving signal. In addition, any IM_2 from two strong in-band signals will fall out of band since their channel separation will always be less than the minimum intended receiving frequency. This relaxes the harmonic mixing problems as well.

Option (3) could be modified for wider frequency band coverage by using multiple RF bandpass filters, each of which covers a "group" of bands, as shown in Fig. 2.16. For example, one might use a filter with 0.8 GHz to 1.5 GHz passband responses to avoid any mixing between 0.9 GHz and 2.4 GHz signals falling in-band, and use another filter covering 1.4 GHz to 2.7 GHz to process the signal at 2.4 GHz. Although this might appear similar to the architecture in Fig. 2.14, the number of required RF bandpass filters could be vastly different. For example, to cover the frequency bands from 0.5 GHz to 5 GHz, the number of filters needed in this topology would be only 4-6, no matter how many standards exist in the range. (The 4-6 variation is due to the amount of overlapping and the chosen frequency ratio.) However, this architecture would likely require out-of-band blocking and linearity requirements similar to those without any bandpass filter. If needed, multiple broadband LNAs can be used for signals from multiple frequency groups as well.

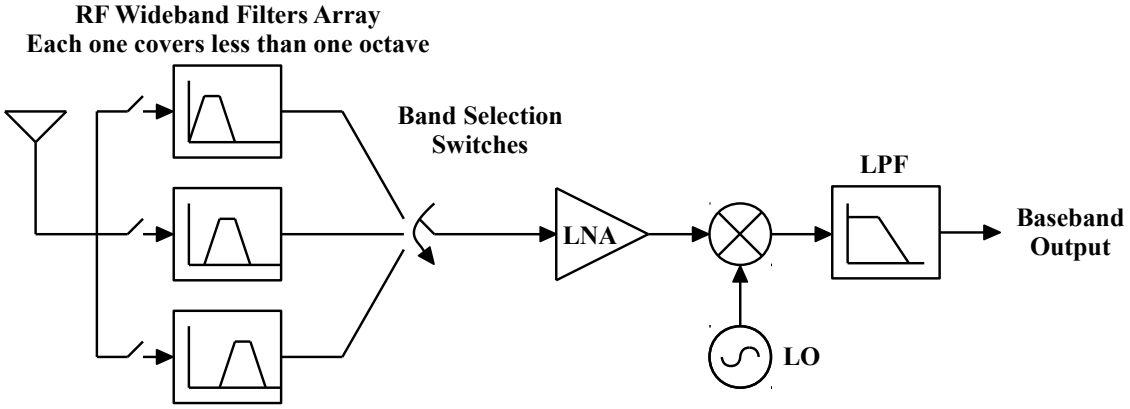


Figure 2.16: A receiver with multiple "wideband" RF bandpass filter

2.6.2 Broadband Receiver Prototype Example

From the previous section, we can see that the key components are broadband front-end building blocks regardless of receiver topologies. In this section, we will examine the basic relationships between the receiver and building block specifications in a prototype

receiver. As a derivative example, the specification requirements of the prototype will be based on multiple standards presented in Table 1.1. Starting with the architecture of the receiver prototype, we will then discuss system parameters such as noise figure, linearity, and dynamic range, as well as block-level specifications.

2.6.2.1 Prototype Receiver Architecture

The conceptual diagram of the receiver can be simplified as shown in Fig. 2.17. In the figure, the major receiver building blocks include low-noise amplifiers (LNA), down-conversion mixers, a frequency synthesizer (for LO signal generation), low-pass filters, variable-gain amplifiers (VGA), and analog-to-digital data converters (A/D).

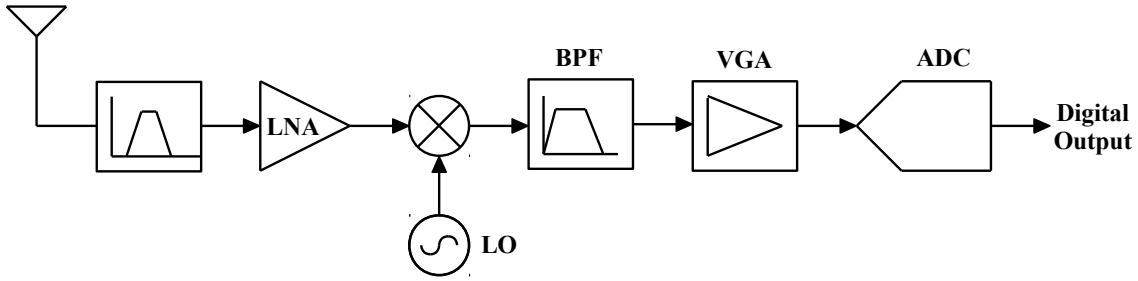


Figure 2.17: Conceptual diagram of the receiver

In this lineup, the LNA is broadband, but it could be designed as one broadband LNA or several narrow band LNAs in parallel. The I/Q image-rejection mixers down-convert the incoming signal from RF to IF frequency[1]. The LO signal is supplied by the frequency synthesizer. The synthesizer needs a voltage-controlled oscillator (VCO) that has a wide frequency tuning range in order to work with multiple bands and standards BERNY; NIKNEJAD; MEYER (2005). Also, it is necessary to have a channel bandwidth adjustment scheme that accommodates different channel bandwidths for different standards. Channel bandwidth adjustments can be implemented using the direct conversion frequency plan with a tunable low-pass IF filter, or a low-IF architecture with a tunable bandpass IF filter. The first approach is simpler but may suffer from the problems with DC offset and 1/f noise, especially if the channel bandwidth is low, as in GSM standards . The second approach, on the other hand, does not have low-frequency problems, but the filter design is more complicated and requires good image rejection. If needed, a low-pass filter with DC offset cancellation or AC blocking capacitors could also be used in a low-IF architecture. However, this would result in higher dynamic range requirements for the VGA and the A/D, since the adjacent channel blocker (located near DC at IF) will not be filtered out.

2.6.2.2 Basic System and Building Block Requirements

As an example, the targeted receiver requirements will be based on multiple standards shown in Table 1.1, and repeated below in Table 2.1 for important receiver requirements.

To meet the requirements of all the standards in Table 2.1, the receiver (not just the front-end) needs to have the following specifications:

- Frequency range: 0.9 GHz - 5 GHz
- RF Channel bandwith: 200 kHz - 20 MHz

[1]It should be noted that the above conceptual diagram shows only one mixer.

Table 2.1: Receiver requirements for different wireless standards

Range	WAN		LAN	PAN	MAN
System	GSM/DCS	UMTS	802.11a	Bluetooth	DECT
Frequency	0.9/1.8 GHz	2 GHz	5 GHz	2.4 GHz	1.9 GHz
Channel spacing	200 kHz	5 MHz	20 MHz	1 MHz	1.728 MHz
Rx NF	9 dB	9 dB	7.5 dB	23 dB	18 dB
Rx IIP_3	-18 dBm	-4 dBm	- 20 dBm	-15 dBm	-22 dBm
Phase noise	-141 dBc@3M	-150 dBc@135M	-102 dBc@1M	-105 dBc@1M	-99 dBc@2.2M

- Noise Figure < 7.5 dB
- IIP_3 > -4dBm
- Phase Noise: -141 dBc @ 3 MHz

Aside from the parameters shown in Table 2.1, receiver designs have many other requirements. Some examples of these specifications include: IIP_2, image rejection, input compression and desensitization, DC offset corrections, turn-on and turn-around time, input impedance matching, and filter ripple and group delay requirements. In addition, several issues that arise specifically with wideband receivers need to be considered, and will be discussed in section 2.6.1.

In the following analysis, however, we focus only on the requirements for noise figure, IIP_3, signal level plan, and output range, since these performance metrics have the greatest impact LNA and mixer designs, and these two blocks are the focus of this dissertation.

The specifications in Table 2.1 are for a receiving path that includes everything from an antenna to the A/D outputs. In practical applications, any losses due to PCB traces or passive components at the receiver input will directly increase the overall system noise figure. Assuming that the total loss between the antenna and the chip pins is 3 dB, the total noise figure at the receiver chip input needs to be 7.5 dB - 3 dB = 4.5 dB. The system IIP3, on the other hand, could be relaxed by the amount of loss before the input. In this case, the IIP_3 specifications can be reduced to (-4 dBm - 3 dB) = -7 dBm at the chip input. However, since the amount of loss varies as frequency changes, and the exact amount of loss could be higher or lower than 3 dB as a design margin, the IIP_3 target should be kept at -4 dBm.

If we allocate 1 dB of noise figure degradation from blocks following the LNA, the LNA itself needs to have noise figures of 4.5 dB - 1 dB = 3.5 dB or better. For IIP_3, if the IF filter provides sufficient stop-band rejection, any subsequence blocks (such as VGA and A/D) will have minimal impact on the system IIP_3 since any interference will be highly attenuated at the filter output. As a result, the total front-end IIP_3 can be estimated using (2.26) along with the gain and linearity profiles of the LNA, mixers, and IF filters. An example of an RF front-end building block specification that meets the noise figure and IIP_3 requirements (NF < 4.5 dB, IIP_3 > -4 dBm) is given below:

In Table 2.2 two examples of front-end building block specification were given. The specifications given to front-end 1 were more demanding on individual blocks such as: the IIP_3 for mixer. A second set of specifications was given to front-end 2, in this case the linearity for the mixer was relaxed at the cost of a more demanding noise figure for the LNA. This noise figure may not be so difficult to achieve, since there are works reported on the literature on that subject BRUCCOLERI; KLUMPERINK; NAUTA (2004).

Table 2.2: Example of LNA, mixer and filter specifications

Front-end Blocks	Front-end 1			Front-end 2		
	Gain (dB)	NF (dB)	$IIP_{3,1}$ (dBm)	Gain (dB)	NF (dB)	IIP_3 (dBm)
LNA	16	3.5	0	13.5	2.5	3
Mixer	15	10	15	10	10	10
Filter and subsequence blocks	50	20	30	57.5	20	30
Cascaded (LNA-Mixer-Filter)	81	4.1	-3.1	81	4.2	-3.63

Another important design consideration is the signal level plan, or how the signal level is adjusted along the receiver path. More specifically, the receiver gain control and A/D interface need to be chosen so that:

1. There is enough gain to meet the signal level requirement when the incoming signal level is low.
2. The receiver has enough dynamic range to handle significant interference in the event that the desired signal is weak (near-far problem). Even with channel filtering, the incoming blockers can be substantially larger than the desired signal at the receiver output. This dictates the receiver linearity requirement, channel filter out-of-band rejection, and A/D dynamic range.
3. Finally, in the event that the desired receiving signal is very strong, the minimum receiver gain (from LNA to VGA) needs to be low enough so that the output signal level will not be compressed along the signal path (likely at the VGA output or A/D input). This requirement is different from that in (2) above because the desired signal will not be attenuated by the filter as in the previous case.

For example, if a 10-bit A/D with $1V_{p-p}$ input full-scale voltage swing is used at the receiver output, the A/D dynamic range will be approximately 60 dB (around 6 dB per bit) with 1 mV LSB. The required maximum gain of the receiver can be calculated from the LSB of the A/D and the required signal level above the A/D quantization noise. For example, if the system requires the rms signal level to be 30 dB above the A/D LSB, and the required sensitivity is -100 dBm (-113 dBVrms), the required maximum receiver gain is then:

$$RxGain_{max} = (30 + 20log(1m)\,dBVrms) - (-113\,dBVrms) = 83\,dB \tag{2.34}$$

The required minimum gain of the receiver, on the other hand, can be calculated from the A/D full-scale range and the largest possible receiving or interfering signal. Because an unwanted signal will be heavily attenuated by the IF filter, the minimum gain of the receiver can be determined by the maximum input level of the desired signal and the A/D full-scale range (which is 60 dB above LSB). If the maximum desired input level is -15 dBm (-28 dBVrms), the required minimum receiver gain is then:

$$RxGain_{min} = (60 + 20log(1m)\,dBVrms) - (-28\,dBVrms) = 28\,dB \tag{2.35}$$

Usually, we can attenuate the desired signal at the LNA input, since noise figure is not a concern in this situation (the signal level is already high, so the SNR degradation is

not a concern). If a large interference is present when the desired signal is low (near-far situation), the LNA gain must be kept high in order to maintain the low noise figure of the system, and the filter rejection needs to be large enough to prevent any signal compression at the receiver output (A/D input). For example, if the interference can be as high as -20 dBm (-38 dBVrms) while the desired signal is at -100 dBm (-113 dBVrms), the receiver gain needs to be 83 dB according to (2.28), while the rejection needs to be high enough to keep the inference level below the A/D range. This can be written as:

$$\begin{gathered}(60+20log(1m)\,dBVrms) > (-38\,dBVrms) + (83\,dB) - Rejection \\ Rejection > 45\,dB\end{gathered} \tag{2.36}$$

Another requirement in this situation is that the blocks preceding the IF filter are linear enough to handle the -25 dBm interference.

3 ACTIVE DOWNCONVERSION MIXERS FOR MULTI-BAND RECEIVERS

3.1 Introduction

The mixer is one the most important blocks in virtually all wireless receivers. The primary function of a mixer is to perform frequency translation of the signal between the carrier frequency and baseband. The mixer's performance strongly affects the overall performance of the receiver, and it is a major component in the receiver front-end. In section 3.2 we will review the Gilbert-cell mixer. Section 3.3 covers the improvements for the Gilbert-cell mixer. Section 3.4 presents the linearity performance of the Gilbert-cell mixer based on Volterra series analysis, section 3.5 will review mixers for multi-band multi-standard front-ends. Section 3.6 presents a modified Gilbert-cell mixer suitable for multi-band receivers. Finally, section 3.7 gives the conclusions.

3.2 Gilbert-Cell Mixer: Review

One of the most popular type of mixer is the Gilbert-cell mixer. Instead of commutating the RF signals in voltage, a Gilbert-cell mixer commutates the RF signals in current GILBERT (1968). Fig. 3.1 shows an example of Gilbert-cell mixer. A pair of transistors converts the RF input voltage into a current, and then a differential pair of transistors commutates the current to the complementary IF outputs at each LO period. Because it doesn't need a large swing between the gates of the differential pair to commutate the current, the requirement of the LO drive is greatly reduced. A Gilbert-cell mixer provides better isolation between LO and RF than a passive mixer because there is no direct signal path from LO to RF. However, there is still LO leakage into the IF port through the parasitic capacitors between the gate and the drain of the switches in a single balanced Gilbert-cell mixer. A double balanced Gilbert-cell mixer solves this problem by coupling differential LO signals into the same IF output. As shown in Fig. 3.1, each side of IF output is connected with two switches with 180 degree phased LO signals so that the LO leakage from the two switches cancels each other. Therefore, only the mixed products of RF and LO appear at the IF outputs. Various modifications can be made both to the input stage and the load stage resulting in the so-called Gilbert-cell-like mixers KIVEKAS et al. (2001), PRETL et al. (2000). The common feature is the presence of differential input transconductor and four current commutating switches in double balanced configuration.

In the following subsections, low-voltage architectures, conversion gain, noise and linearity of a double balanced Gilbert-cell mixer are discussed.

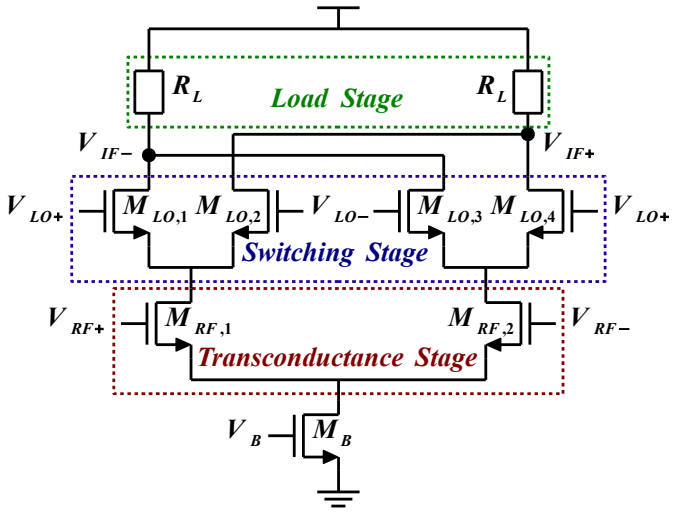


Figure 3.1: Classic CMOS Gilbert-cell type mixer

3.2.1 Low-Voltage Architectures

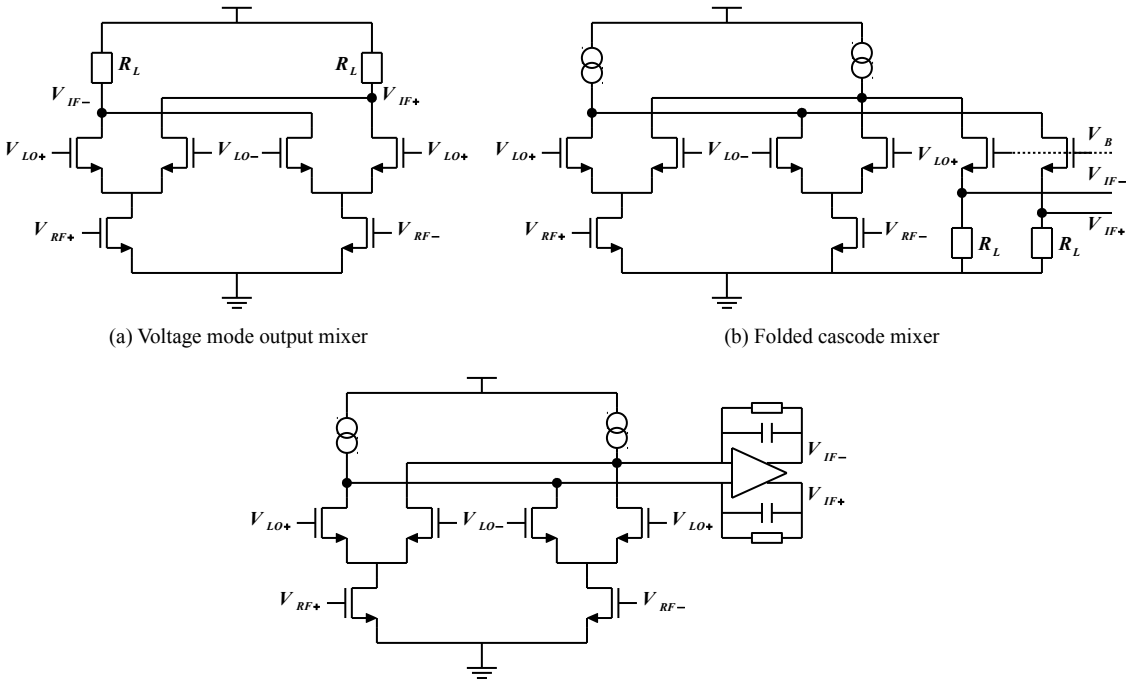
Modern radio frequency transceivers implemented fully in CMOS technologies have to operate under low supply voltages because high-speed MOS transistors required for radio frequency applications have very thin gate oxide which can be easily damaged if applied voltage exceeds a breakdown value. As gate oxide thickness decreases with technology scaling, breakdown voltage decreases simultaneously, necessitating the supply voltage to scale down as well.

In order to maintain reasonable performance of downconversion mixers despite low voltage operation, the conventional Gilbert-cell architecture has to be replaced with some modified topology. To increase the available voltage headroom, a so-called pseudo-differential input stage which doesn't contain a tail current source, as depicted in Fig. 3.2a, can be used. By removing the tail current source, odd-order nonlinearity is improved simultaneously because the saturation mechanism caused by the tail current is eliminated. Unfortunately, the common mode rejection ratio (CMRR) is degraded together with the even-order nonlinearity.

Further savings in voltage headroom can be achieved by a current boosting technique as described e.g. in KIVEKAS et al. (2001). The technique reduces voltage drop across load resistors by decreasing the amount of biasing current flowing through them and the switching network. This is accomplished by using additional current sources coupled to the drains of the input stage transistors.

Another approach is to utilize an input stage with current reuse as described e.g. in VIDOJKOVIC et al. (2004), VIDOJKOVIC et al. (2005). Similarly to the current boosting approach, the amount of biasing current flowing through the load resistors and thus the static voltage drop are decreased. Additionally, the effective input stage transconductance (and thus the mixer gain) can be significantly increased in comparison with the traditional input stage for the same biasing current consumption.

Yet another technique uses AC coupling between the input stage and the switching stage TANG et al. (2001), allowing to reduce the number of devices stacked between voltage supply and ground. However, inductors are required to cause resonance and thus allow current signal flow to the switches. As inductors occupy a lot of chip area, they make this solution quite expensive.



(a) Voltage mode output mixer

(b) Folded cascode mixer

(b) Opamp based current mode output mixer

Figure 3.2: Low voltage mixer architectures

A very good overall performance at low supply voltage can be obtained by using a so-called current mode output architecture. Two versions, based on a folded cascode topology and a fully differential opamp topology, are shown in Fig. 3.2b and in Fig. 3.2c, respectively. In this case the output current signal is in principle driven into a low impedance node, thereby producing negligible voltage swings at the output of the switching stage. In both cases, care has to be taken to provide sufficiently low impedance not only at baseband but also at frequencies corresponding to the blocking signals. This is more difficult to achieve with opamp based circuit configuration due to its inherent speed limitations.

The current mode output architecture improves switching stage linearity and allows to avoid output voltage signal clipping, which occurs in traditional resistively loaded mixers at high mixer input signal levels. Accordingly, the overall mixer linearity is limited by the input stage.

Both folded-cascode and opamp-based current mode output mixers convert the output current back to voltage in the mixer-IF interface. The opamp-based solution enables higher gain and better large signal linearity in comparison to the folded-cascode approach, because output voltage signal can swing almost rail-to-rail, i.e. it may vary between ground and VDD without clipping. It should be noted, however, that baseband signal processing can be based also on current mode filtering. In such a case, folded cascode or opamp can be replaced with a current buffer having low input impedance.

3.2.2 Conversion Gain

As opposed to passive mixers, a Gilbert-cell mixer can have a positive conversion gain. The conversion gain consists of three parts, the transconductance of the RF input MOS ($g_{m,RF}$), the switching gain/loss of the Gilbert-cell (A_{sw}) and the output impedance

(R_L). The voltage conversion gain is given by Eq. 3.1.

$$CG = g_{m,RF} \cdot R_L \cdot A_{SW} \tag{3.1}$$

Here, A_{sw} is a function of the shape and the amplitude of the LO drive and the over-drive voltage of the switching pair ($V_{od,sw}$). If the LO signal is a square wave with sharp rising and falling edges and its amplitude is larger than $V_{od,sw}$, i.e., the interval time of both the transistors of a switching pair being on is negligible, the switching gain is $2/\pi$, i.e., -3.9 dB. If the LO signal is a sinusoid with a amplitude V_{LO} much larger than $V_{od,sw}$ the switching gain is close to that using a square wave; therefore, the switching gain is close to $2/\pi$. Fig. 3.3 shows the switching gain of a typical Gilbert-cell mixer. The switching gain is proportional to the LO amplitude when the LO amplitude is smaller than the over-drive voltage; and it is clamped to the point which is slightly less than $2/\pi$ due to the parasitic loss when the LO amplitude is sufficiently large.

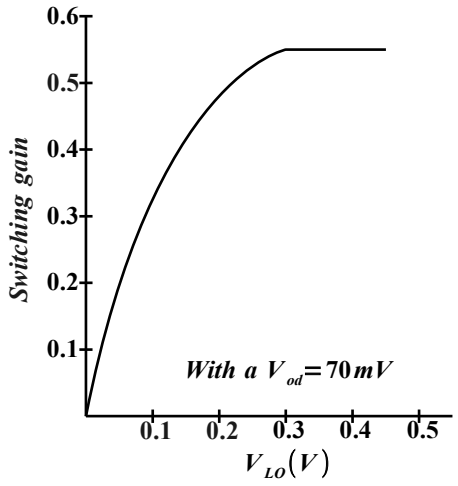


Figure 3.3: Switching gain curve of a Gilbert-cell mixer

The overdrive voltage of the switching transistor depends on the drain current of the RF input transistor and the size of the switching transistor.

Although a larger LO drive can provide a higher switching gain, too large a LO drive also degrades the conversion gain because even order harmonics are coupled into the common source of the differential pair, which is also connected to the drain of the RF input transistors. A large LO harmonic can reduce the drain voltage of the input transistor and finally push the transistor into the triode region.

Instead of increasing the LO drive, decreasing the overdrive voltage of the differential pair can increase the conversion gain. DC current stealing is often used to achieve a small over-drive voltage, as is shown in Fig. 3.3. A current source is connected to the common source of the differential pair to steal part of DC current from the drain of the input transistor so that there is less DC current flowing through the differential pair and the over-drive voltage becomes smaller. Only the DC current at the output is reduced while the AC current which contains all the signals remains unchanged.

3.2.3 Linearity

For multi-band receivers, the mixer still remains the limiting element for the overral receiver linearity. The linearity of the Gilbert-cell mixer is often limited by the transconductance of the RF input MOSFETs.

The linearity of the RF input transconductance can be expressed in term of IIV_3 or IIP_3. Short channel MOSFETs generate odd order distortion at the output even with a differential design. Usually the third order distortion dominates when the input signal is small. The input referred third-order intercept voltage point (IIV_3) of a MOSFET is given by Eq. 3.3 SOORAPANTH; LEE (1997), where α is a measure of the channel velocity saturation and the mobility degradation. Let us note that A_{IP3}, described in chapter two, and IIV_3 are the same thing. So for that reason both terminologies are interchangeable.

$$IIV_3 = \frac{4\sqrt{2}}{3} V_{OV} \qquad V_{OV} = V_{GS} - V_T \qquad Long\,Channel \tag{3.2}$$

$$IIV_3 = \sqrt{\frac{8}{3}\frac{1}{\alpha} V_{OV} \left(1 + \frac{1}{2}\alpha V_{OV}\right) (1 + \alpha V_{OV})^2} \qquad Short\,Channel \tag{3.3}$$

$$\alpha = \theta + \frac{\mu_0}{2 v_{sat} L} \tag{3.4}$$

$$IIP_3 = \frac{IIV_3^2}{2R_S} \tag{3.5}$$

Note that the IIV_3 increases with the over-drive voltage V_{OV}. However, the DC power consumption also increases with V_{OV}. There is always a trade off between the linearity and the power consumption in linear circuit design. Since IIP_3 is often used rather than IIV_3 in RF system level design, Eq. 3.5 relates IIV_3 with IIP_3 , where R_S is 50Ω. A more detailed analysis of Gilbert-cell mixer distortion is described in Appendix A.

As Eq. 3.6 is a general expression at circuit abstraction level, we can see that the linearity is strongly related with the bias point of the circuit.

An expression for IIV_3 given by Eq. 3.6, using the nonlinearities of the ACM model transistor was developed, DA SILVA et al. (2008).

$$IIV_{3,ACM} = \sqrt{\frac{8 \cdot g_{m,RF}}{g''_{m,RF}}} \tag{3.6}$$

The value of $g''_{m,RF}$ is the second derivative of the gate transconductance, $g_{m,RF}$. As Eq. 3.6 is a general expression at the circuit abstraction level, we can see that the linearity is strongly related with the bias point of the circuit. This will be useful in the design procedure covered in chapter 4.

3.2.4 Noise

There are three major noise sources in a down-conversion mixer: the noise generated in the RF input transistors, the switching noise and the noise from the output load.

The noise generated in the input transistors is primarily from two parts. First is the drain thermal noise, as is given by Eq. 3.7. The input referred drain noise voltage of this source can also be given by Eq. 3.8.

$$i^2_{d,noise} = 4kT\gamma g_{m,RF} \tag{3.7}$$

$$v^2_{in,thermalnoise} = \frac{4kT\gamma}{g_{m,RF}} \tag{3.8}$$

Eq. 3.9 gives the input referred noise voltage of the flicker noise, where K is a process parameter. Note that the flicker noise is inversely proportional to the frequency and becomes a dominant noise source at low frequencies. For the majority of IF circuits it is desirable to use large-sized transistors so that their corner frequency is lower than the signal band.

$$v^2_{n,flicker}(f) = \frac{K}{WLC_{ox}f} \tag{3.9}$$

Another important noise source in the input transistor is the induced gate noise, whose input referred value is given by Eq. 3.10, where ω is the operating angular frequency, C_{gs} is the gate-to-source capacitance and g_{d0} is the drain conductance when V_{ds} equals zero

$$i^2_{g,noise} = 4kT\delta g_g \tag{3.10}$$

where

$$g_g = \frac{\omega^2 C^2_{gs}}{5g_{d0}} \tag{3.11}$$

The induced gate noise is partially correlated to the drain thermal noise. The noise figure of the mixer can be optimized by use of a proper input impedance. The differential pair switches the RF current between the two transistors at LO frequency. It also contributes noise into the signal path. One noise contribution is from the switching loss and the other is from the noise on the LO signals. The signal-to-noise ratio decreases by the same amount as the switching loss, which in turn increases the noise figure of the mixer. The noise at the gate of the differential pair consists of the phase noise and the thermal noise on the LO signals and the induced gate noise. When the LO amplitude is much higher than the differential pair's over-drive voltage, i.e., the interval of both the transistors of the differential pair is much smaller than the LO period, both the LO thermal noise and the induced gate noise have much less impact than the LO phase noise.

A theoretical analysis undertaken by Terrovitis and Meyer TERROVITIS; MEYER (1999) gives an approximate model for the noise figure of the CMOS Gilbert cell-based mixers. The time-varying power spectral density of noise generated in the RF stage (M_{RF1} and M_{RF2}) is:

$$S^0_{nRF} = \alpha \cdot 4kT \cdot (R_S + 2 \cdot r_{g,RF} + \frac{2\gamma}{g_{m,RF}}) \cdot g^2_{m,RF} \tag{3.12}$$

The time-average output noise power spectral density generated in the switching pair is given by

$$S^0_{nSW}(f) = 8kT \cdot \gamma(\frac{1}{T_{LO}} \int_0^{T_{LO}} G(t) \cdot dt) = 8kT \cdot \gamma \cdot \bar{G}, \tag{3.13}$$

where $\bar{G}$ is the time average of $G(t) = 2\frac{g_{m,LO1} \cdot g_{mLO2}}{g_{m,LO1} + g_{m,LO2}}$, the small signal transconductance of the differential pair. Another switch noise component is flicker noise, which can be modeled as a voltage source in series with the gate. Its time-average power spectral density is given by RAZAVI (1998), where W_{LO} and L_{LO} are the witch and length of each switching transistor, respectively.

$$S_{nflicker,SW}(f) = 2\frac{K}{W_{LO}L_{LO}C_{ox}}\frac{1}{f}, \tag{3.14}$$

The contribution of the flicker noise to the output noise power spectral density is the same as of parasitic gate resistances. However, since flicker noise is no white and Eq. 3.14 yields negligible values at high frequencies, in this case using only the DC Fourier coefficient of $G(t)$ and its contribution can be calculated:

$$S^0_{nflicker,SW}(f) = (\bar{G})^2 S_{nflicker,SW}(f) \tag{3.15}$$

The time-average power spectral density of noise from the LO port is defined as

$$S^0_{nLO}(f) = 4kT(4r_{g,LO})\bar{G^2}. \tag{3.16}$$

Having calculated the noise contribution from the various sources to the output, the mixer noise figure can be estimated. Consider that the load introduces output noise which can be represented by an equivalent noise resistance R_L. The time-average power spectral density of the Gilbert-cell mixer total output noise is

$$S^0_{nMIXER}(f) = S^0_{nRF}(f) + S^0_{nSWITCH}(f) + S^0_{nflicker,SW}(f) + S^0_{nLO}(f) + 4kT(\frac{1}{R_L}). \tag{3.17}$$

The time-average power spectral density of the mixer input noise is

$$S^0_{IN}(f) = 4kT \cdot R_S(c \cdot g_{m,RF})^2. \tag{3.18}$$

where "c" represents the conversion gain of the switching pair alone. So, the single sideband (SSB) noise figure of a Gilbert cell type mixer is :

$$NF_{(SSB)} = 10 \cdot \log\left[\frac{S^0_{nMIXER}(f)}{S^0_{IN}(f)}\right] \tag{3.19}$$

$$NF_{(SSB)} = 10 \cdot \log\left[\frac{S^0_{nMIXER}(f)}{S^0_{IN}(f)}\right]$$

$$= 10 \cdot \log\left[\frac{\alpha}{c^2} + \frac{2(\gamma_{RF} + r_{g,RF} \cdot g_{m,RF})\alpha \cdot g_{m,RF} + 4\gamma_{LO}\bar{G} + 4\frac{K(\bar{G})^2}{W_{LO}L_{LO}C_{ox}}\frac{1}{f} + (4r_{g,LO})\bar{G^2} + \frac{1}{R_L}}{R_S \cdot c^2(g_{m,RF})^2}\right] \tag{3.20}$$

If the useful signal is present in both sidebands around the LO frequency, the double-sideband noise figure is the appropriate noise performance metric:

$$NF_{(DSB)} = 10 \cdot \log\left[\frac{S^0_{nMIXER}(f)}{2S^0_{IN}(f)}\right] = NF_{(SSB)} - 3dB \tag{3.21}$$

3.3 Gilbert-Cell Mixer: Improvements

3.3.1 Current-Bleeding Technique

The current-bleeding technique is an enhancement of traditional Gilbert-cell mixer. This technique improves the conversion gain without a significant degradation of linearity. In order to improve both gain and linearity, we should increase the bias current (I_{BIAS}) of the RF stage without varying the bias current of the switching pair LEE; CHOI (2000).

The current-bleeding technique can be explained more clearly using a single-balanced mixer. Fig. 3.4 shows a single-balanced mixer in which a bleeding current source (I_{BLD}) is added. Without this current source, the total bias current is $I_{BIAS} = I_{D1} + I_{D2}$. With the bleeding current source and without changing I_{D1} or I_{D2}, I_{BIAS} increases to $I_{BIAS} = I_{D1} + I_{D2} + I_{BLD}$.

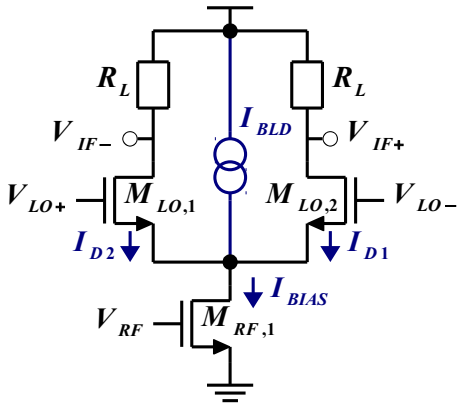


Figure 3.4: Single-balanced mixer with current-bleeding source

Therefore, it will be possible to improve linearity and conversion gain at the same time. However, the total power consumption of the circuit would increase.

Alternatively, it is possible to keep constant the total bias current and thus the power consumption. In this case, by adding the bleeding source, I_{D1} and I_{D2} should decrease. Then, the load resistor R_L must increase to not destroy the bias conditions of the switching pair. It follows that the conversion gain will be improved without improving the IIP_3.

Fig. 3.5 shows the double-balanced Gilbert-cell mixer with the current-bleeding technique. The PMOS transistors $M_{BL,1}$ and $M_{BL,2}$ are used as bleeding current sources. If low voltage operation is required, the PMOS transistors added for bleeding purposes can be replaced by resistive loads.

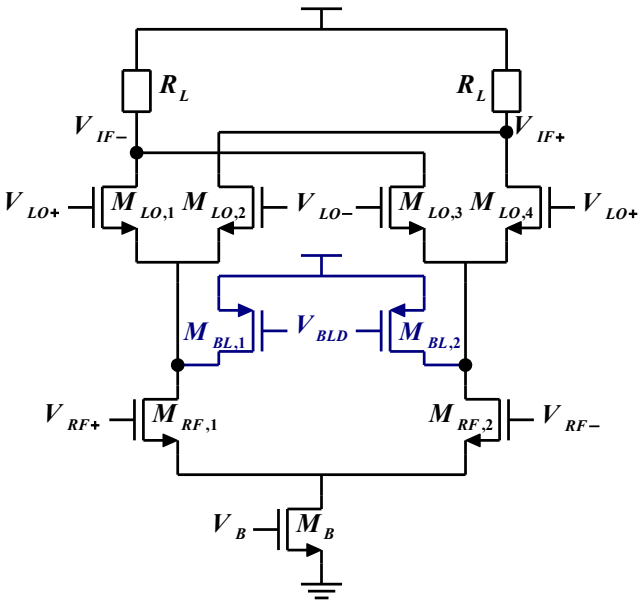


Figure 3.5: Double-balanced mixer with current-bleeding technique

In the Gilbert-cell mixer, the mismatches of the switching pair result in a small amount of flicker noise leaking to the output. Since the mixer is driven by a large sine-wave LO signal, the actual voltage switching the differential pair consists of a sine-wave LO with a noisy base line determined by the flicker noise of the switches. Therefore, the switching event is advanced or retarded by an amount of Δt defined by the switches noise magnitude. This results in a pulse train of random widths Δt, and a fixed amplitude of $2I$ at a frequency of twice the LO frequency, where I is the bias current of the switching pair.

Since the noise pulses have a frequency of twice the LO frequency, the mixer output spectrum consists of a DC term as well as components at the LO even harmonics. The output flicker noise current is the DC average of pulses. One way to improve the flicker noise of the Gilbert-cell mixer is to reduce the *height* of the noise pulses. This could be only accomplished by reducing the bias current of the mixer switches, as the height of the pulses is equal to $2xI$.

Conventionally the current-bleeding technique injects a fixed current to the switching pairs lowering the effective current commutated by them. This reduces the height of the noise pulses, and as a result lowers the switching pair's flicker noise. However, this technique suffers from a few important drawbacks. First, reducing the bias current of the switching pair raises the impedance seen at the their source, allowing more RF current to be shunted by the parasitic capacitance at that node. This reduces the mixer bandwidth and degrades its linearity. Second, the white noise of the current source adds to that of the transconductance stage, increasing the mixer white noise figure.

Since the noise pulses are only present at the switching instant, a *dynamic* current equal to the bias current of each pair at *only* the switching event is injected to the switching pairs. This is sufficient to eliminate the output flicker noise component completely. This *dynamic current injection* method is shown Fig. 3.6, DARABI; CHIU (2005).

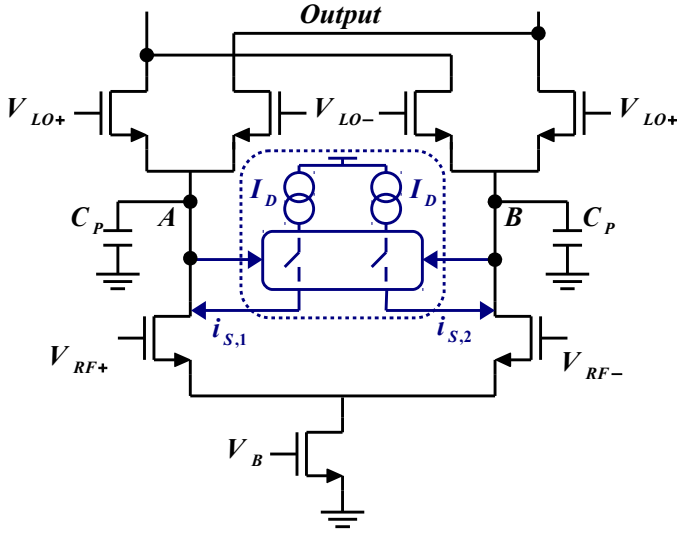


Figure 3.6: Conceptual idea of dynamic current injection

3.3.2 Linearization of Transconductance Stage

There are several mechanisms that originate intermodulation in CMOS downconversion mixers: self-mixing, transconductor nonlinearity, switching pairs non-linearity, and mismatch in load resistors MANSTRETTA; BRANDOLINI; SVELTO (2003).

In the Gilbert-cell mixer, the nonlinearity effects are mostly dominated by the input transconductor. Hence, linearization of the MOSFET transconductor stage is a significant consideration

Considering the input-stage differential pair of the double balanced mixer shown in Fig. 3.1, the Taylor series expansion of the time-varying current $i_{d,RF}$ around a bias point appropriately chosen on the I-V characteristics of M_{RF} is expressed as:

$$i_{d,RF} = g_{m,RF} v_{gs,RF} + g^{'}_{m,RF} v^2_{gs,RF} + g^{''}_{m,RF} v^3_{gs,RF} + \dots \tag{3.22}$$

where $v_{gs,RF}$ is the variation of the gate-to-source voltage around a bias point, $g_{m,RF}$, $g^{'}_{m,RF}$, $g^{''}_{m,RF}$ are the fundamental transconductance, second- and third-order nonlinearity coefficients respectively.

The second- and third-order terms in equation 3.22 are the main degrading contributions of the second- and third-order intermodulation distortion products in RF systems. The IIP_3 is degraded by both the intrinsic third-order distortion and the "second-order interaction" (caused by intrinsic second-order distortion combined with feedback), while IIP_2 originates from intrinsic second-order distortion.

Table 3.1: Overview of distortion source and Linearization techniques (table from ZHANG; SANCHEZ-SINENCIO (2011))

Distortion Sources	g_m				g_{ds}
Linearization Techniques	Intrinsic 2^{nd}-order	Intrinsic 3^{rd}-order	2^{nd}-order interaction	Higher order	
Feedback	√	√		√	√
Harmonic termination		√	√		
Optimal biasing		√			
Feedforward	√	√			√
Derivative superposition (DS)		√			
Complementary (DS)	√	√			
Differential DS	√	√			
Modified DS		√	√		
IM_2 injection		√	√		
Noise distortion Cancellation	√	√			
Post-distortion	√	√			

Obviously the goal of every linearization technique is minimizing $g^{'}_{m,RF}$, $g^{''}_{m,RF}$ for the circuit. In ZHANG; SANCHEZ-SINENCIO (2011) previously reported CMOS LNA linearization techniques, that can be applied to the linearization of the transconductance stage of the Gilbert-cell mixer. Eight different clusters were categorized: a) feedback; b) harmonic termination; c) optimum biasing; d) feedforward; e) derivative superposition (DS); f) IM_2 injection; g) noise/distortion cancellation; and h) post-distortion. Note that DS, IM_2 injection, and noise/distortion cancellation are special cases of the feedforward technique.

Table 3.1 illustrates the distortion sources and the corresponding linearization techniques. Most of the reported linearization techniques focus on suppressing second- and third-order distortion of transconductance. Therefore, linearization of higher order terms (beyond third order) and output conductance still remains an open problem.

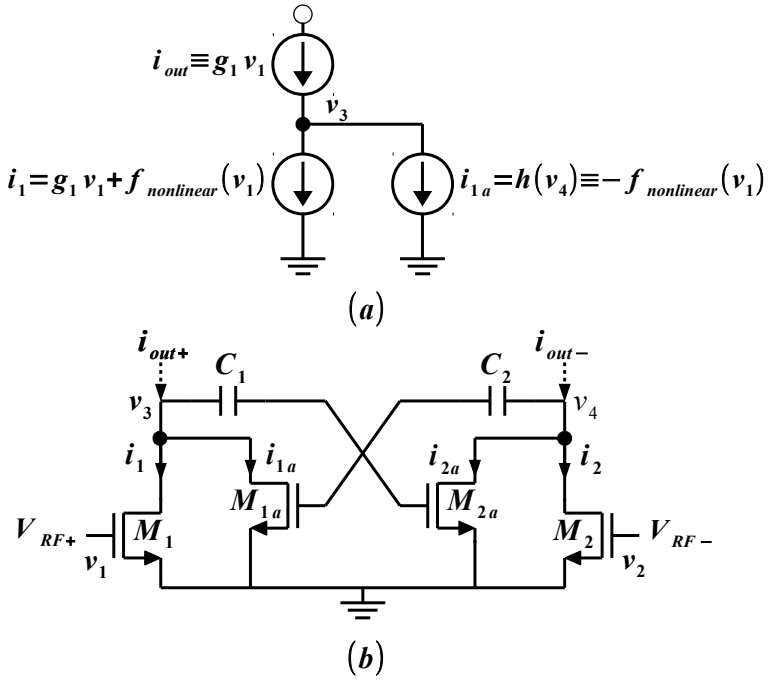


Figure 3.7: a) Post-distortion harmonic cancellation principle. b) PDHC applied to a pseudo-differential pair

From the several linearization techniques that use an auxiliary transistor's nonlinearity to cancel that of the main device ZHANG; SANCHEZ-SINENCIO (2011), the post-distortion harmonic cancellation (PDHC) technique was chosen for the following reason: The auxiliary transistor is connected to the output of main device instead of directly to the input, minimizing the impact on input matching, allowing an all-NMOS implementation, which can be matched very well in layout, resulting in more robust distortion cancellation.

Fig. 3.7 shows the conceptual idea of the post-distortion technique applied to the pseudo-differential pair, an auxiliary transistor which acts as a *linearizer* (M_{1a}) is connected to the output of the main transistor (M_1) cancelling the nonlinear components of the later. The nonlinear currents can be approximated by

$$i_1 = g_1 v_1 + g_2 v_1^2 + g_3 v_1^3 \tag{3.23}$$

$$i_{1a} = g_{1a} v_4 + g_{2a} v_4^2 + g_{3a} v_4^3 \tag{3.24}$$

$$i_2 = -g_1 v_1 + g_2 v_1^2 - g_3 v_1^3 \tag{3.25}$$

where, v_1 and v_4 are the small signal inputs of M_1 and M_{1a} respectively. The cross-coupled configuration of the main and the auxiliary transistor relates v_1 and v_4 by

$$\begin{aligned} v_4 = -i_2 r_{ds} &= g_1 r_{ds} v_1 - g_2 r_{ds} v_1^2 + g_3 r_{ds} v_1^3 \\ &= a v_1 - b v_1^2 + c v_1^3 \end{aligned} \tag{3.26}$$

r_{ds} is the drain resistance of the main transistor (M_1, M_2). The two nonlinear currents i_1 and i_{1a} at the node v_3, yield the output current i^+_{out}:

$$\begin{aligned} i^+_{out} &= i_1 + i_{1a} = (g_1 + g_{1a})v_1 \\ &+(g_2 + a^2 g_{2a} - b g_{a1})v_1^2 \\ &+(g_3 + c g_{a1} - 2ab g_{2a} + a^3 g_{3a})v_1^3 \end{aligned} \tag{3.27}$$

It can be seen that current i_{1a} partially cancels both the second- and third-order terms of the current i_1.

3.3.3 Noise Reduction of Transconductance Stage

Gilbert-cell mixers often exhibit a large amount of noise. This leads to strict requirements for the noise figure (NF) of the low-noise amplifier (LNA) preceding the mixer such that a particular signal-to-noise ratio can be achieved. However, these requirements can be relaxed if the mixer NF is low enough.

One of the major contributors in the mixer NF is the transconductance stage, so the cancellation of noise contribution to the mixer NF becomes a major concern. A noise-cancelling technique developed for broadband LNA design can be applied to the transconductance stage of the Gilbert-cell mixer as well BRUCCOLERI; KLUMPERINK; NAUTA (2004). This technique is appealing because no inductors are required, while a sub 3 dB NF is achievable. The circuit is, therefore, very compact and there is also broadband input matching.

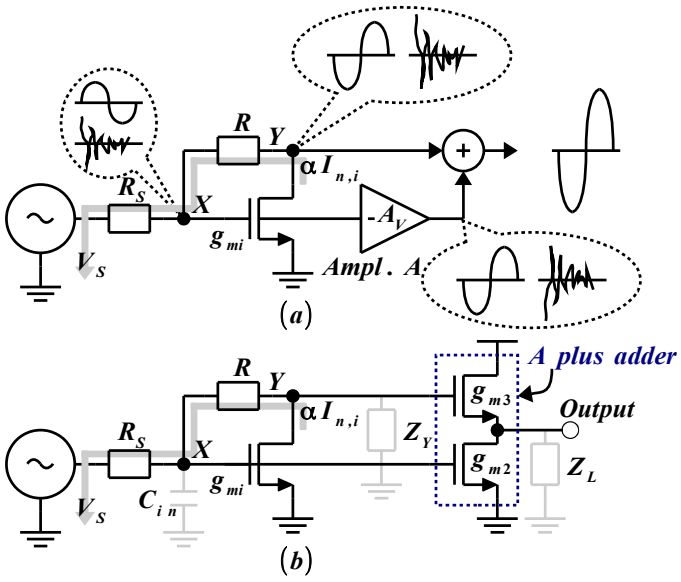


Figure 3.8: a) Wide-band LNA exploiting noise cancelling. b) Elementary implementation of amplifier A plus adder (biasing not shown). From BRUCCOLERI; KLUMPERINK; NAUTA (2004)

The technique is explained by analyzing the signal and the noise voltages at the input node X and output node Y, both with respect to ground, Fig. 3.8a. Depending on the relation between $Z_{IN} = 1/g_{mi}$ and R_S, a noise current flows out the matching MOSFET through R and R_S. This current causes two instantaneous noise voltages at nodes X and Y, which have equal sign. On the other hand, the signal voltages at nodes X and Y have opposite sign, because the gain of the matching MOSFET is negative. This *difference in sign*

for noise and signal makes it possible to *cancel the noise* of the matching device, while simultaneously *adding the signal* contributions constructively. This is done by creating a new output, where the voltage at node Y is added to a scaled negative replica of the voltage at node X. Figure 3.8b shows an elementary implementation of the noise-canceling LNA in Fig. 3.8a. Amplifier A and the adder are replaced with the common-source stage M_2–M_3, rendering an output voltage equal to the voltage at node X times the gain $A_v = g_{m2}/g_{m3}$. Transistor M_3 also acts as a source follower, copying the voltage at node Y to the output. The superposition principle renders the final addition of voltages with an overall gain $A_{VF} = 1 - g_{mi}R_S - g_{m2}/g_{m3}$. The noise cancellation condition is achieved by

$$\frac{g_{m2}}{g_{m3}} = 1 + \frac{R}{R_S} \tag{3.28}$$

In HO; SAAVEDRA (2010) the noise-cancelling technique was applied to the transconductance stage of the Gilbert-cell mixer. Fig. 3.9 shows the topology. It is comprised of three building blocks: noise-cancelling transconductors, a current-bleeding circuit, and switching pairs.

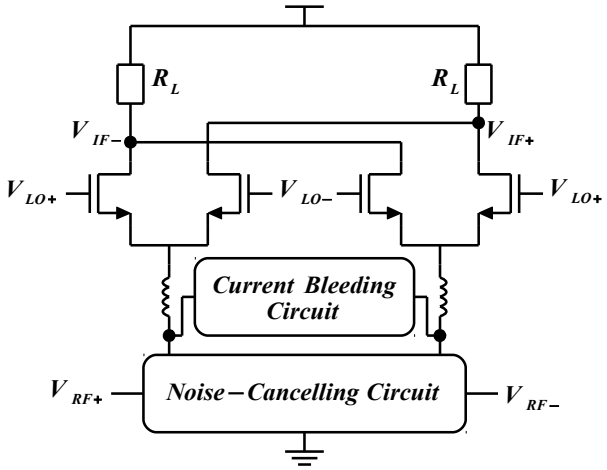


Figure 3.9: Block diagram of the proposed low-noise mixer from HO; SAAVEDRA (2010)

3.3.4 IM_2 suppression due to Switching Pairs

Direct conversion and low-intermediate-frequency (IF) receivers can suffer from second-order intermodulation (IM_2), the first of dc offset and flicker noise whereas the second of sensitivity impairment due to IM_2 products. Usually, the downconverter mixer determines the achievable second-order input intercept point (IIP_2) of the receiver.

Several mechanisms are at the origin of second-order intermodulation distortion in CMOS downconversion mixers MANSTRETTA; BRANDOLINI; SVELTO (2003): self-mixing, transconductor nonlinearity, switching pairs non- linearity, and mismatch in load resistors shown in Fig. 3.10. Most of these mechanisms can be made negligible by adopting ad hoc circuit and layout solutions.

The ultimate limit to the downconverter mixer IIP_2 is due to nonlinearity and mismatches in the switching stage. A dramatic drop is detected at radio- frequency. The main cause is the parasitic capacitance (C_{par}) loading the common source of the switching pair, and this detrimental effect will now be intuitively explained MANSTRETTA; BRANDOLINI; SVELTO (2003).

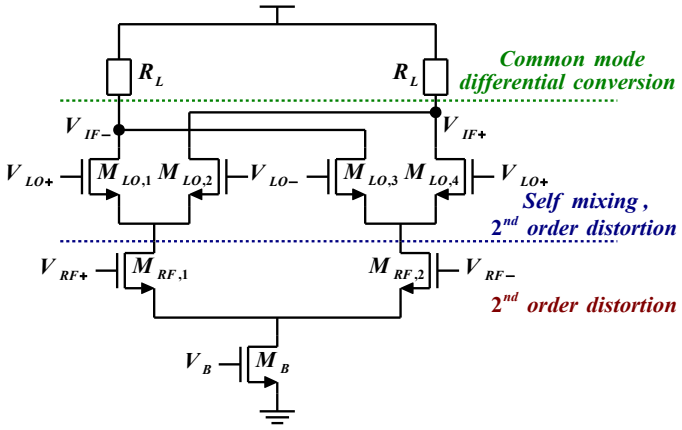


Figure 3.10: Gilbert-cell mixer: mechanisms of second-order intermodulation distortion

Due to the switching action, the offset voltage of the switching pair charges and discharges the parasitic capacitance C_{par} every LO period. This action makes the voltage at the common source of the switching pair present odd harmonics of the local oscillator and generates an interfering signal that modulates the non-linear transconductance stage. Correspondingly, second-order intermodulation sidebands around the LO odd harmonics in the source voltage spectrum arise. A current flowing in the capacitor C_{par} is finally down-converted as second-order inter-modulation product at mixer output, by device commutation.

Switching pair IIP_2 values increase rapidly with the biasing current. However, increasing the biasing current also raises both thermal and flicker noise contributions.

An IIP_2 improvement can be achieve by filtering out the fundamental LO frequency, together with side-bands, with a significant improvement in the expected IIP2 performance BRANDOLINI et al. (2006). An inductor L_{SW} is chosen to resonate out the parasitic capacitor C_{par} at the local oscillator frequency. The IM_2 current to be down-converted is thus reduced by a factor Q. The LC filter also improves flicker noise performance, because inductor L_{SW} cancels out the parasitic capacitor C_{par}, responsible for flicker noise transfer to downconversion mixer output DARABI; ABIDI (2000). It is worth to notice that for the same noise, the switching pair can then be biased at a higher current, leading to an even larger IIP_2 improvement.

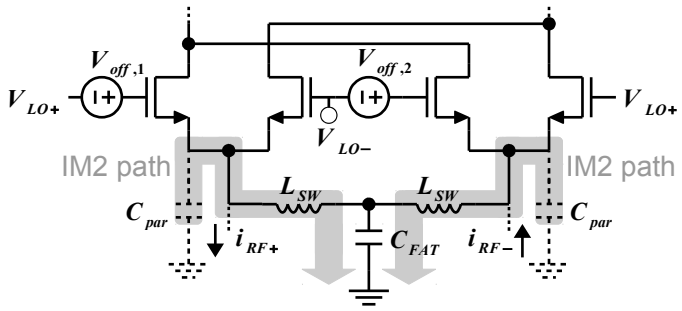


Figure 3.11: Enhancement for high IIP2 switching pair

Fig. 3.11 shows the implementation of the IIP_2 enhancement. Capacitor C_{FAT} provides an AC ground to the intermodulation currents. Finally, inductor L_{SW} suppresses any differential low-frequency IM_2 component coming from the transconductor.

3.4 Gilbert-Cell Mixer: Nonlinear Volterra Series Analysis

3.4.1 Volterra Series

The distortion behaviour of a Gilbert-cell mixer (subsection 3.2.3 and appendix A) was made assuming:

- V_{LO} is no switching and the mixer is a nonlinear time invariant (NLTI) system.
- No memory effects due to reactive components (capacitors and inductors).

This assumptions are only valid for low frequency. At high frequency, Eq. 3.22 is no longer valid. A method to calculate high-frequency distortion for a NLTI system, including memory effect, is through Volterra series. When applied to circuits it shows that the high frequency effect can degrade the distortion performance easily by close to 100% more than predicted using low frequency analysis. Also when applied to fully differential (balanced) circuits with no mismatch, it reveals the surprising result that there can be second harmonic distortion (HD_2) as high as –32 dB, when the low frequency analysis predicts the HD_2 should be zero. This HD_2 would have come from a circuit with an equivalent mismatch as high as 2.5 % and can be a major concern because it means RF feedthrough will still be present in a balanced mixer with zero mismatch. The use of Volterra series for high frequency distortion in mixers has been adopted in many popular simulators (e.g. SpectreRF).

We introduce the concept of Volterra series by going through systems of increasing complexity.

For a linear system without memory:

$$y(t) = h \cdot x(t) \tag{3.29}$$

where the output y only depends on input x at that instant only. h represents a linear gain.

For a linear, discrete and NLTI system with memory(described by summing all the effects of past inputs) :

$$y(n) = \sum_{i=0}^{n} h(\tau_i) \cdot x(n - \tau_i) \tag{3.30}$$

where n is the time index and $h(\tau)$ is the impulse response. In the continuous time domain (the convolution sum becomes a convolution integral)

$$y(t) = \int_0^t h(\tau)x(t-\tau)d\tau \tag{3.31}$$

Generalizing for a nth-order nonlinear system, first the memory-less system:

$$y(t) = h_1 \cdot x(t) + h_2 \cdot x^2(t) + \ldots + h_n \cdot x^n(t) \tag{3.32}$$

For a system with memory:

$$\begin{gathered} y(t) = \int_0^t h_1(\tau_1)x(t-\tau_1)d\tau_1 \\ + \int\int_0^t h_2(\tau_1,\tau_2)x(t-\tau_1)x(t-\tau_2)d\tau_1 d\tau_2 \\ + \int\int\int_0^t h_3(\tau_1,\tau_2,\tau_3)x(t-\tau_1)x(t-\tau_2)x(t-\tau_3)d\tau_1 d\tau_2 d\tau_3 \\ + \ldots + \int\ldots\int_0^t h_n(\tau_1,\tau_2\ldots\tau_n)x(t-\tau_1)x(t-\tau_2)\ldots x(t-\tau_n)d\tau_1 d\tau_2\ldots d\tau_n \end{gathered} \tag{3.33}$$

where $h_n(\tau_1,\ldots,\tau_n)$ are the nth-order Volterra Kernels (nth-order impulse response of the system).

Eq. 3.33 is the Volterra series expansion of an nth-order order nonlinear system, that can be understood as an infinite sum of multidimensional convolution integrals.

Frequency domain Volterra kernels are needed to calculate distortion, eg. HD_2, HD_3, IMD_3, ... Applying the Fourier transform to the nth-order Volterra kernel $h_n(\tau_1,\ldots,\tau_n)$

$$\begin{aligned} H_n(\omega_1,\ldots\omega_n) &= F\{h_n(\tau_1,\ldots,\tau_n)\} \\ &= \int\ldots\int h_n(\tau_1,\ldots,\tau_n)e^{-j\omega_1\tau_1}\ldots e^{-j\omega_n\tau_n}d\tau_1\ldots d\tau_n \end{aligned} \tag{3.34}$$

where H_n is the nth-order frequency domain Volterra kernel.

Using an input with m frequency components:

$$X = A(cos\omega_1 t + cos\omega_2 t + \ldots + cos\omega_m t) \tag{3.35}$$

the output of the nth order nonlinear system can be denoted as:

$$Y = H_1(j\omega_{p1})\circ X + H_2(j\omega_{p1}, j\omega_{p2})\circ X^2 + \ldots + H_n(j\omega_{p1}, j\omega_{p2},\ldots j\omega_{pm})\circ X^n \tag{3.36}$$

where $\omega_{p1}, \omega_{p2}, \ldots \omega_{pm}$ can be chosen from $\pm\omega_1, \pm\omega_2, \ldots \pm\omega_m$. They can be equal or different, and have both the + and – combination, for each term, the frequency components in H_n are the same as in X_n. The operator $\circ$ means:

- Multiply each frequency component in X_n by $\left|H_n(j\omega_{p1}, j\omega_{p2},\ldots j\omega_{pm})\right|$
- Shift phase by $\angle H_n(j\omega_{p1}, j\omega_{p2},\ldots j\omega_{pm})$

which can be understood as a filtering operation. For example, an input with two frequency components:

$$X = A(cos\omega_1 t + cos\omega_2 t) \tag{3.37}$$

ω_{p1}, ω_{p2} can be chosen from $\pm\omega_1, \pm\omega_2$. The term $H_2(j\omega_{p1}, j\omega_{p2})\circ X^2$ represents the following terms:

$$\begin{aligned} |H_2(j\omega_1, j\omega_1)|X^2\angle H_2(j\omega_1, j\omega_1) &= \frac{1}{2}|H_2(j\omega_1, j\omega_1)|A^2 cos(2\omega_1 t + \angle H_2(j2\omega_1)) \\ |H_2(j\omega_1, -j\omega_1)|X^2\angle H_2(j\omega_1, -j\omega_1) &= \frac{1}{2}|H_2(j\omega_1, -j\omega_1)|A^2 \\ |H_2(j\omega_1, j\omega_2)|X^2\angle H_2(j\omega_1, j\omega_2) &= |H_2(j\omega_1, j\omega_2)|A^2 cos(\omega_1 t + \omega_2 t + \angle H_2(j(\omega_1+\omega_2))) \\ |H_2(j\omega_1, -j\omega_2)|X^2\angle H_2(j\omega_1, -j\omega_2) &= |H_2(j\omega_1, -j\omega_2)|A^2 cos(\omega_1 t - \omega_2 t + \angle H_2(j(\omega_1-\omega_2))) \\ |H_2(j\omega_2, j\omega_2)|X^2\angle H_2(j\omega_2, j\omega_2) &= \frac{1}{2}|H_2(j\omega_2, j\omega_2)|A^2 cos(2\omega_2 t + \angle H_2(j2\omega_2)) \end{aligned} \tag{3.38}$$

We can definde HD_2, HD_3 and IM_3, using the Volterra Kernel. Table 3.2 shows a comparison between the Volterra and Taylor series representation of harmonic and intermodulation distortion. Taylor series or Power series representation is treated extensively in appendix A.

Volterra series incorporates the frequency dependent effect. The following relation:

$$H_3(j\omega_1, j\omega_1, j\omega_1) \neq H_3(j\omega_1, j\omega_1, -j\omega_2) \tag{3.39}$$

because the Volterra kernel are frequency dependent, Eq. 2.22 is no longer valid

$$IM_3 \neq 3HD_3 \tag{3.40}$$

Table 3.2: Harmonic and Intermodulation Distortion representation using Volterra and Taylor Series

	Volterra Series	Taylor Series
HD_2	$\frac{1}{2}\frac{\lvert H_2(j\omega_1, j\omega_1)\rvert}{H_1(j\omega_1)}A$	$\frac{1}{2}\frac{\alpha_2}{\alpha_1}A$
HD_3	$\frac{1}{4}\frac{\lvert H_3(j\omega_1, j\omega_1, j\omega_1)\rvert}{H_1(j\omega_1)}A^2$	$\frac{1}{4}\frac{\alpha_3}{\alpha_1}A^2$
IM_3	$\frac{3}{4}\frac{\lvert H_3(j\omega_1, j\omega_1, -j\omega_2)\rvert}{H_1(j\omega_1)}A^2$	$\frac{3}{4}\frac{\alpha_3}{\alpha_1}A^2$

3.4.2 Gilbert-Cell Mixer Distortion: High-Frequency Case

The previous introduction to Volterra series was made with the intent to obtain the IIP_3 expression of the Gilbert-cell mixer at high frequency. Again we assume that at high frequency the distortion is still dominated by the input transconductance stage, the source coupled pair. Hence let us redraw source coupled pair, this time including parasitic capacitance, Fig. 3.12.

In order to simplify the analysis, we consider the parasitic capacitance C_s is linear, though in real life C_s is nonlinear. Hence the only non-linearities comes from the I-V characteristics of the device.

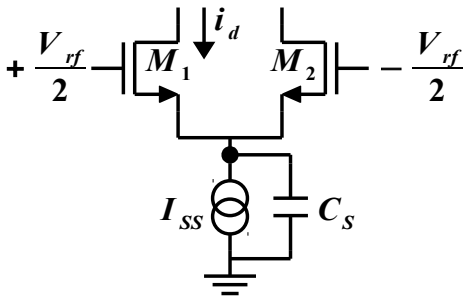


Figure 3.12: Source coupled pair as transconductance stage with parasitic capacitance

3.4.2.1 Summary of steps

First we present a summary of the steps. All small-signals terms are in lowercase. We assume that a small-signal differential input voltage v_{rf} is applied and a small signal output current id is developed. In order to determine distortion in i_d with respect to v_{rf} we do the following:

- Step 1: Write KCL at the tail node (source node) with node voltage v_s and determine the Volterra series expansion of the intermediate variable v_s in terms of input v_{rf}, using the short-hand notation.

$$\begin{aligned} v_s &= H_1 \circ v_{rf} + H_2 \circ v_{rf}^2 + H_3 \circ v_{rf}^3 + \dots \\ &= v_{s1} + v_{s2} + v_{s3} + \dots \end{aligned} \tag{3.41}$$

- Step 2: Use MOS device equation in the small signal form:

$$i_d = \frac{k}{2}\left(v_{rf} - v_s\right)^2 \tag{3.42}$$

to express output current id in terms of input voltage v_{rf} and the intermediate variable v_s.

- Step 3: Substitute v_s, determined by Eq. 3.41 (from step 1), in Eq. 3.42 and derive:

$$i_d = G_1 \circ v_{rf} + G_2 \circ v_{rf}^2 + G_3 \circ v_{rf}^3 + \ldots \tag{3.43}$$

G_n now becomes a function of H_n. Since H_n has been determined in step 1, G_n can now be solved. This calculation will be carried out on each G_n sequentially.

- Step 4: Derive IM_3, HD_3 in terms of G_n. Since G_n has been determined in step 3, IM_3, HD_3 can now be calculated.

3.4.2.2 Determine Volterra Kernel H_n

We begin step 1 by applying KCL at the tail node:

$$C_s\frac{dV_s}{dt} + I_{SS} = \frac{k}{2}\left[\left(V_{gs1} - V_T\right)^2 + \left(V_{gs2} - V_T\right)^2\right] \tag{3.44}$$

I_{SS} is the DC bias current, $I_{SS} = k(V_{GS} - V_T)^2$. V_s, V_{gs1} and V_{gs2} can be written into DC and small signal terms:

$$V_s = V_S + v_s$$

$$V_{gs1} = V_{GS} + v_{gs1} \qquad V_{gs2} = V_{GS} + v_{gs2}$$

$$v_{gs1} = \frac{v_{rf}}{2} - v_s \qquad v_{gs2} = -\frac{v_{rf}}{2} - v_s \tag{3.45}$$

combining Eqs. 3.44 and 3.45 yields:

$$C_s\frac{dv_s}{dt} + 2k(V_{GS} - V_T)v_s - kv_s^2 = \frac{k}{4}v_{rf}^2 \tag{3.46}$$

substituting Eq. 3.41 into 3.46 and taking phasor form of $\dfrac{dv_s}{dt}$

$$\left(j\omega C_s + 2k(V_{GS} - V_T)\right)\left(v_{s1} + v_{s2} + v_{s3} + \ldots\right) - k\left(v_{s1} + v_{s2} + v_{s3} + \ldots\right)^2 = \frac{k}{4}v_{rf}^2 \tag{3.47}$$

keeping only the 1^{st} order terms of equation :

$$\left(j\omega C_s + 2k(V_{GS} - V_T)\right)H_1(\omega) \circ v_{rf} = 0$$

$$H_1(\omega) = 0 \tag{3.48}$$

$$v_{s1} = 0 \tag{3.49}$$

substituing Eq. 3.49 into 3.47, and keeping only the 2^{nd} order terms:

$$\left[j\left(\omega_1 + \omega_2\right)C_s + 2k(V_{GS} - V_T)\right]H_2\left(\omega_1, \omega_2\right) \circ v_{rf}^2 = \frac{k}{4}v_{rf}^2 \tag{3.50}$$

$$H_2(\omega_1, \omega_2) = \frac{\frac{k}{4}}{j(\omega_1+\omega_2)C_s + 2k(V_{GS}-V_T)} \approx \frac{1}{8(V_{GS}-V_T)}\left(1 - \frac{j(\omega_1+\omega_2)C_s}{2k(V_{GS}-V_T)}\right) \tag{3.51}$$

Notice that ω becomes $\omega_1+\omega_2$ because we are interested in the 2^{nd} orders terms. Because of the operator $\circ$, Eq. 3.51 consists of four equations for four diferent cases:

$$\omega_1, \omega_2 = \pm\omega_a, \pm\omega_b$$

where ω_1 and ω_2 are symbols and ω_a, ω_b are the frequency components of input. For the 3^{rd} order term:

$$[j(\omega_1+\omega_2+\omega_3)C_s + 2g_m]H_3(\omega_1, \omega_2, \omega_3) \circ v_{rf}^3 = 0$$

$$H_3(\omega_1, \omega_2, \omega_3) = 0 \tag{3.52}$$

Notice that H_1 always consists of one frequency component (ω_1): H_2 always consists of two (ω_1, ω_2), and H_3 consists of three (ω_1, ω_2, ω_3).

3.4.2.3 Relating Volterra Kernel G_n to H_n

To reiterate, our final goal is to write i_d in the following form:

$$i_d = G_1 \circ v_{rf} + G_2 \circ v_{rf}^2 + G_3 \circ v_{rf}^3 + \ldots \tag{3.53}$$

or, alternately as

$$i_d = i_{d1} + i_{d2} + i_{d3} + \ldots \tag{3.54}$$

Using the MOS device equation containing DC and time varying components:

$$I_d + i_d = \frac{k}{2}\left(V_{GS} + \frac{v_{rf}}{2} - v_s - V_T\right)^2 =$$
$$k(V_{GS}-V_T)\cdot\left(\frac{v_{rf}}{2} - v_s\right) + \frac{k}{2}\left(\frac{v_{rf}}{2} - v_s\right)^2 + \frac{k}{2}(V_{GS}-V_T)^2$$

$$i_d = k(V_{GS}-V_T)\left(\frac{v_{rf}}{2} - v_s\right) + \frac{k}{2}\left(\frac{v_{rf}}{2} - v_s\right)^2 \tag{3.55}$$

Volterra series expansion of i_d becomes:

$$i_{d1} + i_{d2} + i_{d3} = \left[\frac{k(V_{GS}-V_T)}{2} - \frac{k}{2}(v_{s1}+v_{s2}+v_{s3})\right]v_{rf}$$

$$+\frac{k}{8}v_{rf}^2 - k(V_{GS}-V_T)(v_{s1}+v_{s2}+v_{s3}) + \frac{k}{2}(v_{s1}+v_{s2}+v_{s3})^2 \tag{3.56}$$

keeping the 1^{st} order term of v_{rf} coefficients in equation 3.56

$$i_{d1} = \frac{k(V_{GS}-V_T)}{2}v_{rf} = G_1 \circ v_{rf}$$

$$G_1(\omega) = \frac{k(V_{GS} - V_T)}{2} \tag{3.57}$$

isolating the 2^{nd} order terms of v_{rf} coefficients in equation 3.56

$$i_{d2}(\omega_1, \omega_2) = \frac{k}{8} v_{rf}^2 - k(V_{GS} - V_T) H_2(\omega_1, \omega_2) \circ v_{rf}^2 = G_2 \circ v_{rf}^2$$

$$G_2(\omega_1, \omega_2) = \frac{k}{8} \left[1 - \frac{1}{\left[1 + \frac{j(\omega_1 + \omega_2) C_s}{2k(V_{GS} - V_T)} \right]} \right]$$

$$G_2(\omega_1, \omega_2) \approx \frac{1}{16} \frac{j(\omega_1 + \omega_2) C_s}{(V_{GS} - V_T)} \qquad Intermediate\ frequency\ approximation \tag{3.58}$$

Separating the 3^{rd} order temrs of v_{rf} coefficients from Eq. 3.56

$$i_{d3}(\omega_1, \omega_2, \omega_3) = -\frac{k}{2} v_{rf} v_{s2} = -\frac{k}{2} \overline{H_2(\omega_1, \omega_2)} \circ v_{rf}^3 = G_3 \circ v_{rf}^3$$

$$G_3(\omega_1, \omega_2, \omega_3) \equiv -\frac{k}{2} \overline{H_2(\omega_1, \omega_2)} \tag{3.59}$$

$$G_3(\omega_1, \omega_2, \omega_3) \approx -\frac{k}{16(V_{GS} - V_T)} \left[1 - j(\omega_1 + \omega_2 + \omega_3) \frac{C_s}{3k(V_{GS} - V_T)} \right] \tag{3.60}$$

3.4.2.4 Find IM_3, HD_3

The expression of HD_3 valid for cases with/without memory effect:

$$HD_3 = \frac{i_{d3}}{i_{d1}} = \frac{G_3 \circ v_{rf}^3}{G_1 \circ v_{rf}} = \frac{\left| G_3 \circ \left(A_{rf} cos\omega_1 t \right)^3 \right|}{\left| G_1 \circ A_{rf} cos\omega_1 t \right|} = \frac{G_3(\omega_1, \omega_1, \omega_1)}{G_1} \frac{A_{rf}^2}{4} \tag{3.61}$$

next let us generalize the definition of IM_3 valid for cases with/without memory effect;

$$IM_3 = \frac{\left| G_3(\omega_1, \omega_1, \omega_2) \circ A_{rf}^3 (cos\omega_1 t + cos\omega_2 t)^3 \right|}{\left| G_1 \circ A_{rf} cos\omega_1 t \right|} = \frac{3}{4} \frac{|G_3(\omega_1, \omega_1, \omega_2)|}{|G_1|} A_{rf}^2 \tag{3.62}$$

we know that G_3 is expressed in terms of H_2, so Eq. 3.61 yields:

$$HD_3 = \frac{A_{rf}^2}{32(V_{GS} - V_T)^2} \left| 1 - \frac{j(2\omega_1) C_s}{k(V_{GS} - V_T)} \right| \tag{3.63}$$

It should be noted that for IM_3 we have three frequencies (ω_1, ω_1, $\omega_2 = -\omega_1 - \Delta\omega$). For IM_3 caused by adjancent channel interference, ω_2 is so defined (to be at $-\omega_1 - \Delta\omega$) such that $2\omega_1 + \omega_2$ lies on the same frequency as $\omega_1 - \Delta\omega$.

Now we are interested in $G_3(\omega_1, \omega_1, \omega_2)$:

$$G_3(\omega_1,\omega_1,\omega_2) \equiv -\frac{k}{2}\left[\frac{H_2(\omega_1,\omega_1)+H_2(\omega_1,\omega_2)+H_2(\omega_2,\omega_1)}{3}\right]$$

$$\equiv -\frac{k}{16(V_{GS}-V_T)}\left[1-\left(\frac{jC_s}{2k(V_{GS}-V_T)}\times\frac{(\omega_1+\omega_1)+(\omega_1+\omega_2)+(\omega_2+\omega_1)}{3}\right)\right]$$

$$-\frac{k}{16(V_{GS}-V_T)}\left[1-\left(\frac{jC_s}{2k(V_{GS}-V_T)}\times\frac{(\omega_1\overset{\equiv}{+}\omega_1)+(\omega_1-\omega_1-\Delta\omega)+(-\omega_1-\Delta\omega+\omega_1)}{3}\right)\right]$$

$$\equiv -\frac{k}{16(V_{GS}-V_T)}\left[1-\left(\frac{jC_s}{2g_m}\times\frac{2(\omega_1-\Delta\omega)}{3}\right)\right]$$

$$\cong -\frac{k}{16(V_{GS}-V_T)}\left[1-\left(\frac{jC_s}{2k(V_{GS}-V_T)}\times\frac{2\omega_1}{3}\right)\right] \tag{3.64}$$

Substituing G_1 and G_3 into Eq. 3.62, we get

$$IM_3 \equiv \frac{3A^2_{interference}}{32(V_{GS}-V_T)^2}\left[\left|1-\frac{2}{3}\frac{j(\omega_1)C_s}{2k(V_{GS}-V_T)}\right|\right] \tag{3.65}$$

It is instructive to compare Eqs. 3.63 to 3.65 and note that even when we set $A_{rf} = A_{interference}$, $IM_3 \neq 3HD_3$.

3.5 Previous Works on Active Mixers for Multi-Band

In the literature several works have been published on active mixers for multi-band. One major issue for these mixers is linearity. The IMD_3 is the most dominant nonlinearity component. The perfomance measure for this nonlinearity is usually expressed by the third-order input intercept point (IIP_3) per DC power consumption (IIP_3/DC), since the third-order intercept point (IP_3) is usually proportional to DC power consumption. Therefore, it is a great challenge to increase IP_3/DC for extremely low-power systemts such as ZigBee CHOI et al. (2003). The IIP_3 is ultimately limited by the MOSFET transconductance nonlinearity itself.

In KIM; KIM; LEE (2004), MOSFET transconductance linearization by (multiple gated transistor, of MGTR) is use to improve linearity. The transconductance linearization is achieved by canceling the negative peak value of the $g_m^{''}$ of the main transistor with the positive one in the auxiliary transistor. This technique is limited by distortion originated from the combined influence of $g_m^{'}$ and harmonic feedback. MGTR is an effective way to linearize the common-source (CS) MOSFET without increasing DC power consumption KIM; KO; LEE (2000). However, it was also shown that the obtained IIP_3/DC improvement in transconductance, which was shown to be due to various other harmonic mixing KIM; KO; LEE (2001).

BRANDOLINI et al. (2006) presents the design of a 0.18μm active downconversion mixer, tailored to UMTS applications. The input transconductor is RC degenerated to provide both high IIP_2 and IIP_3. The parasitic capacitance at switching pair common source is tuned out by means of an integrated inductor, while loads are accurately matched to make common-mode-to-differential conversion negligible.

In LIANG et al. (2008), a new third-order transconductance $g_m^{''}$ cancellation technique is proposed and applied to a conventional RF mixer for improving linearity. A bulk-to-source voltage is applied to adjust the peak value position of $g_m^{''}$. The cancellation of $g_m^{''}$

is achieved by a negative peak $g_m^{''}$ transistor combined in parallel with a positive peak $g_m^{''}$ transistor. A Gilbert-cell mixer in commercial 0.18um CMOS process was designed using the proposed method to further evaluate the linearity. The compensated $g_m^{''}$ device is placed in the input RF gm-stage and then reducing the principle nonlinearity source of the mixer ELLIS (1998)KWON; LEE (2005).

For direct conversion receivers, the second-order intermodulation (IM_2) from the down-conversion mixer is a challenging issue. Therefore, to meet the required second-order input intercept point (IIP_2) performance, some on-chip calibration or analog techniques is necessary.

VAHIDFAR; SHOAEI (2008) presents a new technique based on calibrating mixer by injecting a programmable nonlinear current into the mixer output. The proposed calibration technique can be used in multistandard mixers. The calibration circuit is low noise in order to not affect the mixer noise figure.

In MOLLAALIPOUR; NAIMI (2012), a new highly linear CMOS mixer is proposed that utilizes second- and third-order distortion cancellation mechanisms using second harmonic (IM_2) injection technique. The proposed circuit can work for wide channel bandwidth applications. The cancellation mechanism is performed in the transconductor stage of the mixer. In order to cancel the second-order intermodulation component, a signal with the same IM_2 amplitude and opposite phase is generated in an auxiliary path and fed to the output of the main path in transconductance stage, and to suppress the third-order intermodulation IM_3, low-frequency second-order intermodulation IM_2 is generated and injected to circuit to generate the IM_3 component with the same amplitude an opposite phase.

Table 3.3 summarizes the above works on active mixer for multi-band.

Table 3.3: Comparison table of prior published works on active mixers for multi-band

Reference	[1]	[2]	[3]	[4]	[5]
Process	0.18 μm	0.18 μm	0.18 μm	65 nm	0.18 μm
Linearization Technique	MGTR (DS)	RC Degeneration	Derivative Superposition (DS)	Calibration of IM_2	IM_2 Injection
Frequency (GHz)	2.4	2.1	2.4	2.1	2.1
IIP_2 (dBm)	N/A	82	N/A	90	93
IIP_3 (dBm)	9	10	15	6	15
Power (mW)	5.4	7.2	14.8	6	8
Gain (dB)	16.5	16	11	12	15
NF (dB)	14.2	18.5	13.8	17.5	14
Area mm^2	0.96	1.2	0.052	-	-

[1]: KIM; KIM; LEE (2004)
[2]: BRANDOLINI et al. (2006)
[3]: LIANG et al. (2008)
[4]: VAHIDFAR; SHOAEI (2008)
[5]: MOLLAALIPOUR; NAIMI (2012)

3.6 Downconversion Mixer for Multi-Band and Multiple Standard Receivers

In order to comply with multi-band and multiple standard operation, two downconversion mixers are proposed. The frequency range of operation for the proposed mixers will constrain key specifications such as: power, gain, noise, distortion among others. For that reason a frequency range of operation between 1 to 6 GHz is chosen to evaluate our proposed topologies. The frequency operation of the first topology is chosen to be 2 GHz, using as reference the previous works on mixers reviewed in section 3.5. And for the second topology the frequency range of 1 to 6 GHz is selected to evaluate it.

3.6.1 First Topology: Circuit Description

For the first topology we focus on the improvement of linearity. For linearization the PDHC technique will be employed KIM; KIM (2008).

Fig. 3.13 presents the schematic diagram of the first topology. The characteristics of this mixer are:

- The transconductance stage : Formed by the pseudo-differential pair (M_1, M_2) and the cross-coupled pair (M_{1a}, M_{2a}), which implements the PDHC, KIM; KIM (2008).
- Switching stage : Formed by four current commutating switches in double balanced configuration (M_{LO}). A dynamic current bleeding (M_{B1}, M_{B2}, M_{BL}) is added for noise reduction, DARABI; CHIU (2005). And the L-C filter, L_{SW} resonates the parasitic capacitance C_{PAR} of the switching pair at the LO frequency to improve the IIP_2 performance, BRANDOLINI et al. (2006).
- Load stage : Formed of the load stage transistors (M_{IF}) and resistors (R_L) with common mode feedback loop (CMFB) for low-voltage operation. The amplifier A_{CM} in the CMFB loop is the same used in the Gilbert-cell mixer characterization.

3.6.2 Second Topology: Circuit Description

For the second topology we combine both noise reduction and linearity improvement: these techniques were reviewed in the previous chapter. For linearization the PDHC technique employed in the first topology is also used for the second. And for noise reduction, the thermal noise cancellation implemented in wideband CMOS LNAs BRUCCOLERI; KLUMPERINK; NAUTA (2004) and CMOS Broadband Low-Noise Mixers HO; SAAVEDRA (2010).

Fig. 3.14 presents the schematic diagram of the second topology. The characteristics of this mixer are:

- The transconductance stage : Formed by the noise-canceling transconductors, M_{1a}, M_{1b}, M_2 and M_3.
- The linearization of the input transconductance stage implements the PDHC through transistors : M_{aux} and $M_{ibuffer}$. M_{aux} cancels the third-order harmonic components, KIM; KIM (2008). $M_{ibuffer}$ acts as a linear current buffer. Additionally, an inductor L_{peak} improves the noise and linearity performance, HO; SAAVEDRA (2010).
- Switching stage : Formed by four current commutating switches in double balanced configuration, (M_{LO}).

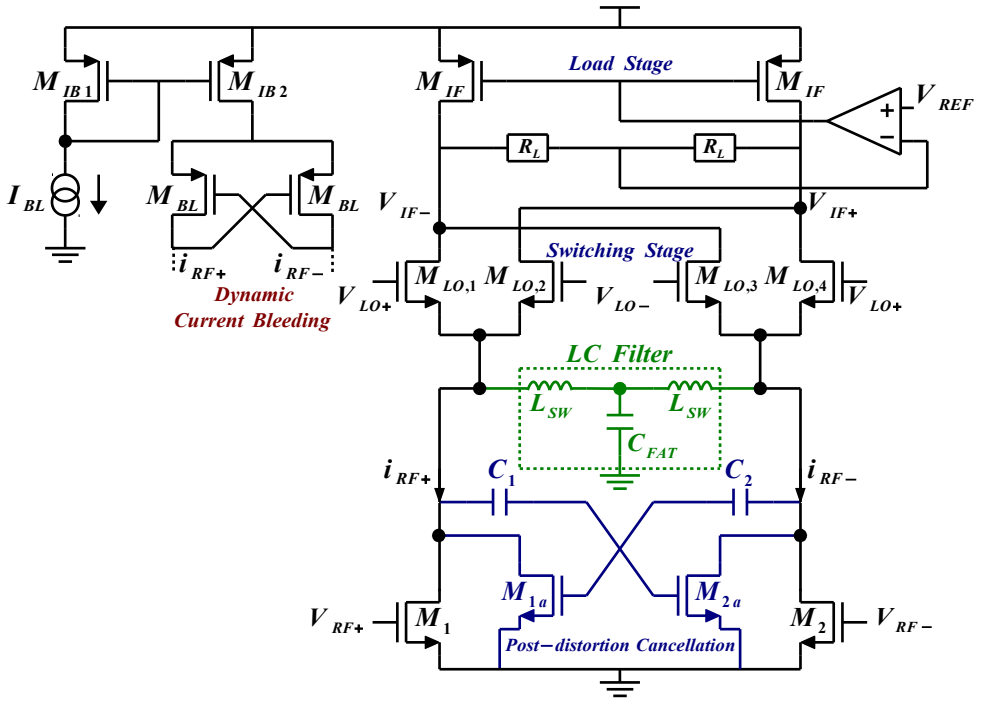


Figure 3.13: First proposed topology for the downconversion mixer

- Load stage : Formed of the load stage transistors (M_{IF}) and resistors (R_L) with common mode feedback loop (CMFB) for low-voltage operation. The amplifier A_{CM} in the CMFB loop is the same used in the first topology.

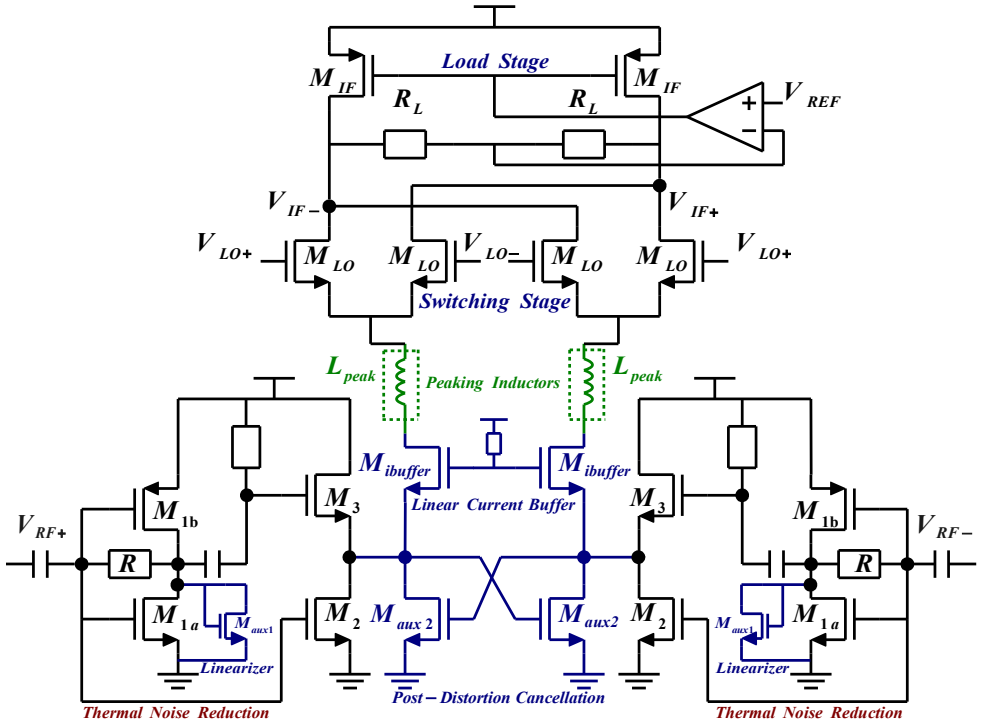


Figure 3.14: Second proposed topology for the downconversion mixer

3.6.3 First Topology: Distortion and Noise Analysis

3.6.3.1 IIP_3 Derivation

A time-varying Volterra series can be used at high frequencies to analyze the high-frequency inter-modulation performance of the proposed mixer. The mixer's distortion is induced by the switching and transconductance stages. TERROVITIS; MEYER (2000) provides a detailed analysis of the intermodulation distortion of the switching pairs. The effectiveness of the applied linearization is determined mainly by the transconductance stage. For simplicity in this analysis of the mixer, distortion due to the switching pairs has been neglected. The parasitic capacitance and resistance of the two auxiliary transistors, except the gate-source capacitance, have also been ignored in the analysis. Fig. 3.15 shows a version of the mixer schematic diagram for use in high-frequency distortion analysis.

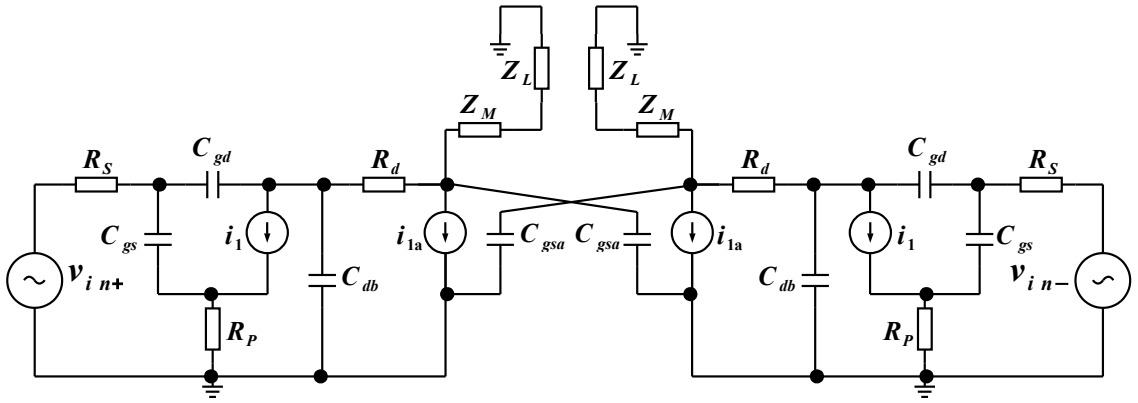


Figure 3.15: Small-signal equivalent circuit diagram of the proposed mixer

This is limited to a third-order analysis, assuming a weakly nonlinear circuit. Using the input harmonic method shown in MAAS (2003) and the Volterrra series analysis described in appendix B, the expression for IIP_3 is given as follows:

$$IIP_3 = \frac{1}{6R_s\,|H(s)|\,|A_1(s)|^3\,|\varepsilon(\Delta s, 2s)|}, \tag{3.66}$$

where

$$H(s) = \frac{1 + sC_{gs}[R_s + R_p] + sC_{gd}R_s}{g_1' - sC[1 + R_p(g_1' + sC_{gs})]} \tag{3.67}$$

$$A_1(s) = \frac{1}{g_1 + g(s)} \cdot \frac{1 + sC_{gd}Z_1(s)}{Z_2(s)} \tag{3.68}$$

$$\varepsilon(\Delta s, 2s) = g_3' - g_{OB} \tag{3.69}$$

$$g_1' = g_1 - ag_1 \tag{3.70}$$

$$g_3' = g_3 - cg_{a1} - 2abg_{a2} - a^3 g_{a3} \tag{3.71}$$

$$g_{OB} = \frac{2(g_2')^2}{3}\left[\frac{2}{g_1' + g(\Delta s)} + \frac{1}{g_1' + g(2s)}\right] \tag{3.72}$$

$$g_2' = g_2 + bg_{a1} + a^2 g_{a2} \tag{3.73}$$

$$g(s) = \frac{1 + sC_{gs}[R_s + Z_2(s)] + sC_{gd}[R_s + Z_1(s)]}{Z_2(s)} \tag{3.74}$$

$$Z_1(s) = \frac{1}{sC_{db}} // \{[(Z_M(s) + Z_L(s)) // \frac{1}{sC_{gsa}}] + R_d\} \tag{3.75}$$

where: Z_M = the equivalent impedance of the switching transistor and Z_L = the equivalent impedance of the load.

$$Z_2(\omega) = R_p + j\omega C_{gd}[R_s R_p + R_s Z_1(\omega) + R_p Z_1(\omega)] \tag{3.76}$$

Eqs. 3.69 to 3.76 imply that the mixer's linearity (IIP_3 or OIP_3) is determined by g_1', g_3', and g_{OB}. Parameter g_{OB} represents the combined effect of the second-order nonlinearity generating the second-order intermodulation product, which is then mixed with the fundamental tones, yielding the third-order products, KIM; KO; LEE (2001). This self-interaction is due to the multiple feedback in the circuit mainly by the gate-drain capacitance.

From Eqs. 3.72 to 3.75 it can be shown that the values of $|H(\omega)|$, $|A_1(\omega)|$, and $|\varepsilon(\Delta\omega, \omega 1 + \omega 2)|$ decrease when the cross-coupling post-distortion technique is implemented in the Gilbert-cell mixer. For this reason, the proposed mixer achieves higher linearity than a double-balanced mixer using a traditional current-bleeding technique.

3.6.3.2 Noise

Noise at the ouput of the mixer is caused mainly by the channel thermal noise and the flicker noise of the transconductance stage, and the thermal noise generated in the switching pair and the load, TERROVITIS; MEYER (1999).

Because the thermal current noise from a transistor is proportional to its transconductance, the noise contribution from the auxiliary transistor is very small and can be neglected in an analysis. The noise figure of the proposed downconversion mixer can be calculated by Eq. 3.77 :

$$NF = 10\log\left[\frac{\alpha}{c^2} + \frac{2(\gamma_1 + \gamma_{g1} g_{m1} + \frac{K}{\alpha f g_{m1}^2})\alpha g_{m1} + 4\gamma_{LO}\bar{G} + 4\gamma_{gLO}\bar{G^2} + \frac{1}{R_L}}{R_S c^2 (g_{m,LO})^2}\right] \tag{3.77}$$

where the quantities α, c, G, and G^2 are evaluated with the bias current of each switch pair and symbols γ_1 and γ_{LO} represent noise factor γ for transistors M_1 and M_{LO}, respectively. Parameter K is a coefficient used in the analysis.

3.7 Conclusions

From a concise review on the literature on Gilbert-cell mixers and their performance improvements such as gain, noise and linearity, two topologies for downconversion based

on Gilbert-cell type mixers exploiting the post-distortion harmonic cancellation are proposed. These topologies may be well suited for software-defined radios (SDRs), as well as multi-band multi-standard communications systems which require highly linear RF front-ends and noise performance.

4 DOWNCONVERSION MIXER FOR MULTI-BAND AND MULTIPLE STANDARDS

4.1 Introduction

In the previous chapter, two topologies of downconversion mixer suitable for multi-band receivers were proposed. In this chapter a design methodology for a Gilbert-cell based on the $\frac{g_m}{I_D}$ methodology for RF circuits will be used to design the proposed mixers. In section 4.2 a design procedure for a Gilbert-cell mixer is developed. Section 4.3 presents the design and simulation results of the proposed downconversion mixer suitable for multi-band receivers. Section 4.4 presents the layout of the designed downconversion mixer. Section 4.5 makes an assessment with respect to the state of the art. Finally, section 4.6 gives the summarizing remarks

4.2 Gilbert-cell Mixer Design Methodology

We employed the $\frac{g_m}{I_D}$ methodology, proposed by Jespers, for transistor sizing SILVEIRA; FLANDRE; JESPERS (1996) and FIORELLI et al. (2011), FIORELLI; SILVEIRA; PERALIAS (2014) $\frac{g_m}{I_D}$ methodology for RF circuits. The specifications of the Gilbert-cell mixer such as: gain conversion (CG), noise figure (NF), input third-order intercept point (IIP_3) and power were characterized as function of the device operation point ($\frac{g_m}{I_D}$, I_D) and circuit parameters (V_{DD}, R_L, P_{LO}) of the Gilbert-cell mixer. This characterization shows the dependency of those parameters in the specifications; the proposed design methodology is based on this dependency. An optimization of each one of the specifications or trade-off between them (power consumption and performance) can be achieved using this design methodology.

Fig. 4.1 shows the Gilbert-cell mixer schematic used to develop the design methodology. The circuit consists of three stages:

- Transconductance stage : Formed by a pseudo-differential pair (M_{RF})
- Switching stage : Formed by four current commutating switches in double balanced configuration, (M_{LO})
- Load stage : Formed of transistors (M_{IF}) and resistors (R_L). A common-mode feedback loop (CMFB) with relatively high gain over the IF signal bandwidth is employed at the mixer output, which regulates the DC output voltage level around V_{REF} and suppress the common-mode IM_2 components, BRANDOLINI; SOSIO; SVELTO (2007). The amplifier A_{CM} in this CMFB loop is displayed in Fig. 4.2. This amplifier is a simple differential pair with self-regulated active load.

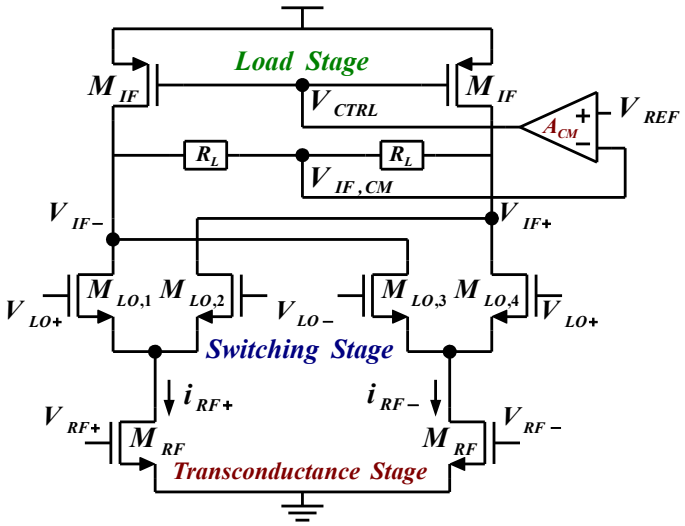


Figure 4.1: Gilbert-cell mixer schematic

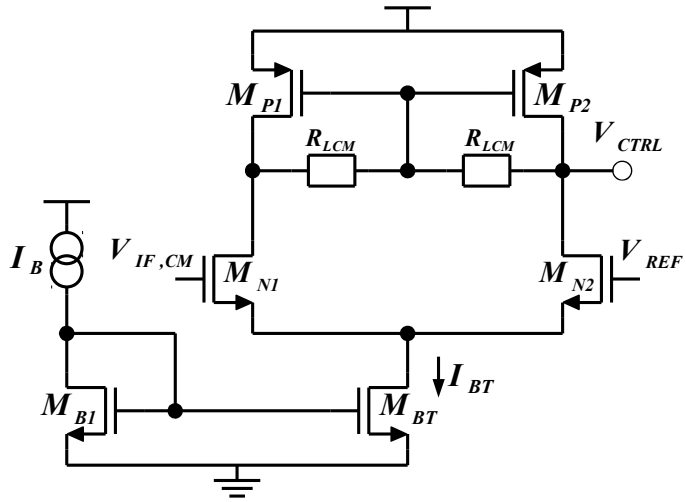


Figure 4.2: Common-mode feedback amplifier at the mixer output

In order to develop the design methodology for the Gilbert-cell mixer of Fig. 4.1, a series of steps were defined. These steps are:

- PDK characterization : A technology characterization for design is made. Data for the transit frequency (f_T) and current density (I_D/W) over a reasonable range of $\frac{gm}{I_D}$ and channel lengths is generated. These parameters are (to first order) independent of transistor width, which enables normalized design.
- Design Space for parameters : A design space for the transistor operation conditions and circuit parameters of the Gilbert-cell mixer is defined. Also, the dependency of those parameters in the specifications is indicated.
- Design Constraint: A design methodology based the dependency of the design space of the parameters is described. Also, a characterization of two specifications : NF and IIP_3 for a given circuit conditions of the Gilbert-cell mixer is made.

4.2.1 Technology Characterization of the PDK IBM 0.13 μm CMOS

A technology characterization of the PDK of IBM CMOS 0.13 μm process was implemented as the first step of the design methodology for the Gilbert-cell mixer.

We will use drain current efficiency ($\frac{g_m}{I_D}$) as the reference axis to compare other transistor parameters (V_{OV}, $\frac{g_m}{g_o}$, f_T and I_D/W). These plots tell us how much transconductance (g_m) we can get for a given current (I_D). In our design methodology we will use two parameters: the transit frequency (f_T) for transistor bandwidth definition and the current density (I_D/W) for transistor sizing. Since V_T depends on the channel length, these parameters were extracted for different channel lengths.

The transit frequency (f_T) is defined as the frequency when the transistor small-signal current gain goes to unity with the source and drain at AC ground.

$$f_T \cong \frac{g_m}{2\pi(C_{gs}+C_{gd}+C_{gb})} = \frac{g_m}{2\pi C_{gg}} \tag{4.1}$$

Overall, the ratio of g_m to C_{gg} comes up often in analog circuits, and is a good metric to compare the device frequency response (speed). Transistor f_T increases with overdrive voltage, if a higher bandwidth is needed, the device must operate at lower values of $\frac{g_m}{I_D}$. Fig. 4.3 shows the transit frequency vs ($\frac{g_m}{I_D}$).

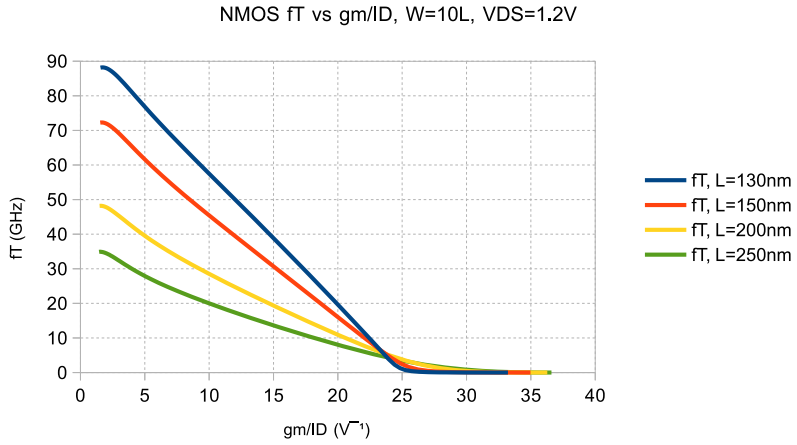


Figure 4.3: Transit frequency (f_T) vs Drain current efficiency ($\frac{g_m}{I_D}$) for different channel lengths

Ultimately, we need to know how to size our devices to get a certain current. The current density (I_D/W) of a transistor increases with increased V_{GS} or overdrive voltage (V_{OV}). High values of $\frac{g_m}{I_D}$ requires low current densities, which implies bigger devices for a given current. Fig. 4.4 shows the current density vs ($\frac{g_m}{I_D}$).

Additionally, plots such as : threshold variation, $\frac{g_m}{I_D}$ vs V_{OV}, $\frac{g_m}{g_o}$ vs V_{OV} and $\frac{g_m}{I_D}$, f_T vs V_{OV}, I_D/W vs V_{GS} were extracted and shown in Appendix D.1.

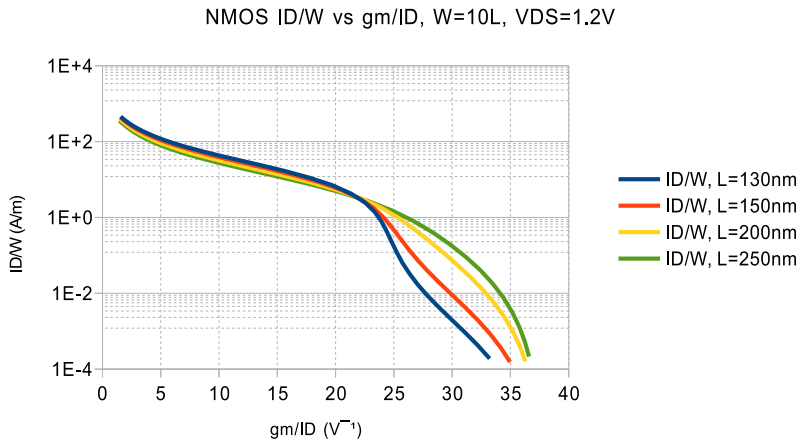


Figure 4.4: Current density (I_D/W) vs Drain current efficiency ($\frac{g_m}{I_D}$) for different channel lengths

4.2.2 Design Space for the Parameters

After the technology characterization is made, the design space of the parameters is defined based on the dependency among them. Parameters such: Channel Length (L) and drain current efficiency ($\frac{g_m}{I_D}$), LO power (P_{LO}) and output load (R_L) are part of the design space exploration in our method, and are taken as first choices for the subsequent design optimizations. The other parameters present a dependency at the device level (L, V_T, $\frac{g_m}{I_D}$, I_D) and circuit level (P_{LO}, power). Table 4.1 lists them.

Table 4.2 shows the inter-dependency between performance and design space parameters of the mixer. Was listed: power, conversion gain, noise figure and IIP_3. For example: the conversion gain (CG) depends on transconductance stage ($g_{m,RF}$), the switch gain (A_{SW}) and the output load (R_L). The IIP_3 and NF strongly depend on the $\frac{g_m}{I_D}$ of the transistors in the transconductance stage. This will be helpful, since we can have a starting point in our mixer design methodology.

4.2.3 Design Constraint

After characterizing the technology and finding the dependency between the specifications and design parameters of the Gilbert-cell mixer, the design procedure will be defined. This completes the last step of the design methodology.

A conceptual diagram of our mixer design methodology is shown in Fig. 4.5. The performance parameters (power, gain, IIP_3 and NF) of our mixer are design goals. Each perfomance evaluation method is represented in a box. We have an analytical model to calculate the parameters related to its dependency. For example a power constraint limits the maximum avalaible I_D for the transconductance stage; an IIP_3 constraint defines the $\frac{g_m}{I_D}$ of the transconductance stage, that can be used to estimate the NF as well.

In our Gilbert-cell mixer design methodology a constraint of power was defined, the other parameters were designed to obtain the best available performance (Highest gain and IIP_3 and the lowest NF). Additionally, two design parameters: transistor size and switch gain were defined. The first calculates the transistor size from (ID/W and I_D) Fig. 4.4, and the second estimates the switching gain (A_{SW}) from (P_{LO}, $(\frac{g_m}{I_D})_{LO}$) obtained in the design.

Table 4.1: Design Space of the Gilbert-cell mixer Parameters

Parameter	**Value/Range**	**Unit**
Channel Length	$0.13 \longleftrightarrow 1$	μm
Drain Current Efficiency ($\frac{g_m}{I_D}$)	$1 \longleftrightarrow 30$	V^{-1}
LO Power (P_{LO})	-10 $\longleftrightarrow$ 10	dBm
Output Load (R_L)	$1 \longleftrightarrow$ 100k	Ω
Parameter	**Dependency**	**Unit**
Threshold Voltage (V_T)	$f(L)$	V
Overdrive Voltage (V_{OV})	$f(\frac{g_m}{I_D}, V_T)$	V
Intrinsic Gain ($\frac{g_m}{g_o}$)	$f(\frac{g_m}{I_D})$	
Transit Frequency (f_T)	$f(V_{OV}, L)$	Hz
Current Density (ID/W)	$f(\frac{g_m}{I_D})$	A/m
Drain Current (I_D)	$f(Power)$	A
Transconductance (g_m)	$f(\frac{g_m}{I_D}, I_D)$	S
Switch Gain (A_{SW})	$f\left(P_{LO}, \left(\frac{g_m}{I_D}\right)_{LO}\right)$	

Table 4.2: Performance Dependence on the Design Space

Specification Parameter	Dependency	Unit
Power	$f(V_{DD}, I_{D,RF})$	W
Conversion Gain (CG)	$f(g_{m,RF}, R_L, A_{SW})$	dB
Input Third-order Intercept Point (IIP_3)	$f(\left(\frac{g_m}{I_D}\right)_{RF}, \left(\frac{g_m}{I_D}\right)_{IF})$	dBm
Noise Figure (NF)	$f(\left(\frac{g_m}{I_D}\right)_{RF}, \left(\frac{g_m}{I_D}\right)_{LO}, CG)$	dB

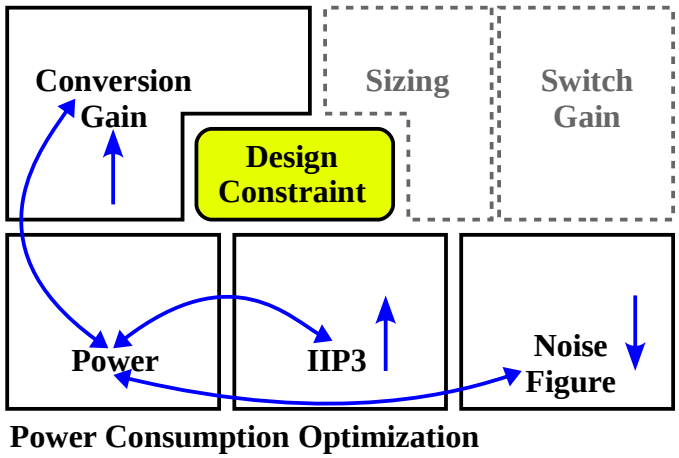


Figure 4.5: Diagram of the proposed Design methodology for the Gilbert-cell mixer

The combination of two constraints is presented in Fig. 4.6. In this case a design constraint of power and gain will affect directly the degradation or improvement of the other perfomance parameters (IIP_3 and NF). This can be applied to another combination

of two constraints. For example, the transconductance stage ($g_{m,RF}$) from the conversion gain, can be calculate from the IIP_3 and Power, or the NF and Power, respectively.

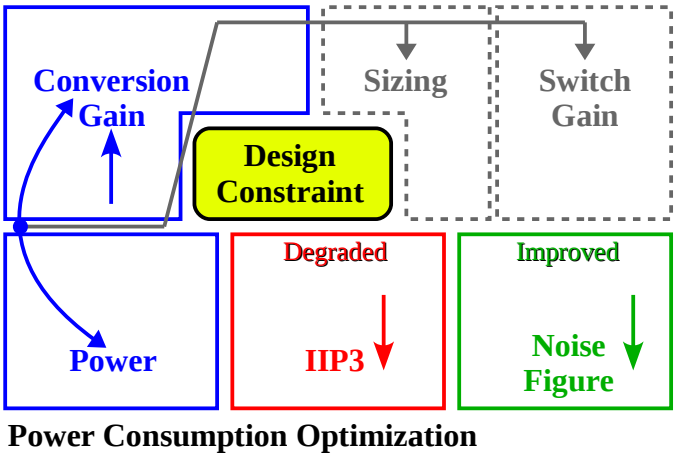


Figure 4.6: Diagram of the proposed Design methodology for the Gilbert-cell mixer

In order to use the design methodology defined above, a parameters characterization: IIP_2, IIP_3 and the NF of Gilbert-cell mixer was implemented. Table 4.3 resumes the employed simulation parameters for the Gilbert-cell mixer characterization. A power and conversion gain were defined as design constraints.

The transition frequency (f_T) of the IBM 0.13 μm process is above 80 GHz and Gilbert-cell mixer characterized at 2 GHz, a transistor channel length of $L = 200nm$ is chosen as trade-off between a low V_T in order to avoiding short-channel effects and speed.

Since the switching gain (A_{SW}) is a function of the shape and the amplitude of the LO Power (P_{LO}) and drain current efficiency of the switching transistors ($(\frac{g_m}{I_D})_{LO}$). In appendix D.2 a plot of A_{SW} was generated showing this dependency.

Table 4.3: Simulation Parameters for the Characterization of the Gilbert-cell mixer

Parameter	Value	Unit
V_{DD}	1.2	V
Power Consumption	5	mW
LO Signal Power (P_{LO})	3.5	dBm
Conversion Gain (CG)	8	dB
Frequency	2	GHz
Tone spacing (for IIP_3)	1	MHz
IF Frequency	500	kHz
Load (R_L) mismatch ($\frac{\Delta_{RL}}{R_L}$)	0.5	%
LO transistor threshold offset (ΔV_T)	0	mV
LO common mode	0.7	V
IF common mode	0.7	V

The noise figure and IIP_3 were plotted as a function of the drain current efficiency of the transistor of the transconductance stage $(\frac{g_m}{I_D})_{RF}$ and are shown in Fig. 4.7 and 4.8, respectively. As was expected both parameters were inversely proportional to the $(\frac{g_m}{I_D})_{RF}$.

Additional plots for the $IP1dB$ and IIP_2 vs $(\frac{g_m}{I_D})_{RF}$, and feedthrough between ports can be found in appendix D.2.

These plots will be used as a starting point in the design of the proposed mixers in the following section.

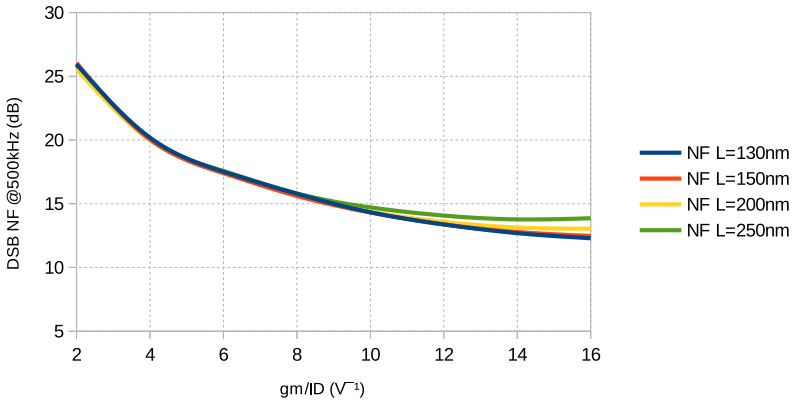


Figure 4.7: DSB NF @ 500kHz vs $(\frac{gm}{I_D})_{RF\ stage}$

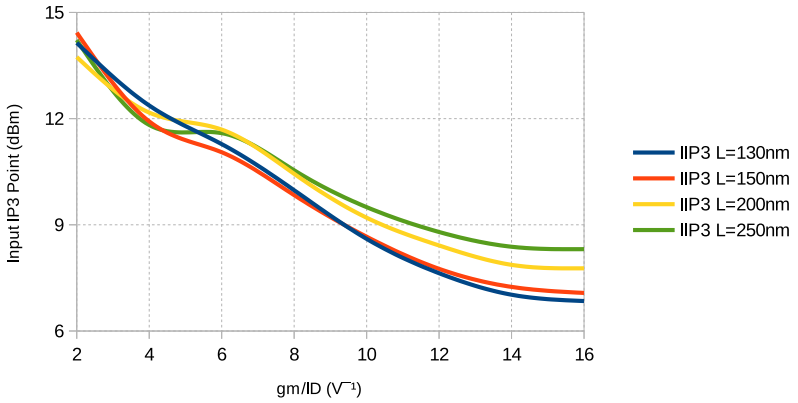


Figure 4.8: IIP_3 vs $(\frac{gm}{I_D})_{RF\ stage}$

Assuming a hard-switching local oscillator (LO) signal and the corresponding square-wave approximation, it can be shown in KIVEKAS; PARSSINEN; HALONEN (2001) that the IIP_2 can be estimated with the following equation when the switching transistor (M_{LO}) are considered ideal:

$$IIP_2 \approx \frac{\sqrt{2}}{\pi \eta_{nom} \alpha_2} \times \frac{4}{2 \cdot \Delta\eta(\Delta g_{m,RF} + \Delta A_{RF}) + \Delta R_L(1\Delta g_{m,RF}+)(1+\Delta A_{RF})} \tag{4.2}$$

Parameters $g_{m,RF}$, α_2 and $\Delta g_{m,RF}$ in Eq. 4.2 are the nominal transconductance, second-order non-linearity coefficient, and transconductance deviation of the two transistors M_{RF}. ΔA_{RF} is the amplitude difference at the RF+ and RF- inputs, and ΔR_L is the discrepancy between the two load resistors. The nominal LO duty cycle is η_{nom}, which has an associated mismatch of $\Delta\eta$ between LO+ and LO-. It is worthwhile to point out that the $\Delta\eta$ term exclusively depends on the LO signal under the ideal switching core assumption, but it becomes strongly affected by threshold voltage offsets of the switching transistors in the practical case. This switching transistor-dependent IIP_2 degradation can be as severe as the degradation due to load mismatches.

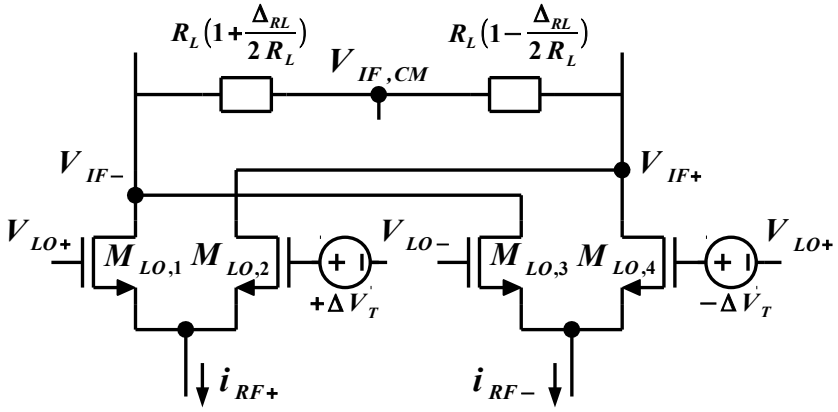


Figure 4.9: LO transistor threshold voltage offset (ΔV_T) and Load resistor mismatch ($\frac{\Delta R_L}{R_L}$) modeling for IIP_2 characterization

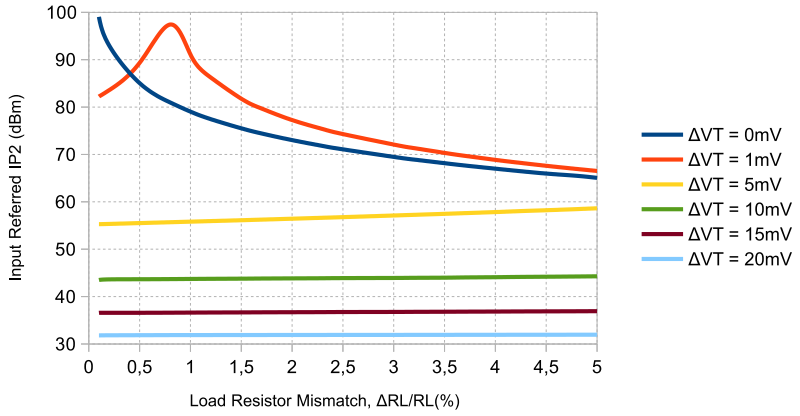


Figure 4.10: IIP_2 characterization, considering LO transistor threshold voltage offset (ΔV_T) and Load resistor mismatch ($\frac{\Delta R_L}{R_L}$)

It can be observed from Eq. 4.2 that any mismatch between the branches deteriorate the IIP_2. Furthermore, the adverse effects from $\Delta g_{m,RF}$ and ΔA_{RF} scale with ΔR_L and

$\Delta\eta$, implying that the fundamental IIP_2 limit depends primarily on the load resistor and LO signal/transistor mismatches. The second term in the second denominator gives rise to the importance of accurate load resistor matching. The mismatch between switching transistors (M_{LO}) is modeled by ΔV_T and the load resistors (R_L) mismatch by ($\frac{\Delta R_L}{R_L}$), Fig. 4.9.

Fig. 4.10 shows the characterization of IIP_2 considering the ΔV_T and $\frac{\Delta R_L}{R_L}$ mismatches. The value of IIP_2 for the mixers designed in the following section will be evaluated through Monte Carlo Analysis.

4.3 Downconversion Mixer for Multi-Band and Multiple Standards

The two proposed topologies for multi-band multi-standard operation proposed in chapter three will be designed. The first topology will work at a central frequency of 2 GHz and the second between 1 to 6 GHz as defined in chapter three. Regarding the specifications for both topologies, Table 4.4 summarizes the specification that may comply with multi-band and multi-standard operation. These specifications were chosen using chapter two as reference.

The design of the two topologies was implemented using the methodology described in the previous section. For the first topology a design constraint of power and gain was chosen to obtain the best trade-off between noise and linearity. For the second topology the same design constraint was selected, but with emphasis on noise reduction.

Table 4.4: Mixer specifications for Multi-Band and Multi-Standard Operation

Specification	Value	Unit
Power	≤ 25	mW
Conversion Gain (CG)	≥ 10	dB
DSB NF @ IF=500 kHz	≤ 15	dB
IIP_3	≥ 0	dBm
IIP_2	≥ 60	dBm

4.3.1 Design Procedure

4.3.1.1 First Topology

Fig. 4.11 presents the schematic diagram of the first topology. We design this topology was designed for a 2 GHz operation. A design constraint between power consumption and the gain was defined, in order to achieve the lowest NF and the highest IIP_3. Table 4.5 summarizes constraints defined for the first topology.

We employ the Gilbert-cell mixer design methodology for transistor sizing. From the previous section we know that the NF and IIP_3 are inversely proportional to the $\frac{gm}{I_D}$ of the transistors of the transconductance stage (M_1, M_2), a value $\left(\frac{gm}{I_D}\right)_{M_1,M_2}$ equal to 10 (moderate inversion) is chosen as a trade-off between noise and distortion. Regarding the linearization transistors (M_{1a}, M_{2a}), we know from section 3.3.3 from chapter 3 that they operate in weak inversion. Recalling the expressions of g'_1, g'_3 of the IIP_3 from section

3.6.3 from chapter 3:

$$g_1' = g_1 - ag_1 \tag{4.3}$$

$$g_3' = g_3 - cg_{a1} - 2abg_{a2} - a^3 g_{a3} \tag{4.4}$$

where the index 1, 2, and 3 of g represent the transconductance, first- and second-order derivative of the transconductance of transistors M_1 and M_{1a}, respectively. We choose the $\left(\frac{gm}{I_D}\right)_{M_{1a},M_{2a}}$ in a manner that g_3' is reduced to a minimum close to zero. This linearization technique is limited by the fact that it expects transistors (M_1, M_2) operating in strong inversion, but we already choose them to operate in moderate inversion (trade-off NF and IIP_3).

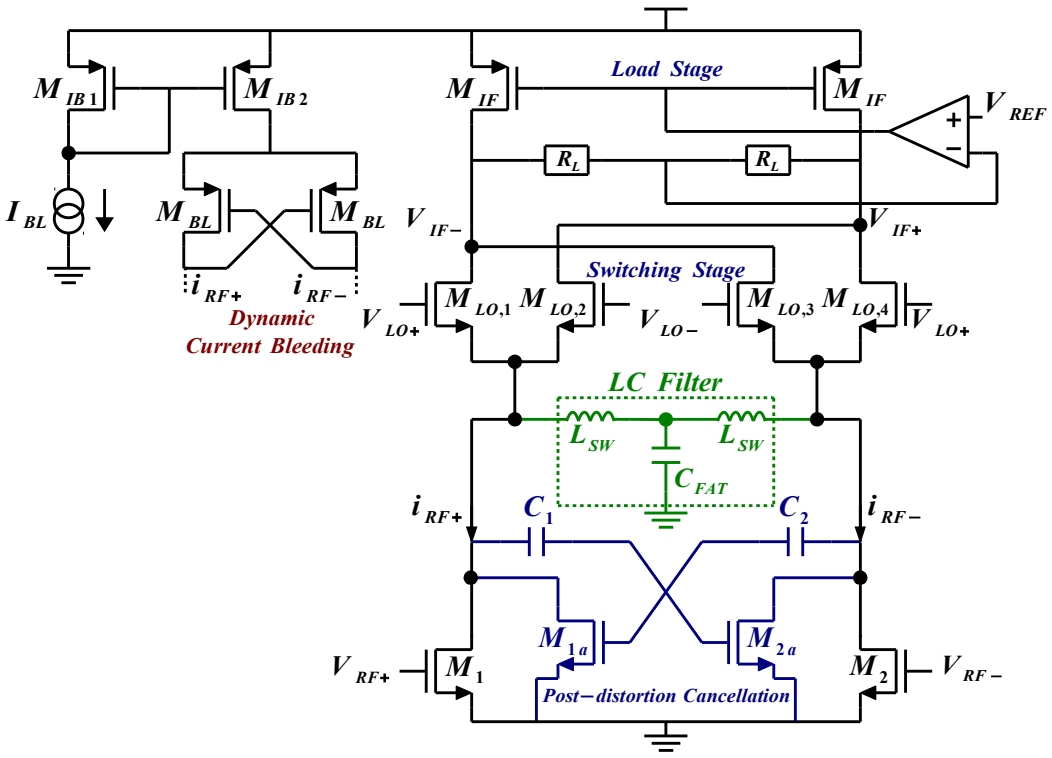


Figure 4.11: First Proposed Topology for the Active Downconversion Mixer

Table 4.5: Constraint Parameters for the First Topology

Parameter	Value	Unit
V_{DD}	1.2	V
Power Consumption	5	mW
Frequency	2	GHz
LO Signal Power (P_{LO})	2.5	dBm
Conversion Gain (CG)	≥ 10	dB

The switching transistors (M_{LO}) are chosen to operate in weak inversion as a compromise between noise and gain. Using the plot generated for the switch gain (A_{SW}) in Fig. D.7 as reference, a $\left(\frac{gm}{I_D}\right)_{M_{LO}}$ of 18 is chosen as a trade-off between A_{SW} and LO power. The value of L_{SW} of the L-C filter is chosen to resonate the parasitic capacitance of the switching transistors at 2 GHz. Capacitor C_{FAT} is chosen to provide an AC ground to the intermodulation currents.

The transistors of the dynamic bleeding current (M_{BL}) are chosen to steer half the current of the switching transistors and to operate in strong inversion in order to keep their size small and minimize their parasitic contribution. Finally the active load transistors (M_{IF}) are chosen to operate in moderate inversion as a compromise between noise and area.

Table 4.6: Comparison of the improvements applied to the First Topology

	$\left(\frac{g_m}{I_D}\right)_{RF}$ = 4.5				$\left(\frac{g_m}{I_D}\right)_{RF}$ =10			
	GC	GC+PDHC	GC+PDHC+LC	GC+PDHC+LC+DCI	GC	GC+PDHC	GC+PDHC+LC	GC+PDHC+LC+DCI
Conversion Gain (dB)	10.3	10.2	10.1	10.3	10.3	10.1	10.2	10.2
Power (mW)	5.14	5.15	5.15	5.3	5.15	5.16	5.16	5.3
Output Load (R_L) (Ω)	700	680	650	520	270	260	260	205
$I_{D,RF}$ (mA)	2	2	2	2	2	2	2	2
$P1dB$ (dBm)	-2.5	-2.4	-2.1	-1.6	-3.9	-3.8	-3.4	-1.8
IIP_3 (dBm)	9.9	10.1	10.9	13.4	6.6	6.7	7.6	10.9
DSB NF@500 kHz	20.2	20.2	19.8	17.3	15	15	14.4	12

In addition to the designed mixer of the first topology with all the added improvements (PDHC, L-C filter, Dynamic Current Bleeding), another mixer was designed, for a $\left(\frac{gm}{I_D}\right)_{M_1,M_2}$ equal to 4.5, to compare the specifications of each design. Table 4.6 shows the two designed versions of the first topology and the impact of each one of the improvements. As it was expected, the mixer designed with the RF transistors in strong inversion presents a higher IIP_3 and NF in comparison to the other mixer with the RF transistors operating in moderate inversion. Regarding the improvements is evindently the gradual improvements of specifications. However, some remarks can be made: The PDHC combined other improvements can achieve nearly 4 dB more of IIP_3 than the Gilbert-cell and has no significative impact on the NF. The Dynamic current bleeding circuit can achieve above 3 dB of NF reduction.

Table 4.7: Design constraint of IIP_3, NF for the First Topology

	DSB NF@500 kHz $\leq$ 11 dB	$IIP_3 \geq$ 13 dBm	Trade-off NF $\leq$ 15 dB $\wedge$ $IIP_3 \geq$ 10 dBm
Conversion Gain (dB)	10.3	10.3	10.2
Power (mW)	5.3	5.3	5.3
Output Load (R_L) (Ω)	160	520	205
$\frac{g_m}{I_D}$, RF transistor (V^{-1})	16	4.5	10
$I_{D,RF\,transistor}$ (mA)	2	2	2
$P1dB$ (dBm)	-4.2	-1.6	-1.8
IIP_3 (dBm)	4.5	13.4	10.9
DSB NF @500 kHz	10.6	17.3	12

A design constraint for an individual specification of NF and IIP_3 was also implemented and compared to the designed mixer of the first topology, Table 4.7 shows the

comparison between those individual designs. Design to achieve any individual specification is straightforward, but can compromise other specs. The final version of the first topology was designed taking into account a spec trade-off between NF and IIP_3.

Table 4.8 summarizes the device parameters of the mixer of the first topology.

Table 4.8: Device Parameters for the First Topology

Active	$\frac{g_m}{I_D}$ (V^{-1})	I_D (mA)	$\underbrace{m}_{multiplier} \times \underbrace{f}_{finger} \times \underbrace{(W/L)}_{unit\ transistor}^{(\mu m/\mu m)}$
M_1, M_2	10	2	12×4×(1.5/0.2)
M_{1a}, M_{2a}	26	0.019	4×4×(1.5/0.2)
M_{LO}	18.3	0.73	16×4×(1.5/0.2)
M_{IF}	12.9	1.33	50×1×(15/0.5)
M_{B1}, M_{B2}	8	0.05 - 1.41	2×1×(5/0.5) - 60×1×(5/0.5)
M_{BL}	4.4	0.7	10×1×(5/0.5)
Passive	Value	Unit	Size (W/L) (μm/μm)
R_L	205	Ω	1.58/1
C	1	pF	11.5/11.5
C_{FAT}	9.6	pF	4×(20/20)
L_{SW}	12	nH	Outer=300um; Width=5u; turns=6

4.3.1.2 Second Topology

Since the second topology, Fig. 4.12, is going to operate in the frequency range of 1 to 6 GHz, two specifications were chosen to be optimize: noise and distortion. For that reason a series of constraints parameters for the design were defined. Table 4.9 summarizes those parameters.

Table 4.9: Constraint parameters for the Gilbert-cell Mixer for Multi-Band (Second Topology)

Parameter	Value	Unit
V_{DD}	1.2	V
Power Consumption	≤ 25	mW
Frequency	$1 \longleftrightarrow 6$	GHz
LO Signal Power (P_{LO})	3.5	dBm
Conversion Gain (CG)	$\geqq 10$	dB
DSB NF @ IF=500 kHz	≤ 10	dB
IIP_3	≥ 0	dBm

Thermal noise cancellation is used to achieve the lowest Noise Figure for the second topology. The noise-canceling transconductors must comply with the following :

$$Z_{IN} = \frac{1}{g_{m,1a} + g_{m,1b}} \qquad Z_{IN} = R_S \tag{4.5}$$

Where Z_{IN} is the input impedance seen from transconductor stage and R_S is the source impedance, which is 50Ω. The noise cancellation condition is achieve when

$$\frac{g_{m2}}{g_{m3}} = 1 + \frac{R}{R_S} \tag{4.6}$$

giving the matching device $M_{1a} - M_{1b}$ the lowest possible Noise Figure BRUCCOLERI; KLUMPERINK; NAUTA (2004). R is the shunt-feedback resistor of the inverter (M_{1a}, M_{1b}).

We employ the Gilbert-cell mixer design methodology for transistor sizing. The transistors of the noise-canceling transconductor are chosen using the above equations as trade-off between noise and power consumption. Regarding the linearization transistors (M_{aux}, $M_{ibuffer}$). M_{aux} is chosen using the method as described in the first topology. $M_{ibuffer}$ operates in strong inversion in the linear region. The switching transistors (M_{LO}) are chosen to operate in weak inversion as a compromise between noise and gain. Finally the active load transistors (M_{IF}) are chosen to operate in the moderate inversion as compromise between noise and area. For all transistors of the second topology a minimum length of 0.12 μm was chosen in order to have the highest f_T per transistor.

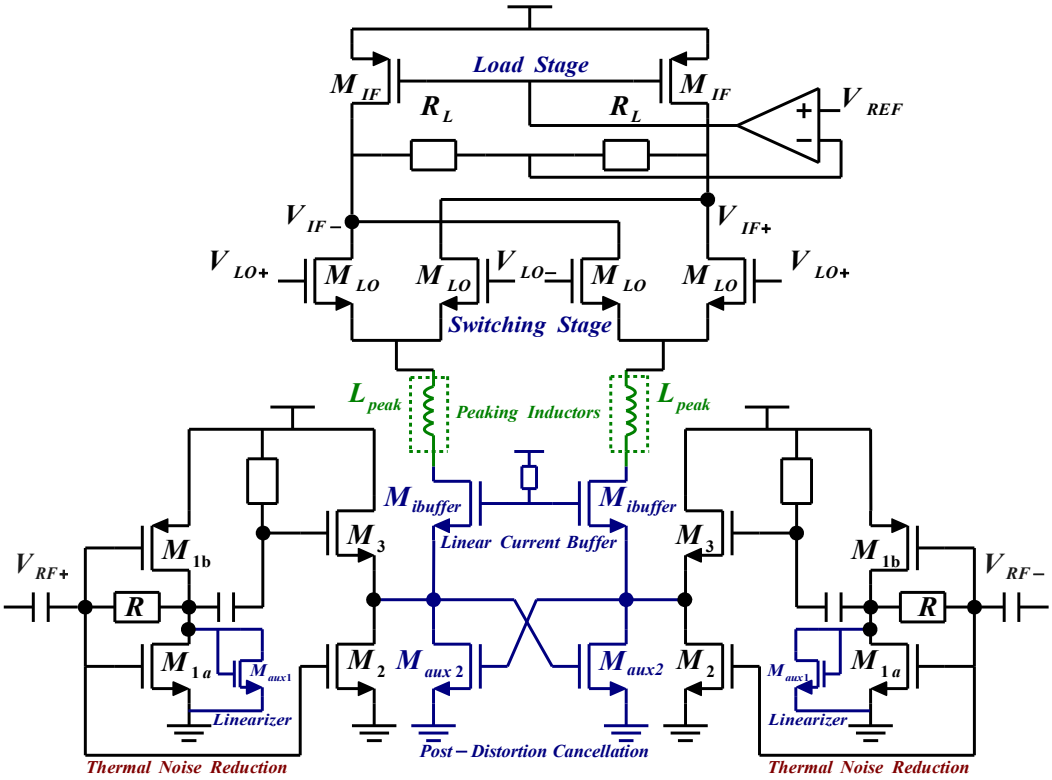


Figure 4.12: Second Proposed Topology for the Active Downconversion Mixer

Table 4.10 summarizes the device parameters of the mixer of the second topology.

Table 4.10: Device parameters for the Second Topology

Active	$\frac{g_m}{I_D}$ (V^{-1})	I_D (mA)	$\underbrace{m}_{multiplier} \times \underbrace{f}_{finger} \times \underbrace{(W/L)(\mu m/\mu m)}_{unit\ transistor}$
M_{1a}	8.6	1.4	4×4×(1.5/0.12)
M_{1b}	7.6	1.74	14×4×(1.5/0.12)
M_2	9	6.06	20×4×1.5/0.12)
M_3	4	6.02	6×4×(1.5/0.12)
M_{aux1}	8.6	0.34	1×4×(1.5/0.12)
M_{aux2}	23.7	0.11	14×4×(1.5/0.12)
$M_{ibuffer}$	2.9	0.15	8×4×(1.5/0.12)
M_{LO}	26.7	0.075	30×4×(1.5/0.2)
M_{IF}	16.6	0.15	50×1×(15/2)
Passive	Value	Unit	Size (W/L) (μm/μm)
R	1k	Ω	1/4
R_L	120	Ω	2.68/1
L_{peak}	1	nH	Outer=100um; Width=5u; turns=3.5

4.3.2 Simulation Results

4.3.2.1 First Topology

The first topology was designed for a frequency of 2 GHz. The specifications of the mixer such as : conversion gain, NF, $IP1dB$, IIP_3 and IIP_2 were simulated at the post-layout level of this circuit. Table 4.11 presents the simulation parameters used to characterize those specifications.

Table 4.11: Simulation Parameters for the First Topology

Parameter	Value	Unit
V_{DD}	1.2	V
LO Signal Power (P_{LO})	2.5	dBm
Frequency	2	GHz
Tone spacing (for IIP_3)	1	MHz
IF Frequency	500	kHz
Load (R_L) mismatch ($\frac{\Delta_{RL}}{R_L}$)	0.5	%
LO transistor threshold offset (ΔV_T)	5	mV
LO common mode	0.7	V
IF common mode	0.7	V

The simulation results for the first topology were obtained with a 1.9995 GHz sinusoidal LO signal having a power of 2.5 dBm. As seen in Fig. 4.13, this mixer has a conversion of 10.2 dB for RF input signals located up to 100 MHz away from the LO frequency. This mixer was optimized to achieve high linearity, this required a conversion gain trade-off that resulted in 10.2 dB of conversion gain.

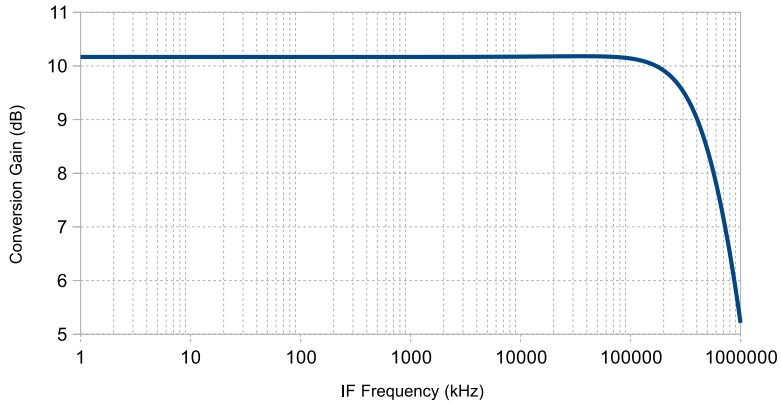


Figure 4.13: Conversion Gain vs. IF Frequency

Fig. 4.14 shows the noise figure (NF), since the designed mixer is going to operate in a low-IF (500 kHz) receiver. The double-sideband (DSB) NF obtained is 12 dB.

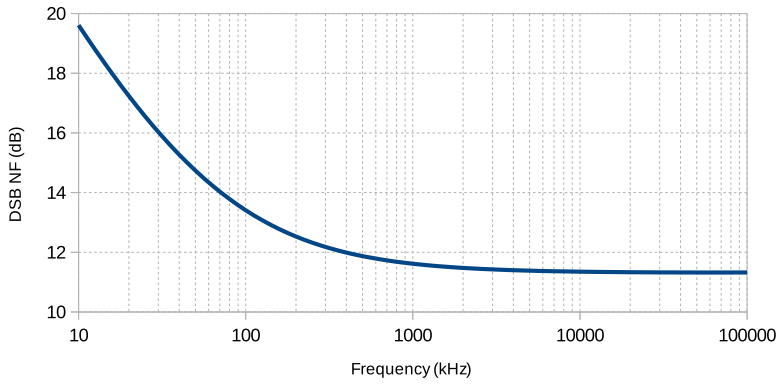


Figure 4.14: DSB Noise Figure vs. Frequency

Linearity characteristics were assessed within a 20 MHz band under consideration that the mixer is intended for broadband wireless target applications. The simulated IIP_3 of 10.9 dBm in Fig. 4.15 was obtained with two tones located at 2.0 GHz and 2.001 GHz (0.5 MHz and 1.5 MHz away from the 1.9995 GHz LO frequency).

Fig. 4.16 shows the transient signals from a simulation of the mixer with a -30 dBm differential RF input signal at 2 GHz and a 2.5 dBm differential LO at 1.9995 GHz. As expected, the differential IF output signal (IF+ to IF-) has a frequency of 1 MHz and an amplitude of 33.2 mV, indicating a conversion gain of 10.2 dB relative to the 10 mV RF input amplitude.

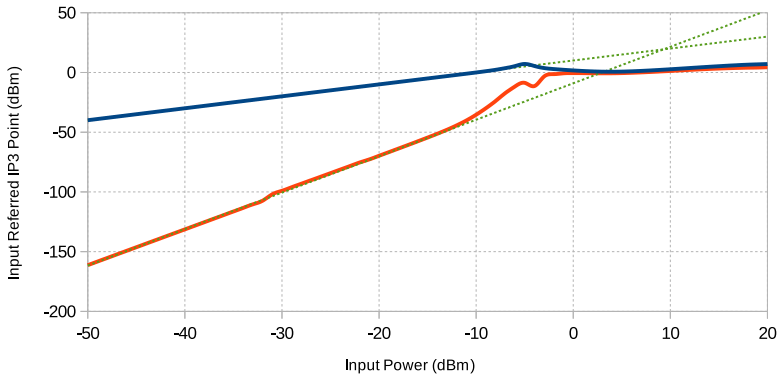


Figure 4.15: IIP_3 vs. Input Power. LO frequency: 1.9995 GHz, RF test tones: 2 GHz, 2.001 GHz, IM_3 frequency: 2 MHz

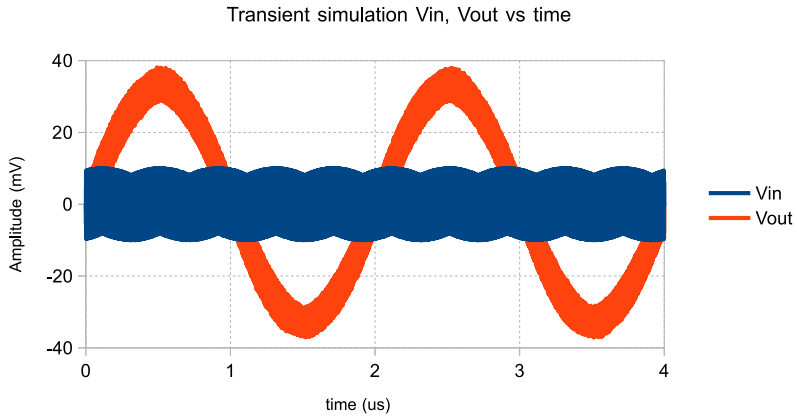


Figure 4.16: Transient simulation with a 500 kHz IF output signal. (LO frequency: 1.9995 GHz, RF input signal: -30dBm at 2GHz)

Under a nominal voltage supply of 1.2 V with a temperature range of [-55 ~125] °C corner simulations were performed in order to test the robustness of the circuit. Table 4.12 presents the corner simulation results. The conversion gain presents minimum value of 9.3 dB and the noise figure a maximum value of 12.6 dB across all corners, and does not deviate to much from the specs. In the other hand we note that the IIP_3 with the exception of two corners (gain sensitive) presents a minimum value of 8.6 dBm confirming the robustness of the linearization technique. In the overall results for first topology are quite good.

Performance variations in the presence of realistic device mismatches in the mixer were estimated at 2 GHz with Monte Carlo analysis. Table 4.13 summarizes the performance variations (mean and standard deviation) for conversion gain, DSB NF, $IP1dB$, IIP_2, IIP_3, and feed-throughs.

We achieved for the first topology working at 2GHz: a conversion gain of 10.2 dB and a DSB NF of 12 dB, with a low-IF of 500kHz. The mixer presents an IIP_2 and IIP_3 of 55.5dBm and 10.9dBm, respectively, while consuming only 5.3mW from a 1.2V supply.

Table 4.12: Corner Simulation of the First Topology

		V_{DD} = 1.2V												
		Temperature = -55 °C				Temperature = 27 °C				Temperature = 125 °C				
Specification	Typ	SS	SF	FS	FF	SS	SF	FS	FF	SS	SF	FS	FF	Unit
Conversion Gain	10.2	11.8	12	12.9	13.2	9.3	9.6	10.5	10.9	14.9	14.6	14	13.6	dB
DSB NF @500 kHz	12	10	9.9	9.1	8.7	12.6	12.3	11.7	11.3	7.2	7.6	8.5	8.9	dB
1-dB compression point	-1.8	-2.2	-2.5	-3.1	-3.6	-1.4	-1.6	-2	-2.4	-2	-1.9	-2.2	-2.3	dBm
IIP_3	10.9	10.6	9.4	5.7	4.4	10.4	11.7	9.9	8.6	8.9	9.9	9.5	10.3	dBm
IIP_2 (With ΔV_T= 5mV and $\frac{\Delta R_L}{R_L}$= 0.5%)	55.5	47.6	46.8	44.8	43.8	57.3	56	54.9	53.4	66.3	64.5	64.8	63	dBm

Table 4.13: Simulated Specifications of the First Topology

	Specification*	Unit
RF frequency	2	GHz
IF bandwidth	< 100	MHz
Conversion Gain† 100% Samples	μ=10.1; σ=0.7 > 7.5	dB
DSB NF @500 kHz† 97% Samples	μ=12; σ=0.4 <13	dB
1-dB compression point† 99% Samples	μ=-2.7; σ=0.8 > -5.1	dBm
IIP_3 † 90% Samples	μ=9; σ=3.1 > 6.2	dBm
IIP_2 (ΔV_T= 5mV and $\frac{\Delta R_L}{R_L}$= 0.5%)	55.51	dBm
IIP_2 † 95% Samples	μ=54.5; σ=9.6 > 42	dBm
RF-IF isolation† 100% Samples	μ=-50; σ=6.6 < -40.8	dB
LO-IF isolation† 100% Samples	μ=-55.8; σ=7.2 < -44.8	dB
LO-RF isolation† 100% Samples	μ=-50; σ=6.6 < -40.8	dB
Power	5.3	mW

* Simulation results; † Process and Mismatch (1000 runs)

In appendix D.3, additional simulation results are shown: linearity specifications ($IP1dB$, IIP_2 and two tones frequency spacing for IIP_3), feedthrough between the mixer ports, the progression of the conversion gain, DSB NF, $IP1dB$, IIP_2 and IIP_3 for a sweep of the LO signal power.

4.3.2.2 Second Topology

The second topology was designed to cover the frequency range between 1 to 6 GHz. The specifications of the mixer such as : conversion gain, NF, S_{11}, $IP1dB$, IIP_3 and IIP_2 were simulated at the schematic level of this circuit. Table 4.14 presents the simulation parameters used to characterize those specifications.

The simulation results for the second topology in the frequency range of 1 to 6 GHz were performed using a sinusoidal LO frequency below 500 kHz the input RF (low-IF) with a power of 3.5 dBm. In order to evaluate the linearization technique implemented

in the first topology in wideband operation, two versions of the second topology were simulated (with and without PDHC).

Table 4.14: Simulation Parameters for Second Topology

Parameter	Value	Unit
V_{DD}	1.2	V
LO Signal Power (P_{LO})	3.5	dBm
Frequency	$1 \longleftrightarrow 6$	GHz
Tone spacing (for IIP_3)	1	MHz
IF Frequency	500	kHz
Load (R_L) mismatch ($\frac{\Delta_{RL}}{R_L}$)	0.5	%
LO transistor threshold offset (ΔV_T)	5	mV
LO common mode	0.7	V
IF common mode	0.7	V

As seen in Fig. 4.17, the mixer with PHDC presents a lower drop in the conversion gain compared to the one without PHDC, the cross-coupled pair acts as a negative resistance compensating the output resistance of the transconductance stage. The noise figure for the circuit with PDHC increases due to the current noise contribution of the cross-coupled pair. The conversion gain presents minimum value of 11 dB and the noise figure a maximum value of 11 dB across the frequency range.

Both circuits present a good matching for the range of 1 to 6 GHz, Fig. 4.18 presents the S_{11} for both circuits.

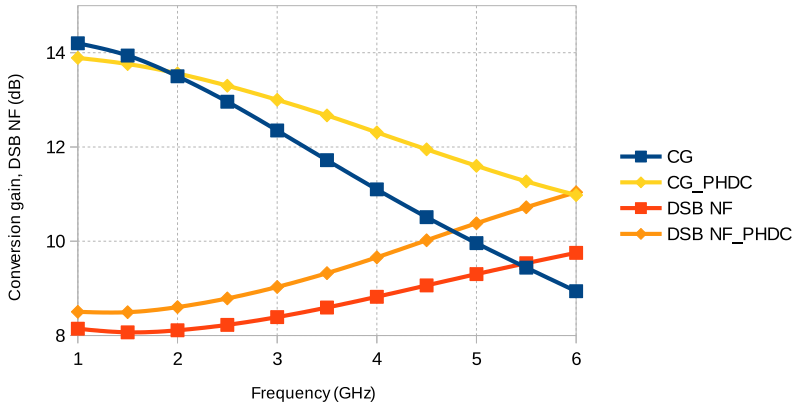


Figure 4.17: Conversion Gain and DSB NF@ 500 kHz (with/without PDHC) for the Frequency Range

Regarding linearity, Fig. 4.19 shows the effects of the PDHC technique, an considerable improvement (about 6dB) in the $IP1dB$ and IIP_3 was achieved. The second topology

was able to maintain an IIP_3 of 0 dBm for the whole frequency range. The IIP_2 was simulated considering a 0.5% load resistor mismatches ($\frac{\Delta R_L}{R_L}$) and 5 mV of mismatch between switching transistors (ΔV_T), shown in Fig. 4.20.

We achieved for the second topology working between 1 to 6 GHz: a conversion gain higher than 11 dB and a DSB NF of lower than 1 dB, with a low-IF of 500kHz. The mixer presents an average IIP_3 of 0 dBm while consuming only 19.3 mW from a 1.2 V supply.

Table 4.15 summarizes the specs of the second topology for the range of 1 to 6 GHz.

In appendix D.4, additional simulation results are shown. The second topology was simulated at 2 GHz input RF, parameters such as : conversion gain, NF, S_{11}, NF, $IP1dB$, IIP_2, IIP_2 and feed-throughs were characterized through corners and Monte Carlo analysis.

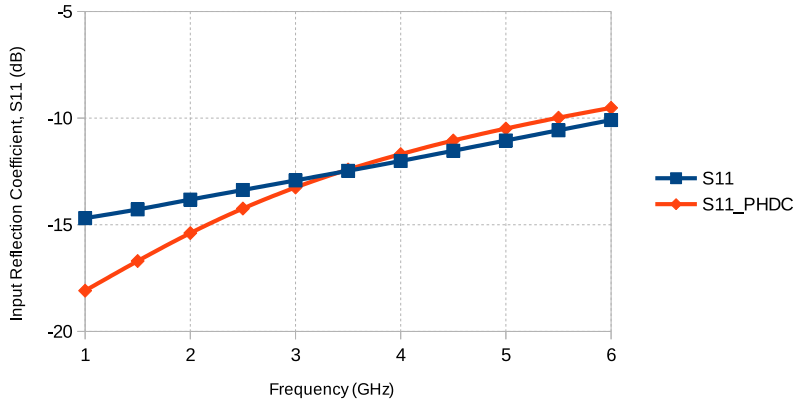


Figure 4.18: Input Reflection Coefficient, S_{11} (with/without PDHC) for the Frequency Range

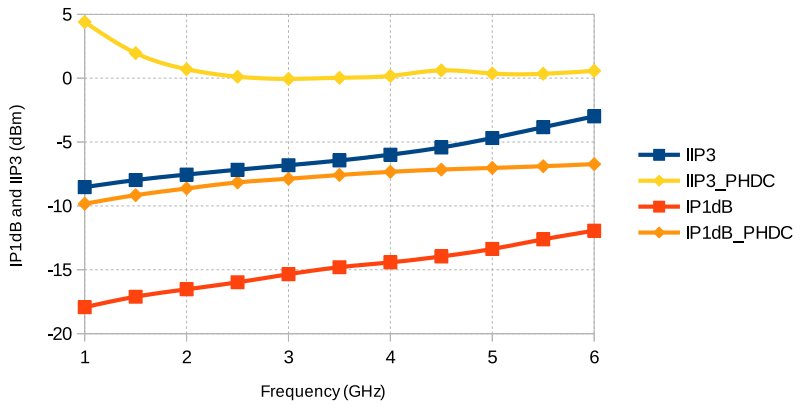


Figure 4.19: Linearity Parameters : $IP1dB$, IIP_3 (with/without PDHC) the Frequency Range.

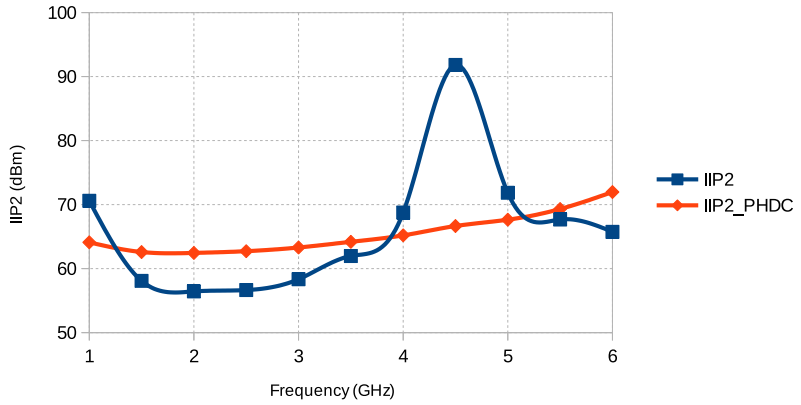


Figure 4.20: IIP_2 (with/without PDHC) for the Frequency Range. (ΔV_{TH}= 5mV and $\frac{\Delta R_L}{R_L}$= 0.5%)

Table 4.15: Simulated Specifications for 1 to 6 GHz for Second Topology

Specification	Value	Unit
RF frequency	$1 \longleftrightarrow 6$	GHz
IF bandwidth	< 100	MHz
Conversion Gain	$13.9 \longleftrightarrow 11$	dB
Input Reflection Coefficient, S_{11}	$-18 \longleftrightarrow -9.5$	dB
DSB NF @500 kHz	$8.5 \longleftrightarrow 11$	dB
1-dB compression point	$-9.8 \longleftrightarrow -6.7$	dBm
IIP_3	$4.4 \longleftrightarrow 0.6$	dBm
IIP_2 (With ΔV_T= 5mV and $\frac{\Delta R_L}{R_L}$= 0.5%)	$64 \longleftrightarrow 72$	dBm
Power	19.3	mW

4.4 Layout

The layout of the Downconversion mixer (First Topology) was implemented using the IBM 0.13 µm process design kit (PDK), CMOS 8RF-DM (CMRF8SF, option DM). A brief introduction to the PDK is presented.

4.4.1 IBM 0.13 μm PDK (CMRF8SF-DM)

The CMOS8RF design kit comes in four versions that correspond to the technology last metal options: LM that has a 0.55 µm thick Cu last metal. AM that has a 4 µm thick Al last metal. DM that has a 0.45 µm aluminum layer LY, a 3 µm thick copper layer E1 followed by a 4 µm thick aluminum top layer MA and OL that has a 3 µm thick copper layer OL followed by a 4 µm thick aluminum top layer LD. They offer designer a wide variety of metal options to choose from.

CMOS8RF designated name by IBM for this 0.13 µm technology that is used on the IBM Customer Connect (ICC). The design kit name is also CMRF8SF which is used in the PDK. Its short designation is 8RF. Both names are used interchangeable.

IBM's CMOS8RF technology starting wafer is doped p-type with a resistivity of 1-2 Ohm-cm. The lithography node is 130 nm. The technology utilizes shallow trench isolation (STI), nominally 0.35 µm deep into the silicon, to provide a dense isolation

between devices. All diffusion and polysilicon are silicided for low resistivity unless the silicide formation is intentionally blocked to form resistors with a higher specific sheet resistance.

The process cross-section is shown in Fig. 4.21.

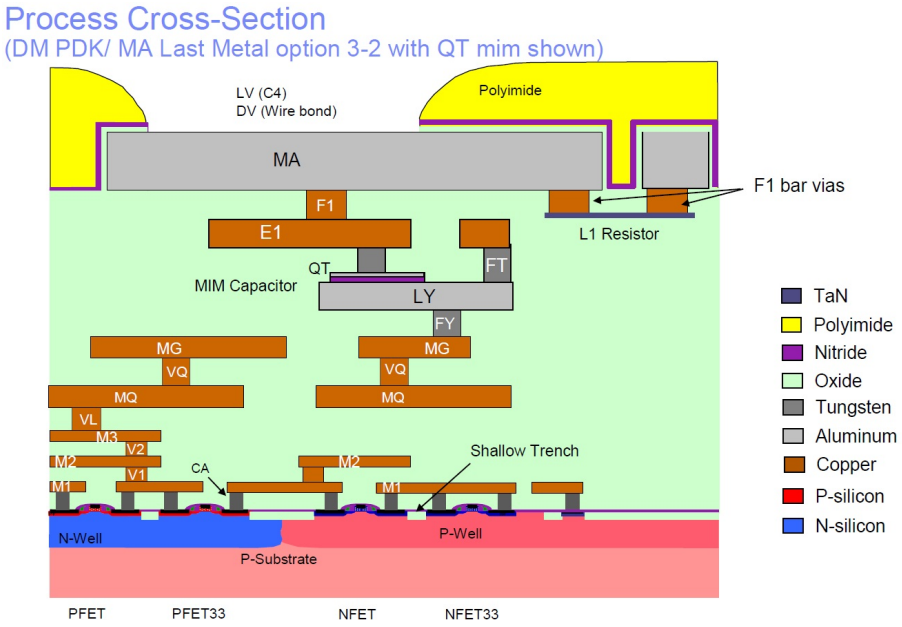


Figure 4.21: IBM 0.13 μm CMOS 8RF Process cross-section

From the devices available on the PDK, those shown in Table 4.16 were used in the layout of the first topology.

Table 4.16: Devices used from the PDK

Device	Name	Type	Characteristics
Resistor	*oprppres*	RP poly over isolation	228 Ω/□, ±8% Tolerance
Capacitors	*dualmimcap*	Metal-Insulator-Metal	4.1 fF/μm^2.
Inductor	*ind_inh*	Spiral inductor	High-Q, Low parasitc, BFMOAT or M1 ground plane
Transistor	*nfet/pfet*	NMOS/PMOS	$V_{DD} = 1.2V$, $t_{ox} = 22\dot{A}$, $L_{min} = 0.12\mu$, $V_{tsat} = 340mV$

4.4.2 Layout Considerations

The performance of analog and RF circuits are heavily influenced by the layout. To maximize RF performance and minimize noise performance, the mixer needs careful layout. There has been many issues regarding to proper layout for specific circuits, and typical layout considerations can be summarized as followed.

- Multi-finger transistors

The width of the transistor is much larger than the length for typical analog and RF transistors. Thus, wide transistors are usually folded so that the gate resistance and S/D junctions are reduced. For our design, all transistors employ this multi-fingers. All transistor gates are connected at both ends to reduce gate resistance.

- Symmetry

The second order nonlinearities in a CMOS differential design can be affected by any asymmetry or systematic mismatch in the differential paths. Therefore, it is important for the layout to be fully symmetric to maximize the differential signal paths matching. Any mismatch or non-symmetry may result in large offsets to the circuit performance. The symmetry of the layout also helps in rejecting the common noise picked up by the circuit from other devices located on the same chip. In addition, the symmetry must be applied to both the devices of interest and their surrounding environment.

During the layout design, the RF input transistors are surrounded by a P+ guard ring to reduce the equivalent substrate resistance and to lower noise injection to the substrate. Dummy diffusions and fingers are placed where applicable to achieve predictable and matched device performance. To improve the RF-port to LO-port isolation, the separation between the RF and the LO sections of the mixer is maximized.

Undesired threshold voltage modulation due to the body effect is one of the factors affecting the linearity characteristics of MOS transistors. It can be eliminated by shorting the source and the bulk of the transistors and surrounding each transistor with sufficient bulk contacts shorted to the source. A similar approach may be used to eliminate the body effect of the P-channel MOS transistor.

- Reference distribution

The reference distribution is a hot issue not even in the analog/RF circuit layout but also in the digital circuit layout. The supply voltage is low, thus a small voltage fluctuation can affect significantly the circuit performance. In the layout, supply and ground rings are kept wide, not only to account for current density, but also to minimize the voltage gradient throughout the chip. The substrate is covered with the lowest layer of metal as a ground plane where possible, to shield it from the noise coming from the high frequency interconnects and pads.

- ESD protection

During the chip layout, the electrostatic discharge (ESD) circuit for RF input and IF output of this mixer is only composed of diodes; this kind of ESD circuit is suitable for high-frequency circuits, and is enough for ESD protection during chip test.

- Passive components

In the given RF technology, there are eight different types of resistor and five of capacitors. Each one has its own pros/cons. For the best perfomance of the designed circuit, the MIM (metal-insulator-metal) capacitor is chosen. Regarding to the resistors, RP poly over isolation is employed, due to its high precision in comparison to other resistors of the PDK.

The most area consuming component is an inductor among passive components. The number and the size of inductors in the circuit normally indicate the size of full-chip. There are three different types of inductors (standard, symmetric, and symmetric with center tap) supported for the chosen CMOS technology. In this design, the standard inductor is chosen to meet our inductance value.

- Metal interconnections

The effect of interconnections is not considered in the circuit design, however it plays a crucial role in real circuit performance through the layout. The most troublesome phenomenon is the crosstalk. Two techniques are well known to reduce the crosstalk. The benefit of the differential signals sitting next each other is the first method. Next, the

shielding is popular to lower the crosstalk effect of signals. Also, a large number of contacts and vias are used to decrease the interconnect resistance.

4.4.3 Mixer Layout Core

The final layout design is shown in Fig. 4.22. As can be seen in the layout, it was implemented the most symmetrical as possible. The total core size of the proposed circuit excluding pad spaces is 0.38 mm^2. Fig. 4.23 shows the microphotograph of the fabricated chip, with the first topology of the downconversion mixer. The fabricated chip area including the pads is 6.25 mm^2.

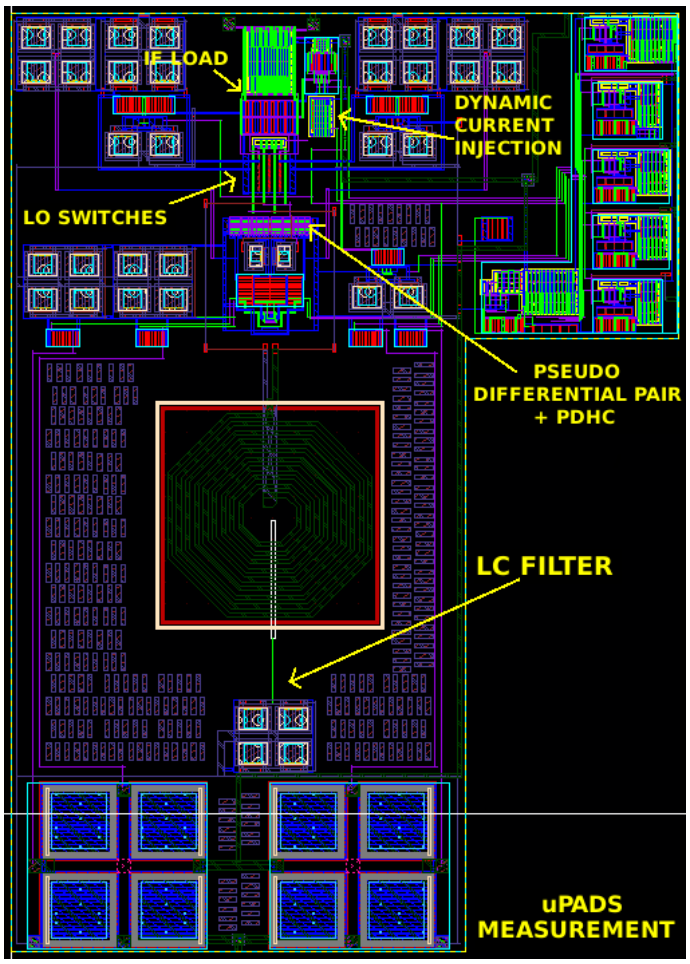


Figure 4.22: Layout of the proposed Downconversion mixer (First Topology)

4.5 Assessment with Respect to the State of the Art

Table 4.17 contains summaries of specifications reported for CMOS downconversion mixers with similar operating frequencies, we listed the ones who present simulation, measurement results and other features (subthreshold design, with IIP_2 enhancement circuitry, etc), the first topology is compared to 1, 3, 4, 5, 6, 8, 10 and the second topology to 2, 7, 9. It must be take into account that only simulations results from the two proposed topologies were available to compare to the listed mixer implementations.

The first topology has the lower power consumption and a comparable gain of 10 dB to the other implementations. The mixers in 3, 8 and 10 presents a higher IIP_3, IIP_2 or

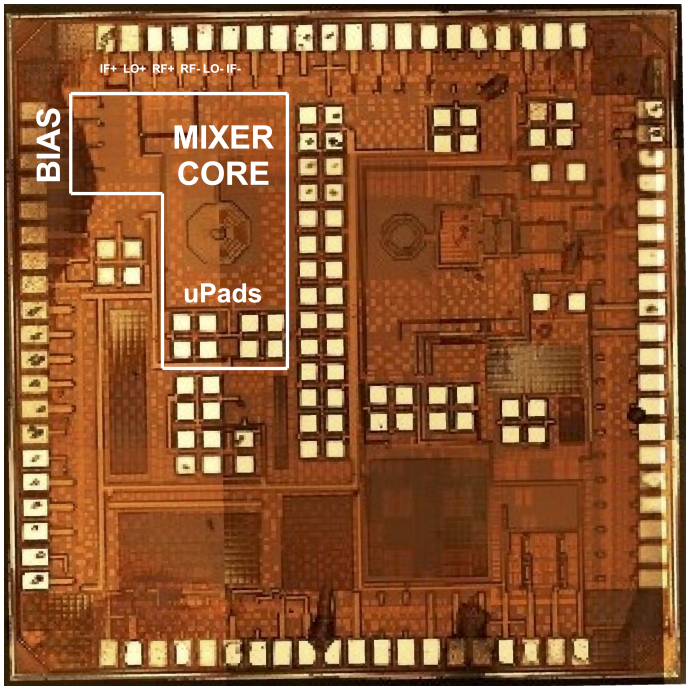


Figure 4.23: Microphotograph of fabricated chip including the proposed Downconversion mixer (highlighted) and other designs by 7 graduate students from UFRGS.

both than the first topology at the cost of higher consumption and additional calibration circuitry. Regarding the noise figure specification, the mixer of the first topology presents the lowest value in comparison to the other implementations. The first topology has lower IIP_2 than other mixers; however, most of the mixers contain auxiliary circuitry for IIP_2 enhancements (4, 5, 6, 10). Notice that they exhibit overall comparable performances but consume more power. In general, the first topology has competitive performance with significantly lower power dissipation in the same range as other reported mixers implementations.

The second topology moderate power consumption and a comparable gain of 13.6 dB to the other implementations. In 7, the mixer presents a lower consumption, high gain and a reasonable noise for the frequency range of operation, but its linearity performarce is meager. The mixer in 2 shows comparable performances to the second topology. In 9, the mixer presents a better gain and noise for the same frequency range, but with a higher consumption and lower IIP_3. In overall, the second topology presents a competitive performance with reasonable power dissipation for the same range as other reported mixers.

4.6 Concluding Remarks

A methodology for design Gilbert-cell mixers is introduced based on constraint design and the $\frac{g_m}{I_D}$ method for transistor sizing. This methodology is employed to design the two topologies of downconversion mixer proposed in chapter 3. Both designs comply with the best trade-off between the key specifications of the mixer.

In order to have a better insight of the feedthrough and IIP_2 during the design, the mismatches of the switching transistors and load resistors must be considered. Ultimately, Monte Carlo simulations should be performed to verify the Feedthrough and IIP_2. The

Table 4.17: Downconversion Mixer Performance Comparison

Reference	This Work*		1	2†	3Δ†	4Δ*	5Δ*	6Δ†	7#†	8	9†	10*
CMOS technology (nm)	130		180	90	180	65	180	130	130	180	130	180
RF Freq. (GHz)	2	1 $\longleftrightarrow$ 6	2.4	2.1	2.1	2.1	3.5	2	3.1 $\longleftrightarrow$ 10.6	2.4	1 $\longleftrightarrow$ 5.5	2.1
IF Freq. (MHz)	<100			<1.2	<4.5	<10	-	<1.5	264		-	
Conversion gain (dB)	10.2	13.9 $\longleftrightarrow$ 11	16.5	9	16	12	10	53	9.8 $\longleftrightarrow$ 14.0	11	17.5 (Power)	15
Noise Meas. or DSB NF (dB)	12	8.5 $\longleftrightarrow$ 11	14.2	9.4	$4\ nV/\sqrt{Hz}^{\oplus}$	16	$4.5\ nV/\sqrt{Hz}^{\oplus}$	$3.5\ nV/\sqrt{Hz}^{\oplus}$	14.5 $\longleftrightarrow$ 19.6	13.8	3.9 (Average)	14
Linearization Technique	Post-distortion Harmonic Cancellation		MGTR (DS)		RC Degeneration	Calibration of IM_2	Digitally Enhanced IIP_2	Digitally Adaptative IIP_2 Calibration		Derivative Superposition (DS)		IM_2 Injection
IIP_3 (dBm)	10.9	4.4 $\longleftrightarrow$ 0.6	9	8.9	9	7	8	12	-11	15	0.84	15
1-dB Comp. Point (dBm)	-1.8	-9.8 $\longleftrightarrow$ -6.7		-	-	-	-	4	-24 -19		-10.5	
IIP_2 (dBm)	55	64 $\longleftrightarrow$ 72	-	> 55.1	> 78	> 75	> 65	~85	-	-	-	93
Supply (V)	1.2		1.8	1	1.8	1	1.8	1.5	1.2	2	1.5	1.8
Power (mW)	5.3	19.3	5.4	6.25^{θ}	7.2	6	-	72	1.85	14.8	34.5	8
Area (mm^2)	0.38	-	0.96	0.4	1.2	-	-	2	0.34	0.052	0.315	-

* Simulation resuslts; † Measurement results; # Subthreshold design; Δ With IIP_2 enhancement circuitry; θ Reported with LO buffer; $\oplus$Reported as input referred noise

[1]: KIM; KIM; LEE (2004)
[2]: PENG; CHEN; BELLAOUAR (2005)
[3]: BRANDOLINI et al. (2006)
[4]: VAHIDFAR; SHOAEI (2008)
[5]: RODRIGUEZ et al. (2008)
[6]: DUFRENE; BOOS; WEIGEL (2008)
[7]: SEO et al. (2008)
[8]: LIANG et al. (2008)
[9]: HO; SAAVEDRA (2010)
[10]: MOLLAALIPOUR; NAIMI (2012)

operation region of the switching transistors (M_{LO}) has an impact on the switching gain A_{SW} and noise as well.

Regarding the first topology some remarks were indicated. The operation region of the transistors in the transconductance stage is a key point in the design, a trade-off between linearity and noise must be take into account. The L-C filter of the first topology, limits the IIP_2 enhancement to narrow frequency range. A compromise between the steer current (dynamic current bleeding circuit) and the current of the switching transistors must be comply to improve the effectiveness of the noise reduction technique, DARABI; CHIU (2005). The reduction of the third-order intermodulation product in the PDHC technique is achieved when the main and auxiliary transistors of the transconductance stage operate in strong and weak inversion, respectively. The efficiency of this technique is reduced because the main transistors are chosen to operate in the moderate inversion.

Regarding the second topology some remarks were indicated. The transistors of the noise-canceling transconductors are sized to have the best trade-off between noise and power consumption. There was no need for a current bleeding in the switching transistor pairs, since the current passing through them is smaller compared it to the first topology. The peaking inductor (L_{peak}) is chosen to improve bandwidth of the second topology.

5 TEST AND MEASUREMENT CONFIGURATION

5.1 Mixer Configuration

In order to test and measure the downconversion mixer circuit (First Topology) previously described, designed and sent to fabrication, a PCB is being designed. As the circuit is going to be packaged, there will be additional parasitic effects due to the package itself. Figure 5.1 shows the mixer configuration for test and measurement. Since our mixer is fully differential (input and output), a passive balun is used before the differential (RF and LO) input ports to generate the differential input signals. As indicated in Fig. 5.1, an external buffer is employed to convert the differential output signal on-chip to a single-ended impedance matched signal off-chip, MAXIM (1999). Additionally the fabricated mixer has a bias and voltage supply section, that will be incorporated to the PCB. All off-chip losses will be calibrated at the operation frequency and de-embedded in the final measurement results.

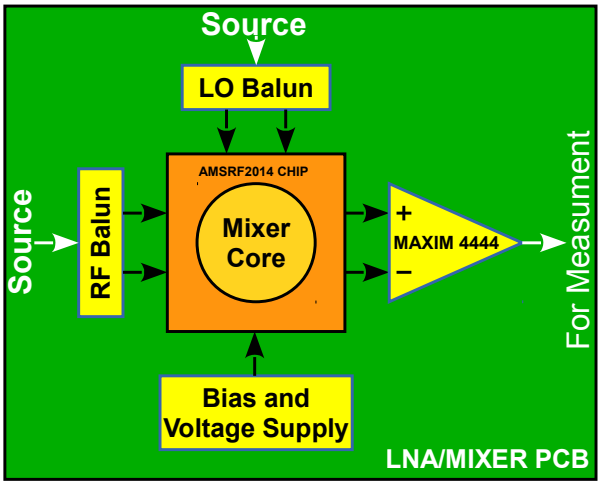


Figure 5.1: Mixer configuration for test and measurement

5.2 PCB Design

The fabricated chip includes multiple circuits (of 7 Master Students). This PCB was designed for the test and measurement of the RF circuits, an LNA and this mixer. The PCB was designed using the software Agilent Advanced Design Systems (ADS) in order to be able to simulate S-parameters. According to this simulation results, the designer is able to estimate coupling between traces, which is important in RF design. The designed

PCB is shown in Figs. 5.2 and 5.3. The PCB was designed with double ground plane (top and bottom layers).

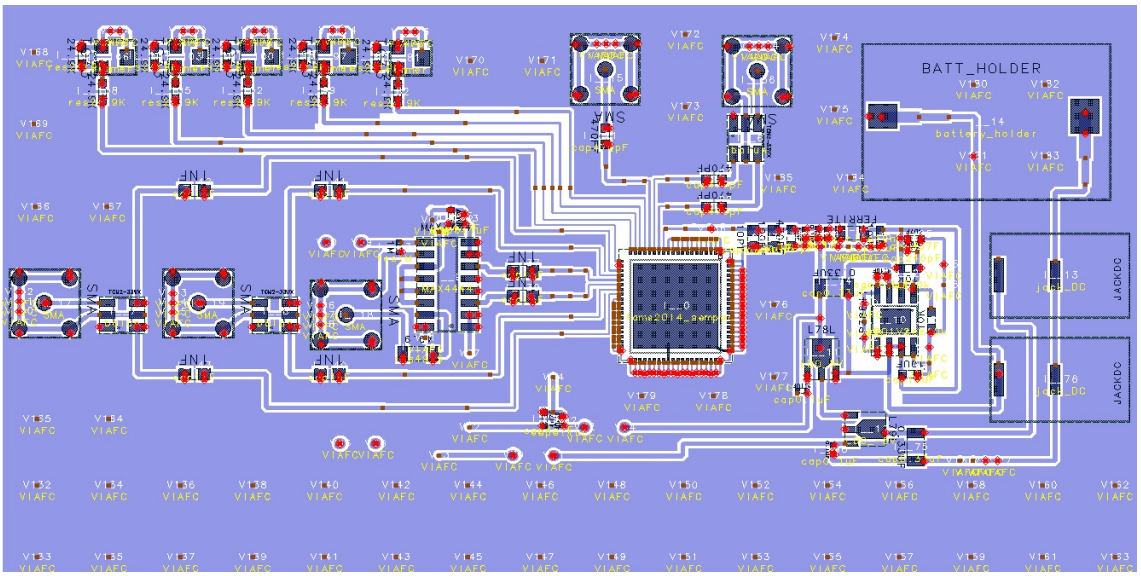


Figure 5.2: Designed PCB in ADS (top layer view).

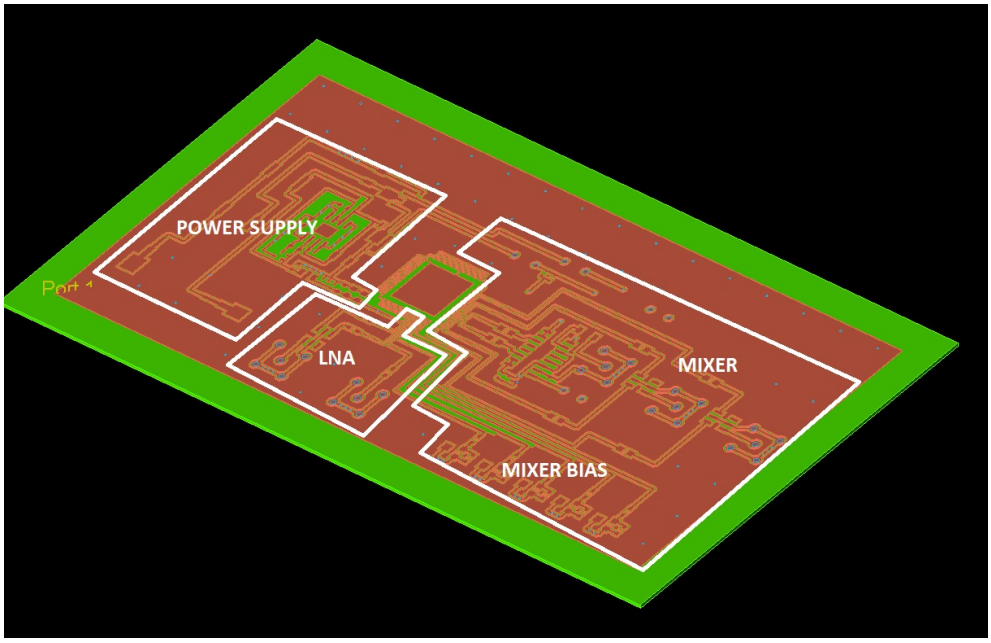


Figure 5.3: 3D view of the designed PCB.

5.3 Test-bench Configuration for Measurements

In this section, all test-benches and measurements details are shown. To characterize the designed mixer the following measurements are planned to be performed: gain, feedthrough between the ports, noise, and linearity.

5.3.1 Gain and Isolation

To characterize the conversion conversion gain as a function of either frequency or amplitude, the mixer should be connected to the Network Analyzer/Vector Network Analyzer for measurements. Depending on the availability of equipments, a 4-port Vector Network Analyzer should be sufficient, since it has two internal generators allowing the simultaneous feed of both the RF and LO signals. If a 4-port VNA is not available, then a 2-port VNA and an external RF signal generator can be used, as indicated below, Fig. 5.4.

Isolation is a measure of the circuit balance within the mixer. When the isolation is high, the amount of "leakage" or "feed through" between the mixer ports will be very small. Typically, mixer isolation falls off with frequency. The same test-bench could also be used to measure feedthrough between ports.

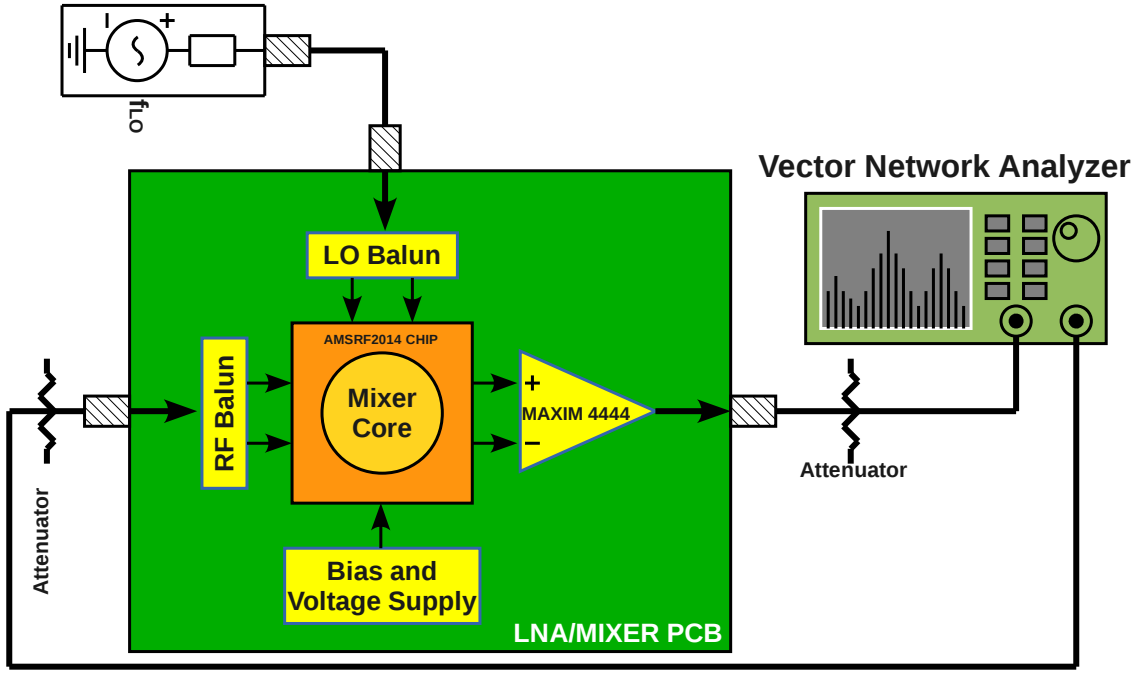


Figure 5.4: Gain Conversion, Feedthrough test-bench

5.3.2 Noise Figure

Measurement methods vary for different applications. As shown in the table above, some applications have high gain and low noise figure (Low Noise Amplifiers), some have low gain and high noise figure (mixers), some have very high gain and wide range of noise figure (receiver systems). Measurement methods have to be chosen carefully. The noise figure analyzer as well as two other popular methods - "gain method" and "Y factor method" - will be discussed.

5.3.2.1 Noise Figure Meter/Analyzer

The noise figure meter/analyzer is shown in Fig. 5.5. The noise figure analyzer generates a pulse signal to drive a noise source, which generates noise to drive the device under test (DUT). The output of the DUT is then measured by the noise figure analyzer. Since the input noise and Signal-to-Noise ratio of the noise source is known to the analyzer, the

noise figure of the DUT can be calculated internally and displayed. For certain applications (mixers and receivers), a LO signal might be needed, as shown in Fig. 5.5. Also, certain parameters need to be set up in the Noise Figure Analyzer before the measurement, such as frequency range, application (Amplifier/Mixer), etc.

Using a noise figure analyzer is the most straightforward way to measure noise figure. In most cases it is also the most accurate. An engineer can measure the noise figure over a certain frequency range, and the analyzer can display the system gain together with the noise figure to help the measurement. A noise figure meter also has limitations. The analyzers have certain frequency limits. For example, the Agilent N8973A works from 10MHz to 3GHz. Also, when measuring high noise figures, e.g., noise figure exceeding 10dB, the result can be very inaccurate. This method requires very expensive equipment.

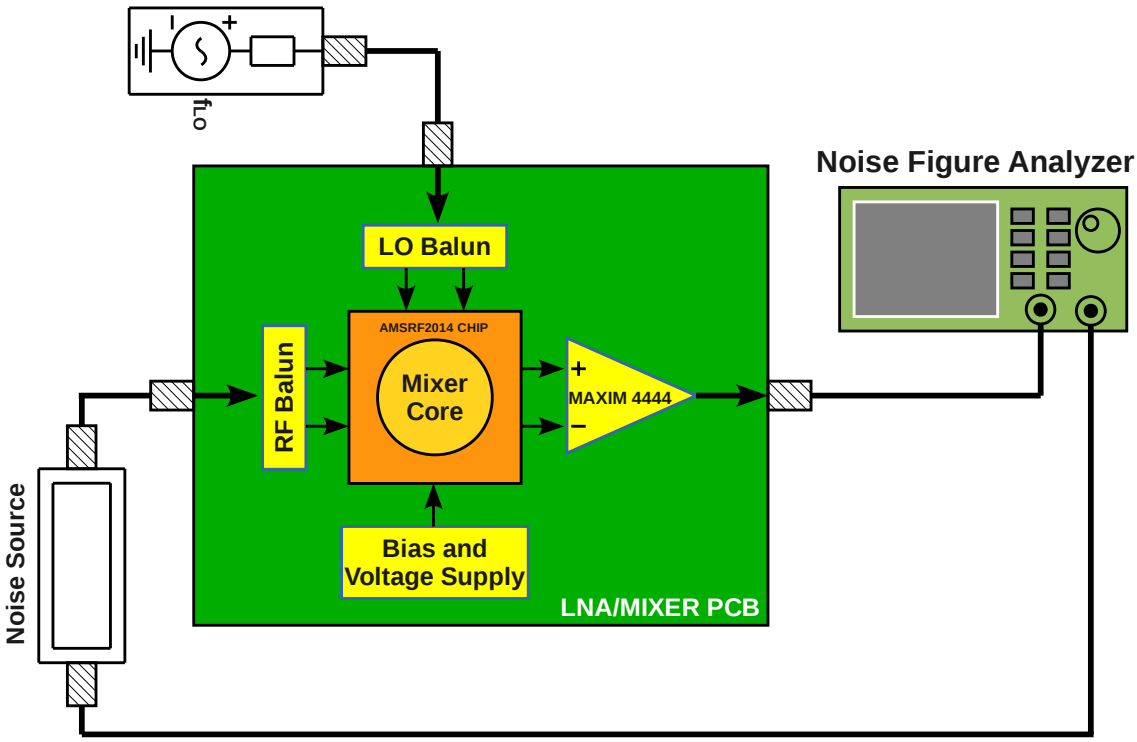


Figure 5.5: Noise Figure Analyzer test-bench

5.3.2.2 Gain Method

As mentioned above, there are other methods to measure noise figure besides directly using a noise figure meter. These methods involve more measurements as well as calculations, but under certain conditions, they turn out to be more convenient and more accurate. One popular method is called gain method, which is based on the noise factor definition given in Eq. 2.1:

$$Noise\,Factor = \frac{Total\,Output\,Noise\,Power}{Output\,Noise\,due\,to\,Input\,Source\,Only} \tag{5.1}$$

In this definition, noise is due to two effects. One is the interference that comes to the input of a RF system in the form of signals that differ from the desired one. The second is due to the random fluctuation of carriers in the RF system (LNA, mixer, receiver, etc).

The second effect is the result of Brownian motion, It applies in thermal equilibrium to any electronic device, and the available noise power from the device is:

$$P_{NA} = kT\Delta F \tag{5.2}$$

where k= Boltzmann's Constant ($1.38 \times 10^{-23} Joules/\Delta K$),
T= Temperature in Kelvin
ΔF = Noise Bandwith (Hz)
At room temperature (290ΔK), the noise power density P_{NAD}= -174dBm/Hz.
Thus we have the following equation:

$$\text{NF} = P_{NOUT} \text{ - (-174dBm/Hz + 10*log10(BW) + Gain)}$$

In the equation above, P_{NOUT} is the measured total output noise power. -174dBm/Hz is the noise density at 290K. BW is the bandwidth. Gain is the system gain. NF is the noise figure of the DUT. Everything in the equation is in log scale. To make the formula simpler, we can directly measure the output noise power density (P_{NOUTD} in dBm/Hz), and the equation becomes:

$$\text{NF} = P_{NOUTD} + 174\text{dBm/Hz - Gain}$$

To use the gain method to measure the noise figure, the gain of the DUT needs to be pre-determined. Then the input of the DUT is terminated with the characteristic impedance (50Ω for most RF applications, 75Ω for video/cable applications). Then the output noise power density is measured with a spectrum analyzer. The setup for the gain method is shown in Fig. 5.6.

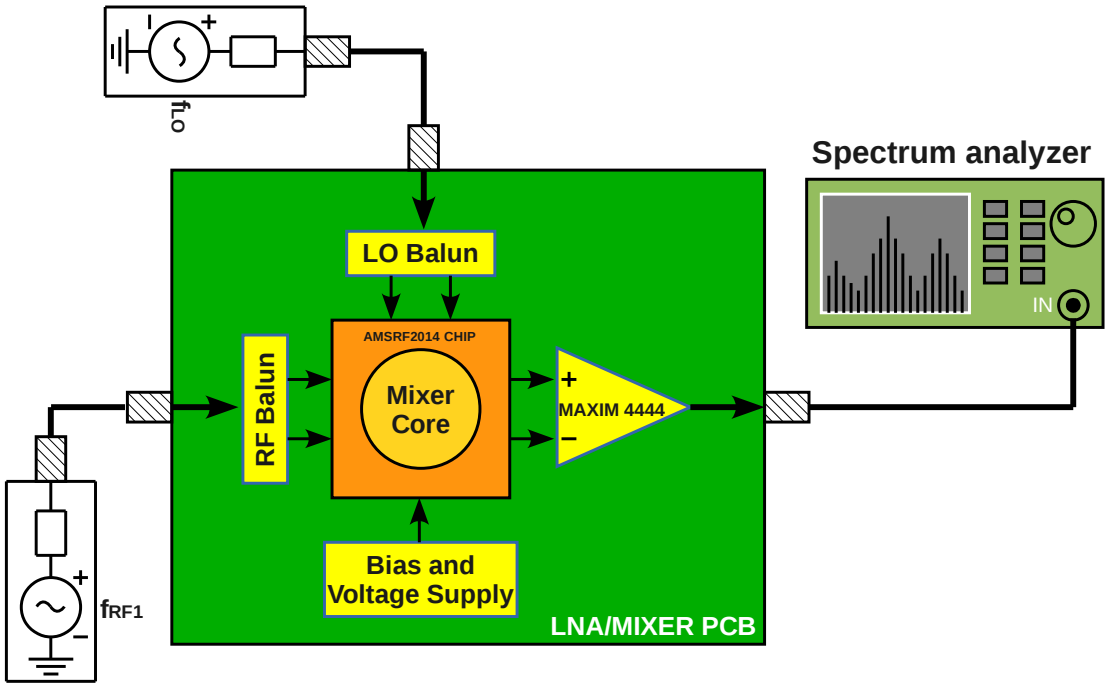


Figure 5.6: Gain method test-bench

The gain method can cover any frequency range, as long as the spectrum analyzer permits. The biggest limitation comes from the noise floor of the spectrum analyzer.

As shown in the equations, when Noise Figure is low (under 10 dB), (P_{NOUTD} - Gain) is close to -170dBm/Hz. Normal LNA gain is about 24dB. In that case, we need to measure a noise power density of -150dBm/Hz, which is lower than the noise floor of most spectrum analyzers.

5.3.2.3 Y Factor Method

The Y factor method is another popular way to measure the noise figure. To use the Y factor method, an ENR (Excess Noise Ratio) source is needed. It is the same thing as the noise source we mentioned earlier in the Noise Figure Analyzer section. The setup is shown in the Fig. 5.7. The ENR head usually requires a high DC voltage supply. Those ENR heads are very wide band and they have a standard noise figure parameter of their own at specified frequencies. Table 5.1 gives examples of ENR heads. The noise figures at frequencies between those markers are interpolated.

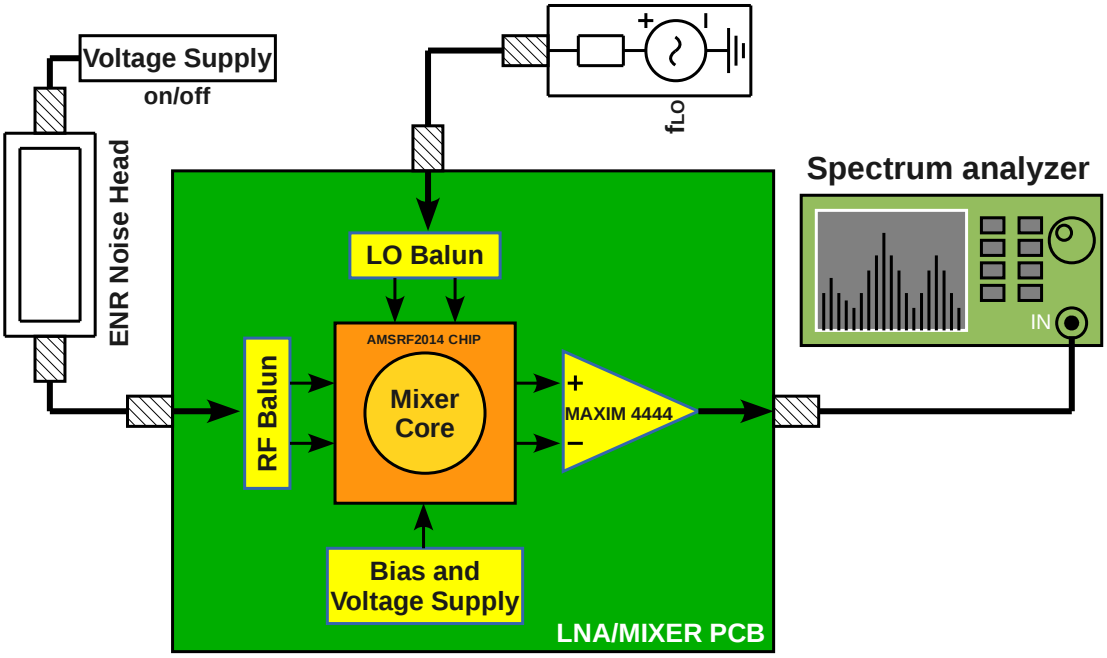


Figure 5.7: Y Factor method test-bench

Table 5.1: Example of ENR of Noise Heads

	HP346A	HP346B
Frequency (Hz)	NF (dB)	NF (dB)
1G	5.39	15.05
2G	5.28	15.01
3G	5.11	14.86
4G	5.07	14.82
5G	5.07	14.81

Turning the noise source on and off (by turning on and off the DC voltage), an engineer measures the change in the output noise power density with a spectrum analyzer. The

formula to calculate noise figure is:

$$Noise\,Figure(NF) = 10 * log_{10}\left(\frac{10^{ENR/10}}{10^{Y/10}-1}\right) \tag{5.3}$$

In which ENR is the number given in the table above. It is normally listed on the ENR heads. Y is the difference between the output noise power density when the noise source is on and off.

The equation comes from the following:

An ENR noise head provides a noise source at two noise temperatures: a hot T = T_H (when a DC voltage is applied) and a cold T = 290K. The definition of ENR of the noise head is

$$ENR = \frac{T_H - 290}{290} \tag{5.4}$$

The excess noise is achieved by biasing a noisy diode. Now consider the ratio power out from the DUT from applying the cold T =290K, followed by applying the hot T = T_H as inputs:

$$Y = \frac{G(T_H + T_{NOM})}{G(290 + T_{NOM})} = \frac{\frac{T_H + T_{NOM}}{290}}{1 + \frac{T_{NOM}}{290}} \tag{5.5}$$

In terms of Noise figure, $F = \frac{T_{NOM}}{290} + 1$, F is the noise factor. Solving equation 5.5:

$$Y = \frac{ENR}{F} + 1 \tag{5.6}$$

5.3.3 Linearity

The test-benches for IIP_3 and 1 dB compression point ($IP1dB$) are different, since to measure IIP_3 one needs two RF power sources. In this case, it will also be necessary to use an RF power combiner so as to sum both signals into one, which is fed into the PCB connector. For IIP_3 measurement, one has to increase the power of both signal sources equally until the intermodulation products show up within the band at the spectrum analyzer. When the intermodulation products are seen at the spectrum analyzer, the corresponding input power is the IIP_3. A slightly different approach goes for the 1 dB compression point, which has only one RF power source. One should increase the power of the signal source until the output power starts dropping relative to a linear increase. When it achieves a 1 dB drop, seen at the spectrum analyzer, the respective input power is the 1 dB compression point. Figs. 5.8 and 5.9 show the test benches.

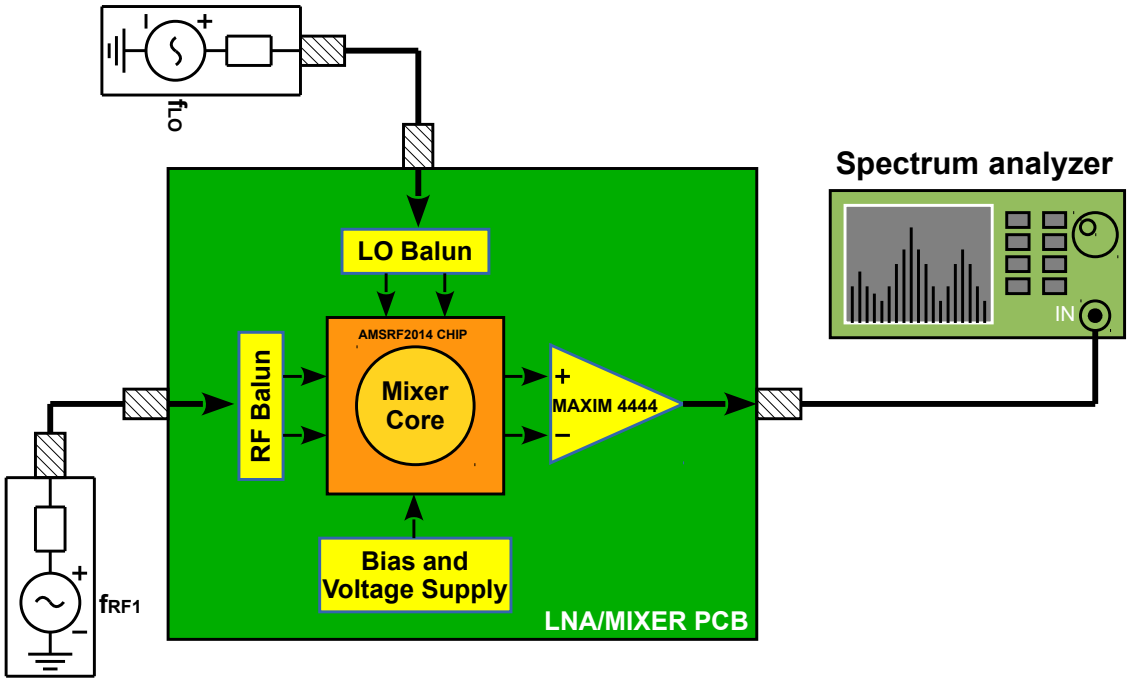


Figure 5.8: Input 1 dB compression point test-bench

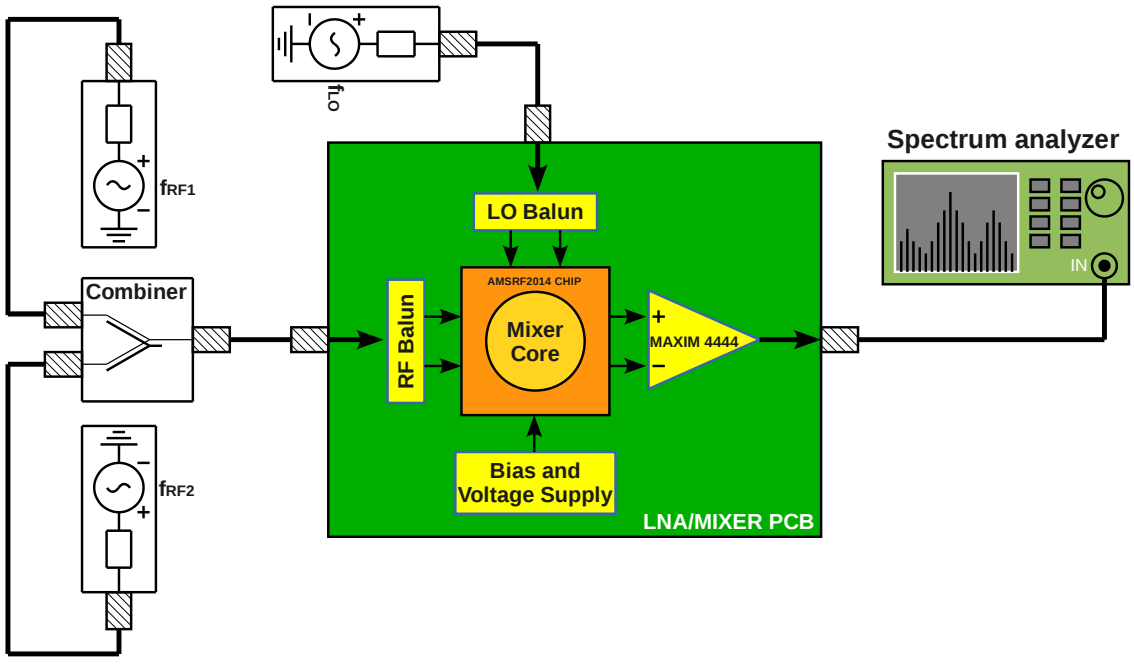


Figure 5.9: Two-tone test-becnh for Input Referred 3^{rd} Intercept Point

6 CONCLUSIONS

Through a concise revision on the state of the art on downconversion mixers, a new downconversion mixer which complies with multi-band and multi-standard operation is presented. Both, linearity and noise were the principal figures of merit for the proposed mixer. For linearity improvement, post-distortion harmonic cancellation (PDHC) was employed, and for noise reduction, dynamic current injection combined with an LC filter tuned at the LO frequency and thermal-noise cancellation were used.

Modeling the distortion of a circuit in a downconversion mixer, through a power series is only suitable for low frequencies, where the influence of the circuit reactances is small. At high frequencies it is no longer valid and modeling the distortion taking into account these reactances become critical for an accurate analysis. A circuit's distortion analysis through Volterra series can accurately model memory effects, which become critical at RF. A Volterra series analysis was performed to the proposed mixer to show the effectiveness of the post-distortion harmonic cancellation technique.

The combination of the $\frac{g_m}{I_D}$ methodology for RF circuits combined with the study previously mentioned makes possible to the designer discover an optimum operating point, on which to trim the mixer design. The added linearization circuitry does not increase the size of the mixer, nor does it degrade conversion gain, noise figure, or power consumption.

Electrical simulations were performed on post-layout level from the first topology and schematic level from the second topology, using an IBM 0.13 μm CMOS process to demonstrate the improvements on IIP_3 and IIP_2 in comparison to the conventional Gilbert-cell mixer.

For the first topology, we achieved a conversion gain of 10.2 dB with a NF of 12 dB for the designed mixer working at 2 GHz, with a low-IF of 500 kHz. And an IIP_2 and IIP_3 of 55 dBm and 10.9 dBm respectively, while consuming only 5.3 mW from a 1.2 V supply.

For the second topology, we achieved a conversion gain range of [13.8 ~11] dB, an input reflection coefficient (S_{11}) of [-18 ~-9.5] dB and a NF of [8.5 ~11] dB in the frequency range of 1 to 6 GHz. For the linearity specs, an IIP_3 of 0 dBm was achieved for the whole frequency range, while consuming 19.3 mW from a 1.2 V supply, making the second topology well suited for multi-band and multi-standard operation.

The linearity and noise requirements in multi-band multi-standard applications make the design of RF CMOS mixers a very challenging task. However, a proper definition of specifications at the receiver combined with linearization and noise reduction techniques enable circuits that complies with multi-band and multi-standard operation.

As future work, the test procedures discussed in chapter 5 will be carried out on the fabricated samples of topology 1 (2 GHz mixer). The second topology will be sent to fabrication in the future.

REFERENCES

ABIDI, A. CMOS wireless transceivers: the new wave. **Communications Magazine, IEEE**, [S.l.], v.37, n.8, p.119–124, Aug 1999.

APARIN, V.; PERSICO, C. Effect of out-of-band terminations on intermodulation distortion in common-emitter circuits. In: MICROWAVE SYMPOSIUM DIGEST, 1999 IEEE MTT-S INTERNATIONAL, 1999. **Proceedings...** [S.l.: s.n.], 1999. v.3, p.977–980 vol.3.

BAGHERI, R. et al. An 800-MHz ndash;6-GHz Software-Defined Wireless Receiver in 90-nm CMOS. **Solid-State Circuits, IEEE Journal of**, [S.l.], v.41, n.12, p.2860–2876, Dec 2006.

BEHZAD, A. **The implementation of high-speed experimental transceiver module with an emphasis on CDMA applications**. 1995. Dissertação (Mestrado em Ciência da Computação) — University of California, Berkeley.

BERNY, A.; NIKNEJAD, A.; MEYER, R. A 1.8-GHz LC VCO with 1.3-GHz tuning range and digital amplitude calibration. **Solid-State Circuits, IEEE Journal of**, [S.l.], v.40, n.4, p.909–917, April 2005.

BRANDOLINI, M. et al. A +78 dBm IIP2 CMOS direct downconversion mixer for fully integrated UMTS receivers. **Solid-State Circuits, IEEE Journal of**, [S.l.], v.41, n.3, p.552–559, March 2006.

BRANDOLINI, M.; SOSIO, M.; SVELTO, F. A 750 mV Fully Integrated Direct Conversion Receiver Front-End for GSM in 90-nm CMOS. **Solid-State Circuits, IEEE Journal of**, [S.l.], v.42, n.6, p.1310–1317, June 2007.

BRUCCOLERI, F.; KLUMPERINK, E.; NAUTA, B. Wide-band CMOS low-noise amplifier exploiting thermal noise canceling. **Solid-State Circuits, IEEE Journal of**, [S.l.], v.39, n.2, p.275–282, Feb 2004.

CAVERS, J.; LIAO, M. Adaptive compensation for imbalance and offset losses in direct conversion transceivers. **Vehicular Technology, IEEE Transactions on**, [S.l.], v.42, n.4, p.581–588, Nov 1993.

CHEN, W.; POOBUAPHEUN, N.; NIKNEJAD, A. **A Broadband High Dynamic Range CMOS Front-End**. [S.l.]: BWRC Summer Retreat, 2006.

CHOI, P. et al. An experimental coin-sized radio for extremely low power WPAN (IEEE802.15.4) application at 2.4GHz. In: SOLID-STATE CIRCUITS CONFERENCE, 2003. DIGEST OF TECHNICAL PAPERS. ISSCC. 2003 IEEE INTERNATIONAL, 2003. **Proceedings...** [S.l.: s.n.], 2003. p.92–480 vol.1.

CORDOVA, D.; BAMPI, S.; FABRIS, E. A CMOS down-conversion mixer with high IIP2 and IIP3 for multi-band and multiple standards. In: INTEGRATED CIRCUITS AND SYSTEMS DESIGN (SBCCI), 2014 27TH SYMPOSIUM ON, 2014. **Proceedings...** [S.l.: s.n.], 2014. p.1–7.

CORDOVA, D.; FABRIS, E.; CAMPANA, R. An efficient CMOS configurable Bias Current Generator with wide dynamic range. In: CIRCUITS AND SYSTEMS (LASCAS), 2013 IEEE FOURTH LATIN AMERICAN SYMPOSIUM ON, 2013. **Proceedings...** [S.l.: s.n.], 2013. p.1–4.

CORDOVA, D.; TOLEDO, P.; FABRIS, E. A low-voltage current reference with high immunity to EMI. In: INTEGRATED CIRCUITS AND SYSTEMS DESIGN (SBCCI), 2014 27TH SYMPOSIUM ON, 2014. **Proceedings...** [S.l.: s.n.], 2014. p.1–6.

CROLS, J.; STEYAERT, M. Low-IF topologies for high-performance analog front ends of fully integrated receivers. **Circuits and Systems II: Analog and Digital Signal Processing, IEEE Transactions on**, [S.l.], v.45, n.3, p.269–282, Mar 1998.

DA SILVA, P. D. et al. Design-oriented model for nonlinearities in MOSFETs. In: CIRCUITS AND SYSTEMS AND TAISA CONFERENCE, 2008. NEWCAS-TAISA 2008. 2008 JOINT 6TH INTERNATIONAL IEEE NORTHEAST WORKSHOP ON, 2008. **Proceedings...** [S.l.: s.n.], 2008. p.153–156.

DARABI, H. A Blocker Filtering Technique for SAW-Less Wireless Receivers. **Solid-State Circuits, IEEE Journal of**, [S.l.], v.42, n.12, p.2766–2773, Dec 2007.

DARABI, H.; ABIDI, A. Noise in RF-CMOS mixers: a simple physical model. **Solid-State Circuits, IEEE Journal of**, [S.l.], v.35, n.1, p.15–25, Jan 2000.

DARABI, H.; CHIU, J. A noise cancellation technique in active RF-CMOS mixers. **Solid-State Circuits, IEEE Journal of**, [S.l.], v.40, n.12, p.2628–2632, Dec 2005.

DUFRENE, K.; BOOS, Z.; WEIGEL, R. Digital Adaptive IIP2 Calibration Scheme for CMOS Downconversion Mixers. **Solid-State Circuits, IEEE Journal of**, [S.l.], v.43, n.11, p.2434–2445, Nov 2008.

ELLIS, T. A modified feed-forward technique for mixer linearization. In: MICROWAVE SYMPOSIUM DIGEST, 1998 IEEE MTT-S INTERNATIONAL, 1998. **Proceedings...** [S.l.: s.n.], 1998. v.3, p.1423–1426 vol.3.

ERDOGAN, O. et al. A single-chip quad-band GSM/GPRS transceiver in 0.18 mu;m standard CMOS. In: SOLID-STATE CIRCUITS CONFERENCE, 2005. DIGEST OF TECHNICAL PAPERS. ISSCC. 2005 IEEE INTERNATIONAL, 2005. **Proceedings...** [S.l.: s.n.], 2005. p.318–601 Vol. 1.

ETSI. **Global System for Mobile Communications**. 1996.

FIORELLI, R. et al. 2.4-GHz single-ended input low-power low-voltage active front-end for ZigBee applications in 90 nm CMOS. In: CIRCUIT THEORY AND DESIGN (ECCTD), 2011 20TH EUROPEAN CONFERENCE ON, 2011. **Proceedings...** [S.l.: s.n.], 2011. p.829–832.

FIORELLI, R.; SILVEIRA, F.; PERALIAS, E. MOST Moderate-Weak-Inversion Region as the Optimum Design Zone for CMOS 2.4-GHz CS-LNAs. **Microwave Theory and Techniques, IEEE Transactions on**, [S.l.], v.62, n.3, p.556–566, March 2014.

GILBERT, B. A precise four-quadrant multiplier with subnanosecond response. **Solid-State Circuits, IEEE Journal of**, [S.l.], v.3, n.4, p.365–373, Dec 1968.

GRAY, P. R. et al. **Analysis and Design of Analog Integrated Circuits**. 4th.ed. New York: Wiley, 2001.

HO, S.; SAAVEDRA, C. A CMOS Broadband Low-Noise Mixer With Noise Cancellation. **Microwave Theory and Techniques, IEEE Transactions on**, [S.l.], v.58, n.5, p.1126–1132, May 2010.

HULL, C.; CHU, R.; LEONG THAM, J. A direct-conversion receiver for 900 MHz (ISM band) spread-spectrum digital cordless telephone. In: SOLID-STATE CIRCUITS CONFERENCE, 1996. DIGEST OF TECHNICAL PAPERS. 42ND ISSCC., 1996 IEEE INTERNATIONAL, 1996. **Proceedings...** [S.l.: s.n.], 1996. p.344–345.

JOHNS, D.; MARTIN, K. **Analog Integrated Circuit Design**. [S.l.]: Wiley, 1997.

KIM, B.; KO, J.-S.; LEE, K. A new linearization technique for MOSFET RF amplifier using multiple gated transistors. **Microwave and Guided Wave Letters, IEEE**, [S.l.], v.10, n.9, p.371–373, Sep 2000.

KIM, B.; KO, J.-S.; LEE, K. Highly linear CMOS RF MMIC amplifier using multiple gated transistors and its Volterra series analysis. In: MICROWAVE SYMPOSIUM DIGEST, 2001 IEEE MTT-S INTERNATIONAL, 2001. **Proceedings...** [S.l.: s.n.], 2001. v.1, p.515–518 vol.1.

KIM, T.-S.; KIM, B.-S. Linearization of differential CMOS low noise amplifier using cross-coupled post distortion canceller. In: RADIO FREQUENCY INTEGRATED CIRCUITS SYMPOSIUM, 2008. RFIC 2008. IEEE, 2008. **Proceedings...** [S.l.: s.n.], 2008. p.83–86.

KIM, T. W.; KIM, B.; LEE, K. Highly linear receiver front-end adopting MOSFET transconductance linearization by multiple gated transistors. **Solid-State Circuits, IEEE Journal of**, [S.l.], v.39, n.1, p.223–229, Jan 2004.

KIVEKAS, K. et al. Design of low-voltage active mixer for direct conversion receivers. In: CIRCUITS AND SYSTEMS, 2001. ISCAS 2001. THE 2001 IEEE INTERNATIONAL SYMPOSIUM ON, 2001. **Proceedings...** [S.l.: s.n.], 2001. v.4, p.382–385 vol. 4.

KIVEKAS, K.; PARSSINEN, A.; HALONEN, K. A. I. Characterization of IIP2 and DC-offsets in transconductance mixers. **Circuits and Systems II: Analog and Digital Signal Processing, IEEE Transactions on**, [S.l.], v.48, n.11, p.1028–1038, Nov 2001.

KWON, I.; LEE, K. An integrated low power highly linear 2.4-GHz CMOS receiver front-end based on current amplification and mixing. **Microwave and Wireless Components Letters, IEEE**, [S.l.], v.15, n.1, p.36–38, Jan 2005.

LEE, S.-G.; CHOI, J.-K. Current-reuse bleeding mixer. **Electronics Letters**, [S.l.], v.36, n.8, p.696–697, Apr 2000.

LEE, T. **The Design of CMOS Radio-Frequency Integrated Circuits**. Cambridge, UK: Cambridge University Press, 1998.

LIANG, K.-H. et al. A New Linearization Technique for CMOS RF Mixer Using Third-Order Transconductance Cancellation. **Microwave and Wireless Components Letters, IEEE**, [S.l.], v.18, n.5, p.350–352, May 2008.

LIMKETKAI, B. **The Design and Implementation of A Downconversion Mixer For a wideband CDMA Receiver**. 1999. Dissertação (Mestrado em Ciência da Computação) — University of California, Berkeley.

MAAS, S. A. **Nonlinear Microwave and RF Circuits**. Norwood, MA: Artech House, 2003. n.Second Edition.

MANKU, T. et al. A single chip direct conversion CMOS transceiver for quad-band GSM/GPRS/EDGE and WLAN with integrated VCO's and fractional-N synthesizer. In: RADIO FREQUENCY INTEGRATED CIRCUITS (RFIC) SYMPOSIUM, 2004. DIGEST OF PAPERS. 2004 IEEE, 2004. **Proceedings...** [S.l.: s.n.], 2004. p.423–426.

MANSTRETTA, D.; BRANDOLINI, M.; SVELTO, F. Second-order intermodulation mechanisms in CMOS downconverters. **Solid-State Circuits, IEEE Journal of**, [S.l.], v.38, n.3, p.394–406, Mar 2003.

MARTIN, K. Complex signal processing is not complex. **Circuits and Systems I: Regular Papers, IEEE Transactions on**, [S.l.], v.51, n.9, p.1823–1836, Sept 2004.

MAXIM. **Ultra-High-Speed, Low-Distortion, Differential-to-Single-Ended Line Receivers with Enable**. 19-1543.ed. [S.l.]: Maxim Integrated Products, 1999.

MEHTA, S. et al. An 802.11g WLAN SoC. **Solid-State Circuits, IEEE Journal of**, [S.l.], v.40, n.12, p.2483–2491, Dec 2005.

MEYER, R. **Advanced Integrated Circuits for Communications**. [S.l.]: UC Berkeley, 2004. (EECS 242 Course Notes).

MEYER, R.; WONG, A. Blocking and desensitization in RF amplifiers. **Solid-State Circuits, IEEE Journal of**, [S.l.], v.30, n.8, p.944–946, Aug 1995.

MOLLAALIPOUR, M.; NAIMI, H. Volterra series analysis of down-conversion CMOS mixer with high IIP2 and IIP3. In: SYNTHESIS, MODELING, ANALYSIS AND SIMULATION METHODS AND APPLICATIONS TO CIRCUIT DESIGN (SMACD), 2012 INTERNATIONAL CONFERENCE ON, 2012. **Proceedings...** [S.l.: s.n.], 2012. p.201–204.

MOORE, G. Cramming More Components Onto Integrated Circuits. **Proceedings of the IEEE**, [S.l.], v.86, n.1, p.82–85, Jan 1998.

NGUYEN, C.-C. Vibrating RF MEMS for next generation wireless applications. In: CUSTOM INTEGRATED CIRCUITS CONFERENCE, 2004. PROCEEDINGS OF THE IEEE 2004, 2004. **Proceedings...** [S.l.: s.n.], 2004. p.257–264.

PENG, S.; CHEN, C.-C.; BELLAOUAR, A. A wide-band mixer for WCDMA/CDMA2000 in 90nm digital CMOS process. In: RADIO FREQUENCY INTEGRATED CIRCUITS (RFIC) SYMPOSIUM, 2005. DIGEST OF PAPERS. 2005 IEEE, 2005. **Proceedings...** [S.l.: s.n.], 2005. p.179–182.

PRETL, H. et al. A SiGe-bipolar down-conversion mixer for a UMTS zero-IF receiver. In: BIPOLAR/BICMOS CIRCUITS AND TECHNOLOGY MEETING, 2000. PROCEEDINGS OF THE 2000, 2000. **Proceedings...** [S.l.: s.n.], 2000. p.40–43.

RABAEY, J.; A.CHANDRAKASAN; NIKOLIC, B. **Digital Integrated Circuits**: a design perspective. 2nd.ed. New Jersey: Prentice-Hall, 2002.

RAZAVI, B. **RF microelectronics**. Upper Saddle River, New Jersey: Prentice-Hall, 1998.

RODRIGUEZ, S. et al. CMOS RF mixer with digitally enhanced IIP2. **Electronics Letters**, [S.l.], v.44, n.2, p.121–122, January 2008.

RUDELL, J. C. **Frequency translation techniques for high-integration high- selectivity multi-standard wireless communication systems**. 2000. Tese (Doutorado em Ciência da Computação) — University of California, Berkeley, Berkely, USA.

RUDELL, J. et al. A 1.9-GHz wide-band IF double conversion CMOS receiver for cordless telephone applications. **Solid-State Circuits, IEEE Journal of**, [S.l.], v.32, n.12, p.2071–2088, Dec 1997.

SEO, J.-B. et al. A Low-Power and High-Gain Mixer for UWB Systems. **Microwave and Wireless Components Letters, IEEE**, [S.l.], v.18, n.12, p.803–805, Dec 2008.

SILVEIRA, F.; FLANDRE, D.; JESPERS, P. G. A. A gm/IDbased methodology for the design of CMOS analog circuits and its application to the synthesis of a silicon-on-insulator micropower OTA. **Solid-State Circuits, IEEE Journal of**, [S.l.], v.31, n.9, p.1314–1319, Sep 1996.

SOORAPANTH, T.; LEE, T. H. RF linearity of short-channel MOSFETS. In: INT. WORKSHOP DESIGN MIXED-MODE INTEGR. CIRCUITS APPL., 1., 1997. **Proceedings...** [S.l.: s.n.], 1997. p.81–84.

STEYAERT, M. et al. A single-chip CMOS transceiver for DCS-1800 wireless communications. In: SOLID-STATE CIRCUITS CONFERENCE, 1998. DIGEST OF TECHNICAL PAPERS. 1998 IEEE INTERNATIONAL, 1998. **Proceedings...** [S.l.: s.n.], 1998. p.48–49.

TANG, C.-C. et al. A 2.4-GHz CMOS down-conversion doubly balanced mixer with low supply voltage. In: CIRCUITS AND SYSTEMS, 2001. ISCAS 2001. THE 2001 IEEE INTERNATIONAL SYMPOSIUM ON, 2001. **Proceedings...** [S.l.: s.n.], 2001. v.4, p.794–797 vol. 4.

TERROVITIS, M.; MEYER, R. Noise in current-commutating CMOS mixers. **Solid-State Circuits, IEEE Journal of**, [S.l.], v.34, n.6, p.772–783, Jun 1999.

TERROVITIS, M.; MEYER, R. Intermodulation distortion in current-commutating CMOS mixers. **Solid-State Circuits, IEEE Journal of**, [S.l.], v.35, n.10, p.1461–1473, Oct 2000.

TOLEDO, P. et al. Self-biased CMOS current reference based on the ZTC operation condition. In: INTEGRATED CIRCUITS AND SYSTEMS DESIGN (SBCCI), 2014 27TH SYMPOSIUM ON, 2014. **Proceedings...** [S.l.: s.n.], 2014. p.1–7.

VAHIDFAR, M.; SHOAEI, O. A High IIP2 Mixer Enhanced by a New Calibration Technique for Zero-IF Receivers. **Circuits and Systems II: Express Briefs, IEEE Transactions on**, [S.l.], v.55, n.3, p.219–223, March 2008.

VIDOJKOVIC, V. et al. A high gain, low voltage folded-switching mixer with current-reuse in 0.18 mu;m CMOS. In: RADIO FREQUENCY INTEGRATED CIRCUITS (RFIC) SYMPOSIUM, 2004. DIGEST OF PAPERS. 2004 IEEE, 2004. **Proceedings...** [S.l.: s.n.], 2004. p.31–34.

VIDOJKOVIC, V. et al. A low-voltage folded-switching mixer in 0.18- mu;m CMOS. **Solid-State Circuits, IEEE Journal of**, [S.l.], v.40, n.6, p.1259–1264, June 2005.

WELDON, J. et al. A 1.75-GHz highly integrated narrow-band CMOS transmitter with harmonic-rejection mixers. **Solid-State Circuits, IEEE Journal of**, [S.l.], v.36, n.12, p.2003–2015, Dec 2001.

YEE, D. et al. A 2-GHz low-power single-chip CMOS receiver for WCDMA applications. In: SOLID-STATE CIRCUITS CONFERENCE, 2000. ESSCIRC '00. PROCEEDINGS OF THE 26RD EUROPEAN, 2000. **Proceedings...** [S.l.: s.n.], 2000. p.57–60.

ZARGARI, M. et al. A single-chip dual-band tri-mode CMOS transceiver for IEEE 802.11a/b/g WLAN. In: SOLID-STATE CIRCUITS CONFERENCE, 2004. DIGEST OF TECHNICAL PAPERS. ISSCC. 2004 IEEE INTERNATIONAL, 2004. **Proceedings...** [S.l.: s.n.], 2004. p.96–515 Vol.1.

ZHANG, H.; SANCHEZ-SINENCIO, E. Linearization Techniques for CMOS Low Noise Amplifiers: a tutorial. **Circuits and Systems I: Regular Papers, IEEE Transactions on**, [S.l.], v.58, n.1, p.22–36, Jan 2011.

LIST OF PUBLICATIONS

Prior to defining the Mixer theme for this Master Thesis, the author worked on current references design, developing a bias current generator covering the range of 62.5 nA to $16\mu A$ with high accuracy and a self-biased current reference based on the MOSFET Zero Temperature Coefficient (ZTC) condition. Also, a new current reference topology with high immunity to Electromagnectic Interference (EMI) was designed. The main features of this circuit is its high PSRR and temperature compensation. These circuits generated 3 publications (LASCAS2013, SBCCI2014). The publications are listed in the references CORDOVA; FABRIS; CAMPANA (2013), CORDOVA; TOLEDO; FABRIS (2014) and TOLEDO et al. (2014) and repeated below for convenience.

The publication regarding the Mixer design appeared at the SBCCI 2014 Symposium is listed below, CORDOVA; BAMPI; FABRIS (2014).

1. Cordova, D., Fabris, E., Campana, S., “An efficient CMOS Configurable Bias Current Generator with Wide Dynamic Range”, IEEE Fourth Latin American Symposium on Circuits and Systems (LASCAS), 2013;
2. Cordova, D., Toledo, P., Fabris, E., “A Low-Voltage Current Reference with High Immunity to EMI”, 27th Symposium on Integrated Circuits and Systems Design (SBCCI), 2014;
3. Toledo, P., Klimach, H., Cordova, D., Bampi, S., Fabris, E., “Self-Biased CMOS Current Reference Based on the ZTC Operation Condition”, 27th Symposium on Integrated Circuits and Systems Design (SBCCI), 2014;
4. Cordova, D., Bampi, S., Fabris, E., “A CMOS Down-Conversion Mixer with High IIP2 and IIP3 for Multi-Band and Multiple Standards”, 27th Symposium on Integrated Circuits and Systems Design (SBCCI), 2014;

APPENDIX A SUMMARY IN PORTUGUESE

MISTURADOR ATIVO CMOS PARA CONVERSÃO A BAIXAS FREQUÊNCIAS COM OPERAÇÃO MULTI-BANDA E MULTI-PROTOCOLO

A.1 INTRODUÇÃO

Produtos de comunicações sem fio continuam possibilitando múltiplos protocolos de comunicações, exigindo que projetistas desenvolvam circuitos e sistemas que funcionem em tantas faixas de frequência e protocolos quantas possível. Por essa razão, é necessário o desenvolvimento de componentes —tais como receptores de banda larga —que possam operar com diversos padrões sem fio em várias faixas de operação. Receptores de conversão direta (DCR) são uma opção atraente devido ao seu alto nível de integração, baixo custo e circuitos de banda base reconfiguráveis mais simples em comparação com outros tipos de receptores.

No entanto, este tipo de receptor sofre de vários problemas desafiadores, incluindo os produtos de intermodulação de segunda e terceira ordem (IM_2, IM_3). Vamos nos concentrar no misturador para conversão a baixas frequências, como o principal responsável pela geração IM_2 e IM_3 em um receptor de conversão direta TERROVITIS; MEYER (2000). Para a linearidade de um misturador, sem sacrificar os outros parâmetros-chave de desempenho do mesmo, é necessário aplicar algumas técnicas de linearização. Inúmeras técnicas de linearização foram desenvolvidos para amplificadores de baixo ruído (LNAs). Um método frequentemene utilizado é a técnica de superposição da derivada KIM; KIM; LEE (2004), LIANG et al. (2008). Esta técnica utiliza transistores auxiliares polarizados em inversão fraca, o que produz uma corrente não-linear para cancelar a intermodulação de terceira ordem gerada pelos transistores principais. Esta abordagem é eficaz principalmente em frequências mais baixas e pode induzir ruído adicional de portã. Recentemente, uma técnica de cancelamento de harmônicos com pós-distorção (PDHC) e uma técnica de acoplamento cruzado PHDC foram implementadas para linearização de LNA, ZHANG; SANCHEZ-SINENCIO (2011), KIM; KIM (2008). Ambos métodos possibilitaram níveis de IIP_3 superiores a 10 dBm sem degradar seriamente os outros parâmetros-chave LNA.

Em DCR, um misturador baseado na célula de Gilbert tem sido amplamente utilizado em CMOS devido ao seu alto isolamento entre RF e oscilador local (LO) GILBERT (1968). No entanto, a elevada figura de ruído (NF) da célula de Gilbert degradará todo o desempenho do receptor, consequentemente exigindo um LNA de alto ganho e baixo ruído para aliviar a NF do receptor inteiro. Isso pode ser resolvido se a NF dos misturadores fot suficientemente baixa HO; SAAVEDRA (2010). Para reduzir o ruído do estágio de transcondutância do misturador, a técnica de cancelamento de ruído usada em LNAs pode ser também aplicada conforme BRUCCOLERI; KLUMPERINK; NAUTA (2004).

Um misturador para conversão a baixas frequências baseado na topologia da célula de Gilbert que usa cancelamento de ruído e aprimoramento na linearidade é o principal desafio desta dissertação, que desenvolve um misturador de faixa larga, de baixo ruído e alta linearidade que cumpra operação multi-banda e multi-protocolo.

A dissertação está organizada da seguinte forma:

O capítulo 2 fornece uma revisão de receptores sem fio para operação multi-banda e multi-protocolo. Começando com arquitetura de receptores, caracterização do desempenho e, finalmente, discutindo os efeitos da distorção em receptores sem fio.

O Capítulo 3 analisa o misturador baseado na célula de Gilbert e faz a caracterização de seu desempenho e propõe possíveis melhorias. Uma análise de Volterra completa do desempenho em linearidade da célula de Gilbert. Uma revisão concisa da literatura de trabalhos anteriores sobre misturadores ativos para receptores multi-banda. As duas topologias propostas de misturador para conversão a baixas frequências são apresentadas.

O desempenho de linearidade utilizando séries de Volterra e a contribuição de ruído da primeira topologia são descritos.

O Capítulo 4 apresenta uma metodologia de projeto de um misturador tipo célula de Gilbert. As especificações principais são caracterizadas em função da eficiência da corrente de dreno ($\frac{g_m}{I_D}$) e os parâmetros do circuito. Usando esta metodologia os misturadores propostos são projetados e avaliados através de simulações e finalmente, uma avaliação dos misturadores projetados é feita em comparação com o estado da arte.

O capítulo 5 discute a configuração do chip de teste para a medição.

O capítulo 6 apresenta a conclusão da tese e sugestões para trabalhos futuros.

A.2 PROJETO DO MISTURADOR ATIVO

A fim de cumprir operação multi-banda e multi-protocolo, dois misturadores para conversão a baixas frequências foram projetados. A primeira topologia é um misturador de banda estreita operando a 2 GHz, mostrado na figura 3.13. O principal objetivo para esta topologia foi a avaliação da melhoria na linearidade do estágio de transcondutância do misturador utilizando a técnica de PDHC proposta em KIM; KIM (2008). Uma vez validada a técnica de linearização, uma segunda topologia com uma frequência de operação de 1 a 6 GHz foi projetada. A topologia combina a técnica de cancelamento de ruído de BRUCCOLERI; KLUMPERINK; NAUTA (2004) com a melhoria de linearidade obtida na primeira topologia, a fim de projetar um misturador que cumpra operação multi-banda e multi-protocolo, mostrada na figura 3.14.

Os misturadores projetados seguem a topologia da célula de Gilbert com melhorias para o ruído e linearidade. Cada misturador é formado por três blocos:

- Estágio de transcondutância: Formado por transcondutores altamente lineares utilizando a técnica de PHDC para a primeira topologia e transcondutores com cancelamento de ruído e aprimoramento de linearidade para a segunda topologia.
- Estágio de chaveamento: Formado por quatro chaves de comutação em configuração de balanceamento duplo ($M_{LO)}$ para as duas topologias. Além disso, um circuito de redução dinâmica de corrente (*current bleeding*) para redução de ruído e um filtro LC que ressona com a capacitância parasita das chaves de comutação na frequência do LO para aumentar o IIP_2 foram adicionados à primeira topologia.
- Estágio de carga: Formado pelos transistores (M_{IF}) e resistores (R_L) de carga com uma rede de realimentação modo-comum CMFB (*Common Mode FeedBack*) para operação em baixa tensão nas duas topologias.

Foi desenvolvida uma metodologia de projeto para um misturador tipo célula de Gilbert baseada na metodología $\frac{g_m}{I_D}$ proposta por SILVEIRA; FLANDRE; JESPERS (1996) para dimensionamento de transistores e a metodología $\frac{g_m}{I_D}$ para circuitos de RF proposta por FIORELLI et al. (2011). Os parâmetros de desempenho dos misturadores, tais como: ganho de conversão (GC), figura de ruído (NF), ponto interceptação de terceira ordem referido à entrada (IIP_3) e potência foram caracterizados em função de ($\frac{g_m}{I_D}$), I_{DD} e parâmetros do circuito (V_{DD}, R_L, P_{LO}) criando um espaço de projeto para a otimização das especificações. A metodología é descrita como segue:

- Caracterização da Tecnologia: A caracterização do processo CMOS de 0.13 μm da IBM foi implementado. Usando eficiência de corrente de dreno ($\frac{g_m}{I_D}$) como o eixo de referência para comparar outros parâmetros do dispositivo (V_{OV}, $\frac{g_m}{g_o}$, f_T e

I_D/W). Esses gráficos nos dizem a transcondutância (g_m) que pode ser obtida para uma corrente (I_D) dada. A frequência de trânsito (f_T) e a densidade de corrente (I_D/W) são utilizados para a definição da largura de faixa e dimensionamento de transistores, respectivamente.

- Espaço de projeto para os parâmetros: Após a caracterização da tecnologia, o espaço de projeto para os parâmetros é definido baseado na dependência entre eles. Parâmetros tais como: comprimento de canal (L), eficiência de corrente de dreno ($\frac{g_m}{I_D}$), potência de LO (P_{LO}) e cargas de saída (R_L) fazem parte da exploração do espaço de projeto em nosso método, e são tomados como primeiras escolhas para as otimizações de projeto subsequentes. Os outros parâmetros apresentam uma dependência no nível do dispositivo (L, V_T, $g_m I_D$, I_D) e no nível do circuito (P_{LO} , potência). A Tabela 4.1 os enumera e a Tabela 4.2 mostra a interdependência entre os parâmetros de desempenho e espaço de projeto do misturador. Foram listados: potência, ganho de conversão, figura de ruído e IIP_3. Por exemplo: o ganho de conversão (GC) depende do estágio de transcondutância ($g_{m,RF}$), o ganho de chaveamento (A_{SW}) e a carga de saída (R_L). O IIP_3 e a figura de ruído dependem fortemente do $\frac{g_m}{I_D}$ dos transistores no estágio transcondutância. Isso é útil, oferecendo um ponto de partida no projeto dos misturadores.
- Restrições de projeto: Um diagrama conceitual da metodologia de projeto do misturador é mostrado na figura 4.5. Os parâmetros de desempenho (potência, ganho IIP_3 e NF) do misturador são objetivos do projeto. Cada parâmetro de desempenho é representado em uma caixa. Um modelo analítico para calcular os parâmetros relacionados com a sua dependência é apresentado. Por exemplo, uma restrição de potência limita a I_D máxima disponível para o estágio de transcondutância; uma restrição no IIP_3 define o $\frac{g_m}{I_D}$ do estágio de transcondutância, que pode ser utilizado para estimar o NF. Na metodologia de projeto do misturador uma restrição de potência foi definida. Os outros parâmetros foram projetados de forma a obter o melhor rendimento disponível (maior ganho e IIP_3 e o menor NF). Além disso, dois parâmetros de projeto foram definidos: o tamanho do transistor e o ganho de chaveamento. O primeiro calcula o tamanho do transistor a partir de (ID/W e I_D), figura 4.4, e o segundo estima o ganho de chaveamento (A_{SW}) a partir de (P_{LO}, $(\frac{g_m}{I_D})_{LO}$) obtido no projeto. A combinação de duas restrições, por exemplo restrição de projeto de potência e de ganho afeta diretamente a degradação ou a melhoria dos outros parâmetros de desempenho (IIP_3 e NF). Isto pode ser aplicado a outra combinação de duas restrições. Por exemplo, o estágio transcondutância ($g_{m,RF}$) a partir do ganho de conversão , pode ser calculado a partir do IIP_3 e potência, ou a NF e potência, respectivamente.

Os misturadores foram projetados usando a metodologia descrita acima. Foi definida uma restrição de projeto de consumo de energia, a fim de atingir o mais alto CG e IIP_3 com a menor NF, as outras restrições foram definidas na Tabela 4.5 e Tabela 4.9 para a primeira e segunda topologia, respectivamente.

Os resultados das simulações pós-layout e esquemático, para a primeira e a segunda topologia são mostrados na seção 4.3 do capítulo 4. Para dar uma idea do isolamento entre as portas e do IIP_2, os misturadores foram simulados considerando descasamentos entre os resistores de carga ($\frac{\Delta R_L}{R_L}$) e os transistores de chaveamento (ΔV_T). Em última análise, simulações de Monte Carlo apresentam uma melhor estimativa do IIP_2 e do isolamento entre as portas em presença de descasamentos reais dos dispositivos .

A primeira topologia alcança IIP_2 e IIP_3 iguais da 55.5 dBm e 10.9 dBm a 2GHz, respectivamente. O ganho de conversão é 10.2 dB com uma NF de 12 dB, consumindo apenas 5.3 mW a partir de uma fonte de 1.2 V. A segunda topologia apresenta um bom compromisso entre o ruído e o ganho em toda a extensão de frequência com uma figura de ruído de faixa lateral dupla abaixo de 10 dB e um ganho de conversão acima de 12 dB na faixa de 1 a 6 GHz. O circuito apresenta um valor médio de IIP_3 de 0 dBm, enquanto consome apenas 19.3 mW de uma fonte de 1.2 V.

Na seção 4.4 do capítulo 4, está descrito como foi feito o projeto do layout da primeira topologia, incluindo as especificações do PDK utilizado. Foram utilizados resistores de poli-silício, que possuem maior resistência por unidade de área se comparados aos demais resistores disponíveis na especificação do processo de fabricação (PDK). Os capacitores utilizados foram do tipo MIM (Metal-Isolante-Metal) com plano de terra do tipo SUB. Os transistores utilizados foram os FET regulares de 1.2 V, com V_{TH} típico de 355 mV para os transistores NMOS de comprimento mínimo de canal.

O casamento entre dispositivos não foi um problema neste circuito, então, somente transistores dummy foram utilizados para manter a borda de todos os dispositivos. Para uma melhor isolação de RF, anéis de guarda foram utilizados em todos os transistores desse projeto.

Os PADs utilizados foram os fornecidos pelo PDK com tamanho próximo ao mínimo e proteções ESD foram inseridas no projeto do misturador fabricado, na primeira topologia.

A comparação entre os misturadores reportados e os projetados neste trabalho foi feita. Neste momento apenas resultados de simulação dos misturadores projetados neste trabalho estavam disponíveis para comparar com outras implementações na literatura. Em relação à primeira topologia, o misturador possui o menor consumo e um ganho de 10 dB comparável a outras implementações de faixa estreita. A segunda topologia foi comparada com outros misturadores de faixa larga relatados na literatura disponível. Nenhum deles usa técnicas de linearização para melhorar o IIP_3. Em geral, os misturadores projetados apresentam um desempenho competitivo com uma dissipação de potência razoável para a mesma faixa que outros misturadores comparados .

O capítulo 5 descreve como foi projetada uma Placa de Circuito Impresso (PCI) para medir o circuito integrado contendo o misturador que foi submetido à fabricação (primeira topologia). Esse capítulo descreve principalmente as técnicas de RF para obter o melhor projeto de PCI possível, tentando utilizar trilhas o mais afastadas entre si, o conjunto de capacitores da linha de alimentação próximos ao circuito integrado, cuidados com a largura das trilhas que contém sinais de RF, plano de terra na camada inferior e superior da placa. Além disso, VIAs foram colocadas espaçadas 1/20 avos do comprimento de onda do pior caso de sinal de RF para reduzir acoplamento entre os sinais.

Ao final do capítulo 5, são discutidos os topologias de medição. Basicamente, como a PCI será conectada aos equipamentos de medição: analisador de espectro, analisador de rede, analisador de figura de ruído.

A.3 CONCLUSÃO

Através de uma revisão concisa sobre o estado da arte sobre misturadores, um novo misturador para conversão a baixas frequências que cumpre operação multi-banda e multi-protocolo é apresentada. Linearidade e ruído foram as principais figuras de mérito consideradas para o misturadores propostos. Para aumento linearidade, foi utilizada uma técnica de cancelamento de harmônicas pós-distorção (PDHC). E, para redução de ruído,

foi utilizado um circuito de redução dinâmica de corrente combinada com um filtro LC sintonizado na frequência do LO e cancelamento de ruído térmico.

Foi demonstrado que o modelamento da distorção de um circuito, ou seja, um misturador para conversão a baixas frequências, através de séries de potência só é adequado para baixas frequências, onde a influência das reactâncias do circuito é pequena. Em altas frequências não é mais válido e modelar a distorção tendo em conta estas reatâncias tornou-se crítica para uma análise mais precisa.

A análise de distorção de um circuito através de séries de Volterra pode modelar com precisão os efeitos de memória, que se tornam críticos em RF. A análise de séries de Volterra que foi realizada para o misturador proposto é apresentada nesta Dissertação para mostrar a eficácia da técnica de cancelamento de harmônicas pós-distorção (PDHC).

A combinação da metodologia $\frac{g_m}{I_D}$ para circuitos de RF com o estudo citado anteriormente possibilita ao projetista obter um ponto de operação ótimo de forma a otimizar o misturador. O circuito de linearização adicionado não aumenta o tamanho do misturador, nem degrada ganho de conversão, figura de ruído, ou consumo de potência.

Simulações elétricas foram realizadas para o esquemático elétrico extraído pós-layout para a primeira topologia e nível esquemático para a segunda topologia, usando o processo CMOS de 0.13 μm da IBM. As melhorias em IIP_2 e IIP_3 são apresentadas em comparação com o misturador do tipo célula de Gilbert convencional.

Para a primeira topologia, foi obtido um ganho de conversão de 10.2 dB com uma NF de 12 dB para o misturador projetado funcionando a 2 GHz, com uma frequência intermediária de 500 kHz. E um IIP_2 e IIP_3 de 55 dBm e 10.9 dBm, respectivamente, consumindo apenas 5.3 mW de uma fonte de 1.2 V.

Para a segunda topologia, foram obtidos um ganho de conversão de [13.8 ~11] dB, um coeficiente de reflexão na entrada (S_{11}) de [-18 ~-9.5] dB e um NF de [8.5 ~11] dB no intervalo de 1 a 6 GHz. Para as especificações de linearidade, um valor médio de IIP_3 de 0 dBm foi alcançado para toda a faixa de frequência, consumindo 19.3 mW a partir de uma fonte de 1.2 V. Espeficações adequadas para operação multi-banda e multi-protocolo.

Os requisitos de linearidade e de ruído em aplicações multi-banda e multi-protocolo fazem do projeto de misturadores CMOS de RF uma tarefa muito desafiadora. No entanto, uma definição adequada das especificações do bloco no nível do receptor combinado com técnicas de linearização e redução de ruído possibilitam circuitos que permitem a operação multi-banda e multi-protocolo.

Como trabalhos futuros, os procedimentos de ensaio discutidos no capítulo 5 serão realizados nas amostras fabricadas da primeira topologia (misturador a 2 GHz). A segunda topologia será enviada para fabricação em outra oportunidade no futuro.

APPENDIX B DISTORTION, LOW-FREQUENCY CASE OF GILBERT-CELL MIXER

B.1 Low-Frequency Case

Returning to the Gilbert mixer in Fig. 3.1 since we neglect capacitive effect, then individual transistors in the quad pair $M_{LO,1-4}$ are either completely turned on or off. Hence the switching transistors $M_{LO,1-4}$ in Fig. 3.1 do not contribute to distortion.

Therefore distortion comes primarily from the source coupled pair (SCP) $M_{RF,1-2}$, which does the V/I conversion. Furthermore, we assume that this distortion is dominated by the nonlinear square law I-V characteristics of the MOS transistors biased in strong inversion. Referring to the source coupled pair (SCP) M_{1-2} in Fig. 3.12, we can write, for transistor M_1

$$I_{rf}^{+} = \frac{k}{2}\left(V_{gs1} - V_T\right)^2 \tag{B.1}$$

next the loop equation gives us:

$$V_{rf}^{+} - V_{gs1} = V_{rf}^{-} - V_{gs2} \tag{B.2}$$

rearranging Eq. B.2 gives us

$$V_{gs1} = V_{rf}^{+} - V_{rf}^{-} + V_{gs2} = V_{rf} + V_{gs2} \tag{B.3}$$

substituting Eq. B.3 into B.1

$$I_{rf}^{+} = \frac{k}{2}\left(V_{rf} + \left(V_{gs2} - V_T\right)\right)^2 \tag{B.4}$$

repeating the procedure for transistor M_2

$$I_{rf}^{-} = \frac{k}{2}\left(V_{gs2} - V_T\right)^2 \tag{B.5}$$

which means

$$V_{gs2} - V_T = \sqrt{\frac{2I_{rf}^{-}}{k}} \tag{B.6}$$

substituting Eq. B.6 into B.5,

$$I_{rf}^{+} = \frac{k}{2}\left(V_{rf} + \sqrt{\frac{2I_{rf}^{-}}{k}}\right)^{2} = \frac{k}{2}\left(V_{rf} + \sqrt{\frac{2\left(I_{SS} - I_{rf}^{+}\right)}{k}}\right)^{2} \tag{B.7}$$

Let us normalize by defining the normalized I_{rfn}^{+} , I_{SSn} as

$$I_{rfn}^{+} = \frac{2I_{rf}^{+}}{k} \tag{B.8}$$

$$I_{SSn} = \frac{2I_{SS}}{k} \tag{B.9}$$

substituting the normalized variables into Eq. B.7, we have

$$I_{rfn}^{+} = \left(V_{rf} + \sqrt{I_{SSn} - I_{rfn}^{+}}\right)^{2} \tag{B.10}$$

after some algebraic manipulation

$$\sqrt{I_{rfn}^{+}} - V_{rf} = \sqrt{I_{SSn} - I_{rfn}^{+}}$$

$$V_{rf} = \sqrt{I_{rfn}^{+}} - \sqrt{I_{SSn} - I_{rfn}^{+}}$$

$$= \sqrt{i_{rfn}^{+} + \frac{I_{SSn}}{2}} - \sqrt{I_{SSn} - \left(i_{rfn}^{+} + \frac{I_{SSn}}{2}\right)}$$

$$= \sqrt{i_{rfn}^{+} + \frac{I_{SSn}}{2}} - \sqrt{\frac{I_{SSn}}{2} - i_{rfn}^{+}} \tag{B.11}$$

Here, i_{rfn}^{+} is the ac part of I_{rfn}^{+}. Notice that Eq. B.11 represents an odd function of V_{rf} around $\frac{I_{SSn}}{2}$. Factoring out the I_{SSn} term we have:

$$V_{rf} = \sqrt{\frac{I_{SSn}}{2}}\left(\sqrt{1 + \frac{2i_{rfn}^{+}}{I_{SSn}}} - \sqrt{1 - \frac{2i_{rfn}^{+}}{I_{SSn}}}\right) \tag{B.12}$$

Eq. B.12 gives V_{rf} in terms of i_{rfn}^{+}. Since V_{rf} is input and i_{rfn}^{+} is output, we would instead want to express i_{rfn}^{+} in terms of V_{rf}. Since there is no capacitive effect, each i_{rfn}^{+} term can be expanded as a power series (Taylor series; the two terms will be used interchangeably) in powers of V_{rf}:

$$I_{rfn}^{+} = \alpha_1 V_{rf} + \alpha_2 V_{rf}^{2} + \alpha_3 V_{rf}^{3} + \ldots \tag{B.13}$$

where α_1, α_2, α_3 . . . are coefficients.

Unfortunately, since it is not easy to write i_{rfn}^{+} explicitly in terms of V_{rf} [as evidenced in Eq. B.12], we would get around this difficulty by doing two expansions: First we expand the two square root terms inside the bracket in B.12 around $\frac{2i_{rfn}^{+}}{I_{SSn}}$:

$$V_{rf} = \sqrt{\frac{I_{SSn}}{2}} \left[\begin{array}{l} \left(1 + \frac{1}{2}\left(\frac{2i^+_{rfn}}{I_{SSn}}\right) - \frac{1}{8}\left(\frac{2i^+_{rfn}}{I_{SSn}}\right)^2 + \frac{1}{16}\left(\frac{2i^+_{rfn}}{I_{SSn}}\right)^3 + \ldots\right) \\ -\left(1 - \frac{1}{2}\left(\frac{2i^+_{rfn}}{I_{SSn}}\right) - \frac{1}{8}\left(\frac{2i^+_{rfn}}{I_{SSn}}\right)^2 - \frac{1}{16}\left(\frac{2i^+_{rfn}}{I_{SSn}}\right)^3 + \ldots\right) \end{array} \right]$$

$$= \sqrt{\frac{I_{SSn}}{2}} \left[\frac{2i^+_{rfn}}{I_{SSn}} + \frac{1}{8}\left(\frac{2i^+_{rfn}}{I_{SSn}}\right)^3 + \ldots \right] \tag{B.14}$$

Secondly we would expand each of the i^+_{rfn} term in Eq. B.14 using equation B.13. For simplicity we write down only the first three terms when expanding Eq. B.13. Upon substituting in Eq. B.14 we have:

$$V_{rf} = \sqrt{\frac{I_{SSn}}{2}} \left[\frac{2}{I_{SSn}} \left(\alpha_1 V_{rf} + \alpha_2 V_{rf}^2 + \alpha_3 V_{rf}^3 + \ldots\right) + \frac{1}{8}\left(\frac{2}{I_{SSn}}\right)^3 \left(\alpha_1 V_{rf} + \alpha_2 V_{rf}^2 + \alpha_3 V_{rf}^3 + \ldots\right)^3 + \ldots \right] \tag{B.15}$$

Finally we can solve for the coefficients α_1, α_2, α_3... by equating the coefficients of V_{rf}, V_{rf}^2, ... on both sides of Eq. B.15. For the V_{rf} term

$$1 = \sqrt{\frac{I_{SSn}}{2}} \left(\frac{2}{I_{SSn}}\alpha_1\right) \qquad \therefore \alpha_1 = \sqrt{\frac{I_{SSn}}{2}} \tag{B.16}$$

For the V_{rf}^2 term:

$$0 = \sqrt{\frac{I_{SSn}}{2}} \left(\frac{2}{I_{SSn}}\alpha_2\right) \qquad \therefore \alpha_2 = 0 \tag{B.17}$$

For the V_{rf}^3 term:

$$0 = \sqrt{\frac{I_{SSn}}{2}} \left(\frac{2}{I_{SSn}}\alpha_3 + \frac{1}{8}\left(\frac{2}{I_{SSn}}\right)^3 \alpha_1^3\right) \qquad \therefore \alpha_3 = -\frac{1}{8}\left(\frac{2}{I_{SSn}}\right)^3 \alpha_1^3 \tag{B.18}$$

Let us apply the definition of HD_3 as given in equation 2.18 to the present case

$$HD_3 = \frac{I^+_{rf}\Big|\, 3^{rd} - order - term}{I^+_{rf}\Big|\, fundamental} = \frac{1}{4}\frac{\alpha_3}{\alpha_1} A_{rf}^2 \tag{B.19}$$

substituting the calculated coefficients into Eq. B.19

$$HD_3 = \frac{1}{4}\left| -\frac{1}{8}\left(\frac{2}{I_{SSn}}\right)^3 \right| \frac{I_{SSn}}{2} A_{rf}^2 = \frac{1}{32}\frac{k}{I_{SS}} A_{rf}^2 = \frac{A_{rf}^2}{32(V_{GS} - V_T)^2} \tag{B.20}$$

From Eq. 2.22 $IM_3 = 3HD_3$, and we can substitute Eq. B.20 into this to obtain IM_3.

$$IM_3 = \frac{3A_{rf}^2}{32(V_{GS} - V_T)^2} \tag{B.21}$$

Notice that for IM_3, normally we are interested in the I_{D3} generated in the desired signal frequency from the two adjacent channel interferences. These interferences are denoted as $v_{interference}$ and have amplitudes denoted as $A_{interference}$. To quantify the IM_3 in this case, we rewrite Eq. B.21 as follows:

$$IM_3 = \frac{3A^2_{interference}}{32(V_{GS}-V_T)^2} \tag{B.22}$$

We can characterize this distortion using A_{IP3}, the amplitude of v_{RF} or $v_{interference}$ at the third order intercept point, as well. We start from Eq. 2.25, $IIP_3|_{dBm} = P_{in}|_{dBm} - \frac{IM_3|dB}{2}$.

This equation will lead to the equation $A^2_{IP3} = \frac{A^2_{interference}}{IM_3}$. Substituting IM_3 obtained in Eq. B.22 we have

$$A^2_{IP3} = \frac{A^2_{interference}}{IM_3} = \frac{32(V_{GS}-V_T)^2}{3}$$

$$A_{IP3} = 4\sqrt{\frac{2}{3}}(V_{GS}-V_T) \tag{B.23}$$

B.2 Numerical Examples

B.2.1 Numerical example 1

Referring to Fig. 3.1 let us assume that $M_{RF,1-2}$ and $M_{LO,1-4}$ have a $\frac{W}{L}$ of 16μm/0.2μm and we make $V_{GS}-V_T$ = 0.3 V. A switch gain (A_{SW}) of 0.55 is chosen, see Fig. 3.3.

$$\text{k'= 350 } \mu\text{A/V}^2\text{, then k= 28000 } \mu\text{A/V}^2,$$

$$g_{m,RF} = k(V_{GS}-V_T) = 8.4 \text{ mS}.$$

Suppose we want to design for a conversion gain of 10 dB. Substituting this in equation 3.1 we get

$$CG = g_{m,RF} \cdot R_L \cdot A_{SW} = 0.55 \times R_L \times 8.4\text{mS} = 3.16$$

which gives R_L= 684.5 Ω.

B.2.2 Numerical example 2

Calculate the mixer's distortion behavior: HD_3, IM_3, IIP_3. Assume that a Gilbert mixer operates under the following condition:

$V_{GS}-V_T$ = 0.3 V

$A_{rf} = A_{interference}$= 0.316 V_p or 0 dBm assume that the V_{LO} is not switching

Under these conditions the Gilbert-cell mixer's distortion is dominated by the transconductance stage. Substituting the foregoing values in Eqs. B.20 and B.22 we have

$$HD_3 = \frac{A^2_{rf}}{32(V_{GS}-V_T)^2} = \frac{(0.316)^2}{32\,(0.3)^2} = -29.19dB$$

$$IM_3 = \frac{3A_{rf}^2}{32(V_{GS}-V_T)^2} = \frac{3\,(0.01)^2}{32\,(0.16)^2} = -19.65dB$$

$$IIP_3 = P_{in} - \frac{IM_3|_{dB}}{2} = 0 + \frac{19.65}{2} = 9.82 \text{ dBm}$$

B.2.3 Numerical example 3

In this example we want to design this mixer with some safety margin. Let us arbitrarily set the specifications to be

$$IIP_3 = 5 \text{ dBm}$$

$$\text{Power} = 5 \text{ mW}$$

$$V_{DD} = 1.2 \text{ V}$$

$$\text{k'} = 350\ uA/V^2$$

Assuming that V_{LO} is no switching, calculate the $\frac{W}{L}$ for the transistors of the transconductance stage.

$IIP_3 = 5$ dBm means that 5 dBm = $10 \log \frac{A_{IP3}^2}{2 \times 50}$.

Solving we have $A_{IP3} = \sqrt{2 \times 50 \times 10^{\frac{A_{IP3}|\,dBmV}{10}}} = \sqrt{2 \times 50 \times 10^{\frac{5dBmV}{10}}}$ =0.56V.

substituting into Eq. B.23 we have

$$V_{GS} - V_T = 0.17 \text{ V}.$$

Now with P = 5 mW, V_{DD} = 1.2 V, we have

$$\text{I} = 4.17\text{mA}.$$

substituting half of this value of current into the square law current equation, with a given k' = 350 uA/V^2, we get

$$\frac{W}{L} = 401.6.$$

B.2.4 Numerical example 4

Assume that a Gilbert mixer has a V-I converter as shown in Fig. 3.12. Referring to Fig. 3.12 let both NMOS transistors have a $\frac{W}{L}$ of 16μm/0.2μm.

Let us apply a V_{rf} at 2 GHz and two interference signals $V_{interference}$ at 2.0005 GHz and 2.0015 GHz. Their power levels are set at 0 dBm. Again we make $V_{GS} - V_T$ = 0.3 V. Now assume k'= 350 μA/V^2. This means k = 126000 μA/V^2. C_s is given as C_s= 100 fF.

Finally let us assume that V_{LO} is not switching and that the Gilbert mixer's distortion is dominated by the V-I converter.

(a) Assume intermediate frequency approximation holds, find IM_3 of this Gilbert mixer.

(b) Assume intermediate frequency approximation does not hold, find HD_2 of this Gilbert mixer.

(a) Since interference signal has a power level of 0 dBm, this means $A_{interference}$= 10m V_p. Substituting this and other relevant values into Eq. 3.65, the expression for IM_3 using intermediate frequency approximation, we have

$$IM_3 = \frac{3(0.316)^2}{32(0.3)^2}\left[\left|1 - \frac{2}{3}\frac{j(2\pi \times 2.0005G)\,100fF}{2 \times 126000\mu A/V^2(0.3)}\right|\right] = 0.1041\,|1 - 0.04987j|$$

$$= 0.1042 = -19.63dB$$

(b) First we extend the definition of HD_3 given in Eq. 3.61 to HD_2. After some simplification we get

$$HD_2 = \frac{i_{d2}}{i_{d1}} = \frac{A_{rf}\,|G_2|}{2\,|G_1|}$$

Next we calculate G_2. Since the intermediate frequency approximation does not hold, we use the full expression for G_2 as given in Eq. 3.58. Substituting the proper values, we have

$$G_2 = \frac{k}{8}\left[1 - \frac{1}{\left[1 + \frac{j(\omega_1 + \omega_2)C_s}{2k(V_{GS} - V_T)}\right]}\right] =$$

$$\frac{28000\mu A/V^2}{8}\left[1 - \frac{1}{\left[1 + \frac{j(2 \times 2\pi \times 2.0005G)\,100fF}{2 \times 28000\mu A/V^2(0.3)}\right]}\right]$$

$$|G_2| = \left|\frac{28000\mu A/V^2}{8}\left[1 - \frac{1}{\left[1 + \frac{j(2 \times 2\pi \times 2.0005G)\,100fF}{2 \times 28000\mu A/V^2(0.3)}\right]}\right]\right|$$

$$= \left|3500\mu A/V^2\left[1 - \frac{1}{[1 + 0.149j]}\right]\right| = 3500\mu A/V^2 \times 0.148$$

$$|G_2|_{\omega_1 = \omega_2 = 2GHz} = 517.96\mu A/V^2$$

Next we calculate G_1 by substituting the proper values into Eq. 3.57.
We have

$$G_1 = \frac{k}{2}(V_{GS} - V_T) = 14000\mu A/V^2(0.3V) = 4200\mu A/V^2$$

Finally substituting G_1, G_2 into the definition of HD_2 we have

$$HD_2 = \frac{0.316}{2} \times \frac{517.96\mu A/V^2}{4200\mu A/V^2}$$

$$= 0.00194$$

$$= -34.2\,dB$$

As a comparison, let us repeat the calculation for this HD_2, except this time we ignore the memory effect. For a Gilbert-cell mixer, from Table 3.2. Using the Taylor series representation, $\alpha_2 = 0$. Hence the HD_2 of a Gilbert-cell mixer, ignoring memory effect, is 0. This is different from the HD_2 calculated incorporating memory effect. This difference may not be surprising because when we include memory effect the Gilbert-cell mixer no longer has odd symmetry in the ac sense and therefore $HD_2 \neq 0$.

APPENDIX C NONLINEAR VOLTERRA SERIES ANALYSIS OF CMOS AMPLIFIERS

In this part, the distortion analysis of a common source (CS) amplifier using Volterra series is described. Consider a commonly used CS amplifier without the DC bias circuit, as shown in Fig. C.1a. To generalize the circuit for any conditions, the degeneration and load impedances are denoted by Z_S and Z_L, respectively. Z_L can be either a cascode device or load impedance, depending on the design. The complete small-signal equivalent circuit for the simplified CS amplifier with C_{gd} and C_{gs} is shown in Fig. C.1b. The external impedances such as the source resistance and matching components, are combined as Z_1.

For the simplicity of the Volterra Series derivation, the following assumptions are made.

- The resistance values for gate, source, and drain are insignificant. The gate resistance will be small in most LNA designs, since it has a direct effect on noise figure. The drain and source resistances will be kept small as well.
- The amplifier will be operating in the weakly nonlinear region.
- The body effect will be negligible, i.e., $g_{mb} \approx 0$.
- The gate-source and gate-drain capacitances are constant at a fixed bias point.

From a time-invariant memoryless nonlinear system model the drain current of a MOSFET can be modeled by the power series representation

$$i_d(v_{gs}) = g_1 \cdot v_{gs} + g_2 \cdot v_{gs}^2 + g_3 \cdot v_{gs}^3 + ... \tag{C.1}$$

where g_1 is the small-signal transconductance, g_2 is the first-order derivative of , g_3 and is the second-order derivative of g_1. The final goal is to derive the relationship between the input voltage and the output current so that the third-order nonlinearity coefficient can be identified. In weakly nonlinear operation, the output current can be represented by the following truncated Volterra series:

$$i_{out}(v_x) = C_1(s) \circ v_x + C_2(s_1, s_2) \circ v_x^2 + C_3(s_1, s_2, s_3) \circ \cdot v_x^3 + ..., \tag{C.2}$$

The gate-source voltage and gate-drain voltage can be expressed by a truncated Volterra series, as a function of input voltage, as well

$$v_{gs}(v_x) = A_1(s) \circ v_x + A_2(s_1, s_2) \circ v_x^2 + A_3(s_1, s_2, s_3) \circ \cdot v_x^3 + ..., \tag{C.3}$$

$$v_{gs}(v_x) = B_1(s) \circ v_x + B_2(s_1, s_2) \circ v_x^2 + B_3(s_1, s_2, s_3) \circ \cdot v_x^3 + ..., \tag{C.4}$$

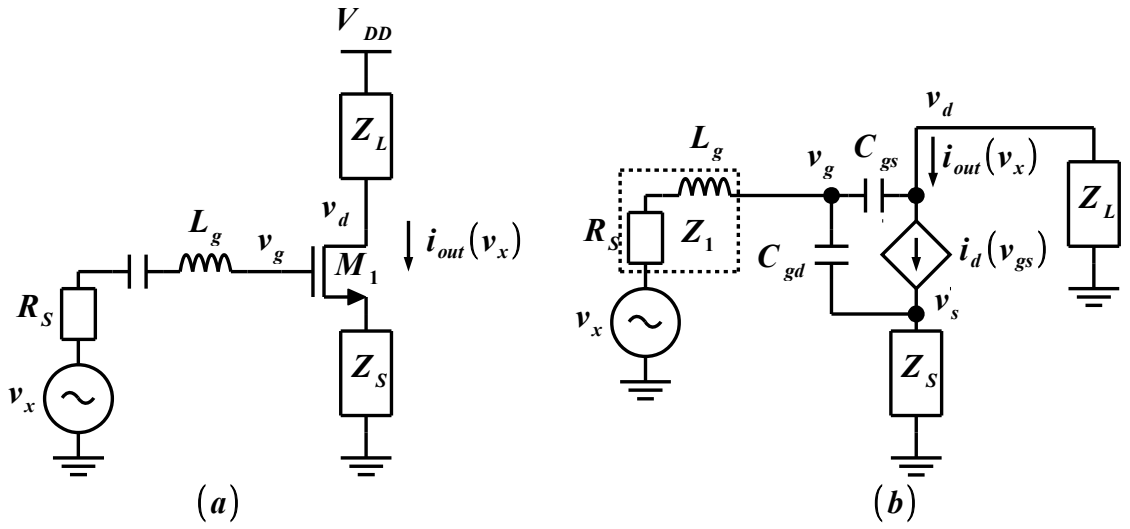


Figure C.1: (a) Simplified common-source amplifier. (b) Equivalent circuit for CS amplifier including C_{gd} and C_{gs}

where $A_n(s_1,s_2,...,s_n)$ and $B_n(s_1,s_2,...,s_n)$ are the Laplace transforms of the nth-order Volterra kernels. From Fig. C.1b, a nodal equation at the drain node can be derived as

$$i_{out} = i_d - sC_{gd} \cdot v_{gd} \tag{C.5}$$

where s can be s_1, s_1+s_2 , or $s_1+s_2+s_3$ depending on the nonlinearity order. By inserting Eqs. C.1, C.2, C.3, and C.4 into C.5, the Volterra kernels can be expressed in the manner $A_n(s_1,s_2,...,s_n)$ of and $B_n(s_1,s_2,...,s_n)$. Therefore, the first step is to determine them. The *harmonic input* method will be used to calculate each Volterra kernel in Eqs. C.2, C.3, and C.4, MAAS (2003). This method is based on multi-tone excitation and solving the nodal equations in the frequency domain at the sum of all input frequencies.

In order to calculate the Voltage kernels, we will apply the KLC equations for each node of the circuit in Fig. C.1b

$$\frac{v_x - v_g}{Z_1(s)} - sC_{gd} \cdot v_{gd} - sC_{gs} \cdot v_{gs} = 0 \tag{C.6}$$

$$i_d - sC_{gd} \cdot v_{gd} - i_{out} = 0 \tag{C.7}$$

$$i_d + sC_{gs} \cdot v_{gs} - \frac{Z_S(s)}{v_s} = 0 \tag{C.8}$$

where i_d, i_{out}, v_{gs}, and v_{gd} are defined by Eqs. C.2, C.3, C.4, and C.5 respectively. The solution of Eq. C.6 for v_x is

$$v_x = [(Z_1(s) + Z_S(s)) \cdot b(s) + 1] \cdot v_{gs} + Z_1(s) \cdot a(s) \cdot v_{gd} + Z_S(s) \cdot i_d \tag{C.9}$$

where $a(s) = sC_{gd}$ and $b(s) = sC_{gs}$. Now, the gate-drain voltage (v_{gd}) can be written as

$$v_{gd} = \frac{[Z(s) \cdot b(s) + 1] \cdot v_{gs} + [Z_S(s) + Z_L(s)] \cdot i_d}{1 + Z_L(s)a(s)} \tag{C.10}$$

Inserting Eqs. C.2, C.3, and C.4 into Eqs. C.9 and C.10 and exciting the circuit single tone, $v_x = e^{st}$, the linear transfer function of v_{gd}, $B_1(s)$ can be evaluated for e^{st} from Eqs. C.9 and C.10.

$$B_1(s) = \frac{1 - A_1(s) \cdot [b(s) \cdot (Z_1(s) + Z_S(s)) + g_1 Z_S(s) + 1]}{Z_1(s) a(s)} \tag{C.11}$$

$$B_1(s) = \frac{A(s) \cdot [b(s) \cdot (Z(s) + g_1 \cdot (Z_S(s) + Z_L(s)) + 1]}{1 + Z_L(s) a(s)} \tag{C.12}$$

Since Eqs. C.11 and C.12 are two different expressions for $B_1(s)$ and both contain $A_1(s)$, $A_1(s)$ can be derived by setting Eq. C.11 = C.12. So

$$A_1(s) = \frac{1}{g_1 + g(s)} \cdot \frac{1 + Z_L(s) a(s)}{Z_x(s)} \tag{C.13}$$

where

$$g(s) = \frac{1 + a(s) \cdot (Z_1(s) + Z_L(s)) + b(s) \cdot (Z_1(s) + Z_x(s))}{Z_x(s)} \tag{C.14}$$

$$Z_x(s) = Z_S(s) + a(s) \cdot Z_{123}(s) \tag{C.15}$$

$$Z_{123}(s) = Z_1(s) Z_L(s) + Z_S(s) Z_L(s) + Z_S(s) Z_1(s) \tag{C.16}$$

$$\begin{aligned} C_1(s) &= g_1 A_1(s) - a(s) B_1(s) \\ &= \tfrac{A_1(s)}{1 + a(s) Z_L(s)} \cdot [g_1 - a(s)(1 + Z_S(s)(g_1 + b(s)))] \end{aligned} \tag{C.17}$$

By following the same procedure with a two-tone excitation, $v_x = e^{s_1 t} + e^{s_2 t}$, and evaluating for $e^{(s_1 + s_2)t}$, the second-order Volterra kernels, $A_2(s_1, s_2)$ and $B_2(s_1, s_2)$, can be found as Eqs. C.20 and C.21, respectively.

$$\begin{aligned} 0 = {} & [(Z_1(s_1 + s_2) + Z_S(s_1 + s_2)) \cdot b(s_1 + s_2) + 1] \cdot A_2(s_1, s_2) \\ & + Z_1(s_1 + s_2) \cdot a(s_1 + s_2) \cdot B_2(s_1 + s_2) \\ & + Z_S(s_1 + s_2) \cdot (g_1 A_2(s_1, s_2) + g_2 A_1(s_1) A_1(s_2)) \tfrac{1}{Z_1(s_1 + s_2) a(s_1 + s_2)} \end{aligned} \tag{C.18}$$

$$\begin{aligned} B_2(s_1, s_2) = {} & [(Z_S(s_1 + s_2) \cdot b(s_1 + s_2) + 1) \cdot A_2(s_1, s_2) \\ & + (Z_S(s_1 + s_2) + Z_L(s_1 + s_2)) \cdot (g_1 A_2(s_1, s_2) \\ & + g_2 A_1(s_1) A_1(s_2))] \cdot \tfrac{1}{1 + Z_L(s_1 + s_2) a(s_1 + s_2)} \end{aligned} \tag{C.19}$$

$$A_2(s_1, s_2) = -\frac{1}{g_1 + g(s_1 + s_2)} \cdot g_2 A_1(s_1) A_1(s_2) \tag{C.20}$$

$$\begin{aligned} B_2(s_1, s_2) = {} & [A_2(s_1, s_2) \cdot (Z_S(s_1 + s_2)) \cdot b(s_1 + s_2) + g_1 (Z_S(s_1 + s_2) + Z_L(s_1 + s_2)) + 1) \\ & + g_2 A_1(s_1) A_1(s_2) (Z_S(s_1 + s_2) \\ & + Z_L(s_1 + s_2))] \tfrac{1}{1 + Z_L(s_1 + s_2) a(s_1 + s_2)} \end{aligned} \tag{C.21}$$

$$C_2(s_1, s_2) = g_1 \cdot A_2(s_1, s_2) + g_2 \cdot A_1(s_1) A_2(s_2) - a(s_1 + s_2) B_2(s_1, s_2) \tag{C.22}$$

With three-tone excitation, $v_x = e^{s_1 t} + e^{s_2 t} + e^{s_3 t}$, and evaluating for $e^{(s_1+s_2+s_3))t}$, the third-order Volterra kernels, $A_3(s_1,s_2,s_3)$ and $B_3(s_1,s_2,s_3)$, can be found as Eqs. C.25 and C.26, respectively.

$$\begin{aligned} 0 \;=\; & [(Z_1(s_{1,2,3}) + Z_S(s_{1,2,3})) \cdot b(s_{1,2,3}) + 1] \cdot A_3(s_1,s_2,s_3) \\ & + Z_1(s_{1,2,3}) \cdot a(s_{1,2,3}) \cdot B_2(s_{1,2,3}) + Z_S(s_{1,2,3}) \cdot (g_1 \cdot A_3(s_1,s_2,s_3) \\ & + 2g_2 \cdot \overline{A_1(s_1)A_2(s_2,s_3)} + g_3 \cdot A_1(s_1)A_1(s_3)A_1(s_3)) \frac{1}{Z_1(s_{1,2,3})a(s_{1,2,3})} \end{aligned} \tag{C.23}$$

$$\begin{aligned} B_3(s_1,s_2,s_3) \;=\; & [(Z_S(s_{1,2,3}) \cdot b(s_{1,2,3}) + 1) \cdot A_3(s_1,s_2,s_3) + (Z_S(s_{1,2,3}) + Z_L(s_{1,2,3})) \\ & \cdot (g_1 \cdot A_3(s_1,s_2,s_3) + 2g_2 \cdot \overline{A_1(s_1)A_2(s_2,s_3)} \\ & + g_3 \cdot A_1(s_1)A_1(s_3)A_1(s_3))] \cdot \frac{1}{1+Z_L(s_{1,2,3})a(s_{1,2,3})} \end{aligned} \tag{C.24}$$

$$A_3(s_1,s_2,s_3) = -\frac{1}{g_1 + g(s_{1,2,3})} \cdot [2g_2 \cdot \overline{A_1(s_1)A_2(s_2,s_3)} + g_3 \cdot A_1(s_1)A_1(s_3)A_1(s_3)] \tag{C.25}$$

$$\begin{aligned} B_3(s_1,s_2,s_3) \;=\; & [A_3(s_1,s_2,s_3) \cdot (Z_S(s_{1,2,3})) \cdot b(s_{1,2,3})) \\ & + g_1(Z_S(s_{1,2,3}) + Z_L(s_{1,2,3})) + 1 + 2g_2 \cdot \overline{A_1(s_1)A_2(s_2,s_3)} \\ & + g_3 \cdot A_1(s_1)A_1(s_3)A_1(s_3)(Z_S(s_{1,2,3}) + Z_L(s_{1,2,3}))] \frac{1}{1+Z_L(s_{1,2,3})a(s_{1,2,3})} \end{aligned} \tag{C.26}$$

where $s_{1,2,3}$ means $s_1 + s_2 + s_3$. The overbar in equations C.25 and C.26 indicates the symmetrization of all possible permutations of the Laplace variables, MAAS (2003), i. e.,

$$\overline{A_1(s_1)A_2(s_2,s_3)} = \frac{1}{3}[A_1(s_1)A_2(s_2,s_3) + A_1(s_2)A_2(s_1,s_3) + A_1(s_3)A_2(s_1,s_2)] \tag{C.27}$$

For the IM_3 test case, Eq. C.27 can be simplified into Eqs. C.28 and C.29, since $s_1 = s_2 = s_2$ and $s_3 = -s_1$ for $2\omega_2 - \omega_1$, and $s_1 = s_2 = s_1$ and $s_3 = -s_2$ for $2\omega_1 - \omega_2$ and

$$\overline{A_1(s_2)A_2(s_2,-s_1)} = \frac{1}{3}[2A_1(s_2)A_2(s_2,-s_1) + A_1(-s_1)A_2(s_2,s_2)] \tag{C.28}$$

$$\overline{A_1(s_1)A_2(s_1,-s_2)} = \frac{1}{3}[2A_1(s_1)A_2(s_1,-s_2) + A_1(-s_2)A_2(s_1,s_1)] \tag{C.29}$$

Inserting Eqs. C.13 and C.20 into Eqs. C.28 and C.29

$$\overline{A_1(s_2)A_2(s_2,-s_1)} = \frac{1}{3} \cdot g_2 A_1^2(s_2)A_1(-s_1) \cdot \left[\frac{2}{g_1 + g(s_2 - s_1)} + \frac{1}{g_1 + g(2s_2)}\right] \tag{C.30}$$

$$\overline{A_1(s_1)A_2(s_1,-s_2)} = \frac{1}{3} \cdot g_2 A_1^2(s_1)A_1(-s_2) \cdot \left[\frac{2}{g_1 + g(s_1 - s_2)} + \frac{1}{g_1 + g(2s_1)}\right] \tag{C.31}$$

Assuming closely spaced frequencies such that $s_1 \approx s_2 \approx s$. The third-order Volterra kernel, $A_3(s_2, s_2, -s_1)$. can be expressed as

$$A_3(s_2, s_2, -s_1) = \frac{-1}{g_1 + g(s)} |A_1(s)|^3 \cdot \varepsilon(\triangle s, 2s) \tag{C.32}$$

where $\triangle s = s_2 - s_1$

$$\varepsilon(\triangle s, 2s) = g_3 - \frac{2}{3} g_2^2 \times \left[\frac{2}{g_1 + g(\triangle s)} + \frac{1}{g_1 + g(2s)} \right] \tag{C.33}$$

Commuting s_2 with s_1, the expression for $A_3(s_1, s_1, -s_2)$ can be done due to the symmetrization of Volterra kernel. Using Eq. C.7 with the equations above and the harmonic excitation method as before, the third-order Volterra kernel of the final output can be found

$$C_3(s_2, s_2, -s_1) = |A_1(s)|^3 \times \left[\frac{1}{g_1 + g(s)} \cdot \frac{\alpha(s)}{Z_x(s)} \right] \times \varepsilon(\triangle s, 2s) \tag{C.34}$$

where

$$\alpha(s) = b(s) \cdot [Z_1(s) + Z_S(s)] + a(s) Z_1(s) + 1. \tag{C.35}$$

For calculate IIP_3, we need to compute the ratio of $C_1(s)/C_3(s_2, s_2, -s_1)$. Using equations C.17 and C.34, we get

$$\frac{C_1(s)}{C_3(s_2, s_2, -s_1)} = \frac{1}{H(s) |A_1(s)|^3 \varepsilon(\triangle s, 2s)} \tag{C.36}$$

where

$$H(s) = \frac{b(s)(Z_1 + Z_S) + a(s) Z_1(s) + 1}{g_1 - a(s)[1 + Z_S(s)(b(s) + g_1)]} \tag{C.37}$$

Using the calculated ratio of $C_1(s)/C_3(s_2, s_2, -s_1)$, we find IM_3

$$IM_3 = \frac{3}{4} \left| \frac{C_3(s_2, s_2, -s_1)}{C_1(s)} \right| A_{rf}^2 \tag{C.38}$$

where A_{rf} is the amplitude of the tones, since IIP_3 is defined as the power of each tone at which $IM_3 = 1$. Substituting $IM_3 = 1$ into Eq. C.38, we can find:

$$A_{IP3} = \sqrt{\frac{4}{3} \left| \frac{C_1(s)}{C_3(s_2, s_2, -s_1)} \right|} \tag{C.39}$$

and

$$IIP_3 = \frac{A_{IP3}^2}{2} = \frac{2}{3} \left| \frac{C_1(s)}{C_3(s_2, s_2, -s_1)} \right| \tag{C.40}$$

We will treat IIP_3 as the available power of the signal generator. It is given by APARIN; PERSICO (1999)

$$IIP_{3,2\omega_2 - \omega_1} = \frac{A_{IP3,2\omega_2 - \omega_1}^2}{8 Re(Z_1(s))} = \frac{1}{6 Re(Z_1(s))} \left| \frac{C_1(s)}{C_3(s_2, s_2, -s_1)} \right| \tag{C.41}$$

$$IIP_{3,2\omega_2-\omega_1} = \frac{1}{6Re(Z_1(s))\,|H(s)|\,|A_1(s)|^3\,|\varepsilon(\Delta s, 2s)|}, \tag{C.42}$$

where

$$H(s) = \frac{1 + sC_{gs}[Z_1(s) + Z_S(s)] + sC_{gd}Z_1(s)}{g_1 - sC_{gd}[1 + Z_S(s)(g_1 + sC_{gd})]} \tag{C.43}$$

$$A_1(\omega) = \frac{1}{g_1 + g(s)} \cdot \frac{1 + sC_{gd}Z_L(s)}{Z(s)} \tag{C.44}$$

$$\varepsilon(\Delta s, 2s) = g_3 - g_{OB} \tag{C.45}$$

$$g_{OB} = \frac{2g_2^2}{3}\left[\frac{2}{g_1 + g(\Delta s)} + \frac{1}{g_1 + g(2s)}\right] \tag{C.46}$$

$$g(s) = \frac{1 + sC_{gs}[Z_1(s) + Z(s)] + sC_{gd}[Z_1(s) + Z_L(s)]}{Z(s)} \tag{C.47}$$

$$Z(s) = Z_S(s) + sC_{gd}\{Z_S(s)[Z_1(s) + Z_L(s)] + Z_1(s)Z_L(s)\} \tag{C.48}$$

Here have neglect the dependence of IIP_3 on Δs ($\Delta s = s_2 - s_1$) assuming that the latter is much smaller than s ($s \approx s_1 \approx s_2$).

The equation of interest here is C.45. To cancel the second-order contribution, the second term of Eq. C.45 should be set to zero. This requires $g(2s)$ to be infinite, which can only happen if $Z(2s) = 0$ according to Eq. C.47.

The second term of Eq. C.45 can be zeroed by tuning the FET terminal impedances Z_1 and Z_L at the second-order harmonic frequency.

APPENDIX D COMPLEMENTARY SIMULATIONS RESULTS

D.1 Technology Characterization of the PDK IBM 0.13 μm CMOS

As mentioned in section 4.2.1 additional plots were extracted the technology.

The transistor channel length, L , dependence of the threshold voltage V_T is shown in Fig. D.1. In our designed mixers we use two different channel lengths, a $L = 0.2\mu m$ for the first topology and $L = 0.12\mu m$ for the second topology.

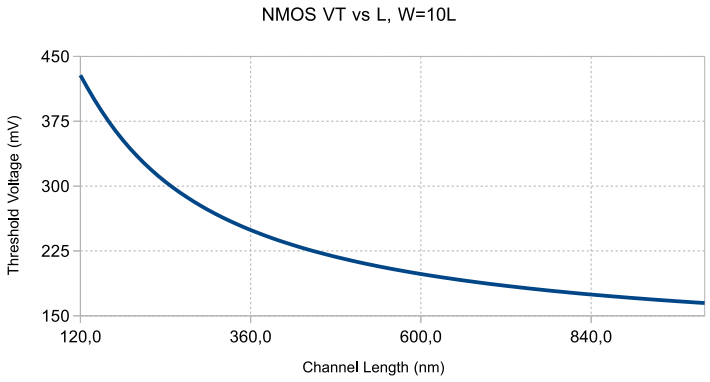


Figure D.1: V_T variation due to channel length of the IBM 0.13 μm CMOS process

The relation between the drain current efficiency ($\frac{g_m}{I_D}$) and the overdrive voltage (V_{OV}) was is shown in Fig. D.2. It was extracted for different channel lengths.

The transistor intrinsic gain ($\frac{g_m}{g_o}$) was plotted against the overdrive voltage (V_{OV}) and the drain current efficiency ($\frac{g_m}{I_D}$), and are shown in Figs. D.3 and D.4, respectively. The transistor has higher intrinsic gain at lower overdrive values due to the output resistance decreasing faster than the transconductance, which increases at higher current levels.

The transit frequency f_T vs V_{OV} is shown in Fig. D.5.

The current density I_D/W vs V_{GS} is shown in Fig. D.6.

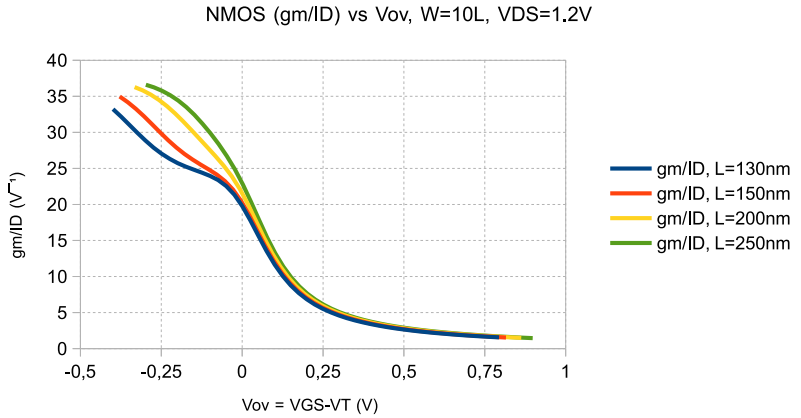


Figure D.2: Drain current efficiency ($\frac{g_m}{I_D}$) vs Overdrive Voltage (V_{OV}) for different channel lengths

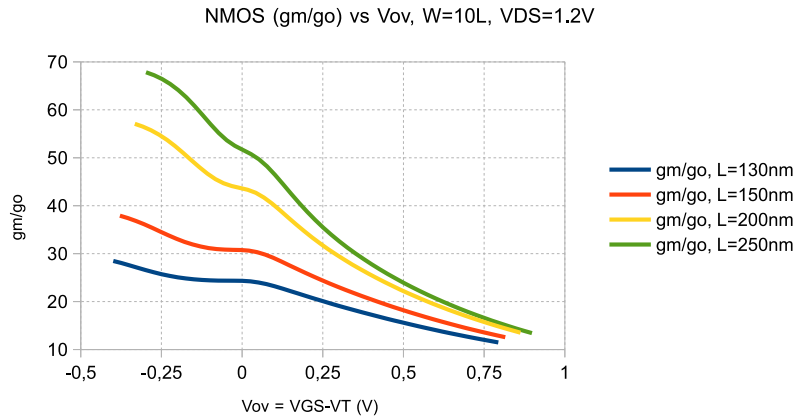


Figure D.3: Intrinsic transistor gain ($\frac{g_m}{g_o}$) vs Overdrive Voltage (V_{OV}) for different channel lengths

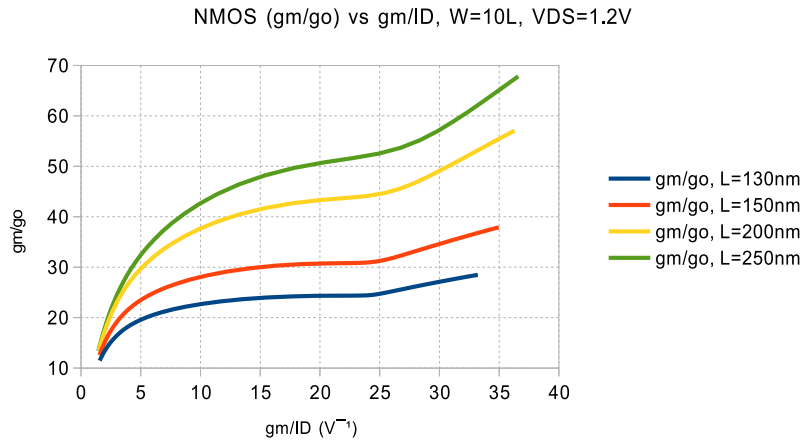


Figure D.4: Intrinsic transistor gain ($\frac{g_m}{g_o}$) vs Drain current efficiency ($\frac{g_m}{I_D}$) for different channel lengths

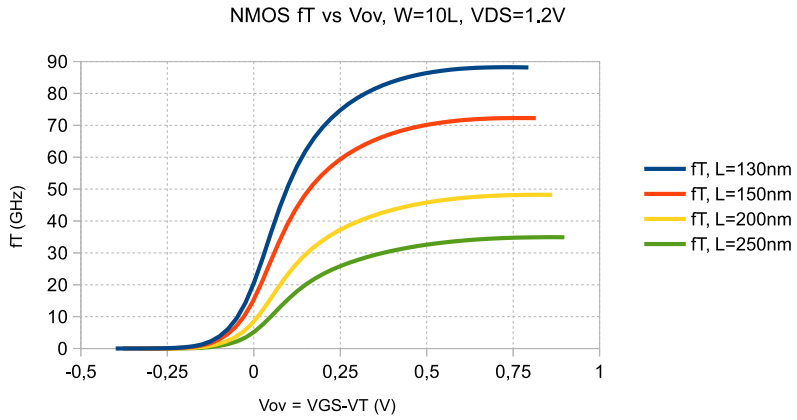


Figure D.5: Transit frequency (f_T) vs Overdrive Voltage (V_{OV}) for different channel lengths

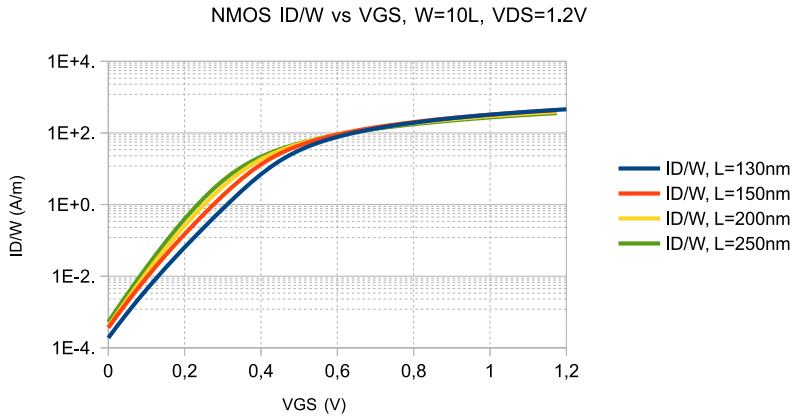


Figure D.6: Current density (I_D/W) vs V_{GS} for different channel lengths

D.2 Design Constraint

As mentioned in section 4.2.3, the switching gain A_{SW} was plotted as a function of the LO Power (P_{LO}) for different values of the drain current efficiency of the switching transistors $(\frac{g_m}{I_D})_{LO}$, Fig. D.7.

Linearity parameters such as: $IP1dB$ and Fig. IIP_2 are shown in Figs. D.8 and D.9, respectively, as a function of the drain current efficiency of the transistor of the transconductance stage $(\frac{g_m}{I_D})_{RF}$.

Finally, the feedthrough between ports: RF-IF, LO-IF, and LO-RF are shown in Figs. D.10 and D.11.

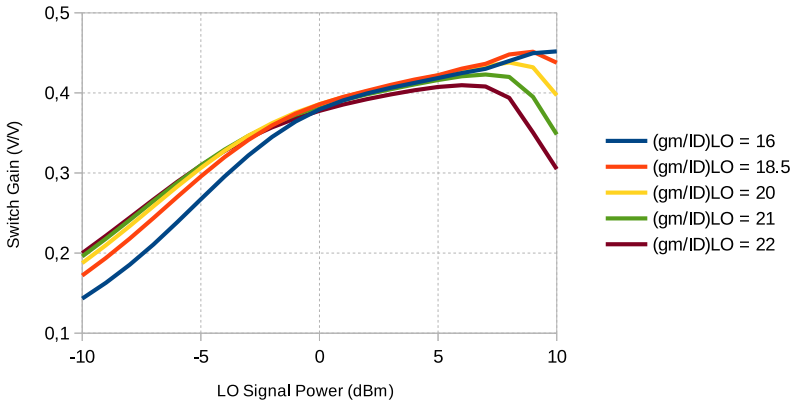


Figure D.7: Switching Gain (A_{SW}) vs LO Signal Power

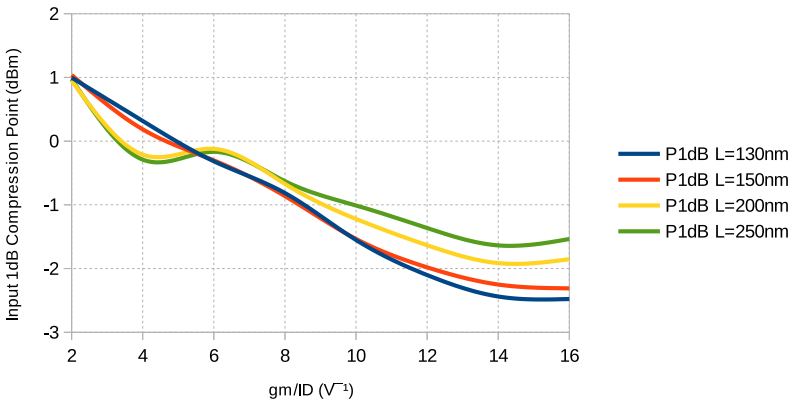


Figure D.8: $IP1dB$ vs $(\frac{gm}{I_D})_{RF\ stage}$

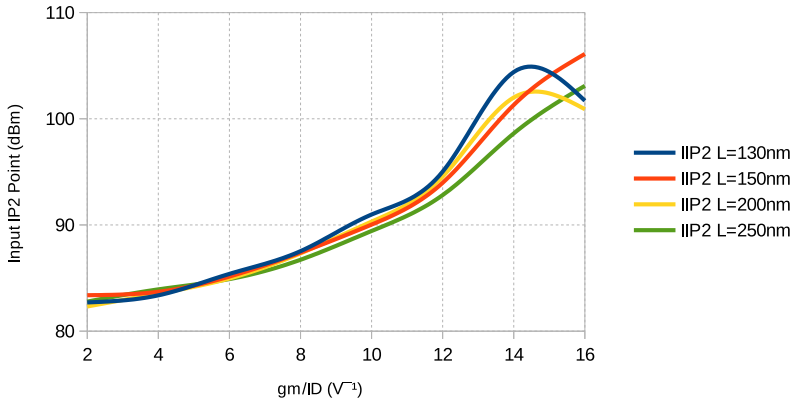


Figure D.9: IIP_2 vs $(\frac{gm}{I_D})_{RF\ stage}$. ($\Delta V_{TH}$= 0 and $\frac{\Delta R_L}{R_L}$= 0.5%)

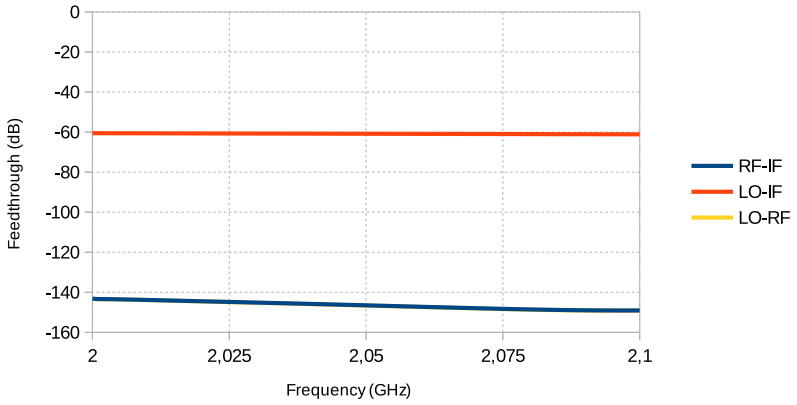


Figure D.10: Feedthrough between mixers ports. (ΔV_T= 0 and $\frac{\Delta R_L}{R_L}$= 0.5%)

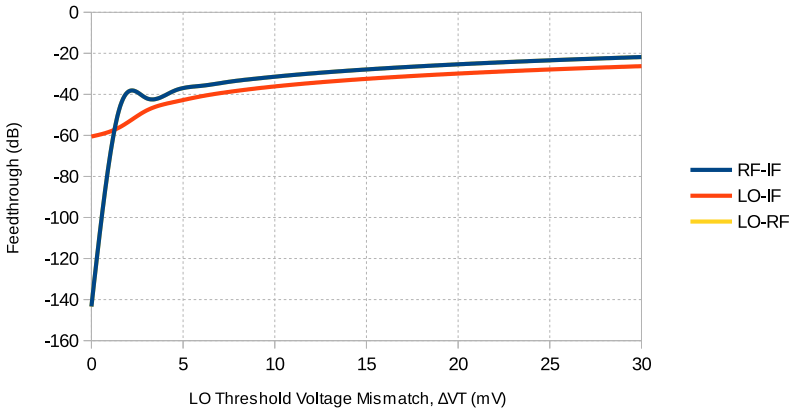


Figure D.11: Feedthrough characterization, considering LO transistor threshold voltage offset (ΔV_T)

D.3 Simulations Results : First Topology

As mentioned in subsection 4.3.2.1, additional simulation were performed. Fig. D.12 shows the mixer has a 1 dB compression point of -1.8 dBm, which was determined by sweeping the power of a single 2 GHz RF input tone. In the same way an IIP_2 of 55.5 dBm was obtained, Fig. D.14. In Fig D.13 a simulation was performed to determine how the IIP_3 changes as a function of the frequency space between the two RF test tones, the frequency space between them is varied within 0.5 - 30 MHz range.

Fig. D.15 shows the port-to-port feedthrough, considering a 0.5% load resistor mismatches ($\frac{\Delta R_L}{R_L}$) and 5 mV of mismatch between switching transistors (ΔV_T).

The progression of the simulated conversion gain, DSB NF, $IP1dB$, IIP_2 and IIP_3 for a sweep of the LO signal power can be observed in figures D.16, D.17, D.18. Based on the specification trade-offs in these plots, the LO power of 2.5 dBm was selected for this mixer design.

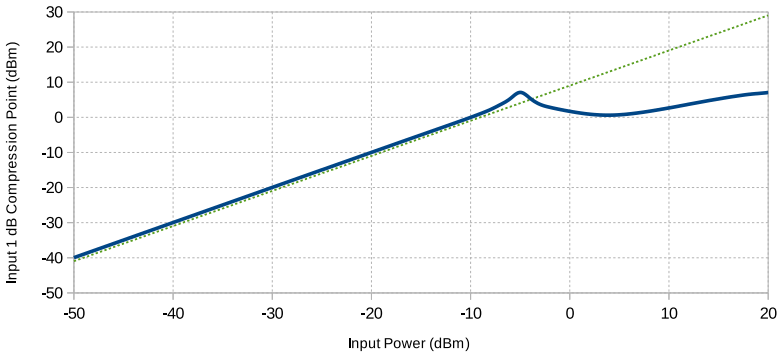


Figure D.12: $P1dB$ vs. Input Power.

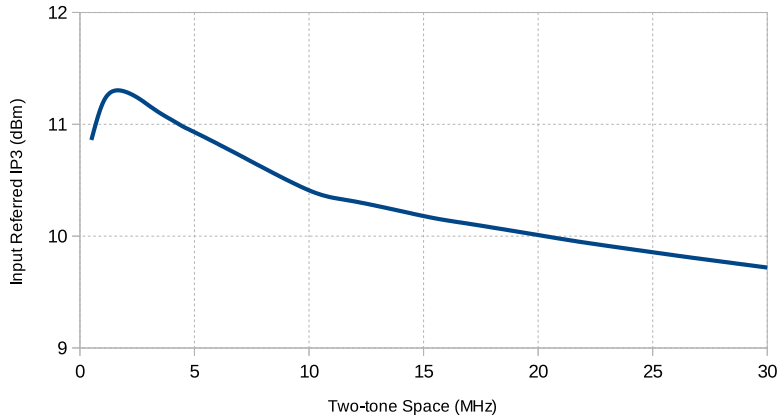


Figure D.13: IIP_3 vs. Frequency space between RF test tones. LO frequency: 1.9995 GHz, RF test tone: 2 GHz

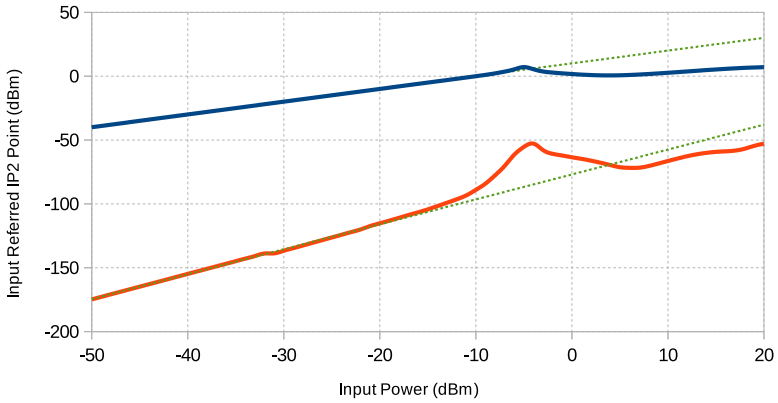


Figure D.14: IIP_2 vs. Input Power. LO frequency: 1.9995 GHz, RF test tones: 2 GHz, 2.001 GHz, IM_2 frequency: 1 MHz. Feedthrough between mixers ports. (ΔV_T= 5mV and $\frac{\Delta R_L}{R_L}$= 0.5%)

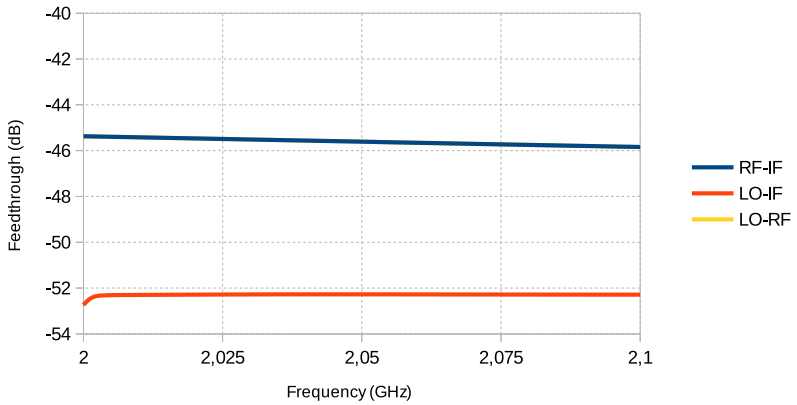


Figure D.15: Feedthrough between mixers ports. (ΔV_T= 5mV and $\frac{\Delta R_L}{R_L}$= 0.5%)

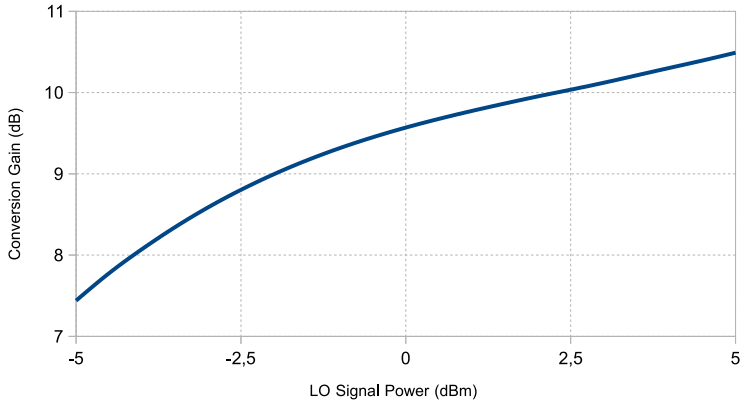


Figure D.16: Conversion Gain vs. LO Signal Power. (LO =1.9995 GHz, RF = 2GHz, IF = 500 kHz)

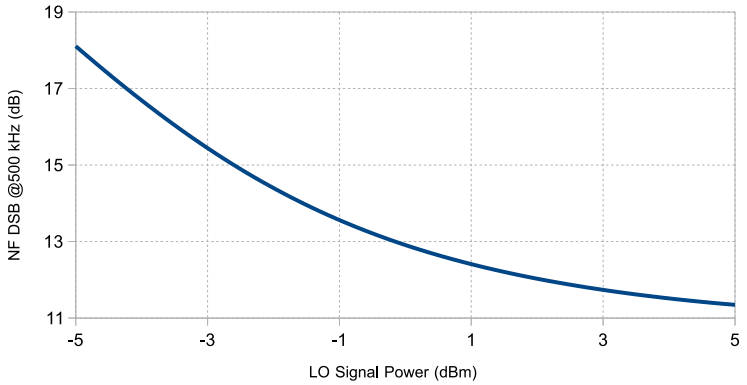


Figure D.17: DSB Noise Figure at 500 kHz vs. LO Signal Power

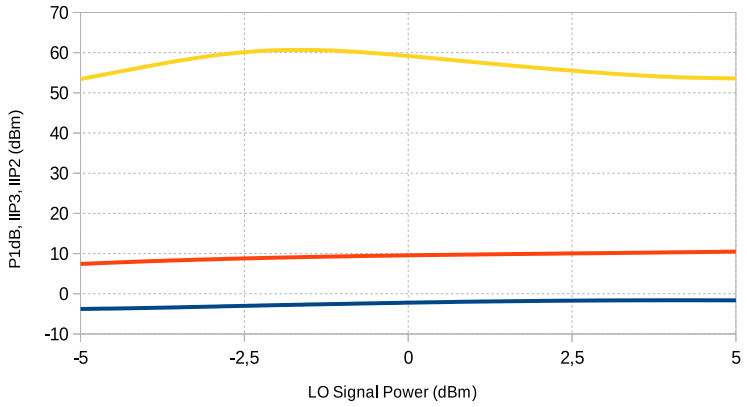


Figure D.18: $IP1dB$, IIP_2 and IIP_3 vs. LO signal power. LO frequency: 1.9995 GHz, RF test tones: 2 GHz, 2.001 GHz, IM_2 frequency: 1 MHz, IM_3 frequency: 2 MHz. (ΔV_T= 5mV and $\frac{\Delta R_L}{R_L}$= 0.5%)

D.4 Simulations Results : Second Topology

As mentioned in subsection 4.3.2.2, the mixer was simulated at 2 GHz input RF, parameters such as : conversion gain, NF, S_{11}, NF, $IP1dB$, IIP_2, IIP_2 and feed-throughs were characterized through corners and Monte Carlo analysis. The simulation results for thi mixer were obtained with a 1.9995 GHz sinusoidal LO signal having a power of 3.5 dBm.

As seen in Fig. D.19, this mixer has a conversion of 13.6 dB for RF input signals located up to 100 MHz away from the LO frequency.

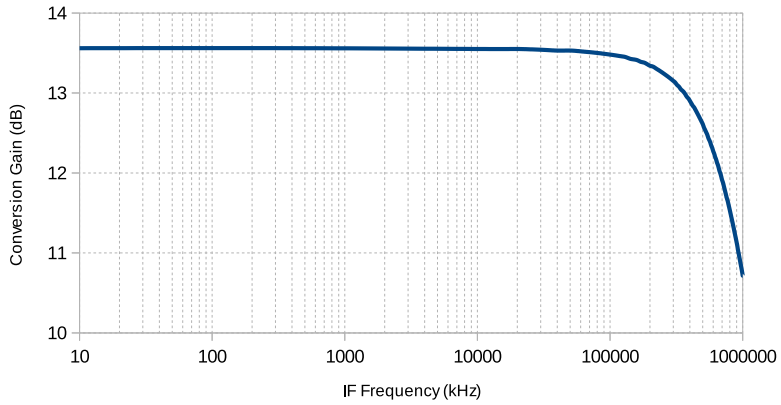


Figure D.19: Conversion Gain vs. IF Frequency

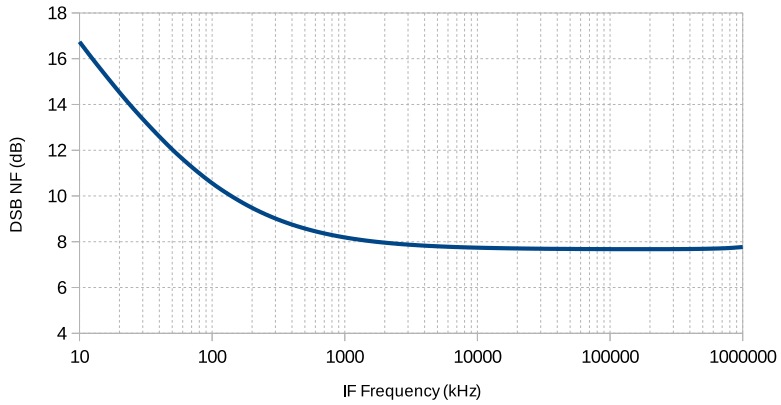


Figure D.20: DSB Noise Figure vs. IF Frequency

Fig. D.20 shows the noise figure (NF), since the designed mixer is going to operate in a low-IF (500 kHz) receiver. The double-sideband (DSB) NF obtained is 8.6 dB. Fig. D.21 shows the input reflection coefficient, S_{11} for the input RF frequency, presenting a good matching for operation up to 3 GHz.

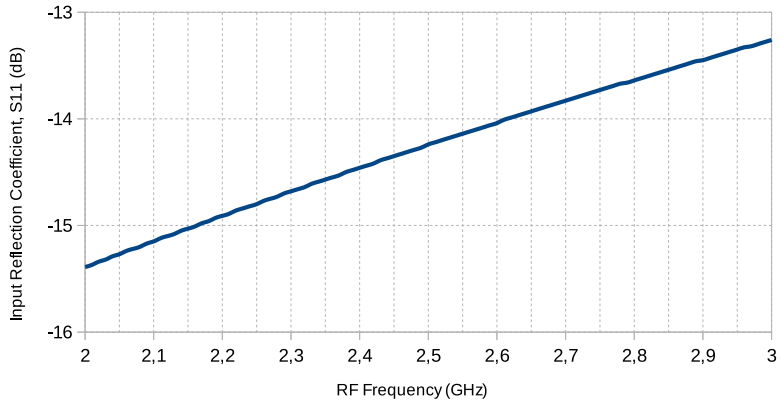


Figure D.21: Input Reflection Coefficient, S_{11} vs. RF Frequency

Linearity characteristics were assessed within a 20 MHz band under consideration that the mixer is intended for broadband wireless target applications. Fig D.22 presents the mixer has a 1 dB compression point of -6.5 dBm, which was determined by sweeping the power of a single 2 GHz RF input tone. The simulated IIP_3 of 0.7 dBm in figure D.23 was obtained with two tones located at 2.0 GHz and 2.001 GHz (0.5 MHz and 1.5 MHz away from the 1.9995 GHz LO frequency). Figure D.24 shows the simulated IIP_2, considering a 0.5% load resistor mismatches ($\frac{\Delta R_L}{R_L}$) and 5 mV of mismatch between switching transistors (ΔV_T) for both simulations.

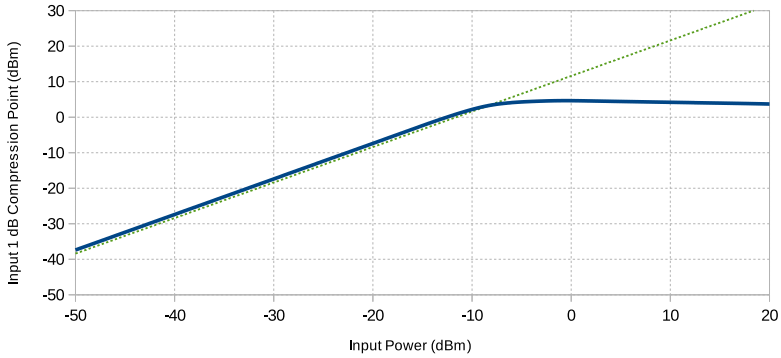


Figure D.22: $P1dB$ vs. Input Power.

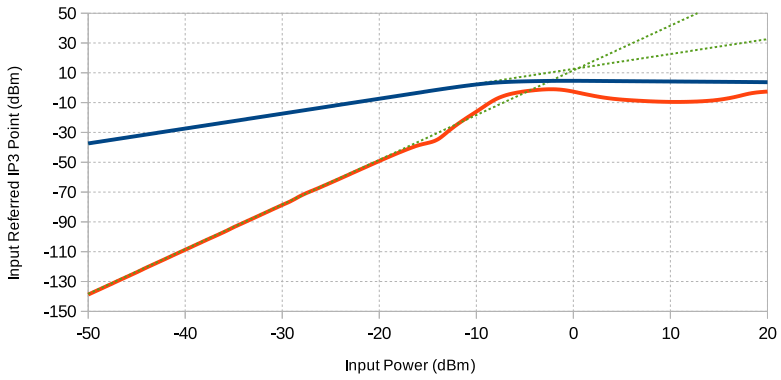


Figure D.23: IIP_3 vs. Input Power. LO frequency: 1.9995 GHz, RF test tones: 2 GHz, 2.001 GHz, IM_3 frequency: 2 MHz

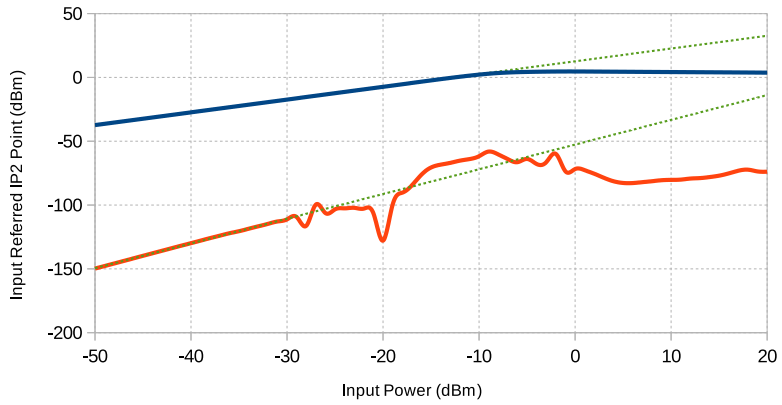


Figure D.24: IIP_2 vs. Input Power. LO frequency: 1.9995 GHz, RF test tones: 2 GHz, 2.001 GHz, IM_2 frequency: 1 MHz. Feedthrough between mixers ports. (ΔV_T= 5mV and $\frac{\Delta R_L}{R_L}$= 0.5%)

Under a nominal voltage supply of 1.2 V with a temperature range of [-55 ~125] °C corner simulations were performed in order to test the robustness of the circuit. Table D.1 presents the corner simulation results. The conversion gain presents minimum value of 8.3 dB and the noise figure a maximum value of 11.4 dB across all corners, and does not deviate to much from the specs. In the other hand we note that the IIP_3 with the exception of four corners presents a minimum value of -4.3 dBm showing that the linearization technique is temperature sensitive (-55 °C) for this topology.

Performance variations in the presence of realistic device mismatches in the mixer were estimated at 2 GHz with Monte Carlo analysis. Table D.2 summarizes the performance variations (mean and standard deviation) for conversion gain, DSB NF, $IP1dB$, IIP_2, IIP_3, and feed-throughs.

Table D.1: Corner Simulation of the Second Topology at 2GHz

		V_{DD} = 1.2V												
		Temperature = -55 °C				Temperature = 27 °C				Temperature = 125 °C				
Specification	Typ	SS	SF	FS	FF	SS	SF	FS	FF	SS	SF	FS	FF	Unit
Conversion Gain	13.6	1.8	8.9	8.3	13.6	10.7	12.7	14.3	15.6	10.4	10.2	12.9	11.7	dB
DSB NF @500 kHz	8.6	11.4	8.2	8.3	6.8	9.5	9	8.2	8.1	11.2	11.1	9.9	9.8	dB
Input Reflection Coefficient, S_{11}	-15.4	-14.9	-14.8	-14.8	-15.1	-15.4	-15.4	-15.5	-15.7	-15.8	-15.8	-15.9	-16	dB
1-dB compression point	-8.6	7	0.1	0.5	-4.9	-5.5	-8.7	-9.3	-11.9	-10.1	-9.8	-12.7	-11.5	dBm
IIP_3	0.7	-13.6	-7.2	-15.7	-11.5	1.1	-0.5	-2.6	-0.3	-0.2	0.6	-4.3	0.1	dBm
IIP_2 (With ΔV_T= 5mV and $\frac{\Delta R_L}{R_L}$= 0.5%)	62.4	41.89	47.6	64.8	40.4	71.4	64.3	62.7	73.75	54.3	62.2	62.2	50.9	dBm

Table D.2: Simulated Specifications at 2 GHz for Second Topology

	Specification*	Unit
RF frequency	2	GHz
IF bandwidth	< 100	MHz
Conversion Gain† 100% Samples	μ=13.5; σ=1.7 > 8.4	dB
$S_{11}{}^\dagger$ 100% Samples	μ=15.7; σ=0.2 < -15	dB
DSB NF @500 kHz† 100% Samples	μ=8.7; σ=0.5 < 10	dB
1-dB compression point† 95% Samples	μ=-6.5; σ=0.7 > -12.4	dBm
IIP_3 † 98% Samples	μ=6; σ=2.8 > -4.3	dBm
IIP_2 (ΔV_T= 5mV and $\frac{\Delta R_L}{R_L}$= 0.5%)	64.4	dBm
IIP_2 † 100% Samples	μ=47.9; σ=9 > 41	dBm
RF-IF isolation† 100% Samples	μ=-44; σ=7.8 < -35	dB
LO-IF isolation† 100% Samples	μ=-45.5; σ=7.8 < -35	dB
LO-RF isolation† 100% Samples	μ=-44.4; σ=7.8 < -35	dB
Power	19.3	mW

* Simulation results; † Process and Mismatch (1000 runs)